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Introductory Invited Paper

CCGA packages for space applications

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Abstract

Commercial-off-the-shelf (COTS) area array packaging technologies in high reliability versions are now being considered for applications, including use in a number of NASA electronic systems being utilized for both the Space Shuttle and Mars Rover missions. Indeed, recently a ceramic package version specifically tailored for high reliability applications was used to provide the processing power required for the Spirit and Opportunity Mars Rovers built by NASA-JPL. Both Rovers successfully completed their 3-months mission requirements and continued exploring the Martian surface for many more moths, providing amazing new information on previous environmental conditions of Mars and strong evidence that water exists on Mars.

Understanding process, reliability, and quality assurance (QA) indicators for reliability are important for low risk insertion of these newly available packages in high reliability applications. In a previous investigation, thermal cycle test results for a non-functional daisy-chained peripheral ceramic column grid array (CCGA) and its plastic ball grid array (PBGA) version, both having 560 I/Os, were gathered and are presented here. Test results included environmental data for three different thermal cycle regimes (−55/125 °C, −55/100 °C, and −50/75 °C). Detailed information on these—especially failure type for assemblies with high and low solder volumes—are presented. The thermal cycle test procedure followed those recommended by IPC-9701 for tin–lead solder joint assemblies. Its revision A covers guideline thermal cycle requirements for Pb-free solder joints. Key points on this specification are also discussed.

In a recent investigation a fully populated CCGA with 717 I/Os was considered for assembly reliability evaluation. The functional package is a field-programmable gate array that has much higher processing power than its previous version. This new package is smaller in dimension, has no interposer, and has a thinner column wrapped with copper for reliability improvement. This paper will also present thermal cycle test results for assemblies of this and its plastic package version with 728 I/Os, both of which were exposed to four different cycle regimes. Two of these cycle profiles are specified by IPC-9701A for tin–lead, namely, −55 to 100 °C and −55 to 125 °C. One is a cycle profile specified by Mil-Std-883, namely, −65/150 °C, generally used for ceramic hybrid packages screening and qualification. The last cycle is in the range of −120 to 85 °C, a representative of electronic systems directly exposed to the Martian environment without use in a thermal control enclosure. Per IPC-9701A, test vehicles were built using daisy chain packages and were continuously monitored and/or manually checked for opens at intervals. The effects of many process and assembly variables—including corner staking commonly used for improving resistance to mechanical loading such as drop and vibration loads—were also considered as part of the test matrix. Optical photomicrographs were taken at various thermal cycle intervals to document damage progress and behavior. Representative samples of these are presented along with cross-sectional photomicrographs at higher magnification taken by scanning electron microscopy (SEM) to determine crack propagation and failure analyses for packages.

1. Introduction

Ball grid arrays (BGAs) and chip scale packages (CSPs) are now widely used for many electronic applications, including portable and telecommunication products. Systems-in-a-package (SiP) development is the most recent response to further ever increasing demand for integration of different functions into one unit to reduce size and cost and improve functionality. The SiP is now included in the iNEMI2005 [1] (International Electronics Manufacturing Initiative) roadmap stating that this technology "has rapidly evolved from specialty technology used in a very narrow set of markets to a broad market base, high volume

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technology that has a wide-ranging impact on the electronics market''. The BGA version has now started to be extensively implemented for high reliability applications with generally more severe thermal and mechanical cycling requirements. The plastic BGA version of the area array package, introduced in the late 1980s and implemented with great caution in the early 1990s, was further evolved in the mid 1990s to the CSP (also known as fine pitch BGA) having a much finer pitch from 0.4 mm to 0.3 mm. Because of these developments, it is becoming even more difficult to distinguish different array packages by size and pitch.

Extensive work has been carried out by the JPL-led Consortia in understanding technology implementation of area array packages for high reliability applications. This work (among other things) included process optimization, assembly reliability characterization, and the use of inspection tools, including X-ray and optical microscopy, for quality control and damage detection due to environmental exposures. Lessons learned by the JPL-led team and others have been continuously published [2–7].

The BGA package with 1.27 mm pitch has been the package of choice for commercial applications. However, recently a ceramic package version specifically tailored for high reliability applications was used to provide processing power required for the Spirit and Opportunity Mars Rovers built by NASA-JPL. Both Rovers successfully completed their 3-months mission requirements and continued exploring the Martian surface for many more moths, providing amazing new information on previous environmental conditions of Mars and strong evidence that water exists on Mars. It is important to note that the field-programmable gate array (FPGA) area array packages were kept in a benign warm electronic box (WEM) environment, and the mission is considered to be relatively short. Electronics in a WEM are heated in order to avoid exposure to the extreme Martian weather that can reach as low as −130 °C. Thermal cycling represents the on–off environmental condition for most electronic products and therefore is a key factor that defines assembly reliability.

Area arrays come in many different package styles. These include the plastic ball grid array (PBGA) with ball composition of eutectic Sn63Pb37 alloy or slight variations such as Sn60Pb40. The ceramic BGA package uses a higher melting ball (Pb90Sn10) with eutectic attachment to the die and board. The column grid array (CGA) or ceramic column grid array (CCGA) is similar to a BGA except that it uses column interconnects instead of balls. The lead-free CCGA uses a copper instead of high melting lead/tin column. The flip chip BGA (FCBGA) is similar to the BGA, except that internally a flip chip die rather than a wire bonded die is used.

Three array configurations are popular. These are (a) full array; (b) staggered array; and (c) peripheral array. Plastic packages come in all styles, whereas ceramic package are generally limited to a full array configuration. Fully populated array packages presents some significant routing challenges if a conventional PWB with plated-through-hole vias (PTHVs) are considered for the design. Peripheral plastic packages have been developed to reduce solder joint failures at the die edge as well as to improve routability characteristics. However, for ceramic packages there is a lesser need for a peripheral array because the CTE mismatch between die and package material is negligible. Hence, most ceramic packages are supplied in full array configuration including the CCGA 717 I/Os used in this investigation. When the ceramic package pad pattern simulates its plastic package version, e.g., the CCGA 560 I/Os, the package might come in the form of a peripheral array.

This paper first presents a summary of key parameters that affect assembly reliability of CBGAs and CCGAs based on a comprehensive literature search. This also includes the effect of tin–lead solder volume on reliability since it is shown that optimum volumes for the ball and column arrays are different. SEM photomicrographs of failures for Sn–Pb and Pb-free for CCGA assemblies after thermal cycling are compared. Guidelines for Pb-free solder joint attachment were given in a recent Revision A of IPC-9701 [8] that includes a recommendation for dwell times with consideration of thermal cycle efficiency and creep. This specification; however, neither includes the background information nor the discussion made during its development. Hence, a brief discussion with some background information on this topic will also be presented. Numerous test vehicles with two CCGA package styles and their counterpart's plastic packages were assembled on printed wiring boards (PWBs) and were subjected to thermal cycling and their failures established. Details on the design and assembly of experimental test vehicles (TVs) is also summarized, including the following: PWB design and solder paste print efficiency using automatic and manual printing, reflow by vapor phase or rework station, corner-staking adhesive and conformal coating will also be summarized. The TVs were subjected to five different thermal cycle regimes including −50 to 75 °C. Representative cycles to failure, failure mechanisms, and cross-sectional photomicrographs for these package assemblies under different thermal cycle regimes are also presented.

1.1. IPC standard for thermal cycle performance requirement for SMT assemblies

An industry-wide guideline document, IPC-SM-785 for accelerated reliability testing of solder attachments, *Guidelines for Accelerated Reliability Testing of Surface Mount Solder Attachments*, has been in existence for more than a decade. Only recently has industry agreed to release an industry-wide specification, IPC-9701, in response to needs for implementation of BGA and CSP technology [8]. Although the IPC-SM-785 guidelines document remains very valuable and is still valid in terms of providing fundamental understanding, it sets no testing requirements and performance standards. As has been well established by industry and the JPL Consortia [1–5], many variables could

be manipulated to either favor or disfavor environmental test results. In addition, a novice user/supplier may waste considerable resources and time to generate failure data not related to solder attachment. An example of mishap is the use of a surface finish having the potential of inducing interfacial rather than solder joint failure.

The IPC-9701 specification addresses how thermal expansion mismatch between the package and the PWB affects solder joint reliability. In order to compare solder joint reliability for different package technologies, numerous materials and process parameters were specified, including the following:

- Specifies 0.093 in. for the PWB (e.g., FR-4) thickness in order to minimize bending and to achieve conservative values on cycles-to-failure data.
- Limits surface finish choices to OSP (organic solder preservative) and HASL (hot air solder level) in order to eliminate the potential of interfacial failure.
- Limits pad configuration to NSMD (non-solder mask defined or Cu defined) in order to eliminate failure due to stress risers.
- Defines PWB-pad size to be 80–100% of the package-pad size in order to have a more realistic failure.

The newest revision, IPC-9701A, has been updated to include guidelines for Pb-free solder alloys. Appendix B of this specification provides guidelines for modifications for Pb-free solder joints. Currently, there are only limited data and insight to determine acceleration factors and acceleration models for Pb-free [9–12]. Data on the impact of various thermal cycle profiles on the results of accelerated testing in comparison to eutectic tin–lead solder are still being gathered by industry.

Acceleration thermal cycle test results—especially when are compared to lead-free solder alloys—are sometimes inaccurately assumed to be the same as product reliability. Correlations between acceleration testing and product reliability for Sn–Pb have been more or less established during many years of investigation and product use. For the lesser understood Pb-free solder attachments, such correlations remain to be better established. Reliability is the ability of a product, here surface mount solder attachments, to function under given conditions and for a specified period without exceeding acceptable failure levels. Therefore, the supposition that Pb-free solder joints are either more or less reliable than standard Sn–Pb solder joints is based only on unsubstantiated laboratory test results Such general statements are incomplete when either the Pb-free alloy composition or when product information and use conditions are not specified. It must be emphasized that product reliability needs to be estimated for solder joints under relevant use conditions.

Modifying IPC-9701 to include the requirements for Pb-free solder attachment was assumed to be an easy task at the start of the effort since abundant information on thermal cycling for Sn–Pb was already well established. However, it soon became apparent that even a trend cannot be established for accelerated thermal cycling data for Pb-free solder joints. The literature data are summarized by this author and plotted in Fig. 1 as relative cycles to failure for Pb-free compared to Sn–Pb on the y-axis and thermal cycle conditions on the x-axis. Here Pb-free means that a SAC alloy, that is, an alloy of tin–silver–copper (SnAgCu, hence SAC) was used. Relative cycles to failures may be better (>1) or worse (<1) than Sn–Pb depending on package type, thermal cycle range, cycle profile, and dwell times at the maximum temperatures. For example, cycles to failures for Pb-free PBGA 256 I/Os (plastic ball grid array) assemblies are about twice and those for LCCCs (leadless ceramic chip carrier) are about half of those for Sn–Pb components/assemblies respectively when subjected to accelerated thermal cycling in the range of −40 to 125 °C. Temperature range and dwell time also affect relative accelerated failure cycles as is apparent from the test data generated for CBGA 625 I/Os from 0 to 100 °C and −40 to 125 °C.

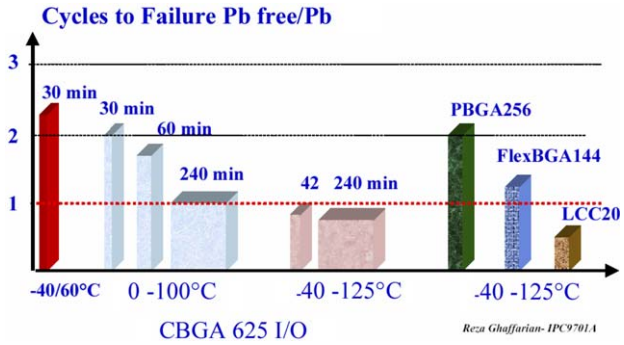

Fig. 1. Cycles to failure for SAC (SnAgCu) solder attachments dependence on thermal cycle range and state of stress/strain (data drawn from different sources including [12]). Here when the ratio on the y-axis is larger than 1, it means lead-free solder lasted longer than tin–lead solder joints. The 30, 60, and 240 min represent increase in dwell time in minute at the maximum temperature.

Various authors have attempted to theoretically explain the apparent contradiction of accelerated test results. Projections can be made by using creep hysteresis loops (energy) as the baseline for modeling. The effect of dwell time depends on the temperature range and the maximum temperature. As predicted by modeling, such effects can be either low to high. Dr. Jean-Paul Clech has shown theoretically in Ref. [11] that the most efficient dwell times at 100 °C (0–100 °C cycle) are 10 min for tin–silver–copper (SAC) and 3–4 min for Sn–Pb solder joints, respectively. Based on very limited test data and contrary to conventional understanding, he also postulates that thermal cycling at higher mean temperatures may show improved cycles to failures when compared to a lower mean temperature.

Extensive discussions were made among the IPC-9701 committee team members as how best to capture the apparent conflicting accelerated test data and generate

suitable requirements from them. Initially, a large number of figures representative of such conflicting test results were included in the Appendix B of IPC-9701A to show different team members' points of view for specifying the dwell time requirements. However, based on comments received after its wider distribution to industry, these figures were removed from this specification. Later, they were published by this author at the APEX 2006 conference sponsored by the IPC. In addition, the Appendix B title of IPC-9701A was changed to "*guideline*" rather than "requirement" since no industry-wide agreement could be reached on even the definition of a thermal cycle profile. Based on numerous discussions within the last two years, two thermal cycle profiles were recommended for (SAC) solder attachments depending on the reliability approach and use conditions. These are:

- Condition D10 (10 min dwell) requiring 10-min dwells at both the hot and cold temperature extremes. This is possibly the most efficient accelerated thermal cycle profile since it induces the most strain energy per unit of time (considering the entire cycle) or per unit dwell time. Cycles-to-failure data generated under this condition should generally be used as stand-alone only and only when damage accumulation is understood by modeling. The test results could be used for comparison to those of lead-based solder assemblies to show theoretically whether their performance is better or worse.
- Condition D30^{+} (30 min or higher dwell) requiring dwells of 30 min and higher (60 min) at the hot and cold temperature extremes in order experimentally to induce creep damage some what comparable to lead-based solder. Modeling in conjunction with experimental data at different dwell times may be required to better define such a comparison.

An OSP surface is recommended for the Pb-free base solder alloys even though the final version of the specification includes immersion silver (IAg) based on additional inputs by industry. For Sn–Pb, the acceptable surface finish was HASL. HASL is not allowed since it is not compatible with Pb-free solder interconnections. Other surface finishes can be used for the manufacturer's internal data comparison. Electroless nickel/immersion gold (ENIG) surface finish also can be used for internal data comparison; however, there is a risk of introducing unintended immature failure as documented by industry. In this specification, the thermal cycle (TC) test ranges, test profile, and the number of test cycles (NTC) reported were also standardized. These include the reference cycle in the range from 0 to 100 °C (TC1) and the severe military cycle condition from −55 to 125 °C (TC4). Three out of five total TC conditions are identical to the test conditions recommended by JEDEC 22 Method A104, Revision A. The NTCs varied from a minimum value of 200 cycles to a reference value of 6000 cycles.

1.2. Tin–lead and Pb-free solders with ceramic column grid arrays

Fig. 2 shows SEM photomicrographs and cross-sections of the 560 I/Os CCGA assemblies after cracking due to thermal cycling. Fig. 3 shows the microstructure of another CCGA package assembled with Pb-free (Sn/Ag/Cu) solder [13]. For CCGA assemblies, the 3D optical microscopy and visual inspection are limited to inspection of the outer rows. Such inspection can be performed only when sufficient gaps are allowed between the assembled parts. Note that the assemblies show signs of damage/cracking after thermal cycling.

1.3. Literature survey on CBGA/CCGA assembly reliability

Table 1 lists cycles to failure for a number of CCGAs/CBGAs having different configurations, selected from the very limited data set reported in the literature [14–20]. Data were chosen to illustrate the effects of a few key parameters

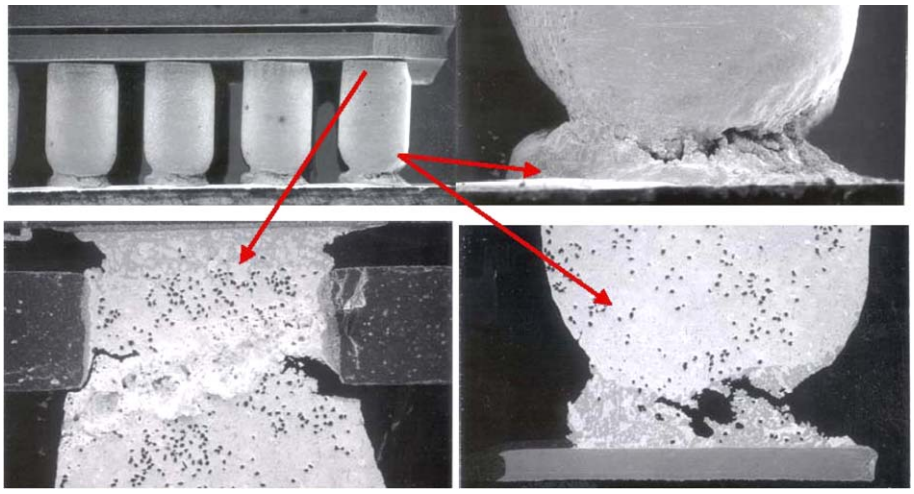

Fig. 2. SEM photomicrographs and cross-sections of CCGA 560 I/Os assembled with tin–lead solder after thermal cycling showing damage/cracks.

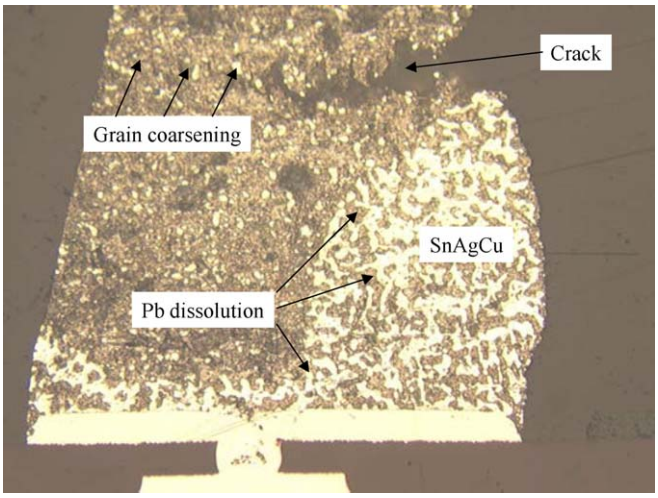

Fig. 3. 1657 I/Os CCGA high-lead solder column on a microvia pad PWB with Sn–Ag–Cu solder joints (courtesy of Dr. D. Shangguan/T. Castello).

on the reliability. The following parameters were considered when test data were tabulated even though in some cases specific information was not reported and in fact was missing.

- *Thermal cycle range, ramp rate, dwell times:* For example, the CT50%F (cycles-to-fifty percent-failure) for the CBGA 361 over the range of 0/100 °C was 4535 cycles (Case #2); it diminished to 1190 cycles when the temperature range was broadened to −55/110 °C (Case #6).
- *Package size, thickness, materials, configuration, and I/Os:* Comparing Case #2 to Case #3, a relatively large reduction in CT50%F is shown when the package thickness is increased from 0.8 mm to 1.2 mm (4535 vs 2700 cycles). When the package thickness is further increased to 2.9 mm, the CT50%F is further reduced, a reduction by 3.2 times relative to the package with 0.8 mm thickness. A similar reduction was observed for the CCGA 1657 I/Os when the package thickness is increased from 1.5 mm to 3.7 mm (Case #13). The reliability decreases by increasing the package I/O since the distance to neutral point is increased. The CT50%F is reduced from 4535 cycles to 2462 cycles when the I/Os for the 0.8 mm thick package increased from 361 to 625 (Case #2 vs Case #5). The use of higher CTE ceramic materials—to better match the ceramic CTE to the PWB—also improves the reliability. For example, compare Case #6 to the Case #7 for the 361 I/O CBGA assemblies. The CT50%F increased from 1190 to 2160 cycles for the HiCTE package.
- *Die size and its relation to the package size and ball configuration:* The effects of die size and package configuration (full vs peripheral) arrays on reliability are more pronounced for plastic than for ceramic package assemblies.
- *PWB thickness, pad definition, surface finish:* The preferred thickness was defined as 2.3 mm in IPC-9701(7) since generally plastic packages assembled on thinner PWBs show higher cycles to failure. The effect of board thickness for ceramic packages is not well established, but its effect may be less critical for column grid array assemblies than for plastic package assemblies, especially when the dominant failure is the columns rather than solder joints.

Single side or double side, relative offset of package on top and bottom

Previously, an example was give for reduction in life cycle due to double-sided mirror image assemblies. The effect of mirror image assemblies on reliability for CBGAs/CCGAs is not presently known.

1.4. Effect of solder joint volume on CCGA assembly reliability

In contrast to PBGA assemblies, CCGAs/CBGAs assembly reliability is significantly affected by the amount of solder volume. In fact, solder volume is the most important key process variable affecting the reliability of CCGAs/CBGAs. Recommended minimum, optimum and maximum solder-paste volumes for both CBGA and CCGAs are shown in Table 2 [21,22]. The effect of solder volume for CBGAs is intuitive since higher solder volume increases the solder balls' stand-off height, but this is not the case for the CCGA assemblies where column flexibility also plays a role in reliability.

For CBGAs, it has been shown that increasing solder-paste volume increases reliability, but only up to a point. When the paste volume passes 10,000 mil^3 (0.16 mm^3), the reliability no longer increases because the solder paste has filled the area between the ball and the card. Additional solder paste moves up the ball toward the module, making the ball look like a column. When the fillet dimension at the card surface is maximized, so is the reliability.

This trend may not be true for at least one type of CCGA package, the one with 1.27 mm pitch. Unlike the CBGA product, high solder-paste volume can actually start to decrease the interconnection reliability. As the volume increases, so does the fillet height on the column. This increased fillet height reduces the effective length of the flexible column, thus making it stiffer. This effect—while true for both cast and wire—is more pronounced for the cast because it is stiffer in nature due to its larger diameter [16]. In a comprehensive investigation performed for this category of packages, it has been shown that assemblies with a minimum acceptable solder paste showed slightly higher reliability than those with nominal and much better than those with higher solder volume. To avoid inducing opens however, the use of nominal rather than minimum solder-paste volume is recommended.

2. Objectives

The purpose of this investigation was to characterize the reliability of area array packages with 560, 717, and 728

Table 1
Cycles-to-failure data illustrating the effect of a number of key variables

Case number	Package I/O-pitch	Pkg size (die size) mm	Thermal cycle condition (ramp, dwell, cycle/h)	First failure	Mean life ($N_{63.2\%}$)	Comments
1	CBGA-255-1.27	21 × 21 (1 mm substrate)	0–100 °C (10, 5, 2 cycles/h)	1980 (1% failure)	2426 ($N_{50\%}$)	PWB, 0.55 mm Thk Ref. Burrnette [17]
2	CBGA-361-1.27	25 × 25 (substrate 0.8 mm Thk)	0–100 °C (3 cycles/h)	NA	4535 ($N_{50\%}$)	Avg solder paste vol 5900 mil^3 PWB, 1.57 mm Thk die 15 × 10 mm
3	CBGA-361-1.27	25 × 25 (substrate 1.2 mm Thk)	0–100 °C (3 cycles/h)	NA	2700 ($N_{50\%}$)	Note: Increase from die Thk .8 to 1.2 and 2.9, reliability reduction by 1.8 and 3.2 times
5	CBGA-625-1.27	32.5 × 32.5 (substrate 0.8 mm Thk)	0–100 °C (3 cycles/h)	NA	2462 ($N_{50\%}$)	PWB, 1.57 mm Thk Ref. [18]
6	CBGA-361-1.27	25 × 25 (substrate 0.8 mm Thk)	−55 to 110 °C (2 cycles/h)	890 (100 ppm)	1190 ($N_{50\%}$)	PWB, 1.57 mm Thk Ref. [15]
7	CBGA-361-1.27-HiCTE substrate	25 × 25 (substrate 0.8 mm Thk)	−55 to 110 °C (2 cycles/h)	1310 (100 ppm)	2160 ($N_{50\%}$)	Substrate CTE, 12.2 ppm Ref. [15]
8	CGA–361-1.27-Interposer	25 × 25 (substrate 0.8 mm Thk)	−55 to 110 °C (2 cycles/h)	1350 (100 ppm)	2320 ($N_{50\%}$)	NTK Interposer CGA PWB, 1.57 Ref. [15]
9	CGA-361-1.27-IBM	25 × 25 (substrate 0.8 mm Thk)	−55 to 110 °C (2 cycles/h)	1080 (100 ppm)	1520 ($N_{50\%}$)	Ref. [15]
10	CBGA-1681-1.27-HiTCE	42.5 × 42.5 × 1.85 (substrate)	−25 to 125 °C (1, 9 min, 3 cycles/h)	613 (first failure)	1142 ($N_{50\%}$)	PWB, 93 mm Thk Ref. [19]
11	CBGA-625-1.0	32 × 32 × 2.4 mm (substrate)	0–100 °C (2 cycles/h)	NA	740 ($N_{50\%}$)	Ref. [16] IBM-2003
12	CBGA-937-1.0	32 × 32 × 1.5 (substrate) 32 × 32 × 2.4	0–100 °C (2 cycles/h)	NA	1860 ($N_{50\%}$) 1310 ($N_{50\%}$)	Ref. [16]
13	CCGA-1657-1.0	42 × 42 × 1.5 42 × 42 × 2.55 42 × 42 × 3.7	0–100 °C (2 cycles/h)	NA	1530 ($N_{50\%}$) 990 ($N_{50\%}$) 620 ($N_{50\%}$)	Ref. [16]
14	CCGA 1657-1.0 Cu	42.5 × 42.5 × 2.55	0–100 °C (2 cycles/h)	1660 (first failure)	2410 ($N_{50\%}$)	Cu Column, solder paste 96.5Sn3.5Ag Ref. [20]

Table 2
Solder paste recommendation for CBGA and CCGA, 1.27 mm pitch

Component type	Minimum paste volume mil^3 (mm^3)	Optimal paste volume mil^3 (mm^3)	Maximum paste volume mil^3 (mm^3)
CBGA	4800 (0.089)	6500–7500 (0.10–0.20)	10000 (0.160)
CCGA	3000 (0.0470)	5000–5600 (0.078–0.088)	7600 (0.120)

I/Os. It presents the results of the 560 I/O second level package assemblies, the effect of corner staking, and thermal cycle range on the failure of CCGAs and their plastic BGA counterparts with the identical peripheral package configuration. An additional discussion of first failure for low and high solder volumes is also presented.

The new area array packages used in this investigation are fully populated with 728 I/Os in the plastic configuration and 717 I/Os in the ceramic column grid array (CCGA) package (see Fig. 4). They are new versions of the field-programmable gate array package having higher processing power and are smaller in dimension and of less weight. For the CCGA 717, the three-corner solder columns from each package corner have been removed by the package manufacturer to improve reliability (Fig. 5). Comparing this figure to Fig. 1 for the CCGA 560 I/O package, it is evident that the columns for the CCGA 717 I/Os are thinner and present different features. For this reason, assembly processing parameters are different from the 560 I/O package and need to be optimized prior to establishing their second level solder joint reliability.

A design of experiment (DOE) was utilized to cover processing as well as other aspects that are considered to be unique for the potential use of these packages for high reliability applications. Solder joint reliability is affected by many variables including solder volume. The following parameters were either characterized or evaluated as part of the DOE implementation:

- Designed two pad sizes, one for the CCGA 560 I/Os and smaller pads for the PBGA attachment. PBGAs were assembled on both pad sizes to evaluate PBGA interchangeability with the CCGA.

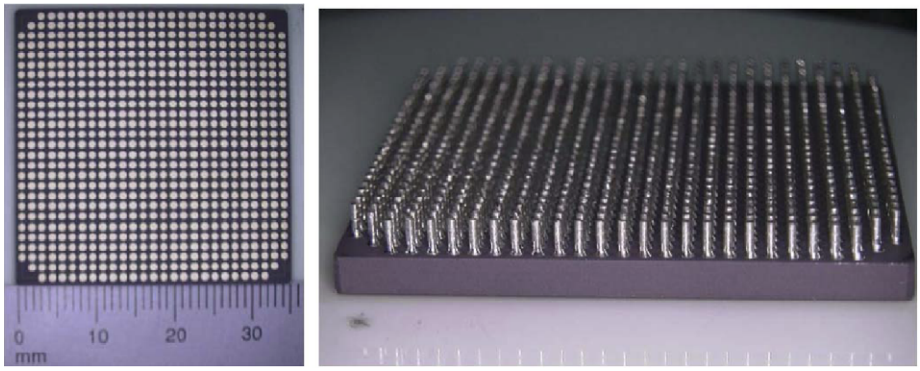

Fig. 4. Photomicrograph of a CCGA 717 I/O package showing its dimensions and its column feature having no corner columns for reliability improvement.

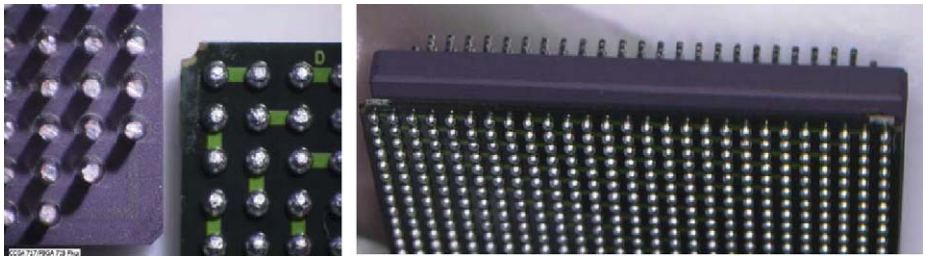

Fig. 5. Photomicrograph of a CCGA 717 I/O package contrasted with its plastic counterparts with its corner balls removed to assemble the PBGA package on the CCGA PWB pad design.

- Assembled CCGA 717 I/Os and 728 I/Os on one pad considered to be acceptable for the CCGA 717 I/Os. PBGA corner balls were removed in the PBGA 728 assembly to utilize the 717 I/O pad pattern (see Fig. 4).
- Utilized four different stencil thicknesses, 6, 7, 8, and 10.5 mils., A relatively thicker mini-stencil (for paste deposition of only one package) of 10.5 mil thick especially designed for the CCGA 560, an 8 mil thick stencil designed for the CCGA 717 I/Os, and a standard 6 mil thick stencil to assemble PBGAs and other surface mount packages. Solder paste print volumes varied significantly depending on package types, stencil design, and paste printing process.
- Included CCGA and PBGA assemblies with an added corner-staking adhesive and conformal coating. Corner-staking adhesive bonds are generally used to enhance the resistance to mechanical shock and vibration loads and the function of the conformal coating is to protect solder joints from contamination, including shorts due to conductive particulates.
- Assembled packages in a vapor phase reflow machine or individually assembled using a rework station to establish differences in reliability between the two techniques. A rework station is an option for assembly in a high reliability manufacturing environment when only a few systems are being built. Obviously, it is not an option for high volume manufacturing.

The assemblies were subjected to five types of thermal cycles. Both the process and reliability results for the CCGA package assemblies are discussed below and compared to their PBGA counterparts.

2.1. Test vehicles

For the CCGA/PBGA 560 I/Os, a polyimide PWB was designed to accommodate two pad configurations, one configuration for the PBGAs and the other for the CCGAs. The pad sizes for the PBGA and CCGA were 24 and 33 mils, respectively. These pads were connected by traces to their 24 mil diameter plated-through-hole vias (PTHVs). Specific pairs of PWB pads were designed so that their connections within a package pad pair after assembly completed a specific daisy chain pattern. Four key daisy chains for each package were used for continuous monitoring during thermal cycling. Four additional pads were added at each side of the package for manual probing and failure identification. For the CCGA 717 I/Os and PBGA 728 I/Os, a high temperature FR-4 PWB with 0.091 in. thickness as specified by IPC-9701A with 32 mil pads connected to PTHVs was used. Fig. 6 shows an assembled test vehicle having both CCGA 717 I/O and PBGA 728 I/O packages. Note the input and output traces extending to the board edge and also the probing pads at the package peripheral for manually detecting failures.

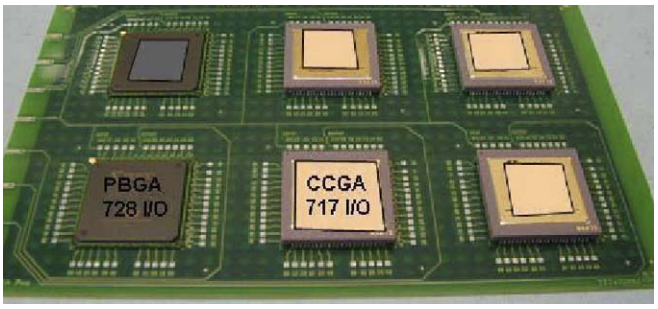

Fig. 6. PWB design showing CCGA and PBGA packages, probing pads, and via daisy chains.

HASL and OSP surface finishes are specified in IPC-9701A as the recommended surface finishes for solder attachment reliability evaluation of tin–lead solder alloy. The PWB pads had HASL surface finish to avoid potential immature intermetallic failures such as those occasionally observed for the Au/Ni surface finish. Currently, only OSP and IAg surface finishes are recommended for Pb-free solder alloys.

2.2. Stencil design, paste print, and volume measurement

Table 3 lists estimated solder-paste volumes achievable with different stencil thicknesses and aperture openings. The 6 and 7 mil stencil thicknesses represent the general stencil that could be used for paste application on PBGA and CCGA pad patterns, respectively. The mini-stencil with 8 and 10.5 mil thicknesses were used only for the manual paste print application for CCGA in order to achieve the higher paste volume recommended by the package supplier. In one case, a step down stencil design, from 8 mil to 6 mil thickness, was used to accommodate quality assembly of both the CCGA and the other finer pitch standard surface mount packages. For this case, numerous conventional packages in the vicinity of a CCGA had to be hand soldered since they were masked during automatic paste printing. The CCGAs were assembled in two facilities, each facility using its approved RMA paste and assembly process procedures.

Table 3
Stencil parameters and solder volumes

Stencil parameters	Solder volume (mil^3)	Stencil type
BGA 560 I/O-Aperture 23 mil-dia stencil 7 mil	2909	Stencil
CCGA 560 I/O-Aperture 32 mil-dia stencil 7 mil	5632	Stencil
CCGA 560 I/O-Aperture 32 mil-dia stencil 8 mil	6430	Stencil
CCGA 560 I/O-Aperture 32 mil-dia stencil 10.5 mil	8440	Mini-stencil
PBGA 728 I/O-Aperture 6 mil-dia stencil 28 mil	4823	Mini-stencil
CCGA 717 I/O-Aperture 32 mil-dia stencil 8 mil	6430	Mini-stencil

Two RMA pastes at two facilities, Type III (−325 + 500) mesh, were used for paste printing using automatic and normal manufacturing parameters. Manual paste printing was performed when the mini-stencil was used. After printing each paste print on the PWB was visually inspected for gross defects such as bridging or insufficient paste. Paste print quality was improved by adding a small amount of paste when insufficient paste was detected. When bridging was discovered, solder paste was removed to open the bridge. Special attention was given during inspection of the corner pads. Solder paste heights were measured using two different laser profilometers and an optical microscope with 3D dimensional measurement capability. Measurements were made at numerous locations—including corner and peripheral center pads—to gather solder volume data and their corresponding distributions.

An example of laser measurement for the top left corner and solder paste distribution values is shown in Fig. 7. The specific tool provides automatic control for measurement and has an undesirable maximum level cut-off value feature, making it very difficult to expand the theoretical measurement by software to include the volume under the peak values. This limitation of software led on many occasion to wrong readings for often observed an abrupt paste print. Eventually, the paste print height had to be verified by using filler gages and the uniformity of print verified by inspection using an optical microscope. On the other hand, the 3D optical microscope could reveal the distribution covering for a larger area, but it lacked accuracy (see Fig. 8).

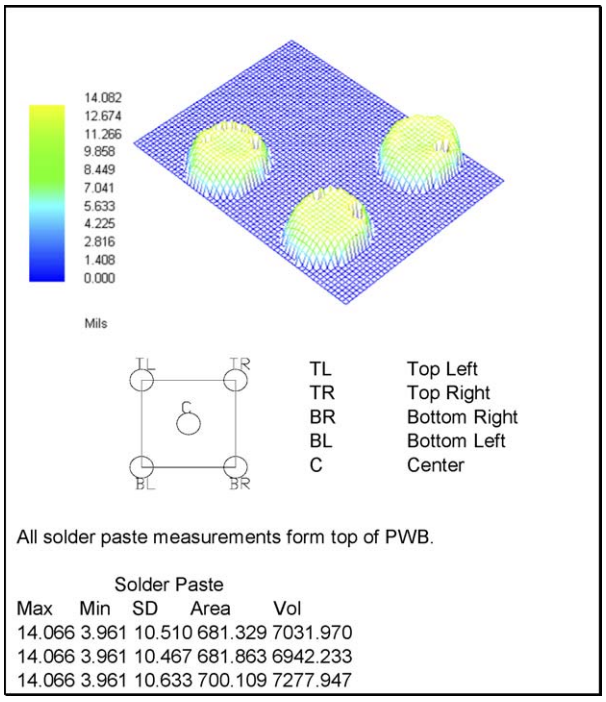

Fig. 7. Solder paste distribution using a laser profilometer showing the calculated paste volume.

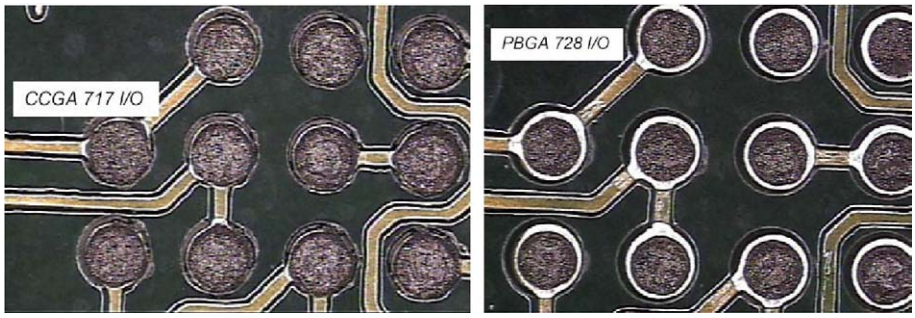

Fig. 8. Solder paste deposition for CCGA 717 and PBGA 728 using the pad design for CCGA 717 I/O—higher solder paste volume required for CCGA package assembly to achieve optimum reliability.

3. Test results

3.1. Inspection before environmental tests

For high reliability electronic applications, visual inspection is traditionally performed by Quality Assurance personnel at various levels of the packaging and assembly, known as mandatory inspection points (MIPs). Solder joints are inspected and accepted or rejected based on specific sets of criteria. Further assurance is gained by subsequent short-time environmental exposure, by thermal cycling, vibration, and mechanical shock, and so forth. These screening tests also allow detection of anomalies due to workmanship defects or design flaws at the system level. For space applications, generally 100% visual inspection is performed for the hybrid package presealing (precap) and after assembly prior to shipment.

Visual inspection is only somewhat useful for the area array packages since obviously it is of no value for hidden balls and columns under the package. X-ray inspection is needed for area array packages. However, in the case of CCGAs, the hidden solder joints could not be distinguished because of the heavy ceramic lid that inhibited X-ray penetration [6]. Visual inspection can often be used in examining CBGA and CCGA assemblies since generally the solder fails at the exposed corners or periphery ball attachments. Peripheral balls and columns were inspected visually using an optical microscope at the start and during thermal cycling to document damage progress. Fig. 9 shows photomicrographs of solder joints of CCGA 717 assemblies prior to thermal cycling. Note the good solder joints with smooth surfaces adjacent to a joint with ridged solder. Minor modification in reflow did not remove this unevenness.

3.2. Thermal cycle test profile

Five different thermal cycle profiles were used with the following thermal profiles. These are:

(1) *Cycle A:* Ranges from −50 to 75 °C with a 2 to 5 °C/min heating/cooling rate. Dwells at extreme temperatures are at east 10 min with a duration of 105 min for each cycle.
(2) *Cycle B:* Ranges from −55 to 100 °C with a 2 to 5 °C/min heating/cooling rate. Dwells at extreme temperatures are 15 min.
(3) *Cycle C:* Ranges from −55 to 125 °C with a 2 to 5 °C/min heating/cooling rate. Dwells at extreme temperatures are at east 10 min with a duration of 159 min for each cycle.
(4) *Cycle D:* Ranges from −65 to 150 °C with about a 10 °C/min heating/cooling rate. Dwells at extreme temperatures are at least 10 min with a duration of about one hour for each cycle.
(5) *Cycle E:* Ranges from −120 to 85 °C with about 5 °C/min heating/cooling rate and 10 min dwells.

The criteria for an open solder joint specified in IPC-9701A were used as guidelines to interpret electrical interruptions. Generally, once the first interruption was observed, many additional interruptions within 10% of

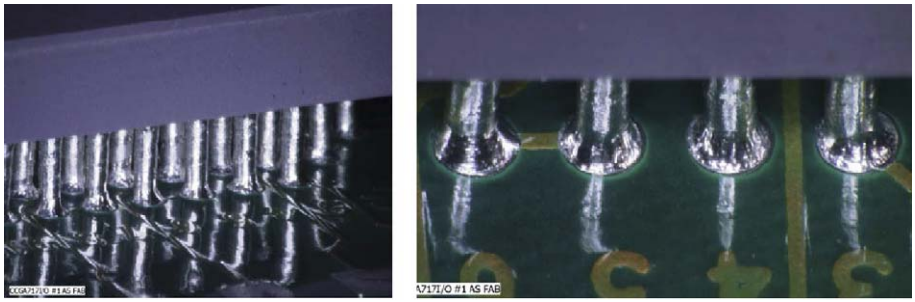

Fig. 9. Optical photomicrographs of a PBGA and a CCGA after assembly but prior to thermal cycling.

the cycle life also occurred. This was especially true for the ceramic packages. Opens were manually verified after removal from the chamber at the earliest convenient time.

3.3. Test results after thermal cycling

3.3.1. CCGA 560 I/O failure characterizations by optical microscopy

3.3.1.1. Effect of solder volume. Fig. 10 shows optical photomicrographs of both PBGA and CCGA 560 I/O assemblies after 991 Cycle A (−50/75 °C) thermal cycles. Even though no outright failures were observed, the CCGA solder joints showed some signs of damage. This is not significant if only solder interconnects to the board is considered. Fig. 11 shows the first failure occurrence for an assembly with high solder volume detected by continuous monitoring at 1075 cycles and removed at 1138 cycles for inspection and failure verification. It is interesting to note that failure did not occur at the board site, a more common failure location; rather, it occurred at the package site. Hence, solder joint damage at the board interface may not always be used as a representative of damage progress. In addition, solder joint failure is not at the corner columns as generally expected to occur for ceramic area array package assemblies. Solder joint damage conditions for assemblies with low and high solder volume are shown in Fig. 12 showing significant damage at the board site for the low solder volume condition. Failures were in solder joints at the board site for the assembly with low solder volume as shown in Fig. 13 taken at 1459 thermal cycles. Note that the corner columns at the board site are tilted more toward the center of the package due to the higher CTE mismatch compared to the interface at the package site.

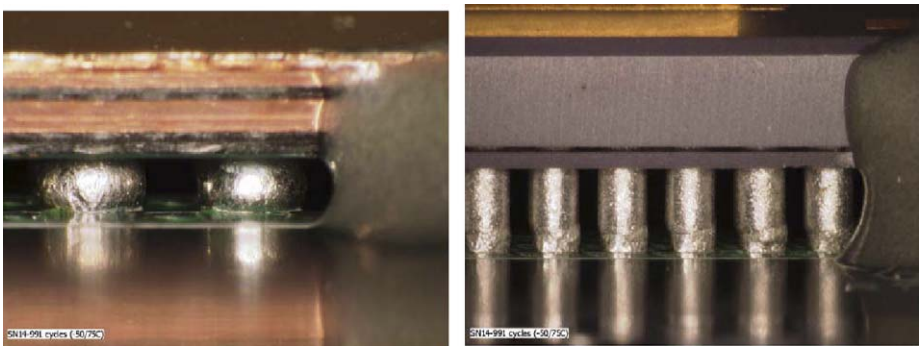

Fig. 10. Optical photomicrographs of PBGA (left) and CCGA built with a 10.5 mil thick stencil after 991 cycles Cycle A (−50/75 °C)—corner staking adhesives apparent at the two corners.

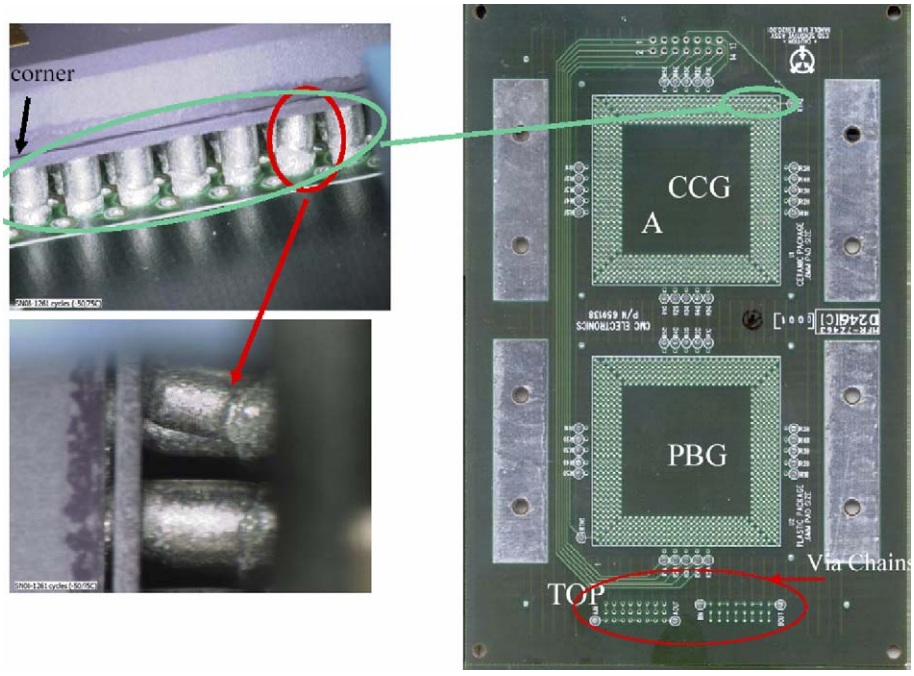

Fig. 11. Optical photomicrographs of CCGA built with a 10.5 mil thick stencil after 1138 cycles Cycle A (−50/75 °C)—cracking from the package site rather than the board site commonly occurring.

3.3.1.2. Corner-staking adhesive and failure mechanism change. Fig. 14 compares optical and SEM photomicrograph of a PBGA balls after exposure to 1819 cycles Cycle A (−50/75 °C) and another one subjected to 588 cycles in the range of −55/125 °C (Cycle C condition). Both assemblies had corner staking. No significant microstructural changes for the Cycle A condition was found, whereas a small microcrack was initiated in the solder joint at the package interface for the Cycle C condition (−55/125 °C). The latter photograph also clearly shows the grain growth due to exposure at elevated temperature. Similar optical photomicrographs for CCGA assemblies with corner staking after the same number of cycles and conditions: 1819 (−50/75 °C) and 588 (−55/125 °C) are shown in Fig. 15. Although both assemblies had identical build condition with identical corner staking materials, the failure mechanisms were different and dependent on the temperature cycle range and the maximum temperature. One failed away from staking whereas the other (−55/125 °C) failed within the staking adhesive at the interposer solder interconnection interfaces.

3.3.2. CCGA 717 I/O failure characterizations by optical microscopy

Fig. 16 shows optical and SEM photomicrographs of two CCGA 717 I/O assemblies at 200 and 500 thermal cycles Cycle B condition (−55/100 °C). The solder joints show signs of minor damage. Optical photomicrographs for a CCGA package assembly with and without corner-staking adhesive after 950 thermal cycles are shown in Fig. 17. At this high number of cycles, damage has not yet significantly increased. It is more severe for the one with

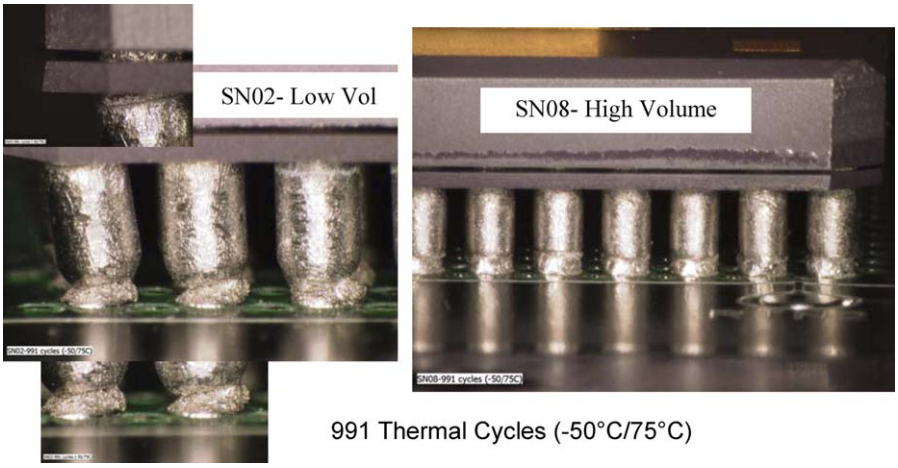

Fig. 12. Optical photomicrographs of CCGA assemblies built with an 8 mil (left) and 10.5 mil thick stencil after 991 cycles Cycle A (−50/75 °C).

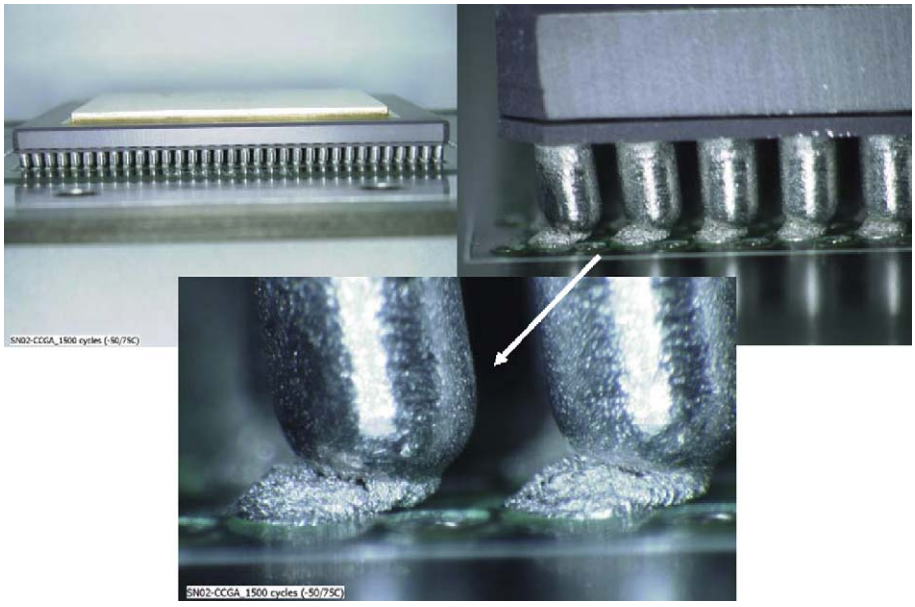

Fig. 13. Optical photomicrographs of CCGA built with an 8 mil thick stencil after 1459 cycles Cycle A (−50/75 °C)—cracks in solder joints at the board site and shift of the corner columns towards the package center.

corner staking. SEM photomicrographs for different columns after 950 cycles are shown in Fig. 18. No failures were yet detected by electrical monitoring, but signs of damage at the board and package sites are apparent. Fig. 19 shows an optical photomicrograph of CCGA assemblies with and without corner staking and conformal coat after 340 extreme thermal cycles in the range of −120/85 °C (Cycle E). Both show signs of damage, but the damage is more pronounced for the one with corner staking and conformal coat. The columns appear to have been squeezed out at the copper wrap strips, possibly due to continuous exerted pressure by stiffened staking and conformal coating polymeric materials due to exposure to the very low temperature during thermal cycling. Generally, polymeric materials become more rigid as temperature decreases; therefore, they induce more stress due to CTE mismatches during thermal cycling.

Fig. 20 compares the effect of a severe thermal cycle exposure on a NSMD pad design with good solder fillet and a SMD design with poor fillet. This figure shows optical and SEM photomicrographs at 400 thermal cycles in the range of −65 to 150 °C (Cycle D condition). The solder joints with the NSMD pad design show signs of severe damage and minor cracking, whereas those with the SMD pad designs are near failure with severe cracking at several column attachments. Even though such failures are well known for ball grid arrays, this is the first time that the effect of SMD pad design on promoting cracking has been seen for a column grid array assembly.

3.3.2.1. Projection of cycles to failure to 0–100 °C for CCGA 560 and 717 I/Os test results. Fig. 21 compares cycles to first failures (about 5% failure) for the CCGA 560 I/Os and CCGA 717 I/Os. The plots include the test results presented here and also data points from a comprehensive thermal cycle test performed in the range of 0–100 °C by another investigator [23]. These plots also include projection from our test results under various thermal conditions to 0/100 °C, a more common thermal cycle temperature range for commercial applications. A similar projection was made for CBGA failure data using Coffin–Manson relationship covering different thermal cycle regimes and

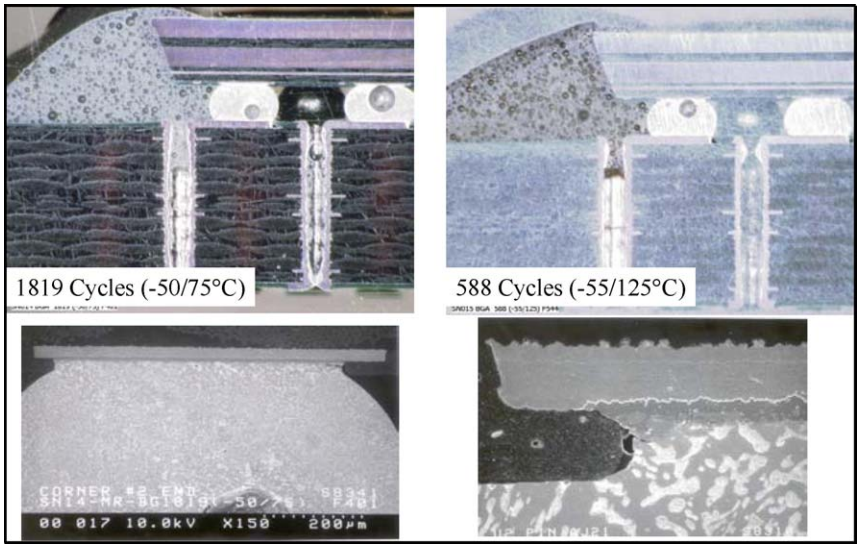

Fig. 14. SEM photomicrographs before and after cross-section for a PBGA package after 588 cycles (−55/125 °C).

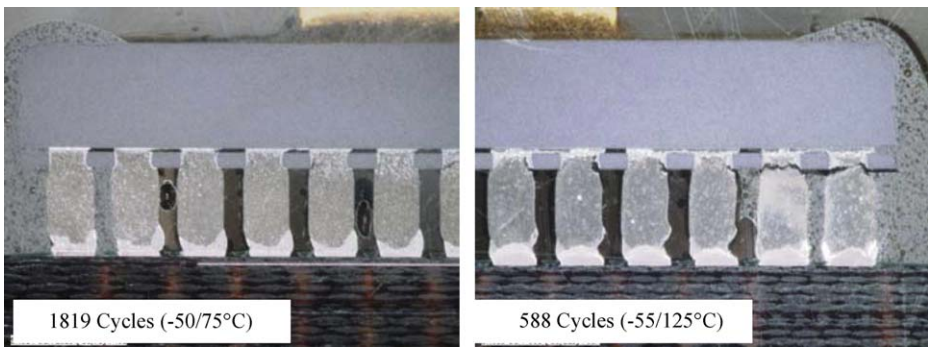

Fig. 15. Photomicrographs of column failure at interposer with corner staking over two thermal cycle ranges.

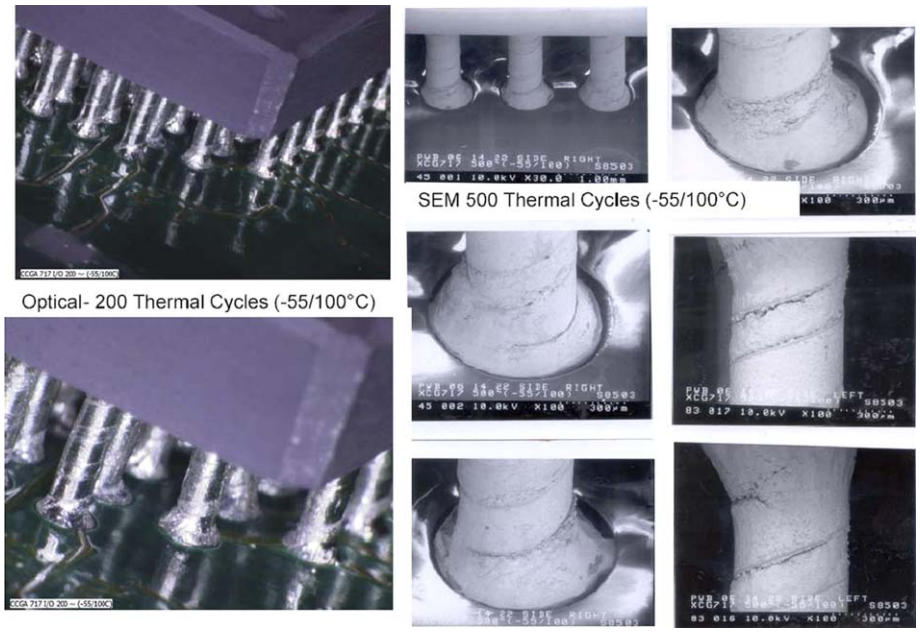

Fig. 16. Optical photomicrographs of CCGA a 717 I/O assembly (left) at 200 and SEM photomicrographs at 500 thermal cycles Cycle B (−55/100 °C)—signs of damage at 500 cycles is apparent.

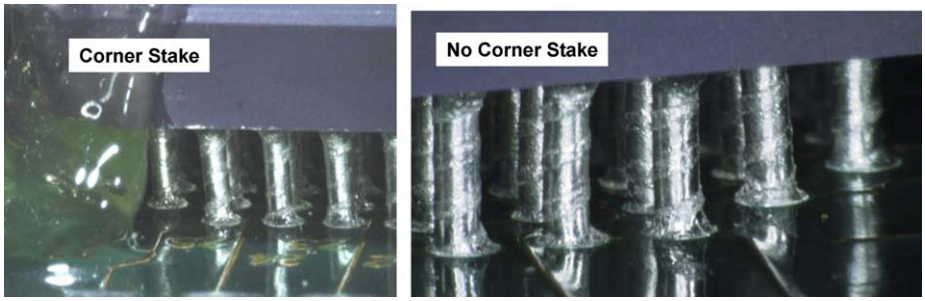

Fig. 17. Optical photomicrographs of two CCGA 717 I/O assemblies with (left) and without corner staking at 950 thermal cycles Cycle B (−55/100 °C) with a minor cracking at the corner column with corner staking.

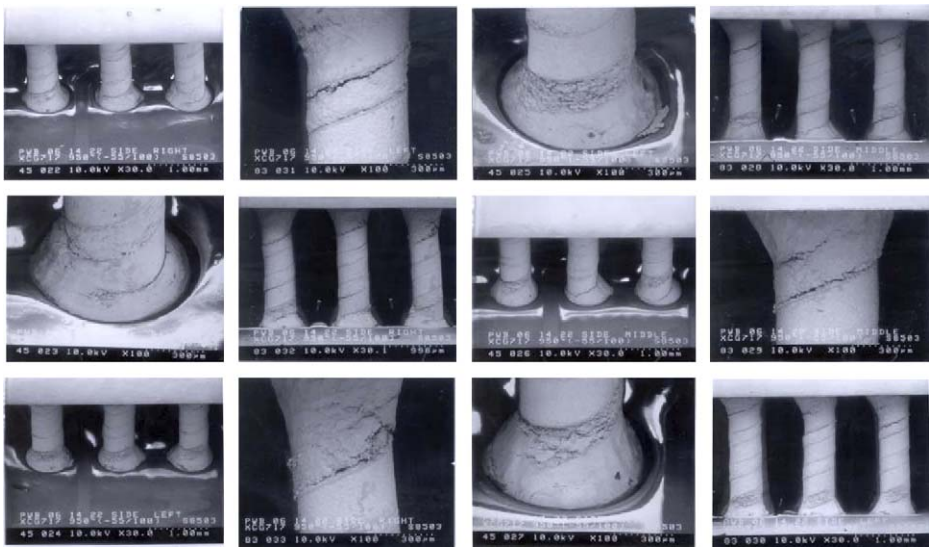

Fig. 18. SEM photomicrographs of CCGA 717 I/O assembly at 950 thermal cycles (−55/100 °C) showing signs of microcracking.

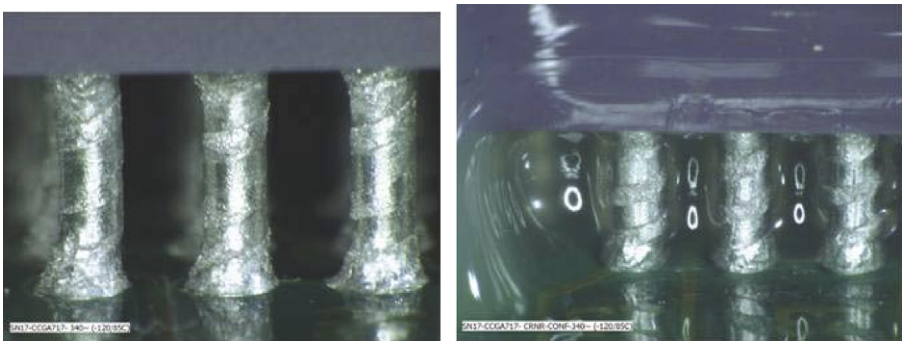

Fig. 19. Optical photomicrographs of CCGA 717 I/O assembly at 340 thermal cycles (−120/85 °C) showing signs of damage, left with no conformal coat and no corner staking and right with conformal coat and corner staking.

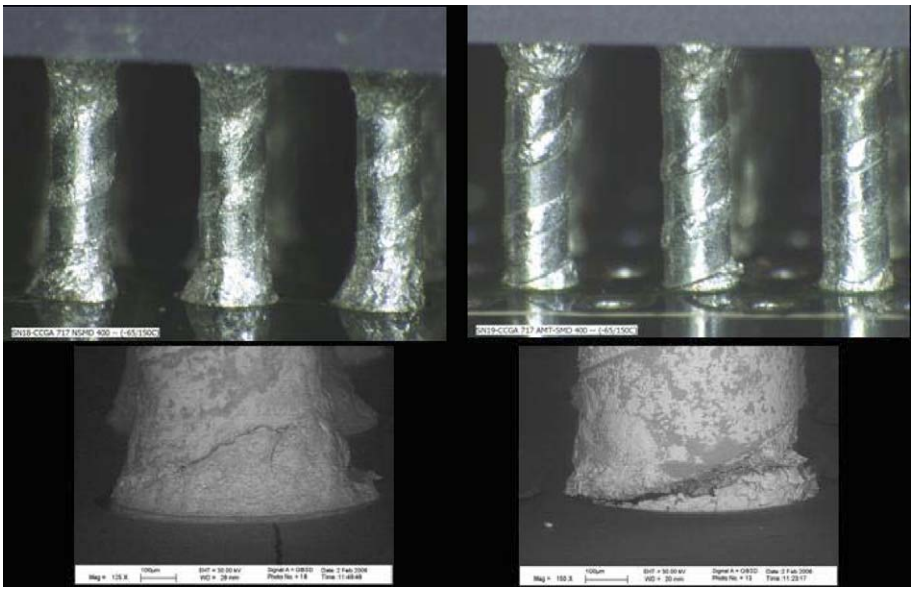

Fig. 20. Optical and SEM (bottom) photomicrographs of CCGA 717 I/O assembly at 400 thermal cycles (−65/150 °C) showing signs of cracking for NSMD pad design with good solder fillet (left) and failure for SMD (right) with lack of solder fillet.

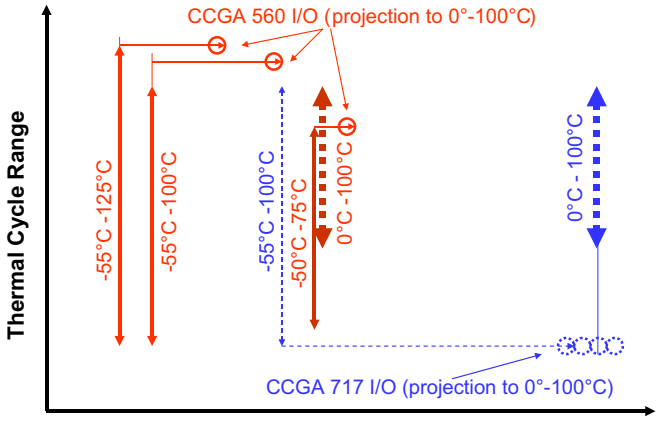

Fig. 21. Effect of temperature range on first failure for CCGA 560 I/Os and no failure yet (−55/100 °C) for CCGA 717 I/Os using a modified Coffin–Manson relationship.

ramp rates [7]. Coffin–Manson relationship is one of many numerous parametric modeling analysis methods that have been proposed and used by industry to project CTF from one thermal cycle condition to a field application. A number of these models for reliability projection of tin–lead solder joint attachments are listed in Table 4 [24].

In the Coffin–Manson relationship, CTF is inversely proportional to the creep strain. Its modified version includes the effects of frequency as well as the maximum temperature. It is given by Eq. (1) below:

$$(N_1/N_2) \propto (\Delta\gamma_2/\Delta\gamma_1)^{\beta}(f_1/f_2)^{\kappa}\exp\{1414(1/T_1 - 1/T_2)\} \quad (1)$$

- N_1 and N_2 represent cycles to failure under two plastic strain conditions. β is the fatigue exponential and is generally assumed to be equal to 1.9 [3,21].
- $\Delta\gamma$ is proportional to $(\mathrm{DNP}/h)\Delta\alpha\Delta T$, where DNP is the distance from the neutral point at the center of package, h is equal to the solder joint height, $\Delta\alpha$ is the difference in the coefficient of thermal expansion of the package and PWB, and ΔT is the cycling temperature range.

Table 4
Summary of various reliability models developed for plastic and ceramic grid array packages

Model	Reliablity/life-prediction representation
Coffin–Manson	$N_f = 2.277 \times 10^{-3}$ (Max $\varepsilon_{eqv})^{-2.61}$: J.H. Lau $N_f = 1.2938(\Delta\varepsilon_{eqv})^{-1.96}$: B.Z. Hong $N_f = 0.4405(\Delta\varepsilon^{eqv})^{-1.96}$: K.N. Chiang et al. $N_f = K(\varepsilon_p^{-2})$: M. Farooq et al. $N_f = 0.5(\Delta\gamma/2\varepsilon'_f)^{1/C}$: Howieson, M. et al. $N_f = 82.4(De_{in})^{-0.863}$: Perkins, A. et al.
Engelmaier	$N_f(x\%) = \frac{1}{2}\left[\frac{2\varepsilon'_f}{F}\frac{h}{L_D\Delta\alpha\Delta T_c}\right]^{-1/c} \cdot \left[\frac{\ln(1-0.01x)}{\ln(0.5)}\right]^{1/\beta}$
Norris–Landzberg	$AF = \frac{N_p}{N_t} = \left(\frac{\Delta T_t}{\Delta T_p}\right)^{1.9}\left(\frac{f_p}{f_t}\right)^{1/3} e^{1414\left(\frac{1}{T_{max,p}}-\frac{1}{T_{max,t}}\right)}$: S.Y. Teng $N_{50\%} = \left(\frac{100}{\Delta T}\right)^{1.9}\left(\frac{f}{2}\right) e^{1414\left(\frac{1}{T_{max}}-\frac{1}{373}\right)}(G)$ $G = (12439 - 70.1A - 434B - 1301C - 930D - 272E + 302CD)$; A: Substrate size, B: Board and substrate CTE mismatch C: Substrate thickness, D: Board thickness, E: Ball pitch: A. Perkins et al.
Darveaux	$N_{init} = C_1(\Delta W_{ave})^{C_2}, da/dN = C_3(\Delta W_{ave})^{C_4}$ $C_1 = 13173$, $C_2 = -1.38$ to -1.45, $C_3 = 1.72$–3.92, $C_4 = 1.12$–1.15
SRS	$N_{63.2\%}/A + C_1(\Delta W_{in})^{C_2}$ $C_2 = -1$: J. Clech $N_f = (\Delta W)^{1.51}\left(\frac{A_i}{A_D}\right)A_D = 5.9 \times 10^{-3}$ mm^2: Wong, T.E. et al.
Lall	$N_{1\%f} = (\text{DietnBcdyRatio})^{b1}$ $(\text{BallCount})^{b2}(\text{BallDiaMM})^{b3}$ $(\text{PCBthkMM})^{b4}(\text{EMCFiIIID})^{b5}$ $(\text{MaskDefID})^{b6}$ $(\text{BoardFinishID})^{b7}\Delta T^{b8}$ $N_{1\%f}$ is the cycle to 1% failure, A and the indices bi's ($b1, b2, \ldots, b8$) are the coefficients of the model

- f_1 and f_2 are fatigue frequencies. κ is the frequency exponential varying from 0 to 1, with value 0 for no frequency effect and 1 for the maximum effect depending on the materials and testing conditions. A value equal to 1/3 is commonly used to extrapolate the laboratory accelerated thermal cycles-to-failure data with short duration (high frequency) to on/off field operating cycle with long duration (low frequency), i.e., a shorter field cycles-to-failure projection.
- T_1 and T_2 are maximum temperatures (in K) under the two cycling conditions.

The above relationship was used to correlate the test results for the CCGA 560 I/Os for three thermal cycling conditions with increasing temperature ranges, i.e., −50/75 °C, −55/100 °C, and −55/125 °C to a control cycle data set in the range of 0/100 °C. As the peak temperature and temperature range increase, projections become less accurate. Projection is the least accurate for the extreme range of −55 to 125 °C and better matches the CTF data for −50/75 °C. So, the test results are either conservative or non-conservative depending upon as how they are considered for a field application—the use of 560 I/O FPGA packages for the Mars Rover become questionable when the CTF data for the higher cycle range first became available and did not meet the 3× life cycle requirement for the mission. For example, if data generated by the package supplier, generally in the range of 0/100 °C, are considered as the baseline for the CTF projection to a harsher requirement of −55 to 125 °C as another baseline for data comparison, then projection could result in unrealistic non-conservative CTF data. On the other hand, if the extreme temperature data are consider, its conservative projection could cause rejection of a package that might be suitable for a field application. Microstructural and failure mechanism changes due to corner staking (demonstrated here by testing) are also unknown factors that must be considered for such environmental applications.

Even though no failures have yet been observed for CCGA 717 I/O assemblies for thermal cycling in the various ranges, including −55/100 °C; however, projections were made based on the current 950 thermal cycles. This value [What value?] was used to project CTF from this temperature range to the control data set and is included in the plots. Projection for the case of CCGA 717 I/Os contradicts those made for CCGA 560 I/Os. Projection from our thermal cycle test data (−55/100 °C) to the package supplier's thermal cycle range (0/100 °C) results in higher values even though identical test vehicles were used for both thermal cycle conditions. They were, however, assembled at two different facilities. Solder volume and more accurate process control may be one possible explanation for the improvement observed relative to the package supplier's test condition. The other possible explanation may be related to column design; the copper wrap may be such that the effects of exposure below 0 °C become of less critical. None of these hypotheses have been verified and remain as postulated until they are tested by a more comprehensive design of experiment with control variables, including various thermal cycle parameters.

4. Conclusions

It is well established that solder joint reliability of plastic packages on polymeric boards is typically better than that of their ceramic counterparts. This trend was verified during our investigation. The current status of thermal cycles for the two CCGA package assemblies is as follows:

- Plastic package assemblies did not show failures to 2000 cycles, whereas CCGA 560 I/O assemblies showed first failure at 1075 cycles when subjected to the −50/75 °C cycle. The first failure was from the package site since a relatively high solder paste amount was used for assembly. For a lower solder volume, failures occurred at the board site. For CCGA, effect of solder volume is not the same as for CBGA.
- The CCGA 717 I/O assemblies showed various levels of solder joint damage at 1000 cycles (−55/100 °C) when inspected optically and by SEM. For those with corner-staking adhesive, the corner columns showed a higher damage level compared to their counterparts without staking.
- None of the PBGA 728 I/O and CCGA 717 I/O assemblies failed during continuous monitoring when subjected to 1000 thermal cycles in the range of −55 to 100 °C. These include those assembled with either vapor phase reflow at the two assembly facilities or the rework station and assembled with and without corner staking as well as those with conformal coating. Visual inspection and manual probing was performed at numerous intervals and revealed no signs of opens, further verifying continuous monitoring test results.
- None of the PBGA 728 I/O and CCGA 717 I/O assemblies failed during continuous monitoring when subjected to 200 thermal cycles in the range of −55 to 125 °C. Assemblies tested include those with and without corner staking and conformal coating.
- No failure for CCGA 717 I/O assemblies (the 728 I/O assemblies were not tested) after 200 thermal cycles in the range of −120 to 85 °C. Assemblies tested include those with and without corner staking and conformal coating.
- No failure for CCGA 717 I/O assemblies after 200 thermal cycles in the range of −65 to 150 °C. Only two assemblies that had no staking/coating were tested.
- The CCGA 717 I/Os assembled onto PWBs with SMD pad design showed severe damage and cracking compare to NSMD design when subjected to −65 to 150 °C thermal cycling.
- Using the modified Coffin–Manson relationship, cycles to failures for CCGA 560 I/Os and CCGA 717 I/Os under three thermal cycle conditions (−55/125°C, −55/100 °C, 0/100 °C) were projected to CTF test data under another thermal cycle condition (0/100°C), preferred condition specified by IPC-9701A. CTF projections for CCGA 560 I/Os were lower, whereas for CCGA 717 I/Os were higher than CTF data for preferred cycle condition. The root cause of such conflicting projections based on the test results is unknown at this time even though package style, column type, and assembly process differences may have contributed to the difference.

4.1. Recommendation for space application

Qualification and verification steps for CCGA, CBGA, BGA, and CSP packages for various NASA missions are summarized below. Prior to design, it is recommended to review industry standards on this subject including IPC-7095, *Design and Assembly Process Implementation for BGAs*, and IPC-9701A [8].

Recommendations for NASA or space mission implementation are as follows:

- Define the overall mission environmental requirements including radiation, mechanical, thermal, life cycle, etc.
- Define the appropriate potential package technology and package types including CCGA, CBGA, BGA, CSP, numberof I/Os, build up, materials, solder geometry and materials, heat distribution, etc.
- Determine if package properties are within the envelope of mission environmental requirements to avoid early overstress failures. Examples are: radiation capability of die, temperature limits of package materials including softening (glass transition temperature, T_g) and junction temperatures.
- Determine if the packaging internal materials and interconnections including wire bonds can meet package/part qualification requirements, including static and dynamic burn-in and qualification. Minimize burn-in order to avoid consuming most of package life.
- For life thermal cycle qualification, determine the life cycle requirements for the mission. The life cycle requirement shall be three (3) times the realistic worst-case life consumption including ground test.

For the purpose of further narrowing the package selection, consider the following four categories of missions.

- A: Benign thermal cycle exposure with short mission duration.
- B: Benign thermal cycles with long mission duration.
- C: Extreme thermal cycles with short mission duration.
- D: Extreme temperature cycle exposure with long mission duration.
- If details on life cycle requirements are not available, then use the following rules-of-thumb to estimate the number of accelerated thermal cycles for the missions.
- For the A and B missions, thermal life cycle requirements are estimated to vary from 100 to 500 NASA thermal cycles (−55/100 °C).
- For the C and D missions, estimate the flight allowable temperature ranges plus the ground exposure and multiply mission life cycles by three (3).

- Review heritage/vendor data for CCGA, CBGA, BGA, and CSP packages. Use the following generic guidelines formeeting the requirements.
- Most plastic BGAs on polymeric circuit boards have sufficient life cycles to meet the A and B mission categories. Plastic packages with very large die may be required to be qualified for use under the B category. Low I/O ceramic packages (<400 I/Os) may have sufficient life for A category missions, but should be verified for the B category missions. High I/O ceramic column grid array packages (>500 I/Os) may or may not meet either A or B mission categories. For example, CCGA 717 I/Os presented in this paper will meet the A and possibly B and C mission categories. It may also meet the D category depending on environment and duration.
- Most CCGA and BGA packages may be required to be qualified when they are considered for the C and D mission categories.
- Most ceramic and plastic CSPs may meet the A mission category requirements. CSPs may be required to be qualified for the B, C, and D mission categories.
- Use the following guidelines when the review of the heritage data indicates that package qualification and verification is required.
- Use a daisy chain package as the test article for accelerated thermal cycle tests. Daisy chain packages are generally built using similar materials and lay up as the functional package with the exception of using a dummy die with even/odd pad connections. Die size affects solder joint reliability and therefore should be the same size or larger than the flight-like package.
- COTS active parts—including area array packages—generally are not designed or manufactured to meet any particular level of radiation hardness for total ionizing dose (TID), single event effects (SEE), and latch up. Therefore, radiation hardness assurance (RHA) assessments have to be performed on every lot. This is true even for follow-up buys of previously procured part types because process improvements, die shrinks, etc. occur almost continuously with COTS parts and such changes can negatively impact radiation performance.
- To perform SEE testing at accelerator is difficult to perform for these advanced packages. Special steps may have to be taken in order to accomplish these tests because of the effects of packaging materials on the ion beam such that the beam must go through in order to reach the part.

PWB design considerations:

- Design in local fiducials, especially for CSPs. Use NSMD for pad design. Include microvia and buried build-up technology if they are used in the flight PWB design. Refer to IPC-2315, 6016, and 4104 for HDI PWB design guidelines. Note that the PWB thickness affects solder joint reliability. Balance the board to avoid PWB warpage. Control warpage by specification and verify by measurement. Review the plated-through hole and microvia aspect ratio, plating thickness, and copper elongation.
- Design a double-sided assembly if it mimics flight configuration. Double-sided, mirror image, assemblies are known to have major reduction in solder joint reliability.
- Use hot air solder leveling (HASL) surface finish and avoid immersion gold on Ni or other exotic finishes. Immersion silver (IAg) is rapidly becoming another finish option, especially for the lead-free solder use.
- For inspection/rework purposes, allow enough clearance (0.15 in.) for optical inspection/rework.

Package assembly considerations:

- Follow the guideline documents for package/PWB preparation, e.g., assure that BGA/CSP balls have sufficient package attachment shear strength, perform the wetability test for ball/PWB, bake the PWB and packages prior to assembly, etc.
- BGAs and most CSPs are robust in assembly and will self-align during reflow. Heavy BGAs may collapse beyond an acceptable level. Note that CCGAs and CBGAs are weak in self-alignment.
- Optimize your reflow thermal profile, especially for a mixed technology assembly. Remember that (1) process optimization and process control are key parameters that control solder attachment integrity, and (2) workmanship cannot be verified by optical/visual inspection, as commonly used for most other electronic packages at NASA. Use of an RMA (rosin mildly activated) flux is recommended. Measure the paste release consistency, and clean after assembly.
- Perform real time X-ray and optical inspection if possible. Use of an X-ray machine with laminography capability is recommended.
- Use a continuous monitoring system to detect electrical interruptions during thermal cycling as detailed in IPC-9701A. Remove at specified intervals for optical/visual inspection to document damage progress and verify the accuracy of the monitoring systems. Use nondestructive and destructive techniques to confirm early failures or non-failures at the end of qualification.
- Use of underfill is not recommended for BGAs, but may be required for CSPs. Select an underfill having a close CTE match to the PWB. If no heritage data is available. However, the underfilled packages must be qualified since their effects on reliability cannot be extrapolated from one package to another. Do not consider underfilling packages with large gaps such as CCGA or very fine gaps such as thin and ultrathin CSPs.
- Reworkable underfill materials are preferred if they can be qualified. Normally their large CTEs do not cause early failure.

- Use corner staking rather than underfilling when it is required for CCGA and CBGA. Be careful to not induce early failures or failures induced by using extreme thermal cycling not representative of the mission environment.

4.1.1. Summary

The key issues and concerns for BGAs and CSPs are:

1. No flight heritage data yet exists, but the CCGA 560 I/Os package performed successfully when used in a benign warm electronic box environment of the Mars Rovers.
2. BGAs and CSPs withstand fewer second level (assembly) thermal cycles than their leaded counterparts. CSPs have lower life than BGAs.
3. If doubt exists regarding the reliability or if the application requires the ability to withstand significant thermal cycling, dummy daisy chain package/boards should be tested
4. A non-destructive inspection technique for interconnection cracks has not yet been developed. Also, individual balls cannot be reworked.
5. Most packages are built for commercial applications and many issues with COTS BGAs/CSPs are similar to those encountered with conventional COTS microcircuits and their packages.

The interconnections of plastic BGAs mounted to polymeric circuit boards are generally more reliable under thermal cycling when compared to ceramic BGA packages mounted to polymeric circuit boards. This is due to a closer match in the materials' coefficient of thermal expansion (CTE). For NASA missions with relatively benign environments, most ceramic packages may be appropriate. For longer NASA missions, plastic packages better meet thermal cycle reliability requirements. Note, however, that COTS plastic encapsulated microcircuits may exhibit other reliability problems.

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