NISTIR 6430

U.S. DEPARTMENT OF COMMERCE

Technology Administration

National Institute of Standards and Technology

NIST

Electronics and Electrical Engineering Laboratory

Semiconductor Electronics Division

Programs, Activities, and Accomplishments

The Electronics and Electrical Engineering Laboratory

Through its technical laboratory research programs, the Electronics and Electrical Engineering Laboratory (EEEL) supports the U.S. electronics industry, its suppliers, and its customers by providing measurement technology needed to maintain and improve their competitive position. EEEL also provides support to the federal government as needed to improve efficiency in technical operations and cooperates with academia in the development and use of measurement methods and scientific data.

EEEL consists of five programmatic divisions and two matrix-managed offices:

- Electricity Division
- Semiconductor Electronics Division
- Radio-Frequency Technology Division
- Electromagnetic Technology Division
- Optoelectronics Division
- Office of Microelectronic Programs
- Office of Law Enforcement Standards

This document describes the technical programs of the Semiconductor Electronics Division. Similar documents describing the other Divisions and Offices are available. Contact NIST/EEEL, 100 Bureau Drive, MS 8100, Gaithersburg, MD 20899-8100, Telephone: (301) 975-2220, On the Web: www.eeel.nist.gov

Cover Caption: (front to back) effective isotropic radiated MEMS-based microwave power sensor, 1.7 mm^2 wire-bonded chip in a ceramic pin grid array (PGA) package, test wafer from SEMATECH (provided by Gennadi Bersuker), and a close-up of copper circuitry for IBM's CMOS 7S chip, the first to exploit copper circuitry.

Electronics and Electrical Engineering Laboratory

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January 2000

U.S. DEPARTMENT OF COMMERCE
William M. Daley, Secretary

Technology Administration
Dr. Cheryl L. Shavers, Under Secretary of Commerce for Technology

National Institute of Standards and Technology
Raymond G. Kammer, Director

Contents

Welcome

David G. Seiler, Division Chief

"The Semiconductor Roadmap is a blueprint for technology development required to maintain the productivity of the semiconductor industry. It does this by targeting research for leading edge technology."

Karen Brown, Characterization and Metrology for ULSI Technology, AIP Press, 1998

The Semiconductor Electronics Division (SED) provides leadership in developing the semiconductor measurement infrastructure essential to improving U.S. economic competitiveness. It provides necessary measurements, physical standards, and supporting data and technology; associated generic technology; and fundamental research results to industry, government, and academia. The primary mission of the Division is to provide the measurement infrastructure to U.S. industry for mainstream silicon CMOS (complementary metal-oxide semiconductor) technology. The Division's programs also respond to industry measurement needs related to compound semiconductors and power devices.

The Division has extensive interactions with individual companies, industry organizations, and professional groups; these activities enable the development of a research agenda responsive to the needs of industry. Active participation in industry roadmapping such as the Semiconductor Industry Association's International Roadmap for Semiconductors and standards activities such as committee work for the American Society for Testing and Materials also is used extensively by the Division to prioritize and establish programs with the highest potential impact.

The Division, with a staff of nearly 50, is based in Gaithersburg, Maryland. The Division is one of five divisions within the Electronics and Electrical Engineering Laboratory at NIST. The Division's technical activities are organized into three Groups: the Materials Technology Group, Device Technology Group, and IC Technology Group. The Division affects industry by providing tools such as standard reference materials (SRMs), test chips, standard reference data, and software that support the needed measurement infrastructure. Division personnel visit industrial sites, host a variety of visitors, and make available tutorial material on an as-needed basis. We also are active in conference and workshop activities that directly benefit the industry. The Division receives and is responsive to hundreds of special requests for assistance from industry each year.

A broad array of activities that serve the semiconductor industry is currently underway in the Division. The staff of the SED addresses projects ranging from materials qualification to test structures for integrated circuits. Some of these projects are supported by the NIST National Semiconductor Metrology Program (NSMP), which is managed by the Electronics and Electrical Engineering Laboratory's Office of Microelectronic Programs. For more information on the NSMP, go to www.eeel.nist.gov/omp.

The Division widely disseminates the results of its research, especially in the areas of standardized test methods and SRMs, through a variety of channels - publications, software, conferences and workshops, and participation in standards organizations and consortia. NIST also actively seeks industrial, academic, and non-profit research partners to work collaboratively on projects of mutual benefit. Our NRC Postdoctoral Opportunities page lists those areas where collaborative efforts are available, with access to the Division laboratory facilities.

The technical programs, activities, and accomplishments described here for each Division Project clearly demonstrate the SED's leadership and effective service as it continues to respond to the needs of industry and to contribute to the scientific and engineering communities.

Thank you for your interest in our Division! I welcome your comments and suggestions. Feel free to e-mail me at david.seiler@nist.gov.

David G. Seiler

Semiconductor Electronics Division Staff

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Mission

The **Semiconductor Electronics Division** provides leadership in developing the semiconductor measurement infrastructure essential to improving U.S. economic competitiveness by providing necessary measurements, physical standards, and supporting data and technology; associated generic technology; and fundamental research results to industry, government, and academia. The primary focus is on mainstream silicon. The Division's programs also respond to industry measurement needs related to compound semiconductors, power devices, and silicon-on-insulator devices.

"The nature of the vision's purpose is not only to achieve a meaningful strategic or company goal, but also to build a dedicated community"

Jay A. Conger, The Brave New World of Leadership Training, IEEE Eng. Mgmt. Review (1996)

Vision

The **Semiconductor Electronics Division** is recognized as a dynamic world-class resource for semiconductor measurements, data, models, and standards focused on enhancing U.S. technological competitiveness in the world market.

Values

The **Semiconductor Electronics Division** values its commitment to identify and to meet crucial measurement technology needs. The Division values its collaboration with all segments of the semiconductor community. It strives for integrity, excellence, objectivity, responsiveness, and creativity, while maximizing and utilizing the potential of its employees.

The Division mission, vision, values, and goals were developed by a strategic planning process facilitated by a professional consultant. This process involved extensive workforce involvement, the Division leadership, and numerous meetings and informal discussions.

Goals

The Division will:

- Aggressively pursue and achieve select metrology needs as identified in the International Technology Roadmap for Semiconductors for mainstream silicon.
- Develop new and improved process-monitoring tools, methodologies, and data for the more efficient manufacture of silicon and compound-semiconductor devices.
- Develop cooperative, multidisciplinary projects within the Diviison and synergistic external collaborative efforts to better meet the critical needs of the semiconductor industry.
- Support novel research that has high potential for providing break-throughs in materials, process, devices, and measurement technologies for the semiconductor industry.

SEMICONDUCTORS: Backbone of the Electronic/Digital Revolution

"... we are at the dawn of a new technology and telecommunications renaissance, one that is still in its infancy... Its creation is so revolutionary - the changes it has wrought are so vast - that even those of us who have worked on it for years cannot predict its full impact."

Vice President Al Gore, Speech at the 15th International ITU Conference, October 12, 1998

"The U.S. economy has undergone a fundamental shift in the 1990's. New industries dependent on innovation are now the source of jobs, income, and growth. Without warning, the U.S. has been transformed into a high technology economy that thrives on information appliances, high tech tools that enable people to communicate, and the creativity of a highly trained and entrepreneurial workforce. One technology outshines all the others and in fact, enables the others to prosper - the semiconductor. The tiny microchip drives virtually all electronics products. Even the internet is, in reality, a world wide web of semiconductors."

Semiconductor Industry Association (SIA) Report, March 1998

Semiconductors, transistors, and their applications represent one of the greatest scientific and technological breakthroughs of the twentieth century. Consider their far reaching influence on our society in general and on our daily lives. Can you imagine life without them? Semiconductors are pervasive in the microelectronic components used in computers, entertainment equipment, automotive electronics, medical instrumentation, telecommunications, space technology, television, radio, cell phones, and a whole host of other information technologies. Today, you can even purchase a CDMA-based watch phone, which combines the functions of a digital watch with that of a wireless communications handset. Every hospital, school, factory, car, airplane, office, bank, and household contains transistors, microprocessors, and other semiconductor devices.

These breakthroughs are possible because of the miniaturization of the transistor dimensions, which allow the construction of compact systems with tremendous computing power and memory. Miniaturization, in turn, is possible because of the perfection of fabrication techniques that allow the "integration" of circuits and thus the production of chips containing millions of elements per square centimeter. The foundation stone of this complex technology is silicon. Meeting the demands for these large-scale, complex, integrated circuits (ICs) continues to require technological advances in materials, processing, circuit design, characterization, testing, and standards.

The semiconductor electronics industry is outstripping the measurement capability needed for maintaining and improving U.S. international competitiveness. Important factors affected are product performance, price, quality, compatibility, time to market, etc. The Division provides three major classes of deliverables: measurement capability, technology development, and fundamental research. It provides the measurement capability needed to support the efforts of U.S. industry to improve its competitiveness. In order to support this effort, the Division also engages in technology development and fundamental research, and makes the findings available to industry.

The Division focuses the largest part of its resources on the development and delivery of measurement capability for two principal reasons:

- Measurement capability has a very high impact on U.S. industry because measurement capability supports manufacturers in addressing so many of the challenges that they face in realizing competitive products in the marketplace.
- NIST is the official lead U.S. Government agency for measurements.

The Division focuses on developing measurement capability that is beyond the reach of the broad range of individual companies. Companies seek NIST's help for several reasons:

- The companies need NIST's special technical capability for measurement development.
- The companies need NIST's acknowledged impartiality for diagnosing a measurement problem affecting the industry broadly or for achieving adoption of a solution across the industry.
- The companies cannot develop the measurement capability needed by the industry broadly because they cannot individually capture the returns of the cost of development.

- Industry's quality standards require that key measurements be traceable to the national measurement reference standards that NIST maintains. This is a requirement of growing importance in export markets.

The Division continues to interact/collaborate with a wide variety of companies, consortia (such as Semiconductor Manufacturing Technology (SEMATECH), Semiconductor Equipment and Materials International (SEMI), and the Semiconductor Research Corporation (SRC)), academia, and other government labs to accomplish its mission. Specific details are given in the Project Sheets that follow. Work in the Division results in extensive outputs or deliverables that cover knowledge/improvements in physical understanding, test methods/measurements, Standard Reference Materials (SRMs), Standard Reference Data (SRD) sets, standards, test structures/test chips, software, measurement accuracy/traceability, publications/reports, patents/Cooperative Research and Development Agreements (CRADAs), round robins, data and models, talks/short courses, company visits, conferences/workshops, consortia participation, and various activities and leadership roles on committees and working groups.

The Standard Reference Materials Program of NIST provides science, industry, and government with a central source of well-characterized materials certified for some chemical or physical property. These materials are designated Standards Reference Materials (SRMs). For more information, see the NIST web site at: ts.nist.gov/srm

Division staff serve the semiconductor community in leadership roles on standards committees such as American Society for Testing and Materials (ASTM) and Electronic Industries Alliance (EIA) / Joint Electron Device Engineering Council (JEDEC), societies such as IEEE and ECS, and on numerous semiconductor conferences/workshops. A large number of test methods and standards have been developed and written over the years by NIST staff for ASTM and EIA/JEDEC, including ones for resistivity, oxygen in silicon, thin dielectrics, electromigration, and device characterization. This past year, staff have served on various Technical Working Groups to help put together the 1999 International Technology Roadmap for Semiconductors (ITRS). These Groups were Process Integration, Devices, and Structures; Assembly and Packaging; Lithography; Interconnect; and Front End Processes. The ITRS provides targets for equipment, material, and software suppliers, targets for researchers, and serves as a common reference for the semiconductor industry.

The Division has also impacted the semiconductor community by producing a number of SRMs. To date, over 2500 SRMs have been sold and distributed for resistivity, oxygen in silicon, and optical thickness by ellipsometry. Hundreds of companies throughout the world have purchased these SRMs to maintain and improve their measurement capability.

Mounting a silicon wafer on the resistivity instrument stage prior to taking measurements for SRM certification.

National Institute of Standards & Technology

Certificate

Standard Reference Material® 2544

Silicon Resistivity Standard - 10 ohm.cm Level

This Standard Reference Material (SRM) is intended primarily for use in the determination of sheet resistance and bulk resistivity using the DC four-point probe method. SRM 2544 is a nominal 100 mm diameter float zone n-type silicon wafer with (111) crystallographic orientation, doped with phosphorus by the Neutron Transmutation Doping (NTD) process... The certified sheet resistance and resistivity values at the wafer's center are given in Table 1a and the sheet resistance is given at 60 increments on the radii of 5 mm and 10 mm circles in Table 1b. The stated uncertainty values for this unit are derived from a statistical analysis of the entire lot of wafers produced at the 10 ohm-cm resistivity level.

Semiconductor Electronics Division Organization

The Fiscal Year 2000 organization of the Semiconductor Electronics Division is reflected. The Optical Metrology for Semiconductor Manufacturing Project has been integrated into other Projects. The Linewidth and Overlay Standards for Nanometer Metrology Project was formerly titled Metrology for Process and Tool Control.

Legend:

AO = Administrative Officer
CTR = Contractor
FH = Faculty Hire
FM = Facility Manager
GL = Group Leader
GR = Guest Researcher
PD = Postdoctural Appointment
PL = Project Leader
PT = Part Time
S = Student

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2049 MARSHALL, Janet C. (PT)
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2052 ZAGHLOUL, Mona E. (FH)
2073 ZINCKE, Christian A. (GR)

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2052 WILKES, Jane M., Secretary
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2234 SCHAFFT, Harry A.
4723 VOGEL, Eric
2111 WANG, Bin (GR)
2111 WU, Huixian (GR)

Metrology for Compound Semiconductor Manufacturing

Technical Contact:
Joseph G. Pellegrino

Staff-Years:
6.0 professionals
1.0 technician

Funding Sources:
NIST (100%)

Parent Program:
Semiconductors, Compound

"We have learned that real-time process control by in-situ monitoring is essential for fabricating high quality, epitaxial layers on compound semiconductor wafers at low cost and high yields."

Harvey Serreze, Director of R&D, Spire Corporation, June 8, 1999

Project Goals

Provide technological leadership to semiconductor and equipment manufacturers by developing and evaluating the methods, tools, and artifacts needed to improve the state of the art in compound-semiconductor growth and nanometrology (measurements on a scale of 10 nm to 100 nm). Provide measurements of growth and structural parameters in addition to fabrication properties required for the reliable manufacture of nanostructure devices. Develop research materials and methods to improve measurement standards. Provide reference methods and reference materials to assist the U.S. III-V manufacturing community.

Performing *in-situ* X-ray emission measurements.

Customer Needs

The GaAs and III-V compound semiconductor manufacturing community has experienced tremendous growth in the last fifteen years. A large part of this growth has been due to the wireless and cellular phone market. These growth opportunities are also coupled with new technological challenges for the GaAs manufacturing industry. This growth has resulted in new demand for equipment manufacturers. End users of III-V material now require epilayer heterostructures with compositional tolerances less than one percent and for some devices, thickness tolerances at the atomic monolayer level. *In-situ* probe manufacturers look to NIST for cross-correlation of their probes with complementary measurements. Increasingly, epilayer foundries are looking to real-time process monitors to reduce costs and improve manufacturing efficiency. *In-situ* metrology has emerged as a key enabling technology to improve real-time monitoring and control. With new and improved real-time probes, manufacturers look forward to reduced losses from material that is not within spec. As the cost and complexity of epilayers increases, the epilayer growers and end users need to be able to reliably and reproducibly generate epilayers with thickness control at the atomic level as well as temperature control to within 1 °C! Controlling thickness, temperature, and composition are among the greatest challenges that currently confront manufacturers. *In-situ* growth control offers the tools for advancing epilayer deposition technology.

Technical Strategy

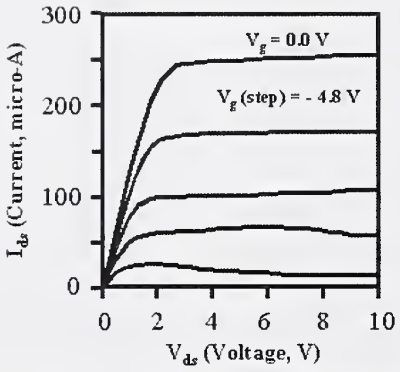
There are several technical thrusts within the project. A major focus involves the deployment of *in-situ* techniques to advance real-time control of the III-V deposition process, based on an array of optical, electron, and X-ray probes. These probes are used to determine layer thickness, composition, and temperature in real time. This includes a one-of-a-kind *in-situ*, X-ray emission probe capable of detecting the surface epilayer composition in real time, even while the substrate rotates. An *in-situ* diffuse reflectance probe makes use of the substrate's absorption edge to monitor surface temperature to within 1 °C while the sample rotates. This probe can be used passively or in an active feedback mode to both control and monitor surface temperature during growth. Other *in-situ* probes include spectroscopic ellipsometry for composition, thickness, and temperature monitoring during the deposition process as well as Reflection High Energy Electron Diffraction (RHEED) and desorption spectroscopy.

One of the Project's on-going efforts is to correlate the materials parameters measured during the growth of III-V heterostructures with the electrical properties of devices fabricated from this same material. The psuedomorphic high electron mobility transistor (pHEMT) is one device we are addressing within the project. Working with the Gallium Arsenide (GaAs) manufacturing community, we are able to provide advice on the efficiency of a specific probe for an extensive real-time monitor on our *in-situ* MBE growth chamber. Companies use

"Such (sensor) techniques enable more precise epitaxial growth of material structures with multiple layers and compositions, thus resulting in higher wafer yields and therefore lowering wafer costs."

Dr. Leye Aina, Director, Epitaxial Technologies, January 8, 1999

FET characteristics



Focused Ion Beam (FIB) direct-write on 2-DEG materials to form laterally gated HEMT Structures, Mat. Lett. 40 (1999) 235-239

our *in-situ* facility as a testbed for new probes as well as a resource for additional *in-situ* information to compare with their own measurements. In this way, the project provides a valuable service to sensor manufacturers. By directly measuring critical growth parameters, we help the III-V manufacturers to more efficiently control the epilayer growth process in order to meet new technology challenges. Project goals also include efforts to build measurement consensus among major GaAs manufacturers.

Project staff work to provide the III-V community with benchmarks for artifacts and procedures. These efforts include an electronic website for Hall measurements.

MILESTONE: By 2000, produce a web-based electronic Hall measurement page that industrial and academic users can reference to benchmark their measurement procedures and Hall data analysis.

Project staff have also initiated an international Hall round robin among major GaAs manufacturers in order to assess and ultimately establish measurement consensus related to mobility and sheet carrier concentrations.

MILESTONE: By 2000, produce a compilation of the industrial round robin results for public dissemination.

Project activities include a collaboration with other NIST Divisions (Optoelectronics, Ceramics, Surface and Microanalysis Science) to develop III-V compositional standards. This is part of an intramural program sponsored by NIST's Advanced Technology Program (ATP).

Project staff are working with the Manufacturing Engineering Laboratory (MEL) to develop an artifact transferal system that allows transport of an MBE wafer in a UHV environment to MEL's STM facility for surface characterization. This work is part of the National Manufacturing Testbed (NAMT) program within MEL. Collaboration with MEL includes a GaAs-based linewidth artifact for use by semiconductor equipment manufacturers. The artifact will be used for pitch as well as linewidth measurements.

The Project received competence funding to explore the metrology and properties of a new class of semiconductor materials called Photonic Crystals. The competence program includes the Optoelectronics Division and the Electromagnetic Technology Division. Project goals are to use MBE growth, *in-situ* monitoring and control, as well as post-growth processing to explore the metrology of photonic crystals and molecules. Applications for this new class of material include photon-generator turnstiles and wave-guides. Focused ion beam technology and wet chemistry facilities within the Division are used by Project staff for processing.

Milestone: By 2003, fabricate and characterize a photonic molecule using focused ion beam technology.

Accomplishments

- Demonstrated that unique *in-situ* X-ray emission probe can measure composition of ternary semiconductors during growth. The X-ray probe results agreed with conventional RHEED measurements done prior to growth to within 1.4 % indium content for an InGaAs (indium gallium arsenide) wafer grown on GaAs. Showed that controlling the electron beam current is critical to obtaining good quantitative analysis. Have installed a Faraday cup on the *in-situ* electron gun to measure electron beam current before and after data acquisition.

- Implemented a Hall Round Robin to help build measurement consensus among GaAs manufacturers. The round robin involves 11 companies (domestic and foreign): AXT, QED, Airtron, Picogiga, Aixtron, Ovation, Emcore, Macom, Epitronics, Hitachi Cable, and Freiburger.

- Implemented diffuse reflectance spectrometer (DRS) for active control of

"If the compound semiconductor industry is to achieve low cost and high performance in submicron devices, there needs to be established various in-situ control schemes to ensure high yield to very tight specifications on layer thickness, doping concentration and profiles, and layer composition."

Dan Rode, President, Pendragon Corporation, March 1, 1998

substrate temperature during MBE growth. Employed DRS in fabrication of pseudomorphic high electron mobility transistors (pHEMTs). Eliminated 70 °C overshoot experienced by conventional, thermocouple controlled samples. Identified and corrected acquisition and output errors in DRS software by collaborating with equipment manufacturer, Thermionics Northwest. Helped the manufacturer supply the user community with a more effective and useful product.

- Used Division's FIB facility to fabricate laterally gated AlGaAs/InGaAs pseudomorphic high-electron-mobility transistors. The fabricated transistors show typical field-effect transistor (FET) characteristics. The transfer characteristics in the subthreshold region show gate leakage similar to that of metal-semiconductor FETs.

- Established an extensive WWW site at www.eeel.nist.gov/812/itrcs.html to disseminate information about compound semiconductors and to gather comments from industry concerning the proposed International Technology Roadmap for Compound Semiconductors.

- Identified and corrected acquisition errors in RHEED analysis software. Collaborated with k-Space Associates. Aided the Group's metrology needs for growth rate calibration. Helped manufacturer supply user community with more accurate software.

- EMCORE used NIST MBE as test platform for their new emissivity corrected pyrometer. Implemented emissivity corrected pyrometer on Division MBE as part of a collaboration with EMCORE Corporation. Demonstrated effectiveness of this instrument for MBE use, as well as for CVD where it had been tested before. Demonstrated superiority over conventional thermocouple, with comparable sensitivity and responsiveness to DRS, in temperature range of interest. Furthered Group mission of evaluating the measurement methods needed for compound semiconductor manufacturing. Identified potential market for the manufacturer.

- Grew a series of low-temperature GaAs epilayers as part of a collaboration with the Electricity Division to make use of the fast recombination times of low temperature GaAs to make devices that can be used for ultra-fast pulse characterization. The low temperature growth was facilitated by use of the Diffuse Reflectance *in-situ* probe that was used to accurately control the wafer temperature at low growth temperatures. Such control is not possible with conventional pyrometry.

- Examined the optical properties of low temperature GaAs films with *in-situ* and *ex-situ* spectroscopic ellipsometry. Results indicate that there is a marked deviation between the optical responses of the as-grown and annealed low-temperature films. This difference increases at lower growth temperatures. Measurements reveal that some of the low temperature GaAs behave like GaAs that has been ion implanted. Ellipsometry measurements were correlated with diffuse reflectance, RHEED, and X-ray diffraction measurements.

FY Deliverables

Collaborations

Optoelectronics Division, MSEL-852, and CSTL-837, ATP proposal funded jointly to develop compound SC standards (J. Pellegrino)

MSEL-852, vacuum suitcase project (J. Pellegrino)

CSTL-837 and MSEL-855, MBE X-ray fluorescence sensor project (J. Pellegrino)

MEL-821, NAMT funded atom-based linewidth standards (J. Pellegrino)

Precision Engineering Division and the University of Maryland, low temperature GaAs (J. Pellegrino)

Optoelectronics Division and Electromagnetic Technology Division, photonic molecules competence project (J. Pellegrino)

CSTL-837 (Chemistry Division), improve analysis procedures for glancing angle fluorescence measurements (W. Tseng)

MSEL (Ceramics Division), study buried interfaces using X-ray standing waves and other synchrotron techniques (W. Tseng)

External Recognition

J. Pellegrino was elected to the GaAs MANTECH Executive Committee.

J. Pellegrino was elected Exhibits Chairperson for the 2000 GaAs MANTECH conference.

J. Pellegrino served on the selection evaluation board for the ATP Electronics competition (three months).

J. Pellegrino wrote a competence proposal with the Optoelectronics Division and the Electromagnetic Technology Division entitled "Photonic Molecules, Lattices, and Turnstiles," that was approved for funding.

Publications

Bennett, H. S., Pellegrino, J. G., Rode, D. L., Shaffner, T. J., and Seiler, D. G., Do We Need a Roadmap?, Compound Semiconductors 5 (3), pp. 43-44 (April 1999).

Gupta, J. A., Woicik, J. C., Watkins, S. P., Miyano, K. E., Pellegrino, J. G., and Crozier, E. D., An X-Ray Standing Wave Study of Ultrathin InAs Films in GaAs (001) Grown by

Atomic Layer Epitaxy, J. Crystal Growth, 195, pp. 34-40 (1998).

Kim, J. S., A Matrix Formalism of Hall Effects in Multicarrier Semiconductor Systems, J. Appl. Phys. 86 (6), pp. 3187-3194 (15 September 1999).

Pellegrino, J. G., Armstrong, J., Lowney, J. R., Dicamillo, B., and Woicik, J. C., Electron Beam Induced X-Ray Emission: *In-Situ* probe for Composition Determination During Molecular Beam Epitaxy Growth Appl. Phys. Lett. 73 (24), 3580-3582.

Tseng, W. F., and Monk, D. H., Sub-Threshold Characteristics of Laterally Gated AlGaAs/InGaAs pHEMT Fabricated with Focused Ion Beam Implantation, Materials Letters, 40/5, pp. 235-239, September 1999.

Optical Metrology for Semiconductor Manufacturing

Technical Contact:
Paul M. Amirtharaj

Staff-Years:
2.3 professionals
1.0 guest researcher

Funding Sources:
NIST (100%)

Parent Program:
Semiconductors, Compound

Project Goals

Develop and implement advanced and robust optical probes needed by the semiconductor industry to qualify semiconductor materials and device structures. Develop research materials and methods and compile standard reference data to improve device design and fabrication.

Performing in-situ X-ray emission measurements.

Customer Needs

Rapid developments in the Si IC industry, driven by advances in scaling and functionality, are leading to ever-increasing demands for quantitative analytical techniques with unprecedented accuracy, robustness, and ease of use. Optical techniques have been called upon to fill some of these critical needs because they are nondestructive and contactless, and are compatible with most materials growth and processing environments. This project has focused on applying low-energy optical techniques such as infrared absorption and photoluminescence to detect and quantify impurities in various technologically important semiconductors, alloy composition in compound semiconductors, and the chemical state of ultrathin insulators on silicon.

Technical Strategy

While often the basic physics of the interaction of light with semiconductor materials are well understood, it is not possible to translate the knowledge to help make accurate measurements. The emphasis in the published literature has been on the spectroscopic aspects achieved at the expense of photometric accuracy. Our approach has been to place equal emphasis on both, which has led to unprecedented accuracy in measuring the optical response, which in turn has translated to superior metrological accuracy.

MILESTONE: By 1999, complete FTIR methodology to improve the accuracy of the optical constants, n and k, by a factor of 10 in the 2.5 μm to 20 μm region.

Optical constants represent the most basic form of interaction of light with a material. Detailed knowledge of these is essential for accurate characterization of the material, in particular to analyze the deviation from perfect structural and chemical composition. The accuracy of the optical constants of silicon was improved by a factor of 10.

MILESTONE: By 1999, develop FTIR measurement of interstitial oxygen in conducting wafers: (a) Complete modeling of IR response of conducting Si wafers, and (b) Complete 300K reflection and transmission measurements on wafers with $\rho \geq 0.02$ Ω.cm (n-type) and $\rho \geq 0.1$ Ω.cm (p-type) wafers.

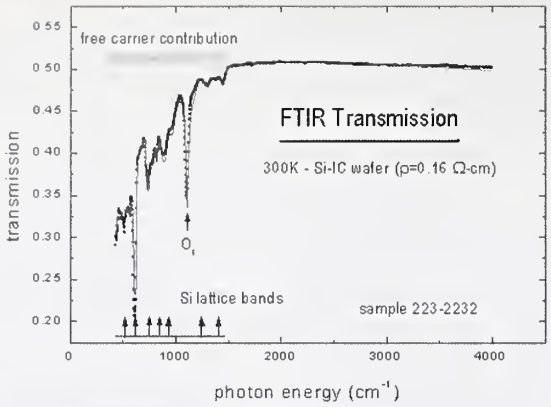
The semiconductor industry has relied on high-accuracy and precision measurements of oxygen in silicon by FTIR since the early 1970's. At that time, it was first recognized that oxygen, when precipitated, results in crystal defects that entrap metal impurities away from active device junctions at the surface. In spite of the successful development of this technology over the past two decades, little progress has been made in measuring interstitial oxygen (O_i) in heavily doped silicon, the material of choice for current and future IC fabrication. The problem arises from free-carrier-induced reflection and absorption of infrared light in such conducting substrates. The FTIR methodology to determine the concentration of oxygen in medium resistivity wafers was developed. Work towards developing a technique capable of analyzing heavily doped wafers is in progress.

MILESTONE: By 1999, complete photoluminescence and photoreflectance measurements on AlGaAs samples for alloy composition standards development.

Modern compound semiconductor devices are fabricated using a number of alloys with varying bandgap, interface discontinuities, and related properties. The behavior of these devices depends critically on the exact composition of the alloy, and industry has been demanding robust

"Nondestructive FTIR methodology for the measurement of oxygen content in heavily doped silicon is one of five metrology innovation gaps that exist today."

SRC, SEMATECH and International SEMATECH, Provided by Steve Knight, OMP



Infrared transmission spectrum from a conducting Czochralski wafer: data (line) and model calculations (dots) are shown. Note that all the observed features Si lattice, oxygen impurity and the charge carriers are observed and reproduced by the model.

methodologies as well as artifacts. Photoluminescence and photoreflectance methods were developed for this purpose in collaboration with the other NIST researchers.

Accomplishments

- Developed differential FTIR absorption methodology for the detection and quantitative analysis of interstitial and precipitated oxygen in 300 mm Czochralski silicon wafers for emerging IC applications. Analyses of samples processed at SEMATECH indicate that the ASTM procedure (F1188-93a) used to measure interstitial oxygen in annealed samples contains a source of error. Quantitative analyses of the error and procedures to correct this are underway. Measurements using wedged samples, required for high-resolution low-temperature analyses, introduced a large spectral artifact as a result of distortion to the complex beam path. A mechanical compensation procedure was established with assistance from the instrument manufacturer. The optical components needed were obtained from the instrument manufacturer and tested.

- The capability to perform IR transmission measurements using polarized light has been added. IR polarizers were borrowed from the Physics lab for these measurements. The added capability is required to cross check the n and k measurement results we obtained in fiscal year 1998. Ultrahigh purity silicon wafers ($\rho >$ 30,000 Ω-cm) were prepared to cross check earlier measurements. The modeling capability was improved to accommodate small deviations from collimation, thereby increasing the signal-to-noise measurement by a factor of 10. A study of temperature effects to eliminate error due to temperature variations was completed. The n and k measurements on several new samples were completed to establish the statistical limits of the measurement. Our analyses indicate that n can be determined to an accuracy of better than a part in 10^4, and k can be measured to better than ±5 x 10^{-5}, absolute.

- Completed rewriting FORTRAN codes, developed earlier for compound semiconductors, to model the IR response of the silicon wafer in the 400 cm^{-1} to 4000 cm^{-1} region. The model takes into account the absorption by the Si lattice, free carriers, and the interstitial oxygen. The model reproduces all the observed spectroscopic features, namely the multiphonon bands in the 400 cm^{-1} to 1050 cm^{-1} frequency region, the oxygen absorption at 1107 cm^{-1} and, most notably, the large, monotonic low frequency dip in the transmission due to the free carriers. A complete set of 11 samples with resistivities ranging from 0.3 Ω-cm to 10 Ω-cm (p-type) and 0.02 Ω-cm to 3 Ω-cm (n-type) was obtained. Virginia Semiconductors polished these wafers on both sides for optical measurements. The transmission of the medium resistivity wafers was measured and the response was modeled satisfactorily using the above-mentioned procedure for all but the 0.02 Ω-cm (n-type) wafer. The medium resistivity wafers are essential to validate the model calculations. The predictions of the model for heavily doped wafers ($\rho <$ 0.01 Ω-cm) indicate reflectivity changes of less than 1 part in 10^4, which strongly suggests the need for specialized measurement procedures for the heavily doped wafers.

- Completed 10K photoluminescence (PL) measurements on nanostructures (stripes and squares) produced using the focused ion beam (FIB) system. Both the degree of FIB damage and the effects of confinement were evident in the PL spectra. The initial results were presented at the Fall MRS conference in Boston, MA. We completed initial room-temperature cathodoluminescence (CL) measurements on the above samples. The width of the FIB lines, variations in its width, and possible process-induced damage were evident in the CL images. The CL measurements were performed in collaboration with Wen Tseng from the Materials Technology Group and Phillip Boyd and Donna Advena from the U.S. Army Research Laboratory, Adelphi, Maryland.

- Completed 12K photoluminescence and 295K photoreflectance measurements on a set of

eight MBE-grown $Al_{1-x}Ga_xAs$ samples with $0 \leq x \leq 0.4$. The precision in measuring x from the optical spectra was ± 0.0007 for both PL and PR, but the absolute x value could be established to only ± 0.0015 mainly due to the effects of doping on near band edge absorption.

- Critical review and compilation of published data to date are being prepared for publication in the Journal of Physical and Chemical Reference Data.

FY Deliverables

Collaborations

EEEL, Optoelectronics Division, K. Berteness; MSEL, Ceramics Division, L. Robbins; and CSTL, Surface and Microanalysis Science Division, J. Armstrong, compound semiconductor standards, supported by ATP, FY98-FY00 (P. Amirtharaj)

PL, Optical Technology Division, L. Hanssen, nondestructive and contactless infrared diagnostic methodology for semiconductor manufacturing, supported by ATP, FY98-FY00 (P. Amirtharaj)

CSTL, Process Measurements Division, J. Maslar, contactless and nondestructive optical methodology for quantifying oxygen in heavily doped silicon, supported by OMP, FY99-FY00 (P. Amirtharaj)

Army Night Vision Labs, characterization of infrared detector materials (P. Amirtharaj)

SEMATECH, FTIR analyses of partially annealed IC-Si wafers (P. Amirtharaj)

Bio-Rad, K. Krishman, oxygen metrology in doped Si wafers (P. Amirtharaj)

Publications

Balchin, G. A., Amirtharaj, P. M., Silvestre, C., and Thompson, P., Photoluminescence Quenching in $Si_{1-x}Ge_x/Si$ Multiple Quantum Wells Grown with Atomic Hydrogen, App. Phys. Lett. 85 (5), pp. 2875-2880 (1 March 1999).

Chandler-Horowitz, D., Amirtharaj, P. M., and Stoup, J. R., High-Resolution, High-Accuracy, Mid-IR ($450 < \omega < 4000$ cm^{-1}) Refractive Index Measurements in Silicon, Proceedings of the 1998 International Conference on Characterization and Metrology for ULSI Technology, Gaithersburg, Maryland, March 23-27, 1998, pp. 207-211.

Scanning-Probe Microscope Metrology

Technical Contact:
Joseph J. Kopanski

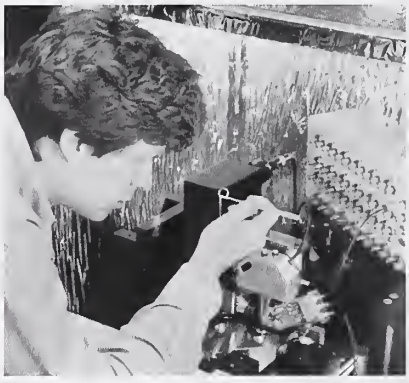
Staff-Years:
3.6 professionals

Funding Sources:
NIST (100%)

Parent Program:
Semiconductors, Silicon

Project Goals

Provide technological leadership to semiconductor and equipment manufacturers and other government agencies by developing and evaluating the methods, tools, and artifacts needed to apply scanning-probe microscopes (SPM) and other electrical characterization methods to semiconductor materials and processes. Provide silicon and compound semiconductor manufacturers with advanced scanning-probe electrical metrology techniques and models to improve device performance and reliability. A specific goal is to provide the technology computer-aided design (TCAD) community with quantitative two-dimensional dopant profiles to calibrate and enhance the predictivity of simulators.



Loading a sample into the Scanning Capacitance Microscope.

Customer Needs

The Semiconductor Industry Association's (SIA) International Technology Roadmap for Semiconductors identifies two- and three-dimensional carrier profiling as a key enabling technology for the development of next-generation integrated circuits. The goals in 1999 for 2-D carrier profiles are for a spatial resolution of 5 nm and a precision (in concentration) of 35%; these demands increase to less than 1 nm and 32% by 2015. The Scanning Capacitance Microscope (SCM) has emerged as the leading contender to provide 2-D carrier profiles.

While SCMs are commercially available, models to accurately interpret details of the SCM images have lagged. Much work remains to be done to develop robust three-dimensional physical models of SCM capable of extracting quantitative carrier profiles from SCM images. Likewise, the measurement methodology for quantitative SCM is still evolving. The need for, and form of, standard reference materials for SCM have yet to be defined. Other SPM-based techniques for semiconductor metrology suffer similar problems - microscopes have been invented, but standard measurement and interpretation techniques are not available.

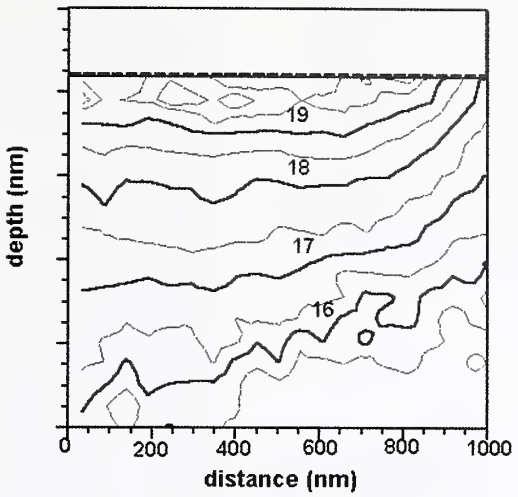
Technical Strategy

The current primary goal is to develop the measurement methodology, physically-based models, and interpretation formalisms to make SCM a practical metrology for 2-D carrier profiling of silicon. Best measurement practices are being determined via collaborative projects with industrial users and research into the physics of the silicon surface preparation. The focus of the Project's modeling effort has been to develop 2-D and 3-D finite-element solutions of Poisson's equation for the SCM geometry. The expertise of the Project with interpreting SCM images is being transferred to industry through the software program FASTC2D. The program features an easy to use interface, rapid profile extraction, and a Windows environment. Updates to the interpretation software will be available via the Internet in FY2000.

The project is also actively investigating other SPM-based characterization techniques. Project staff plan on extending the SCM carrier profiling capacity to SiC and III-V semiconductors. Intermittent-contact SCM is sensitive to variations in the dielectric constant of thin films and can detect metal layers buried beneath insulating films. Optically-pumped SCM is sensitive to variations in carrier lifetime. The scanning microwave microscope (SMWM) is of interest because it can provide both the real and imaginary parts of impedance at frequencies from dc to 50 GHz.

The first generation software utilizes a database of pre-calculated solutions that can very rapidly determine a 2-D carrier profile from an SCM image. When used in conjunction with SIMS measurements or a reference sample, relatively accurate profiles can be obtained. The FASTC2D software package will be available to users in Winter of 2000.

MILESTONE: By 2000, make SCM interpretation software based on a dopant gradient independent model available to industrial users.



Two-dimensional carrier profile of 50 keV boron implant into silicon extracted from SCM image using NIST's FASTC2D software.

"Two-Dimensional dopant profiling has been a highly ranked need in both the process integration and TCAD (simulation) sections of the National Technology Roadmap for Semiconductors (NTRS) since its inception."

Michael Duane, Advanced Micro Devices, Characterization and Metrology for ULSI Technology, p. 715.

Proper interpretation of carrier profiles of current interest to the integrated circuit industry will require consideration of the local dopant gradient. Project staff have estimated the magnitude of this effect through simulations. Project staff have also investigated experimentally and theoretically the effect of the p-n junction on the SCM signal, and they have developed techniques to help locate the p-n junction location in an SCM image.

MILESTONE: By 2001, release second-generation code that can correct for the effect of the local dopant gradient and the presence of p-n junctions.

An inverse solution of the SCM requires repeated solutions of the forward (calculate SCM signal from carrier profile) problem. The candidate carrier profile is adjusted until a carrier profile is found that makes the calculated SCM signal self-consistent with the measured SCM signal. Project staff have demonstrated the techniques necessary to do this with a 2-D solver. Project staff are currently investigating various 3-D solvers.

MILESTONE: By 2002, demonstrate inverse solutions of the SCM measurement.

Accomplishments

- Determined the magnitude of the dopant gradient effect on carrier profiles measured with the SCM. The first part of the study was a full simulation, using a knife-edge probe, of the SCM signal across a model dopant gradient. The second part compared the model dopant profile with the gradient independent profile extracted from the simulated signal using the FASTC2D approach. Project staff are now able to quantify how different tip radii and dopant gradients affect the accuracy of carrier profiles extracted using first generation models. Project staff found that the accuracy of first generation models depends on both the dopant gradient (dN/dx) and the dopant curvature (d^2N/dx^2). This insight will eventually yield a better inverse solution of the SCM. Results were reported at Ultra-Shallow Junctions-99 (USJ-99) and are to appear in J. Vac. Sci. Technol. B, Jan. 2000.

- Modeled SCM data for a set of abrupt-transition p-n junctions with finite-element software. A combination of measurements and simulations were used to validate an expression for locating a p-n junction with the SCM and to suggest a method of extending the calibration curve method to samples containing p-n junctions.

- Imaged with SCM a set of 18 samples consisting of ion-implanted profiles and epilayers on both like-type and opposite-type substrates. A complete matrix of samples (n+ on n, n+ on p, p+ on n, and p+ on p) with high-to-low dopant gradients of 10, 100, and 1000 was available. The unique range in dopant gradient of these "known" samples allowed measurement of the dopant gradient and p-n junction effects that have been simulated. Results were reported at USJ-99 and are to appear in J. Vac. Sci. Technol. B, Jan. 2000.

- Dr. Duncan McBride of the NSF joined the project as a COM-SCI Fellow for 1999. Dr. McBride conducted a study of "enhanced" native oxides on silicon for use as the insulating layer in SCM measurements. Surface preparation conditions at 200 °C to 350 °C, for 0.5 h to 8 h, with and without UV light, as well as an ultraviolet ozone photoreactor were investigated. The oxides were characterized by measuring dC versus V curves with the SCM, traditional C-V measurements with a Hg-probe, and ellipsometric measurement of oxide thickness. Project staff can readily produce SCM samples with "enhanced" native oxides of sufficient quality to support SCM measurements of carrier profiles. These oxides have a thickness of about 1.5 nm and are clearly in the regime where quantum mechanical (QM) effects must be considered.

- Coding of core functions of FASTC2D was completed. The Project's SCM signal extraction algorithm was re-written to include the effect of

the high frequency voltage. The tip model has been extended to include both a flat and curved region. The utility of the extended model has been investigated on the sample profiles presented at USJ-99. Two-dimensional data conversion and display have been coded and tested. An interactive help function has been added. An installable version of the code for WINDOWS 9x and NT has been tested.

- A talk entitled, "SCM Imaging Conditions that Assure Reliable Conversion to Carrier Profiles," was presented at the SEMATECH Dopant Profiling Working Group at INTEL in December 1998.

- A DoC SBIR grant has been made to Atolytics, Inc. in State College, PA to develop their Scanning Microwave Microscope (SMWM). The goals of phase I are to demonstrate both 1-D (surface into depth) and 2-D (x-y scanned) carrier profiling with the SMWM.

FY Deliverables

Collaborations

Los Alamos National Laboratories (LANL), collaboration that will provide access to the LaGriT three-dimensional finite-element code. Jay Marchiando visited David Cartwright and Denise George at LANL. Implementation of a Poisson solver with this code will enable full three-dimensional simulations of the SCM. Such results will be critical for 2nd generation models of the SCM necessary to meet future ITRS goals for carrier profiling.

ThermoMicroscopes Inc., collaboration to develop SCM calibration test structures (J. Kopanski)

Software

Development of the first generation of FASTC2D (2-D SCM Image-to-Carrier Profile software) was completed (J. Kopanski, B. Rennex, and J. Marchiando)

External Recognition

J. Kopanski was invited to present talks to the SEMATECH working group on dopant profiling at INTEL in December and at NIST in March.

Publications

Kopanski, J. J., Marchiando, J. F., Albers, J., and Rennex, B. G., Comparison of Measured and Modeled Scanning Capacitance Microscopy Images Across P-N Junctions, Proceedings of the 1998 International Conference on Characterization and Metrology for ULSI Technology, Gaithersburg, Maryland, March 23-27, 1998, pp. 725-729.

Kopanski, J. J., Marchiando, J. F., and Rennex, B. G., Carrier Concentration Profile Dependence of Scanning Capacitance Microscopy Signal in the Vicinity of p-n Junctions, Proceedings of the Fifth International Workshop on the Measurement, Characterization, and Modeling of Ultra-Shallow Doping Profiles in Semiconductors, at Research Triangle Park, NC, March 28-31, 1999, p. 202.

Marchiando, J. F., Kopanski, J. J., and Albers, J., Limitations of the Calibration Curve Method for Determining Dopant Profiles from Scanning Capacitance Microscope Measurements, Proceedings of the Fifth International Workshop on the Measurement, Characterization, and Modeling of Ultra-Shallow Doping Profiles in Semiconductors, at Research Triangle Park, NC, March 28-31, 1999, pp. 461-463.

Mayo, S., Kopanski, J. J., and Guthrie, W. F., Intermittent-Contact Scanning Capacitance Microscopy Imaging and Modeling for Overlay Metrology, Proceedings of the 1998 International Conference on Characterization and Metrology for ULSI Technology, Gaithersburg, Maryland, March 23-27, 1998, pp. 567-572.

Ukraintsev, V. A., List, R. S., Chang, M.-C., Edward H., Machala, C. F., Martin, R. S., Zavyalov, V., McMurray, J. S., Williams, C. C., De Wolf, P., Vandervorst, W., Venables, D., Neogi, S. S., Ottaviani, D. L., Kopanski, J. J., Marchiando, J. F., Rennex, B. G., Nxumalo, J. N., Li, Y., and Thomson, D. J., Dopant Characterization Round-Robin Study Performed on Two-Dimensional Test Structures Fabricated at Texas Instruments, Proceedings of the 1998 International Conference on Characterization and Metrology for ULSI Technology, Gaithersburg, Maryland, March 23-27, 1998, pp. 741-745.

Thin-Film Process Metrology

Technical Contact:
James R. Ehrstein

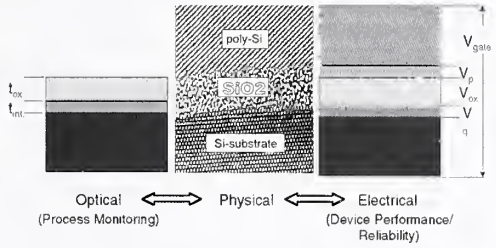
Staff-Years:
2.9 professionals
2.0 technicians

Funding Sources:
NIST (94%)
Other Government Agencies (6%)

Parent Program:
Semiconductors, Silicon

Project Goals

Develop new and improved electrical and optical measurements, models, data, and reference materials to enable better and more accurate measurements of select critical silicon Complementary Metal Oxide Semiconductor (CMOS) technology thin-film parameters. Major focus is placed on requirements for silicon dioxide, oxynitrides, and gate stacks for advanced gate dielectrics detailed in the 1999 International Technical Roadmap for Semiconductors (ITRS).



A cross section of an advanced gate-oxide structure probed by HRTEM and schematic representations of that gate structure as "seen" by optical process monitor measurements and by device electrical measurements.

Customer Needs

Ellipsometry will continue to be the leading method for film thickness and composition metrology.

National Technology Roadmap for Semiconductors

The evolving decrease of the gate dielectric film thickness to an oxide-equivalent value of 1 nm is identified as a critical front-end technology issue in the ITRS (1999). For effective gate dielectric thicknesses below ≈ 2.0 nm, SiO_2 is expected to be replaced, initially by stacks utilizing silicon oxides and nitrides, and then by either metal oxides or silicates. Process control tolerance needs for dielectric thickness are projected to be ±4 % (3σ), which translates to less than 0.1 nm for 2 nm films. Requirements for process control measurements are a factor of ten smaller still.

Spectroscopic ellipsometry is expected to continue as the preferred measurement for process monitoring of future gate dielectric films. Industry metrology needs not only include improved methods to accurately determine film thickness, but also include (1) techniques to determine the structure of the individual films and the interfaces between them, (2) an improved understanding of the relationship between physical, electrical, and optical determinations of film properties, and (3) mechanisms for traceability to NIST (such as reference materials) to support film metrology.

In order for SE to meet process control requirements of film thickness and unambiguously determine film composition and morphology, the optical properties of these advanced dielectric film systems must be characterized.

Technical Strategy

This project focuses on the issues of (1) relating optical, electrical, and physical measurements of thickness, composition, and interface structure, (2) developing and providing the basis for traceability to NIST for film thickness measurements, and (3) identifying structural models and developing preferred optical index dispersion models or data for improved ellipsometric analysis of future-generation gate dielectric film systems.

Relation between optical, electrical and physical measurements of thickness - Through collaborations with SEMATECH, IC industry companies, and SRC university staff, as well as with key researchers in other parts of NIST, Project staff are leading and participating in a number of multimethod comparison studies of various ultra thin gate dielectric films. These multimethod studies utilize techniques such as X-ray and neutron reflectivity, high resolution TEM, angle-resolved XPS, SIMS, C-V and I-V analysis as well as spectroscopic ellipsometry and reflectivity. The results of these multimethod studies improve the general understanding of state of the art (SOA) measurement capability for very thin films, and also allow Project staff to assess the results of various optical models being applied to the analysis of these films. SOA C-V and I-V measurement capability for gate films has been established in the project. Advanced analysis software from commercial and university sources is being established and benchmarked to determine the effect of model sophistication on film thickness values calculated from C-V and I-V data. An *in-situ* two-terminal electrical evaluation technique for buried interface roughness is being extended to 0.25 μm MOSFETs and beyond.

MILESTONE: By 2000, identify preferred advanced electrical analysis software and use to improve agreement between electrical and ellipsometric thickness scales.

The development of innovative optical models that correlate with electrical measurements are especially needed as film thicknesses shrink below 2 nm.

National Technology Roadmap for Semiconductors

Establish and transfer basis of accuracy for thin dielectric films - Industry requirements for future thin dielectric film optical measurements and calibration standards were identified at a NIST sponsored workshop in FY 98. Core ellipsometry measurement capability is being expanded and strengthened to meet these requirements. An investigation has been started into cleaning and recontamination issues for film calibration standards to determine whether a workshop-expressed goal of 0.015 nm long-term reproducibility of reference artifact values is obtainable. Procedures are being developed to enable traceability to NIST for suppliers of secondary thin-film reference materials without volume production of NIST SRMs.

MILESTONE: By 2001, transfer traceability to NIST to 1st Level commercial suppliers of Reference Materials for oxide films down to 2 nm.

Reference material, optical constants of one to two monolayers of gate dielectric materials, standard procedures, and optical models for non SiO_2 materials need to be developed.

National Technology Roadmap for Semiconductors

Structural and optical models for ellipsometry - A custom-built high-accuracy spectroscopic ellipsometer with a spectral range of 1.5-6 eV is being used for this Project, and Project staff are working with SEMATECH, IC industry companies, and SRC university staff to obtain and optically characterize advanced oxynitrides, oxide/nitride stacks, and metal oxide films such as tantalum pentoxide and titanium dioxide. This work is directed at determining preferred structural models, spectroscopic index of refraction values, or preferred optical dispersion models for each of these film systems, and, where possible, the variability of these parameters due to differences in film fabrication processes. Analysis is done with software developed by NIST for spectroscopic ellipsometry; this software allows maximum flexibility for addition of the latest published or custom-developed optical response models as appropriate for each material system investigated.

MILESTONE: By 2002, establish preferred process-monitor capable ellipsometric models and analyses for stable-process replacement gate dielectric materials.

Accomplishments

- Showed, for a series of expected oxide/nitride/oxide stacks in the 3 nm to 4 nm thickness range, that there was no optical evidence of a Si_3/N_4 layer. These films were best modeled as effective single-layer films using a Sellmeier dispersion for the index of refraction. The film thicknesses by ellipsometry were in the same relative order as determined by X-ray diffraction and SIMS, although the differences in absolute thicknesses by these techniques ranged from 0.1 nm to 0.3 nm. Relative nitrogen content, as determined by the index of refraction, was in the same relative order as determined by SIMS and XPS.

- Determined for a series of amorphous, low temperature annealed, Ta_2O_5 (high-k) films over a silicon oxide transition layer that a Tauc-Lorentz dispersion provides a good fit of the index of refraction, and that the optical gap for these films is 4.1 eV. Project staff showed that the variation in the value of the index of refraction among these films is strongly related to the film quality due to different anneal cycles, and to the thickness of the silicon oxide interlayer, as determined by TEM. Project staff also found that while high temperature annealed, polycrystalline Ta_2O_5 films are not well described by the Tauc-Lorentz dispersion, it is readily evident from the ellipsometric data in the 4 eV to 6 eV range, whether the films are amorphous or polycrystalline.

- Designed and initiated a multi-laboratory comparison study of the thickness of very thin SiO_2 films using spectroscopic ellipsometry, X-ray and neutron reflectivity, and C-V measurements. A thermal desorption cleaning process just prior to measurement was required for all participating laboratories. This procedure was based on results obtained during initial studies at NIST on the effectiveness of a variety of cleaning procedures.

- Initiated the process of adding spectroscopic capability to the master high-accuracy ellipsometer that is used for Reference Material and traceability activities. Prior to the completion of that upgrade, we are evaluating a hybrid process for establishing traceability to NIST for spectroscopic measurements in conjunction with VLSI Standards Inc. This activity focuses on spectroscopic measurements of silicon nitride films, and will be based on comparison of spectroscopic measurements at VLSI Standards and at NIST, done on a separate research spectroscopic ellipsometer. In addition, measurements at 632.8 nm on the NIST master ellipsometer will be compared with values at 632.8 nm extracted from data of the two spectroscopic instruments. Two wafers at each of three film thicknesses will be exchanged three times to complete this evaluation.

- Acquired, installed, and determined the operating capabilities of six different sets of advanced university and commercial sector

software capable of accounting for polysilicon depletion and quantum mechanical effects that obscure the determination of thickness of thin dielectric films from C-V and I-V measurements. The relative performance of these software sets, which have various levels of sophistication, will be determined by comparing results for a model capacitor test structure having a range of polysilicon and substrate doping levels, as well as oxide thicknesses. It is necessary to understand the role of advanced analysis software in order to improve the understanding of electrical versus optical measurement of thin dielectric film thickness.

- Demonstrated that Weak Localization can be applied to measuring interface roughness down to 0.1 nm for 0.25 μm technology node structures.

FY Deliverables

SRMs

Issued SRM 2543 for Silicon Resistivity (J. Ehrstein and D. Ricks)

Collaborations

VLSI Standards (Prabha Durgapal) comparative spectroscopic and single-wavelength ellipsometry measurements on Si_3N_4 thin films (B. Belzer, N. Nguyen, and J. Ehrstein)

Atomic Physics Division (R. Deslattes), Polymers Division (W. L. Wu), and NIST Center for Neutron Research (J. Dura), Bede Scientific, Four-Dimensions Inc., J. A. Woollam Co., KLA-Tencor, n and k Technology Inc., NC State Univ., Oak Ridge Nat. Labs, Rudolph Technologies, Solid State Measurements Inc., and Therma-Wave, Inc. multi-method comparison of very thin SiO_2 on Si (co-organized with Rutgers University) (J. Ehrstein, C. Richter)

SEMATECH (A. Diebold), NCSU (D. Venables and D. Maher), and KLA-Tencor Corporation (C. Hayzelden), metrology for ultra-thin oxides, gate stacks and high-k dielectric materials (J. Ehrstein, C. Richter and N. Nguyen)

SEMATECH (A. Diebold and D. Brady), Lucent Technologies (R. Opila), and Div. 842 (R. Deslattes), study of oxynitride ultra thin films (C. Richter, N. Nguyen)

NIST Center for Neutron Research (J. Dura), spectroscopic ellipsometry, neutron reflectivity, and X-ray reflectivity measurement comparison for thin SiO_2 on Si (C. Richter, N. Nguyen)

Lucent Technologies (Glenn B. Alers) and SEMATECH (H. Huff and M. Gilmer), optical properties of Ta_2O_5 for use as a gate dielectric (N. Nguyen, C. Richter)

Jet Process Corporation (T. Tamagawa) and Yale Univ. (Prof. T. P. Ma), electrical and optical properties of jet vapor deposited high-k gate dielectrics (C. Richter, N. Nguyen)

U. Texas at Austin (Prof. J. Lee), optical properties of ZrO_2 and HfO_2 for use as high-k gate dielectrics (C. Richter, N. Nguyen)

Texas Instruments (G. Brown), ASTM, JEDEC, electrical and reliability characterization of ultra-thin gate oxides (J. Suehle, C. Richter)

Polymers Division (W. Wu), X-ray and optical study of low-K "spin-on" dielectric films (N. Nguyen)

SEMATECH/U. Texas at Austin (A. Diebold and J. Canterbury), spectroscopic ellipsometry analysis of oxynitrides (C. Richter, N. Nguyen)

Semiconductor Electronics Division (D. Gajewski and J. Pellegrino), *ex-situ* and *in-situ* characterization of AlGaAs films and surface oxidation (N. Nguyen)

COMPAQ, silicon interface property measurements (C. Richter)

Lucent Technologies (S. Martin), correlation of interface roughness and device noise (C. Richter)

Standards Committee Participation

ASTM F-1 on Electronics, Subcommittee F1.06, Section B on Thin Film Characterization, Leader, FY 97-99 (J. Ehrstein)

ASTM F-1 on Electronics, Subcommittee F6 on Silicon Materials and Process Control, co-chair, FY 97-99 (J. Ehrstein)

ASTM Committee F-1 on Electronics, Executive Committee, FY 97-99 (J. Ehrstein)

Software

Development of a second generation modeling and analysis program for spectroscopic ellipsometry: Spectroscopic Ellipsometry Studio V.2, Semiconductor Electronics Division. Copies distributed for evaluation and use to VLSI Standards Inc., SEMATECH, Gaertner Instruments, Penn State Univ.

External Recognition

Curt Richter was invited to co-organize a Symposium on Ultrathin SiO_2 and High-k Materials for ULSI Gate Dielectrics in conjunction with the Spring 1999 general meeting of the Materials Research Society.

Publications

Dura, J. A., Richter, C. A., Majkrzak, C. F., and Nguyen, N. V., Neutron Reflectometry, X-Ray Reflectometry, and Spectroscopic Ellipsometry Characterization of Thin SiO_2 on Si, App. Phys. Lett. 73 (15), 2131-2133 (12 October 1998).

Durgapal, P., Ehrstein, J. R., and Nguyen, N. V., Thin-Film Ellipsometry Metrology, Proceedings of the 1998 International Conference on Characterization and Metrology for ULSI Technology, Gaithersburg, Maryland, March 23-27, 1998, pp. 121-131.

Ehrstein, J. R., and Croarkin, M. C., NIST Special Publication 260-131, Standard Reference Materials: The Certification of 100 mm Diameter Silicon Resistivity SRMs 2541 through 2547 Using Dual-Configuration Four-Point Measurements, Revised June 1999.

Huff, H. R., Richter, C. A., Green, M. L., Lucovsky, G., and Hattori, T., eds., Ultrathin SiO_2 and High-k Materials for ULSI Gate Dielectrics, Mater. Res. Soc. Proc., Vol. 567, Pittsburgh, September 1999, 615 p.

Richter, C. A., Nguyen, N. V., and Alers, G. B., Spectroscopic Ellipsometry of Ta_2O_5 On Si, in Ultrathin SiO_2

and High-k Materials for ULSI Gate Dielectrics, edited by H. R. Huff, C. A. Richter, M. L. Green, G. Lucovsky, and T. Hattori, Mater. Res. Soc. Proc., Vol. 567, Pittsburgh, September 1999, pp. 559-566.

Richter, C. A., Nguyen, N. V., Dura, J. A., and Majkrzak, C. F., Characterization of Thin $Si0_2$ on Si by Spectroscopic Ellipsometry, Neutron Reflectometry, and X-Ray Reflectometry, Proceedings of the 1998 International Conference on Characterization and Metrology for ULSI Technology, Gaithersburg, Maryland, March 23-27, 1998, pp. 185-189.

Metrology for Simulation and Computer-Aided Design

Technical Contact:
Allen R. Hefner, Jr.

Staff-Years:
4.5 professionals
2.0 guest researchers

Funding Sources:
NIST (98%)
Other Government Agencies (2%)

Parent Program:
Semiconductors, Silicon

The National Research Council (NRC) Workshop on Modeling and Simulation Opportunities in Manufacturing identified the process of model validation and accreditation as an issue to be addressed in developing a national research agenda for modeling and simulation.

Project Goals

The goal of the project is to facilitate the efficient and reliable application of semiconductor computer-aided design (CAD) tools by providing leadership for the development of an industry infrastructure for establishing model accuracy, developing methods for simulator model validation and benchmarking, developing metrology necessary for providing model data and model parameter extraction sequences, and developing models and techniques necessary for advanced device, process, package, and system simulation.

Test system used for IGBT parameter extraction and model validation.

Customer Needs

Efficient and reliable simulation methods are becoming more important as device structures and packages rapidly evolve. In addition, higher speed and higher power devices increase the importance of including the effects of packages in system performance simulation. However, advanced device electrical and thermal characterization procedures and validation of models used in computer-aided design tools have not kept pace with the application of the new device types and processes.

Several device technologies have evolved to an extent that conventional modeling and simulation capabilities are not suitable. For example, as CMOS devices are scaled to atomic dimensions, simulators must include quantum mechanical physics. The SRC/NIST/NSF Workshop on Nanoscale Transistors: Technology, Physics, and Simulation (Feb. 1999) identified quantum mechanical device simulation as an area required for device simulator progress. In addition, the device types used for power and microwave applications can no longer be represented by conventional device models provided in circuit and system simulation programs.

Technical Strategy

NIST addresses these needs by developing the theoretical foundations, standards, model validation procedures, and associated experimental techniques for the measurement of device electrical and thermal characteristics, and package electrical and thermal characteristics. NIST is developing, with industry, accepted procedures for validating device models for circuit simulation. NIST is developing procedures for characterizing the thermal and electrical performance of micro-electronic packages that are compatible and useful for CAD of boards and systems.

Device and Process Simulation Benchmarking - Accurate models and benchmarking procedures are becoming more important for device and process simulators. Current tasks include development of mobility, band gap, and intrinsic carrier concentration models for accurate simulation of compound semiconductor devices, and collaboration with the Scanning Capacitance Microscopy Project to validate process simulators for ultra-shallow junctions.

MILESTONE: By FY 2000, complete benchmarking of semiconductor device simulation tools that include quantum mechanical effects including: MEDICI, UTQuant, NCSU code, and NEMO.

Compact Package Electrical Interconnect Models - Interconnect structures are becoming a dominant factor in limiting the performance of modern computer, communication, and power systems. The Time-Domain Reflectometry (TDR) technique is being applied to characterize various multi-chip module and discrete packages interconnect systems.

MILESTONE: By FY 2001, develop a TDR test system with low source impedance (10 Ω), and characterize low-impedance interconnects used in microprocessor voltage regulator modules, advanced memory busses, and power electronic systems.

The International Technology Roadmap for Semiconductor (ITRS) identifies modeling and simulation as cross-cutting technologies, and the availability of calibrated and easy-to-use technology computer-aided-design tools for device, process, and circuit simulation as areas requiring development and support to achieve the 15-year goals of the Roadmap. The ITRS also states that using accurate computer models shortens time scales, lowers costs, and increases quality of each technology area.

Package Thermal Metrology and Models - Accurate and timely simulation of system thermal performance requires new temperature measurement methods, new simulation methodologies, and validation procedures. Current tasks include the NIST electro-thermal network simulation methodology, including thermal network component models for semiconductor packages and heatsinks, and development of methodologies to validate the performance and accuracy of compact package thermal models.

Compact Device Electrical Models - Only recently has there been a significant effort in developing an infrastructure for validating the performance of compact models. An example of this activity is the NIST/IEEE Model Validation Working Group, founded in 1994 and now having over 200 members from 100 different technical organizations. For more information see http://ray.eeel.nist.gov/modval.html.

MILESTONE: By FY 2002, develop test system and models for SiC three terminal device.

Accomplishments

- Provided leadership in developing a national agenda for modeling and simulation. Hefner presented an invited talk entitled, "Model Verification, Validation, and Accreditation of Semiconductor Device CAD Systems," at the National Academy of Science, National Research Council Workshop on Modeling and Simulation Opportunities in Manufacturing, April 26-27, 1999. The talk described the methodology for model validation being applied by the NIST/IEEE Working Group on Model Validation. The objective of the workshop was to develop a prospectus for a study that will recommend a national research agenda to address shortcomings in current modeling and simulation capabilities and to develop enhanced opportunities for coupling modeling and simulation with manufacturing.

- Impact study published on NIST models. An assessment of the U.S. economic impacts of the NIST IGBT model is detailed in a recent study entitled NIST Planning Report 99-3: Benefit Analysis of IGBT Power Device Simulation, prepared by M. Gallaher and S. Martin, Research Triangle Institute Center for Economic Research (April 1999). The press release announcing this study appeared in the front page of the NIST web site, appeared in the NIST Update, and was highlighted in the NIST directors State-of-the-Institute (also in NIST Connections article entitled "NIST Measuring Up, Kammer Says"). The economic impact study quantified the direct impacts of the NIST IGBT modeling at $18M (30 times the cost of the NIST program) and the indirect benefits at $40 M/year largely due to energy savings.

- NIST interconnect metrology proves valuable for EMI simulation. Models obtained from recent interconnect metrology research at NIST enabled the simulation of the EMI performance of various power converter topologies, as described in two NIST publications. In recent years, Electro-Magnetic-Interference (EMI) considerations have become increasingly important as Electro-Magnetic-Compatibility (EMC) regulations have become more stringent. The NIST metrology provides, for the first time, the capability to use simulation in the design of power converters with reduced EMI emissions.

- Developed IGBT model validation procedures and applied to component library. Developed circuits and measurement methods for validating IGBT models for soft-switching conditions, applied the methods to models provided in a software vendors component library, and published results. Enhancements were made to the Hefner IGBT model that is provided in commercial circuit simulators as a result of this validation work. The NIST IGBT model was then used to simulate IGBT soft-switching performance in two papers; one describing reduced EMI emissions for soft-switched inverters, and the other describing the difference in soft-switching performance between different IGBT types.

- Developed High-Speed Semiconductor Device Transient Thermal Imaging System. The system provides the capability to measure the transient temperature distributions on the surface of a silicon chip with 100 ns temporal, 15 μm spatial resolution. The system uses computer-control software with a graphical user interface for controlling the translation stages, digitizing oscilloscope, and device test fixture temperature controller. The system also required the development of algorithms for calibrating and extracting transient temperature waveform from an infrared microscope signal.

- Developed Capability to Characterize and Predict IGBT Dynamic Failures. The dynamic failure characteristics and avalanche-sustaining capability of various IGBT types, including new high-energy capable IGBTs, were measured

A recent Benefit Analysis Study by the Research Triangle Institute identified areas where NIST future involvement could significantly increase benefit: supporting enhancements to IGBT model, developing extraction tool/procedure eliminating need for structure data, and supporting model development of other classes of devices identified as weak links in modeling chain.

Benefit Analysis of IGBT, Research Triangle Institute Modeling, 1999

using the unique NIST nondestructive failure tester and simulated using the NIST IGBT model. The measurements and simulations enabled the prediction of the mechanism resulting in High Avalanche Energy IGBTs and demonstrated the capability of the NIST IGBT model to predict the sustaining time and conditions for failure of both high-energy and conventional IGBT types.

- Developed Software Package for IGBT Model Parameter Extraction (IMPACT). The software consists of five programs, LINMSR, SATMSR, LFTMSR, BTAMSR, and CVMSR, that extract the 20 physical and structural parameters of the most recent version of the NIST IGBT model. The programs have a graphical user interface, use the IEEE 488 bus to control the measurement instruments and collect data, and use various algorithms for fitting the IGBT model equations to the data. The new software package will facilitate the development of IGBT component libraries and enable end users of the simulation software products to extract model parameters themselves.

- Plasma doping meeting organized by NIST-sponsored Ion Implant Users Group. Albers spearheaded the planning and organization of the First Joint Ion Implant Users Group / Plasma Doping Users Group Meeting held on Thursday, April 22, 1999 at the Peabody Marriott, Peabody, MA, USA. The primary topic for the meeting was Plasma Doping, which is an up-and-coming doping technology that will be providing the ultra-shallow junctions envisioned in the ITRS Roadmap.

- SRC/NIST/NSF Workshop held at NIST. The Workshop, "Research Issues and Directions for Nanotransistors: Technology, Physics, and Simulation," was attended by over 50 researchers from industry, academia, and government. The Workshop identified critical modeling and simulation issues, such as quantum effects, that must be solved if modeling and simulation is to have a significant impact on the development of future nano-transistors. Modeling and simulation can speed progress in the development of future transistors if the infrastructure and physics are in place to attack relevant problems.

FY Deliverables

Collaborations

SCM Project and Analytical Chemistry Division, metrology and benchmarking of simulators for ultra-shallow junctions (A. Hefner)

MEMS Project, compact modeling of MEMS devices from CIF files (A. Hefner)

Thin-Film Process Metrology Project and Gate Dielectric and Interconnect Reliability Project, benchmarking quantum-mechanical device simulation (A. Hefner)

Electricity Division, development of low-characteristic impedance time domain reflectometry (A. Hefner)

Analogy and IR, development of IGBT and thermal model component library (A. Hefner)

Analogy and POWERX, development of high power IGBT module component library (A. Hefner)

Harris Semiconductor, development of component models for Harris IGBTs (A. Hefner)

General Electric CRD, development of IGBT module parameter extraction tools (A. Hefner)

CREE, development of SiC MPS-diode electro-thermal model (A. Hefner)

Rockwell Science Center, development of SiC transistor models (A. Hefner)

University of Maryland, Reliability Physics Department, IGBT dynamic failure (A. Hefner)

Virginia Tech., eleetrical characterization of power module and system interconnects (A. Hefner)

NIST ITL, regression analyses of electron mobility model for p-type AlGaAs (H. Bennett)

Semiconductor Research Corporation (SRC), Blackburn assigned as SRC Director for Advanced Devices and Technology (D. Blackburn)

NIST Center for Building and Fire Research, Heat Flux Metrology Competence, modeling of conduction heat flux gauge calibration fixture (D. Blackburn)

Standards Committee Participation

EIA/SEMATECH Compact Model Council, FY 96-99 (A. Hefner)

IEEE Electron Devices Society, Standards Technical Committee, Chairman, FY 96-99 (A. Hefner)

Software

Copies of the RESPAC (NIST SP 400-91) and HOTPAC (NIST SP 400-96) software packages have been distributed (J. Albers)

Copies of NIST IGBT Simulation Software INSTANT and Saber IGBT model template were distributed (A. Hefner)

External Recognition

J. Albers received, in April 1999, an award from Eaton and Varian, the two primary U.S. ion implanter manufacturers, citing, "In appreciation for your continued commitment and support to the East Coast Implant Users Group and the ion implant community."

Publications

Bennett, H. S., High Dopant and Carrier Concentration Effects in Gallium Aluminum Arsenide: Band Structure, Effective Carrier Concentrations, and Mobilities, published in the Proceedings of the International Conference on Surfaces and Interfaces of Mesoscopic Devices, Maui, Hawaii, December 8-13, 1997.

Bennett, H. S., Viewpoint: Roadmaps for Compound Semiconductors: Knowledge-Based Investments for Next Century, IEEE Spectrum, pp. 54-55 (January 1999).

Bennett, H. S., Pellegrino, J. G., Rode, D. L., Shaffner, T. J., and Seiler, D. G., Do We Need a Roadmap?, Compound Semiconduc. 5 (3), pp. 43-44 (April 1999).

Bennett, H. S., Snowden, C., and Atta, R. V., Are Coordinated Roadmaps for Compound Semiconductor Based Technologies Needed? A Proposal for Smarter Investments, in the book "Future Trends in Microelectronics: The Road Ahead," John Wiley and Sons, Inc., New York, pp. 369-379, July 1999.

Bennett, H. S., and Turton, R. J., For EMIS/INSPEC of IEEE Data Review Series on Silicon 7.5 Indirect Energy Gap of Si, Doping Dependence, EMIS Data Review, pp. 54-55 (January 1999).

Berning, D. W., and Hefner, Jr., A. R., IGBT Model Validation, IEEE Industry Application Magazine, (4) 6, pp. 23-34 (November/December 1998).

Blackburn, D. L., Semiconductor Device Temperature Measurements Using Electrical Parameters, Future Circuits International, Volume 4, Technology Publishing Limited, London, pp. 75-83 (December 1998).

Kopanski, J. J., Blackburn, D. L., Harman, G. G., and Berning, D. W, Assessment of Reliability Concerns for Wide-Temperature Operation of Semiconductor Devices and Circuits, Proceedings of the IEEE Components, Packaging, and Manufacturing Technology Society, pp. 77-82.

Kopanski, J. J., Marchiando, J. F., Albers, J., and Rennex, B. G., Comparison of Measured and Modeled Scanning Capacitance Microscopy Images Across P-N Junctions, Proceedings of the 1998 International Conference on Characterization and Metrology for ULSI Technology, Gaithersburg, Maryland, March 23-27, 1998, pp. 725-729.

Marchiando, J. F., Kopanski, J. J., and Albers, J., Limitations of the Calibration Curve Method for Determining Dopant Profiles from Scanning Capacitance Microscope Measurements, Proceedings of the Fifth International Workshop on the Measurement, Characterization, and Modeling of Ultra-Shallow Doping Profiles in Semiconductors, at Research Triangle Park, NC, March 28-31, 1999, pp. 461-463.

Shen, C.-C., Hefner, Jr., A. R., Berning, D. W., and Bernstein, J. B., Failure Dynamics of the IGBT During Turn-Off for Unclamped Inductive Loading Conditions, in the Conferenee Proceedings of the 1998 IEEE Industry Applications Society Meeting, St. Louis, Missouri, October 12-16, 1998, pp. 831-839.

Zhu, H., Hefner, Jr., A. R., and Lai, J., Characterization of Power Electronics System Interconnect Parasitics Using Time Domain Reflectometry, in IEEE Transactions on Power Electronics, p. 622, vol. 14, July 1999.

Zhu, H., Lai, J.-S., Tang, Y., Hefner, Jr., A. R., and Chen, C., Analysis of Conducted EMI Emissions from PWM Inverters Based on Empirical Models and Comparative Experiments, in Proceedings of 1999 Annual Power Electronics Specialist Conference, p. 861 (June 1999).

"The NIST IGBT model is internationally accepted as the standard by which other IGBT models are compared."

Benefit Analysis of IGBT, Research Triangle Institute Modeling, 1999

MicroElectroMechanical Systems (MEMS)

Technical Contact:
Michael Gaitan

Staff-Years:
2.0 professionals
11.0 guest researchers

Funding Sources:
NIST (87%)
Other Government Agencies (13%)

Parent Program:
Semiconductors, Silicon

"... Standardization of test methods such as residual stress and elastic modulus will save manufacturers time and money."

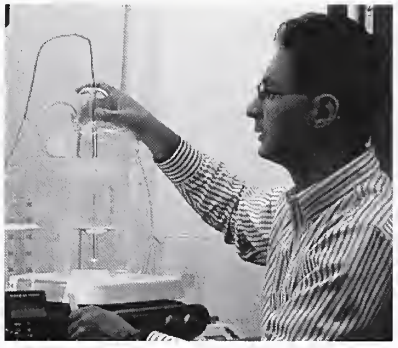
Nicholas Swart, Analog Devices

"Janet Marshall and others in the MEMS program at NIST are an integral part of the core group of the ASTM standardization effort. Through their involvement, NIST plays crucial role in the development of standards and shapes the future of the MEMS industry in the United States."

Chris Muhlstein, ASTM Committee

Project Goals

Provide domestic industry with MEMS-based test structures and standardized test methods for characterizing the thermo-electro-mechanical properties of thin films used in integrated circuit (IC) and MEMS technologies. Work with IC foundries to develop measurement infrastructure for improved system-on-a-chip manufacturing. Research and develop novel metrology applications of MEMS technology.



Silicon micromachining CMOS ICs using TMAH anisotrobic etchant.

Customer Needs

The MEMS project serves its customers in the following three areas: ITRS Roadmap, System-On-A-Chip, and Micro-Metrology Tools.

System-On-A-Chip

Manufacturers of MEMS products, such as air bag acceleration sensors for automotive exploders and deformable mirror displays, are mainstream U.S. IC companies. These products integrate electromechanical elements within the IC. This progress is part of the semiconductor industry's move towards "system-on-a-chip."

System-on-a-chip will link the functionality of the IC (information processor) with information gathering (sensing the environment) and actuation (changing the environment). System-on-a-chip ICs will include mixed-signal RF, MEMS, electro-optical, and micro-fluidic systems.

New test structures, test methods, and standards are required for improving device and reliability characterization. The Project's customers are MEMS IC manufacturers and government laboratories.

ITRS Roadmap

Increasing device density in integrated circuits leads to more interconnect layers with smaller cross-sectional area and higher aspect ratio; all of which increase the probability of failure by mechanisms such as electromigration, stress migration, and delamination. These reliability problems reside in the interconnect and dielectric layers of the IC. The interconnect and dielectric layers of an IC can be thought of as laminates of a multilayer film composite. The IC industry requires new measurement methods to characterize the mechanical strain in these multilayer films. Results can then be used to verify finite element models of the stress in the films and to correlate mechanical stress data with reliability testing. MEMS-based test structures being developed in this project offer new ways to characterize the mechanical stress in multilayer films.

Micro-Metrology Tools

Miniaturization technologies developed by the semiconductor industry such as thin-film deposition and growth, photolithography, etching, and micro machining are increasingly being used to make new metrology tools. Such tools can improve the way we presently measure things or create totally new ways to measure things. To this end, the Project's customers come from within the NIST laboratories and other government agencies to draw on the Project staff expertise in micro fabrication.

Technical Strategy

MEMS Test Structure Standardization - The MEMS technical community, composed of companies, universities, and government laboratories, has developed many types of test structures to characterize the fabrication process and device performance. What is lacking is standardized test methods and standard reference materials. The MEMS project plays an active role in the new ASTM Task Group E08.05.03, metrology for thin-film electromechanical properties of MEMS-based IC technologies.

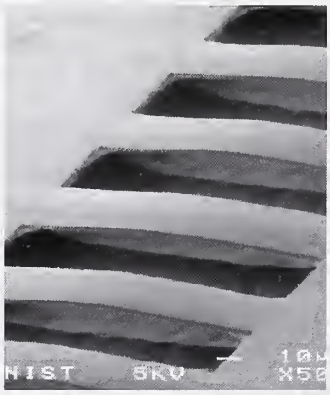
MILESTONE: By 2000, develop a standard test method for residual stress.

MILESTONE: By 2001, develop a standard test method for elastic modulus.

"Physical ... measurements are required for implementation of statistical metrology ... test structures [for the purpose of evaluating stress in interconnects] can be MEMS fabricated using traditional silicon process technologies."

ITRS Roadmap

IC Interconnect Characterization - Micro machining techniques, test structures, and test methods are being developed to characterize the stress, elastic modulus, and adhesion properties in IC interconnects. These test structures are fabricated in the standard IC process on fully fabricated ICs. Fixed-fixed beam and cantilever test structures with interconnect layers are micro machined in the fully processed IC. Measurements of deflection of buckled beams give information on the stress in each interconnect layer. Measurements of mechanical resonance give information on the elastic



Fixed-fixed beam test structure array for measurement of mechanical strain and interconnects in multilayer structures.

modulus of the films. These test structures can also be integrated with micro heating elements for accelerated testing.

MILESTONE: By 2001, develop a test method for elastic modulus in IC interconnects.

Micro Fabrication Laboratory - Micro fabrication methods developed by the semiconductor industry can be used to create new measurement tools. The MEMS project is utilizing this technology to develop tools for the IC industry. The project is also working with other NIST Groups and Divisions to create new tools for other industries. To this end, a shared-access micro fabrication laboratory is being developed. The facility will increase accessibility of micro fabrication processes, increase payoff to investment, and facilitate an environment where scientists can interact with each other on cross-disciplinary applications.

Accomplishments

- Test structures and analysis to measure mechanical stress/strain of interconnects in fully fabricated ICs were developed. A test chip containing the new test structure designs was fabricated on the commercial foundry 1.2 μm CMOS technology run through MOSIS. Following fabrication, the test structures were silicon micromachined in order to mechanically release them. These test chips contained test structures to measure the longitudinal stress component in IC interconnects. New designs are being developed to measure the lateral and normal components of stress as well. As Integrated Circuit (IC) device sizes shrink, thermo-mechanical stress in interconnects is an ever-increasing reliability concern. Current state-of-the-art IC technology uses 5 interconnect layers with aspect ratios (height/width) of 1.8. According to the 1997 SIA Roadmap, these numbers are expected to increase to 9.0 and 3.0, respectively, by the year 2012. Despite the increasing number of interconnect layers in IC technology, existing stress determination and modeling studies have been limited to single level metallization, with few exceptions. This is due, in large part, to the lack of experimental techniques for measuring strain in narrow linewidth (< 10 mm) multilayer structures. This work allows, for the first time, the measurement of stress in multilayer structures in fully fabricated ICs.

- The first round robin experiment was completed for the ASTM Task Group formed on MEMS. The experiment explored the precision and bias associated with the residual stress test structures in a round robin experiment for residual stress. The round robin, which had 11 other organizations involved, was sponsored by the ASTM Task Group E08.05.03 on "Structural Films for MEMS and Electronic Applications," which develops standards for electronic and MEMS applications. This task group has undertaken sponsorship of a series of round robin testing of residual stress and elastic modulus in test structures on a test die passed among participating laboratories. These parameters are important to the fabrication of MEMS devices. The first series of tests for this round robin emphasized the metrology of the structures that is required for the calculations of residual stress. Participation in the ASTM Task Group gives NIST an active role in supporting metrology for the semiconductor industry. In addition, measurement methods that are discussed and developed at the task group meetings are useful to the MEMS Project activities.

- A MEMS test structure was developed in collaboration with Analog Devices that was based on prior work by Liwei Lin, UC Berkeley. The new test structure was optimized to

appropriately measure tensile strain in the Analog Devices' commercial MEMS process, however it can be used to measure compressive strain as well. This new "folded beam micro strain gauge" has a vernier resolution of 0.1 μm. It was fabricated in Analog Devices' process. Theories and designs from this activity are available to other MEMS manufacturers. The MEMS industry requires standardized tools such as test methods and test structures to manufacture their products. Analog Devices supplied test chip space to the NIST designs in their commercial process. This test structure has been passed on to the ASTM E08.05.03 Task Group for possible inclusion in a residual stress round robin.

- Invented CMOS 1D and 2D accelerometers that operate based on heat convection, requiring no solid proof mass. The devices consist of microheaters and thermocouple sensors separated by a gap and placed in differential configurations. Thermocouple sensors measure the temperature difference between the two sides of the microheater caused by the effect of acceleration on free convection in the surrounding gas. The devices show a small linearity error of <0.5% under tilt conditions from –90 degrees to 90 degrees, and <1.6% under acceleration from 0 g^1 to 8 g. Sensitivity of the devices is a nearly linear function of heater power (temperature). For operating power between 35 mW and 45 mW, a sensitivity of 20 μV/g to 30 μV/g was measured. This is a spin-off of OA-sponsored work on Micromachined Passive Microwave Components in CMOS Technology. An invention disclosure has been written which resulted in material that was patented by NIST and our CRADA partner, RF Microsystems. This activity exemplifies our leadership role in MEMS/Microsystems Technology (MST).

FY Deliverables

Collaborations

CSTL/Analytical Chemistry Division, microfluidic systems (M. Gaitan)

Electronics and Electrical Engineering Laboratory/Electromagnetic Fields, feasibility of utilizing CMOS MEMS coplanar waveguide structure to measure dielectric constant of film (M. Gaitan)

Advanced Technology Program/Materials and Manufacturing Technology Office, development of MEMS-focused program entitled Microsystems Integration (M. Gaitan)

Analog Devices, MCNC, MSEL/Materials Reliability Division, MOSIS, metrology for thin-film electromechanical properties of MEMS-based IC technologies (J. Marshall, M. Gaitan)

Optical E.T.C., Inc., Integrated Dynamic Thermal Emitter Arrays (M. Gaitan)

RF Microsystems, Inc., Microwave CMOS Micromachined Power Systems (M. Gaitan)

NIST Nano/Micro/Meso-Scale Coordination Committee, EEEL, MEL, MSEL, PL, CSTL, Microfab Cooperative (M. Gaitan)

ASTM Task Group E08.05.03, metrology for thin-film electromechanical properties of MEMS-based IC technologies (J. Marshall)

Statistical Engineering Division, metrology for thin-film electromechanical properties of MEMS-based IC technologies (J. Marshall)

Cronos Integrated Microsystems, Inc., metrology for thin-film electromechanical properties of MEMS-based IC technologies (J. Marshall)

Standards Committee Participation

ASTM MEMS Residual Stress Round Robin, ensured round robin's success with the development of the MEMS Linear Dimensional Metrology (J. Marshall)

Software

Software was received from Statistical Engineering Division and is being further modified for a portion of the analyses of the fixed-fixed beam cantilever and micro strain gauge test structures (J. Marshall)

External Recognition

M. Gaitan has been asked to serve as a reviewer at the National Science Foundation (NSF) for proposals on Engineering Microsystems: "XYZ on a Chip." This review took place on February 25-26, 1999.

Publications

Milanovic, V., Bowen, E., Tea, N., Suehle, J. S., Payne, B., Zaghloul, M., and Gaitan, M., Convection-Based Accelerometer and Tilt Sensor Implemented in Standard CMOS, Proceedings of the 1998 International Mechanical Engineering Congress and Exposition, Anaheim, California, November 15-20, 1998, pp. 487-490.

Milanovic, V., Hopcroft, M., Zincke, C. A., Gaitan, M., and Zaghloul, M. E., Optimization of CMOS MEMS Microwave Power Sensors, Proceedings of the 1999 International Symposium on Circuits and Systems, Orlando, Florida, May 30-June 2, 1999.

Ozgur, M., Zaghloul, M. E., and Gaitan, M., High Q Backside Micromachined CMOS Inductors, Proceedings of the 1999 IEEE International Symposium on Circuits and Systems, Orlando, Florida, March 30-June 2, 1999.

Smee, S., Gaitan, M., Joshi, Y., and Blackburn, D. L., MEMS-Based Test Structures for IC Technology, Proceedings of the MEMS-Based Test Structures for IC Technology, pp. 147-149.

Linewidth and Overlay Standards for Nanometer Metrology

Technical Contact:
Michael W. Cresswell

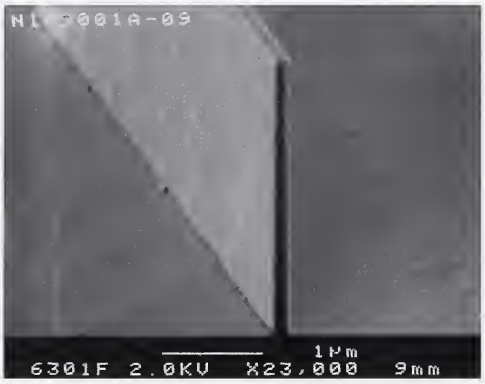
Staff-Years:
2.8 professionals
1.0 technician
2.0 guest researchers

Funding Sources:
NIST (94%)
Other Government Agencies (6%)

Parent Program:
Semiconductors, Silicon

Project Goals

Develop test-structure-based electrical metrology methods and related reference materials with primary emphasis on overlay and linewidth metrology and calibration; contribute to standards groups supporting the development of a litho-metrology infrastructure for the semiconductor tool industry.



Part of an electrical test structure formed in single-crystal silicon. This structure, developed in cooperation with Sandia National Labs, will help to resolve differences between electrical, SEM, and optical CD measurements.

Customer Needs

The Semiconductor Industry Association's (SIA) International Technology Roadmap for Semiconductors (ITRS) states that it is critically important to have suitable reference materials for lithography support available when on-wafer measurements are made as a new technology generation in integrated circuit (IC) manufacturing is introduced, and particularly during development of advanced materials and process tools. Each generation of ICs is characterized by the transistor gate length whose control to specifications during IC fabrication is a primary determinant of manufacturing success. The SIA projects the decrease of gate linewidths used in state-of-the-art IC manufacturing from present levels of up to 350 nm to below 90 nm within several years. Scanning electron microscopes (SEM) and other systems used for traditional linewidth control exhibit measurement uncertainties exceeding SIA-specified tolerances for these applications. It is widely believed that these uncertainties can be at least partially managed through the use of reference materials with linewidths traceable to nanometer-level uncertainties. Until now, such reference materials have been unavailable because the technology needed for their fabrication and certification has not been available. It is also widely believed that the usefulness of SEM metrology for monitoring wafers in advanced development and production will become inadequate at some future IC generation. Thus, there exists a need for new techniques to meet future metrology requirements.

Technical Strategy

The technical strategy that the Project staff have developed for fabricating linewidth and overlay reference materials is known as the Single-Crystal Silicon-on-Insulator Reference-Material implementation. Patterning with lattice-plane selective etches of the kind used in silicon micro-machining provides reference features with atomically planar sidewalls, as shown in the figure above. Selection of bond and etch-back silicon-on-insulator (BESOI) starting material with (110) surface orientation that is thermo-mechanically bonded to a (100) handle wafer provides reference-feature-sidewall verticality.

The traceability path for dimensional certification is provided by High Resolution Transmission Electron Microscopy (HRTEM) imaging. This method provides nanometer-level accuracy, but is sample-destructive and prohibitively costly to implement. This project's unique traceability strategy thus features the sub-nanometer repeatability of electrical CD metrology as a secondary reference means. Low-cost, whole-wafer electrical measurements are effectively calibrated with a few local HRTEM lattice-plane image counts. Typical reference features are several-thousand lattice planes wide. HRTEM lattice-plane image counts are achieved by high-density digitization, and numerical differentiation of the photographic record requires 3000 bpi digitization and highly-specialized, but proven image-analysis software. Both Sandia National Laboratories and Los Alamos National Laboratory have provided invaluable assistance in the development of this procedure.

The technical strategy has to be responsive to industry's requirement for reference materials to

"The Photomask industry as well as the Semiconductor industry have a problem meeting the technical road map using optical systems to measure IC patterns. As the time line moves forward we get closer to a point that our current measurement systems will not be able to satisfy the requirements. This is why the project of electronic measurement has appeal to Photronics. We would like to continue supporting this project and hopefully as the electronic measurement tools become viable NIST has a traceable standard. Thanks for your continuation of this standard."

Dave Owens, Photronics Laboratories

have the physical properties of standard 200 mm wafers. This project's technical strategy is to dice each 150 mm wafer and mount the separate chips in micro-machined standard 200 mm wafers to accommodate the test chips. The result is that finished units are user-friendly at an acceptable cost.

Project staff use the Single-Crystal Silicon-on-Insulator technical strategy also for a class of overlay reference materials known as tool-induced shift extractors. The special requirement here is the replication of features with different heights from the same photo-lithographic reticle. Project staff have devised a way of doing this with a unique selection of otherwise standard CMOS fabrication steps.

A key requirement that linewidth reference materials must satisfy is edge-definition sufficient to render width certification as meaningful. The fabrication and certification strategy complies with this requirement. Project staff have devised a method for fabricating the reference materials with suitable geometries and a method of certifying their widths at an acceptable cost. The next milestone is to perform electrical measurements and HRTEM on the same features and, through their correlation, to establish low-cost electrical linewidth metrology as a secondary reference means for the SOI-BESOI implementation.

MILESTONE: By 2000, fabricate and certify Single-Crystal Silicon-on-Insulator Reference-Materials with linewidths traceable to silicon lattice counts with uncertainties less than 3 nm.

The certification of tool-induced shift extractors will require (110) handle wafers and (100) surface wafers, the inverse of that employed for the linewidth reference materials. This approach allows the utilization of HRTEM images of lattice planes for the determination of the pitches of line pairs.

MILESTONE: By 2001, demonstrate the fabrication and certification of overlay reference materials with uncertainties below the 5-nm level and extend the technology to pitch reference materials.

The technical strategy for on-reticle linewidth metrology is to extract linewidths of control features electrically from test pads located outside the pellicle and therefore accessible to both the user and the supplier. These, in effect, serve as a built-in reference for the calibration of the optical microscopes used by both parties. In this application, the < 2-nm repeatability and robustness of electrical metrology is anticipated to have unique advantages. although we have yet to develop a traceability strategy

MILESTONE: By 2002, demonstrate electrical CD metrology as a means of providing on-reticle optical calibration.

Accomplishments

- High-resolution transmission electron microscopy has revealed (111) lattice fringes spanning the entire width of a NIST [112] mono-crystalline linewidth reference feature patterned on (110) BESOI material. A preliminary lattice-plane count of the HRTEM image was made by inspection of a photographic print obtained by an optical microscope. Use of a drum scanner has demonstrated that the lattice-plane count can be fully automated. The width of the feature was determined to be 583 um, with a combined standard uncertainty (coverage factor k = 2) of 2.5 μm.

- Standard 200 mm wafers were micro-machined to serve as reference-material test-chip carriers. The fabrication process features three-step lithography and etching with thermal oxide and low-temperature nitride hard masking. A technique for mounting the reference-material test chips in the carriers was developed. Samples of the carriers were delivered to, and used by, all major semiconductor manufacturers.

- In collaboration with Photronics Laboratories, Inc., Project staff developed and fabricated electrical linewidth-control features for inspection of photo-mask reticles used in integrated-circuit manufacture. The design allows probe-card access to electrical test pads advantageously located outside the pellicle while uniquely providing for electrical testing of the process-replicated linewidth-control features at the wafer level.

- A process for fabricating microstructures for calibrating optical-overlay metrology tools used in the manufacture of integrated circuits was developed. It features a unique combination of process steps extracted from CMOS processing, SOI, and silicon micro-machining unit-processes. These structures have all the properties, such as atomically-planar feature side-walls, geometrical symmetry, material uniformity, and provisions for traceability, that are necessary for monitoring the fabrication of emerging generations of sub-tenth micrometer integrated circuits. A unique fabrication process in which different layers of the micro-structure are imaged at the same time

"The single crystal linewidth standard project currently under joint development by NIST and Sandia National Labs will satisfy a major void that has previously existed in the metrology section of the International Roadmap for Semiconductors. The researchers from NIST have also, very cleverly, devised a rock-solid traceability methodology into the standard that starts with counting atom pairs within the silicon lattice. This atomic count is the basis for final certification of the quantity of standards that the industry will require. The final manufacturable phase is accomplished by employing a direct correlation between the atomic count and an electrical certification."

Bradley W. Scheer, Director of Research, VLSI Standards, Incorporated

from a single reticle enhances built-in overlay-vector traceability.

- A new generation of Single-Crystal Silicon-on-Insulator Reference-Material test chips fabricated on BESOI starting material and having feature linewidths less than 200 nm were delivered to a consortium of eleven integrated-circuit manufacturers for evaluation. The distribution was accompanied by NIST electrical-linewidth measurements for the respective features. The consortium members returned their own measurements. The consortium's measurements track this project's measurements, in most cases, to within less than 25 nm.

- The effective electrical linewidths of single-crystal linewidth reference features replicated on (100) BESOI substrates were modulated by DC biasing the handle wafer with respect to the cross-bridge resistor in which the reference feature was embedded. Both the sheet resistance and the electrical linewidths of the reference features closely tracked the predictions of theoretical models.

- The use of off-lattice alignment of reference features to enable their replication with linewidths as narrow as 90 nm with a 0.5 μm lithography projection aligner was convincingly demonstrated. The results of this activity may enable the narrower features to be routinely replicated using an all-optical standard fabrication process.

- A first set of edge-detector test structures for the development of process-specific reference materials was fabricated using a standard 0.5 μm CMOS interconnect process featuring tungsten-plug inter-level vias. Electrical testing has shown that such test structures may be useable as overlay reference materials with uncertainties as low as 10 nm. Such a structure is not currently available, but is in demand by industry.

FY Deliverables

Collaborations

Sandia National Labs, Statistical Engineering Division, and Precision Engineering Division, SEMATECH reference artifacts for critical dimension measurements (M. Cresswell, L. Linholm, and R. Allen)

International SEMATECH, development of single-crystal critical dimension reference materials and development of electrical overlay techniques (M. Cresswell, R. Allen)

International SEMATECH member companies (AMD, Compaq, Conexant, Hewlett-Packard, IBM, Intel, Lucent Technologies, Motorola, Texas Instruments, Hyundai, Infineon Technologies, Philips, STMicroelectronics, TSMC), development of single-crystal critical dimension reference materials (M. Cresswell, R. Allen)

VLSI Standards, development of single-crystal critical dimension reference materials (M. Cresswell, R. Allen)

Photronics, development of optical/electrical hybrid critical dimension measurement for photomasks (R. Allen, M. Cresswell)

Bio-Rad Semiconductor, evaluation of single-crystal CD structures using scatterometry techniques (R. Allen, M. Cresswell, and L. Linholm)

University of Edinburgh, National Semiconductor Ltd., modeling of current flow in three dimensional Van der Pauw test structures (M. Cresswell, L. Linholm, and R. Allen)

Sandia National Laboratories Microelectronics Development Laboratory, Sandia National Laboratories Compound Semiconductor Research Laboratory, Sandia National Laboratories Integrated Materials Research Laboratory, Los Alamos National Laboratory, NIST Statistical Engineering, Precision Engineering Divisions, and SEMATECH on fabrication and certification of reference materials for linewidth and overlay metrology (M. Cresswell, L. Linholm, and R. Allen)

VLSI Standards, Inc., and SEMATECH, development of commercial architecture and distribution plan for single-crystal CD reference materials (M. Cresswell, and R. Allen)

Simplex Solutions, Inc., procedures and algorithms for CD extraction from test features having conformal coatings (M. Cresswell)

Standards Committee Participation

SEMI International Standards Microlithography Committee, member, FY 97-99 (R. Allen)

SEMI International Standards Electrical Metrology Test Structures Task Force, Co-Chair, FY 97-99 (R. Allen)

SEMI International Standards, NA Regional Micro-Lithography Committee, Co-chair (M. Cresswell)

SEMI International Standards, Global Microlithography Coordinating Committee (M. Cresswell)

SEMI International Task-Force on X-Ray Lithography Mask Standard, Leader (M. Cresswell)

External Recognition

R. Allen received the U.S. Department of Commerce Bronze Medal Award, December 1998. Citation reads: "For providing reliable measurements on experimental microelectronic test structures in support of NIST consortia, including single-crystal devices."

M. Cresswell received a certificate of appreciation from SEMI International Standards for standards committee and task-force leadership activities.

Publications

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Dielectric and Interconnect Reliability Metrology

Technical Contact:
John S. Suehle

Staff-Years:
6.0 professionals
1.0 technician
6.0 guest researchers

Funding Sources:
NIST (100%)

Parent Program:
Semiconductors, Silicon

"For 100 nm devices and below, the gate dielectrics will be so thin that gate current will become a very important design factor. Improvements in basic understanding are needed, including reliability aspects."

SIA National Technology Roadmap for Semiconductors

Project Goals

Provide technological leadership to semiconductor and equipment manufacturers by developing and evaluating the methods, tools, diagnostic procedures, data, and physical models for understanding and improving the reliability of (1) ultra-thin silicon dioxide and alternative gate dielectric films, and (2) metal interconnects, such as copper, used in advanced CMOS technologies.

Test wafer being loaded on wafer prober for long-term dielectric testing.

Customer Needs

Ultra-thin gate dielectrics for future microelectronic device scaling are regarded as one of the most difficult challenges by the Semiconductor Industry Association (SIA) International Technology Roadmap for Semiconductors (ITRS). As the semiconductor industry continues to scale device dimensions to achieve channel lengths below 180 nm, gate dielectrics must be scaled to have an equivalent thickness below 2 nm. Ultra-thin SiO_2 dielectrics exhibit high tunneling currents, and the impact on device reliability is not well understood. The physics of failure and traditional reliability testing techniques must be reexamined for ultra-thin gate oxides that exhibit excessive tunneling currents and soft breakdown.

As device scaling continues, an alternative high-dielectric constant (high-k) gate dielectric system will be required due to the excessive tunneling currents exhibited by sub-2 nm SiO_2 films. The ITRS states that no suitable alternative high dielectric constant material has been identified with the stability and interface characteristics to serve as a gate dielectric. Years of research and development are required to identify and qualify a suitable alternative material.

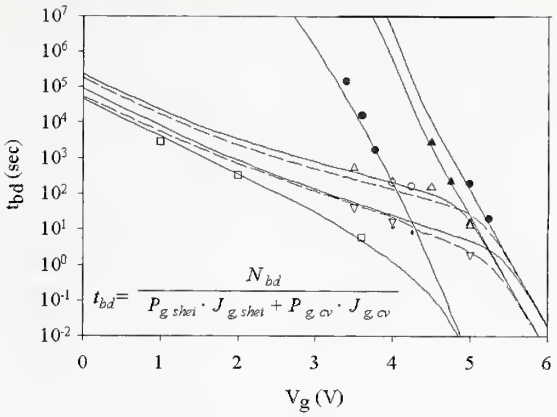
This project focuses on (1) the physics of failure and the reexamination of traditional reliability testing techniques of ultra-thin SiO_2 gate oxides that exhibit excessive tunneling currents and soft breakdown, (2) providing an understanding of the electrical characterization methodologies and reliability characterization required for alternative high-k gate dielectrics for advanced CMOS devices, and (3) developing critical electromigration standards and metrology methods for advanced metallization systems, including copper.

Technical Strategy

Test structure designs and test methods for characterizing copper interconnects will also be developed in collaboration with partners in the Semiconductor Industry. Special NIST-designed test chips include numerous structures for evaluating via and straight line electromigration and will be used as a vehicle to develop and validate test procedures and analysis techniques.

MILESTONE: By 2000, reliability test chips NIST 33 and 34 will be designed for experiments that include the determination of the precision of three electromigration standards: ASRM F1260 (constant current density and temperature test), JEP119 (SWEAT test), and JESD61 (isothermal test) for single-level metal.

The physical mechanisms responsible for "soft" or "quasi" breakdown modes in ultra-thin SiO_2 films and its implications for device reliability will be investigated as a function of test conditions and temperature. Long-term time-dependent-dielectric breakdown tests will be conducted on SiO_2 films as thin as 1.5 nm at lower electric fields closer to operating conditions. These tests will be used to determine the thermal and electrical acceleration parameters of device breakdown. Experiments will be conducted to investigate the differences of gate oxide breakdown and wear-out due to high oxide field and hot-carrier injection. This study will provide insight into the physical mechanisms of ultra-thin gate oxide wear-out and breakdown.



Plot above shows model and data for the combined effects of substrate hot-electron injection and high voltage stress on the lifetime of ultra-thin gate oxides.

"Time-Dependent-Dielectric Breakdown (TDDB) voltage and temperature dependence of new gate stack materials are not known."

SEMATECH Reliability Technology Advisory Board Supplement to the 1999 International Technology Roadmap for Semiconductors

Highly accelerated breakdown tests used to monitor manufacturing by the U.S. Semiconductor Industry must also be reevaluated for ultra-thin gate oxides. Traditional ramped voltage and current breakdown tests are not able to detect breakdown in films less than 4 nm thick. In FY98, a new voltage ramp technique had been developed through a NIST-coordinated collaboration between the Electronic Industries Association Joint Electron Device Engineering Council (EIA-JEDEC) and American Society for Testing and Materials (ASTM). A round robin was planned and initiated to evaluate the new test. Twelve laboratories are currently participating. NIST will continue its leadership role in the JEDEC and ASTM standards committees.

MILESTONE: By 2001, a new standard constant voltage stress test will be developed for determining Time-Dependent-Dielectric Breakdown (TDDB) acceleration parameters in sub-3 nm thick SiO_2 films. The new test will utilize current or voltage noise as breakdown criteria when films exhibit soft breakdown. Such a test will find application by the Semiconductor Industry when qualifying new manufacturing processes.

High-k gate dielectric films will be obtained from key industrial and university groups. Electrical characterization methodologies will be developed to address various issues associated with these films, including large leakage currents, quantum effects, thickness dependent properties, large trap densities, transient (non-steady state) behavior, unknown physical properties, and the lack of physical models.

Examples of measurement problems that are being addressed include modifying and verifying electrical defect density measurement techniques, including conductance-frequency, capacitance-voltage, and charge-pumping.

MILESTONE: By 2002, electrical and reliability characterization methodologies and analysis will be established for high-k dielectric materials. These methodologies will include the characterization of interface electrical properties, dielectric integrity, and long-term electrical stability and reliability.

Accomplishments

- A systematic study of the uncertainties, sensitivity, and limitations of the conductance technique for extracting the interface state density of metal-oxide-semiconductor (MOS) devices with ultra-thin (< 3.0 nm) oxides was completed. Capacitance and conductance characterization of MOS devices are used to determine properties such as oxide thickness, substrate doping, and interface state density. However, with the advent of ultra-thin oxides, effects such as tunnel current, series resistance, and quantum mechanical confinement in the substrate require additional consideration. This work provides a detailed analysis of the impact of these effects on parameter extraction using conductance and capacitance characterization of MOS devices with ultra-thin oxides.

- A new Standard Reference Database (SRD) program was initiated to provide the semiconductor industry with electrical and physical properties of alternative gate dielectrics for MOS devices from peer-reviewed journal articles. The goal for the first year of the program is to collect articles representing the main body of knowledge on alternative dielectrics for silicon. Due to increased power consumption and device and circuit instabilities associated with ultra-thin SiO_2, a high permittivity gate with low leakage current and at least equivalent capacitance, performance, and reliability will be required. However, as compared to SiO_2, very little is known about the electrical and physical properties of these films as gate dielectrics. The formation of an SRD to document the properties of these materials would provide the semiconductor industry a comprehensive database of evaluated properties from a variety of sources to use in the further research and development of alternative gate dielectrics.

- A new study has been initiated to study soft breakdown in 1.3 nm to 2.5 nm SiO_2 films and to study the temperature dependence of time-dependent dielectric breakdown. A more dramatic temperature dependence of wear-out has been observed, which raises serious reliability concerns. The purpose of this study is to obtain the temperature dependence of time-dependent

"The gate dielectric has emerged as one of the most difficult challenges for future device scaling. ... No suitable alternative high dielectric constant material has been identified with the stability and interface characteristics to serve as a gate dielectric. Years of research and development are required to identify and qualify a suitable alternative material."

SIA National Technology Roadmap for Semiconductors

dielectric breakdown for films as thin as 1.3 nm and to determine if soft breakdown modes influence the temperature dependence. The reliability of gate oxides is becoming a critical concern in advanced CMOS technologies where devices will operate with higher gate electric fields and direct tunneling currents. The physical mechanism responsible for new "soft" breakdown modes and its implications for device reliability will be investigated as a function of test conditions and temperature. These tests will provide critically important field acceleration parameters and thermal activation energies that are required for reliability extrapolation of ultra-thin oxides.

- A new research program to develop metrology for the semiconductor industry's next generation gate dielectric has been established at NIST. The program concentrates on the development of techniques and analysis for the electrical and reliability characterization of alternative dielectric materials for advanced microelectronics. Collaborations have been established with Texas Instruments, University of Delaware, the SRC/SEMATECH Front End Processing Center, the University of Minnesota, North Carolina State University, and Lucent Technologies. Thin gate dielectrics for future device scaling is regarded as one of the most difficult challenges by the ITRS. No suitable alternative high dielectric constant material has been identified with the stability and interface characteristics to serve as a gate dielectric. Significant research and development are required to identify and qualify a suitable alternative material.

- Interconnect reliability test chips NIST 33 and NIST 36 were designed, fabricated, and are being used. These chips are a collection of test structures designed in collaboration with members of JEDEC Committee JC14.2 on Wafer Level Reliability and with industry researchers. They are vehicles for improving existing reliability standards and for developing new ones for interconnects that are based on the results of inter-laboratory and other experiments. Wafers of NIST 33 were fabricated by the Stanford Nanofabrication Facility using single-level metal structures of an Al 1% Si alloy. Wafers of NIST 36 were recently fabricated for NIST by Silicon Graphics (formerly Cray Research) using a cladded Al-1%Cu metallization. Inter-laboratory experiments with these wafers are underway with LSI Logic Corporation and Infineon Technologies serving as additional reference laboratories. NIST 36 contains a variety of single-level metal and via-type electromigration test structures for evaluating the designs of these test structures and their use in test methods to characterize the reliability of interconnects. It also includes structures to measure stress voiding, electromigration-driven noise, metal sheet resistance and linewidth, and oxide thermal conductivity. The availability of via-type test structures on NIST 36 is intended to stimulate critically needed activities in JEDEC for the development of metrology tools for characterizing stress voiding and electromigration in vias.

FY Deliverables

SRDs

SRD program on alternate dielectrics initiated (E. Vogel)

Collaborations

Revised JESD35 (JEDEC-EIA), procedures for wafer-level testing of thin oxides (J. Suehle)

Analog Devices, Dynamic Research Corporation, Fairchild Semiconductor, National Semiconductor, Lucent Technologies, Texas Instruments, Advanced Micro Devices, Motorola, National Microelectronics Research Center, Penn State University, University of Maryland, ultra-thin gate oxide reliability (J. Suehle)

CSTL/Process Measurements Division, University of Maryland, microhotplate-based sensor arrays (J. Suehle, M. Gaitan)

General Electric, Sterling Semiconductor, Cree Research, gate dielectrics on SiC (J. Suehle)

University of Maryland, George Washington University, MIT Lincoln Laboratories, microhotplate-based chemical sensors (J. Suehle)

Texas Instruments, electrical and reliability characterization of ultra-thin gate oxides (J. Suehle, C. Richter)

University of Delaware, alternative dielectrics (J. Suehle)

NIST Boulder, National Semiconductor, SEMATECH, Rowan University, electromigration of Cu interconnects (H. Schafft)

LSI Logic Infineon, interlaboratory electromigration experiment (H. Schafft)

UMC, Silicon Graphics, electromigration of Al interconnects (H. Schafft)

Statistical Engineering Division, temperature dependence of copper resistivity (H. Schafft)

SRC/SEMATECH Front End Processing Center, University of Delaware, University of Minnesota (TiO_2), N.C. State University (oxynitrides, nitrides, ultra-thin SiO_2), alternative gate dielectrics (E. Vogel)

University of Maryland, gate dielectric reliability (E. Vogel)

Standards Committee Participation

JEDEC JC14.2 Dielectric Working Group, Chairman (J. Suehle)

ASTM, F-1 on Electronics, Subcommittee F1.11 on Quality and Hardness Assurance, member, FY 82-99 (H. Schafft)

EIA/JEDEC JC 14.2 on Wafer Level Reliability, Technical Advisor, FY 93-99 (H. Schafft)

Software

Windows-based electrical characterization software developed (E. Vogel)

Invited Talks

"Reliability Characterization of Ultra-Thin Film Dielectrics," at the ASTM Conference on Gate Dielectric Integrity: Material, Process, and Tool Qualification on January 25 in San Jose, CA. (J. Suehle)

"Round-Robin on GOI Measurements being Conducted in the USA," at the ASTM Conference on Gate Dielectric Integrity: Material, Process, and Tool Qualification on January 25 in San Jose, CA. (J. Suehle)

"Ultra-Thin Film Oxide Reliability," NASA Jet Propulsion Laboratory, Pasadena, CA, January 25, 1999. (J. Suehle)

"Properties of N- and P- Channel MOSFETs with Ultra-thin RTCVD Oxynitride Gate Dielectrics," Electrochemical Society Spring Meeting, Seattle, Washington, May 5, 1999. (E. Vogel)

"Reliability of Ultra-thin Oxides for MOS Devices," Short Course at North Carolina State University, Dept. of Electrical and Computer Engineering, April 22, 1999. (E. Vogel)

"Alternative Dielectric Technology and Metrology," University of Delaware, Dept. of Electrical and Computer Engineering, July 13, 1999. (E. Vogel)

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Allen, R. A., Vogel, E. M., Linholm, L. W., and Cresswell, M. W., "Sheet and Line Resistance of Patterned SOI Surface Film CD Reference Materials as a Function of Substrate Bias," Proceedings of the 1999 IEEE International Conference on Microelectronic Test Structures, Goteborg, Sweden, March 15-18, 1999, pp. 51-55.

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Schafft, H. A., "Interconnect Reliability Test Chip NIST 36: For Development of Measurement Tools & Standards," 1998 IEEE International Integrated Reliability Workshop Final Report, Lake Tahoe, California, October 12-15, 1998., pp. 109-111, IEEE Catalog Number 98TH8363.

Major Facilities / Laboratories

MicroFabrication Facility

Furnaces: 100mm (4"):

Thermal Oxidation (Wet, Dry), Chemical Vapor Deposition (Silicon Dioxide, Silicon Nitride, Polysilicon), Annealing

Photolithography:

Mask Contact Aligner (4") (5 μm feature size), SEM E-Beam (sub-μm feature size)

Etching:

Wet Chemical Etching, Isotropic Plasma Etching, XeF_2 Isotropic SI etch

Thin-Metal Film Deposition:

Sputtering and Evaporation of Metal Films

Packaging:

Wafer Saw, Al Wedge and Gold Ball Wire Bonders

Contact: Michael Gaitan, 301-975-2070

Molecular Beam Epitaxy Facility

A research facility for growing and utilizing high-quality epitaxial films of III-V compound semiconductors and for developing *in-situ* metrology to control their growth properties.

Dual-chamber MBE growth system

Contact: Joseph G. Pellegrino, 301-975-2123

Materials Characterization Labs

High-Resolution Optical:

Spectroscopic Ellipsometry, High-Resolution Fourier Transform Infrared Spectroscopy, Photoluminescence, Raman Scattering, Photoreflectance, and other Modulation Spectroscopies

Electrical:

Resistivity, Spreading Resistance, Lifetime, Hall Effect, Deep-Level Transient Spectroscopy, Deep-Level Optical Spectroscopy, Charge-Pumping Measurements, Capacitance-Voltage (high frequency & quasi-static), Surface Photovoltage, AC Impedance Analysis, Scanning Capacitance/Atomic Force Microscopy

X-Ray:

Double-Crystal Rocking Curve, Laue Orientation Facility

Device and Test Structure Characterization Labs

Semiconductor Electrical and Package Thermal
Power Device Model Extraction and Validation
Packaging, Assembly, and Bonding Evaluation
Package Interconnect
Scanning Electron Microscope
Scanning-Probe Microscope
Automatic Wafer-Level Measurement
Gate Dielectric Integrity
MEMS Electrical, Mechanical, Optical, and Microwave

Computer-Aided Design Labs

Test Structure Layout and Design
Integrated Circuit Layout, Design, and Simulation
Finite Element Thermal Analysis Tools and Computational Fluid Simulations
System, Device, Process, Interconnect, and Virtual Fabrications Simulations

National Research Council (NRC) Postdoctoral Opportunities

The Semiconductor Electronics Division at the National Institute of Standards and Technology (NIST), in cooperation with the National Research Council (NRC), offers awards for postdoctoral research for American citizens in the fields described below. The Division conducts research in semiconductor materials, processing, devices, and integrated circuits to provide, through both experimental and theoretical work, the necessary basis for understanding measurement-related requirements in semiconductor technology.

NIST affords great freedom and an opportunity for both interdisciplinary research and research in well-defined disciplines. These technical activities listed below are conducted in laboratories based in Gaithersburg, a Maryland suburb of metropolitan Washington, DC. Although applications for NIST Research Associateships are accepted throughout the year, they are evaluated by the panels only during February. To be eligible for review in February, completed application materials must be postmarked no later than Jan. 15, 2000, and received by the Associateship Programs office no later than Jan. 25, 2000. Supporting documents must be received by the Associateship Programs by Feb. 15, 2000. These times will also be approximately the same in 2001.

Scanning Probe Metrology

This project explores scanning probe microscope techniques to measure the spatial variation of physical and electrical properties of electronic devices and materials to the nanometer resolution scale. Scanning capacitance microscopy is being developed as a tool for measuring the dopant profile in two dimensions across a silicon p-n junction. Our project is developing both the experimental apparatus, which is based on an atomic-force microscope, and the theoretical modeling needed to interpret the results. Interests extend to other scanning probe techniques, including nano-spreading resistance, various optically pumped scanning probes, and scanning microwave microscopy.

Contact: David G. Seiler, 301-975-2054

Overlay- and CD-Metrology Development for Characterization of Advanced Lithography Systems

Projected CD and overlay control-tolerances for emerging generations of ICs drive final output-metrology uncertainty requirements down to the several-nanometer region. Similar requirements apply to metrology for the characterization of lithographic tools used for wafer processing. However, the development of CD and overlay metrologies is not maintaining the pace of lithographic resolution capabilities of the advanced imaging systems that will be coming on line in the near future. In addition, preferred processing options such as chemical/mechanical polishing tend to render existing overlay-metrology less effective for key process steps. The IC Technology Group seeks individuals interested in conducting further research into novel overlay-sensing instruments and techniques, and CD-extraction methodologies that are specifically optimized for lithographic tool characterization. We also encourage applicants with research experience in noncontact/nonintrusive electrical CD extraction and multimode overlay-sensor development, including overlay and CD-target and test-structure designs which are customized for the subject application.

Contact: Michael W. Cresswell, 301-975-2072

Reference Materials for the Evaluation of CD, Overlay, and Placement Instrumentation Traceable to Fundamental Length Standards

Participants in the National Semiconductor Metrology Program, which has been established at NIST, are regularly contacted by IC-industry groups for reference-material substrates that have structures and grids with certified CDs, overlay, and feature placements consistent with SIA-projected requirements. Applications include validating metrology-instrument performance and optimizing image-deconvolution algorithms. In the case of CDs, citing such reference materials is especially difficult because features having definitive cross-section profiles of particular geometries, dimensions, and material uniformity

are difficult to manufacture, thus challenging the reference-material certification process. In collaboration with other national laboratories and several commercial organizations, the IC Technology Group has recently begun a new project to fabricate and evaluate artifacts fabricated by novel techniques involving silicon-on-insulator materials to address the stated purposes. Our goal is to enable the low-cost manufacture and certification of reference materials to support the calibration and maintenance of metrology instruments used in advanced semiconductor manufacturing.

Contact: Michael W. Cresswell, 301-975-2072

Electrical Characterization of Semiconductor Compounds, Alloys, and Microstructures

A wide variety of electrical and magnetotransport techniques are being developed and utilized to characterize the electronic properties of compound semiconductor materials and microstructures. Measurement techniques include CV dopant profiling, deep-level transient spectroscopy, magnetotransport (H• 8 T), and conventional and photo Hall methods. Our goal is to understand the physical phenomena associated with these techniques and use them to investigate and characterize compound semiconductors of interest to industry.

Contact: David G. Seiler, 301-975-2054

Optical and Spectroscopic Properties of Semiconductors

Research focuses on understanding the electronic behavior of semiconductor materials and microstructures from their optical and spectroscopic response. Areas of investigation include the role of impurities and native defects in bulk crystals, and novel and useful optical properties induced by quantum confinement in reduced dimensional structures (heterostructures, quantum wells, superlattices, and quantum wires and dots). The broad range of cw optical probes that is available include reflection, transmission and absorption (1 mdV to 7 eV), and modulation spectroscopy; photoluminescence and photoluminescence excitation; Raman and resonant-Raman scattering; and spectroscopic ellipsometry. Emphasis is placed on understanding technology relevant properties, developing accurate measurement techniques, and producing standard reference materials and data required by U.S. industry.

Contact: David G. Seiler, 301-975-2054

Molecular Beam Epitaxy: Characterization and *In-Situ* Metrology

The unique growth capabilities of molecular beam epitaxy (MBE) have resulted in a variety of new electronic and optical devices which depend on engineered bandgaps and controlled interfaces. NIST's MBE facility consists of a dual chamber GaAs-based III-V system. One side is devoted to the growth of GaAs-based heterostructures to address the materials and growth metrology issues for electronic and opto-electronic devices. This includes confinement-type devices such as high electron mobility transistors, resonant tunneling devices, and laser structures. A current research area involves correlating the structural properties of interfaces with the transport and optical properties for modulation-doped field effect transistors. The other GaAs chamber is used to develop the essential metrology for implementing *in-situ* electrical, optical, and X-ray-based probes in an ultrahigh vacuum growth environment. These probes include X-ray fluorescence, specular and off-specular reflectance, and spectroscopic ellipsometry probes. The MBE effort is interactive because growth and characterization within the MBE facility is supported by a comprehensive set of ex situ electronic, structural, optical, and magnetotransport spectroscopies. In addition, facilities exist within the Division for simple lII-V processing. Opportunities are available for candidates interested in studying growth and materials-related issues of semiconductors, as well as implementing real-time in situ probes for better control over growth parameters.

Contact: Joseph G. Pellegrino, 301-975-2123

Physics of Semiconductor Devices

Device-modeling and theoretical-device physics research are in progress to interpret measurements of model parameters. One goal of this work is predictive physical models of devices with high carrier and doping concentrations. For example, topics include high-concentration effects, carrier lifetimes, carrier mobilities, and radiation effects that affect the operation and performance of semiconductor devices. The approach in this work involves the careful examination, extension, and experimental verification of the theoretical basis used in device

models for silicon, gallium-arsenide, and other compound semiconductor devices. Collaborations are in progress to include these improved physical models in device simulations and then to verify, validate, and benchmark these enhancements.

Contact: Herbert S. Bennett, 301-975-2079

Microelectronic Package Characterization

Research focuses on the electrical and thermal properties of microelectronic packages and interconnects. Our objectives are to improve methods for characterizing these properties for advanced packages and modules; improve measurement methods and techniques; and verify "compact" electrical and thermal models for packages and modules, and parameter extraction techniques for the models. We have fully equipped thermal and electrical characterization laboratories including an infrared thermal imager and a time domain interconnect parameter analyzer, and several computer workstations with a compliment of thermal and electrical modeling and analysis software.

Contact: David L. Blackburn, 301-975-2068

Integrated-Circuit Test Structures

This research is directed toward developing and verifying integrated-circuit test structures for process control, circuit-design reliability, and product assurance of integrated circuits. This involves test-structure design, mathematical modeling, fabrication, data acquisition, and data analysis using expert systems. Test structures for random-fault detection, yield analysis, and dynamic-circuit characterization are under study. A computer-aided design system and computer-controlled wafer-probe equipment are available for this work.

Contact: Harry A. Schafft, 301-975-2234

Modeling Advanced Semiconductor Devices for Circuit Simulation

Accurate circuit simulator models for advanced semiconductor devices are required for effective computer-aided design of electronic circuits and systems. However, the semiconductor device models provided in most commercial circuit simulators (e.g., simulation program with integrated circuit emphasis) are based on microelectronic devices, and they do not adequately describe the dynamic behavior of advanced semiconductor devices. Therefore, research focuses on the following: (1) physics-based models - for advanced semiconductor devices such as power and compound semiconductor devices; these models are implemented into available circuit and system simulation programs; (2) parameter extraction algorithms - for obtaining model parameters from terminal electrical measurements; and (3) characterization procedures - for verifying the models' ability to simulate the behavior of the devices within application circuits. NIST also works closely with commercial software vendors to make the new models available to circuit design engineers, and has established the NIST/IEEE Working Group on Model Validation to develop comprehensive procedures for evaluating the performance of circuit simulator models. (For more information, see ray.eeel.nist.gov/modval.html.)

Contact: Allen R. Hefner, Jr., 301-975-2071

Ultrasmall Devices and Nanoelectronics

The objective of this research is to develop the principles behind new fabrication technologies and highly accurate metrology of nanometer-scale devices for application to quantum standards and quantum-based nanoelectronics. The ultrasmall devices are based on quantum resonant tunneling, Coulomb blockade, ballistic transport, and mesoscopic effects. Research includes the development of (1) technologies needed for cost-effective ways to fabricate device structures in nanometer scale dimensions in order to improve performance of these new devices, (2) improved methods to characterize and model their electrical and optical behavior, and (3) capabilities to measure and understand quantum devices that are necessary for future electrical standards.

Contact: Wen F. Tseng, 301-975-5291

MicroElectroMechanical Systems

The Micro-Electro-Mechanical Systems (MEMS) project centers on the development and modeling of novel electro-mechanical sensors and actuators manufactured by integrated circuit fabrication techniques. Research includes the design, fabrication, and modeling of microheating elements, mechanically resonant structures, optical systems on a chip, microwave transmission lines, power sensors, antennas, and microfluidic systems. Metrology efforts involve

developing MEMS test structures and test methods to characterize device properties, test their performance and reliability, and to develop device models based on these measurements. MEMS-based test structures are also being utilized to characterize film properties in mainline semiconductor fabrication processes.

Contact: Michael Gaitan, 301-975-2070

Reliability of Integrated Circuit Dielectric Films

Aggressive scaling of gate oxide thickness used in silicon integrated circuits necessitates the understanding of the physical mechanisms responsible for dielectric degradation and breakdown. We are particularly concerned with the reliability of ultra-thin gate oxides that are in the direct tunneling regime during circuit operation. Research focuses on (1) identifying parameters to determine the physics of time-dependent dielectric breakdown of ultra-thin dielectric films in the tunneling regime; (2) determining the effectiveness of highly accelerated stress tests to predict long-term reliability of thin dielectric films; (3) relating analytical characterization of oxide bulk and interfaces to electrical behavior; (4) identifying and controlling fabrication process parameters that affect intrinsic and extrinsic failure modes; and (5) characterizing and evaluating alternate dielectrics for use as substitutes for silicon oxide in advanced circuit technologies.

Contact: John S. Suehle, 301-975-2247

Electrical Characterization of Integrated Circuit Metallizations

Integrated circuit (IC) interconnect metal lines and vias are operated at increasingly higher current densities (~MA/cm^2) because of reduction in critical dimensions needed for higher integration scale. We are investigating structural properties and design factors that influence the electrical transport properties in metallizations operated at temperatures ranging from a cryogenic regime to 300 °C above room temperature, with passivated or unpassivated pure metals or alloys based on aluminum, copper, and tungsten. Metallization failure induced by electromigration and stress voiding, which determine interconnect reliability limitations, is correlated with normal operative IC service conditions. Data collected with submicrometer metallizations are analyzed in terms of the metal deposition techniques/conditions and subsequent annealing procedures which determine grain size and orientation distributions, and bamboo structure formation. Computer simulation and modeling is developed for test structure design, experiment design, and data analysis. Dimensional metrology involving atomic-resolution scanning probe microscopy complements scanning electron and transmission electron microscopies used to monitor and characterize interconnect damage developed under stress conditions. An important objective of this research is to identify and understand those design and process parameters that affect interconnect reliability.

Contact: Harry A. Schafft, 301-975-2234

Physical and Electrical Properties of Thin Dielectric Films

It is becoming difficult to characterize ultrathin gate dielectric films (typically less than 5 nm) used in MOS devices because technology is driving them thinner. We are developing electrical test methods (using conventional techniques such as I-V and C-V, as well as low-temperature magnetotransport techniques) to measure the physical properties (e.g., film thickness and permittivity) of such films. Electrical results are compared with those of optical and other measurement methods, and physical models are developed to be effective for more than one measurement technique. The interface between the dielectric film and the silicon substrate is critical to understanding these measurements. We are also developing techniques to characterize buried interfaces (i.e., interface roughness) and are determining how the interface and physical properties affect device performance and reliability.

Contact: Curt A. Richter, 301-975-2082

In-Situ and Real-Time Thin-Film Metrology and Material Process Control

To improve reliability and throughput, integrated circuit device fabrication techniques require rigorous control of material growth and deposition. *In-situ* measurements and methods are seen as effective tools for such a requirement. We have set up a sophisticated, flexible ultrahigh vacuum system to investigate the various *in-situ* metrology techniques and to apply these techniques to real thin-film fabrication processes. At this early stage, research focuses on producing an accurate optical data base for semiconductor

materials and thin films at room and higher temperatures. The metrology techniques of interest are mostly optical probes including spectroscopic ellipsometry, light scattering, and vapor deposition and plasma processes. Opportunities exist for proposals that center on instrumentation, thin-film fabrication, and characterization. Various *ex-situ* material characterization techniques are also available in collaboration with other projects in this Division.

Contact: Nhan V. Nguyen, 301-975-2044

Measurement Traceability for Thin Dielectric Films

The development and fabrication of ultrathin, increasingly sophisticated gate dielectrics is a key technology for integrated circuits at the 0.25 mm feature size and beyond. With the use of single-wavelength and spectroscopic ellipsometry, thin dielectric films are characterized for use in the calibration of instruments to monitor and control gate dielectric fabrication. Research involves the development of physical standards and supporting methodologies that will provide traceability to NIST for advanced gate dielectrics. Input from various physical, optical, and electrical techniques is needed to improve our knowledge of the structure and composition of advanced dielectrics and their interfaces for correct interpretation of ellipsometric measurements. Research will focus on relating the analyses of XTEM, surface second harmonic generation, scanning probe methods, X-ray reflectance, and various electrical techniques to improve our understanding of the structure of thin dielectric films, which would strengthen and extend NIST's capability for providing thin dielectric measurement traceability.

Contact: Curt A. Richter, 301-975-2082, or Nhan V. Nguyen, 301-975-2044

Conferences and Workshops

Future Events

March 20 - 24, 2000

The 2000 Government Microcircuit Applications Conference (GOMAC) will be held in Anaheim, CA, USA. GOMAC is a government-sponsored conference established primarily to review developments in microelectronics applications for government systems. GOMAC has been used to announce major government microelectronic initiatives, such as VHSIC and MMIC, and provides a forum for program reviews.
Contact: Loren W. Linholm, 301-975-2052

June 26 - 29, 2000

The 2000 International Conference on Characterization and Metrology for ULSI Technology will be held at NIST, Gaithersburg, MD, USA. The conference will bring together scientists and engineers interested in all aspects of the technology and characterization techniques for silicon device research, development, manufacturing, and diagnostics: chemical and physical, electrical, optical, *in-situ*, and real-time control and monitoring.
Contact: David G. Seiler, 301-975-2054

March 19 - 22, 2001

The IEEE International Conference on Microelectronic Test Structures (ICMTS) will be held in Kobe, Japan. The ICMTS is the premier conference devoted to the development, measurement, and analysis of test structures, providing a forum for designers and users of test structures to discuss recent developments and future directions. The meeting is a IEEE conference, sponsored by the IEEE Electron Devices Society.
Contact: Loren W. Linholm, 301-975-2052

Past Events

March 9 - 11, 1999

The Semiconductor Thermal Measurement and Management Symposium was held in San Diego, CA, USA. Technical papers on current thermal management, modeling, and measurement work on electronic components and systems in the following areas were presented at the conference: Thermal Characterization - Component Through System, Analytical and Computational Modeling and Simulation, Experimental Methods and Applications, Thermal Design and Testing for Reliability, Thermal Aspects of High-Temperature Electronics, Simulation, Tools for Concurrent Design of Electronic Systems, and Electro-Thermal Modeling of Semiconductor Devices.
Contact: David L. Blackburn, 301-975-2068

February 8 - 11, 1999

SRC/NIST/NSF Research Issues and Directions for Nanoscale Transistors: Technology, Physics, and Simulation was held at NIST, Gaithersburg, MD. The conference was attended by over 50 researchers from industry, academia, and government. The Workshop identified critical modeling and simulation issues, such as quantum effects, that must be solved if modeling and simulation is to have a significant impact on the development of future nano-transistors.
Contact: David L. Blackburn, 301-975-2068

November 30 - December 2, 1998

The Fourth VLSI Packaging Workshop of Japan, jointly sponsored by the IEEE CPMT Society and NIST, was held in Kyoto, Japan. The workshop served the growing need of our information-oriented society, which is becoming more reliant on "Mobile Communication," "Personal Computing," and "Computer Networks."
Contact: George G. Harman, 301-975-2097

Proceedings

September 1999

Ultrathin SiO_2 and High-k Materials for ULSI Gate Dielectrics, the proceedings of a recent Materials Research Society Symposium, was published in September 1999. The book gives an account of fundamental research into the materials, processes, and manufacturing challenges that must be resolved before the high-k gate stack module can be used in mainstream IC manufacturing.

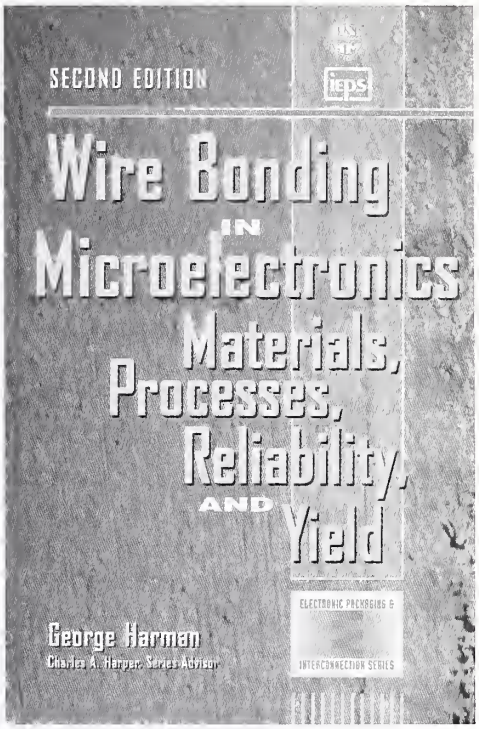
November 1998

The *Characterization and Metrology for ULSI Technology* conference proceedings was published in November 1998. This book summarizes major issues and gives critical reviews of important measurement techniques that are crucial to continue the advances in semiconductor technology.

Semiconductor Wire Bonding 'Bible' Revised

Every year, about 4 trillion wire bonds are made to interconnect silicon chips to their electrical package or circuitry. This process, called wire bonding, is the world's most frequently performed sophisticated manufacturing step. Now, George Harman, a NIST fellow in EEEL's Semiconductor Electronics Division, has made life a little less complicated for those who make and use such bonds. He recently revised and expanded *Wire Bonding in Microelectronics - Materials, Processes, Reliability and Yield*, a technical bible for chip manufacturers since 1989. In addition to reviewing classical metallurgical problems, the updated edition provides information on new materials, new interconnect techniques, and the pros and cons of alternative bonding technologies. It offers guidance on testing wire bonds; cleaning bond pads to improve bondability and reliability; and solving cratering, bond fatigue, and other mechanical problems. The book provides contemporary details such as bonding to multichip modules, applying new bonding metallurgies, and a description of the wire bonding mechanism. The new (second) edition is part of McGraw-Hill's series on Electronic Packaging and Interconnection and is available from them and from the International Microelectronics and Packaging Society.

NIST Connections, November 1997



G.G. Harman, the world's foremost authority on wire bonding in microelectronics, signs a copy of the second edition of his book for J.C. French, Founding Director of the Electronics and Electrical Engineering Laboratory.

"contains everything an assembly engineer needs to know about wire bonding"

Co-Founder of Orthodyne Electronics Corp.

"excellent reference, one of the most useful I have come across in all engineering"

- VP, Design, Package, and Test Engineering, Anadigics, Inc.

New Book Confronts Issues Challenging Semiconductor Industry

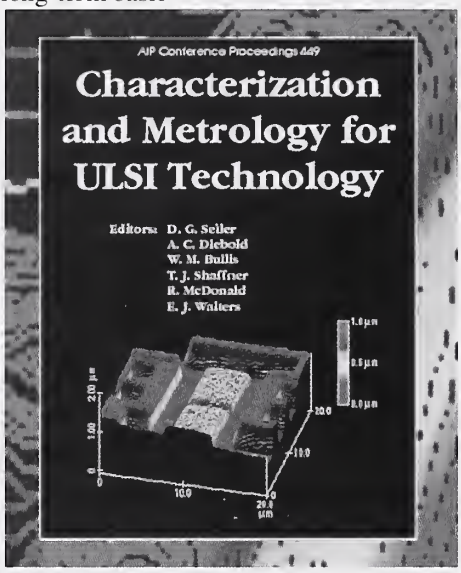
"Once in a while, a reference work comes along that can truly be referred to as 'seminal.' This is the case with Characterization and Metrology for ULSI Technology."

Semiconductor International, April 1999

"All 140-plus papers focus on some leading-edge aspect of metrology and inspection...All of the papers are authored by leaders in their fields, who are involved in edge-of-technology work."

Semiconductor International, April 1999

A wide range of issues important to the U.S. semiconductor industry - and a strategy to correct what some experts see as a potentially dangerous trend of declining long-term basic research and development - are discussed in a volume of scientific and engineering papers. Released during the American Vacuum Society's 45th International Symposium, November 2-6, 1998 in Baltimore, the volume, totaling more than 1,000 pages, is entitled *Characterization and Metrology for ULSI Technology*. It was published by the American Institute of Physics (AIP #449) and edited by six scientists from industry and government. According to Alexander E. Braun, Associate Editor of Semiconductor International, "the feature that really opens up this work for use as a reference source is that the reader not only has the book available but a key-word searchable CD-ROM version of the text and figures as well."



The worldwide semiconductor community faces increasingly difficult challenges as it moves into the manufacturing of chips with feature sizes approaching 100 nm. Many of these challenges are materials-related, such as transistors with high-k dielectrics and on-chip interconnects made from copper and low-k dielectrics.

This proceedings volume summarizes these and other major issues and gives critical reviews of important techniques that are crucial to advancing semiconductor technology. The papers collected provide a concise and effective portrayal of the unique characterization requirements of silicon IC development and manufacturing. Sessions on silicon ICs were based on the technology drivers in the National Technology Roadmap for Semiconductors. The papers also present a discussion of the problems that must be addressed by industry, academia, and government to continue the dramatic progress in this field.

The 1998 conference brought together leading scientists and engineers who are involved in all aspects of metrology and characterization techniques for silicon research including development, manufacturing, and diagnostics. Key papers were delivered by, among others, Mark Melliar-Smith, President and CEO of SEMATECH, on Metrology Needs for the Semiconductor Industry Over the Next Decade; Robert Helms of Texas Instruments on Industry / University / Government Partnerships for Metrology: A New Paradign for the Future; and David S. Perloff of Veeco Instruments on Gaging the Future: Long Term Business Outlook for Metrology and Wafer Inspection Equipment.

Characterization and metrology are key enablers for developing semiconductor process technology and in improving manufacturing. This is one of the few books available today that emphasize the science and technology of semiconductor characterization in the factory environment. The increasing importance of monitoring and controlling semiconductor processes makes it particularly timely.

Mark Melliar-Smith, President and CEO of SEMATCH, opened the Conference with a challenging talk on Metrology Needs for the Semiconductor Industry over the Next Decade.

Duncan McBride Serves as First ComSci Fellow in SED

Duncan McBride, from the National Science Foundation (NSF), worked in the Semiconductor Electronics Division (SED) throughout fiscal year 1999. Duncan, who serves as a Physicist and Program Director for the Division of Undergraduate Education at NSF, worked with the SED on the process and criteria for selecting, evaluating, and strengthening projects in the Division. Additionally, he worked with the Scanning-Probe Microscope Metrology Project on a study of the optimal conditions for growing oxide on sectioned silicon wafers to permit scanning capacitance microscopy for 2-dimensional dopant measurements. Duncan conducted a study of "enhanced" native oxides on silicon for use as the insulating layer in SCM measurements. Surface preparation conditions at 200 °C to 350 °C, for 0.5 h to 8 h, with and without UV light, as well as, an ultraviolet ozone photoreactor were investigated. The oxides were characterized by measuring dC versus V curves with the SCM, traditional C-V measurements with a Hg-probe, and ellipsometric measurement of oxide thickness.

Duncan obtained his Ph.D. from the University of California at Berkeley in Condensed Matter Physics. He joined NSF in 1985. In 1996, he achieved the Director's Award for Management Excellence. Duncan continues to work in the SED as a Guest Researcher.

Rita Colwell, director of The National Science Foundation, presents a Science and Technology Fellowship Program Certificate to Duncan McBride.

The U.S. Department of Commerce Science and Technology Fellowship (ComSci) Program was established in 1964 to provide Federal Government employees in a professional or management series with an opportunity to study national and international issues relating to the development, application, and management of science and technology. With the exception of several years, the ComSci Program has been in existence since 1964.

The purpose of the ComSci Program is to provide a hands-on learning experience for participants, and to increase their understanding of technological innovation as a source of national and international economic growth; the relationship of science and technology to government policies on economics, trade, education, and fiscal matters; the organization of scientific and technological activities in the Federal Government; and the technical activities and problems which exist in other executive, legislative, and judicial agencies of the government, thereby motivating and encouraging the development of cooperative endeavors and programs.

Collaborations with the Semiconductor Research Corporation

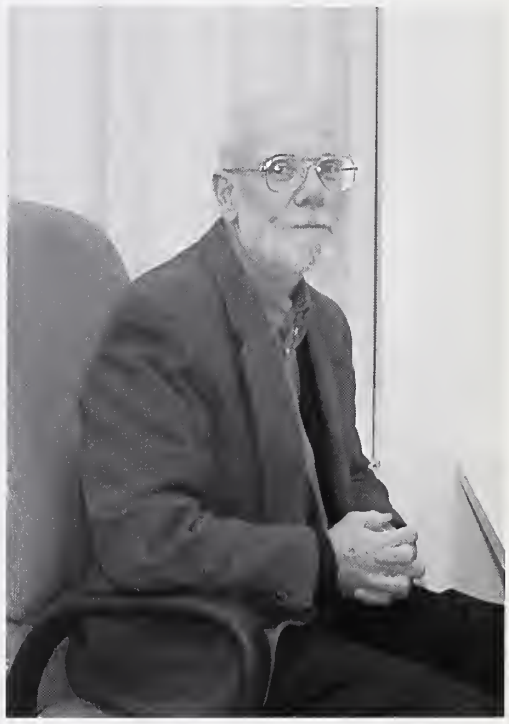
"In 1982, the SIA formed the Semiconductor Research Corporation with dual objectives of developing highly qualified technical personnel for employment in the industry and conducting a program of long-range, pre-competitive research and technology development. The program is carried out at a large number of universities, and is unique in its industry/university relations."

Research Technology Management, 1997, p. 46

David Blackburn has been on a two-year Intergovernmental Personnel Agreement (IPA) as a Government Assignee to the Semiconductor Research Corporation (SRC) in Research Triangle Park, N.C., since January 1998. The SRC was established in 1982 as not-for-profit research management consortium to help solve the North American Semiconductor Industry's technical challenges. The major functions of the SRC are to manage precompetitive research at North American Universities, support development of a relevantly-educated technical work force, to facilitate long-range technical planning for the industry, and to champion interorganizational communications. Full members of the SRC include Advanced Micro Devices, Compaq Computer, Eastman Kodak, Hewlett-Packard, IBM, Intel, Intersil, LSI Logic, Lucent Technologies, Motorola, National Semiconductor, Northrop Grumman, and Texas Instruments. NIST is a government participant.

David's major responsibility at the SRC has been to manage the research contracts in the Advanced Devices and Technology (ADT) Thrust Area. The priorities of that research are to advance traditional complementary metal-oxide semiconductor (CMOS) to its practical limits, to narrow the options for the next device that will replace CMOS, and to generate options for novel devices and structures that can carry the semiconductor industry well into the 21st century. The SRC typically has 3-5 Industry Assignees at any one time, and David, who will return to NIST full time in January 2000, is the first Government Assignee to the SRC. It is expected that the knowledge and experience gained by David on this assignment will prove invaluable to the Division as it plans and executes its programs for the 21st century.

NIST has had a long and fruitful relationship with the SRC. In addition to David's assignment, current Division interactions include those of Jim Ehrstein and Harry Schafft, who are members of Technical Advisor Boards for Front End Processing and Interconnects, respectively, and John Suehle and Curt Richter, who serve as "Industrial Liaisons" for specific technical tasks, and thus assist in advising and directing the research directions for those tasks. Also, NIST supports the NIST/SRC Graduate Fellowship. The current Fellow is doing research at the University of California at Berkeley on gate dielectric reliability. Also, Eric Vogel, a recently hired staff member in the dielectric reliability area was an SRC-supported student at North Carolina State University where he received his Ph.D.



David L. Blackburn, Deputy Division Chief and former assignee to the Semiconductor Research Corporation.

January 2000

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