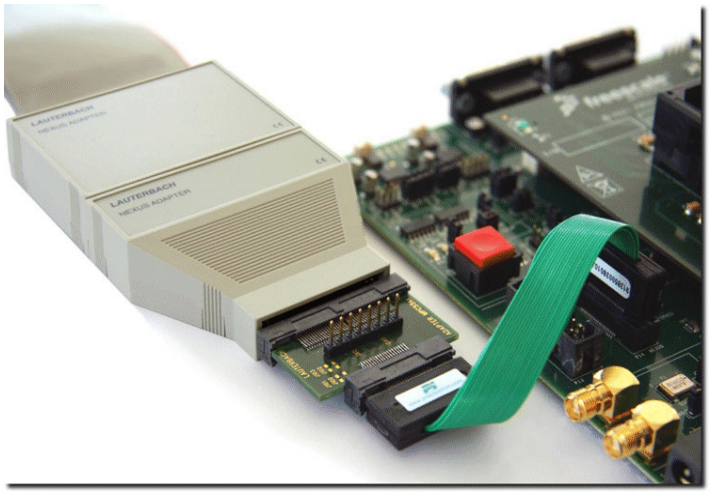
TRACE32®

Technical Information

NEXUS-MPC5500



MPC55xx/MPC56xx NEXUS Debugger and Trace

- Support for NEXUS standard class 1 to 3+
- Easy high-level and assembler debugging
- Program flow and Data trace
- Watchpoint and Ownership tracing
- Up to 4 GByte trace memory
- Trigger programming
- Interface to all hosts
- USB and ETHERNET interface included
- Support for VLE (Variable Length Encoding)
- eTPU, GTM and SPT debuggers included
- eTPU program and data trace supported
- Data trace for additional trace clients (e.g. DMA, FlexRay)

MPC5514
MPC5515
MPC5516
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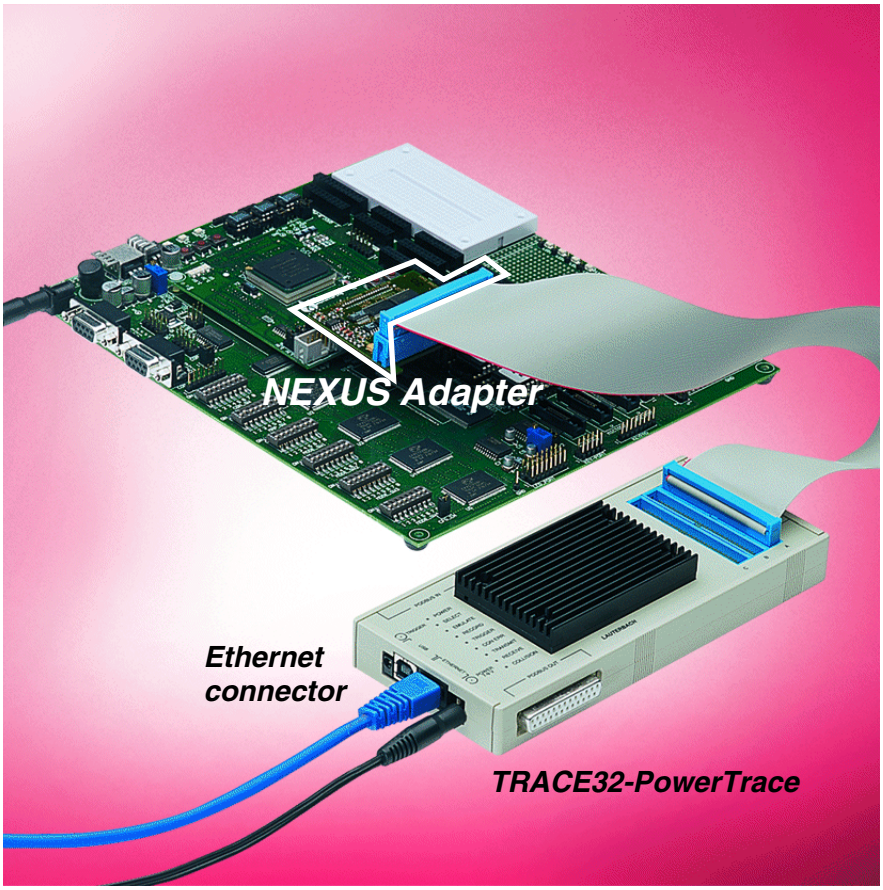
DEVELOPMENT TOOLS

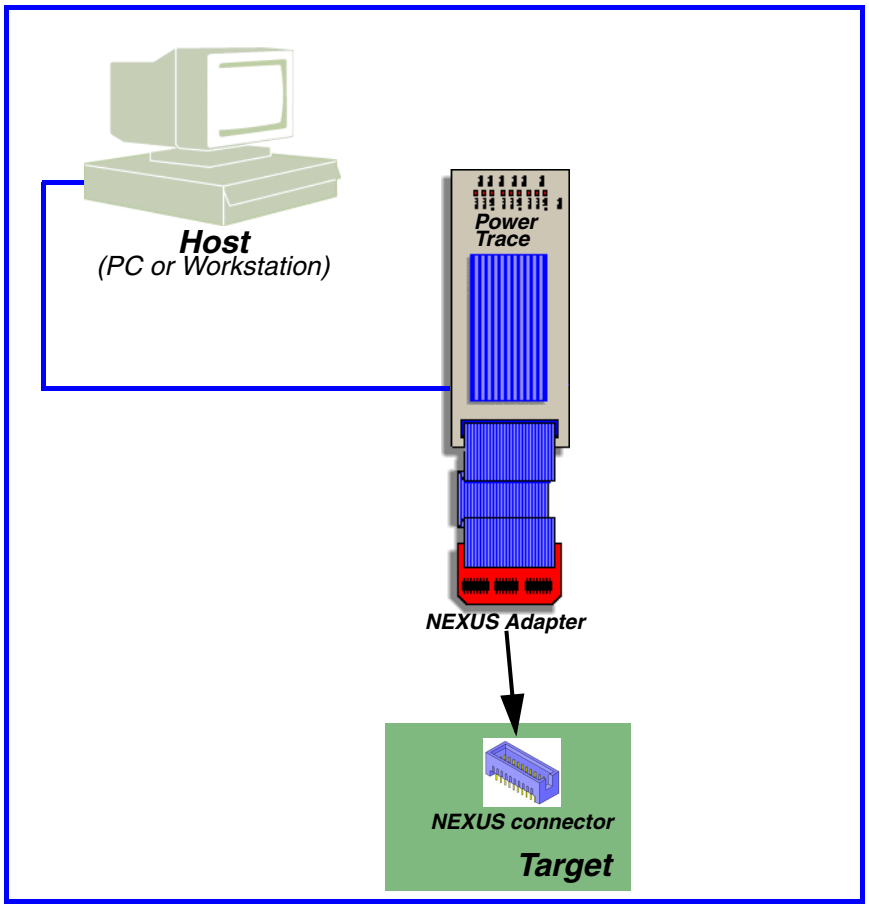
Hardware Concept

TRACE32-PowerTrace/NEXUS

The NEXUS support is based on the universal hardware module TRACE32-PowerTrace. The connection to the NEXUS interface on the target is done by a CPU specific NEXUS adapter.

TRACE32-PowerTrace includes a USB and Ethernet interface.



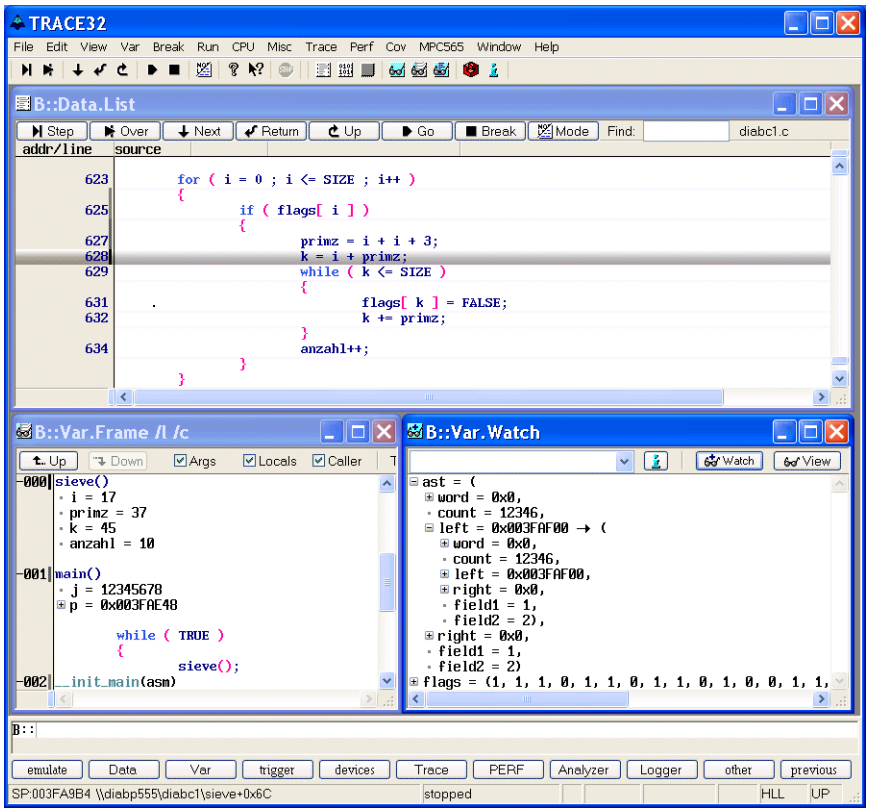


PowerTrace

- ❏ Universal debugger hardware for all architectures
- ❏ Ethernet or USB interface included
- ❏ Program and data flow trace for NEXUS up to 200 MHz
- ❏ 16/32 MFrame trace memory
- ❏ 96 channels
- ❏ 32 bit time stamp, 20 ns resolution
- ❏ CPU specific NEXUS Adapter

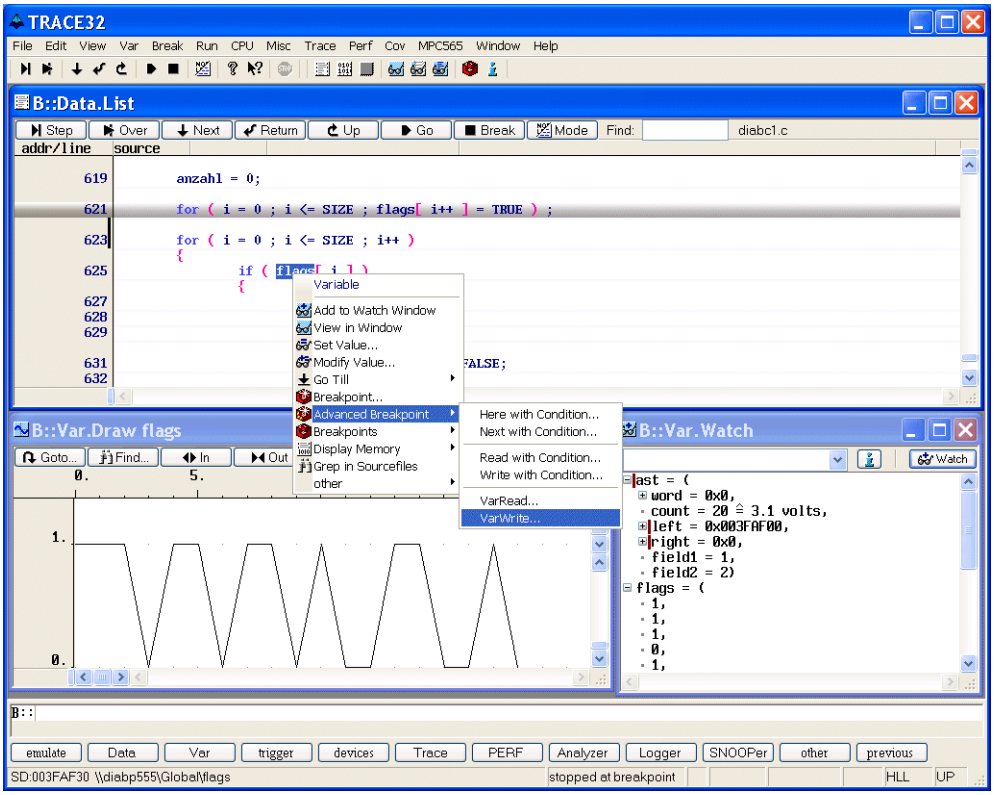
Software Concept Debugger

Symbolic Debugging



A hierarchical symbol database enables structured symbolic debugging. Symbol names can be used to show single program addresses, module names and memory classes. The disassembler can use the symbols for labels and/or operands. Demangling for C++ signatures is supported.

High-Level Language Debugging



TRACE32 can directly load the output of all standard compilers for C, C++, JAVA, Pascal, Modula2, PEARL and ADA from most compiler vendors. Program display and debugging can be done in assembler, high-level or in a mixture of both. It is possible to construct both assembler and high-level windows on the screen simultaneously. All variable types specific to the high-level language can be displayed and modified. Addresses can be absolute, relative or line number based.

Real-time update

Real-time update of memory and variables is possible while the CPU is running.

Debugging

The debugger uses the following breakpoint implementations to stop the program execution at a certain instruction:

- ❏ unlimited number of software breakpoints for code in RAM
- ❏ Umlimited Code Breakpoints in FLASH areas
- ❏ a limited number of onchip breakpoints for code in ROM/ FLASH

The onchip breakpoints can also be used to stop the program execution after a read/write access to a specific memory address.

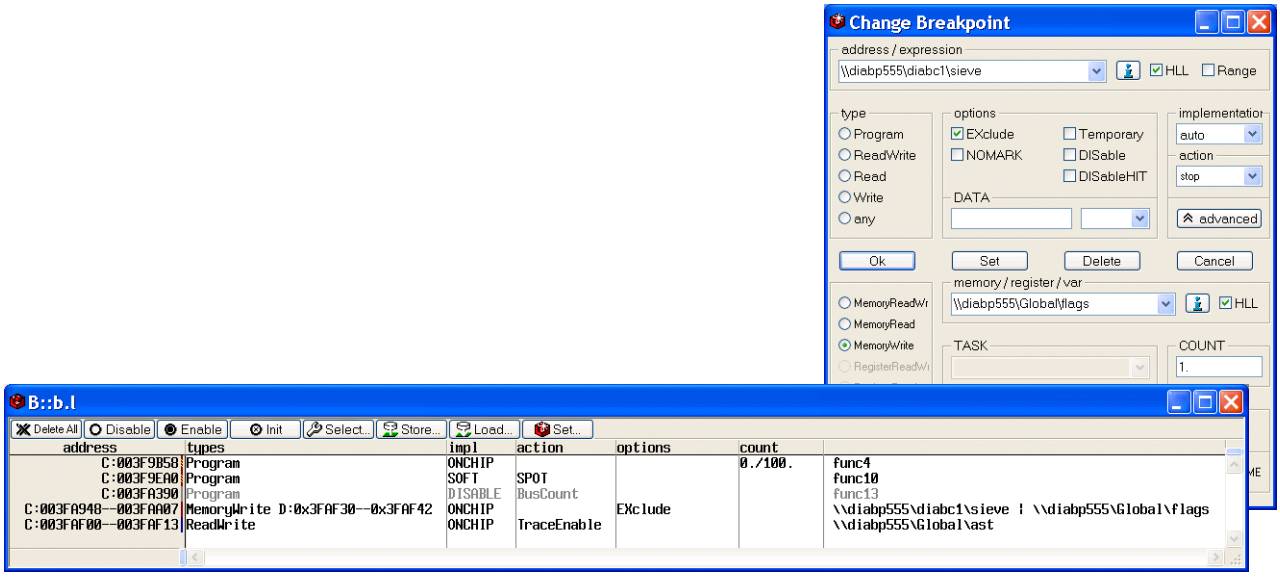
The number of available onchip breakpoints depends on the resources provided by the CPU used.

Advanced breakpoints

The NEXUS provides also a simple way to set complex break conditions:

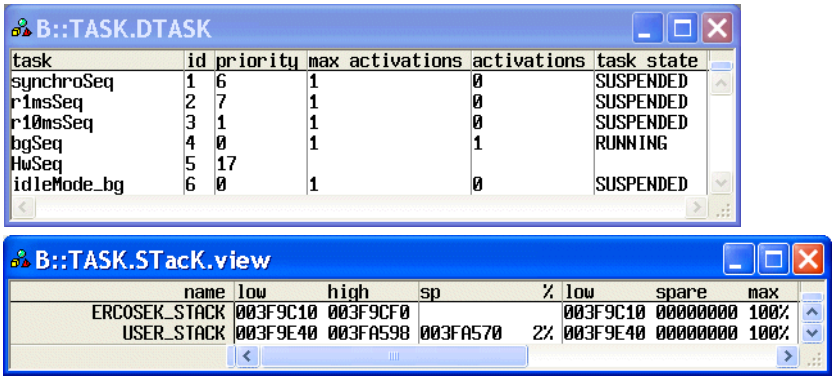
- ❏ Setting of breakpoints to the reading and writing of specific data values
- ❏ Linking the breakpoint with a condition
- ❏ Linking the breakpoint with commands that are executed whenever the breakpoint is reached
- ❏ Spot breakpoints on data accesses

A combination of all 4 new features is also possible.



RTOS Awareness

The NEXUS Debuggers provide display functions, closely mirroring the command set of the integral debugger of the RTOS. The system resources e.g. tasks, objects, partitions, queues, regions and semaphores can be displayed. These functions are also available if the integral debugger is not linked to the software.

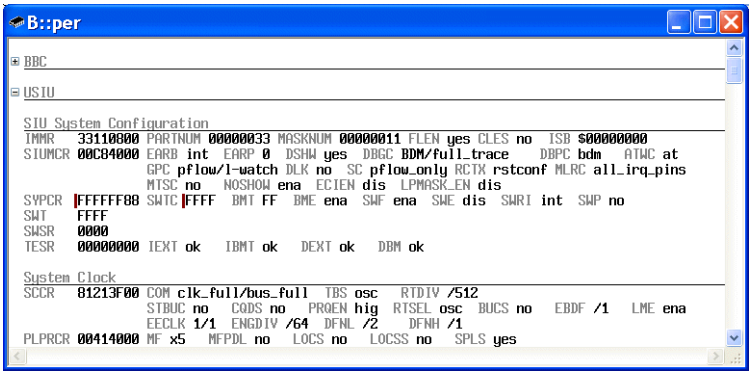


OSEK awareness with ORTI support

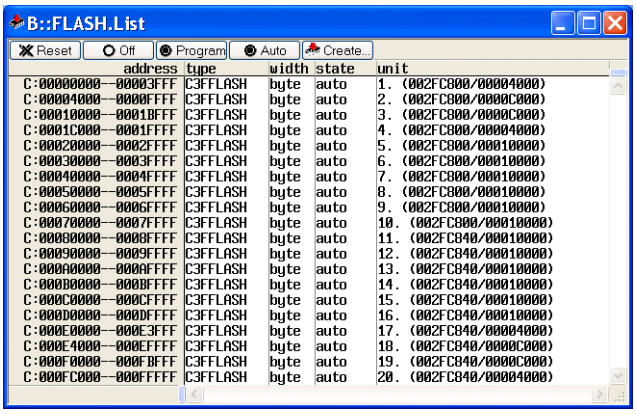
ASAP2 based scaled variable display

Peripherals

- ❏ Display of onchip peripherals
- ❏ User definable display of the onchip peripherals
- ❏ Definition is done interactive supported by softkeys
- ❏ Pull down menues for settings
- ❏ Additional description for each field



Flash Programming

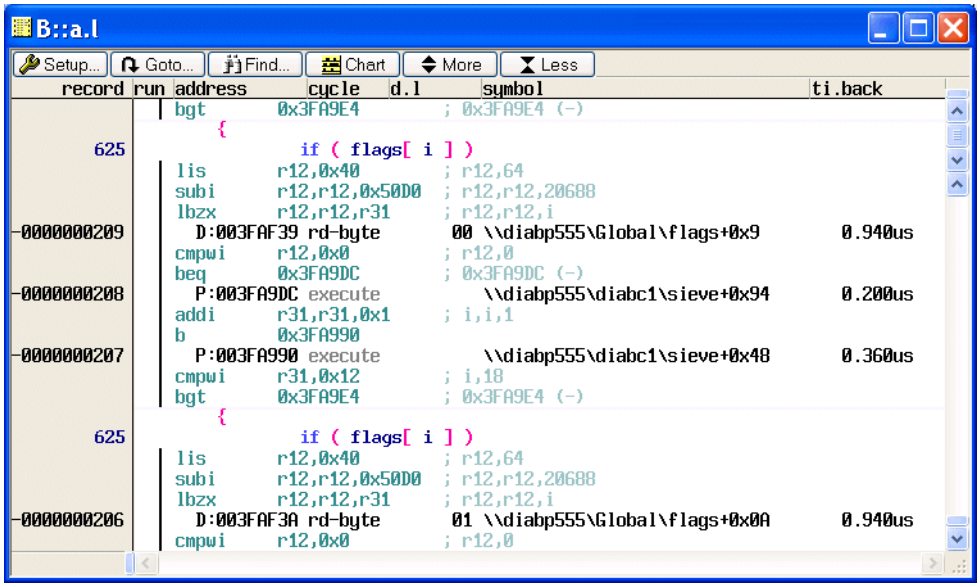


The NEXUS debugger support the programming of external flash memory as well as the programming of internal flash memory of microcontrollers. The programming can be controlled by the debugger or by a routine in the target system.

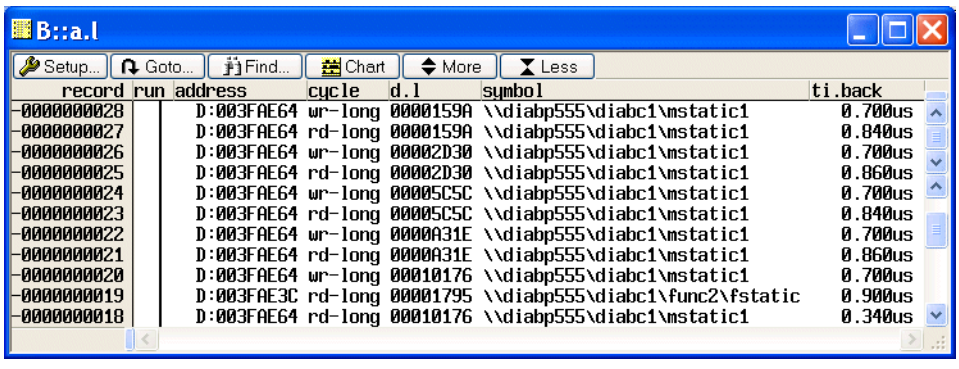
Software Concept Trace

Program/Data Flow Trace

TRACE32-PowerTrace for NEXUS samples all trace messages output via the NEXUS Auxiliary Output Port e.g. branch trace messages, data trace messages….



Selective Tracing

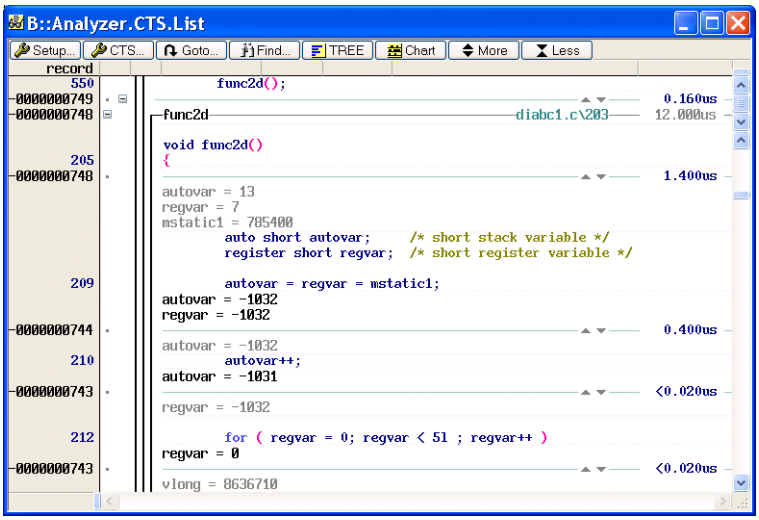


TRACE32-PowerTrace/NEXUS supports selective tracing on 2 data address ranges. Selective tracing is supported on:

- ❏ Specified data accesses only

- Specified data accesses plus the complete program flow information

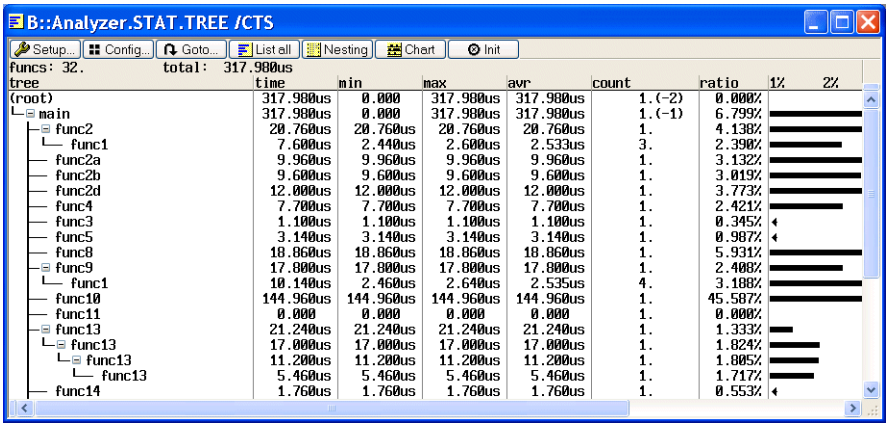
CTS Context Tracking System and SmartTrace



- Reconstucts registers and memory from trace
- SmartTrace fills trace gaps caused by buffer overflow

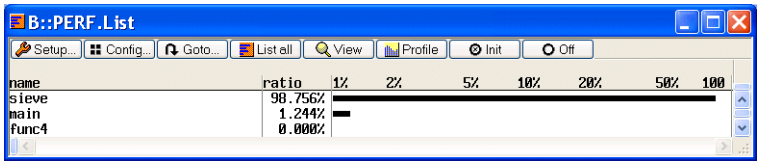
Statistic functions

The very large trace buffer allows function runtime analysis over a long period.



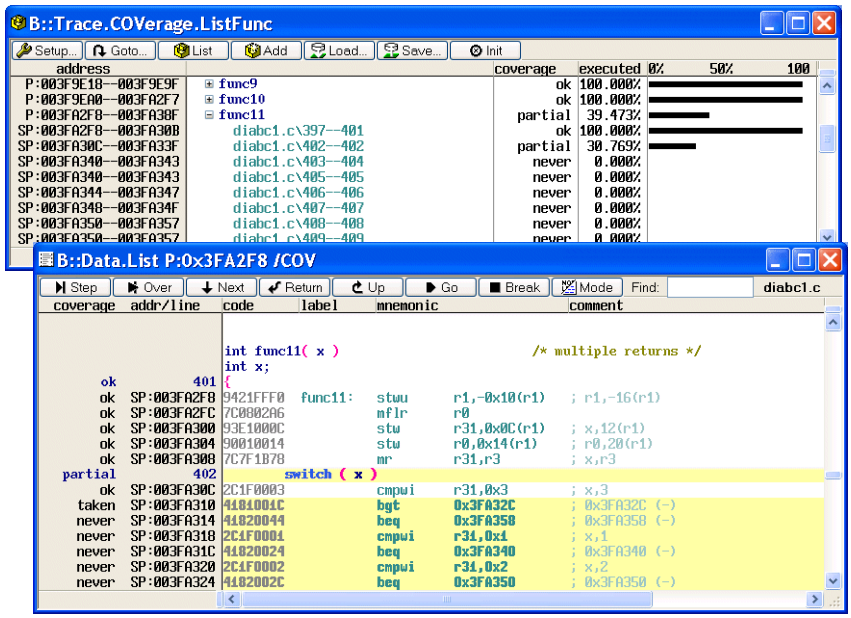
Trace-based Performance Analysis

The performance measurement used by TRACE32-PowerTrace/NEXUS is a statistical process. To determine for example which function or which module uses the greatest proportion of the total runtime the recording into the trace memory is stopped briefly to determine the current program counter contents. This measurement has absolutely no influence on the real-time behaviour.



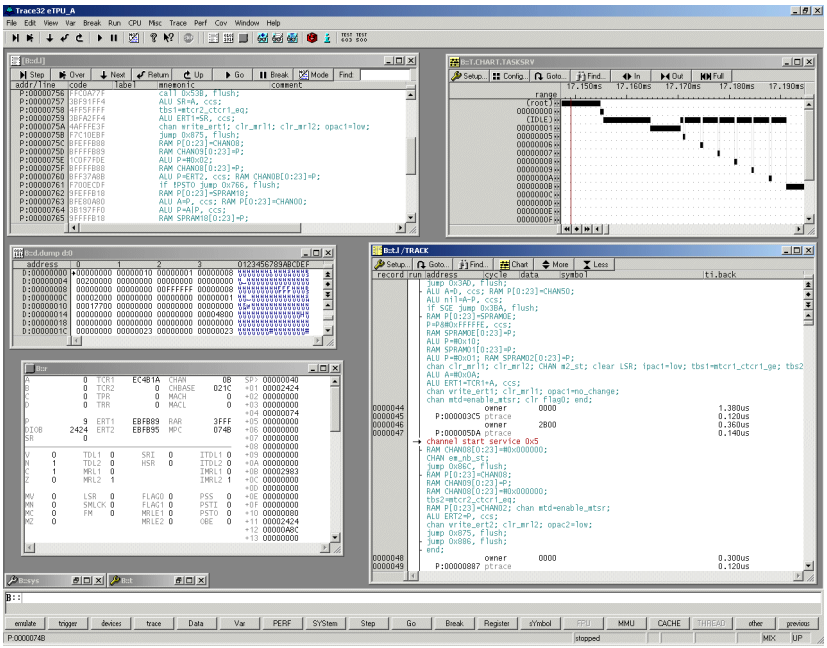
Code Coverage

It is also possible to perform a code coverage analysis based on the comprehensive information from the trace memory.



eTPU Support

- ❏ Full-featured Debugger and Trace
- ❏ Source and HLL debugging
- ❏ Support for all Onchip breakpoints
- ❏ View of all eTPU registers
- ❏ Debugging of all eTPUs and PPC synchronously
- ❏ CTS (Context Tracking System)



Code Compression

- ❏ Will be supported for future MPC55xx devices

Standby Mode

Standby mode and debugging thru power-down cycle is supported.

CTU (Complex Trigger Unit)

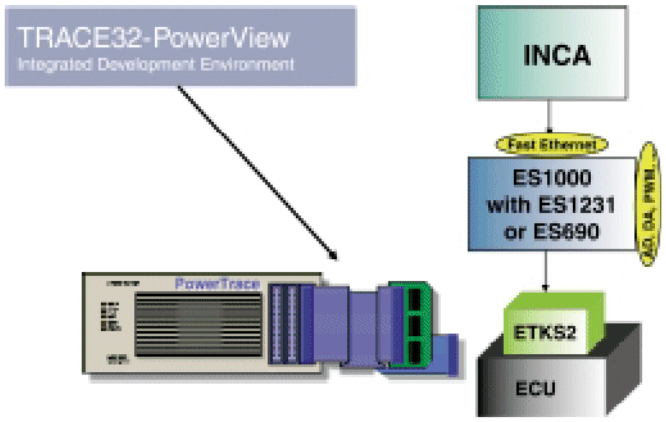
- ❏ Selective data trace
- ❏ Markers
- ❏ Trace control
- ❏ Counters
- ❏ 4 trigger levels
- ❏ Trigger inputs and outputs

Trace

- ❏ 4 bit mode
- ❏ 12 bit mode

ETK Support

The NEXUS for PowerPC can work with ETAS ETK



DSPACE Support

Fast prototyping and debugging simultaneously.

Supported Processors

tbd

Operation Voltage and Frequency

Operation Voltage

This list contains information on probes available for other voltage ranges. Probes not noted here supply an operation voltage range from 4.5V to 5.5V.

tbd

Frequency Trace

The maximum operation frequency of TRACE32-RISC Trace or PowerTrace depends on:

- ❏ The max. frequency of the CPU
- ❏ The number of waitstates (bus trace)
- ❏ The divide factor between trace clock and core clock
- ❏ The speed of the trace adapter

Dimensions and Adapters

Connector (MICTOR)

Signal	Pin	Pin	Signal
MDO12	1	2	MDO13
MDO14	3	4	MDO15
MDO09	5	6	(CLKOUT)
N/C	7	8	MDO08
RSTIN-	9	10	EVTI-
TDO	11	12	VTREF
MDO10	13	14	RDY-
TCK	15	16	MDO07
TMS	17	18	MDO06
TDI	19	20	MDO05
JCOMP	21	22	MDO04
MDO11	23	24	MDO03
RESETOUT	25	26	MDO02
TDET/WDTDIS	27	28	MDO01
BGRNT	29	30	MDO00
N/C	31	32	EVTO-
N/C	33	34	MCKO
BREQ	35	36	MSEO1-
N/C	37	38	MSEO0-

Connector (Glenair)

Pin	Signal
1	N/C
2	N/C
3	N/C
4	ARBREQ(TOOLIO0)
5	TDO
6	RDY-
7	RSTIN-
8	VREF
9	EVTI-
10	GND
11	TRST-
12	GND
13	TMS
14	GND
15	TDI
16	GND
17	TCK
18	GND
19	MDO0
20	GND
21	MCKO
22	GND
23	EVTO-
24	GND
25	MSEO0-
26	MDO9
27	MDO1
28	GND
29	MDO2
30	GND
31	MDO3
32	GND
33	ARBGRT(TOOLIO1)
34	GND
35	MSEO1-
36	GND
37	MDO4
38	GND
39	MDO5
40	GND
41	MDO6
42	GND
43	MDO7
44	GND
45	MDO8
46	GND
47	MDO10
48	GND
49	MDO11
50	GND (TDET)
51	RSTOUT(VENIO2)

Connector (SAMTEC 50)

Signal	Pin	Pin	Signal
MSEO0-	1	2	VREF
MSEO1-	3	4	TCK
GND	5	6	TMS
MDO00	7	8	TDI
MDO01	9	10	TDO
GND	11	12	TRST- (JCOMP)
MDO02	13	14	DBGACK- (RDY)
MDO03	15	16	EVTI-
GND	17	18	EVTO-
MCKO	19	20	RSTIN-
MDO04	21	22	RSTOUT
GND	23	24	GND
MDO05	25	26	CLKOUT
MDO06	27	28	TD/WDTE
GND	29	30	GND
MDO07	31	32	DAI1
MDO08	33	34	DAI2
GND	35	36	GND
MDO09	37	38	ARBREQ
MDO10	39	40	ARBGRT
GND	41	42	GND
MDO11	43	44	MDO13
MDO12	45	46	MDO14
GND	47	48	GND
MDO15	49	50	N/C

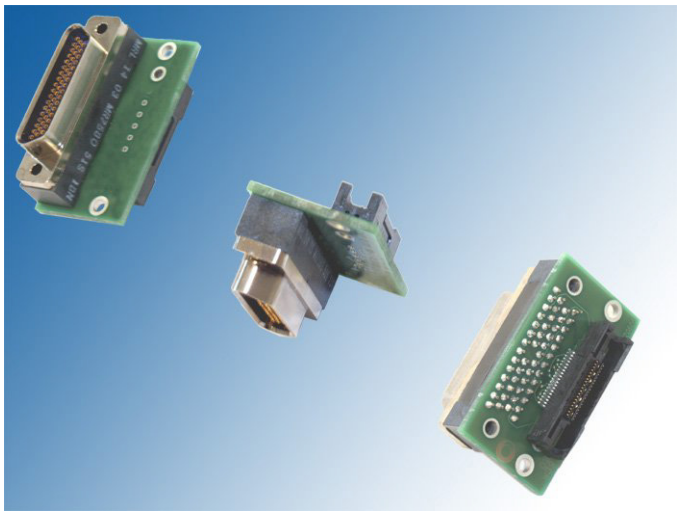
Table 1:

Connector (SAMTEC 20)

Signal	Pin	Pin	Signal
MSEO0-	1	2	VREF
MSEO1-	3	4	TCK
GND	5	6	TMS
MDO00	7	8	TDI
MDO01	9	10	TDO
GND	11	12	TRST- (JCOMP)
MDO02	13	14	DBGACK- (RDY)
MDO03	15	16	EVTI-
GND	17	18	EVTO-
MCKO	19	20	RSTIN-

Table 2:

Modules and Adapters



tbd

Order Information

Module Description

Detailed Order Information

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