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Hua, Yuan ; Lu, Qi ; Li, Shuangmu ; Zhao, Bo; Du, Sijun

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A 90.6% Efficient, 0.333 W/mm^2 Power Density Direct 48V-to-1V Dual Inductor Hybrid Converter With Delay-Line-Based V2D Controller

Yuan Hua, Qi Lu, Shuangmu Li, Bo Zhao, *Senior Member, IEEE*, and Sijun Du, *Senior Member, IEEE*

***Abstract*—This brief presents a 48V-to-1V 10-level dual inductor hybrid converter (DIHC) containing 11 on-chip switches and an off-chip gallium nitride (GaN) switch. Thanks to the 10-level Dickson switched-capacitor (SC) circuit, most of the voltage stress will be taken over by off-chip capacitors, which reduces the voltage stress of each switch to 4.8 V and takes full advantage of the voltage pressure on the 5-V on-chip transistors. This proposed structure is implemented in a 0.18-μm BCD process to convert 48-V input to 1-V output with up to 18-A current load. The post-layout simulations show that a peak power efficiency of 90.6% can be achieved at 5.2-A loading and the power density is about 0.333 W/mm^2 considering the power stage area.**

***Index Terms*—Hybrid DC-DC converter, 10-level, 48V-to-1V, switched capacitor, GaN switch, 5-V on-chip transistors.**

I. Introduction

THE RAPID development of automotive applications and data center causes demand for efficient DC-DC converter. Compared to a 48-/12-/1-V DC-DC converter, the direct 48-/1-V architecture can reduce I^2R distribution loss by 16 times and increase the power density. However, for high voltage converters, achieving extremely short on-time and improving efficiency have always been a major challenge.

To address these challenges, several switched-capacitor based hybrid topologies have been explored. A N-level flying capacitor multilevel (FCML) converter is presented in [1]. 2(N-1) switches and N-2 flying capacitors are needed, and with current-limit control, voltage balance of capacitors can be achieved. A peak efficiency of 85% can be reached for a 48V-to-2V converter. However, high conduction loss in the FCML converter due to multi-switches in series limits the output current. To efficiently utilize the switches, [2] adopts a hybrid Dickson switched-capacitor converter. Split-phase control is used to achieve complete soft-charging. However, its duty cycle is reduced by 2, $D = \frac{NV_{out}}{2V_{in}}$. Thus, [3] presents a dual inductor hybrid converter (DIHC). Soft-charging is achieved by optimizing the size of the flying capacitors. Two naturally interleaved inductors here can support large output current and produce the original duty cycle, $D = \frac{NV_{out}}{V_{in}}$, realizing large conversion ratio. However, all these converters mentioned above need high voltage-stress transistors. A 12-level hybrid Dickson converter is introduced in [4]. In this architecture, the capacitors take over most of the input voltage, making the circuit to be an equivalent 4V-to-1V converter. This allows the on-chip 5-V transistor in the 48 V design. However, the 5-V transistor here only bears 4-V voltage.

In this brief, a 10-level Dickson switched-capacitor connected with a two-phase switched-inductor circuit is proposed, which turns the 48-V into a 4.8-V equivalent input. The proposed design achieves higher overall efficiency compared to state-of-the-art designs with less on-chip and external switches. This brief is organized as follows. Section II describes the overall architecture, operation principle and circuit implementation of the proposed converter. The simulation results are presented in Section III, where also the comparisons between this brief and the previous ones are discussed. Finally, a conclusion is drawn in Section IV.

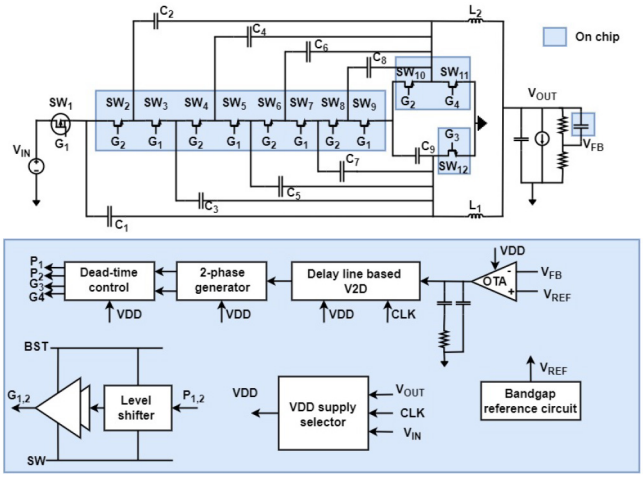

Fig. 1. Detailed circuit diagram of the proposed DIHC.

II. Proposed Topology

A. Overall Architecture

Fig. 1 shows the detailed block diagram of the proposed 10-level dual inductor hybrid converter with a delay line based voltage to duty cycle (V2D) controller and a type-III compensator. 10 high-side switches SW_1-SW_{10} are connected in series, and two low-side switches SW_{11}-SW_{12} are connected between two inductors L_1, L_2 and ground. The SW_1 is an off-chip e-mode GaN FET (EPC2035) with maximum 60-V

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Yuan Hua, Qi Lu, Shuangmu Li, and Sijun Du are with the Department of Microelectronics, Delft University of Technology, 2628 CD Delft, The Netherlands (e-mail: sijun.du@tudelft.nl).

Bo Zhao is with the Institute of VLSI Design, Zhejiang University, Hangzhou 310058, China.

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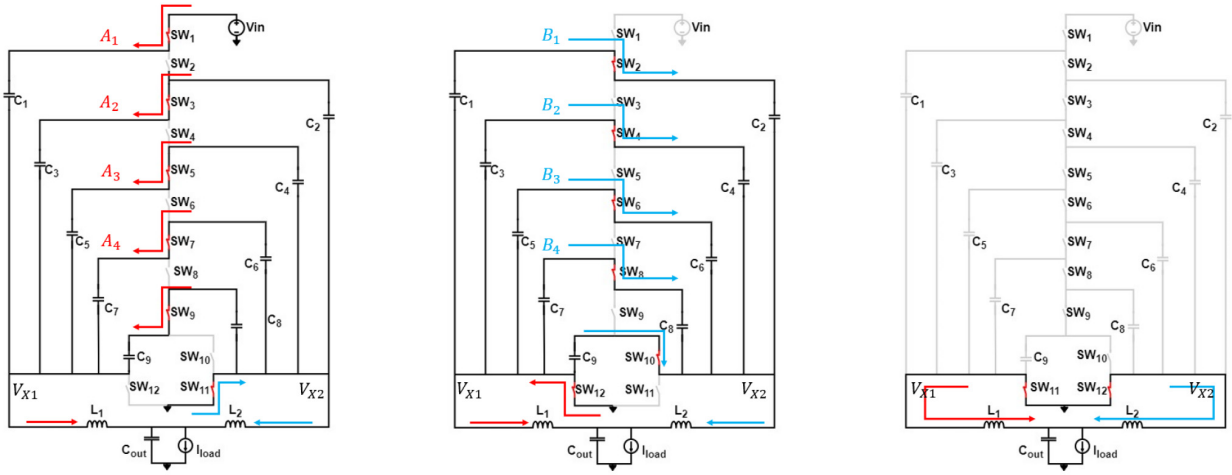


(a) State 1 (b) State 3 (c) State 2 and 4

Fig. 2. Operation states of the proposed structure.

continuous V_{DS} to block the full input voltage at the power-on period, and SW_2-SW_{12} are on-chip 5-V NMOS switches. The proposed converter includes 9 capacitors. The switches and capacitors form a 10:1 Dickson step-down converter and the hybrid converter forms a 4.8:1 equivalent Buck converter. The input voltage for the hybrid can be considered as 4.8 V, which makes the stress voltage being fully utilized by 5-V on-chip MOSFET devices. Also, the overall structure has reduced the number of both transistors and capacitors by 2 compared to the 12-stage converter presented in [4] which leads to a better performance in power efficiency and excellent switch quality. Besides, a VDD supply selector, which mainly consists of an low-dropout linear regulator (LDO) and 1:5 SC DC-DC converter, inherits the fast transient response of LDO and the high efficiency of SC converter, providing the power for the feedback circuit and reducing the its impact on the efficiency in the steady state.

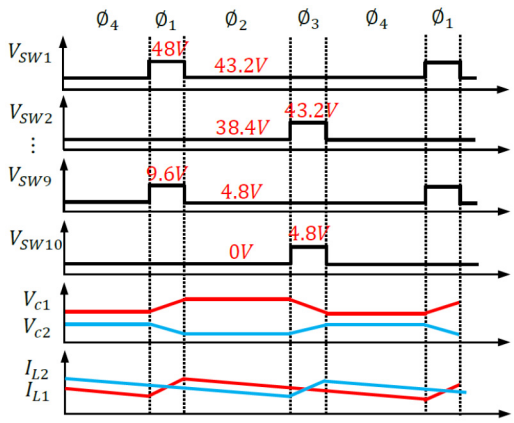


Fig. 3. Operation waveforms.

B. Operation Principle

The 10-level DIHC converter's operation is similar as the original DIHC converters [3]. Fig. 2 demonstrates the four states of the proposed converter. Components in grey are in idle state. Operation waveforms are shown in Fig. 3.

State $\phi 1$: The odd-number switches turn on and the odd-number capacitors are charged. Inductor L_1 stores the energy and L_2 releases the energy. The power supply is connected to the whole circuit to provide power. The current flow is shown in Fig. 2(a).

State $\phi 3$: The even-number switches turn on and the even-number capacitors are charged. L_1 releases the energy and L_2 stores the energy. The current flow is shown in Fig. 2(b).

State $\phi 2$ and $\phi 4$: The low-side switches turn on and all the other switches turn off. The capacitors are idle. L_1 and L_2 will be the power supply for the converter. The current flow is shown in Fig. 2(c).

For continuous conduction mode, according to the inductor voltage-second balance, if the same duty cycle is applied to state 1 and state 3, expressions for the conversion ratio and flying capacitor voltages during the steady state are given as

$$D = \frac{V_o}{V_{in}/10} \tag{1}$$

$$V_{Ck} = \frac{10-k}{10} V_{in}, k = 1, 2, \ldots, 9 \tag{2}$$

where, V_{Ck}, V_{in}, and V_o are the average flying capacitor voltages, input voltage and output voltage, respectively [6].

To maintain capacitor charge balance, charges shared among all the flying capacitors need to be the same, thus, $I_{Ck} = I_{C(k+1)}$. Inductors L_1 and L_2 see the same number of capacitors in both branches, which results in the same average current in the two inductors. This indicates that the current balance is automatically achieved [4]. The inductor current ripple in the inductors is given as

$$\Delta i_L \approx \frac{V_o(1 - 10V_o/V_{in})}{f_{SW}L} \tag{3}$$

C. Driver Design

The driver circuit contains a bootstrap circuit, a level shifter and a buffer driver.

Directly producing the bootstrap voltage from 48-V input could result in considerable loss, particularly for the lower level switches [4]. Thus, two types of driver circuits are used for the 10 high-side switches, shown in Fig. 4.

A dual level shifter (DLS) with both pulse-triggered (PT) and level-triggered (LT) level shifter [9] is adopted, shown

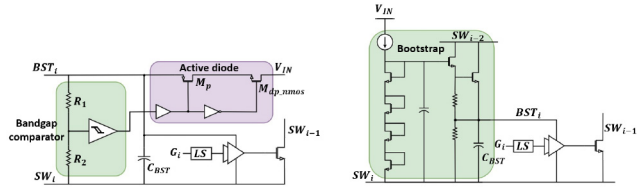


Fig. 4. High-side drivers (a) for SW_1 and SW_2 and (b) for SW_3 - SW_{10}.

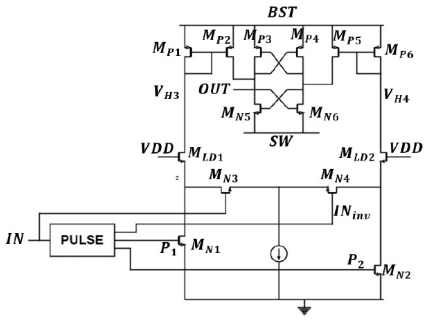


Fig. 5. Schematic of a dual level shifter.

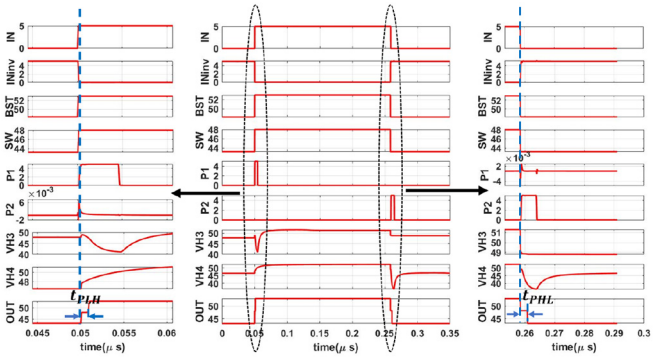


Fig. 6. Timing waveforms of DLS.

in Fig. 5. The pulse-triggered level shifter establishes the signal at the rising and falling edges of the input control signal, with short propagation delay and relatively large instantaneous power consumption. The level-triggered level shifter is to maintain the signal, after this brief pulse has vanished. The propagation delay is relatively long, but the average power consumption is low. The two collaborate to ensure fast and accurate delivery of the low-side control signal to the high-side. Timing waveforms of this DLS are shown in Fig. 6. Simulated propagation delays of t_{PLH} and t_{PHL} are 0.9ns and 2.3ns.

D. Delay Line Based Voltage to Duty Cycle Controller

In this brief, a delay-line based V2D controller with calibration loop is adopted to fit the high switching frequency used and overcome the delay-related problems caused by the comparator in the conventional ramp-comparator-based V2D controller. The block diagram is shown in Fig. 7. It consists of two parts, a fixed small duty cycle generator and a V2D controller. Two same V2D cell are used in each part to realise the bias calibration [8]. Fig. 8(a) shows the V2D cell in the V2D controller. It generates a duty cycle signal by changing the delay of the falling edge of the clock based on the control

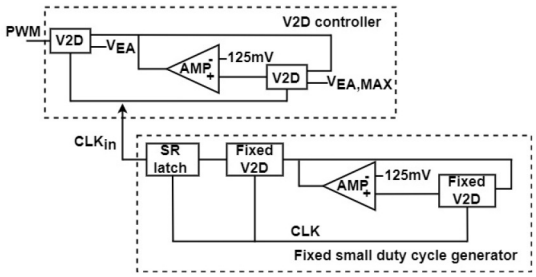


Fig. 7. Block diagram of the delay line based V2D controller.

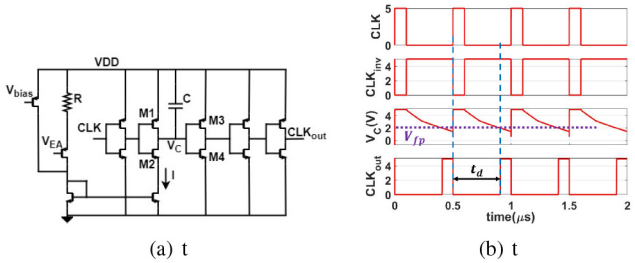


Fig. 8. Schematic (a) and timing diagram (b) of the V2D cell.

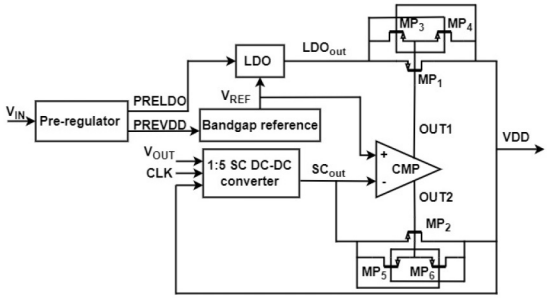


Fig. 9. Block diagram of the proposed VDD supply selector.

voltage V_{EA} from the previous stage. The timing diagram of the V2D circuit is shown in Fig. 8(b). The changed time t_d can be expressed as:

$$t_d = \frac{C(VDD - V_{fp})}{I} \tag{4}$$

where V_{fp} is the flip voltage of the inverter; I is controlled by both the bias voltage V_{bias} and control voltage of the error amplifier V_{EA} in the previous stage.

E. VDD Supply Selector

The proposed VDD supply selector consists of high-voltage pre-regulator, LDO, bandgap reference, comparator, 1:5 SC DC-DC converter and switches, as shown in Fig. 9. The pre-regulator here enables the use of low voltage transistors in the following circuits. For the two switches MP_1 and MP_2, two additional PMOS are added to each switch to connect the bulk of the two switches to the higher voltage level to eliminate the effect of parasitic bipolar [7]. The operation of this proposed supply selector is shown in Fig. 10. At the beginning, the VDD supply is provided by the LDO. As long as the output voltage of SC converter builds up, the output of the comparator changes and SC converter will replace the less efficient LDO to provide the VDD supply. Fig. 11 shows that there is an increase in feedback controller duty cycle when

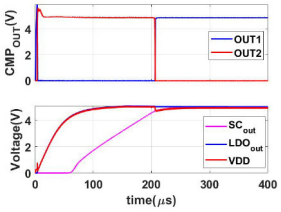


Fig. 10. Operation of the proposed VDD supply selecting circuit.

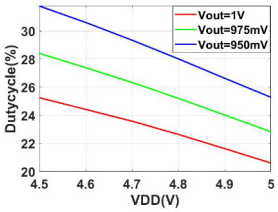


Fig. 11. Duty cycle with VDD.

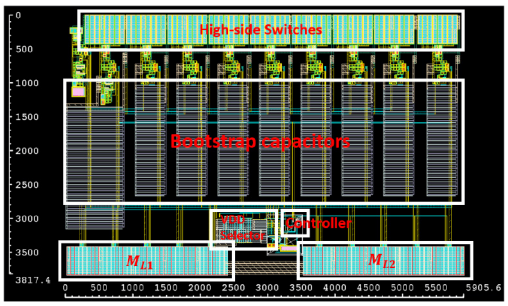
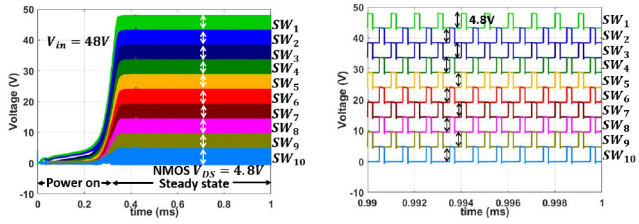


Fig. 12. Layout of the proposed converter with an area of 3.8mm × 5.9mm.



(a) (b)

Fig. 13. Simulated waveform of switching nodes of NMOS switches during (a) power ON and (b) steady-stage operations.

the VDD supply decreases. This can help increase the load capability of the converter, as when it carries heavy loads, the output voltage may go below 1V and thus the VDD supply also decreases, which can further increase the duty cycle to help the voltage go back to 1V.

III. Post-Layout Simulation Results

The proposed 10-level DIHC converter was designed in a 0.18-μm BCD process and the results are based on post-layout simulations of the whole chip. Fig. 12 shows the layout of the proposed converter. The active size is 3.8mm × 5.9mm, with an area of around 22 mm^2. The converter was simulated under the following conditions: input voltage is 48 V, output voltage is regulated at 1 V, and the switching frequency is 1 MHz. GaN Spectre model provided by EPC is used for SW_1 switch.

Fig. 13 shows the simulated waveforms of the switching nodes. During the power-on period, only SW_1 (GaN) takes

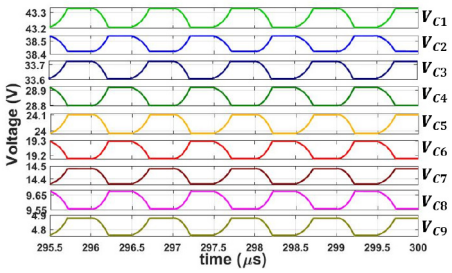


Fig. 14. Simulated waveform of flying capacitor voltages.

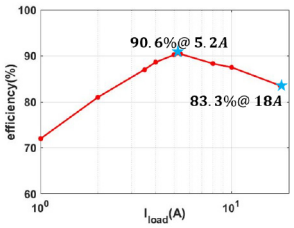


Fig. 15. Simulated power efficiency.

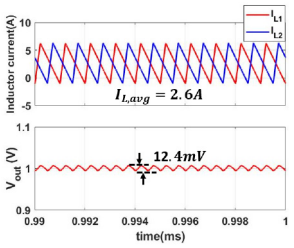


Fig. 16. Inductor current and output voltage at the optimum load.

up to 48-V voltage stress and all NMOS switches take up to 4.8-V voltage stress to secure a safe power-on stage for these 5-V devices. During the steady state, as shown in Fig. 13(b), the voltage swing of all switching nodes is 4.8 V, which is $V_{in}/10$, i.e., the voltage of SW1 is between 48 V and 43.2 V. Operation waveform of flying capacitor voltages is shown in Fig. 14.

The simulated efficiency values in a range of load current are shown in Fig. 15. Taking all the on-chip parasitics into account, the converter achieves a peak efficiency of 90.6% at 5.2-A load. Simulated under different corners, the peak efficiency does not seem to have changed much. When considering the parasitics on the testing PCB, this value will be slightly lower. For a large range of load current from 2 A to maximum 18 A, the efficiency is above 80%. The inductor current and output voltage at the optimum load (I_{load} = 5.2 A) are illustrated in Fig. 16. The output voltage is maintained at 1 V with a small ripple of 12.4 mV. The inductor current waveform shows that there is uniform current distribution between the two inductors. Fig. 17 shows the simulated load transient responses of the proposed converter. The output capacitor is $47\mu F \times 2$ with 5 mΩ ESR for each. When load current steps up from 0 A to the optimal load current 5.2 A, the undershoot voltage is 46.4mV and the recovery time is about 4μs. When load current steps down, the recovery time is 3.7μs, and the overshoot voltage is 50mV. The proposed converter performs a quite fast transient response.

Fig. 18 gives an estimated loss breakdown based on post-layout simulation results. The proposed design adopts 1 μF capacitor with 5 mΩ for all flying capacitors, and 110 nH

TABLE I
COMPARISON WITH THE PREVIOUS WORK

Structure	Dual-phase dual inductor [5]	Dual-phase multi-inductor [6]	12-level Dickson [4]	This work
V_{in}[V]	48-54	48	36-60	48
V_{out}[V]	1-2	1-5	0.5-1	1
Switching frequency [KHz]	300	330	2500	1000
Inductors [H]	$1.5\mu \times 2$	$1\mu \times 4$	$110n \times 2$	$110n \times 2$
Capacitors [F]	5 C_{fly} $(2.2\mu, 1.5\mu \times 2, 1\mu \times 2)$ + 1 C_{out} (6.8μ)	3 C_{fly} $(5.8\mu, 5\mu, 4.3\mu)$ + 1 C_{out} (unknown)	11 C_{fly} $(1\mu \times 11)$ + 1 C_{out} $(47\mu \times 4)$	9 C_{fly} $(1\mu \times 9)$ + 1 C_{out} $(47\mu \times 2)$
Power transistor	8 GaN	8 GaN	13 On-chip 5V MOSFET + 1 GaN	11 On-chip 5V MOSFET + 1 GaN
I_{omax}[A]	10	100	8	18
Peak efficiency when $V_{in} = 48$V	93% (measured)	90.9% (measured)	90.2% (measured)	90.6% (post-simulation)
Power density $[W/mm^2]$	0.00147	0.0178	0.16	0.333

* Calculated from 18 A maximum load current and power stage area (around 54 mm^2) estimated from [4].

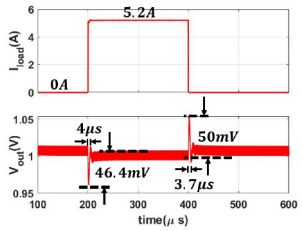


Fig. 17. Simulated load transient responses between 0 and optimum load with $C_{out} = 47\mu$F×2.

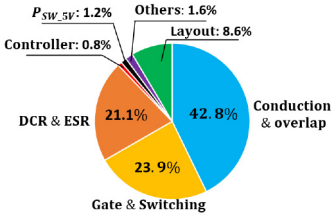


Fig. 18. Estimated loss breakdown at the optimum load.

inductor with 3 mΩ DC resistance for the two inductors. The conduction and overlap loss, the gate and switching loss, the DCR and ESR loss, and the layout loss account for 42.8%, 23.9%, 23.1% and 8.6%, respectively. For the gate and switching loss, more than half of it is consumed by the switches SW_1 and SW_2, as their bootstrap voltages are directly powered by the input voltage.

The comparison between this proposed 10-level DIHC and state-of-the-art designs is shown in Table I. Compared with the 12-level converter in [4], this converter uses two less on-chip switches and two less flying capacitors to achieve 48-V to 1-V conversion. It is able to carry maximum 18-A load, and achieves higher peak efficiency at 90.6% and more than two times higher power density. Compared with two other works, the proposed design only employs one single off-chip GaN switch, which significantly reduces the system form factor.

IV. CONCLUSION

In this brief, a novel 10-level Dual Inductor Hybrid Converter (DIHC) is presented, which converts 48 V directly to 1 V at 1-MHz switching frequency for data center applications. The proposed converter takes full advantage of the voltage pressure on the 5-V transistors. This converter exhibits higher efficiency and improved power density compared with the state-of-the-art works, achieving 90.6% peak power efficiency with loads up to 18 A and about 0.333 W/mm^2 power density. Besides, the efficiency can stay above 80% in a large range of load current from 2 A to 18 A. The performance of the proposed design has been well verified with post-layout simulations designed in a 0.18-μm BCD technology.

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