

# RIDLEYBOX®



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NEW ACTIVITY

Paul Shepherd 1 hr
Has anyone used supercapacitors instead of electrolytics for bulk capacitors? AVX, for example, offers 20V, 6.8mF capacitors which could be suitable for a bulk capacitor on a 12V rail. In high pulse-load applications, it seems like this could be a good option to reduce the voltage drop compared with electrolytics. In my case, I have a 2ms, 1A pulse current, and I'm working aerospace, so cost isn't a big barrier.
Thanks!
4 7 Comments

- Sandeep Kr What is the internal resistance and impedance In your desired frequency range for this particular supercap?
Alex Porter Some super caps have a fairly high impedance so watch out
Dave Lafferty I have used Cap-X and Some supercap.modules.from Tecate Group. Make sure to keep the ESR low to prevent voltage dip.
Hamish Laird And super cap lifetime engineering is a bit of a challenge

there for a few ms.

Like · Reply · 33m



**Paul Shepherd** So I guess the analysis is to compare the higher ESR and higher Capacitance of the super cap vs an electrolytic.

Like · Reply · 32m



**Cameron Stewart** For a 12V, 1A application this seems like more trouble than it is worth.

A three terminal regulator with a 15V head voltage and an aluminum polymer organic output capacitor would seem like a better approach.  
... See More

Like · Reply · 9m



Write a comment...



**Furkan Eroglu** shared his first post.

New Member · 9 hrs

**BOOTSTRAPPING**

Hello friends, I just opened a facebook account to enter this group. So thank you very much for accepting me.

I want to ask a question, I would be very happy if you can help me.

I've designed a bootstrap circuit that will be use in a circuit with 100kHz PWM signals.

But I got some issues.

1-I can't receive the PWM signals when I connect the oscilloscope to the HIGH SIDE VCC and VEE line when the mosfets are not connected.

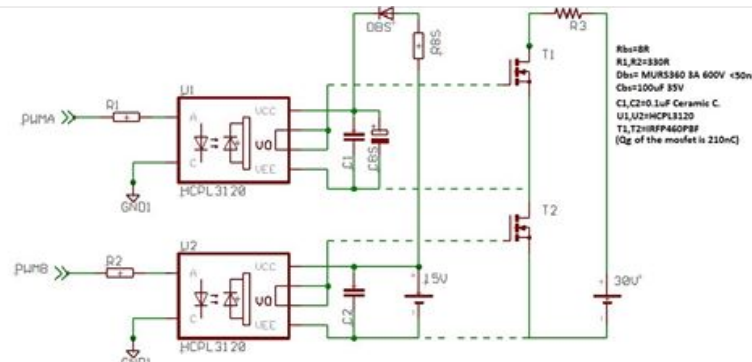
2-Then,by adding the mosfetes to the circuit and also connecting the source of T1 to the drain of T2 and without energizing the circuit,

We took measurements again through VCC and VEE pin, but didn not work again.

3-After adding R3 to the circuit and giving a voltage of 30V, the situation did not change.

where do I make a mistake?

Thanks in advance!



4

21 Comments



Like



Comment



**Col Johns** T2 must be gated on for some pulses to allow the top bootstrap cap to charge thru DBS, if VC1 gets too low the top gate driver may stop, RBS must be 10 ohm or less.

Like · Reply · 9h



**Furkan Eroglu** RBS value is 80hm (4Watts) does that make sense?

Like · Reply · 9h



of 1uF should be fine.  
Also, read some app notes on the design steps for bootstrapped gate drives and you will become the expert. 😊

Like · Reply · 8h · Edited



**Furkan Eroğlu** 🙌 I've calculated the CBS value around the 25.5nFarads  
I thought it was more advantageous to put a higher capacity capacitor, but it seems a wrong method.

Thank you sir.

Like · Reply · 7h · Edited



**Prashant Sharma** **Furkan Eroğlu** put 1 uF, my personal experience 10 years before when calculation gave 27nF so 100nF was quite sufficient but practical need more gate charge, use 1uF and your problems will solve

Like · Reply · 3h



**Shimul Dam** As **Tony Salsich** indicated, RBS and CBS values seem to be too large. You can follow the calculation process given in <https://www.google.com/url?sa=t&source=web&rct=j...>

Like · Reply · 8h



**Furkan Eroğlu** 🙌 Does it make sense to take another bootstrap application notes of another manufacturers? The reason that I'm asking is that I use the device of broadcom.. or are they all the same?

Thank you sir.

Like · Reply · 7h



**Shimul Dam** **Furkan Eroğlu** the calculation process described here is pretty generic in nature.. it requires the total gate charge of the device and the maximum quiescent current of the driver IC.. thus, it should work for other drivers and devices as well

Like · Reply · 7h



**Emre Oğuz** To create the bootstrap voltage on CBS you should turn on T2 for a while to charge CBS capacitor. Because it is relatively a large capacitor. (A few microfarad will be enough.) Then when you start gating T1 & T2 one after another, your ton interval for T2 must be large enough to keep CBS charged.  
And if you don't have an isolated oscilloscope, you should carry your measurement ground to the source of T1 to measure CBS voltage. Because T1 source jumps from 0V to 30V during your switchings.

Like · Reply · 8h · Edited



**Furkan Eroğlu** 🙌 I use an isolated oscilloscope sir, and what do you think about the placement of the load?  
I have read somewhere. They are talking about connecting the load between the reference of the driver on the high side and the ground..

Thank you sir.

Like · Reply · 7h



**Furkan Eroğlu** 🙌 I've taken broadcom's application note AN-5490 as reference.  
I made these calculations looking there like the figure below.

Also the link is below ;

<https://docs.broadcom.com/docs/AV02-2718EN>

In other words, would it be more accurate to choose a value closer to it than a capacitor larger than the value I calculated.

f = gate-drive PWM switching frequency	100kHz
m = modulation index for PWM duty cycle of IGBT, Q1	0.90
I <sub>CC</sub> = gate-drive supply current	5mA
Q <sub>g</sub> = gate charge for IGBT, Q1	210nC
I <sub>CS(max)</sub> = bootstrap capacitor leakage current	4µA
V <sub>max</sub> = maximum ripple voltage allowed	15V

Like · Reply · 8h

**Yuri de Klerk** As Col Johs and Emre Oğuz already noted: You need to turn on T2 first before anything will happen with the high-side (HS).  
Furkan Eroğlu , did you do that?

Like · Reply · 7h · Edited

**Furkan Eroğlu** 🙌 Yup, I've looked to the VEE and VCC pins signals of the low side driver , and it was fine. Also the D-S measurements of T2 were fine. So I just thought the problem was on the high side.

Like · Reply · 7h · Edited

**Yuri de Klerk** So T2 D-S is switching, also when you check T1 ?

Like · Reply · 7h

**Furkan Eroğlu** 🙌 Yes, T2 was working at all of the above steps. I will send the oscilloscope images after lowering CBS and RBS values tomorrow or the next day , that way it will be more useful..

Like · Reply · 7h

Write a reply...

**Rahul Davare** Make sure following is true:  
1. you are using differential probe for measurement (or floating oscilloscope with only one channel connected at a time)  
2. Your bootstrap supply voltage is above the high side UVLO of your driver.  
3. Your input PWM signal is within input specifications of the driver.

Like · Reply · 6h

**Manu Raj** Furkan Eroğlu Opto coupler with 500ns delay is not suitable for 100kHz operation. You can't see anything in the output if you operates at less duty cycle. Try at 20kHz frequency your gate voltage.?

Like · Reply · 5h · Edited

**Tony Salsich** Manu Raj, I think you are referring to pulse width distortion and prop delay differences, in which case the spec sheet does indicate ~350nS, and this can cause problems with low duty pulses.

Like · Reply · 4h · Edited

**Manu Raj** Yes Tony, Its not clear at which duty cycle he is operating. At 100khz the 350ns delay is dominant for low duty.

Like · Reply · 4h

**Furkan Eroğlu** 🙌 Manu Raj sir , I've take the 100kHz signals on the low side.. Only not on the high side

Like · Reply · 40m

Write a reply...

**George William Tyler** Bootstrap needs bottom fet to switch on to charge the top driver bootstrap cap. Bottom fet is in the charging loop

Like · Reply · 2h

Write a comment...

What am I missing? I am designing a power supply and was looking at two different cores made P material from Mag-Inc. The data sheet for P material states that it's core loss at 100mT, 100C, 100kHz is 70 mW/cm<sup>3</sup>. They list a toroid OP47313TC as 129-142 mW/cm<sup>3</sup> and a U core as 201 mW/cm<sup>3</sup> with the same material and under the same conditions. Any help would be appreciated.

Darrell Hambley 16 Comments

Like Comment

**Alain Laprade** Have you compared exposed surface areas for thermal dissipation capability per unit volume?  
Like · Reply · 1d

**Darrell Hambley** This is indeed annoying. Ferroxcube does the same thing. For example, E58/11/38-3C95 data sheet shows this 24.6cc core to be <14.8W at 100C, 200mT, 100kHz which is 602mW/cc but the 3C95 data page states 290mW/cc under the same conditions.  
I can only imagine the higher value is a worst-case parameter but, double the nominal? That would indicate poor variations from batch to batch.  
Edit to my earlier comment. The losses stated in the material data sheets is usually based on the loss of a toroid with an even field. The E core which I referenced has a very non-uniform field because the flux lines have to crowd together to get around corners. This causes hot spots and an average higher loss.  
Like · Reply · 1d · Edited

**Yuri de Klerk** Can not upload .pdf, but the google link is: <https://www.google.nl/url?sa=t&source=web&rct=j...>  
Like · Reply · 1d

**Yuri de Klerk** Last page of this Bruce Carsten piece is about bulk eddy currents. My guess is your problem has to do with it.  
Like · Reply · 1d

**Michael Allen** Thanks for the link. Mag-Inc seems to list the same core loss for almost all of their toroids regardless of their size so it does not appear to be an eddy current issue. I tell my young engineers that when they get old like me they will be able to see the flux too. I can certainly appreciate that with the U core there is a very non uniform cross section and therefore the flux will certainly get crowded and cause a higher loss, Maybe even the almost 3 X that is stated. I also can see the flux is not uniform across the diameter of a toroid but I can not see the 2X that is stated.  
Like · Reply · 1d

**George William Tyler** Flux density for a core is an average over the core cross section figure, actual density varies over the cross section, so loss will vary with core shapes?  
Like · Reply · 1d

**Col Johns** yes and size.  
Like · Reply · 1d

**Yuri de Klerk** For ETD and PQ's that sounds as a logical explanation. But for toroid vs U-core I wouldn't think so since both have a constant core cross section.  
Like · Reply · 1d

**George William Tyler** it's not just a changing cross section, the flux density in a toriod is higher on the inner circumference than outer as circumference varies with diameter, it's also the path length.

**Colin Tuck** Yuri de Klerk the mag path length is much shorter in the corners for rectangular U cores - the flux density B goes way up in the corners - FEA confirms this as does simple loss observation, the density spread is far more linear in a toroid. This is why gapping at the corners is seen in advanced designs ...

Like · Reply · 22h · Edited

**Yuri de Klerk** Ok, ok. So flux density is not uniform in many cases. But according **Michael Allen** the difference for core shapes can range from 70 to 200. Is it really? I can't find this data at manufacturers website, but did you get it directly from Mag-inc engineers Michael Allen ?

Like · Reply · 10h · Edited

**Michael Allen** Yuri de Klerk I am sorry I should have included links to the datasheets. The U core <https://www.mag-inc.com/.../Magn.../Datasheets/0P49920UC.pdf> The toroid <https://www.mag-inc.com/.../Magn.../Datasheets/ZP47313TC.pdf> and the "P" material <https://www.mag-inc.com/Products/Ferrite-Cores/P-Material>

Like · Reply · 4h

Write a reply...

**Colin Tuck** Dimensional resonance is a loss issue as size goes up with frequency - this is why even ferrite cores must be laminated for large cores at high frequencies ...

Like · Reply · 22h

**Alex Berestov** That's weird. Ferrite is isotropic material in respect to wound/laminated cores. However the material losses are stated for toroid about inch and a half in diameter. That's said  
a) each cut destroys material near surface  
b) EE core will have three gaps with fringe losses  
c) it might be B versus delta B in different documents.

Like · Reply · 6h · Edited

**Col Johns** EE core can have 6 gaps ...  
Like · Reply · 8m

**Dan Cousin** Col Johns



Like · Reply · 3m

Write a reply...

Write a comment...

April 3 at 10:37 AM

Many years ago I designed a flyback for 600v mains. I used a a Sanyo 2SK1413. It was a very nice part and I recall they were less than a dollar. I see they are discontinued. I am curious what people are using for flyback 480/590v mains designs. I find it an interesting topic. Also there was an app note by Power Integration that described using 2 800v mosfets in series to accomplish HV switching. I did one of these designs as I had the space and mosfets were SMT which reduced assembly. Jut thought I would throw it out here. I got to thinking about this when the (very good) Snubber post came up.

5

7 Comments



Like



Comment



**Cameron Stewart** Digikey brings up the following replacement:

On Semiconductor  
PN: NDUL03N150CG  
\$2.18 Ea in 100pc quantities  
1500V, 2.5A, 10.5 ohms  
TO-3PL, Fully Isolated Case

I haven't actually used this part. But this is what I probably would use.

Like · Reply · 2d · Edited



**Roswell Bob LaFrank** Nice part. I would use it too. The Sanyo part was in a TO-220 plastic package so no isolation needed. I recall it was higher RDS on, but worked good for a simple housekeeping supply.

Like · Reply · 1d



**David Seal** They are still a lot more expensive, but the new SiC MOSFETS have excellent specs. I have switched to using GaN, which is right about the same price as silicon for similar ratings, but I don't think any of those have that voltage rating yet.

Like · Reply · 1d



**Cameron Stewart** If you don't mind paying \$50 per mosfet rather than \$2 - for a 1A application - a 1500V silicon carbide part is a great way to go .....

Like · Reply · 1d



**Magnus Rosén** SiC mosfet is by far the superior flyback switch in apps above 400V.  
 $\$/rDS(on) * vDS$  is competitive

Like · Reply · 1d



**Colin Tuck** 2SK1413 1500V 2A, MJ8501 ( TO3 can ) 1400V 2.5A  
BUW1215, 1500V 16A TO-247  
KSD5703 1500V 10A Full-pak  
or 1400V IGBT: IRG7PK35UD1 TO-247  
IGA03N120H2 1200V 2A igbt TO-220

Like · Reply · 21h · Edited



**Tony Salsich** STFW3N170 is a great and affordable part.

Like · Reply · 8h



Write a comment...



**Arief Noor Rahman**

Conversation Starter · April 2 at 11:17 PM





converter designer(maybe <1kW/a few A)?

I kinda observe different style of discussion between people from different background, I am just wondering if their background play significant role in the difference...

5

26 Comments



Like



Comment



**John Baillie** One thing that is clearly different is that as you get into high power, you tend to be obliged to design or specify custom parts rather than being to build your converter from digikey stock parts. I've spent months for example specifying high current inductors, meeting with the suppliers, type testing and refining. There is definitely less pressure on cost so auxiliary components tend to be beefy.

[Like](#) · [Reply](#) · 2d



**Arief Noor Rahman** 🗨️ ah...yes, I am also working on 20kW converter...I dont even pay too much attention on the cost...

aux supply just take from meanwell off the shelf...  
gate driver, fully isolated with individual gate driver isolation converter  
control loop bandwidth is relatively low, so no need for very detail fancy modeling

[Like](#) · [Reply](#) · 2d



**Manu Raj** What output voltage and current? And topology?

[Like](#) · [Reply](#) · 2d



**Arief Noor Rahman** 🗨️ Standard two level 3phase inverter, and interleaved SR buck

[Like](#) · [Reply](#) · 2d



**Darrell Hambley** [Arief Noor Rahman](#) That sounds interesting Arief. Is this for an EV? Please tell us more.

[Like](#) · [Reply](#) · 1d



**Arief Noor Rahman** 🗨️ Hi [Darrell Hambley](#), that particular project is actually a high power PFC pre regulator to be used for LED lighting in fishing ship, our customer is LED lighting company trying to get into fishing ship business...

Of course the circuit can also be used in EV charger

Thus, we are also looking for collaboration to work on EV charger and inverter drive application

[Like](#) · [Reply](#) · 13h



Write a reply...



**Jonathan Beaver** Definitely a difference from what I've observed. In the wireless power industry, for all that the physics is the same, the problems encountered, techniques used, solutions preferred and acceptable tradeoffs/outcomes are all different enough to make them essentially incompatible. There are of course other differences that push people's approaches to problems in different directions (cost requirements being the other strong one).

[Like](#) · [Reply](#) · 2d



**John MacLeod** The bangs are bigger (and more expensive!).

The physics is the same, just with different numbers. If you're working with higher power (or frequency), the numbers mean that you'll have to actually deal with more of the small/subtle stuff that is often ignored at lower power (or frequency)

[Like](#) · [Reply](#) · 2d



for high power we tend to easily oversize everything, and assume components to be more ideal since we also dont typically force everything to have very high bandwidth

Like · Reply · 2d

**John MacLeod Arief** I once saw a large air-spaced inductor heat the side of a cabinet red hot - acting as an induction hob (not my design, honestly!). My point is that energy has to go somewhere and won't necessarily dissipate as quietly and easily as it can do on lower power designs. So you have to pay very close attention to all those Joules looking for somewhere to go.

Like · Reply · 2d

**Arief Noor Rahman** Indeed...i spent quite a lot of time designing thermal

Like · Reply · 1d

Write a reply... [emojis]

**Yuri de Klerk** How about testing ? If I start testing a 300W powersupply, I might just power it up with hard mains voltage. That's very quick. If it blows, well, it's repaired in 10 minutes max. For a 6kW it can take the same time for testing, but repair could take several hours. That's something to consider during design also.

Like · Reply · 2d · Edited

**Arief Noor Rahman** I dont know, i never did low power really... I think the circuit in general is same, except maybe more components due to requirement to handle more power..but if everything is purely module based, actually it can be faster

Like · Reply · 2d

**John MacLeod Yuri** I agree. I had one system where the test time was defined by how long it took us to rebuild the converter: Press start; run for less than 1sec; big bang; A full day to rebuild, meanwhile I'd be analysing the single shot scope captures and planning where to put the probes next time. Rinse and repeat. Got so bad I went home, switched on the room light and looked up expecting the bulb to go bang.

Like · Reply · 2d

**Yuri de Klerk John MacLeod**

Like · Reply · 2d

Write a reply... [emojis]

**Ray Ridley** There is a tremendous difference between the high power and low power world. In the last few years, I have gained a good understanding of the design philosophies that make this so.

Like · Reply · 1d

**Arief Noor Rahman** Some of them are?

Like · Reply · 1d



The higher the power goes the scarier it becomes and less errors it forgives and pricier it becomes.  
 1 kW is so different from 10k. Same goes for 100k and so on.  
 Once there was an accident with MW converter. Basically primary feeding busbar at the shop gave up (loose connection I would assume). So one line comes open while unit delivered around 2.5MW. Metal conduit could not contain arc and was blown. Primary power protection kicked in and tripped primary circuit breaker. Bang was damn loud, however everything was contained inside.  
 In regard to damage. For instance 12 gage wire was torn off.  
 At the end just one of four inverters and one rectifier units died.  
 You will appreciate the fact cabinets are made of rather thick steel etc. etc.



Like · Reply · 1d · Edited



**Arief Noor Rahman** 🗨️ Plenty of safety precaution can often be enforced on high power design, maybe some of it due to everybody are more aware of potential trouble

Like · Reply · 9h



**George William Tyler** I remember my first higher power design, I ran a design business from Home, I have the house built with a special "garage" for the business. Had a 63A 220V supply to the house, same as all the rest of the houses. I could not run it off a plug, had to wire it straight into the DB, bypassing the circuit breakers and still had to watch it as it could blow the fuse on the pole! I was really scared of it, had a visit from the customer and when he saw what was happening he disappeared, never saw him again.

Like · Reply · 1d



**Colin Tuck** I love customers who have no appreciation of the art (-not).

Like · Reply · 22h



**Ray Ridley** 🗨️ Here is the anomaly. An experienced engineer can develop a 200 kW product much faster than a low power engineer engineer can make a 1 kW power supply.

Like · Reply · 1d



**Colin Tuck** Not in the least part due to the fact that there are a lot less standards hoops to jump through on a 200kW design ...

Like · Reply · 22h



**Arief Noor Rahman** 🗨️ At 200kW, the switch used is slower, thus it also helps maintain the EMI low

Like · Reply · 9h



Write a reply...



**Alex Berestov** It's probably easier to make 100kW unit than 1kW. 250kW unit went into production after 3rd proto. And the specs were defined along the way. You can't under appreciate collaborative customer.

Like · Reply · 20h

important, a clueless but demanding customer is definitely the worst

Like · Reply · 9h

Write a reply...

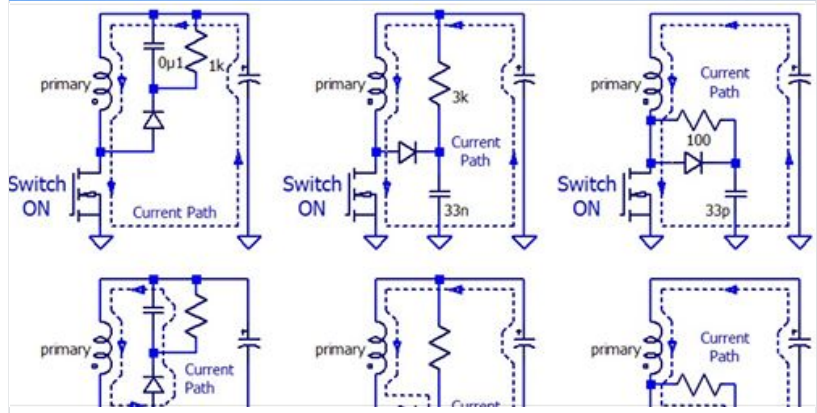
Write a comment...

David Edwards Conversation Starter · April 3 at 5:51 AM

# RCD Clamps and Snubbers

## (for flyback transformers)

### Notice the high di/dt loop areas and component values.



You, Phil Lane and 52 others 12 Comments

Like Comment

**Clive Harvey** With a lower value of R, can we assume lower power for the same voltage spike suppression?

Like · Reply · 2d

**Paul Shepherd** I had to think about this for a moment, because the labelling was not clear to me at first. The "Loop area" label is the subtraction of the two loops, in other words, where current is changing during a switching event. That is why you are analyzing this as the loop area to determine the benefits of the different schematics, which, at first glance, would seem to be functionally equivalent. Nice analysis. Thanks for sharing!

Like · Reply · 2d · Edited

**David Edwards** Thanks for understanding and explaining.

Like · Reply · 2d

instead of across the winding. There are benefits to both, but they seem equivalent if you only consider the node voltage, not the current loop. Both locations will slow the dv/dt of the switched node. A capacitor across the winding will be subject to a bipolar voltage waveform, with lower maximum magnitude, where a cap across the FET will see the full FET voltage stress (which is only positive). The cap across the FET, though, will have a smaller change in the current-flow loop similar to the diagrams here.

Like · Reply · 2d



**Ray Ridley** I think that the traditional has probably evolved that way for a reason. Maybe the answer is in these diagrams?

The snubber cap voltage is minimized for this configuration, I think.

Like · Reply · 2d



**David Edwards** Absolutely, it's a tradeoff.

Like · Reply · 2d



**Ray Ridley** I'm usually a believer in the long time constant of thousands of engineers eventually arriving at the optimum. Kind of like a million monkeys on a typewriter thing, like today's comic strip.

Like · Reply · 2d



**James Keith** In the 2nd and 3rd figures, what is the advantage of connecting the "R" to DC bus vs the Mosfet drain?

Like · Reply · 2d · Edited



**David Edwards** The first and second columns are labeled "RCD Clamp" and have the resistor connected to the high voltage dc bus. The capacitor does not change voltage very much during the cycle and functions as a clamping voltage point. The resistor bleeds off the accumulated charge so that voltage is not pumped up cycle to cycle.

The third column is labeled "RCD Snubber" and the capacitor experiences the same voltage swing as the MOSFET. The capacitor controls the dv/dt of the node transition at higher voltages where the MOSFET capacitance becomes very low (less than 10pF). The example is for the the small high voltage MOSFET in a TOPSwitch IC.

Like · Reply · 2d



**David Edwards** An often overlooked point I was hoping to make clear is that not only is it important to keep loops tight, but one should arrange for switched current to flow in an alternate path that is as much as possible physically congruent with the prior path. This causes the least disturbance (and least EMI).

Like · Reply · 22h 2



**Col Johns** this is also the first 3 rules of power electronics layout ...

Like · Reply · 18h



Write a reply...



**Col Johns** The main issue with having a diode with a catch cap is you invariably get an over-voltage ring up due to the driving inductance and the catch cap - in larger converters you also have the issue of another diode rev recovery every time the switch turns on - exacerbated by having a charged cap right there to supply the current. Empirically the RCD snubber at left in the pictures along with a small RC snubber on the fet (and snubber on the o/p diode(s) ) - is likely the best one can do - short of modifying the fet ON-OFF drive, and of course re-designing the Tx for minimum pri C and min leakage ...

Like · Reply · 18h · Edited 1



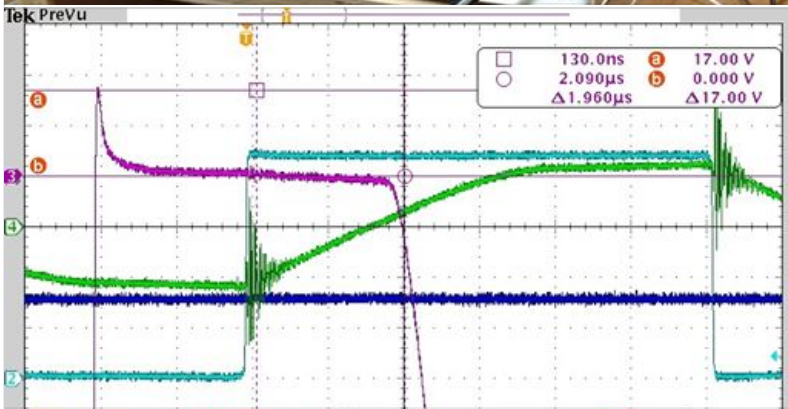
Write a comment...

March 30 at 7:35 PM

I have been working through the wonders of the parallel resonant half-bridge converter. Why? To power this magnificent plasma tweeter (pure bliss from 700 to >50kHz). The whole system needs ~3kv at ~150mA average (five class A current sinks as amplifiers).

What my post is really about is the secondary side rectifiers. One would expect that a PRC running from 81khz to 300kHz requires very fast reverse recovery rectifiers, but one might be mistaken - at least when using minority carrier silicon diodes. Why? Because of forward recovery! The circulating current during diode turn-on can be quite large (SF1600 diodes from Vishay). The forward recovery voltage seen on one diode (one of four in series) was 17Volts. These are overheating and I wondered why. I think this is the culprit. I could be wrong, but I am pretty sure that the super fast (30nS) diodes I was about to drop a lot of cash on will not do better than the 75nS SF1600 parts. Anyone know better? I am prepared to be wrong (that's why I am posting). Thanks!

For those who tend to simulate a lot before trying to build; remember that old saying (I made up): simulation tells you a lot at first, but eventually you spend outrageous amounts of more time trying to learn tiny bits more. Just build and measure...and break things. As long as you have good tools...



Darrell Hambley, Jay Philipbar and 12 others 98 Comments

Like

Comment

**Dan Watts** Not sure this applies in your case but the reverse recovery for some diode can be 10X longer than listed on the top of the data sheet, when the part gets warm. Hot is worse but some 75nS TRR diodes only achieve stated 75nS TRR at low current AND room temperature. I spent a lot of time building my own test set up for measuring TRR at full current and in an oven set at real world operating temp.

Like · Reply · 5d

**Col Johns** The losses during forward recovery are miniscule compared with reverse recovery - also Trr & Irev pk go up with temp quite markedly ...

Like · Reply · 5d

Sometimes it can be huge, almost same as reverse recovery. As you mentioned 17v for forward recovery voltage is large. Then it will come down to turn on current and forward recovery time.

Like · Reply · 5d

**Alex Berestov** Somebody is paid too much 😊

Like · Reply · 5d

**Alex Berestov** Anyway, it's unreasonable to get 3kV from a single rectifier stage severe limiting yourself in hardware availability. 3 or 4 windings with separate rectifiers connected in series will do. There are HV diodes but they would not operate @ 50 kc not mentioning 300. May be SiC p-i-n or Schottky will. Helium powered vanity fair unit owner should stomach \$30 a piece diodes.

Like · Reply · 5d · Edited

**David Edwards** 🗣️ How does such a sound transducer avoid making a lot of ozone?

Like · Reply · 5d

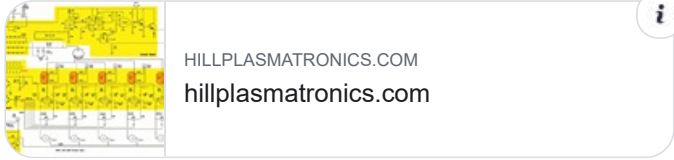
**Tony Salsich** High temps destroy ozone.

Like · Reply · 5d

**Alex Berestov** It's fed by helium (He) from a dedicated vessel. (300 hrs)

Like · Reply · 5d

**Alex Berestov** <http://hillplasmatronics.com/.../10/Failing-Resistors1.jpg>



Like · Reply · 5d

**Tony Salsich** Great comments and insights from you all! Many thanks! I will go back to focusing on the reverse recovery aspect.

This is indeed a very esoteric transducer; these speakers were well beyond the financial reach of most (including me), costing \$12k in 1980's dollars. But I did not buy them - they were a wedding present from Alan and Carol Hill. I was fortunate enough to have worked for him for 12 years and did all the tech work on their design (drew the schematic above). They have not functioned for nearly 33 years, and for all that time I have been thinking about creating a switching PS and a solid state replacement for the 6MJ6 tube amps that control the current.

BTW, Ozone is destroyed by the very high temperature of this glow discharge. That is not to say that no oxides are created...

Like · Reply · 5d

**Jay Phillipbar** Tony Salsich, we need to have a phone call!

Like · Reply · 5d

**Ray Ridley** 🗣️ Do you know the frequency range of the tweeter? Oops, never mind, it is in your post.

A good attempt to make a zero mass speaker, but obviously never caught on. Safety immediately comes to mind. 😊

I am sure your bride appreciated the wedding gift!

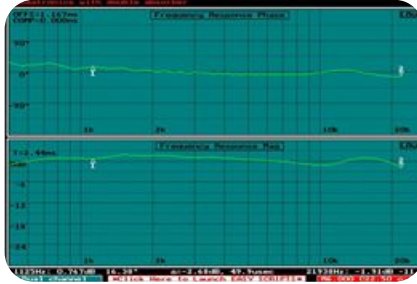
Like · Reply · 5d · Edited

**Tony Salsich** This driver was behind a grounded metal screen in the product.

Like · Reply · 5d



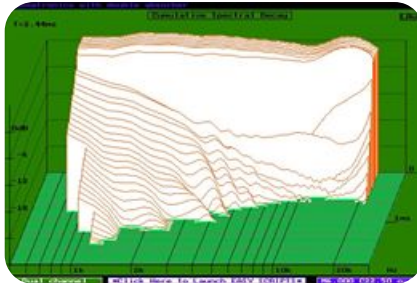
twenty years ago. It has excellent and uniform response.



Like · Reply · 5d · Edited



**Jay Philippbar** Here's a cumulative spectral decay plot of the plasma. No other loudspeaker comes close to this level of acoustic performance as it's free from stored energy and nasty resonances.



Like · Reply · 5d · Edited



**Jay Philippbar** These measurements were made with a microphone and hardware only rated to 20kHz.

Like · Reply · 4d



Write a reply...



**Magnus Rosén** Silicon carbide schottky diode is your answer. Majority carrier and low  $C_j$

Like · Reply · 5d



**Jay Philippbar** Here is one option with a good datasheet and SPICE model. The reverse recovery is spec'ed at 175 degrees C. [http://www.genesicsemi.com/sic\\_pin/GA01PNS80-220.pdf](http://www.genesicsemi.com/sic_pin/GA01PNS80-220.pdf)

Like · Reply · 5d



**Bob Gudgel** So, why aren't there GaN diodes if they are so fast ?

Like · Reply · 5d



**Jay Philippbar** Bob, I asked a few companies that make GaN devices and I never got a satisfactory answer. There was a GaN diode that was created by a German based researcher however it wasn't ready for production. The research papers that I have read use a reconfigured GaN FET. I thought that a diode would be easier to design however it doesn't seem that way. Maybe Alex Lidow at EPC can chime in.

Like · Reply · 5d



**Bob Gudgel** Jay OK great answer ! So evidently not the same as SiC as far as diodes.

Like · Reply · 5d



They are planar devices that work by modulating the presence/conductivity of a two dimensional electron gas (2DEG) that forms spontaneously at the boundary of GaN and AlGaN. There is no junction as there exists in Si diodes.

Some companies have tried to make vertical GaN devices (e.g. Avogy, now defunct) without success. Even if there were vertical GaN devices, given that GaN uses this 2DEG, it would be interesting to see how a diode could be made. It is probably possible as back in the mid-1990s Motorola made some diodes out of GaAs which works on the 2DEG as GaN. Maybe Alex Lidow could comment on this.

[Like](#) · [Reply](#) · 5d · Edited



**Bob Gudgel** What are HEMTs reverse characteristics ? Do they need parallel external diodes when using them ins SMPS circuit ?

I know that HEMTs were used MANY years ago in microwave radio circuits but to me, use in power supplies are more of a recent thing

[Like](#) · [Reply](#) · 4d



**Col Johns** GaN diodes are used in RF ... and of course LED's

[Like](#) · [Reply](#) · 4d · Edited



**Bob White** **Bob Gudgel** GaN HEMTs are more or less bidirectional although they are not symmetric - there is a longer region from gate to drain than from gate to source.

If you ground the gate and pull the drain negative the GaN HEMT will start to conduct when the gate-to-drain voltage is about the threshold voltage. This voltage is much higher than the usual diode forward drop. However, since GaN HEMTs have no reverse recovery adding an external diode with a reverse recovery loss is not usually a winning a proposition. It is better to just turn the device on when it is going to conduct "in reverse" (from source to drain).

Although it was several years ago the basics have not changed. This seminar on GaN devices, which I presented at APEC 2012 (with the support of and in collaboration with EPC) might be of interest:

[http://www.embeddedpowerlabs.com/.../APEC\\_2012\\_Putting..](http://www.embeddedpowerlabs.com/.../APEC_2012_Putting..)

EMBEDDEDPOWERLABS.COM

[www.embeddedpowerlabs.com](http://www.embeddedpowerlabs.com)

[Like](#) · [Reply](#) · 4d



**Jay Philippbar** **Bob White**, have you ever been told that you explain things very clearly? Thanks!!! 😊

[Like](#) · [Reply](#) · 4d



**Bob White** **Jay Philippbar** Thank you for your kind words.

[Like](#) · [Reply](#) · 4d



**Bob White** I found this link after the questions here led me to wonder about GaN diodes. It is long and I have yet to read it all but it looks like a fairly authoritative description:

<https://www.intechopen.com/.../gan-based-schottky-diode>



INTECHOPEN.COM

GaN-Based Schottky Diode | IntechOpen

[Like](#) · [Reply](#) · 4d



**Bob Gudgel** Ahhh yes. Thanks Bob. I keep forgetting that the self-turn-on is just the gate-source TH voltage !





Write a reply...



**Alex Berestov** Does the plasma produce that nasty hissing sound without modulation?

With all that options of a newer devices there are a lot of HV PSU out there. As well as HV diodes and modules like this [www.hvproducts.de](http://www.hvproducts.de). Jusr go easier on frequency and you'll be ok.

Like · Reply · 4d · Edited

^ Hide 51 Replies



**Tony Salsich** No, it is very quiet because it is DC and because the hollow cathodes are shielded from oxidation by the helium flowing through them

Like · Reply · 4d



**Col Johns** Isn't Helium kinda scarce and expensive these days? what is the white cotton wool or mist at the top and bottom please?

Like · Reply · 4d



**Alex Berestov** I used to design ozone generators and discharge is rather loud.  
Col Johns it's likely the felt made of alumina or quartz.

Like · Reply · 4d



**Jay Phillipbar** **Col Johns**, I'll let Tony answer your questions however helium is still low enough cost to be used in millions of party balloons every year. I agree that it's getting scarce.

Like · Reply · 4d · Edited



**Tony Salsich** **Col Johns** Yes, helium is about a dollar a cubic foot, I am told. That adds up to about \$3 per hour to run these things.

The white material is Cerablanket (Alumina wool) that helps control the convective air flow which destabilizes the discharge. This driver has been modified from the original which had a fused quartz plate on top and another (with one inch hole) in the front.

Like · Reply · 4d



**Ray Ridley** 🙄 I'll take a nice ribbon over this. Way too much maintenance needed, I have enough of that already.

Like · Reply · 3d



**Tony Salsich** **Ray Ridley**, listening to the plasmas for an extended period used to make listening to even the best 'normal' speakers a sad experience.

Like · Reply · 3d · Edited



**Ray Ridley** 🙄 I am sure. I wish I could hear them for myself. I just can't imagine the maintenance!

Nothing worse than a harsh tweeter, that is for sure.

Like · Reply · 3d



**Ray Ridley** 🙄 I used the almost weightless Maggie ribbons for many years, so i can imagine how the plasma sounds. I then transitioned to the Newform ribbons. I have some good engineering stories about both of them.....

Like · Reply · 3d



four feet tall.

Part I

We were planning on going to CES (actually T.H.E. show which was concurrent with CES in 2005) to exhibit some amplifiers and preamps. That was what we thought we were good at.

We tried 6 months ahead to team up with speaker makers to exhibit with us. They pretty much universally had the same comment to us - "why should we? The electronics don't make a difference to the sound. All the magic is in the speakers."

So Denise Ridley said, well, just make your own speakers. I don't know anything about speaker making, I replied. Well, take the ones that are in the living room and make it a product. should be easy. Um.....OK. NO problem. Engineering can do that.

She designed the shape of the cabinet, and we sent it a few months later to a wood work place in Seattle to make the parts, planning on veneering upon return.

Three weeks later, 300 lbs of machined MDF were shipped by UPS to Atlanta. None of them packed properly, just loose in a big cardboard box. Every one of them was broken.

Great. Three weeks to the show, no speakers.

Part II soon: finding another vendor with three weeks to go....

Like · Reply · 3d · Edited



**Tony Salsich** We always found that the electronics made a big difference.

Like · Reply · 3d



**Ray Ridley** No kidding. More to come after some food.....

Like · Reply · 3d



**Alex Berestov** Wow what a ramblings! Yes, some do have gold ears, like my daughter. No way anybody seasoned enough can hear 16 kHz just by physiology of it. I use to hear 18.5 kc being a student. After working with high power converters it seems some frequencies can't be recognized anymore.

Like · Reply · 3d



**Ray Ridley** Part II Tweeter ramblings...

So we found another woodworker in Atlanta with three weeks before we had to ship to Vegas. He promised to make wood casings, 3D CNC, fully veneers and finished in 10 days. wow. So we signed him up.

10 days later all is ready and finished for pickup. we took all the drivers and 50 lb tweeters to test install them. The tweeters didn't fit. They were U-shaped bent steel at the back with fairly sloppy tolerance that isn't on the spec sheet.

Options? Either cut into the beautifully finished curly cherry finish, or reduce the size of the tweeter housing. He had a big grinding machine in his factory. Nothing to lose, right? Some delicate ribbon tweeters going through a metal grinder... Can you guess what came next?

Fed the tweeter through, it ground perfectly flat. Lovely. But in the stress of the moment, we didn't realize that all the steel filings would get attracted to the powerful permanent magnets and attach themselves solidly inside the tweeter where the ribbon lived!

Well, the woodworker said, I have a high pressure airhose.....want to try blasting them out? It's moving to the realm of comedy at this point. Not much to lose. Sure. So we did that and it worked like a charm. I gained a great deal of respect for the ruggedness of the Newform tweeters at that point. They tweeters still worked. Now we had four days to assemble, listen for the first time, and ship them all out.

**Ray Ridley** Here is one of the speakers. Not bad for a 10 day fabrication!  
Part III coming....



Like · Reply · 3d · Edited

**Ray Ridley** In hindsight, grinding a steel frame in the presence of a very strong magnetic field was not the best choice. Needless to say, when we ground the second tweeter, we taped up the opening first.  
Good engineers learn fast from their mistakes. 😎

Like · Reply · 3d

**Ray Ridley** Looks like i am down to an audience of one.....

Like · Reply · 2d

**Col Johns** **Ray Ridley** - not at all - great stories - I am sure there are a lot of readers, who, in the best British tradition, smile at the reading but refrain from adding comments to what is already a classic tale.

Like · Reply · 2d · Edited

**Ray Ridley** Yes indeed stiff upper lips and all that. Next chapter has a happy ending but trouble along the way.....

Like · Reply · 2d

**Alex Berestov** What is self-sacrifice (like silence of Spanish infantry no matter what) in regard to the topic?

Like · Reply · 2d · Edited

**Ray Ridley** **Alex Berestov** your posts are always colorfully cryptic.

Like · Reply · 2d

**Bob Gudge** Uh OH. Ray... What is that audiophile looking turntable ?

Like · Reply · 2d

**Jay Philippbar** **Ray Ridley**, keep going!

Like · Reply · 2d

**Bob Gudge** Here's what you need ! Only a couple hundred thousand dollars I think !



Like · Reply · 2d



Like · Reply · 2d

**Bob Gudgel** And then... This is why I live on the street now...



Like · Reply · 2d

**Ray Ridley** Bob Gudgel I resemble that remark.

Haha · Reply · 2d

**Ray Ridley** Bob Gudgel Home made turntable. 😊

Like · Reply · 1d

**Bob Gudgel** Ray Really ? The problem I always had in the 1970s and 80s was low frequency feedback. Tried several ways to acoustically isolate. Things helped of course but never could crank the gain up on certain things. Digital is way better for that now.

Like · Reply · 1d



We arrive in Vegas two days ahead of time, and all our 10 shipped cases are intact. About 800 lbs of equipment. Thankfully it is not a union-run show like APEC, so the shipping, receiving and moving charges to the room are really pretty low. No \$400 trash cans.

One day ahead, we spend 6 hours assembling the speakers that come in 4 parts so none of them are over 60 lbs each. Otherwise you have a 250 lb speaker to move and position - nuts. All sounds good, and we wander around the pre show watching people set up.

One guy was in his room with his powered speakers completely in pieces and he had no EE skills so he was practically in tears. I don't think he ever opened up. Feeling good that we didn't have that happen to us. Had a fun visit with Atmosphere owner as well, very cool guy.

Day of the show - all suited up, champagne on ice to woo the reviewers, turned on the amps - POOF! - we let the smoke out of one of them! Emergency surgery, 1 hour to go, soldering iron and voltmeter the only tools available, plus a complete spare amp to raid parts from, and extra output assemblies.

Two more FET output assemblies blow up after poking on board. At this point, 1/2 hour to go, I am stripped down to my underwear so as not to sweat so much in my nice clothes! No one else can help but look on in horror (presumably at me in my underwear). Sign goes up on the locked door that we'll be opening soon.

Finally find a jumping around voltage on the bias when pushing on the board, and that is traced to a FAILED resistor! Expensive \$5 part with wires bonded on the side of the element in a really crappy manner that didn't survive the shipping. Ohmrite I think, can't remember. It was that best of things to debug, an intermittent, that all of you with experience know all about.

Resistors replaced, last pair of FETs installed, prayers uttered and success! No more smoke. Clothes go back on (I remembered that) door is unlocked and we are ready.

The very first person to walk in the door is none other than Jonathan Valin of the Absolute Sound. (google him if you don't know.) Game on....

Part IV of the saga a little later.

Like · Reply · 1d



**Ray Ridley** <https://www.theabsolutesound.com/.../2019-golden-ear.../>



THEABSOLUTESOUND.COM

2019 Golden Ear Awards:  
Jonathan Valin



Like · Reply · 1d



**Ray Ridley** **Bob Gudge** I understand the LF feedback issue. If I REALLY crank it, there is a 5 Hz resonance in my room. I need to reinforce the floor joists, but I think I will just turn things down.

I have many adventures with LF subsonic feedback, I don't think many on here will care about them though. One experiment involved 1000 lbs of sand under the turntable. As you might know, at low frequencies (ie earthquakes), sand acts a lot like a fluid. that was an interesting lesson.

Like · Reply · 1d



**Tony Salsich** **Ray Ridley** Maybe try the techniques used with laser experiments. I that heard Lloyd Cross once used a bathtub filled with sand and floated on inner tubes to isolate his holography setup. Think of how well that would look in your listening room.

Like · Reply · 1d · Edited



learning.

[Like](#) · [Reply](#) · 1d



**Bob Gudge** Was that tweeter writeup from a CES show ? Did you used o be in the hi-fi business ? I went to CES in LV for several years, late 1970s-early 80s when we had a company (Spectro-Acoustics) As I remember though, they used a labor union ? Maybe I am thinking of CES in Chicago though ? Been to shows in Vegas lately and they do use unions. They're a PITA sometimes to deal with ! Good times though at CES ! I love my bass !

[Like](#) · [Reply](#) · 1d



**Ray Ridley** We entertained the idea for a while. After exhibiting we realized this was a worse business to be in than power supplies, so we decided to keep it as a hobby for the time being.

[Like](#) · [Reply](#) · 1d



**Ray Ridley** T.H.E. show ran at the old las vegas sands at the same time as the CES show. They kept it low cost, but ultimately got steamrolled by the sheer size of CES.

Lots of high-end vendors hated CES. You move the room furniture just 1" and you have a \$400 union bill for your trouble. \$25 bagels as well. In the end though, they had no choice since the press didn't have time to go to T.H.E. show.

On those same lines, we wanted to get a keg of beer for APEC last year, but just couldn't stomach the \$750 price. Plus \$140 per hour for someone to serve it. And 20% service charge. Sheer extortion.

[Wow](#) · [Reply](#) · 1d



**Ray Ridley** You will like this story, Bob. One year at the show, a subwoofer vendor took two rooms and cut a 2' x 2' hole between the two rooms. Then they took a large fan, and modulated the blade pitch with subsonic frequencies to pressurize one of the rooms.

The sound of a helicopter landing was awesome!

Engineers get very creative and crazy when you let them.

If you tried that stunt at the CES venues it would probably cost half a million in room repairs.

Fun times.

[Haha](#) · [Reply](#) · 1d



**Tony Salsich** **Bob Gudge** , We from Plasmatronics were showing at Winter and Summer CES from 1978 through 1980. Maybe you heard the speakers(?).

[Like](#) · [Reply](#) · 1d



**Tony Salsich** **Ray Ridley**, We at Plasmatronics also decided that the audio world was too bizarre. People had the strangest notions - science did (does) not play a big role there.

[Like](#) · [Reply](#) · 1d · Edited



**Ray Ridley** **Tony Salsich** yes see part IV when I write it.

[Like](#) · [Reply](#) · 1d



**Darrell Hambley** **Bob Gudge** CES Chicago, what a memory that was! We were displaying our 'Stereo Phone Mute', our device which softly quieted the stereo when the phone rang. It won one of the 'top 100 products of the year' award.

[Like](#) · [Reply](#) · 1d · Edited



**Bob Gudge** **Darrell** Did you sell any ?

[Like](#) · [Reply](#) · 1d



That is where I heard them and remember them I think. I remember the little arc and the tiny bit of hiss you would hear if you put your ear up to them.

Like · Reply · 1d



**Bob Gudgel** Although, these days, when I think of Plasmatronics, I think of the little solar charge controller company in Australia...  
<http://www.plasmatronics.com.au/>

<b>SMAT</b>	PLASMATRONICS.COM.AU	
	Plasmatronics - Solar Power Regulators	

Like · Reply · Remove Preview · 1d



**Tony Salsich** **Bob Gudgel** My photo above is of the 'naked' driver. I am resurrecting it without the tubes. It's ALIVE!!

Love · Reply · 1d



**Bob Gudgel** But if you use "tubes" you can multiply your profits by X100 !!

Like · Reply · 1d



**Tony Salsich** **Bob Gudgel** Hah! Right you are! The tubes cost us ~\$5 each back in '79. We lost money on every pair of speakers we sold - even at \$12k/pair. The reasons were myriad, but the tubes had little to do with it. BTW, those same tubes are in the \$90 range now (if you can get them). The FETs I am now using are ~\$20 from Digikey - not bad at all.

Like · Reply · 1d · Edited



**Bob Gudgel** I have seen some on YouTube that are making their own vacuum tubes. I kind of miss tooobs. They are noisy and hogs for filament power but are fun in many ways and still good for HF RF amplifiers for ham radio, etc. Imagine making a computer like they used to do with tubes !



Like · Reply · 1d



**Bob Gudgel** We were working on a product fairly recently and just had to add a tube (for looks)



Like · Reply · 1d

Sharper Image. Our business manager eventually signed a bad deal with Phillips of Germany and they got most everything, patent rights and all.

Sad · Reply · 1d

Write a reply...

Ray Ridley Sorry Tony, didn't mean to hijack your original thread. Just got carried away!

Like · Reply · 1d

Tony Salsich This is what High-end Audio does to people 😊

Like · Reply · 1d

Alex Berestov Medieval Spanish infantry charged in full silence, no matter what, even if everyone is being killed. One of the reasons they rarely loose. It looks pretty close to "stiff upper lip", which means sacrifice for a higher purpose.

Like · Reply · 1d · Edited

Ray Ridley Alex Berestov that's not the British meaning quite. But I get your point.

Like · Reply · 1d

Alex Berestov I've assumed it is a definition of stoicism.

Like · Reply · 1d

Ray Ridley Alex Berestov not complaining under duress and pain is the British way. Stiff upper lip. Doesn't hurt a bit.

Like · Reply · 1d

Ray Ridley Alex Berestov pretty much right.

Like · Reply · 1d

Write a reply...

Bruce Wilkinson My personal experience with high voltage hyperfast silicon rectifiers is that they have to be severely derated to avoid thermal runaway due to reverse recovery loss. In many instances I switched to SiC.

Like · Reply · 1d

Darrell Hambley Now this was just funny! <https://www.youtube.com/watch?v=93T0mVddBgM>

EMIAN RHAPS BOHEMIAN RHAPSODY BY QUEEN MEETS SINGING TESLA COILS!!! YOUTUBE.COM Bohemian Rhapsody by Queen Meets Singing Tesla Coils

Wow · Reply · 1d

Bob Gudgel THAT'S what we need to do with our non-varnished magnetics when they sing ! Store some songs in the micro and play some tunes with our PWM !

Like · Reply · 1d

Write a reply...

George William Tyler You trying to get faster forward recovery by selecting for reverse recovery? There is an inverse relationship, if any?

Like · Reply · 23h





- in Si ( and doped Si, e.g. Au and Pt doped ) diodes ...

Like · Reply · 22h · Edited



**Bob Gudgel** The "lower" meaning, faster the  $T_{rr}$  ?? i.e. Worse in one is better in the other ?

Like · Reply · 22h



**Tony Salsich** Right-ho. The recombination centers (e.g., Platinum) that speed reverse recovery also inhibit turn on time and increase forward drop.

Like · Reply · 20h · Edited



**Colin Tuck** **Bob Gudgel** yes, lower means smaller  $T_{rr}$  - the physics of each are somewhat diametrically opposed, any type of Schottky barrier ( e.g. SiC, Si-metal ) is different physics.

Like · Reply · 19h



**George William Tyler** You may be better off with a slower rectifier.

Like · Reply · 19h



**George William Tyler** there are other issues, Like, is that spike real? probe compensation issues can look just like that!

Like · Reply · 19h



Write a reply...



Write a comment...



**Ray Ridley**



Admin · April 2 at 10:57 PM

Social Distancing

# OHM CONFINEMENT WEEK 4



You, Norman Elias and 21 others 4 Comments

Like Comment

**Ray Ridley** This is a comic strip custom created for the power electronics engineer (you). We are always interested in creative/funny ideas you might have for future strips.

Like · Reply · 2d

**Ray Ridley** Our cartoonist is a young artist in our town. Please click on a "like" to show your appreciation for her work. 😊

Like · Reply · 2d

**Bill Stutz** Love her work

**HAHA**

Like · Reply · 22h

**Eliseo Badillo** Good job!!!

Like · Reply · 19h

Write a comment... 🗨️ 📷 🎬 🗑️

**Ray Ridley** Admin · April 3 at 2:55 PM

RidleyWorks-PSIM Webinar April 24 10 am Pacific Coast Time

In this webinar, we'll show how you get a full design done in RidleyWorks, and passed over to PSIM with the click of a button. We will demonstrate with live simulations the speed of PSIM doing a sweep on a transient circuit, and compare that to LTspice.

Moving to a new simulator like PSIM is always tough to do since your plate is already full. You might have wanted to try it, but just don't have the bandwidth. We are making that transition easy by generating a working circuit automatically for you.

<https://psim.powersimtech.com/webinar-introducing-the-link-from-ridleyworks-to-psim>





### Join the Webinar.

Brian Faley and 20 others 8 Comments

Like Comment

**Nicola Rosano** Do you accept request from attendees or examples are already planned?  
Like · Reply · 1d

**Ray Ridley** Depends on how tough it is. Requests are always welcome, but whether we have time to implement is another issue.  
Like · Reply · 1d

**Nicola Rosano** Ray Ridley i would go for a full LLC design. Do you think is possible?  
Like · Reply · 1d

**Ray Ridley** No. Ridley works doesn't do that. However it will set up a half bridge ready to measure the loop. Modify as needed to convert to LLC and simulate away. Loops or transients.  
Like · Reply · 1d

**Guru Bogdan** April not March 😊  
Like · Reply · 1d

**Ray Ridley** Thank you yes of course april.  
Like · Reply · 1d

**David Edwards** Will the presentation be viewing only or will it be interactive in real time? Will any special software be required to participate in real time (if available)?  
Like · Reply · 22h

**Ray Ridley** Well this is our first go into the webinar world, except for a magnetics seminar a couple of years ago. This one will not be a play along, but we want to do that with the Education Seminar coming up a bit later. We might change our minds, but there is a lot to get done in the next three weeks.  
Like · Reply · 21h

Write a reply... Write a comment...

**Bryan Horton** April 1 at 6:34 PM  
During initial layout/routing, what is your trusted method of sizing PCB power traces or planes?  
Please include rationale.  
1 20 Comments  
Like Comment



answers roll in now.....

Wow · Reply · 3d



**Bryan Horton** Ray Ridley exactly

Like · Reply · 3d



**George T. Ottinger** What looks good to my eye, which is usually as large as possible.

Similar to Supreme Court Justice Potter Stewart's famous quote in 1964 about porn - that he could not use words to describe pornography but "I know it when I see it", I can't tell you how large to make traces/planes, but I know what is right when I see it on the layout. 😊

Like · Reply · 3d · Edited



**David Edwards** 🗨️ Determine your acceptable temperature rise and trace current. Then determine whether the trace will be on an outer layer or inner layer. Then use the IPC-2221 curves to calculate trace cross sectional area based on what ounce thickness copper you will be using. MIL standards also have curves for this.

[https://www.ultracad.com/using\\_ipc\\_temp\\_charts.pdf](https://www.ultracad.com/using_ipc_temp_charts.pdf)

Like · Reply · 3d · Edited



**Bryan Horton** David Edwards IPC has a newer doc on this subject. Can you point us to the MIL-STD doc?

Like · Reply · 3d



**David Edwards** 🗨️ MIL-STD-275. It's probably obsolete and may have been replaced by the latest IPC document (IPC-2152). I haven't looked at the MIL standards in over a couple of decades.

Like · Reply · 3d · Edited



**Yuri de Klerk** PCBTemp.exe

Like · Reply · 3d



**LA Serantes** 🙌 Check Saturn pcb design tool, give you a good value 😊

Like · Reply · 3d



**Roswell Bob LaFrank** If you have a power supply efficiency specification the pcb losses can become significantly important. Big fat tracks on pcb have become more available over the past 20 years or so.

Like · Reply · 3d



**Andrew Ferencz** Experience. It isn't easy if you are doing a very high current board - do you go with thicker copper, more layer, what is the impact on trace/space, cost, etc. Obviously it comes down to temperature rise and/or efficiency including the vias. For planes the typical tools will not work - look, you can put 1A in a 1mil gold wire bond. The tools are great for aspect ratios that are more than a 'few to 1'. If you are lucky you have a program that can simulate the losses. I just worked with a company that could take the ODB++ and simulate 450A into the PCB including semiconductor conduction losses and come up with a temperature rise.

If you are talking about anything like a 5A trace ... then you just need to google it or check out the tables or run that Saturn tool.

Like · Reply · 3d · Edited



**David Edwards** 🗨️ One possibility that hasn't been mentioned yet for high current traces that must neck down to get through tight spots is to leave off the solder mask from those traces in those tight areas. The idea is to let the solder surface tension create a bulging convex meniscus channel of solder to add to the conductivity of the trace.

If this is not enough, one can add preformed bare copper wire jumpers on top of the trace (like mini busbars) to decrease the resistance of the run.

**Paul Xavier Matthews** Considering the far lower electrical conductivity of most solders compared to copper, this may be less effective than people think. There is also the fact that skin effect can push currents into less conductive regions.

Like · Reply · 3d

**Brian Faley** If one must be constrained by the board layers alone, adding heatsinking to the traces to reduce the temperature can increase the current handling capacity substantially. Coupling the traces on the board to a heatsink with a good thermally conductive material can more than double the current handling capacity. FR-4 is a lousy thermal conductor. About 0.5W/mK for FR-4 vs 380W/mK for copper. A good gap filler is 6-10W/mK. One of the popular IMS materials touts the fact that their aluminum substrate with 2oz copper is equivalent to 4oz copper on FR-4. Thermal vias can also be used to couple heat from hot traces to improve current carrying capacity.

Like · Reply · 3d

**Ray Ridley** Here is the reason this is a complex question to answer. What is the current density allowed in a wire or trace? You really can't answer the question without knowing how long it is. If you ever have looked inside a FET package, the bond wires are really tiny. but they are short, so it is not a problem thermally or from an efficiency standpoint.  
  
Same applies to the board. And the same to any magnetics components. Assigning a current density is really meaningless and many books and designers fall into this trap.  
  
Hence common sense overrides regulations in most applications.

Like · Reply · 3d

**Bryan Horton** **Ray Ridley** I completely agree. Even slightly complicated layouts or stackups make the standards mostly nonapplicable. What is really needed is thermal analysis, but that's a chicken and egg problem. I'm sure we've all had fun trying to justify iterative design flows to management

Like · Reply · 2d

**Brian Faley** Another good reason for a thermal camera... and thermocouples. It is usually faster to try it and see, than to waste a lot of time on calculations which yield little useful information. One more reason real experience is invaluable.

Like · Reply · 2d

**Bryan Horton** **Brian Faley** Respins are painful, field failures can be fatal. That leads to a follow up question to the original. How do you folks validate your design methodology, ie find flaws before they become real problems? (Aside from burn-in, and qual)

Like · Reply · 2d

**Brian Faley** Until you've faced and dealt with an NTSB recall... Painful. I wish I had learned really early in my career that testing was everything. Until you have proven that your very cool, very innovative, game changing circuit is perfect: it isn't. Test, test, test.

Like · Reply · 2d

**Col Johns** We generally design for <= 0.5 watt per square inch of pcb due to track losses - but as Ray says there are no hard and fast rules - if you have the space it is generally a good idea to lower trace loss where you can. Keeping send and return tight is usually of more concern in a power electronics layout.

Like · Reply · 2d

**Bill Stutz** Has anyone looked at the recent signal integrity and power Integrity software that's available

Like · Reply · 21h

Write a comment... [emojis]



**Sumukh Surya** shared his first post.

New Member · April 3 at 3:19 PM

Hi all,

I am trying to build a boost converter in CCM with design specification mentioned below. Please let me know how to get the ESR value for the inductor? Also please let me know the website for getting ESR values for inductors

I have followed this approach to design the inductor value with ESR

1. Calculation of Inductor assuming ideal conditions
2. Check the nearest value in the datasheet and note down it's ESR
2. Recalculate duty cycle with the new ESR value

L in ideal case =176uH but the standard value is 180uH and it's ESR is 0.738 ohms. I calculated D based on ESR of L. But D was a complex number. Could you please let me know if the parasitic values have to be changed? The ratio of output voltage to input voltage was taken from a standard text book (Erickson)

Specifications of the converter

Input voltage =174V

Output voltage= 300V

Output current=80A

Voltage ripple = 5%

Current ripple = 15%

Vd=0.5V

rd=0.16ohms

rds=0.54ohms

rl=0.785 ohms for 180uH

Regards,

Sumukh



3

17 Comments



Like



Comment



**Colin Tuck** your input current appears to be ~ 160 amps, a good idea to think about spitting into several parallel sections ...

Like · Reply · 1d



**Sumukh Surya** Thank you. But right now I am in the simulation stage. Could you please answer my question on ESR of L?

Like · Reply · 1d



**Col Johns** you calculate the max ESR based on the amount of watts you want to dissipate in the winding - e.g.  $160^2 \times 10$  milliohms = 256 watts, 30% higher at 100 deg C ...

Like · Reply · 1d



**Bryce Hesterman** **Sumukh Surya** The ESR is frequency dependent, and you don't want to use it to calculate D. Use the dc resistance to calculate D.

Like · Reply · 1d



me in detail? Output voltage contains a term called  $r$  which is the ESR value. Since the L actual has ESR  $\neq 0$  and is different from L in datasheet, D will change

Like · Reply · 1d



**Sumukh Surya** Bryce Hesterman please let me know the link wherein the DC resistance value can be obtained

Like · Reply · 1d



**Ray Ridley** I would be curious to know why the value of 176 uH is so ideal? A current ripple of 15 % is way too large an inductor for my liking.

If you want to design fast and accurately, and know the resistance, dc and ac, try our design software. It will get you there in minutes. The methods you are using are not going to work well at all.

Like · Reply · 1d



**Phil Lane** Inductor DCR/ESR is ignorable for a baseline D calculation. I guess you could reduce  $V_{in}$  a bit to account for it. Here's very helpful online calculator: [http://schmidt-walter-schaltnetzteile.de/.../aww\\_smps\\_e.html](http://schmidt-walter-schaltnetzteile.de/.../aww_smps_e.html)

SCHMIDT-WALTER-SCHALTNETZTEILE.DE

Boost Converter

Like · Reply · 1d

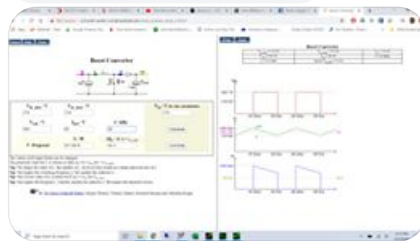


**Phil Lane** Input current is a "bit" high, not sure how you'd handle it. MOSFET as big as toaster? Will stay tuned...

Like · Reply · 1d



**Phil Lane** Something like this?



Like · Reply · 1d



**Kishor Gaikwad** I think you should follow the following process if you are designing the magnetics:

1. Assume copper loss and calculate the critical inductor value with equation for Ideal converter [steady state operation] and then select the value which will ensure that it operates in CCM
2. After selecting the wire AWG and number of turns, calculate the resistance with updated values of  $A_c$  and  $n$ . This will give you exact copper loss in the inductor
3. Check for temperature rise in the L component with this much loss. If the rise is within limits you can go ahead.

If you are thinking to buy ready made component then its choice about the how much losses you want in the inductor.

Like · Reply · 1d · Edited



**Ray Ridley** Kishor Gaikwad please tell us the equation for the ideal converter inductor design.

Like · Reply · 1d



**Kishor Gaikwad** Ray Ridley Apologies for the bad wording

Like · Reply · 1d

amps in ...

and the fet, Rds-on = 0.54 ohms, but as its a SIM, just put 10 in //, 7 watts cond loss in each for D = 0.5, now for 10 chokes to feed each fet too, but at a lot less than 785m-ohm each ...

I do like the smell of an overcooked simulated 24kW booster in the morning ( apologies to Apocalypse Now )

Like · Reply · 1d · Edited



Kevin Azul



Like · Reply · 1d



Clive Harvey 🗨️ Speaking as someone that had nowhere near the experience of those replying.

Might I suggest 24kW isn't the best power level to start at?

I'd suggest getting used to a design at less than 100W, use this too learn and then build up in steps.

Each jump in power will present different challenges and a new learning curve.

24kW worth of power, is enough to go very wrong very badly.

Also, how do you intend to source this power?

That's beyond most domestic supplies? I'm assuming this is a rectified mains your sourcing from?

This sounds like a electrical fire in the making right now.

Like · Reply · 1d



Colin Tuck He is doing it all on sim - so no appreciation of real world issues needed or required.

Like · Reply · 22h



Write a reply...



Write a comment...



Bruce Wilkinson

April 3 at 7:15 PM

I'm retired and don't have any questions for the experts but I would like from time to time post a little formula or share a spreadsheet function. I have one that solves the cubic equation by formula. For this post I will give the formula for calculating the number of turns of wire of a given diameter that will fit in a single layer in a toroid.

ID = Inside diameter of the toroid

WD = Diameter of the wire

$$N = \text{INT}(\text{PI} / \text{ASIN}(\text{WD} / (\text{ID} - \text{WD})))$$

For the next layer in ID becomes ID-2\*WD and so forth.

The formula is based on the arc sine being expressed in radians, if it is in degrees change PI to 180.



8

3 Comments



Like



Comment



Col Johns radians ... also { Pi . ID\_mm / N = wire dia\_mm }

[Pi = 3.141 etc ]

Like · Reply · 1d · Edited



and core use the same units for diameter. The formula you give works if the wire diameter is very small compared to the core ID. The formula I presented works for wire diameters up to one half the core ID.

Like · Reply · 1d

**Colin Tuck** at 2 turns it reduces to  $ID / N = \text{wire dia}$  (less tol for fit)

the single layer toroidal winding has many advantages, not least of which is a reduction in  $R_{ac}$  compared to multi-layer windings on an EI ( ETD etc ) type core, and the lack of leakage flux - excepting the flux from the one large turn equivalent.

Like · Reply · 22h

Write a reply...

Write a comment...

**Ray Ridley** created a poll. Admin · April 3 at 8:16 AM

Webinar time of day

Looks like Friday is the clear winner by a mile. I am thinking 8 am West coast. Too early for the LA dudes to be up?

That way it is just before lunch on the east coast, and Europe is still at work. (Well, maybe. but it can be enjoyed with your favorite adult beverage too. )

- 8 am Pacific Coast +32
- 10 am Pacific Coast +21
- 1 pm Pacific Coast +7
- 9 am Pacific Coast
- + Add option

7 7 Comments

Like Comment

**Ray Ridley** Man, west coast people have trouble getting up in the morning. Unless, of course, it's to go surfing. You can't do that now, though.....

Like · Reply · 2d

**Albert Dunford** I suppose webinar beers are out if it is first thing?

Like · Reply · 2d

**Ray Ridley** Why would you assume that? I won't tell.....

Like · Reply · 2d

**Norman Elias** Pick your parody: 1) Beer or no beer? 2) Let's go surfing now. Everybody's learning how,


Like · Reply · 2d · Edited

**Broox Le** Well, my preference might be 10 for timing margins, but I'd still make the extra efforts for an 8a Ridley webinar! Be sure to record it though since such things can live on as a great library of knowledge & practical application wisdom long after we're gone.

Like · Reply · 2d 1

**Broox Le** Also, sometimes Facebook announcements don't show up until \_after\_ the live event.

Like · Reply · 2d · Edited

 **Venkat Karthik** How about this 8 AM pacific. 8 AM pacific- 10 AM Central- 11 AM EST- 5 PM CEST Europe- 8 PM India - 11 PM (China, Singapore, Taiwan)

Like · Reply · 1d

Write a comment...

 **Ray Ridley** Admin · April 2 at 11:56 AM

**Expanding PWM Converter Control Horizons**

In about 5 weeks from now, we will be starting a 3-part webinar series from my professional education seminar. This is not the same version you might have downloaded from the APEC website, it is much enhanced and updated from the time of submission.

In this seminar, we deal with the topic of controlling elements outside of the converter itself. Every text you find deals with the converter transfer functions, but very few designers or teachers go beyond that in their analysis.

Things get much more complex and interesting when you use the PWM signal to control input and output filters. This is a hugely important topic as we move towards higher and higher efficiency converters in many different applications. Traditional damping of filters cannot be used without excessive loss and oversized components.

The seminar is open to everyone, and we are announcing this first to our loyal group members here to give you a chance to reserve a space first.

Send an email to [info@ridleyengineering.com](mailto:info@ridleyengineering.com) if you would like to be on the priority list for this. In a few days, we will be expanding our invitations beyond this group.

**Expanding PWM Converter Control Horizons**



**APEC 2020 Seminar**

**New Orleans, Louisiana**


**Dr. Ray Ridley**

**[www.ridleyengineering.com](http://www.ridleyengineering.com)**



 Brian Faley, Norman Elias and 48 others  11 Comments

 Like  Comment

 **Bob White** There will be a fee for this webinar series? And even though it is web based the number of participants will be limited? This is what I infer from the announcement.

Like · Reply · 3d



Webinars always have a limit, otherwise costs go up. You will see many of them filling up to capacity these days. Last time we did an IEEE webinar they had to expand capacity at the last minute due to oversubscription.

There is no inference in my posts, that is reading way too much into things. I am just giving this group first option.

[Like](#) · [Reply](#) · 3d



**Ray Ridley** 🗳️ On the webinar, we will be doing things we couldn't do in the APEC environment. Live simulations and probably measurements too. Using your own computer was always a no-no with the AV staff at the conference, so we didn't try that in a large room.

Those of you that have RidleyWorks will be able to follow along on your own computers.

[Like](#) · [Reply](#) · 3d



**Ray Ridley** 🗳️ Ok, signups are already coming in - don't delay if you want to be included.

[Like](#) · [Reply](#) · 3d



**Ray Ridley** 🗳️ what is the best day of the week for everybody?

[Like](#) · [Reply](#) · 2d



**Ray Ridley** 🗳️ If everyone in the group buys our software, I will do nothing but webinar presentations for you all for a whole year 🤖

That would be the dream.....

[Like](#) · [Reply](#) · 2d · Edited



**Norman Elias** Will the free Buck version suffice?

[Like](#) · [Reply](#) · 2d



**Norman Elias** I vote for either M-W or Tu-Th but I'm flexible.

[Like](#) · [Reply](#) · 2d



**Ray Ridley** 🗳️ go vote in the poll. you can choose more than one.

[Like](#) · [Reply](#) · 2d



**Col Johns** Many years ago it was mooted to put large RC dampeners across the blocking cap or caps in a Cuk converter - to avoid unsightly LF oscillations in volt mode control. I never did this, hypothesising that if the freq was high enough ( away from the resonances in the system ) then there was simply no need - this proved to be the case - although in depth feedback design needed.

I very much like the idea of a webinar educating about issues of very high Q ( low loss ) filters and their effect on converter design as we seek efficiencies above 98% ...

[Like](#) · [Reply](#) · 2d · Edited



**Ray Ridley** 🗳️ We first ran into this trying to design a current-source converter that needed some serious filtering.

That would be the case for many applications, including solar cell processing converters.

Even dc-dc converters end up as a current source at higher frequencies.

[Like](#) · [Reply](#) · 2d



**Sanchit Mishra**

Write a comment...  
April 2 at 11:31 PM

Query about "reverse polarity protection diode" (diode is marked as a red oval in the image attached).

I was reading this reference design from TI which contains a aerospace design. The first stage is PFC (boost converter) AC/DC (**shown in this**



**Some specs:**

Input = 96VAC, 400Hz, rectified passively. This makes PFC input.

PFC output = 240VDC (stored at PFC bulk capacitors).

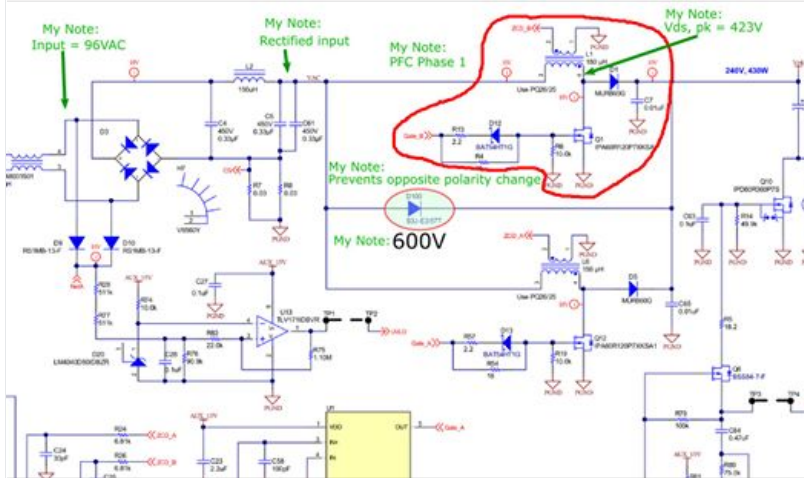
LLC stage = converts output to 30VDC

**Query:**

\*What is the diode that bypasses PFC stage doing ? \*

- 
- 1) \*I thought it for charging of PFC bulk capacitor during AC connection (i.e. startup). But, the the PFC Inductor + PFC diode does the same job.
- 2) Is the diode for "reverse polarity protection" or start up charging or somethign entirely different ?

Diode PN: S3J-E3/57T, Diode Standard 600V 3A Surface Mount DO-214AB (SMC)



You and 8 others

32 Comments



Like



Comment



**Casper Hjort Wilson** It's for precharging the bulk capacitors. It's often a diode with high I2t rating (low freq, standard diode).

Like · Reply · 2d



**Sanchit Mishra** The PFC boost with FET held OFF can pre-charge the bulk capacitor. Is that not correct ?

Like · Reply · 2d



**Col Johns** A step voltage into an unloaded LC ckt can ring up to twice the step input volts ( 2 x 325V ) it is there to stop damage to the electro ....

Like · Reply · 2d · Edited



**Casper Hjort Wilson** Sanchit Mishra You are most likely saturating the inductor and stressing the PFC diode. Therefore you insert an extra "heavy" I2t diode to take the hit. And also as Col Johns said 👍😊

Like · Reply · 2d



Write a reply...



**John DeFiore** Exactly, the inrush current can saturate the PFC inductor without the diode, and if you turn on the FET into a saturated inductor you can get smoke.

Like · Reply · 2d

already connected to an "inrush limiter" and a FET (titled 'Q10' located in the right hand side of the figure) in series with the bulk capacitor for limiting the inrush current.  
Thanks for pointing out the saturation of the boost inductor. This large SMC package of this extra diode will provide significant metal for power loss/temp rise during start up inrush current draw.

Like · Reply · 2d · Edited

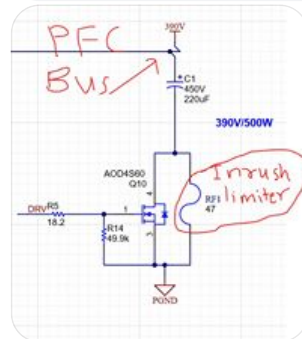


**Col Johns** Can you show us " the fet in series with the bulk cap " please ? I have got to see that one ...

Like · Reply · 2d



**Sanchit Mishra** Col Johns This figure is from an extremely similar design (the only different is that this is non aerospace and some schematic BoM changes)



Like · Reply · 2d



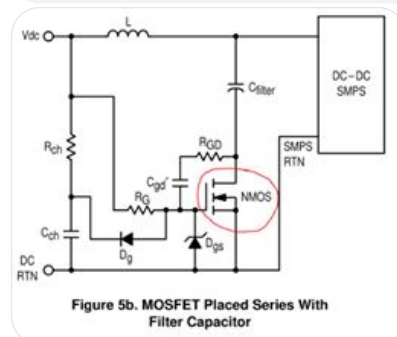
**Col Johns** Sanchit Mishra - why does that look like a bad idea ...?

Like · Reply · 2d



**Sanchit Mishra** Col Johns Only since your comment I'd been googling it as I did not think it was an inherently bad idea. I found this document which discusses it being used by Motorola before [App note - Motorola AN1542].

Link = <http://www.mosaic-industries.com/.../motorola-an1542...>



Like · Reply · 2d · Edited

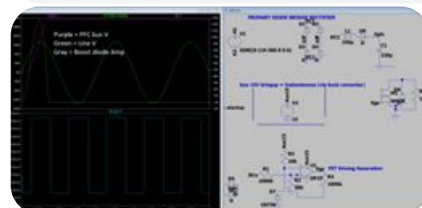


**Sanchit Mishra** Col Johns, I made a simple Ltspice simulation with and without the FET based inrush limiter.

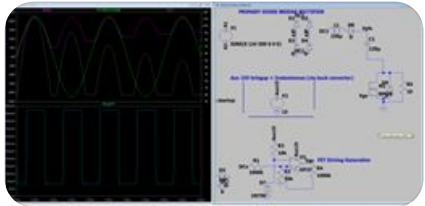
Without the inrush limiter, the peak current through boost diode is 130A.

With inrush limiter (FET driven from analog control and 10 ohms resistance connected in parallel in LTspice) the peak current is 11A.

Here is figure without inrush limiter :



**Sanchit Mishra** Col Johns here is figure with inrush limiter.



Like · Reply · 2d

**Sanchit Mishra** And, this is the actual hardware result from TI for inrush limiting as AC is turned ON --

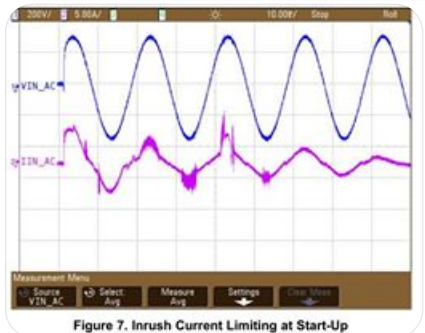


Figure 7. Inrush Current Limiting at Start-Up

Like · Reply · 2d

Write a reply...

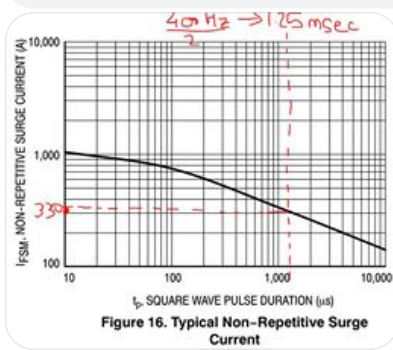
**Col Johns** The  $Z_o = \text{SQRT}(150\mu\text{H} / 220\mu\text{F}) = 0.825 \text{ ohm}$ , for 240Vac + 10%, Vpk at switch on can be 373 volts = 452A pk in the diode and L ( assuming the L is linear to this current - it won't be ) - what is the peak I rated in the diode for an half cycle ...?

With 47E (cold) inrush limiter Ipk = 8A, and no inrush diode needed - but what happens if someone switches the unit off and on again when the ntc inrush limiter is hot ...?

Like · Reply · 2d · Edited

Hide 12 Replies

**Sanchit Mishra** Let me know if this is not the right way -- Since this is aerospace, 400Hz is the operating frequency. I used the "surge current" graph from the datasheet.



Like · Reply · 2d

**Sanchit Mishra** Also, I'd like to add that the operating voltage for this reference design was like this -- 96VAC to 134VAC, 400Hz - 800Hz.

Like · Reply · 2d

**Col Johns** about 150 amps for 10mS ...

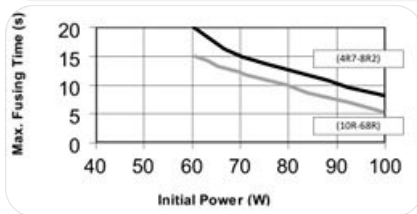
Like · Reply · 2d

**Col Johns** What is the "hot" resistance for the 47E ntc?

Like · Reply · 2d



It's resistance range is 4.7Ohm to 67Ohm. After fusing resistance is 100x nominal value. "



Like · Reply · 2d



**Col Johns** Sanchit Mishra - but you are using it as an inrush limiter ...?  $189Vpk / 4E7 = 40Apk$  ...

Like · Reply · 2d · Edited



**Col Johns** At 40A it takes 1mS to charge 220uF to 189V...

Like · Reply · 2d

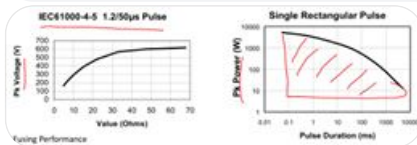


**Col Johns** Depending on the physical size of the fusible R it will die at some stage after several on/off cycles ...

Like · Reply · 2d



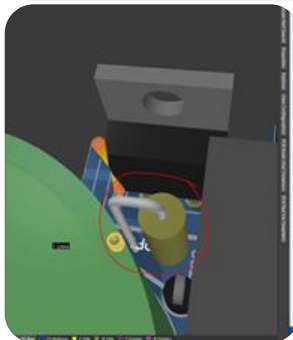
**Sanchit Mishra** Col Johns From the 3D model the size is big (close to the size of TO-220). Once the resistor fuses, its permanent. Did you mean to say from a life-time perspective that eventually this resistor will go bad permanently after a fixed number of ON/OFF cycles ? In the datasheet, I could only find this relevant figure which discusses maximum power and voltage (when tested with the IEC pulse) allowed across this resistor.



Like · Reply · 2d



**Sanchit Mishra** Size from the 3D model of the PCB -



Like · Reply · 2d



**Col Johns** Well - it is one of those things - will the unit be turned on and off a lot ... ?

Like · Reply · 2d · Edited



**Casper Hjort Wilson** Col Johns Yes, the thermal "memory effect" shall not be forgotten when using NTCs 😊

Like · Reply · 2d



Write a reply...



diode can take as I2T of fast diode is lower than standard. When the cap is charged, there will be high energy stored in the inductor and, depending on values the voltage will rise to possibly dangerous values, although this is normally less likely.

Like · Reply · 2d

**Colin Tuck** totally depends on series R, also the PFC choke, upon saturation, lessens the effect of resonant ring up ...

Like · Reply · 2d

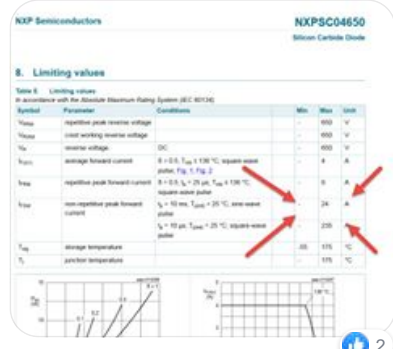
**李小道** The diode is necessary for much bigger inrush charging current. Basically, high speed diode is good for high efficiency but bad for inrush current.

Like · Reply · 2d

**Sanchit Mishra** This is what I learnt today, thank you for your response. I always thought the inrush current (even if it saturates the PFC inductor) is such a small scale event that we don't need to take special precautions besides targeting AC fuse.

Like · Reply · 2d

**Andrew Ferencz** Most people these days use SiC for the PFC diode. They have a specified maximum current that can be exceeding during inrush or transient spikes. Thus you need to protect it. And it is a real spec - you would think the SiC can take a hit right? Nope .. just breaks. But they are getting more rugged. 10 years ago they were much more delicate than today.



Like · Reply · 2d

**Bruce Wilkinson** That diode was first used in a PFC boost circuit by my late coworker Jack Swoboda. It was to prevent saturation of the boost inductor at turn on. As for inrush protection we never used NTC thermistors because of the thermal memory. We used a high joule value resistor and a switch. In some instances we used a PTC thermistor in place of the resistor for fault protection.

Like · Reply · 2d

**Mike Tommasi**  
Write a comment...  
April 3 at 2:06 AM

Hi all.

Am I the only one puzzled by IEC 61000-3-2 Class D harmonic limits? (I will use the 3rd harmonic here, but same applies to all odd harmonics).

IEC 61000-3-2 specifies limits only for 230 Vac.  
At 230 V the fundamental is 1/230 = 4.35 mA/W.  
The 3rd harmonic limit is 3.4 mA/W, which is **78.2%** of fundamental.

Would you agree that, logically, any test for harmonics at lower voltages should adjust harmonic limits in order to maintain the same levels w.r.t. the fundamental?

In other words, at 115 Vac the 3rd harmonic should be 6.8 mA/W, thus remaining at 78.2% of fundamental. Without adjustment, you would have stricter harmonic level requirements at lower voltages (as % of fundamental).

I have not found much about standards applicable at 115 Vac (USA), but





is calculated taking the nominal voltage of all the available public electricity supply systems as  $V_{nom}$ ."

Also, Yokogawa's Harmonic Measurement Software (User Manual, p. 1-11) supports this idea of adjustment: "IEC 61000-3-2 assumes a phase voltage of 230 V [...], for equipment of differing rated voltage [...] convert the limits of all the classes using: [...] Converted limit = Limit of each class  $\times$  230 / Rated voltage of the equipment"

Yet, I have seen papers where that 3.4 mA/W limit is used at 115 Vac, unadjusted, thus requiring it to be 39.1% of fundamental.

Any thoughts?

TIA!



1

17 Comments



Like



Comment



**Hamish Laird** IEC world is 230/240. Are their harmonic limits in the 115 world??

Like · Reply · 2d



**Mike Tommasi** don't know

Like · Reply · 2d



**Col Johns** no mandated harmonic limits in the USA yet, - I think ...

Like · Reply · 2d



**Mike Tommasi** OK, strange though. IEC 61000-3-2 is more than 20 years old.

Like · Reply · 2d



**Mike Tommasi** So given that all AC adapters are universal input and thus are designed to Japanese and European harmonics norms, the USA gets products with good harmonics thanks to non-US rules. SMART! 😊

Like · Reply · 2d



**Yuri de Klerk** Class D is for PC's , monitor's and television receivers. PC powersupplies (>300W or so) nowadays have PFC, so no problem (I guess).

For the following categories of equipment, limits are not specified in this standard:

– equipment with a rated power of 75 W or less, other than lighting equipment.

This means all PC, monitor, television which have a power >75W could be made without PFC, as long as you can comply with the 3.4mA/W as you mentioned. This is actually already some kind of bargain, because there's room to not use a PFC as long as you're doing it 'carefully'. Universal mains is probably not reachable, but single range 200-240 is.

For US there's the energy star with THD limit, but for Japan I don't know.

I never did a non-PFC for 100-120V which had to comply with 3.4mA/W, and there's a lot of non-linearity when applying a 50Hz choke, a resistor and a bulk-cap, so don't know how hard it is.

There's still the trick with 2 bulk-cap's in quasi-series and other tricks with valley-filling.

Did you already perform some simulation for a 100-120V circuit and compare it with 200-240V circuit where both comply with the 3.4mA/W requirement?

The bulk-caps will be bigger anyhow for 100-120V even without harmonic limits, but the comparison for inductors would be interesting.

Like · Reply · 2d

be bigger in capacitance, but not bigger physically. For a given power level, the energy to be stored to achieve PFC is the same at any voltage. The caps will be higher capacitance lower voltage, so same size roughly.

Like · Reply · 2d

**Mike Tommasi** As mentioned, Japan has same standard as Europe, scaled to the current levels there (X 230 / 100).

Like · Reply · 2d

**Yuri de Klerk** So Japan is ok. But which country uses the 3.4mA/W from IEC 61000-3-2 and has a mains voltage of 100-120V ?

Like · Reply · 2d · Edited

**Mike Tommasi** none; but I have seen papers that imply so, using for example 39.1 % for the 3rd harmonic (as % of fundamental) instead of 78.2%.

Like · Reply · 2d

**Yuri de Klerk** Ok. I guess if you want to make a universal mains power supply AND comply with these limits , the 39.1% is mandatory. As long as you stick with single range the problem does not exist.

Like · Reply · 2d

**Mike Tommasi** well no, that is the point. It is 78.2% at all voltages.

Like · Reply · 2d

**Yuri de Klerk** The phrase: "when the rated voltage [is] a voltage range...", I can not find it in the European standard, is it ?  
I searched the 2009 and 2018 version, but no mention of it. Is it only in the Japan version ?  
If so, it does allow us to do 78.2% at 230V , but only in Japan (which makes it useless of course).

Like · Reply · 2d · Edited

**Mike Tommasi** No, this is to comply with Japanese standard. EU standard is 230 V only

Like · Reply · 2d

**Yuri de Klerk** My last comment is not really correct.  
So  
EU = 3.4mA/W @ 230V  
JP = 3.4mA/W @ 230V and 6.8mA/W @ 115V  
US = Energy Star with PF requirement  
I couldn't find THD in the Energy Star now, but since I'm not USian I could be wrong.

Like · Reply · 2d

Write a reply...

**Phil Lane** Back in 1982 a guy (at Boeing) told me "6dB above nothing is still nothing".

Like · Reply · 2d

👍 🤔 3

**Ray Ridley** Unless nothing is zero dB

Like · Reply · 2d

👍 2

Write a comment...

**Ray Ridley** created a poll. Admin · April 2 at 1:53 PM

What is the best day of the week for you to attend a Webinar?

- Friday
- However long Dr. Ridley needs to cover the material is OK with me.
- Thursday
- Saturday  
Added by you
- Wednesday
- 5 More Options...

👍🤔 13 38 Comments

👍 Like Comment

**Nelson Garcia** 60 minutes  
Like · Reply · 2d

**Rafael Arellano** 60 minutes  
Like · Reply · 2d

**Martin Martinez** 1 hour  
Like · Reply · 2d

**Shardul Adkar** 1 hour!  
Like · Reply · 2d

**John Baillie** 45mins  
Like · Reply · 2d

**Emma Raszmann** 1 hour  
Like · Reply · 2d

**Navroop Singh** 1 hour  
Like · Reply · 2d

**Manish Niraula** 1 hour  
Like · Reply · 2d

**Bob Gudgel** As long as it takes  
Like · Reply · 2d

**Ray Ridley** 🛡️ 6 hours?  
Like · Reply · 2d

**Bob Gudgel** Great !  
Like · Reply · 2d

**Bob Gudgel** Webinars are too often rushed. I know that there may be a lot of wasted time the first half hour or so, so add that half hour to the 1 hour for a typical webinar and maybe another 1/2 hour for questions and answers. I'd say that would make it 2 hours at least.  
Like · Reply · 2d

**Tony Salsich** agreed  
Like · Reply · 2d

**Robert Muniz** If it's a valuable training resource (which Ray excels at) I see no problem with committing several hours or even a full day as I would for any training course, let alone a FREE one!

Write a reply...

**Charlie Elliott** up to 90 mins

Like · Reply · 2d

**Brian Faley** 90-120mins

Like · Reply · 2d

**Ray Ridley** Why does everyone prefer Friday so much?

Like · Reply · 2d

**Bob Gudel** Because Friday night is the time to go out and eat drink and be merry ? Oh, nevermind... Not supposed to be doing that right now.

Like · Reply · 2d · Edited

**Brian Faley** since no one is going out drinking with the lab crew on Friday, might as well be part of a webinar with fellow nerds.

Like · Reply · 2d

**Ray Ridley** It used to be Friday lunchtime at my first job. Times were different then....  
I visited Dialog Semiconductor in Germany a couple of years ago to give them a workshop. The company kept the fridge full of beer for all the hardworking engineers. Pretty awesome!

Like · Reply · 2d

**Brian Faley** My first boss would hold Friday afternoon debrief meetings at the local watering hole. He always bought the first pitcher and listened to us compare notes about the week in the lab. We called it the attitude adjustment hour, and it worked.

Like · Reply · 2d

**Jonathan Beaver** As I noted below, Friday in the US will be Saturday elsewhere in the world, which may limit some international attendance.

Like · Reply · 2d

**Ray Ridley** I hear you, but i think the masses have spoken on this.

Like · Reply · 2d

**Norman Elias** You may wish to consider those whose religious faith prohibits work on certain days. Observant Jews will not participate on a Friday afternoon as they prepare for the Sabbath and will not return to work until Sunday morning.

Like · Reply · 2d

Write a reply...

**Jimbo Hissem** 1hr

Like · Reply · 2d

**Khor San Lee** 90min

Like · Reply · 2d

**Jonathan Beaver** Anywhere 1 to 2 hours is fine. My preference would be 'anything but Friday', because Friday in the USA is Saturday in New Zealand.

Like · Reply · 2d

**Ray Ridley** always an outlier in the group.....  
Everyday is a weekend day now - does it matter?

Jonathan Beaver Ray Ridley I'd say it still matters for anyone who isn't in lockdown yet or who are still keeping to 'regular' hours during this time for whatever reason. I'm not sure what the distribution of nationalities is here in the group but I'm surprised that it would be considered 'that' much of an outlier? Friday 'day', west coast US is Friday night UK/EU, Saturday early morning through to Saturday day for the rest of the world. I wonder if some of the responses above might not just be 'Friday' but instead 'Friday in my time zone'? Edit: Lost a word somewhere along the way, apparently.

Like · Reply · 2d · Edited

Michael Delany 90min+

Like · Reply · 2d

Eliseo Badillo Max two (2) hours.

Like · Reply · 2d

Tony Salsich When you do announce the time and date, I will tell all of my colleagues.

Like · Reply · 2d

Rahulnab Das Sunday sir

Like · Reply · 2d

Shiv Kumar Mishra Sunday , 1hour

Like · Reply · 2d

Dipak Patel Friday

Like · Reply · 2d

Manfred Wimmer Beeing european, the time is more important than the day.

Like · Reply · 2d 4

Ray Ridley Manfred Wimmer I'm thinking 8 am west coast. Not going earlier than that!

Like · Reply · 2d

Write a reply...

Frank Warnes Any day for 1 to 2 hrs

Like · Reply · 2d

Write a comment...

LA Serantes New Member · April 1 at 8:31 AM

Dear al, I have a fast question:

Darrell Hambley and 3 others 18 Comments

Like Comment

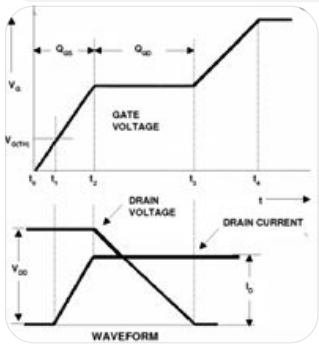
**Casper Hjort Wilson** LLC or traditional HB?  
Like · Reply · 4d

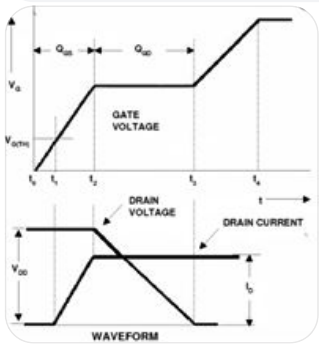
**Pranit Pawar** there's a brilliant quite paper by EPC on deadtime optimisation  
<https://www.google.com/url?sa=t&source=web&rct=j...>  
Like · Reply · 4d

**Ray Ridley** It might be a fast question - it is anything but a fast answer.  
Like · Reply · 4d

**Bob Gudgel** So true !  
Like · Reply · 2d · Edited

**Darrell Hambley** 1. Sum the maximum worst case times for:  
Tdelay of the HS gate driver + Fall time of Vg to Vg\_on + HS miller time + HS current fall time.  
2. Sum the minimum worst case time for:  
Tdelay of LS gate drive + Rise time of Vg from 0V to Vg\_on  
3. Subtract the result of #1 from #2. That should be your minimum dead time that you set between the edges which you send to the gate drivers.  
Note that most every value which I mentioned above requires a calculation for your unique circuit, except the gate driver delay times, which you can get straight from the data sheets.  
Like · Reply · 4d · Edited

**James Keith** Darrell Hambley : When you say "Fall time of Vg to Vg\_on + HS miller time" : what does this mean? Is it the time from t4 to t0 as shown in the attached picture? Lets say Vg = 12V, t0 to t4 would be 0 V to 12V or 12V down to 0V ( which includes the miller plateau).  




Like · Reply · 2d

**Darrell Hambley** For Vg\_on I meant basically the miller plateau, which could be a broad range around 4V to 6V or more.  
Like · Reply · 2d

**Charlie Elliott** Keep reducing it until it goes bang and then back off a bit 🤔🤔  
Like · Reply · 4d

**Ray Ridley** Nothing like a little bit of WCA to make your day go better, Charlie Elliott.  
Let me quote a student of the modern way at you: "can you please provide a detailed equation of how to calculate with Mathcad exactly what is the number for 'a bit'"  
I like your style though, sounds like an engineer who has been in the trenches for a while.

**Charlie Emmott** **Ray Ridley** I just couldn't resist! I am constantly amazed as to how many people think they do power electronics but don't do switch testing or basic worst case timing analysis on gate drive and switch combinations. Most of the time they get away with it but when they don't it can get expensive very quickly!

[Like](#) · [Reply](#) · 3d

**Ray Ridley** The more sophisticated digital controllers of the day actually adjust the dead time for maximum efficiency. Parameters are input and output voltage, power level, temperature, and phase of the moon.  
If you invest 50 man years or so, you can do this too!

[Like](#) · [Reply](#) · 4d

**Brian Faley** Be sure to account for the highest and lowest temperature operation as well. There is not one answer that is right all the time for optimum dead-time. Enough but not too much. Too little is worst! It's more fun when you find out you have too little at 60C ambient, 120% load, 90%RH in a military testing facility!

[Like](#) · [Reply](#) · 4d

**Ray Ridley** Add some transient and surge testing on top of that just for good measure.  
Dealing with the bridge is actually the easy part. Secondary sync rectifiers are much more challenging.

[Like](#) · [Reply](#) · 4d

**Venkat Karthik** What are you using IGBT's, MOSFET's, SiC, GAN? What is your switching frequency and DC bus voltage?

[Like](#) · [Reply](#) · 3d · Edited

**Col Johns** As a very rough guide line:  
At 20kHz, 500nS (not uS) or more if using slow IGBT's  
50kHz, 200nS assuming using fast fets, or ultra-fast IGBT's  
100kHz, 100nS  
200kHz, 50nS, can use more if resonant ZVS  
do we need to go higher?

[Like](#) · [Reply](#) · 3d · Edited 1

**Ray Ridley** I think you mean 500 ns for 20 kHz.

[Like](#) · [Reply](#) · 2d

**Ray Ridley** New EPC boards expect to run at up to 5 MHz.  
Looks like you want to say 1% of Fs as a generic answer.

[Like](#) · [Reply](#) · 2d

**Col Johns** **Ray Ridley** - yes - 500nS will correct ... and yes - about 1% of the total period approx ...

[Like](#) · [Reply](#) · 2d · Edited

Write a reply...

Write a comment...

Hi every body,  
I'm looking for a common mode filtre for a flyback smps with out using the ground.  
Cordially

3 45 Comments

Like

Comment

**Alex Berestov** Well, where you think one could redirect the CM current without GND connection. However you still may increase CM impedance. There was a discussion here a while ago.

Like · Reply · 3d

**Hicham Boutouche** Alex Berestov how can we increase the cm impedance

Like · Reply · 3d

**Bob Gudgel** One way to make a CM filter without a ground connection is to just run all output wires and all input wires through a proper ferrite. Capacitors will need to be connected to ground for CM AFAIK

Like · Reply · 3d · Edited

**Hicham Boutouche** Bob Gudgel how the the ferrite is designed

Like · Reply · 3d

**Bob Gudgel** Depends on the frequency or frequencies of interest usually. Go to a company like Fair-Rite or Laird and see some of their application notes. In one of my new designs, I use two different materials... One for low frequency and one for high frequency. You will want one with a high insertion loss for the frequency band of interest. Not just permeability or AL or inductance etc.

Like · Reply · 3d

**Hicham Boutouche** Bob Gudgel thanks

Like · Reply · 3d

Write a reply...

**Col Johns** You are limited to CM chokes, usually one for LF and one for HF - if no gnd connection available ...

Like · Reply · 3d

**Hicham Boutouche** Col Johns if I understood I must use two bobined

Like · Reply · 3d

**David Edwards** 🙄 It is usually a bad idea to face the line with Y-capacitors as the last stage of a common mode EMI filter. This is because the local ground always has some noise on it and the Y-caps will inject this straight into the line. Some form of T filter is good with a high frequency common mode choke facing the line.

Like · Reply · 3d · Edited

**Hicham Boutouche** David Edwards you some documents about the t filter for cm noise

Like · Reply · 3d





caps, which contradicts actual analysis and testing. We've all seen this caps-last mistake on many commercial supplies and wall warts, the smoking gun being that huge bead we see on many input AC cords, which is a band aid added after they found that they're out of spec after visiting an EMI test lab.

Like · Reply · 3d



**Bob Gudge** Darrell Yes, absolutely ! I like to try at least to make these CM filters symmetrical if possible so that they can also help for EMC / EMI susceptibility... T-Filter L-C-L That's my feeling on it anyway

Like · Reply · 3d



Write a reply...



**Doddapaneni Venkata Nagesh Babu** If the application is similar to medical field for lower ground leakage, still small amount of Y cap to be considered. Otherwise common mode choke will be large but still may not EMI compliant. Other option is to use a step down transformer and low voltage DC DC converter. This approach is feasible for smaller power converter.

Like · Reply · 3d · Edited



**Hicham Boutouche** Doddapaneni Venkata Nagesh Babu yes it's for medical devices

Like · Reply · 3d



**Hicham Boutouche** I would like to know if there another solution, because in my case I'm using a flyback transformer

Like · Reply · 3d



**Doddapaneni Venkata Nagesh Babu** **Hicham Boutouche** if power is less than 50 watts , usually 50hz or 60hz step down transformer and then DC DC stage recommended. Usually this transformer offers good amount of EMI immunity when add x caps on line. If larger power , it's a struggle . 100uA leakage current to be budgeted into various line y caps and other blocks . I used to add 100pf Y caps double insulated type. No caps vs very small caps actually helps to reduce CM choke. Also recommend to check if equipment is patient vicinity dependant or remote. As I understand , remotely used equipment doesn't need such low leakage.

Like · Reply · 2d



Write a reply...



**David Edwards** 🇺🇸 . Hello <https://www.facebook.com/hicham.boutouch>

Are you using a single ended flyback topology driven by a single low side MOSFET? If so, be aware that this topology can generate extremely fast dv/dts at the end of the switch transition. This can lead to excess EMI at ten to hundreds of megahertz. Snubbers help, but the best solution may be active dv/dt limiting.



Hicham Boutouche

Like · Reply · 3d

^ Hide 23 Replies

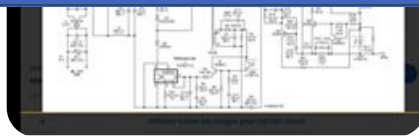


**Hicham Boutouche** **David Edwards** thank very much I will share with you my circuit to see its what you are talking about

Like · Reply · 3d



**Hicham Boutouche**



Like · Reply · 3d



**David Edwards** 🇺🇸 You are using a TOPSwitch with an integrated MOSFET so its gate is inaccessible, leaving no possibility for active  $dv/dt$  limiting. However, you can still add an RC damper right across the TOPSwitch MOSFET drain and source. The capacitor should be equal to the value of the MOSFET  $C_{oss}$  ( $=C_{ds}+C_{gd}$ ) at 30V to 50V and the resistor should be selected to limit turn on current to within the Top Switch's peak current rating. I am guessing the capacitor value should be about 33pF at 800V and the resistor value should be about 200 ohms with an  $f^*C*V^2$  power rating.

These should be surface mount parts placed as close as possible to the TOPSwitch. The idea is to keep the current flowing as close as possible to the same path when the switch turns off. This makes the loop subjected to fast  $di/dt$  as small as possible.

EDIT: Upon further thought, my advice was incomplete. A series RC damper will not be as effective at limiting initial  $dv/dt$  as an RCD snubber, but it will limit ending  $dv/dt$ , where the current is less and the unlimited  $dv/dt$  is greatest. However, it can be very effective at damping out ringing. I will post a schematic at the bottom of this thread.

Like · Reply · 3d · Edited



**Hicham Boutouche** David Edwards thank you very much, can you please share with me a document who explains more what you have talked about it

Like · Reply · 3d

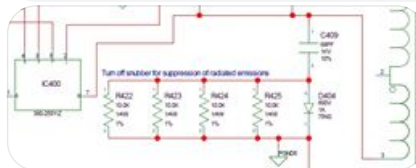


**Hicham Boutouche** I understood what you said me but how do you calculate the value of the resistor

Like · Reply · 3d



**Lynn Schultz** Had a radiated emissions problem using a TOPSWITCH in a 100W flyback design. Had to meet FCC Class B emissions. Added an RCD snubber drain to ground of the TOPSWITCH to slow  $dV/dt$  at turn off to successfully reduce radiated emissions.



Like · Reply · 3d



**Hicham Boutouche** And why the capacitor must has the value of  $c_{gs} + c_{gd}$

Like · Reply · 3d



**Hicham Boutouche** Lynn Schultz thank you very much can you please share with me how do you calculate the value of this circuit snubber

Like · Reply · 3d



**Lynn Schultz** Hicham Boutouche Selection of components is of course circuit related. Transformer capacitance, drain capacitance of the TOPSWITCH, and peak turn off current driven by the transformer leakage inductance determine the  $dV/dt$  at turn off. The cap is chosen to reduce the  $dV/dt$  to reduce emissions. The resistors across the diode in the RCD snubber should be chosen to permit discharge of the snubber cap during the shortest expected on-time of the TOPSWITCH.



Hicham Boutouche Lynn Schultz thanks but I'm talking about the rcd between the drain and the ground

Like · Reply · 3d



Lynn Schultz Hicham Boutouche So was I....

Like · Reply · 3d



Hicham Boutouche So what about the rcd between the drain and the 310 vdc

Like · Reply · 3d



Ray Ridley Here you go for snubber calculations. You have to use a combination of calculation and measurement to get the optimal values.



Like · Reply · 3d



Hicham Boutouche Ray Ridley I read it but between the drain and the ground we use rc snubber or we can also use rcd snubber

Like · Reply · 3d



Ray Ridley what is your question? for low noise you would use both.

Like · Reply · 3d



Ray Ridley Hicham Boutouche did you already have that paper? where did you get it from?

Like · Reply · 3d



Ray Ridley seems to have gone missing from our design center.....

Like · Reply · 3d



Hicham Boutouche My question is what can we use between the drain and the ground : RC snubber or Rcd snubber

Like · Reply · 3d



Hicham Boutouche Ray Ridley I get from you

Like · Reply · 3d



Ray Ridley drain to ground is the RC snubber. RCD goes drain to high side of the input line.

Like · Reply · 3d



Hicham Boutouche Ray Ridley thank you very much

Like · Reply · 3d



Hicham Boutouche I read also an article which talk about rcd-r snubber. have you an idea about it?

Like · Reply · 3d



Lynn Schultz Ray Ridley The RCD snubber I had posted connects drain to ground across the switch. The cap is directly across the drain during turn off with no series R. Effective at controlling dV/dt at turn off. This is not an RCD clamp - I may have confused the conversation when I called my example and RCD snubber.

Write a reply...

**Ray Ridley** I just uploaded the file.

Like · Reply · 3d

**Col Johns** Hicham Boutouche, you don't really need the diode D4 in the schematic. PI actually slowed the turn on of the mosfet in this part to address excessive dv/dt at turn on - which causes a lot of RFI from the o/p diode too. CM radiation can only really be addressed in a finished design with snubbers - as said above, across the Tx pri and on the diode sec.

Like · Reply · 2d

**David Edwards** It is best to put the alternate current path (snubbers) directly across (in a tight loop) the switch (MOSFET or diode) that is opening. Current doesn't like changing paths without a lot of voltage (spikes and ringing) to make it do so.

Like · Reply · 2d · Edited

**Colin Tuck** David Edwards, except that the mosfet sees a lot more peak volts than the Tx - so there is a dissipation issue at freq - I note the Top-Switch has a grounded tab - so that helps for RFI emissions straight away ...  
I note that when the pri switch turns on ( possibly too fast ) the o/p diode is hit with significant dv/dt - so a snubber there seems indicated as well.

Like · Reply · 2d · Edited

**David Edwards** The diode snubber should go across the diode.

Like · Reply · 2d

Write a reply...

Write a comment...

**Frank Warnes** April 2 at 4:41 AM

I have a quick question about the simulator Simetrix to those that are using it. Why does it take so long to start? I usually have to wait at least 10 minutes before I can do anything with it. At the moment I am using the demo version and I did wonder if it was deliberate to encourage you to buy the real version. Another theory is that I have built up a larger library of models so is it just taking a long time to read them all. Anyone any idea?

1 Like 14 Comments

Like Comment

**Greg W Aseige** No idea, it usually very fast you look to have a problem somewhere.

Like · Reply · 3d

**Alain Laprade** Very fast for me. Running a server based license. I did a quick search on the web and didn't find complaints/answers on the topic.

Like · Reply · 3d

**Frank Warnes** Alain Laprade do you keep your model's library on the server?

Like · Reply · 3d

Like · Reply · 3d · Edited


**Paul Lee** Less than ten seconds for me - I'm using the demo version as well  
Like · Reply · 3d

**Paul Lee** Just seen there is an update patch available. Maybe that will help.  
Like · Reply · 3d

**Jesper Birch Carlsen** Model library on server here and it loads inside few Seconds.  
Like · Reply · 3d


**Venkat Karthik** laptop issue? may be too old? It takes less than a min for me.  
Like · Reply · 3d

**Frank Warnes** Ok thanks sounds like something's wrong with my setup  
Like · Reply · 3d





**Kevin Azul**  
  
Like · Reply · 3d

**李小道** Less than 10s for me as well.  
Like · Reply · 3d

**Hamish Laird** Licensing - maybe  
Like · Reply · 2d

**Lev Nemets** antivirus sometime can do this  
Like · Reply · 2d  1





**Jeremy Lister** Been using it for 5 years. Always loads fast.  
Like · Reply · 2d

Write a comment...    

**Farhad Bagheroskouei** April 3 at 12:30 AM

This content isn't available right now  
When this happens, it's usually because the owner only shared it with a small group of people, changed who can see it or it's been deleted.

 Like  Comment

Write a comment...    

**Janamejaya Rox** April 2 at 10:38 PM

**IEEE Webinar Series**  
Dear all,  
I hope you are doing well and are safe.

If you are willing to share your expertise on a specific topic for a duration of 45 - 60 Minutes, please do let me know. Thank you. bcjanmay.edu@gmail.com is my email id.

9

Like

Comment

Write a comment...



Ray Ridley

Admin · March 31 at 2:05 PM

### AP310 vs R&S Output Impedance Measurement

Some time ago, we published some curves here about the performance against "other" analyzers. At the time we were so overwhelmed with testing data versus many, many units, we didn't say which was which.

The fastidious engineers in this group, quite rightly, weren't happy with that.

So this is our first direct comparison here versus a R&S scope used as an analyzer. Three curves are shown - white is the AP310, always our reference.

Red and green are the R&S for two different grounding configurations. (The AP310 doesn't care about the grounding) Strange things happen below 100 Hz. You will notice a lot of the inferior analyzers very carefully avoid this challenging, but crucial, decade of measurement.

We will have a lot more data over the coming months. Stay tuned!



You, Darrell Hambley and 11 others

10 Comments

Like

Comment



Robert L Rauck Night and day difference!

Like · Reply · 4d



Ray Ridley Yes, it's funny. None of the scope makers ever ask me for advice. I have more experience in this topic than anyone else on the planet. Of course, they would have to pay, and that is not going to work.

They don't even know which tests reveal the difference. As long as the interface and graphics look pretty, it all must be good, right?

Like · Reply · 4d

Like · Reply · 4d

**Norman Elias** I hope those other scope makers are seeing this. I wonder how they might respond?!

Like · Reply · 4d

**Ray Ridley** .....with the Sounds of Silence.

Like · Reply · 4d

Write a reply...

**Kevin Azul**



Like · Reply · 4d

**Rok Pajer** I wonder what is the reason for this distortion? Maybe too little samples in low frequency range for good fft calculation or is it too little SNR? I am currently getting familiar with the FFT and facing similar problems in my analysis...

Like · Reply · 3d

**Ray Ridley** Too few bits. and a scope doing things that it was not designed to do. SNR is showing up the problem here. They can never match the AP310 performance, but this LF data is particularly bad.

Like · Reply · 3d

**Jimbo Hissem** Same injection transformer for both?

Like · Reply · 2d



**Ray Ridley** Of course. We only use ours because all of the others on the market are very deficient at low frequencies.



Like · Reply · 2d


Write a comment...

**Ray Ridley** uploaded a file. Admin · March 29 at 1:03 PM

Input filter attenuation and impedance analysis for 5th order filter

 **Filter.xls** Spreadsheet 


  Norman Elias and 18 others 2 Comments

 Like  Comment

**Veda Prakash** Dr. **Ray Ridley**, This is only applicable if the switching power supply is a voltage regulated converter I am assuming. Or in other words not applicable if the power switching power supply is replaced with a power converter with just a current loop (battery charger)? Thanks for the nice file though.

Like · Reply · 2d

**Ray Ridley** It's good for any converter. the input impedance criteria may change, but a current source battery charger is still a constant power device.

Like · Reply · 2d  2

Write a comment...



21 Like Comment

Write a comment...

Ray Ridley Admin · March 27 at 6:27 PM

**Ferroresonance**

For those who have never heard of it, ferroresonance refers to an LC circuit which has an L which is deliberately driven into saturation. The simplest implementation is a series LC tank, followed by a transformer in most cases. The tank is driven by a half bridge, or by a sine wave in the case of the utilities.

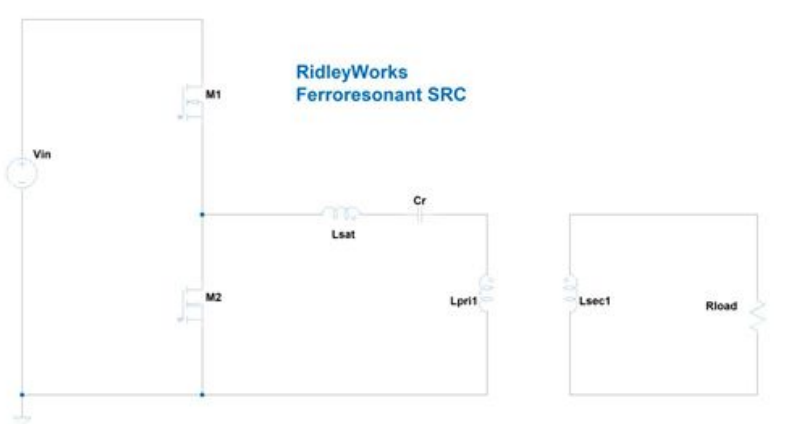
If the switching frequency is above the resonant tank frequency, a phenomenon known as a ferroresonant "jump" occurs. While the inductor is in the linear region, the output voltage will increase linearly with the input voltage amplitude.

When saturation is reached, the output will "jump" to a higher value (how much depends on many factors) and stay there regardless of the input!

A regulated AC output with no control needed.

That's the basis of ferroresonance.

If anyone would like to turn this into a working LTspice circuit and demonstrate it to everyone, fame and fortune (well, just fame) will be yours. Set the switching frequency to 20 kHz just to match the circuit I worked on long ago.



You, Norman Elias and 28 others 44 Comments Like Comment

**Robert L Rauck** The unit I modeled was a 60 Hz design. The configuration was different. I will see if I can resurrect my old notes. It will be fun to discuss. Unfortunately, I no longer have access to the physical unit we used to validate the simulation since my partner passed away several years ago.

Like · Reply · 1w

**David Edwards** Was that Merv Eaton? His entire life was dedicated to the design and manufacture of line frequency ferroresonant transformers. He was ecstatic when he and his team developed accurate LTspice models for ferroresonant magnetics.





**Bob Gudge** I remember Merv! Good man

Like · Reply · 1w · Edited



**Robert L Rauck** [David Edwards](#) No, he was not a well-known person. His name was Bob Burnet and he was a member of the original development team for the Harman Kardon CITATION III Tube Amplifier. He designed a lot of magnets for various purposes.

Like · Reply · 1w · Edited



Write a reply...



**David Seal** Good post.

Like · Reply · 1w



**Robert Turner** Not so much fun when your floating HV network line-ground VTs start exhibiting it though

Like · Reply · 1w



**Ray Ridley** 🗨️ Other configurations are much more complex to understand. That's why we started with this one.

Like · Reply · 1w



**Bob White** What you have described is a a high frequency ferroresonant circuit. There is also a large number of mains frequency ferroresonant converters/rectifiers in use for telecomm and industrial power. These are simply a specialized transformer and a resonant capacitor - no high frequency switching involved.

Like · Reply · 1w



**Bob Gudge** That's where the magnetic shunt comes in I seem to remember  
(Or should I say "Magic Shunt" ) 😊

Like · Reply · 1w · Edited



**Bob White** [Bob Gudge](#) Yes. At AT&T Power Systems/Bell Labs I worked with the late Bob Kakalec who had done a lot of work with ferroresonant rectifiers for telecomm power.

Like · Reply · 1w



**Bob Gudge** I remember once in late 1990s working on the TRIAC battery charger portion (AC line side) of an inverter where the transformer would sometimes BUZZ-HUM in a really loud-ish, weird way... [Brian Faley](#), I think it was, was saying that it sounded like maybe the circuit was going into some kind of ferro-resonant mode when that would happen. (he was the ferro-res guru) This was like a light-dimmer circuit driving the inverter's transformer secondary to regulate the battery side charging. I seem to remember that I had to turn the power off and back on again to get the gawd-awful noise to stop.

Like · Reply · 1w · Edited



**Ray Ridley** 🗨️ [Bob White](#) of course that's correct. Line frequency Ferros are the default.

I just wanted to illustrate it can be done at any frequency.

Like · Reply · 1w



**Brian Faley** My mentor Doug Eaton spent a lot of time modeling ferros at all frequencies with PSIM in the late 90's. I'll see if I can find his sim files.

Like · Reply · 1w



Write a reply...





flattened sine wave or a high quality sinewave (at the cost more bulk filtering). A stable regulation voltage depends directly on a stable line frequency as the two go hand in hand.

[Like](#) · [Reply](#) · 1w



**Alberto Burani** Ferro resonant transformer are still used in microwave oven together with voltage doubler to stabilize the output power of the magnetron.

[Like](#) · [Reply](#) · 1w



**Alex Berestov** Is it really done this way? Never paid attention though.

[Like](#) · [Reply](#) · 1w · Edited



**Julian Waller** Can anyone provide a model for magnetic saturation and real transformer BH in LTSPICE?

[Like](#) · [Reply](#) · 1w



**Ray Ridley** **Julian Waller** don't need a bh loop just the saturation part.

[Like](#) · [Reply](#) · 1w · Edited



**Ray Ridley** Plus it's easier to build and try one at 20 kHz.

[Like](#) · [Reply](#) · 1w



**Colin Tuck** My observations of the "simpler" 60Hz FRT's is that they are standard EI cores with bobbin separated pri and sec and a further higher voltage winding on which the resonant cap sits ( often 600Vac on a 230Vac input ) If the mains volts go up the Tx tends to saturation limiting the Vout ( good for a battery charger ) but if the mains goes down the Vout also reduces ( the limit being zero in )

[Like](#) · [Reply](#) · 1w



**Bruce Wilkinson** One of the high voltage 3kv at 1 amp designs I did used ferro resonance at 30 kHz. It allowed me to utilize leakage inductance and shunt capacitance which can be problematic in high voltage circuits. For the record I did this the mid 1960s. One thing I learned. On start up the primary current draw is very high because the secondary is 180 degrees out of phase with the primary until ferro resonance kicks in.

[Like](#) · [Reply](#) · 1w



**Ray Ridley** So here is the bonus question. Why does the jump happen?

[Like](#) · [Reply](#) · 1w

[Hide 11 Replies](#)



**Col Johns** from a purely analytic point of view - if you run to saturation then there would be extra current in the res cap and more output ... I assume there is an element of magnetic layout not shown in the simple schematic above that comes into play ... (?)

[Like](#) · [Reply](#) · 1w



**Ray Ridley** **Col Johns** everything you need is in the schematic. Just a saturable L.

[Like](#) · [Reply](#) · 1w



**Ray Ridley** I don't expect anyone to get this. It took me almost a year on the bench to come up with an intuitive answer.

[Like](#) · [Reply](#) · 1w



**Bob Gudge** **Ray** So now and after being intuitive, you "feel" it ?

[Like](#) · [Reply](#) · 1w · Edited



It puts the bounce in Gromits bungee.

[Like](#) · [Reply](#) · 1w



**Ray Ridley** I could come up with a great masterclass in the phenomenon but unfortunately the demand is not really there.

[Haha](#) · [Reply](#) · 1w



**Col Johns** OK, at resonance, or just above, when the current is low enough that the L is linear, all the input volts ( nearly all ) are applied to the Tx load. The resonant operation gives a minimum Z from the L & C, as the Vin goes up the current goes up and the L saturates at the current peaks, such saturation vastly reduces the effective L ( although energy is stored ) and now the capacitor is the limiting element as it is no longer resonant ( at the peaks ) so its terminal volts ( at the current peaks ) rise, when the AC drive is reversed, it is in series (aiding) with the charged cap which pushes the core towards saturation the other way more quickly (more voltage drive in total), resulting in the cap being the limiting element again, and so on ad-infinitum.

It is though, hard to see how this results in a constant o/p voltage of the connected transformer ..

The energy delivered to the load would appear to be  $0.5CV^2$  less the energy stored in the inductor when linear (  $0.5LI^2$  ) x 2 x freq. (?)

[Like](#) · [Reply](#) · 6d · Edited



**Bob Gudgel** Ray, you've got it in your blood !

[Like](#) · [Reply](#) · 6d



**Bruce Wilkinson** Ray Ridley I'm not sure what you mean by jump. I suspect that is when the circuit ceases to be linear and the secondary switches from being 180 degrees out phase with the primary to being in phase with the primary. Note that I am referring to a no load condition. Under load the secondary will lag in phase with respect to the primary. A simple but effective model is a series resonant circuit with a saturable reactor across the capacitor. The saturable reactor must have a known saturated inductance.

[Like](#) · [Reply](#) · 6d



**Ray Ridley** The output voltage jumps to a significantly higher voltage with just a small increase in input voltage.

[Like](#) · [Reply](#) · 6d



**Norman Elias** I get it. What you have is a free-running flip-flop. The inductor is flipping from positive saturation to negative driven by current pulses from the resonant capacitor. The capacitor is driven by the voltage jumps at the inductor.

[Like](#) · [Reply](#) · 6d



Write a reply...



**Bruce Wilkinson** Ferro resonance is fairly straightforward. If you want to play with black magic, try doing a parametric transformer. No direct flux coupling between primary and secondary but there is power transfer. Also the secondary is 90 degrees shifted from the primary.

[Like](#) · [Reply](#) · 6d



itself to the drive frequency. Things move very fast with the saturated inductor value, and the "average" value drops (it doesn't really work that way, but you can see the concept i hope).

Since you are now right at resonance, the gain is much higher, and you see the discrete jump in the output voltage.

Then, as you dial the input down, the output stays at the same value. That part is harder to explain without showing the curves which are buried deep in my vaults....

Like · Reply · 6d



**Bob Gudge** "Then, as you dial the input down, the output stays at the same value."

I can almost "feel" that part !

Like · Reply · 6d



**George William Tyler** anyone heard of an "Ott Filter".

Like · Reply · 5d



**Ray Ridley** tell us more...

Like · Reply · 5d



**Brian Faley** I'll bite... An "Ott filter" is a filter used by early square wave inverters (particularly SCR inverters) to shape the output into a low distortion sinewave. It also provides load regulation, and a capacitive load to the inverter.(SCR inverter needed capacitive loading to improve commutation) Class C inverters produce square waves. The Ott filter was used to make sine waves. The GE SCR Manual - 6th Edition - Copyright 1979 ISBN-0-13-796771-3, contains a detailed description of the filter, and complete design procedure (including Smith Charts!). I designed my first around 1982, back in the early days of Renewable energy before there was even such a thing as a high voltage power MOSFET.



Like · 2

Like · Reply · 4d



**Ray Ridley** any more nonlinear analysis in my life will probably make my head explode....

Like · Reply · 3d

Like · 1



**David Edwards** "make my head explode" Didn't you already unintentionally try that once and decide it was a really bad idea? 🤯🤯🤯

Like · Reply · 3d



**Ray Ridley** I did. so i wont 😊

Like · Reply · 3d



**Ray Ridley** I will let the youngsters go there....

Like · Reply · 3d



**Brian Faley** Btw, the ott filter at 60hz was way noisier than a ferroresonant transformer, but also was way lighter. About half the weight. We went through a lot back in those days of 120 transitions per second taking 20usec to turn the scrs off. 250W of idle power at no load.

Like · Reply · 3d



Write a comment...



**David Edwards**

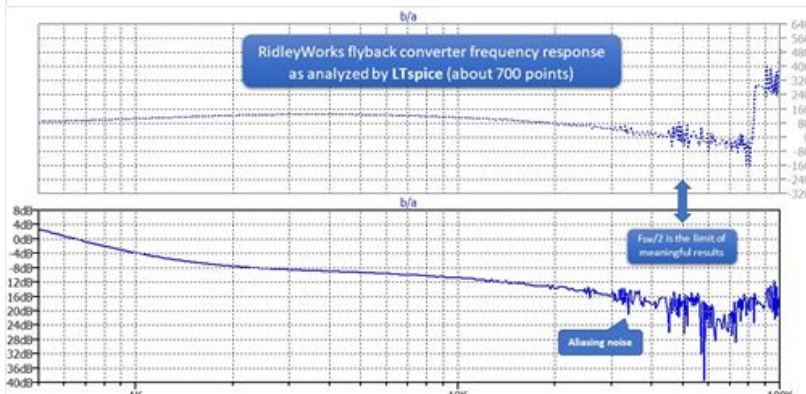
Conversation Starter · March 27 at 2:56 PM

Below is an LTspice loop-gain analysis of the flyback converter from RidleyWorks. I have a fast computer so I had it analyze about 700 points. LTspice performs its frequency response analyzer function with a step command and .meas statements so it does no windowing to mitigate the aliasing effects of partial cycles and cycle misalignment between the test frequency and the switching frequency.

This could be helped by choosing the test frequency to be an integer relation to the switching frequency so that both frequencies consist of full periods at the analysis point (for example, 1:5, 2:7, 2:3, etc.).

The decade sweep step command does not allow this flexibility, but the list version allows each frequency point to be specified. It should be possible to generate the list of points in Excel then copy them into LTspice's step list command. This could allow specifying relatively few points at low frequencies (which take much longer to compute) while increasing point density at high frequencies.

It seems that PSIM suffers from this problem as well whereas SIMPLIS does not.



Norman Elias and 10 others

13 Comments



**Norman Elias** I've encountered the same problem and applied the same solution. Any simulator that provides a windowing function will mitigate the problem but you won't often find a windowing feature built into the AC analysis.

Like · Reply · 1w



**David Edwards** . Hello Norman Elias,

Many years ago I built a frequency response analyzer in LTspice (not a post process via .meas statements) with windowing, but it was painfully slow and still suffered some noise issues. I should dig those files out again as it no doubt would run much faster on the computer I have now.

When you stated that you applied the same solution did you mean choosing the test frequency to be an integer ratio to the switching frequency?

Like · Reply · 1w



the spikes at harmonics of the switching frequency. More than that, I encountered the "noise" you displayed above. It's due to the fact that the number of samples per cycle of the signal is variable. In DSP courses this is called "leakage" and is mitigated by windowing that suppresses samples at either side of the window.

Like · Reply · 1w



**Norman Elias** BTW: I did those simulations with SystemVision. Its frequency domain simulation doesn't provide any built in correction but, if you FFT a transient simulation, you can specify a windowing function that takes care of the problem.

Like · Reply · 1w



Write a reply...



**Ray Ridley** 🌟 Good to see you generating these plots.

It's not really a problem it's just how an analyzer works. You can reduce the noise in the same way that you would with a real analyzer. More cycles, more time.

Simplis has a very different algorithm for solving this so it won't have the issue. Does it matter? Not really unless you are writing some academic papers.

You can always send us files like this and we will help you clean up the sweeps.

The cost of Simplis is prohibitive to most working engineers, that is the downside there.

Like · Reply · 1w



**David Edwards** 🇺🇸 SIMPLIS offers Elements, which is a size limited free version of their insanely expensive program. It would probably work for some if not most of the topologies in RidleyWorks. SIMPLIS produces an output that matches the output of an HP4194 analyzer up to and beyond the switching frequency (even though any results beyond half the switching frequency are only of academic interest).

The LTspice measurement post processing platform does not seem to have the ability to change the x-axis to another variable or an expression as does the main program waveform viewer. The x-axis is fixed to be whatever is stepped in the LTspice simulation. This means that a precisely controlled variable step size is problematic and only available via a list step statement, which is tedious for a large number of steps.

With two cycles of the test frequency, when the test frequency is low there are hundreds or thousands of switching cycles in the same time period so a fractional cycle doesn't contribute significant error. As the test frequency approaches the switching frequency this becomes a problem. One answer, other than integer cycle alignment, would be to increase the number of test frequency cycles at higher frequencies.

Like · Reply · 1w · Edited



**Bryce Hesterman** I have used MathCAD to create frequency sweep lists for LTSpice based on the integer ratios of the sweep and switching frequencies. I also included the number of cycles of the sweep frequency for each data point. This was mostly helpful at higher frequencies. But there is another noise source that wasn't addressed, which is the ringing due to diode recovery that perturbs the duty cycle a bit in converters with current-mode control.

Like · Reply · 1w

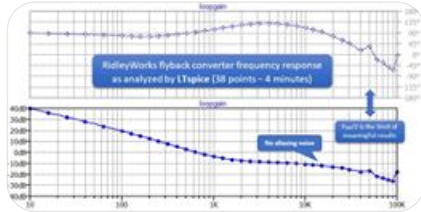


**Ray Ridley** 🌟 If you are down to worrying about that bit of noise, your project is doing well!

Like · Reply · 1w

avoid aliasing at the higher frequencies.

```
.step param Freq list
+ 10 15.8 25.1 39.8 63.1 100
+ 126 158 200 251 316 398 501 631 794 1k
+ 1k26 1k58 2k 2k51 3k16 3k98 5k01 6k31 7k94 10k
+ 12k 15k 20k 25k 30k 40k 50k 60k 70k 80k 90k 100k
* 3 3 1 1 3 2 1 3 7 4 9 1 ; number of cycles
```



Like · Reply · 1w

**Michael Mendley** Very interesting. Can you share the simulation files?

Like · Reply · 1w

**Ray Ridley** Very nice work David Edwards!

Everybody - get your copy of RidleyWorks now so you can all play along and learn a lot!

Like · Reply · 1w

**Ray Ridley** LTspice is great, but you can't do these measurements unless you get the stable loop first from RidleyWorks. Huge time saver.

Like · Reply · 1w

**Kevin Azul**



Like · Reply · 4d

Write a comment...

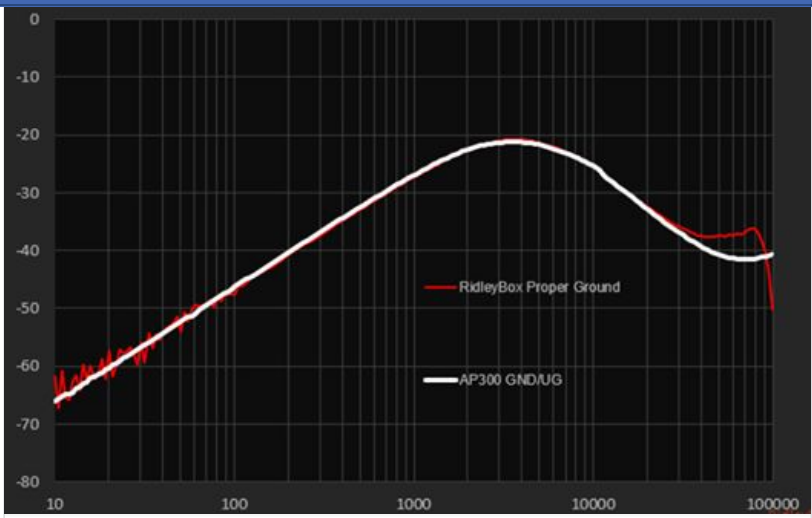
**Ray Ridley** Admin · March 31 at 2:25 PM

### AP310 vs RidleyBox Output Impedance

OK, I know you all have this question - how does the RidleyBox do? Much better than the R&S, that is for sure. Just the caveat that you MUST avoid improper grounding, that is something that we explain in our user manual.

Sometimes you can't - that's when we wheel in the AP310 to verify measurements.

Apart from that, the curves lay on top of each other, and the AP has much better noise rejection - more drive signal, and more dynamic range.



7 5 Comments

Like Comment

**Robert L Rauck** That is rather dramatic!  
Like · Reply · 4d 🤔 1

**Robert L Rauck** But it is less dramatic than the comparison to rival products.  
Like · Reply · 4d

**Ray Ridley** 🛡️ **Robert L Rauck** indeed but this is just one measurement of many.  
Again, the note about grounding is crucial. The AP doesn't care how your system is grounded. Other analyzers will show the differences, sometimes dramatically.  
If you don't have experience it is tough to know how to do the grounding properly.  
Like · Reply · 4d

**David Edwards** 🍷 . **Ray Ridley**,  
I believe Sapphire Instruments Co., Ltd. (<https://www.sapphire.com.tw/>) makes the isolation probe you sell. They make many different models including some 10:1 isolation probes. Perhaps this type of probe could eliminate any grounding issues.  
It seems the RidleyBox uses the PicoScope as the front end and outputs the channels into the Intel computer board, which controls the channel gains and does the DFT calculations. The computer also drives the signal injector output. Perhaps your team designed a custom A/D D/A card for both these inputs and the injector output (do any sound cards have enough bandwidth for this?).  
I would be very interested in a comparison of loop-gain performance between the AP310, RidleyBox and the others.

SAPPHIRE.COM.TW  
Sapphire Instruments Co. Ltd.

**Ray Ridley** 🛡️ **David Edwards** it's all coming. Much work going on with software.  
Like · Reply · 4d

Write a reply... 🗨️ 📷 🎬 🎭





**Clive Harvey**



 Conversation Starter · March 27 at 5:51 AM

Hello all,

Advice on winding flybacks.

I'm currently winding high voltage step up flybacks, turn ratio of as much as 1:100.

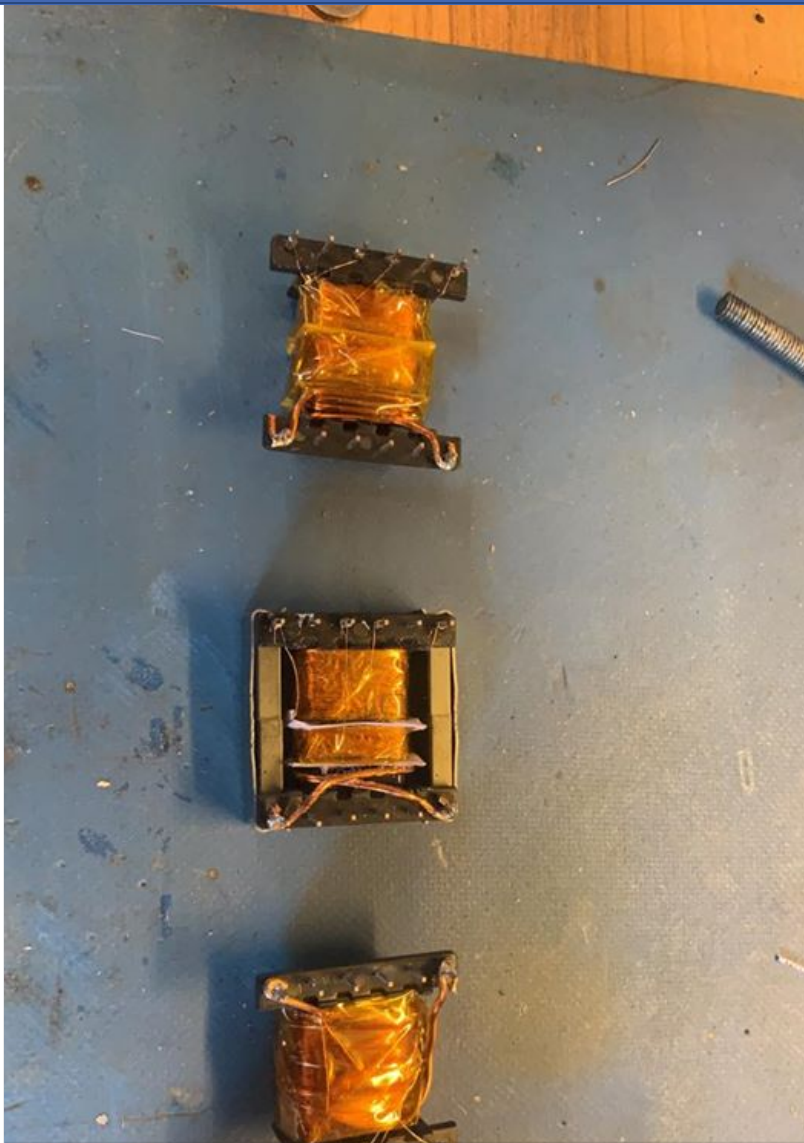
One issue is high leakage inductance, I'm winding in two ways currently.

Primary first and then secondary's over that.

On a split bobbin, so no overlapping of the windings.

Issue being in seeing leakage in the 500n range, so giving me massive voltage spikes.

I'd ideally like to see more than 10x less than that.



6

114 Comments

Like

Comment



**James Gertsen** Flybacks are usually infamous for having troubles with leakage inductance. Have you considered bifilar windings?

Like · Reply · 1w



**Clive Harvey** <sup>👤</sup> **James Gertsen** I'm guessing using bifilar would help with my secondary?

How does this work in high voltage? I'd assume I'd end up with my zero and HV next to each other?

Like · Reply · 1w



**James Gertsen** That is a concern yes. Does your transformer need to be a specific set prototype, or are you allowed to choose of the shelf units as well. If i had the option, i would properly choose an of the shelf transformer, that is close to my desired value, and then modify my other components to match that value in stead.

Like · Reply · 1w



**James Gertsen** <https://www.coilcraft.com/transformsel.cfm>

COILCRAFT.COM

Flyback Transformers (DC-DC, Constant Voltage, Telecom, VDC) | Coilcraft



**Clive Harvey** James Gertsen the coil craft options were my first go too, but unfortunately they just don't offer what I need.

Like · Reply · 1w

**Clive Harvey** What sort of isolation does the bifilar offer?

Like · Reply · 1w

**Jimbo Hissem** Depends on what wire you use, and what standards apply.

Like · Reply · 1w

Write a reply...

**Joel Holland** What about interleaving windings? Also 500nH seems quite small?

Like · Reply · 1w

**Jose Castro** To decrease LL, you want to increase winding coupling. This will increase interwinding capacitance (be aware).

You don't want to use a split bobbin.  
What we have tried in the past is sandwiching the windings.

Like · Reply · 1w

**Clive Harvey** So due to the turn ratio my primary inductance is only targeted around 1u, this obviously means the 500n LL is pretty significant.

One thing I have considered is using some copper tape for the primary, any thoughts on this?

Like · Reply · 1w

**James Gertsen** remember in a flyback the transformer works as a coupled inductor. you need to be careful about that air-gap as well

Like · Reply · 1w

**Clive Harvey** James Gertsen I'm currently using <https://www.digikey.co.uk/.../B664.../495-5534-ND/3914952...>



DIGIKEY.CO.UK  
B66423U0315K187 TDK  
Electronics Inc. | Magnetics -...

Like · Reply · 1w

**Tony Salsich** A high step-up turns ratio will lead to high leakage inductance. Bifilar winding is not really a viable path with a 1:100 ratio, imho. In addition, photo indicates a primary that is not overlapping the secondary which makes leakage even worse. Two separate techniques come to mind:  
1) use a two-switch flyback to clamp the spike to the bus  
or  
2) add a winding that is 1:1 and bifilar to the primary, along with a diode to clamp the spike to the bus  
How many layers is the secondary? What is the primary voltage?  
What is the switch rated for?

Like · Reply · 1w · Edited



topologies, the issue is I ideally need an automotive qualified switcher, that's really restrictive.

So I'm currently using a efd30 bobbin.

This splitting the secondary I have around 6-7mm too wind on.

So if I go with a single turn, primary that's two layers, but obviously if I up my primary inductance, as that's rather low, I'm more into the 3-6 layers.

My primary voltage is 9-18v.

The switch is currently a 60v switch, which was fine when I thought my LL would be below 50n, I'm not considering responding the pcb for a 250v fet.

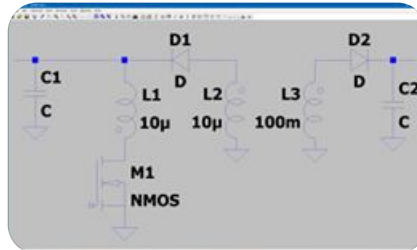
But ideally I need to get this spin working.

[Like](#) · [Reply](#) · 1w



**Tony Salsich** The clamp winding may be a good approach if you have little room for change. It adds the cost of the bifilar winding and a diode, but that's it. See the below simplified sch.

The reflected secondary volts must not reach the value of the lowest bus voltage.



[Like](#) · [Reply](#) · 1w · Edited



**Clive Harvey** 🗨️ **Tony Salsich** well that's doable, does it have to be bifilar? Can I use magnet wire?

[Like](#) · [Reply](#) · 1w



**Tony Salsich** Yes to both. Wrap the the primary with the clamp winding - they are the same wire and the insulation is good enough for your voltages. The 1:100 ratio will have to increase since the reflected volts is limited to Vbus minimum. Another caveat is that the leakage energy will take time to dump back into the bus, and the clamp diode must be rated for the peak current. Nothing is free with mother nature.

[Like](#) · [Reply](#) · 1w · Edited



**Tony Salsich** You can increase the turns of the clamp a bit to increase the VOR allowance, but then leakage becomes an issue again.

[Like](#) · [Reply](#) · 1w



**Clive Harvey** 🗨️ **Tony Salsich** I'm not quite understanding what you mean by "reflected volts being less than Vbus min"

From what I remember the reflected voltage is the output voltage by the ration, so does this mean at min input voltage of 9 volt, output voltage at 2kv.

I'd need a turns ratio of 222?

At which point isn't it acting as a transformer not a flyback?

[Like](#) · [Reply](#) · 1w



**Tony Salsich** The clamp winding is a simple method to limit the spike, but it is another 'output' winding which must not be allowed to put the main stored energy back onto the bus. As I said, you can alter its turns ratio relative to the primary at the cost of increasing its leakage with respect to the primary. Thinking about this more, I suspect your step up ratio is going to prevent you from using a hard switched approach. That is unless you add a voltage multiplier to the output.



Write a reply...



**Stuart Wood** Also, with high step up designs the parasitic capacitance get multiplied by the turns squared!. This is why many designs go to a sinewave drive or resonant converters.

Like · Reply · 1w



**Alain Laprade** automotive requirement gums up the picture. Likely needs to stay out of the AM band. A MUST for most automotive customers.

Like · Reply · 1w



**Stuart Wood** Depending on the output voltage you way want to consider a multi segmented bar frame core.

Like · Reply · 1w



**Clive Harvey** 🗨️ **Stuart Wood** I was shown one of these, it was used for a resonant converter.

Do you know how the gapping works with them?

Like · Reply · 1w



**Stuart Wood** Honestly most are used in forward converters, but I believe you would gap the ends of the bars with tape.

Like · Reply · 1w



**Clive Harvey** 🗨️ **Stuart Wood** ok, that's interesting.

I was shown this, is this what you mean?

[https://elnamagnetics.com/.../Design\\_of\\_CCFL\\_Backlight...](https://elnamagnetics.com/.../Design_of_CCFL_Backlight...)

Like · Reply · 1w



**Stuart Wood** **Clive Harvey** Yes! The CCFL market perfected these for use in the LCD backlighting market. Before LED took over. You can easily get 3KV at 10W out of these with out much effort.

Like · Reply · 1w



**Clive Harvey** 🗨️ **Stuart Wood** and is still be able to run it as a flyback?

My issue is, I have to do this auto qualified, so that's basically limited me too a flyback and probably a boundary mode one.

Like · Reply · 1w



**Stuart Wood** **Clive Harvey** of hand I don't know how hard it would be to control your AL value in this type of core...

Like · Reply · 1w



Write a reply...





I'd recommend getting away from the split bobbin and going to a copper strip primary across the entire width of the bobbin.

Unless you make a resonant flyback design, you need to minimize the number of layers on the secondary.

You will get best results if the secondary is just one layer all the way across. If necessary, oversize the transformer to make this possible. It will minimize leakage inductance, winding capacitance, and transformer self resonance.

Stay away from Kapton tape in a high voltage flyback. The kapton will carbonize in the presence of corona, and will then begin to smoke as the insulation continues to degrade even further while the converter is operating.

I assume your input voltage is a normal 12V car battery system.

What is your required output voltage and current?

[Like](#) · [Reply](#) · 1w · Edited



**Clive Harvey** [Cameron Stewart](#) I have some copper foil tape, I was thinking of trying that with this, would that work?

This is a 2kv and 4kv output 9-18v in.

The output is in series, with the 2kv being controlled and the 4kv being an auxiliary.

Currently designing for 10mA max on the 2kv, the 4kv is very low, 1uA is likely,

[Like](#) · [Reply](#) · 1w



**Cameron Stewart** [Clive Harvey](#)

This is a 20 watt application. Without doing any other calculations, my gut feel is the copper tape will probably work.

If you know the thickness of the copper - typically 2 to 5 mils - you can calculate the total number of mils and the total winding resistance to get an idea of whether or not your copper losses are acceptable.

You will need to winding spacing tape over the copper primary before you wind your secondary, to minimize winding capacitance.

Again, stay away from Kapton!

[Like](#) · [Reply](#) · 1w · Edited



**Dan Watts** Maybe use a voltage doubler on the 2KV out to get your 4KV. Then your turns ratio could be halved.

[Like](#) · [Reply](#) · 1w



**Clive Harvey** [Cameron Stewart](#) I don't know the thickness, I'm going to measure the resistance and see what it comes in at, but I'm hopeful lol

[Like](#) · [Reply](#) · 1w



**Clive Harvey** [Dan Watts](#) that's my option if I can't get this LL down low enough.

Being automotive it's every penny counts, if I can get the magnetics right and not need the extra parts that's my best approach. I think lol

[Like](#) · [Reply](#) · 1w



**Cameron Stewart** [Clive Harvey](#)

Purchase a micrometer from Harbor freight, or other suitable outlet.

You are going to need it for measuring the thickness of your copper tape and your core gapping materials.

Use glass cloth tape with transformer varnish for your insulation, rather than Kapton.

[Like](#) · [Reply](#) · 1w



convinced it'll be accurate enough,

That's a good call, I have some glass fibre tape I think and more varnish on the way.

I can see why that would be superior to kapton, but is the an issue using kapton?

Like · Reply · 1w



**Cameron Stewart** Clive Harvey

You'll see what I mean, after your transformer has been running for 5 minutes and smoke begins to pour out of it, as the Kapton tape carbonizes from the corona your transformer is generating .....

Like · Reply · 1w · Edited



**Clive Harvey** 🗨️ Cameron Stewart arrrr yer that doesn't sound ideal haha

Cheers for the tip.

Like · Reply · 1w



Write a reply...



**Dan Watts** You mentioned cost sensitive so this idea may not fit and it was for a 1:3 ratio but maybe it will give you some new ideas for low leakage flyback design. I needed an ultra low leakage flyback for a single stage isolated PFC with regulated 270VDC output. Input was 100V - 300W. The low leakage was needed because this was for high altitude airborne with no practical way to cool a snubber AND returning energy to the input bus (via diodes) created too much distortion for good PFC/low input harmonics. My solution was to interleave Pri/Sec on a toroid. Start with 3 twisted strands of Litz wire for Pri. Then 3 SETS of twisted 4 strands of Triple safety wire for Sec. All are of equal length and get twisted together (4 sets of pre-twisted wire). Twist the 4 sets in the opposite direction of how they were twisted together or it's a lumpy mess. Now wind your your transformer with the 4 twisted together sets. You then connect the 3 sets of secondaries in SERIES. Must be careful about polarity and insulating the 2 splices. The whole structure was then thermal coupled and mounted to a cold plate for liquid cooling.



Like · Reply · 1w



**Clive Harvey** 🗨️ Dan Watts I can see how that's really well coupled, but I doubt that would work for me given the turns ratio I need.

Like · Reply · 1w



**Dan Watts** Agree, it might be practical (but expensive) to do at say 1:10 ratio but note 1:100. I know you are cost sensitive but it may be cheaper (and more reliable) to consider an off the self x-former and some multiplier diodes OR don't use a flyback. If you must do a flyback with high ratio, chose a core with the widest winding window and use a foil for the Pri

Like · Reply · 1w · Edited



**Clive Harvey** 🗨️ Dan Watts yer foil is going to be the rest of my day lol

Like · Reply · 1w



Write a reply...



this. I recommend using the triple insulated wire for safety and to eliminate the need for margins.

Transformer capacitance will be the limit of what you can do.

Sweep the impedance 😊

Like · Reply · 1w

**Clive Harvey** 🗨️ **Ray Ridley** yer doing a sweep is on my list haha.

Just dug out and old function generate that was thrown away by an old employer, been sitting there for me to test haha

Like · Reply · 1w

**Ray Ridley** 🗨️ That was my first introduction to power electronics. Enjoy!

Share the curves as you gather them.

Like · Reply · 1w

**Clive Harvey** 🗨️ **Ray Ridley** will do, I'll need some help interpreting them.

Like · Reply · 1w

Write a reply... 🗨️ 📷 GIF 🗨️

**Cameron Stewart** There are trade-offs with using the triple insulated wire.

It certainly solves your insulation issues.

However, the extra wall thickness of the triple insulation may be prohibitive in winding your secondary and fitting it on the bobbin.

So, you will need to calculate your winding window requirements carefully to determine the maximum wire plus insulation wall thickness that you can tolerate.

Like · Reply · 1w

**Ray Ridley** 🗨️ Use the VIP wire and there isn't much increase in thickness. I always use theirs for this reason.

Like · Reply · 1w

**Tony Salsich** I am not familiar with VIP (or may have forgotten)

Like · Reply · 1w

**Clive Harvey** 🗨️ **Ray Ridley** where's best to buy it from?

Like · Reply · 1w

**Tony Salsich** Is this the wire from Germany (oder irgendwo anders)?

Like · Reply · 1w · Edited

**Colorado Mike Doherty** Link to source?

Like · Reply · 1w

Write a reply... 🗨️ 📷 GIF 🗨️

**Ray Ridley** 🗨️ It's a good old made in the USA wire. The best there is. They actually have a 590 degree C wire that they sell to JPL.

Like · Reply · 1w

**Ray Ridley** 🗨️ Virginia Insulated Products in Saltville, VA.

Like · Reply · 1w

**Clive Harvey** 🗨️ **Ray Ridley** does this need buying direct?

Like · Reply · 1w





Tell him I sent you 🤔

Like · Reply · 1w



**Ray Ridley** 🌟 Their "normal" wire is class F and it's rated 10 kV dc.

Like · Reply · 1w



**Clive Harvey** 🗨️ **Ray Ridley** awesome cheers.

Like · Reply · 1w



Write a reply...



**Paul Ryan** I've made small HV flyback transformers. Many issues: yes, leakage inductance is a problem, often you just have to live with it, but things you can do: don't use a split bobbin, leakage inductance will be terrible. You can try splitting the secondary and inserting the primary part-way through. A fundamental factor is always the secondary self capacitance, and this gets really big if you're trying to produced the desired DC output directly from the winding; instead it's worth considering following the transformer by a doubler or tripler voltage multiplier. Another key factor is exactly how you wind the secondary. The approach I found works best is to wind in single layers with tape between AND make sure the windings are all wound traversing the same direction along the bobbin, so the layer-layer voltage difference is minimised. And don't forget to allow enough margin tape to prevent arcing between the layers. I got to 6kV on an EFD15 using a doubler.

Like · Reply · 1w



**Clive Harvey** 🗨️ **Paul Ryan** thanks for that.

Can I ask what sort of turns ratio, vin and power you were working with? What LL did you achieve?

The winding method you mentioned, would that be a C or Z winding?

Also I'm playing with using foil for the primary at the moment, have you tried this?

Like · Reply · 1w



**Paul Ryan** I'll reply by private message, I need to be a bit careful because of client confidentiality

Like · Reply · 1w



**Clive Harvey** 🗨️ **Paul Ryan** ok cheers

Like · Reply · 1w



Write a reply...



**Ray Ridley** 🌟 Thanks **Paul Ryan**, solid advice. I wouldn't change a thing.

Like · Reply · 1w



**Markus F.L.** Please, you have with prim 1solid wire Wire ? WHY YOU HVE PRIM 3 WINDING what surfave Surface IS THIS? isnt good make 3 Winding with multiple wire paralell , parallel in one layer, maybe NEXT you can make it ist PRIM//// SEK ////PRIM WITH more ISOLATION LAYER between betreuen and you have less Lstray

Like · Reply · 1w



**Markus F.L.** dont make prim layer Layer ground and Prim Layer out with Paralell! Thats not good!

Like · Reply · 1w



**Clive Harvey** 🗨️ **Markus F.L.** Sorry the translation isn't coming through well, I'm finding it hard too follow what your saying.

Markus F.L. I have auto Auto coorection Cooperation is bad

Like · Reply · 1w

Markus F.L. what i mean is make prim winding Winding with 3 Windings with more single Single wire you must Must have more surface Surface at the komplete komplette layer in the Bobbin space

Like · Reply · 1w

Write a reply... [emojis]

Colin Tuck It's all been said above, T.I.W. / teflon wire with multiple pri's ( in // ) and multiple sec's ( in series ) to get the leakage down ...

Like · Reply · 1w

Clive Harvey @ Colin Tuck

Ok, so would using the thinnest primary I can help with leakage? Or using multiple thiner strands making upto the minimum? I'd taken the approach you use the thickest you can, to minimise losses.

Like · Reply · 1w

Colin Tuck Clive Harvey, Nope, just wind primary ( 2 or 3 parallel wires if you like ) then part sec, then pri again, then part sec, then pri again, then part sec, then pri again. the pri wires will be quite small as you now have so many in parallel, the sec wires will be what they need to be ...

Like · Reply · 1w · Edited

Colin Tuck Spread each pri winding over the full width of the bobbin to reduce leakage ( increase coupling ).

Like · Reply · 1w

Markus F.L. Yes

Like · Reply · 1w

Clive Harvey @ Colin Tuck my issue with my primary winding is so few turns, somewhere from 1-3 turns?

Maybe I could do one turn per layer.

1T primary  
100T secondary  
1T primary  
100T secondary  
1T primary  
100T secondary

Like · Reply · 1w

Col Johns Clive Harvey or use several ( smaller ) wires in parallel for each pri layer to put more "surface" on each layer ...

Like · Reply · 1w

Clive Harvey @ Col Johns arrr got ya, I see what your saying now.

Like · Reply · 1w

Colin Tuck yup ...! to "spread out" the one turn, ( two turns might be better from a coupling point of view ).

Like · Reply · 1w · Edited

Clive Harvey @ Colin Tuck cheers like Marcus just said, I'll try 20x 0.15mm should give greater surface area.

Like · Reply · 1w



**Markus F.L.** FIW 6 Wire only for sek

Like · Reply · 1w



**Markus F.L.** prime try trägt 20x0,25 magnetwire Magnetstreifen not Not HF Litz Wire! 20x0,25 x3 winding Winding = 20mm space

Like · Reply · See Translation · 1w



**Markus F.L.** sek try Gary Fiw FIW 6 ore Orte higher 100 winding Winding with 0,10 mm so you have 17 mm and each edge Edge 2mm isolatin

Like · Reply · 1w



**Markus F.L.** FIW 6 are at the solid wire min 6KV isolation

Like · Reply · 1w



**Markus F.L.** You need Need more surface Surface for prim to sek you have space Space prim 20mm and sek 20mm but you user prim only Unity 3mm to 20mm..

Like · Reply · 1w



**Markus F.L.** And prim layer to sek layer look at the high wire ends ,voltage hub not at the same edge from bobbin

Like · Reply · 1w



**Markus F.L.** Other solution last month i build a flyback EFD 30 with bobbin

Like · Reply · 1w



**Markus F.L.** EFD 20 with this:

Like · Reply · 1w



**Markus F.L.**  
[http://www.pinshine.com/.../pdf/20090901110210\\_link.pdf](http://www.pinshine.com/.../pdf/20090901110210_link.pdf)

Like · Reply · 1w



**Markus F.L.** At this you have to wor with you snubber and elektronik

Like · Reply · 1w



**Markus F.L.** but it give a good solution

Like · Reply · 1w



**Markus F.L.** With ths bobbin even though the stry is not optimum low

Like · Reply · 1w



**Clive Harvey** 🇬🇧 I've just got a split bobbin drawn up to be 3D printed, to see what I can get out of it.

Right now, it's looking like the LL will be too high.

I'm trying to understand your other points, but I'm struggling with the Language barrier,

It seems the main point your making is I have too much separation between my primary and secondary,

The other approach I'm working on is, primary using copper tape, that should be the biggest coupling surface area?

Like · Reply · 1w



**Markus F.L.** Dont use copper tape too much C

Like · Reply · 1w · Edited



**Markus F.L.** start pin 3 connect 20 magnetwires with 0,15 make at bobbin 3 winding spread it connct at pin other side so you have one layer winding 20mm spread with 3 winding

Like · Reply · 1w



the logic now.

Like · Reply · 1w



**Markus F.L.** Excuse me working at mobile phone..

Like · Reply · 1w



**Kevin Enser** Reduce the turns as much as possible, drive it at a higher flux density.

Like · Reply · 1w



**Kevin Enser** To be clear, the motivation is to reduce the factor of turns squared in the leakage inductance formula, it has nothing to do with flux density other than it's going to increase so you'll have to pay attention to Bs at and core losses and maybe change core materials.

Like · Reply · 1w



**David Fletcher** [Kevin Enser](#) What is your desired output voltage

Like · Reply · 1w



**Col Johns** from above posts the Vin is 9 - 18V and Vout is several kV ... 2 outputs in fact : "10mA max on the 2kv, the 4kv is very low, 1uA is likely"

Like · Reply · 1w · Edited



Write a reply...



**Col Johns** For a flyback, even though the Vin is 9 - 18V - the flyback volts could easily be 500V ( 600V device ) as this allows a better turns ratio, i.e. 10 : 30 giving 1500V of o/p per sec wdg, and making it easier to spread the "LV" pri over the bobbin.

& giving lower leakage...

If the HV has a common gnd then the windings can be auto-transformer wound, i.e. 500 + 1500 V = 2kV out ...

getting close to 2kV at full load on one o/p ( 20W ) and close to 4kV on another winding, at the same time, may prove problematic.

Like · Reply · 1w · Edited



**Gerhard van Eerden** If Quasi Resonant flyback is allowed, you could use a split bobbin transformer by adding a large capacitor in parallel to the primary. The resonance frequency determines the operating frequency.

During transistor off time the primary voltage is kind of half sine wave while the secondary voltage is quasi square wave. The primary and secondary being side by side results in a very low primary to secondary capacitance. Together with the more or less sinusoidal waveforms this can give very good emi performance.

The secondary winding capacitance can be lower because the winding width is reduced while the winding height is increased.

If the secondary winding capacitance is still too high you could split the secondary in series connected sections with each one layer, a rectifier and capacitor.



Like · Reply · 1w



**Colin Tuck** Quasi resonant is a lot easier on the o/p diodes ...

Like · Reply · 1w



Write a reply...



**Markus F.L.** 2. solution 2KV Flyback



Like · Reply · 6d



**Clive Harvey** Markus F.L. Isn't that similar too the one I did, but more turns and custom split bobbin?

Like · Reply · 6d



**Markus F.L.** yes

Like · Reply · 6d



**Markus F.L.** but with FIW 6 Wire High Voltage Isolation Wire its for >6000V savetey

Like · Reply · 6d



**Clive Harvey** Markus F.L. Are you saying the primary windings are 6 core?

Also I thought your suggestion before was about not using a sectioned bobbin and spreading the primary over the whole winding window using multiple strands?

I'm currently winding a 4.5t primary with 20 strands of 0.2mm.

Like · Reply · 6d



**David Edwards** Clive Harvey, half turns increase leakage inductance significantly (think about the flux linkages).

Like · Reply · 6d



**Clive Harvey** David Edwards How is it best to return the winding back too the return pin?

Like · Reply · 6d



**Colin Tuck** The above Tx only works well in a resonant ckt ( which CCFL are )

Like · Reply · 5d



**Clive Harvey** Colin Tuck that's where I've seen these Tx's used.

Is that cause it's a sinusoidal waveform? No fast edges to cause voltage spikes?

Like · Reply · 5d



**Colin Tuck** Clive Harvey correct ... you can tell from the multiple input LV wires that it is not a flyback Tx but for a resonant CCFL push pull

Like · Reply · 5d · Edited



**Clive Harvey** Colin Tuck yay I got something right haha

Like · Reply · 5d



Write a reply...

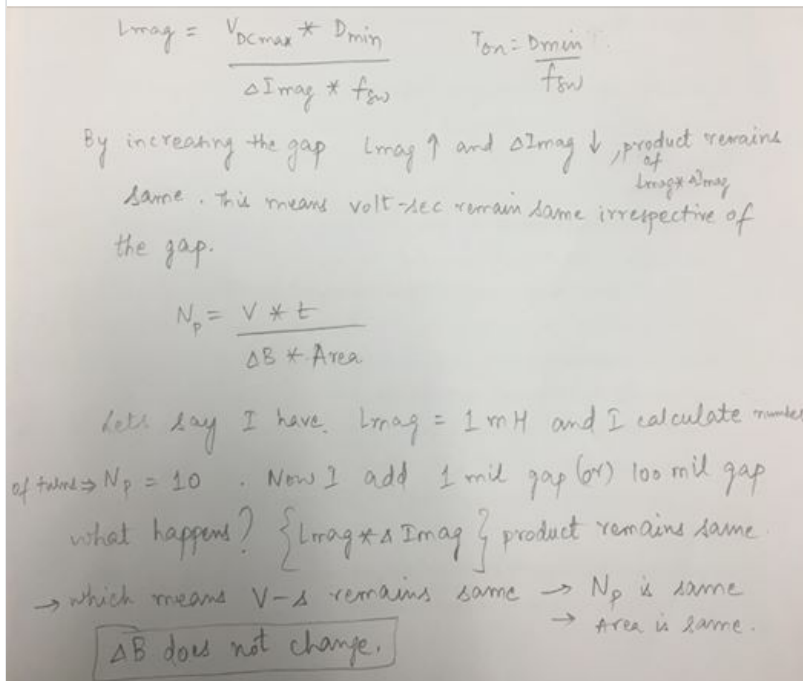


Write a comment...





I was going over the active clamp forward question in this forum. I have put down 2 equations on a paper which show that adding a gap does not help the transformer in avoiding saturation. This appears debatable. Can the engineers share their thoughts?



You and 5 others

38 Comments



Like



Comment



**James Keith** In the school I have plotted the B-H curve on an oscilloscope as a part of power systems course, but the equations do not show dependence on the gap

Like · Reply · 1w



**Ray Ridley** It's a nonlinear thing regarding remanent flux.

Normally the inherent gap in a two-piece core is enough to not worry about it.

Like · Reply · 1w



**Col Johns** worry about which exactly ... ?

Like · Reply · 1w



**Ray Ridley** Col Johns remanence.

Like · Reply · 1w



**Ray Ridley** But that can change for some materials. Nothing is absolute in this business

Like · Reply · 1w



**Col Johns** Ray Ridley surely the remanence is independent of gap - I have never seen any thing to suggest there is a magic ability of the core to reduce its inherent remanence due to the addition of a gap ...?

Like · Reply · 1w · Edited



**Ray Ridley** The bh curve gets tilted so the flux drives to a lower value.

I've never gapped a forward. They have never complained.

Like · Reply · 1w



**Col Johns** Ray Ridley - you have side stepped the question - but that is OK ...



**Ray Ridley** Col Johns not sure I understand?

Like · Reply · 1w



**Col Johns** Ray Ridley it really is of little import, but ( and there it is ) unless the gap is very large indeed - the remanence of the system ( core + gap ) will change very little - the remanence of the core is an intrinsic property of the core which cannot be altered by adding a gap, luckily it is low for soft ferrite ( hence the name soft ). For materials with high remanence adding a gap does give a differing system with apparent lower remanence - but of course the core itself does not have its intrinsic physical properties changed.

Like · Reply · 1w



**Ray Ridley** i think we are using different terminology, but that's ok. I'm not going to worry about this to much.

As you say, not so important to worry about.

Like · Reply · 1w



Write a reply...



**Sobhi Barg** I think increasing the air gap reduces Lmag. Then the core will be able to conduct higher magnetizing current without saturation.

Like · Reply · 1w



**Michael Delany** Sobhi Barg my understanding too is that increasing the air gap reduces permeability and therefore inductance. This results in a higher field strength needed to saturate the core, thus more current.

Like · Reply · 1w



**Michael Delany** Sobhi Barg basically reducing the slope of the BH curve.

Like · Reply · 1w



**Ray Ridley** Darn it, if APEC hadn't been cancelled we could all have gone to the magnetics sessions and figured this out for sure...

Haha · Reply · 1w



**Cameron Stewart** I'm waiting for Dr. Cuk to weigh in on this ....

I've always heard that adding a gap makes it easier for the core to reset back to zero, after excitation is removed.

I don't claim to know exactly why.

Like · Reply · 1w · Edited



**Bruce Wilkinson** Active clamp forward converter has the advantage that the flux in the core is actually reversed allowing use of the full flux capacity of the core. Theoretically no gap is required because the clamp switch keeps the voltage reversed until the volt-second balance is satisfied.

Like · Reply · 1w



**Ray Mayer** Right up to the point where it get hits with a severe transient and V-uS don't balance for a few cycles... (or turning it on or off).

"The worst thing you can do to a power supply is turn it on or off."

Like · Reply · 1w



**Bruce Wilkinson** That's where the witchcraft comes in. It becomes a matter of giving enough flux margin to allow for flux walking and the right balance between magnetizing inductance and clamp capacitance to allow rapid enough clamp voltage change for regaining balance.

Like · Reply · 6d



placing a GAP in SERIES with the magnetic path length this is increased reluctance in the path-length...  $RL = (le / \mu r + lg) / (\mu_0 Ae)$ . you are effectively storing most if not all the energy in the air gap.... It will then return to 0 flux much quicker and easier....but then again is it worth it ?? If your switching frequency is reasonable and you don't want the excessive magnetizing current ??

Like · Reply · 1w



**Alex Berestov** Well, it's yes and no. In forward converter B returns to a Br (remanent or residual) flux density. When you flatten the curve, lowering mu, apparent Br value moves towards zero. Thus usable flux density will be higher. For instance, N87 material, Br is 0.1...0.2T, depending on temperature. Usable delta B looks like 0.1T for gapless and well might be 0.2T for gapped. Secondly higher magnetizing current eases resetting the core.

Like · Reply · 1w · Edited

^ Hide 11 Replies



**Ray Ridley** Alex Berestov thanks for that.

Like · Reply · 1w



**Col Johns** Alex Berestov re: " Usable delta B looks like 0.1T for gapless and well might be 0.2T for gapped."

are you implying you can get extra traverse of BH loop to higher B with no extra losses for gapped core?

Like · Reply · 1w



**Alex Berestov** Yep.

Like · Reply · 1w



**Cameron Stewart** As far as I know, adding a gap increases the Oersted handling capability of the core, not the maximum flux density it will handle, for the same number of primary turns.

At least, that's what the equations say, irrespective of any physical interpretation.

Like · Reply · 1w · Edited



**Col Johns** Alex Berestov that is a really good trick - running a higher B in the core at the same freq - but getting the same losses ...!

Like · Reply · 1w



**Alex Berestov** Where did I say about losses? However one may compare square loop core with the soft loop one in terms of usable delta B.

Like · Reply · 1w



**Bob Gudgel** On an extreme outlook, certainly, gapping the core sort of makes the magnetic circuit more like air so I suppose that reduces Br since air doesn't have any Br.

Like · Reply · 1w



**Col Johns** the limit for useable B in an ungapped core is losses - gapping in no way reduces this limit... i.e. more peak flux = more core losses ...

Like · Reply · 1w · Edited



**Alex Berestov** Sure. However, imagine old BJT Darlington power modules so losses are not a factor. When the trees were high. In reality, in high power applications we've used core biasing, using LV aux pwr supply and inductor.

Like · Reply · 1w



**Col Johns** Yes - a gapped core without a Darlington is like a fish without a bicycle.



**Alex Berestov** That's why the transformers cores were gapless toroids.  
Cheers

Like · Reply · 1w

Write a reply...

**Sesha Sai Kumar** Dear **James Keith** well your analysis is correct. I understand it is bit ambiguous that with same case in an inductor. Firstly, In an inductor when we wish to add airgap to slow down the saturation, Here we still wish to design the inductor for same magnetizing current which is defined more by the topology of the converter. So, now later to maintain same inductance after adding gap we increase the number of turns in that process if you calculate analytically we see the Bmax operating drops for the same magnetizing current. We keep repeating this cycle adjusting the gap as long as we achieve safe Bmax for the rated magnetising current. Now in a transformer if we see, here while inserting a gap itself doesn't help for saturation as long as we wish to increase the no.of turns( as you observed with your equation and also same can be understood from transformer emf equation). So if we dont disturb the no.of turns and just add air gap, it simply drops the magnetising inductance and draws more mag.current.

Like · Reply · 1w · Edited

**Anindya Dasgupta** As others have also pointed out, by just increasing the gap, reluctance increases and Lmag will decrease. On a slightly different perspective, it is strange to see why most of the design articles care so much about putting a gap in the transformer ?! Why not design the transformer as a transformer is supposed to be i.e. without any gap and then add a small inductance as the resonant inductance. For sub 100W category or so where these converters are primarily used, adding a high SRF chip inductance (Lr) with a well designed transformer without gap might be a better option than the gapped one (more lossy).

Like · Reply · 1w

**Alex Berestov** Which way will you connect the inductor of yours? In series or in parallel?

Like · Reply · 1w

**Anindya Dasgupta** series

Like · Reply · 6d

Write a reply...

**Colin Tuck** On the hand drawn notes, it says: " By increasing the gap Lmag ^ and delta Lmag down.." this is in fact the wrong way round, increasing the gap the Lmag goes down and the delta Lmag ^ ...

Like · Reply · 1w

**James Keith** Yes, you are right. Its a typo.

Like · Reply · 1w

Write a reply...

Write a comment...

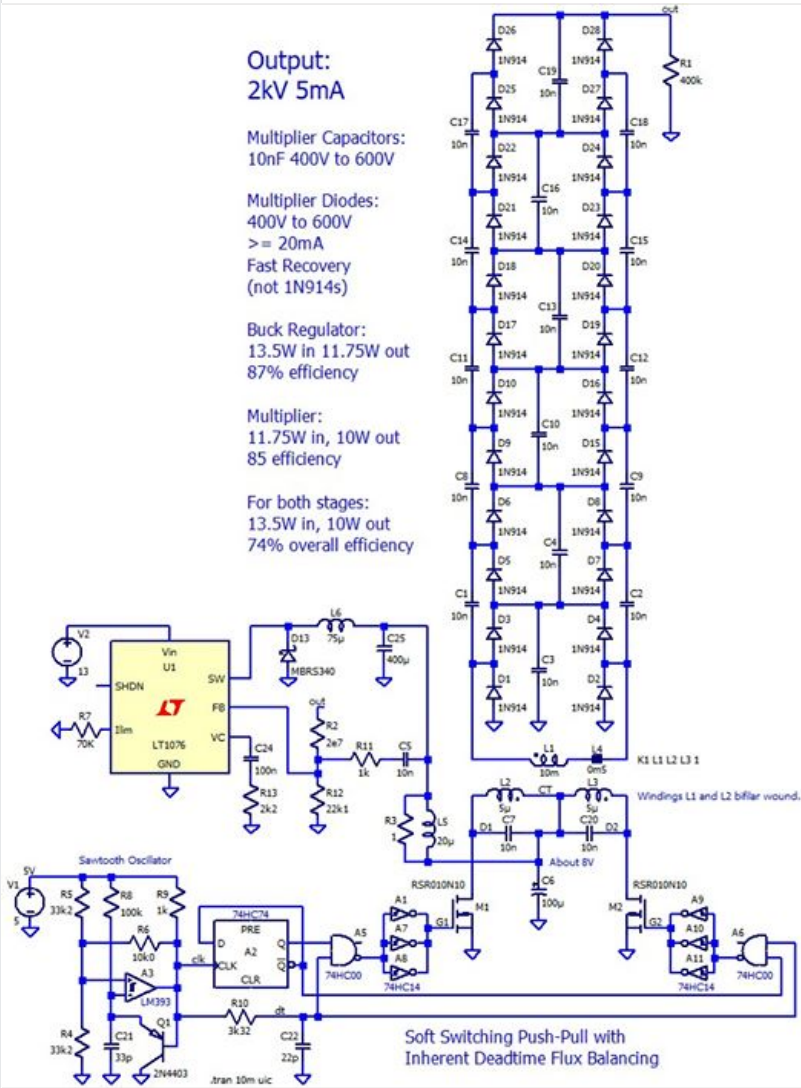


**David Edwards**

Conversation Starter · February 11

Not the LM5155

Here is an alternative to the 2kV 10W LM5155 and flyback transformer design. The components should be surface mount laid out in a row with adequate spacing for the voltage (laid out like the schematic) to avoid corona issues.



👍❤️😄 You and 16 others 56 Comments

👍 Like 💬 Comment



**Scott Styles** we have done similar (although not smt) for some production testers that needed a decent bias. also nicely short circuit proof to keep h&s happy (or as happy as h&s are able to be)

Like · Reply · 7w



I totally get the advantages too this approach, shifting the voltage stress out of the magnetics into the output stage.

But this would double if not triple my board cost and pcb size.

In automotive application that's a deal breaker.

Something I have been considering, is more series secondaries, to spread the voltage out?

So rather than one single layer of 1:100, maybe a single layer split into 4x 1:25 D.C. stacked.

Would this help prevent the corona? Also how much does output current effect corona?

Like · Reply · 7w



**Walter Anton** kann mann so machen, muss man aber nicht....

Like · Reply · See Translation · 7w



**Bob White** David Edwards Very nice work

Like · Reply · 7w



**Stuart Wood** Look at CCFL transformers and drive circuit. You should be able to get 3kv easily. This level does not need excessive voltage multiples 2 at the most.

Like · Reply · 7w



**Ray Ridley** That is a lot of stages. I am with **Stuart Wood** - 2 multipliers is probably enough. The secret is to stay away from corona voltages inside the transformer.

let me ask this, for another project I am peripherally involved in: How would you propose to get 6 kV and 300 W? Line voltage input.

Like · Reply · 7w



**George William Tyler** AC or DC? what;s the application?

Like · Reply · 7w



**Colorado Mike Doherty** Ray Ridley 60 Hz xfmr??

Like · Reply · 7w



**Clive Harvey** Ray Ridley so what parameters create conrona? I assume it's a combination of voltage and frequency, is there a way of calculating a threshold?

Like · Reply · 7w



**Andrew Ferencz** flyback, stacked windings. I designed a very tiny cap charger using stacked windings (which charged 4 caps in series, that is enough to know the application). At 300W you could go discontinous too .. maybe even the 2 transistor flyback discussed earlier. I try to keep the voltage across a winding <1500 peak unless you want to get into more complicated winding methods. key is obviously the start/stop of the winding shall not become too friendly.

Like · Reply · 7w



Write a reply...



**Stuart Wood** I did a 1.6KV system at 1.4 KW, by using 4, 400V 1:1 transformers in a parallel series configuration. Driven by a full bridge. I would not recommend it. I would start with a full bridge driving a 1:2 or 1:3 transformer with a voltage double on the output. Assuming PFC front end at 400V

Like · Reply · 7w



**Andrew Ferencz** that many stages can get you to 20kv or more.

Like · Reply · 7w



you like ) series 600V u-fast Si, or 1200V SiC to handle the PIV. 1200V SiC on the mains side, with ~ 300V of flyback volts ... DCM - QR.

Like · Reply · 7w · Edited



**David Edwards** 🇺🇸 Of course the designer can trade off transformer voltage versus number of multiplier stages. I chose to keep the peak transformer voltage under 400 volts so that corona absolutely is not an issue and the capacitors and diodes cost pennies.

Like · Reply · 7w



**Col Johns** Inherent dead time flux balancing? is this because the ON time is a bit less than the worse case resonant half period ... ?

Like · Reply · 7w



**David Edwards** 🇺🇸 Yes, exactly. And the waveform with soft edges is much kinder to the multiplier.

High voltage diodes are often internally stacked low voltage parts and high voltage surface mount capacitors often have inadequate terminal spacing so using more low voltage parts might be a lower cost solution.

Like · Reply · 7w



**George William Tyler** Is it really soft switching? I think a current fed, tuned load Royer would be better? That can be really self oscillating, and also, as some have said, less stages. sine Wave drive of multiplier. also, Taper multiplier capacitor values, lower further away from the transformer.

Like · Reply · 7w



**David Edwards** 🇺🇸 Yes, it self commutates due to the energy stored in the required gap in the transformer core. Also, all the parts except the buck IC are very low cost and even that could be replaced with jelly bean parts. Probably the increased volume from keeping all the multiplier capacitors the same value results in a lower cost.

Like · Reply · 7w



Write a reply...



**Seppo Turunen** I wonder if a more optimal design would be obtained by making the capacitors of the lowermost stages larger than those at the top. If the capacitors are equal, the voltage swing towards the top becomes quite small when the stack is loaded.

Like · Reply · 7w



**Nathan Ellis** [Seppo Turunen](#) you're correct 😊 but there's caveats.

Like · Reply · 7w



**Colorado Mike Doherty** That's a lot of stages for 2kV, how about more secondary turns instead?

Like · Reply · 7w



**Ray Ridley** 🇺🇸 So this is a push-pull driving the multiplier.

What other topologies might you choose?

Like · Reply · 7w

⤴ Hide 16 Replies



than 1kV? can't remember), I used a single transistor-transformer oscillator. The small transformer (my custom design) had a single output winding. There was output feedback to a small series pass transistor with a zener reference. All very low cost.

The capacitor-diode multiplier design I posted was just a suggestion since [Clive Harvey](#) mentioned he might go there. I created it to be safe and usable without PCB coating, but one could easily increase the number of turns on the output winding to decrease the number of multiplier stages. Trivial to do, but the suggested design might be lower cost because it uses all identical low cost jelly bean parts.

Clive Harvey never mentioned what his output regulation and ripple requirements are. He only mentioned in passing that small size is critical. I think he should use a center gapped flyback transformer core wide enough to lay a 43 AWG output winding in a single layer (with edge margins) after filling the bobbin half or more full with tape to get the winding far away from the gap.

The last winding should either be the primary or a full width shield tape winding (don't short the ends) grounded from the winding's center. Leakage inductance will be high, but Clive Harvey doesn't care about loss, so snubbers and heat-sinking will be necessary.

Transformer size will be dictated by the single layer output windings, so if too big he could shrink the core by adding a single multiplier stage to each of the outputs. Output frequency should be as low as the core allows.

[Like](#) · [Reply](#) · 7w · Edited



**Clive Harvey** [David Edwards](#) we will be conformity coating and possibly potting the whole board.

We would prefer to avoid a heatsink, I'm hoping the track copper will be enough.

Your approach too the gap is interesting, if I understand correctly, you space it with a piece of 43awg wire and then file down the ends and remote the wire?

The outer foil ground layer, is this for emi? Or does it effect corona?

[Like](#) · [Reply](#) · 7w



**David Edwards** [Clive Harvey](#), the shield is for EMI because the output windings will potentially produce high dv/dt. Winding edge margins within the bobbin are typically filled with narrow insulating tape in order to keep the build flat.

[Like](#) · [Reply](#) · 7w



**Ray Ridley** I can't say I follow that gapping technique.

Gapping is really a trivial thing to do. Not sure why people think this is hard.

[Like](#) · [Reply](#) · 7w



**George William Tyler** This project is not hard to do, topology can make all the difference, 2kv is actually not very high.

[Like](#) · [Reply](#) · 7w



With my primary inductance only being 1uH I only have a single primary wind, using 17AWG, that does make the secondary winding rather bumpy lol

Though I'm concerned if I use too much kapton tape I'll reduce coupling.

[Ray Ridley](#) I'll be interested too see something on proper gapping techniques and also how to choose how much?

I have some very thin strip guide I can use to measure the thickness.

[Like](#) · [Reply](#) · 7w



[David Edwards](#) · [Ray Ridley](#), perhaps my description wasn't clear. The core will have only a center gap. The first layer tape filler (half or more of the window height) is to space the windings away from the gap's fringing field. The primary winding construction could be the bread in a sandwich around the output windings (two primaries in parallel to minimize proximity effects). Three or more layers of tape will be required between it and the secondaries.

[Clive Harvey](#) needs to bite the bullet and specify a custom transformer - in detail.

[Like](#) · [Reply](#) · 7w · Edited



[Clive Harvey](#) · [David Edwards](#) the transformer I'm looking at now is solely for prototyping, I have already advised my client we will need a custom transformer designed and made, anything even close to production quality isn't realistic for me at this point.

[Like](#) · [Reply](#) · 7w



[David Edwards](#) · [Clive Harvey](#), you could easily wind your prototype transformers by hand. That's what I always do whenever possible.

[Like](#) · [Reply](#) · 7w



[David Edwards](#) · [George William Tyler](#), please fill in your suggestions with the the topology and transformer winding details. Maybe post a jpg of the schematic (otherwise no one can really know what you are suggesting).

[Like](#) · [Reply](#) · 7w · Edited



[Clive Harvey](#) · [David Edwards](#) they are looking at a winding machine as it's a high tunes ratio, they would spend more time in winding that the cost of a machine many times over after a few transformers.

[Like](#) · [Reply](#) · 7w



[David Edwards](#) A simple, low cost winding machine would be reasonable (or get a colleague to hold a geared, low speed drill). How many prototypes are you anticipating needing?

[Like](#) · [Reply](#) · 7w · Edited



[Stuart Wood](#) This could also be a current fed push pull design. Royer oscillator or similar.

[Like](#) · [Reply](#) · 7w



I suspect there will be 10's made, and for initial example builds.

There is also expectations for upscaling to higher voltages and powers.

The intention being to create a robust PSU board, with interchangeable magnetics.

So over spec'd fet is likely.

Plus there will be some experimentation to get the optimal solution.

Various turns ratio's, primary inductance,

See what we get in reality and the trade offs.

Like · Reply · 7w



**George William Tyler** [David Edwards](#) did you see my comment with a link to the unitrode chip? That is the general idea. If you like I will do a schematic with a simulation so you can see the wave forms?

Like · Reply · 7w



**Joel Holland** [Stuart Wood](#) [David Edwards](#) about the current-fed design. What benefits does it have over the voltage-fed design? I have been thinking about using something similar in my project - I seen this post and have returned to it. Why does your converter not have an output inductor? It is to my knowledge that for a voltage-fed push pull, you require an output inductor. With a current fed one, no output inductor is needed and instead an overlap between the main switch duty cycles is needed. Can you help me understand how you can operate this w/out the output inductor?

Like · Reply · 6d



Write a reply...



**George William Tyler** <http://www.ti.com/lit/ds/symlink/uc3872.pdf>

Like · Reply · 7w



**Clive Harvey** [George William Tyler](#) what do you see as the advantages of using this controller?

Like · Reply · 7w



**George William Tyler** Over the same topology with self oscillating? there is not actually much, it just simplifies drive and has a built in buck to control current. it's neat... It is mainly the topology that makes the difference, posted that and was about to follow it up. see that below, I put it as a new comment by mistake. the topology has many advantages, not sensitive to leakage inductance, no high Dv/Dt, low losses, low component stress etc, all the normal resonant advantages. High voltage rectifiers may be an issue, but with sine wave voltage you can series them. I used 12kv, not very fast. I would have to dig to get the part number but they were easy to get in quantity. We used about 20kHz

Like · Reply · 7w · Edited



**George William Tyler** If you use this leakage inductance is no problem, you can use a UI or small line output transformer core. Custom secondary bobbin with multiple chambers on 1 leg, primary on the other. output rectifier is a voltage doubler, not a multi stage multiplier. for 2kV, use possibly 4 chambers for bobbin, pile wind secondary. I had a company manufacturing neon sign transformers up to 12kV, for that we used 6 chambers. Had no problems with that, manufacturing killed the business... supplier supplied wrong semis and we did not pick it up until they were mounted outside on tall buildings. Customers did not like having to climb 10 store buildings to change them when they died 6 months after installation! We used a BU208D line output transistor in that one, had a collector emitter diode but they supplied BU208 without the diode...

Like · Reply · 7w



**Clive Harvey** 🗨️ [George William Tyler](#) when you say chamber, do you mean a sectioned bobbin?

Oww that's a really horrible way to go, I hope you managed to sue the supplier,

[Like](#) · [Reply](#) · 7w



**George William Tyler** [Clive Harvey](#) yes, we had them made by a retired guy with a lathe, He made a tool to cut all the chambers at one time. then cut a slot across them at an angle for wire to cross to the next chamber. We tried various plastics, Acetyl was the best but was expensive. These days a CNC machine would do it of course.

[Like](#) · [Reply](#) · 7w



**Clive Harvey** 🗨️ [George William Tyler](#) yer Ive worked with acetyl before, great for ESD sensitive stuff, pretty ridged and doesn't come with the issues other materials have with being toxic to machine.

I do hope I don't need to go that route, I can also see that would require multiple layers or a big bobbin, which Would increase capacitance.

Might be an option though. I have seen some sectioned bobbins available off the shelf and I assume a custom supply will be able to do it.

Good thing is, once we have all this sorted, the volumes are quite high.

[Like](#) · [Reply](#) · 7w



**George William Tyler** There were some commercial ones I tried, but our own ones were better, it is easy to wind and fast. No layering, just pile wound. Capacitance is not an issue, there is some in each section bit between sections it's low, and also to anything else.

[Like](#) · [Reply](#) · 7w



**George William Tyler** [Clive Harvey](#) there are some commercial ones we tried



[Like](#) · [Reply](#) · 7w



**Clive Harvey** 🗨️ [George William Tyler](#) what kind of core did you use with those?

So what are the drawback with winding short tall layers along the core, rather than long flat layers?

I'm guessing there's a lot more leakage inductance?

[Like](#) · [Reply](#) · 7w



**George William Tyler** leakage does not matter too much, it's part on the resonant circuit. the voltage across the winding is a sine wave, little in the way of higher harmonics. the narrow windings mean less voltage between layers, and also end to end. have you see line output transformer cores?

[Like](#) · [Reply](#) · 7w · Edited



**George William Tyler** [Clive Harvey](#) look for cores for line output transformers, I. e. Fot crt displays, TVs

[Like](#) · [Reply](#) · 7w · Edited



concern for us.

Like · Reply · 7w

**George William Tyler** Clive Harvey it "depends"... that neon sign transformer I made was a resonant flyback with that transformer. do you know what a TV line output stage looks like? I guess it has been years since a CRT TV was made...

Like · Reply · 7w · Edited

**Clive Harvey** George William Tyler no, never really looked. I can't help but feel there's reasons they phased out, but that said, maybe just cause there's not a lot of applications for high voltage low current.

Like · Reply · 7w

**George William Tyler** yes, TV's don't need 29 kV for CRT's anymore as they use LCD displays.

Like · Reply · 7w

Write a reply...

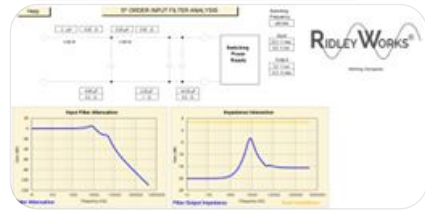
**LA Serantes** New Member · March 29 at 12:55 PM

Hi group!  
 First of all, I would like to thank you all for adding me to this fantastic group about power electronics design.  
 I would like to kindly ask for support with an issue regarding EMI filter... How do you calculate the output and cutoff frequency of a 2-stage LC filter?  
 For a single stage LC filter is:  $Z_{out} = \sqrt{L/C}$  and  $F_{co} = 1/(2 * \pi * \sqrt{LC})$   
 How is with 2-stage or n-stage LC filter...  
 Thanks a lot!  
 Best regards,  
 Luis

Write a comment... 2 11 Comments

Like Comment

**Ray Ridley** Here is the easy way:



Like · Reply · 1w · Edited

**Nicola Rosano** Give a look at the Extra Element theorem.

Like · Reply · 1w

**Ray Ridley** It's a free file we give away, part of what is in RidleyWorks. I will upload it to the group.

Like · Reply · 1w

**Ray Ridley** Here is the file:

Files	
Name	Type
Filter.xls	Spreadsheet

Like · Reply · 1w

Like · Reply · 1w

Col Johns LA Serantes, are you familiar with common mode filtering and differential mode filtering ....?

Like · Reply · 1w

LA Serantes Yes sure. I am looking for DM filtering

Like · Reply · 6d

Ray Ridley Do you want to write equations for the joy of it, or get a job done?

Like · Reply · 6d

LA Serantes I would like to write equations but your excel tool it's fantastic.

Ray Ridley do you make any workshop also in Europe? I've seen that you only plan them in Camarillo, CA...

Like · Reply · 6d

Write a reply...

Michael Green Think about dampening the filter. Note this can change the roll off depending your choice of dampening. A goal of Q < 6 dB is good to start with.

Like · Reply · 6d

Ray Ridley Michael Green I prefer a q of 1. Otherwise the impedance peaks.

Like · Reply · 6d

Write a reply...

Write a comment...

Ray Ridley updated the group cover photo. Admin · March 29 at 5:33 PM



Knowledge is Power

You and 7 others 2 Comments

Like Comment

Rahulnab Das Do you have a whatsapp group to be discussed in power electronics

Like · Reply · 6d

Ray Ridley Rahulnab Das we have this group. What more do you need?

Write a reply... Write a comment...

**Norman Elias** March 22 at 6:03 AM

I don't see much discussion here about component tolerances, worst case analysis, stress analysis and the like. Are these all solved problems or is there some concern about these issues?

You and 6 others 33 Comments

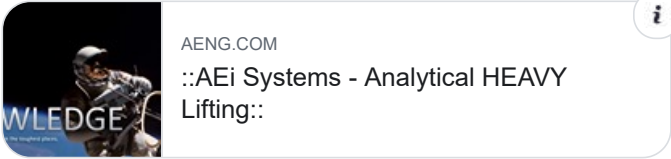
Like Comment

**Arief Noor Rahman** To my understanding...component tolerance normally its not much of an issue, except for resonant converter...  
Stress analysis, we do it all the time for MOSFET current and thermal stress, inductor current stress, caps ripple current stress  
Like · Reply · 2w

**Andrew Ferencz** IPC-9592 is a good source for guidelines, see Appendix A. And a good thermal image helps! Some ratings are not useful like current rating because usually thermal performance will not allow current near ratings. But it is useful for abnormal testing - do you ever exceed the peak rating?  
Like · Reply · 2w

**Norman Elias** Thanks for the reference  
Like · Reply · 2w

**Robert L Rauck** Different categories of products employ different levels of rigor in tolerance and stress analysis. Military and especially Space applications provide the highest levels of scrutiny. AEi Systems is a big organization devoted to WCCA, Parts Stress analysis and related fields. <https://www.aeng.com/>



Like · Reply · 2w

**Norman Elias** Thanks Robert. I know about this outfit. They do a very thorough job.  
Like · Reply · 2w

**Robert L Rauck** That thorough job comes with \$\$\$.  
Like · Reply · 2w

**Darrell Hambley** "solved problems"? No. Each and every design has these issues and good engineers always perform a w.c.a.  
Like · Reply · 2w

**Robert L Rauck** One piece of advice I received many years ago was: "If you don't worst case your circuit, the production line will."  
Like · Reply · 2w

**Alain Laprade** **Robert L Rauck** For those of us old enough to remember, there was an oil commercial in the 70's reminding viewers of the importance of engine oil change. "You can pay me now or you can pay me later. Your choice."  
Like · Reply · 1w

**Robert L Rauck** **Alain Laprade** I remember!



Write a reply...



**Norman Elias** Monte Carlo has played a heavy role in tolerance analysis. Is it used much for anything else or are the sim times just too long?

Like · Reply · 2w



**Cameron Stewart** Power supply design encompasses a wide range of problems. Worst case analysis is just one aspect to power supply design.

Also, during the initial design phase, component derating, calculated MTBF, and loop stability analysis is generally a bigger concern than component tolerancing.

Usually there are only a few places in a circuit where you identify the need for tight tolerance components: Output voltage sensing and oscillator timing circuits are the usual candidates. If you can get transformer and inductor main parameters to hold with-in +/- 10% you are doing pretty good.

I've been through a number of design reviews with the major prime military contractors over the past twenty years. I've never seen one request for Monte Carlo analysis on a power supply design.

If you have the staffing to support Monte Carlo analysis on a power supply development project, it would probably be a task that you would delegate. Usually, the development time, staffing resources, and program priorities are not there to support such an effort.

I'm not saying that Monte Carlo analysis isn't useful. But I have never seen it done over the last 20 years on a power supply project.

Like · Reply · 2w · Edited



**Alain Laprade** Occasionally, I come across automotive customers getting into trouble with loop stability analysis, failing to take into account what happens at temperature extremes with their output capacitors. Particularly at a minimum temperature of -40C. While I'm chiming on that topic, I always wondered why the automotive industry minimum temperature of -40C is used. Many northern regions have situations with cold start below -40C. I will always recall starting up my 1984 Ford Escort at -47C (Chicoutimi, Quebec) one winter. Sounded really rough at startup but it started. I don't hear complaints about this (block heaters CERTAINLY recommended).

Like · Reply · 1w



**Cameron Stewart** Alain Laprade

Organic polymer aluminum capacitors are one way to handle the low temperature problem.

Like · Reply · 1w



**Alain Laprade** Cameron Stewart Agreed. (I should mention my point is in regards to automotive 12 V battery systems). But time after time I have to convince designers they are worth the added individual component cost.

Like · Reply · 1w



Write a reply...



**Norman Elias** I'm guessing that it's probably not worth the effort. I'd love to hear any views to the contrary but your comment supports this hypothesis. One major obstacle would be the availability of accurate statistics on all the components. Datasheets specify min and max values but, with good reason, no data about statistical distributions. On the other side of the picture, there's not much sense in terms of time, effort, and cost, for a product manufacturer to collect statistical data on the parts they purchase. As I say, I'd love to hear any opinions to the contrary.

Like · Reply · 2w

environment where the above concerns were absent, at least to a degree. Does anyone want to guess what I'm thinking of?

Hint; It requires a free exchange of data among all parties, manufacturer(s) of components and of systems. It also requires the ability to recover the costs from the end customer.

Like · Reply · 2w

**Michael Delany Norman Elias** I've heard TI mention in an online training that typical values are statistically within one standard deviation and I believe outside 3 standard deviations is thrown out. I don't know exactly what all goes into this, but that is what was claimed.

Like · Reply · 6d

**Norman Elias** It depends on whether they're talking about variations within an individual chip, chip-to-chip on the same wafer, wafer-to-wafer in the same lot, or lot-to-lot. I doubt that they can guarantee 1 sigma from lot-to-lot unless they're talking about ratios that are maintained.

Like · Reply · 6d

Write a reply... [emojis]

**Kevin Azul**



Like · Reply · 2w

**Cameron Stewart** Before about 1980, it was quite common to find adjustable pots, adjustable trimmer capacitors, and slug tuned transformer/inductors on all types of electronics.

But since that time - partly due to changes in circuit design approaches, partly due to increasingly tight tolerances on components, and partly due to new technologies - the need for adjustable controls to make circuits work has fallen largely by the wayside.

It's rare to see a power supply drop out of final test due to component tolerancing issues. If there is fallout during subassembly testing, it's a known issue that is covered by select-in-test resistors as part of initial bringup.

I used to design with manganin shunt wires for secondary current limiting. The manganin shunt wires were difficult to install with better than 10% resistance repeatability.

Now I can get precision surface mount shunt resistors that do the same thing, eliminating the need for trimming current limit circuits.

In the high reliability world, nobody want's adjust pots anymore because of the negative impact they have on calculated MTBF. And installing select-in-test resistors in circuits is highly labor intensive.

I don't see any adjust pots on my smartphone either, even if I pop the cover. Nor on a flatscreen TV.

It's relatively easy now to get resistors with 0.1% tolerance, capacitors with 1% tolerance, voltage references with 0.5% tolerance, and opamps with input offset voltages of less than 1mV.

If you are doing digital control, you can perform A/D and D/A conversion with high precision, then adjust parameters in the digital domain.

The precision and repeatability of electronic components often well exceeds what is needed in most applications.

Like · Reply · 2w · Edited



Stress analysis is important to assure the desired reliability.

Tolerance analysis is needed to assure a very high yield in manufacturing test. Your converter has to work first time, every time. While six sigma analysis does not work well with electronic components (see my papers from almost 30 years ago) you still need to make sure that the specification is going to be met by every unit that goes down the production line. You cannot afford to have a 1% failure rate at final test. That high a failure would eat the profit from the entire production run.

Like · Reply · 2w



**Norman Elias** OK **Bob White**. Are you suggesting that there may be a role for Monte Carlo analysis or do you handle tolerance issues with WCA?

Like · Reply · 2w



**Bob White** There can be a role for Monte Carlo analysis. One issue is that we do not know the distribution of values for components. Guassian with mean at the specified nominal? Maybe? If so, what is the standard deviation?

Back in the day 1% resistors had a notable gap in values near the nominal because manufacturers were picking parts to sell as 0.1% tolerance parts. Today, as best I can tell, it is less of an issue.

I have my own method for doing Monte Carlo for commercial components that has given good results in a high volume production environment. However, I consider that method one of my trade secrets and am not willing to share it.

Like · Reply · 2w · Edited



**Norman Elias** Actually, now that you mention it, I can think of a way to do a Monte Carlo analysis without knowing the actual component distributions and still be able to derive useful results. In fact, if I were to do a yield analysis today, I wouldn't want to use a normal distribution - too many samples would hover close to nominal where I know my design is good.

I'd love to try it out for a paying customer but I'm not at all sure that anyone out there is looking for that kind of help. That discussion would belong in a PM, not here.

Like · Reply · 2w



**Cameron Stewart** The production quantities involved have a bearing on this.

If you are doing space qualified hardware and only building one ground unit and one flight unit, Monte Carlo analysis isn't useful.

If you are building 10,000 pieces a month of something, statistical spread of parameters becomes important.

Like · Reply · 1w



**Darrell Hambley** **Cameron Stewart** "only building one ground unit and one flight unit" Boy, when I was working on space projects I never got that logic understood by the prime contractors.

Like · Reply · 1w



Write a reply...



**Scott Styles** **Norman Elias**, you're my new BFF. Working in NPI I can say that no design people ever pay enough attention to this.

Like · Reply · 1w



**Ray Ridley** 🗑️ It's not an exciting topic. You won't see papers on it. Like most of us, I really hate that part of the work. 🤔

Like · Reply · 1w

gets handled in a much more awkward and reactive manner downstream in production test...

Like · Reply · 1w

**Col Johns** It generally requires an experienced engineer and a good grad student to look at the parts which cause the greatest change in converter operation - and - usually in a spread sheet - set out worst case output with specific changes in defined ( or all ) parts ...

Like · Reply · 1w

**Norman Elias** Thanks to all for a lively informative discussion.

Like · Reply · 1w

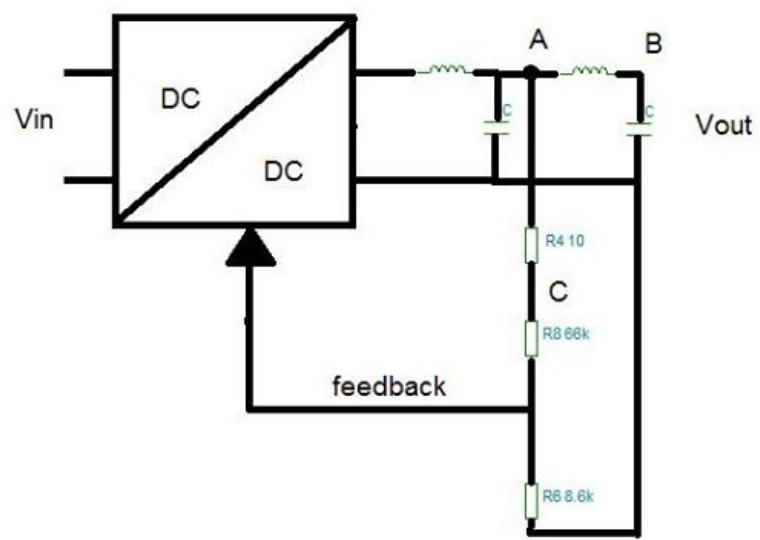
**Bill Stutz** Most Military and Satellite contracts mandate that sort of analysis. In fact most Power Supplies for those applications have lots of specific numbers they have to meet. Usually the analysis has to be part of the PDR package.

Like · Reply · 1w



Write a comment... **Fkhn Ma** March 28 at 11:36 AM

Hi all,  
I am studying the feedback loop in dc/dc converter and have been faced with this question.  
Assume, we have a dc/dc and a two stage LC filter in the output.  
If we put the feedback loop after the first LC filter:  
1.what are the criteria for the feedback to have a stable converter(I know second LC filter changes the bode plot)?  
2: To measure stability and use bode 100, the injection voltage should be applied between point A-C or B-C?(As feedback loop is in point A but the output voltage is in point B)  
thank you in advance



7 27 Comments

Like Comment

**Ray Ridley** It's been studied to death 30 years ago. Results are here:  
<http://ridleyengineering.com/.../1%20second%20stage...>



[Like](#) · [Reply](#) · 1w · Edited

**Prannoy Achuthan Pakideeri Ray Ridley**

[Like](#) · [Reply](#) · 1w



**Ray Ridley** More information here:

<http://ridleyengineering.com/.../86-052-designing-a-two...>

[Like](#) · [Reply](#) · 1w · Edited



**Fkhm Ma** Thank you for your link. Actually, i have already read this article, but I could not link this one to my question. you put the feedback loop after the second stage filter, while in this one, this is between first and second filter.

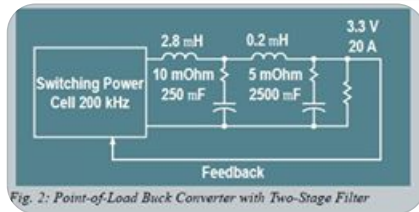


Fig. 2: Point-of-Load Buck Converter with Two-Stage Filter

[Like](#) · [Reply](#) · 1w



**Ray Ridley** It is after the filter. That is the point of the articles, how to design it so the loop can go around it.

[Like](#) · [Reply](#) · 1w



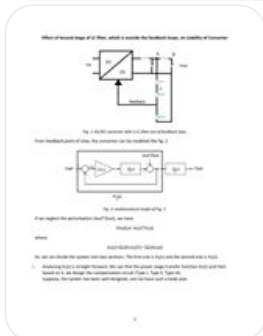
**Alain Laprade** Fkhm, (1) regarding your question, measuring the feedback loop doesn't depart from standard practice. Measurement points A & C are your targets. Measurement B brings nothing to the feedback loop information. CAUTION, having said this, if you do a computer simulation, you MUST include that 2nd stage LC filter as you no longer have a resistive load. It is now a complex impedance load that can influence measurements. (2) Watch out for min/max load regulation. That inductor has ESR, VOUT will vary. (3) To Ray Ridley's point, with some effort, there are better ways of setting up the feedback loop when designing a 2-stage LC filter. It works, but you'll need to do the math. Ray's articles are an excellent source of information to establish base design guidelines. If item (2) above poses an issue, follow Ray's advice.

[Like](#) · [Reply](#) · 1w



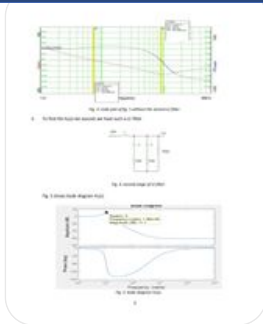
**Fkhm Ma** Thank you [Alain Laprade](#) [Ray Ridley](#)

I agree with point 1. I saw somebody used the point C to measure stability and it made me confused. for the stability I wrote and analyzed it. please check it out and say your opinion



[Like](#) · [Reply](#) · 1w

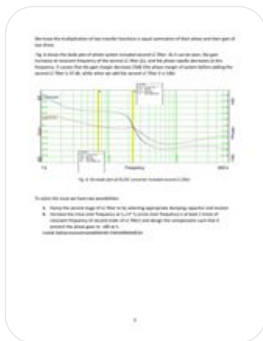




Like · Reply · 1w



Fkhm Ma



Like · Reply · 1w



Fkhm Ma I am still looking for a way to improve gain margin of the converter when we use a LC filter out of the feedback loop.

Like · Reply · 1w



Ray Ridley damp the filter better. Move its frequency out higher, or crossover at a lower frequency.

Like · Reply · 1w



Ray Ridley I don't like the way your plot rises at the end there.

I think that is a test setup issue. Looks like a Venable?

Like · Reply · 1w



Fkhm Ma yes, it is venable

Like · Reply · 1w



Ray Ridley Fkhm Ma try to figure out why the gain is rising.

Like · Reply · 1w



Write a reply...



Venkat Karthik Choose 2nd stage LC corner frequency atleast 5 times the cross over frequency and you are done. The loop gain and phase is measured across A and C

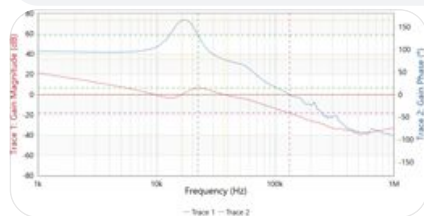
Like · Reply · 1w · Edited



Fkhm Ma I moved the cross over frequency( $f_{co}=30\text{KHz}$ ) 2 times of resonant frequency( $f_0=16\text{KHz}$ ).

what do you think about it?

why phase increase in resonant frequency?



Like · Reply · 1w · Edited




Like · Reply · 1w



**Fkhm Ma** which part of the measurements is not fine?

Like · Reply · 1w



**Ray Ridley**  **Fkhm Ma** beyond 50 kHz. The Venable doesn't have good controls for setting levels, so they are not set right. the LF doesn't make sense to me either.

This is the kind of problem we get into detail with customers when they are using the AP300 or RidleyBox.

Is Venable supporting you with these questions?

Like · Reply · 1w



Write a reply...



**Runo Nielsen** The open- and closed loop gain depends on the load impedance. Adding an LC filter after the feedback point changes the gain  $H3(s)$  because your load is no longer just a resistor, it is a resonant circuit. If you include that change in  $H3(s)$  it is correct that  $Vout(s) = H3(s) * H2(s)$ , but the filter complicates the math. For more inspiration, see <http://www.runonielsen.dk/Feedback.pdf>

Like · Reply · 1w



**Ardy Cristobal** In my experience, for better Bode Plot response, Point B should be the feedback point of the loop. Impedance of the second LC filter also affects the loop and should be part of the compensation network. In this case, 1st LC and 2nd LC filter should be considered in your calculation for selection of components for compensation.

Like · Reply · 1w



**Fkhm Ma** **Ardy Cristobal** if we put the prob in point B, we are injecting voltage across L and 10 ohm instead of only 10 ohm. I sit fine?

Like · Reply · 1w



**Alain Laprade** **Fkhm Ma** No. Don't do that. What Ardy and many of us have been saying is to abandon point A, connect the 10 Ohm injection resistor to point B. Follow Ray Ridley's articles as a start. They work.

Like · Reply · 1w



**Fkhm Ma** **Alain Laprade** Thank you for your comment.

I totally agree with you and the others to put the feedback point after second stage of filter, like the work done by Ray Ridley's in his articles. (because in this case, the output is not regulated and highly depend on the output current and ESR of inductor)

The problem is that they designed in this way and now they have the problem, and in this case, it is impossible to change the circuit.

I have seen this issue interesting, and wanted to see it is possible to find a solution with only changing the circuit's components.

Like · Reply · 1w · Edited

designing an automotive battery connected boost converter with an IC I had responsibility. They insisted on using a using an inductor that was 'preferred'. I wasted a LOT of time advising them to think differently, that their design would not be stable (could not be compensated). I showed them the math and the simulations. Shared my expertise with the part extensively. Well, they 'knew better' and went ahead, deciding I didn't know my shit and would fix it themselves. Sometime later, they got in real trouble and contacted me again for support. They made painful (i.e. they had started prototypes and were now late in the game) BOM change and had to explain themselves to their own end customer (in the automotive world, doing this is not a trivial activity).

Like · Reply · 1w

Write a reply...

**Mohamed Orabi** You can check this article also M. Orabi , "Stability Analysis of Power Supplies Required for Remote Sensing Applications ",INTELEC Korea October .

Like · Reply · 1w

**Ray Ridley** Please try to post readable references that people can get for free, saves everyone duplicating work.

Like · Reply · 6d

Write a comment...

**Pranit Pawar** March 27 at 9:29 PM

VDS Overshoot Calculation

I'm trying out figure out a ball park range of power loop inductance in half-bridge circuit. I'm doing this to get the maximum value of loop inductance my power loop can have such that the VDS overshoot stays below a desired value

I know of one formula -> VDS-overshoot = L \* di/dt

(L = power loop inductance)

I calculated a theoretical value of loop inductance for my application, and the power loop inductance seems to be high.

di=10A, dt=10ns (lowest fall time for my GaN s/w)

allowed overshoot=80V

=> 80 = L \*(10A/10ns)

=> L = 80nH

80nH seems a very high value. Nevertheless, is my loop inductance calculation complete? Have I missed out other factors to consider for overshoot calculation?

2 37 Comments

Like Comment

**David Edwards** The rule of thumb for open loops is 8nH per cm. Traces over ground planes or return paths will be lower in inductance.

Like · Reply · 1w · Edited



present me their work with spike voltage this high...

1. there is no way your estimate of L can be accurate...
2. your di/dt estimate also difficult to justify,
3. besides, you didnt show your layout, there are many layout tricks that can be employed to reduce board parasitic inductance....its all about layout when you are want to minimize board parasitic

Like · Reply · 1w



**Pranit Pawar** What is the theoretical way of estimating overshoot?

Like · Reply · 1w



**Pranit Pawar** di/dt is the rate of current rise/fall 10-90% and vice-versa in each switch

Like · Reply · 1w · Edited



**Arief Noor Rahman**  $V=Ldi/dt$  is the right way...

but, you should show your layout, and present the underlying theory that you use to get 80nH, you should show it, to get a meaningful discussion...otherwise its just chitchat war...

I know what is di/dt, I have developed a few converter with GaN in the past, and I have also developed GaNFET dRdson characterization...

Like · Reply · 1w



**Pranit Pawar** **Arief Noor Rahman** I haven't made the layout yet because I'm trying to get a range of loop inductance first and then choose the best switch (cost/performance), tweak the layout etc. Layout isn't an issue.

Like · Reply · 1w



**Pranit Pawar** **Arief Noor Rahman** The theoretical way 80nH estimate is the  $V=L*di/dt$  formula. This is the max allowable loop inductance. I'll develop the layout accordingly. What I'm asking is have I missed any other factor for inductance calculation?

Like · Reply · 1w



**Arief Noor Rahman** okay...no need to discuss then...its useless...

my suggestion to you is:

i know it maybe scary to make mistake and blowing your circuit will also cost you money...but, you need to make mistake to learn...I was in the same phase, but just thinking will take you nowhere

Like · Reply · 1w



**Arief Noor Rahman** no need to think too much, learn layout example from EPC, GaNSystem, Transphorm, Cree, Rohm, Infineon, Toshiba, Onsemi, STmicro.....

try to understand the common pattern among those layout, and build your own...

Like · Reply · 1w



**Pranit Pawar** **Arief Noor Rahman** I get your point. I'm not arguing Arief. How do you estimate an allowable range of loop inductance your design should have?

Like · Reply · 1w



**Arief Noor Rahman** for GaN <5nH, for SiC <10nH

Like · Reply · 1w · Edited



there has to be some design insight, some boundaries to work within. EPC, GaN systems everyone has a layout practices paper. I've gone through a lot of them to understand the layout recommendations. But that still leaves my question unanswered

Like · Reply · 1w



Write a reply...



**Kadir Yilmaz** You have very bad layout if you have 8cm long power trace

Like · Reply · 1w



**Kadir Yilmaz** Beside 10ns spike will be important for EMI but not important for power circuitry itself

Like · Reply · 1w



**Kadir Yilmaz** Anyway go back to your dwg board

Like · Reply · 1w



**Bob White** Over shoot voltage is not  $L \cdot di/dt$ . It more like  $I_{pk} \cdot \sqrt{L/C}$  where  $\sqrt{L/C}$  is the characteristic impedance of the resonant tank formed by the leakage inductance and the circuit capacitance (mainly the  $C_{oss}$  of the transistors. This complicated by the fact that  $C_{oss}$  is highly nonlinear with voltage so calculations based on a linear capacitance are a rough approximation at best.

Like · Reply · 1w



**Pranit Pawar** Thank you [Bob White](#). Can you share the source of this? Maybe I can get a worst case estimate from this

Like · Reply · 1w



**Bob White** Energy balance.  $(1/2) \cdot L \cdot I_{pk}^2 = (1/2) \cdot C \cdot V_{pk}^2$ . This assumes that all of the energy stored in the inductance ends up stored in the capacitance. This is very basic circuit theory.

Like · Reply · 1w



**Bob White** [Pranit Pawar](#) Also, consider the following circuit problem. You have a dc voltage source. The positive terminal of the dc source is connected to an inductor. The other other terminal of the inductor is connected to a capacitor. The other terminal of the capacitor is connected to the negative terminal of the source. That is, the voltage source, inductor, and capacitor are in series.

At time  $t = 0$  there is no current in the inductor and no voltage on the capacitor.

What will be the maximum voltage on the capacitor at some time later than  $t = 0$ ?

Like · Reply · 1w



**Ray Ridley** 🚫 Capacitors are nonlinear. Don't forget that.

Like · Reply · 1w



**Bob White** [Ray Ridley](#) I made that point in my first response....

Like · Reply · 1w



Write a reply...



What if the device of yours turns off faster. What if there is a OVC event and protection is kicked in. In desat topology current is rather not limited to a nominal value. Just another exercise in math. DC bus has to be as good as practical and there is reason for soft switching of IGBT when overloaded. I doubt that will help with the device, which speed is limited by the package inductance and actual conducting layer is few nm thick. If you apply field it's instantly ON. However this will always keep GaN manufacturers happy.

Like · Reply · 1w · Edited

**Pranit Pawar** Hi Alex Berestov!. The 80nH will tell me how much maximum power loop inductance I can allow in my layout. So depending on the inductance figure, if it is high, I can opt for a cheaper leaded package, make a more "relaxed" layout, get the board done quickly. However if inductance threshold is lower, I'll opt for an expensive smaller package, opt for a 4-layer design, make a compact meticulous design. I'm taking the trouble of extra estimations because I've a tight overshoot and limited turn-around time. Like I told Arief, I can make a board right now and keep on rolling out iterations v1,v2,v3 till the desired overshoot is achieved. But that's expensive for me right now in terms of money and time. Feel free to correct me

Like · Reply · 1w · Edited

**Pranit Pawar** For slow turn on/off, there are resistors to control the slew rates. For OVC, there is soft turn-off

Like · Reply · 1w

**Yuri de Klerk** If you're doing GaN Mosfet's I can not think of a reason to not make the best layout you are able to. In 2016 I made my first SiC design but first proto with 2 layer pcb. Spikes quite high. Second proto with 4 layer and really optimized. Spikes much lower and efficiency 2% higher. You're on the right way with thinking: go for the best layout you can do!

Like · Reply · 1w

**Alex Berestov** What's the point of typing something if one reads the reply not? One can not be taught as the horse brought to the well could not be made to drink, but some can learn. So check ref designs and physics of HEMT before asking whether or not the calculations are relevant and/or correct. Good luck with gate resistor controlled dU.dt in GaN transistor along with desat protection and soft turn-off. P.S. In regard to bus inductance:Quote "in the range of 0.4 nH to 2.0 nH is desirable." end quote

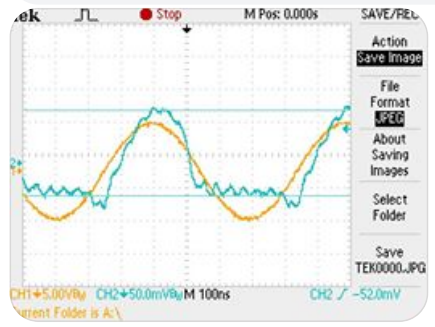
Like · Reply · 1w · Edited

**Pranit Pawar** Thanks Alex!

Like · Reply · 1w

Write a reply... [emojis]

**Alex Berestov** Just for instance. This is actual inverter, switch and load currents. Bus is excited at transitions @ f=24MHz. Assuming local Cbus of 0.2 uF one can estimate bus inductance. Sensors are 10mV/A.



**Ray Ridley** is this a theoretical exercise, or you are looking at hardware?

Like · Reply · 1w

**Pranit Pawar** theoretical exercise first and then will move to hardware. Or you can say its a theoretical exercise for the hardware

Like · Reply · 1w · Edited

**Ray Ridley** You can't really do any calculations in the absence of a board layout plan with all components defined. Otherwise it is just arbitrary numbers and a waste of time and energy.

Like · Reply · 1w

**Pranit Pawar** **Ray Ridley** I'm trying to find the maximum permissible loop inductance (Lp) for a given voltage overshoot threshold. Then, I'll select my components, pcb layers reqd and make the layout such that the loop inductance of the layout stays below Lp. Am I doing a mistake in this approach?

Like · Reply · 1w

Write a reply...

**Alex Berestov** Are you reading what's posted at all? 2nH is absolute max for GaN. Power Electronics Magazine if memory serves me right. Did you check what is HEMT you are about to control before trying to figure out the worst but still working piece of hardware?

Like · Reply · 1w

**Pranit Pawar** I read that but what is the basis of that 2nH? isn't the inductance limit dependent on current slew rate, max operating voltage?

I have a choice to make between leaded package (~1nH inductance) and non-leaded (~100pH inductance). Cost difference is significant, layout efforts increase too. Are you reading what I'm posting about time and money limits? Leaded are available locally, non-leaded have to be procured internationally. There are thermals to be considered too. I'm posting replies lucidly yet I get some out-of-nowhere figures and 'dont-do-that' answers. I'm asking for a reason and a basis of the same.

Like · Reply · 1w · Edited

**Alex Berestov** Design examples are widely published. Look what others are done and see if you can reproduce one money and technology wise. Less than 1 nH is not that hard to make. Check stripline or busbar impedance calculators on the web.

<https://ieeexplore.ieee.org/document/817259>

IEEEEXPLORE.IEEE.ORG  
A plane busbar impedance calculation using Maxwell's...

Like · Reply · 1w

Write a reply...

**Ray Ridley** Suggest you choose a device, layout the board and try it asap. Don't obsess about overanalysis. You will repeat the board regardless.

Like · Reply · 1w · Edited 1

Write a comment...

# OHM CONFINEMENT WEEK 3

HOW IS THE POWER SUPPLY COMING ALONG?



©2020 RIDLEY ENGINEERING INC.



GREAT! ENGINEERING JUST DELIVERED THE FIRST UNIT...

... IT'S WAY AHEAD OF THE LAST PROJECT



AS 2019

You, Norman Elias and 27 others

Like

Comment

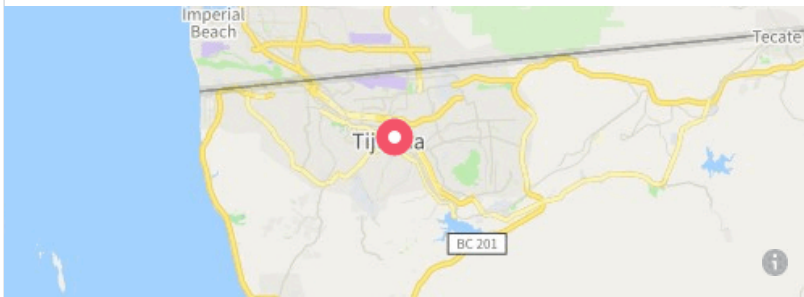
Write a comment...



**Ardy Cristobal** is looking for recommendations.

March 27 at 6:16 AM

Can anyone recommend a transformer supplier experienced in ferroresonant transformer. I am designing a HV generator based from a AC Mains of 220Vac / 50-60Hz with Secondary output of 1KVac. I am using a Voltage Doubler with operating current between 5mA to 50mA. Hoping for your recommendations.



## Looking for Recommendations

1 person recommended 1 place



Terra, Nicole and 212 other friends have asked for recommendations. You can too.

Try It

13 Comments

Like

Comment



**Walter Anton**



Like · Reply · 1w





difficult art form.

In general, ferros do not like nonlinear loads at all. Be careful with that.

All that said, ferros are the most amazing devices in our field. How else could you get an ac regulated output with zero electronics? Their study should be mandatory for all grad students in order to develop nonlinear thinking skills.

Of course I only say that because my first ever power electronics project was a 20 kHz ferro. I will never forget that year in the lab learning things that I still teach from today.

Like · Reply · 1w



**Brian Faley** The chief engineer (David Z) at Pacific Transformer in Anaheim, CA has been doing Ferro's for a long time, in fact his doctoral thesis pertains to them. [pactran.com](http://pactran.com) Properly designed they are stable from no load to short circuit foldback, it is all about how much energy is circulating in the resonant tank. Most common telcom application used to be rectifiers for charging central office batteries.

Like · Reply · 1w · Edited



**Ray Ridley** Ferros give unbelievable noise isolation from input to output. Downside is that they weigh about 2x the equivalent isolation-only transformer.

I have a real love-hate relationship with these things. After slogging through a dozen Russian nonlinear math papers on the things, I finally wrote my first circuit simulator on a TI calculator back in 1981. That was really the start of RidleyWorks!

And no, I don't want to help anyone design one of these things though I will happily watch from the sidelines.

Like · Reply · 1w



**Ray Ridley** The ferroresonant "jump" is an engineering marvel to behold. Does anyone know what I am referring to? (without googling it.)

Like · Reply · 1w



**Colin Tuck** No, please illuminate ( and I thought I knew most things about F.R.T's )

Like · Reply · 1w



**Robert L Rauck** There are two resonant modes and the operating point moves between them as one section of the core saturates. I did a Spice simulation with a saturating core model many years ago that showed the jump. It was really neat.

Like · Reply · 1w



**Ray Ridley** Robert L Rauck simulation is great but doesn't compare to seeing on the screen of your scope!

Can you tell everyone what happens after the jump?

Like · Reply · 1w



**Robert L Rauck** We had a unit running in the lab at the time and were comparing waveforms. Certainly not a perfect match but close enough to see the mechanism was right. My partner in the consulting company used to design and build them all the time. I did not. I was the analyst in that case. One of the modes was series resonant and the other was parallel resonant. Saturation caused the dominant mode to flip to the other case when the design volt-second limit was reached. I am going back into my rusty memory more than 20 years. It was a three-legged device and saturation diverted the flux breaking the link between input and output windings to limit power transfer.

Like · Reply · 1w · Edited

and shape waveforms.

Like · Reply · 1w · Edited

Write a reply...

**Robert L Rauck**  
[https://solahevidutysales.com/power\\_conditioning.htm](https://solahevidutysales.com/power_conditioning.htm)

Like · Reply · 1w

**Robert L Rauck** Superior voltage regulation of  $\pm 1\%$  sets the CVS Series power conditioner apart from other power conditioning technologies on the market. Extremely tight regulation is accomplished by Sola/Hevi-Duty's patented ferroresonant transformer technology.

Like · Reply · 1w

**Brian Faley** Many of the designs used today are controlled ferro's where the inductor winding is selectively shorted out to achieve even better regulation - as good as your reference. There is a lot of art to the craft, because the choice of stored energy, whether the cap winding is separate or part of the output winding, shunt stacks - one in a ferro used for DC rectifiers, and two in an AC output ferro, are tuned for cross sectional area, and air gap to determine the design goals. Much of this is empirical because of fringing flux and variations in saturation flux density of a particular batch of laminations. With those two things - and whether the shunts are parallel or normal to the magnetic field, a good designer can make a huge difference in the stability. Also they set the short circuit current. We used to see at least 85-90dB attenuation input to output. Motor boating is the noise caused when the ferro jumps from series to parallel resonance and back again. Also, fringing fields from the saturation of the steel can turn your analog dial wristwatch motor around like crazy and make time fly. I spent a lot of time with them in my CATV days, 2-4kW. They were heavy. We used a crane on the production line to lift them. At least 50% larger than the equivalent

**Ray Ridley** Admin · March 24 at 8:45 PM

Write a comment...

Our 4,000th Member!

Congratulations **Pablo Fernandez** on becoming the 4,000th member of this dynamic and knowledgeable group. I hope that during these trying times you and all other group members find a sense of community and comfort as we all move into uncharted waters.



# 4,000 Members

**Norman Elias** Something to be proud of. Most groups number in the 10's and are often reduced to ads from the members. This group features substantive discussion. Even the ads from Ridley Engineering are primarily announcements regarding classes. Great job Ray.

Like · Reply · 1w · Edited

**Scott Styles** or people asking for the 100th time what size tyres they can fit on their landcruiser w/o rubbing....

Like · Reply · 1w

**Ray Ridley** Thank you **Norman Elias**. Sorry about the ads, but we do have to pay the bills to keep the lights on.

Needless to say, our courses right now have been cancelled until at least July this year. Not the best time to be a training company! But this will pass.

Like · Reply · 1w 2

**Norman Elias** I honestly don't mind your ads, Ray. They fit right in to the informative nature of this group. Your products and workshops are all about spreading knowledge and expertise about power supply design. The group is defined by that topic and everybody speaks from his/her own viewpoint. Every mention of your products is an expression of your viewpoint. Fits perfectly.

Like · Reply · 1w

Write a reply...

**Pablo Fernandez** Excellent!!! I am proud to be the 4000<sup>th</sup> member of this group. I am anxious to be helped by you in power supply design.

Like · Reply · 1w

Write a comment...

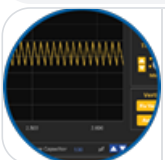
**Ray Ridley** Admin · March 24 at 8:18 PM



You and 27 others 8 Comments

Like Comment

**Ray Ridley** Preliminary specs can be found here: <http://ridleyengineering.com/.../ridleybox-specs-3.html>



RIDLEYENGINEERING.COM  
Ridley Engineering | - Specs

Like · Reply · 1w

Like · Reply · 1w



David Edwards 🇺🇸 Only \$6,000 list. Sweet deal!

Like · Reply · 1w



David Edwards 🇺🇸 Ray Ridley, How and how far in does the front end switch between the oscilloscope circuitry and the frequency response analyzer circuitry? I assume there are small relays to do the switching, but how far into the front end does it occur? Just curious, but I understand you may not wish to share that which you consider proprietary.

Does the box require a tablet or laptop or just a display and mouse? I will look for a manual online, but I bet people would like to read about it here.

As a frequency response analyzer, how does the RidleyBox compare to the AP310? Please comment on resolving signal in the presence of switching noise.

Like · Reply · 1w



Ray Ridley 🇺🇸 David Edwards please see our website for comments about the comparison. It's under the hardware tab.

Computer is in the box 😊

Like · Reply · 1w



Bob Gudge David, why don't you buy one and let us know ?!?

Like · Reply · 1w



Ray Ridley 🇺🇸 David Edwards is retired. We are waiting for everyone else to step up, he already bought our software this week. 🤓

We will have some demo videos pretty soon. We are going as fast as we can in the present circumstances!

Like · Reply · 1w



Ray Ridley 🇺🇸 how does it switch? software.....

I have been working with coders for months, so excuse me if I get cranky sometimes.....

Like · Reply · 1w



Write a reply...



Write a comment...



Norman Elias uploaded a file.

March 26 at 4:25 PM

After the lively discussion on mutual resistance I thought it might be interesting to share some simulation results. As a fan of VHDL-AMS I chose to simulate the model Bryce Hesterman shared in that environment. For those who might be interested, here are the results.

Note: This is for a gapped core and it includes both shorted and open secondary winding

Disclaimer: My purpose is solely to demonstrate the validity of the mutual impedance model. I do not intend this as an indictment of any other model.



Results.pdf PDF



You and 3 others

2 Comments



with product development, software, closed offices etc.

Like · Reply · 1w

**Norman Elias** Thanks Ray. This doesn't have to be a top priority. Just something I chose to share. Stay safe!

Like · Reply · 1w

Write a reply...

Write a comment...



**Ray Ridley**

Admin · March 10 at 8:40 AM

APEC Meeting CANCELLED

## Important Update

In light of growing concerns surrounding the COVID-19 outbreak, and after much thoughtful deliberation, APEC and its sponsors, IEEE IAS, IEEE PELS, and PSMA have decided not to move forward with the in-person conference event scheduled for March 15- 19, in New Orleans, Louisiana.

[Read More](#)

You and 43 others

10 Comments

Like

Comment



**Paul Greenland** About time.

Like · Reply · 3w



**Dimitris Marinis** It took a while to make the decision but now is clear !!

Like · Reply · 3w



**Bob Gudgel** Ray, now see what you started ! 😊

Like · Reply · 3w



**Ray Ridley** That was the virus, **Bob Gudgel**, not me. 😞 I just tried to point out the obvious.

Like · Reply · 3w



**Alain Laprade** I was about to post that ON Semi was pulling out (got an email around noon). A tough and painful call by APEC and exhibitors, but its for the best under the current (a.k.a. confusing) and eventual circumstances.

Like · Reply · 3w



**Norman Elias** Painful but not really tough considering all who had pulled out. The organizers saved others the pain of deciding what to do. I applaud the decision.

Like · Reply · 3w

<https://youtu.be/k2mJui47gmU>



YOUTUBE.COM  
Dr. Eric Berg talking about virus corona - opinion and advice of Dr. Berg on...

Like · Reply · 3w



**Bryce Hesterman** It has become clear how prescient Ray was in being among the first to pull out. New Orleans is now the epicenter of virus growth, probably because of Mardi Gras, which was not long before APEC. <https://www.nytimes.com/.../coronavirus-louisiana-new...>



NYTIMES.COM  
New Orleans Faces a Virus Nightmare, and Mardi Gras May Be Why

Like · Reply · 1w



**Ray Ridley** That's exactly right, [Bryce Hesterman](#). The first case there occurred 14 days after Mardi Gras, followed by a deluge. That explains the explosion of cases so suddenly.

This would have been an absolute disaster for APEC. They are so unbelievably lucky that the exhibitor cancellations forced them to follow suit. A very large bullet was dodged.

I'd like to accept the prescience award, but that goes to [Denise Ridley](#). Two days before I came to my senses she declared "I'm not going there - are you nuts? You are on your own, we won't put our employees in danger either. "

Engineers are not always the best judge of these things.

Love · Reply · 1w



**Ray Ridley** Pretty sure the APEC cancellation-encouragement award will be coming my way soon from the committee. 😊

Like · Reply · 1w · Edited



Write a comment... 🗨️ 📷 GIF 🗑️



**Jim Zydel** March 25 at 5:09 AM

Has anyone used the AP300 to measure the impedance of an inductor while injecting a DC current into the inductor? If so do you have a block diagram of how this was accomplished?

8 Comments



Like



Comment



**Col Johns** You can do it with two identical inductors in series with a large cap end to end - you can look across one of the inductors - the results will be for L/2 ... this will work just with a sig gen too - to give you a very good idea of L with DC bias - at any frequency and at any AC amplitude you care to apply ( from an amplified sig gen )

Like · Reply · 1w



**Ray Ridley** It all depends on how high a frequency you want to measure up to. What would that be, [Jim Zydel](#)?

Like · Reply · 1w

high I'd like the freq. I was thinking the full 50mHz range of the AP300. What is the limitation here?? The inductor is being used to filter the output from a rectifier on a 400Hz 3 phase system. So I think 10kHz at a minimum with a desirement of 100kHz?

Like · Reply · 1w

**Ray Ridley** You can't get proper measurements with DC current bias out to that far. with no dc bias, we resolve winding capacitances down to 2 pF. There is no way to add circuitry to provide the dc bias and not compromise the measurements that we have been able to come up with.

If anyone succeeds, please let us know!

Like · Reply · 1w

**Col Johns** Ray Ridley see above (?) 2 x L in series and look at only one - the other one provides a measure of isolation ... the dc goes thru both - with a cap end to end to put the L's in parallel for AC ...

Like · Reply · 1w

**Ray Ridley** Its the source hooked up that causes the problems.

Like · Reply · 1w

**Col Johns** Ray Ridley OK..

Like · Reply · 1w

**Ray Ridley** We worked hard on trying to solve this. But the sneaky current paths above 1 MHz are pretty impossible to resolve.

Like · Reply · 1w

**Ray Ridley** Admin · March 26 at 11:54 AM

Write a comment...



12

Like

Comment

Write a comment...

**Nicola Rosano** March 26 at 4:40 AM

Dear all, is there someone here from China who can address me on EMC standards and regulation limits used in your country for on board chargers market (electric vehicle related)? Ideally both conducted and radiated.

Thanks a lot

Like Comment

Riccardo Tinivella Ciao nicola obc or inverter?  
Like · Reply · See Translation · 1w

Nicola Rosano obc  
Like · Reply · 1w

Riccardo Tinivella sorry I havent read carefully in the comment, anyhow the main standard is QC/T 895 for obc, this refers to  
 6.7.2 Electromagnetic Disturbance GB/T18487.3-2001  
 6.7.3 Harmonic Current GB17625.1-2003 GB/Z17625.6-2003  
Like · Reply · 1w · Edited

Nicola Rosano great thanks  
Like · Reply · 1w · Edited

Write a reply...
😊 📷 GIF 🗨️

Write a comment...
😊 📷 GIF 🗨️

Janamejaya Rox ⋮  
February 8, 2019

Hello everyone,

Is there an "Short Circuit Withstand Time " equivalent to SiC MOSFET?

I found the Short Circuit Withstand Time from the IGBT datasheet to be 8 us, but I do not see such a number in any SiC FET datasheet.

I was trying to look for a time duration, in case of a fault in the converter/device, within which the device will fail due to high surge current without any Short Circuit Protection Methods.

IGBT: <https://www.onsemi.com/pub/Collateral/HGTD1N120BNS-D.pdf>

SiC FET:  
<https://www.wolfspeed.com/med.../downloads/167/C2M0080120D.pdf>

TI Notes: <http://www.ti.com/lit/an/slua863/slua863.pdf>

Thank you.

**Absolute Maximum Ratings**  $T_C = 25^\circ\text{C}$ , Unless Otherwise Specified

	ALL TYPES	UNITS
Collector to Emitter Voltage .....	1200	V
Collector Current Continuous		
At $T_C = 25^\circ\text{C}$ .....	5.3	A
At $T_C = 110^\circ\text{C}$ .....	2.7	A
Collector Current Pulsed (Note 1) .....	6	A
Gate to Emitter Voltage Continuous .....	±20	V
Gate to Emitter Voltage Pulsed .....	±30	V
Switching Safe Operating Area at $T_J = 150^\circ\text{C}$ (Figure 2) .....	6A at 1200V	
Power Dissipation Total at $T_C = 25^\circ\text{C}$ .....	60	W
Power Dissipation Derating $T_C > 25^\circ\text{C}$ .....	0.476	W/°C
Forward Voltage Avalanche Energy (Note 2) .....	10	mJ
Operating and Storage Junction Temperature Range .....	-55 to 150	°C
Maximum Lead Temperature for Soldering		
Leads at 0.063in (1.6mm) from Case for 10s .....	300	°C
Package Body for 10s, see Techbrief 334 .....	260	°C
Short Circuit Withstand Time (Note 3) at $V_{GE} = 15V$ .....	8	µs
Short Circuit Withstand Time (Note 3) at $V_{GE} = 13V$ .....	13	µs

You and 3 others 47 Comments

Like Comment

Ying Pang Because this is very tricky info — while IGBT quickly reaches saturation under short circuit, SiC doesn't and the current will keep rising very fast  
Like · Reply · 1y



operation in the saturation region?. Short circuit causes the device to enter active region.

Coming to SiC, are there any experimental results done to calculate/estimate the withstand time?.





Like · Reply · 1y

**Ying Pang Janamejaya Rox** I am not sure what you mean — if IGBT is saturated during normal operation then the voltage drop across would be above 7v ca and huge losses

Like · Reply · 1y

**Janamejaya Rox Ying Pang** Thank you for your reply, IMHO isn't the purpose of applying  $V_{ge} > 15V$  (for a Si device) to ensure that the device remains in saturation during normal operation?. If possible, can you please cite a source supporting your explanation. Thank you.

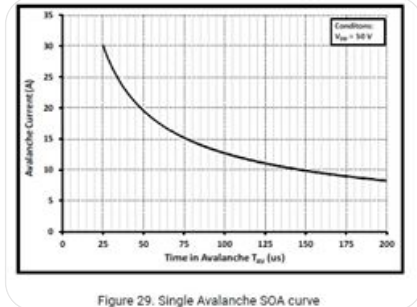
Like · Reply · 1y

Write a reply...    

**Alex Porter** Couldn't you just work this backwards from the SOA and/or transient thermal impedance graph? This would be a bit of a conservative estimated, however.

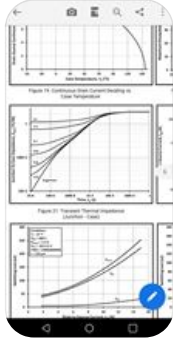
Like · Reply · 1y

**Janamejaya Rox** Thank you Alex, can you please elaborate on your approach. Yes, an estimation would be great.



Like · Reply · 1y

**Alex Porter** Wouldn't it just be matching your expected short circuit current on the left? What I was originally thinking was using something like the graph below and using your anticipated Power dissipation in short circuit, then solving for your required  $Z_{th}$  based on your short circuit power and anticipated  $T_c$  to keep from exceeding  $T_{jmax}$



Like · Reply · 1y

1) I think the SOA approach does not seem right, for example, for 30 A, the avalanche time is 25 us. The Short Circuit Withstand Time is generally less than 3 us. I am not sure how would you relate the two time durations.  
2) Yes, estimating Power dissipation seems like a good idea, I have not used this approach, I will let you know if I decide to use this method.  
Thank you.

Like · Reply · 1y · Edited

Write a reply... [emojis] [camera] [gif] [video]

**Chris Merren** I had a Full-Bridge inverter with FETS... that needed to sustain 10 seconds into a short before shut-down....

Like · Reply · 1y

**Alex Porter** Chris Merren wouldn't short circuit cases for an entire converter be different than that of an individual device?

Like · Reply · 1y

**Chris Merren** Alex Porter Depends what you define as a "short" ..... ie it is just an increased load.... For example.... Between the input filter and the long output cables of an inverter, the short circuit current path has a load.....

Like · Reply · 1y

**Sri Watts** Infineon datasheets spec the short circuit withstand time for SiC MOSFETs to be around 2 us. See datasheet for DF23MR12W1M1\_B11 and its associated application note showing the SC waveform. We design our gate drivers to react in this time range if DESAT protection feature of the gate driver



Like · Reply · 1y

**Janamejaya Rox** Thank you, I greatly appreciate your help. Yes, this was the info I was looking for.

Like · Reply · 1y

**Bob Gudgel** I didn't think that Infineon had any SiC FETs because they could not buy Cree/Wolfspeed ? Do they have their own SiC FETs now ? Or I guess I should ask, Did that buyout finally go through ?

Like · Reply · 1y · Edited

**Janamejaya Rox** Bob Gudgel [https://www.infineon.com/.../coolsic.../df23mr12w1m1\\_b11/...](https://www.infineon.com/.../coolsic.../df23mr12w1m1_b11/...)

INFINEON.COM  
DF23MR12W1M1\_B11 - Infineon Technologies



Like · Reply · 1y

**Bob Gudgel** Yes, I see. But who's SiC FETs are they ? Theirs or Cree's or someone elses? Last I knew, Infineon could not make SiC FETs. Only SiC diodes and wanted to buy Wolfspeed IP

Like · Reply · 1y · Edited

**Janamejaya Rox** Bob Gudgel I get it now, great question, would be good to find out.

Like · Reply · 1y



well. Parameters of Infineon devices are so much different. If it quacks like a duck walks like a duck and looks like a duck it's a duck. I have 23 and 11 mOhm HB modules purchased/not sampled.

[Like](#) · [Reply](#) · 1y



**Charlie Elliott** 🇬🇧 [Bob Gudgel](#) infineon have their own SiC.

[Like](#) · [Reply](#) · 1y



**Charlie Elliott** 🇬🇧 [Sri Wattsa](#) - Hang on - what does that line in the data sheet actually mean? Is it saying that under those conditions the current will typically reach those values and you won't kill the device if you turn off with 2us or something else? If the device isn't going into a current limiting mode of operation then the current you get to within 2us will vary from design to design!!

[Like](#) · [Reply](#) · 1y



Write a reply...



**Bob Gudgel** So, I wasn't sure exactly what this spec meant so I Googled it...  
JDEC says,  
"short-circuit withstand time (tsc)  
The time interval between the instant when the device drive rises to 50% of its peak value and the instant when it falls to 50% of its peak value.  
References:  
JESD24-9, 8/92"

That definition seems to indicate time between "drive" edges. Nothing to do with short-circuits or current. Looking for more info I see figures and graphs that don't make a lot of sense (to me).

[Like](#) · [Reply](#) · 1y



**Chris Merren** It has directly to do with Short circuits... This relates to De-Sat detection and shut-down of the system within (tsc) ... The Vce sat voltage is used to detect when the device is operating in an over-current condition...

[Like](#) · [Reply](#) · 1y



**Bob Gudgel** That's what I was gathering from the times I was seeing in that datasheet and the application notes. I guess j e d e c needs to change their definition. Time to turn off from desat Fault event I understand just fine. Thank you

[Like](#) · [Reply](#) · 1y



**Alex Berestov** SiC is not IGBT by any means, so forget SC withstand time.

[Like](#) · [Reply](#) · 1y



**Bob Gudgel** Well, I don't know for sure but I see a lot of hits for this subject and SiC...

[Like](#) · [Reply](#) · 1y



**Venkat Karthik** Short circuit handling capability is one disadvantage of SiC. It is lower than IGBT.

[Wow](#) · [Reply](#) · 1y



**Charlie Elliott** 🇬🇧 I have asked this from several vendors and received very limited information. S/C ratings on transistors was historically demanded by motor control applications where the drive output terminals to the motor could be easily shorted together or to ground. The fact that you are not seeing it on SiC or GaN data sheets is a direct reflection of the market they were originally targeted at.

[Like](#) · [Reply](#) · 1y



reasonably well protected. Having said that the DESAT detection time is set very fast (1us). There will be a whole raft of tests to be done in this area before production.

[Like](#) · [Reply](#) · 1y · Edited



**Col Johns** Is the de-sat needed because the motor may go short - or another device...?

[Like](#) · [Reply](#) · 1y



**Charlie Elliott** ☹️ Many reasons - gate drive or command fault, short switch detection to try and prevent short across bus, ISO26262 safety case, electrical safety case if get double point insulation failure

[Like](#) · [Reply](#) · 1y



**Bob Gudge** 1 uS is pretty fast de-sat detection from the drivers I have seen with that feature ! Making your own protection ? I suppose detection vs. protection (gate off) are somewhat different things

[Like](#) · [Reply](#) · 1y · Edited



Write a reply...



**Sidharth Gupta** I remember reading for SiC MOSFET , short circuit withstand time to be around 2-3 us..I'll try and find the paper and link it

[Like](#) · [Reply](#) · 1y



**Charlie Elliott** ☹️ It will be interesting to see how they have presented that as s/c time will vary from die m/f to die m/f and also in the specific way it has been pacakged in the discrete device or module.

[Like](#) · [Reply](#) · 1y



**Alex Berestov** Unfortunately JFETs are quite robust in that regard. But SiC fer is actally Baliga pair. In contrast to IGBT and JFET the current on 50 A device can go as high as few hundred Amps and, despite higher thermal conductivity metallization gets destroyed as well. Die size does not help either.

[Like](#) · [Reply](#) · 1y



**Andrii Chub** Here a good reference regarding modules:  
[http://vbn.aau.dk/files/268462337/2017\\_Reigosa\\_TIA.pdf](http://vbn.aau.dk/files/268462337/2017_Reigosa_TIA.pdf)

[Like](#) · [Reply](#) · 1y



**Bob Gudge** There appears to be quite a bit about this on the net regarding SiC SCWT. All I have seen is like your .dk link and is destructive testing. I would think that die size would have a lot to do with this. I know that it does matter for Silicon MOSFETS. I also ran across this theses from Denmark...

[https://projekter.aau.dk/.../MScThesis\\_Pablo\\_Rodriguez\\_de...](https://projekter.aau.dk/.../MScThesis_Pablo_Rodriguez_de...)

[Like](#) · [Reply](#) · 1y



**Andrii Chub** **Bob Gudge** Aalborg University have the biggest in the world research center on reliability of power electronics. They work with numerous components and equipment manufacturers. Probably they can answer this question the best, unless restricted by NDA.

[Like](#) · [Reply](#) · 1y



**Bob Gudge** Seems like this university has its stuff together. There is still some good teaching here in the US but less than it was many years ago I believe. As far as die size, I already know pretty well from years of testing ourselves about die size and "robustness". As long as the die shares pretty well, this makes perfect sense. For SiC which yield is everything, the larger the die, the higher the cost but I think, typically, the better the part will be for the few good SiC suppliers out there now

Write a reply...

**Stephen Berry** Short circuit rating in my view is just another data sheet figure like current rating that means very little. You need to work it out yourself from the SOA. A gate drive that turns off if Vds goes too high sounds like a good idea. **Charlie Elliott**, 1us sounds amazingly short. Must be a special design.

Like · Reply · 1y

**अभी अभी** Actually Short Circuit rating does mean a lot as there are devices which are specifically designed for achieving a higher tsc and Esc at the cost of switching performance.

Like · Reply · 1y

**Charlie Elliott** Hi **Stephen Berry** - Yes 1uS is fast and yes it is a "special project". The gate driver we are using has adjustable blanking time and we have set the passive DESAT filtering quite fast as well. I dont beleive any false trips have been seen yet but it is early days!!

Like · Reply · 1y

**Colin Tuck** Charlie, just put a spanner across the motor terminals to test de-sat effectiveness ...

Like · Reply · 1y

**Bob Gudgel** That's pretty much what I do to test Desat circuitry and the software interrupts.

Like · Reply · 1y

Write a reply...

**अभी अभी** Most of the times devices have an inherent short circuit withstand capability, but the values are mostly published for devices that are used in motor drive applications. You will see the value of SiC MOSFET short circuit for devices which are meant for motor drive applications. Below you will find a datasheet from our latest generation IGBT which is optimized for PFC and DCDC converters. Although the device can handle a shortcircuit event as the device is optimized for switching performance and not tsc the value isn't published.  
<https://www.onsemi.com/pub/Collateral/AFGB40T65SQDN-D.PDF>

Like · Reply · 1y · Edited

**Colin Tuck** No one disputes the short ckt rating of IGBT's, however the OP asked about SiC mosfet - it would be nice to hear from industry, Charlie Elliot has made useful comment based on actual application - this is what should be posted - not too much in the way of speculation I think ..

Like · Reply · 1y

**Matic Uršič** uploaded a file. March 24 at 3:49 AM

Hi everyone. I am looking for some help, opinion.  
I am designing some new Power supply up to 15W, universal input, with various outputs (12V & 5V (regulated)) which are isolated and (12V & 3.3V) which are not isolated. What do you propose to use as a controller, to sufficiently good do the cross regulation so the voltages are in 5% voltage margins.  
I was considering using SSR, but then I came across the information that I might achieve better corss regulation with PSR, as the IC monitors actually AC voltage on the bias winding.  
Secondly I would like to ask you, what approach you go, when you are designing flyback transformer to determine primary inductance, with a known parameters of the IC as the peak current is defined by the IC. I have made some derivation of calculation od the primary inductance so the inductance is calculated as

Many thanks for your propositions and opinions if my derivation is not correct.



5 10 Comments

Like Comment

Alberto Bianco In a traditional flyback, cross regulation is just a matter of transformer & hardware design, the controller can only control one output, or a weighted average of the outputs.

Like · Reply · 1w

Biang Wai Depends on your output currents, RCC may do the works too.

Like · Reply · 1w

Paul Lee A forward converter with a single coupled output inductor for all the outputs can make sense as it can force cross-regulation to improve. If you use a flyback in DCM, there are different combinations of L and i that give the same output power for a given frequency Po.t/efficiency = 0.5Li exp2 so you need to choose where the CCM/DCM boundary is and work back from there. Often set at max duty cycle and load & min input voltage.

Like · Reply · 1w

Venkat Karthik What is the leakage of the transformer your vendor is giving you? I would not consider PSR. Go with SSR, you can save lot of time.

Like · Reply · 1w

Matic Uršič Venkat Karthik we will define, expected is 5% of primary

Like · Reply · 1w

Write a reply...

Col Johns DCM flyback with careful transformer winding - we have done this for 6 o/p ...

Like · Reply · 1w 1

Matic Uršič Col Johns what was the unbalance of the load on different outputs? Did you had outputs referenced to same gnd?

Like · Reply · 1w

Col Johns Because the leakage was very low and balanced - we were able to use a 15V 400mW zener to limit the max Vout on an unloaded o/p - that max unbalance on any o/p from no load to full ( any combination ) was 1V.

Like · Reply · 1w

Matic Uršič And you balanced the leakage by having windings interlaced between the outputs?

Like · Reply · 1w

Col Johns yes, a spread pri, top and bottom and narrower sec's in between ...

Like · Reply · 1w

Write a reply...

Write a comment...

### Power of RidleyWorks® and PSIM

Since we didn't have any conferences in to go to last week, we took the time working remotely to finally finish up our new RidleyWorks® manual, describing how to link to PSIM.

We also ran some new benchmarks versus other techniques and here are the numbers:

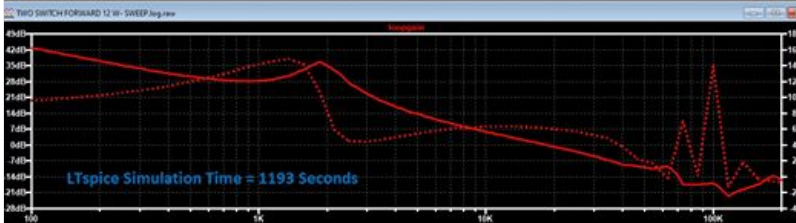
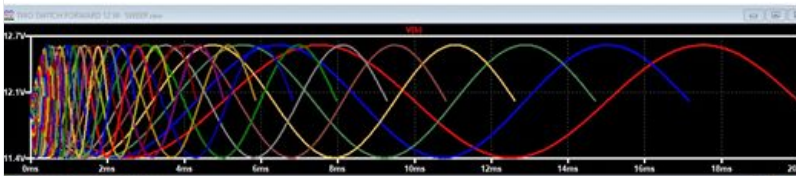
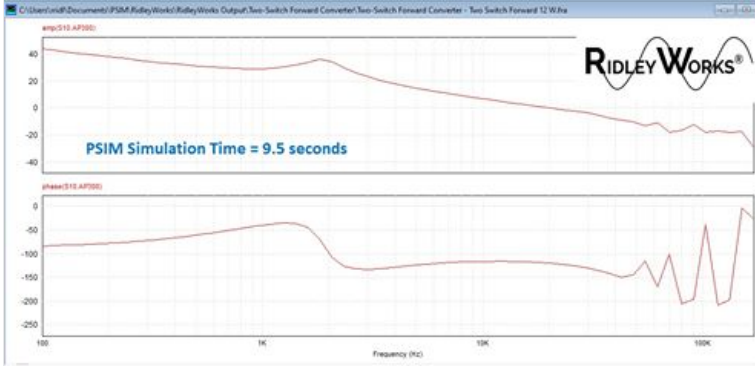
Small signal model in RidleyWorks® - 0 seconds

Swept PSIM circuit from RidleyWorks - 10 seconds

Swept Hardware on AP320 - 17 seconds

Swept LTspice circuit from RidleyWorks - 1190 seconds

We finally have PSIM and its settings working perfectly and running at full power.



Brian Faley and 22 others 30 Comments

Like

Comment

**Ray Ridley** Notable results: PSIM is 120x faster than LTspice. PSIM is 1.7x faster than real-time hardware. That was a new surprise!  
Like · Reply · 2w

**Ray Ridley** Getting used to a new simulation environment like PSIM is hard to get your brain around. We have now made that easy with complete automation of the circuit generation. Once you get inside PSIM, you are going to love working in that environment.  
Like · Reply · 2w

**Ray Ridley** Thanks to **Albert Dunford** for all the work he has put into this project over the last 6+months. We will be doing a webinar about this capability very soon to entertain you while working from 'ohm.  
Like · Reply · 2w · Edited

**Robert L Rauck** That Dunford is OK for a young guy. 😊  
Like · Reply · 2w



Like · Reply · 2w



**Robert L Rauck** [Ray Ridley](#) I have enjoyed working with them for years. Hua Jin is also a great person and brilliant! PSIM is a terrific product with a choice of simulation engines for different purposes! The RidleyWorks link is going to be a major game changer!! The LTSpice link is also really great! The new DSIM functionality that is coming is also going to be great.

Like · Reply · 2w · Edited



**Albert Dunford** [Robert L Rauck](#) you are too kind

Like · Reply · 1w



**Robert L Rauck** [Albert Dunford](#) Albert, I know that!

Like · Reply · 1w



Write a reply...



**John Baillie** Well done everyone involved... will be much appreciated

Like · Reply · 2w



**Norman Elias** Something to look forward to. Will there be a scaled back free version or a student version? I.e., free for simulating RidleyWorks designs with Psim?

Like · Reply · 2w



**Albert Dunford** The demo version of PSIM will be able to run the output from Ridleyworks demo. We already have a component limit version of PSIM which is lower cost than the full pro version. You will likely need to purchase the full pro version of PSIM if you want to use the proximity and core models. There are a few decisions to make still if you have feedback [Norman Elias](#) now is a good time to provide it.

Like · Reply · 1w



**Norman Elias** Thank Al. You might have also seen my PM regarding a beta license for DSIM. I'm interested.

Like · Reply · 1w · Edited



**Albert Dunford** [Norman Elias](#) i didn't notice that. I see it now.

Like · Reply · 1w



Write a reply...



**Ray Ridley** 🙌 You can ask [Albert Dunford](#) that question.

Like · Reply · 2w



**David Edwards** ☕ Hi [Ray Ridley](#),

Copied the files to the SysWOW64 folder as directed. Still no joy. 😞

Like · Reply · 1w



**David Edwards** ☕ Tried rebooting. Seems to work now. 😊

Like · Reply · 1w · Edited



**David Edwards** ☕ Forward converter transient ac loop gain sweep took 131 seconds. 😞

Like · Reply · 1w · Edited



**Ray Ridley** 🙌 [David Edwards](#) that's with LTSpice?

Like · Reply · 1w





PS: Please look for my email for full details.

Like · Reply · 1w · Edited



**Lev Nemets** [David Edwards](#) Could you please share a circuit what you simulated. I would like to see how much time it will take for SIMPLIS

Like · Reply · 1w



Write a reply...



**Ray Ridley** 🗨️ Ok you need the next version. Psim has just worked in the latest speed up.

Like · Reply · 1w



**David Edwards** 🗨️ I have an 8/16 core fast processor, a very fast SSD and 64GB of RAM. I have set up 32GB as a RAM drive, which LTspice uses for saving waveform data. The 131 seconds was what was reported in LTspice's Error Log (output file).

Is the "next version" newer than what I downloaded and installed today?

Like · Reply · 1w · Edited



**Lev Nemets** I just simulated Forward converter (two MOSFETs) with UC3845 controller CT current sense. SIMPLIS takes 6 second to simulate.

Like · Reply · 1w



**Ray Ridley** 🗨️ That's about the same as psim. Just need the latest version.

Like · Reply · 1w



**Ray Ridley** 🗨️ OK sorry, I thought you meant you were using PSIM. that's about right for LTspice. Really happy **you got this** all working.

Like · Reply · 1w



**Ray Ridley** 🗨️ PSIM and Simplis will be comparable speed. PSIM is a fraction of the price, and branching out strongly in digital control areas. I recommend you try it.

Of course, the small signal models in RidleyWorks or those we generate for LTspice are instantaneous.

We use all these tools (not Simplis though).

Like · Reply · 1w



**David Edwards** 🗨️ When I compared PSIM to SIMPLIS maybe five years ago PSIM was much noisier and slower than SIMPLIS. This was for transient ac analysis. I was not impressed. It seems, thanks to [Ray Ridley](#), it's now as good or better.

Like · Reply · 1w



**Ray Ridley** 🗨️ I'm sure [Albert Dunford](#) can get you setup with a trial license.

When we started 6 months ago, you are right, it was pretty awful. We had to teach them a few things about how real-world analyzers work. They are quick learners!

Like · Reply · 1w



**Albert Dunford** [David Edwards](#) So the new sweep is in our 2020 build which should be mid-april. There are a few hang ups regarding a code gen target 28004x that we want to release. The new sweep and the ridley works outputs are good to go. If you want to test drive the beta please PM me your email address and I will set you up.

Like · Reply · 1w · Edited



Like · Reply · 1w



Write a reply...



Write a comment...

**Dan Cousin**

March 23 at 9:33 AM

general question: Why are planar transformers not more popular? I see and do a lot of transformers with wound bobbins but there are always tolerances involved from unit to unit. Where planars are applicable (~100Vin and below flybacks to lower voltage out) what are the downsides to them. Cost and repeatability seem to be pluses. what are the downsides from a production and technical point of view?



4

28 Comments



Like



Comment

**Manu Raj** Mostly need to go with multiple layer PCB

Like · Reply · 1w

**Nelson Garcia** Planar transformers are usually higher cost when compared to traditional bobbin and core transformer.

Like · Reply · 1w · Edited

**David Edwards** 🙄 The field distribution across the planar windings in a gapped planar magnetic element leads to untenably large winding losses. Generally, gaps do not make sense in planar magnetic structures.

Like · Reply · 1w

**Darrell Hambley** please tell more about the bad field distribution. a sketch? Are you thinking only of fringing effect loss or something else?

Like · Reply · 1w · Edited

**Bharadwaj Reddy** I design planar transformers till 100 kw. In general they are expensive compared to wire wound and also needs special technics in connecting turns which most of the companies doesn't know.

Like · Reply · 1w

**Andrew Ferencz** Planar is used in almost all brick power; great for coupling, terrible for EMI if you don't know how to layer windings, costly if you use buried vias ... not good if you need 100 turns, great if you need 1 turn, great if the design is fixed, not good if you keep changing the turns ratio (!), .. better for forward, probably not as good for flyback ..

Like · Reply · 1w



**Yuri de Klerk** Used with punched copper for the windings can do high currents, but high number of turns is not practical. The punched copper makes it relatively expensive. Losses are not lowest with planar, but because of the large surface the thermal behaviour is better, so for low profile converters it's beneficial in terms of size. It's been said planar has high interwinding and prim-sec capacitance, but I didn't read analysis about that. High prim-sec capacitance will of course 'help' the converter to make its EMI signature.

Like · Reply · 1w · Edited

involved with are no less than 6 to 8 layers anyway.....so it's basically free copper area.... I prefer to use the "spiral" copper traces using the Ferroxcube cores.... Gaped cores can be a problem as mentioned by David....This is from fringing effects that can wreak havoc on the copper traces... Fringing gets worse with larger gap.... I use FEA to calculate the fringing and reduce the gap size to reduce the fringing to acceptable size, then then distribute the gap in multiple small gaps in series to achieve the intended gap without the huge fringing.

Like · Reply · 1w · Edited

**Yuri de Klerk** Up to what power did you use PCB integrated planars **Chris Merren** ?

Like · Reply · 1w

**Chris Merren** **Yuri de Klerk** Up to 500W range... Probably can go higher... Planar PCB transformers make excellent Gate Driver isolation circuits... Just watch your creepage and clearances...

Like · Reply · 1w

**Alain Laprade** Are there patent issues? From memory, some company had successfully defended planar magnetics patents years ago. Might have expired by now. I'm intrigued as to how this company ever successfully defended the concept of planar magnetic patents. Methodology was in print by Unitrode circa 1982. I recall a published paper on the topic as well around that time (would have to dig real deep to find a paper copy). I worked at Sperry in Montreal in 1984 and the use of TDK X22 and X40 cores was well established at the time. Ray Ridley may want to chime in on my question; I seem to recall the use of planar magnetics at VPEC ~mid 1980s as well.

Like · Reply · 1w

**Stuart Wood** They also tend to have higher intertwining capacitance. This is one of the reasons that can cause poor EMI performance.

Like · Reply · 1w

**Chris Merren** Well that's a generalization.... You can control you capacitance and leakage based on stack-up ....Prepreg thicknesses and core thicknesses can be set ...

Like · Reply · 1w

**Stuart Wood** **Chris Merren** correct, but we don't have any specifics to talk about, and it's not an easy task to get low capacitance and low leakage, especially in a planar design.

Like · Reply · 1w

**Chris Merren** **Stuart Wood** Low capacitance or low leakage is not the issue.... It's all about if you can achieve whats required for the application..

V DC	
PCB BOARD STACK-UP .062"	
TOTAL # LAYERS	6
TRACE LAYERS	6
CORE-BOARD CLEARANCE	
core window mm =	3.1
CORE to BOARD mils =	8.37
PRI-to-SEC CAPACITANCE	
CAPACITANCE pF =	2.26
PRI-to-SEC LEAKAGE INDUCTANCE	
LEAKAGE nH =	502.9
RESONANT FREQUENCY	
MHz =	136

Like · Reply · 1w

**Chris Merren**



Like · Reply · 1w



**Adhstira Madhyasta Naradhipa** Hi, I also have an issue with the high intra- and inter-winding capacitance in the planar transformer. Do you have any reference on how to analytically calculate the caps? especially when there is more than one turn in a layer. Thank you in advance!.

Like · Reply · 1w



**Arief Noor Rahman** One way is to use one PCB layer as a shield connected to input positive voltage node or negative voltage node...but, it is costly considering that layer will not be useful for any power delivery,

And if the transformer use Pri-Sec-Pri structure, then you must sacrifice two layer only for shield...

Like · Reply · 1w



**Adhstira Madhyasta Naradhipa** The shield is for the caps between pri-sec right? how about the caps between pri-pri?.

Any reference for calculation? or maybe steps to model and simulate for trans caps in FEM software?.



Like · Reply · 1w



**Arief Noor Rahman** Intra winding will be more tricky, my guess you may want to make sure to minimize voltage different for every adjacent primary copper trace...

I am not really a magnetic expert...haha

Like · Reply · 1w



**Dan Cousin** one question. I have a flyback design with 8turns on the primary and 1turn on the sec. Primary had two 4turn layers My concern is the secondary is a single wide trace. im thinking of eddy current due to fringe fields. would making the single turn multiple parallel instead. of a single trace be better?

Like · Reply · 1w



Write a reply...



**Venkat Karthik** Easy to cool them down. Telecom power supplies 36V- 72 Vin -> 12 V out ( bricks) are all planar ( they are 8-12 layers) . Commercial power supplies (< 300 W): Forget about it, 1 layer - 2 layer max. Planar is costly. I have actually heard, planars are less reliable than a wire wound bobbin because if you look at a 8 layer pcb, they are several 2 layer pcbs bonded together and when you are designing a transformer and have to go through layers you have to fill up the blind burried vias. You have to assemble them reliably.

Like · Reply · 1w



**Riccardo Tinivella** In automotive is becoming more and more standard due to cost and vibration advantages. On contrary, parasitic caps and limitations on max turns pro layer are the disadvantages

Like · Reply · 1w

magnet wire in the minimum spacing required for turn to turn isolation on a pcb layer

Like · Reply · 1w



**Ray Ridley** So many types of "planar transformer", there can be many answers to this question.

It is better to start at the beginning - what exactly do you mean by a "planar" transformer? Once this is answered, some specific answers can be given.

Like · Reply · 1w



**Dan Cousin** Im thinking the 1/32 to 1/16 brick market. but incorporating it into the board instead of buying it and soldering it in. typically these are flyback designs. fully isolated. for moderate input voltage to keep the primary turn count down, and single or low turn count secondaries. seems like once the pcb is designed its almost free to get precision aligned windings from unit to unit

Like · Reply · 1w



**Dan Cousin** Thinking the size of E14 or E18 running in the 500-1Mhz range.

Like · Reply · 1w



**Ray Ridley** Multilayer, thick copper PCB boards with blind buried high-current vias are not free. Nor are they more reliable than wires.



Doesn't mean you shouldn't use them - it is just not the right solution for every application. Sometimes it fits, sometimes it doesn't.

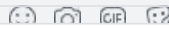
Like · Reply · 1w



Write a reply...



Write a comment...



**Ray Ridley**

Admin · March 25 at 7:21 AM

### APEC 2020 Portal

I have been refraining from posting here about the APEC cancellation for various reasons. However I would like to alert my group members to the email you may have received last week offering access to the materials from APEC. Inside the letter is this innocuous-looking notice that you should consider before jumping in.

**Advisement:** By usage of this conference specific app and/or web portal you agree that you have received benefit from the APEC 2020 conference.



Darrell Hambley and 16 others

8 Comments



Like



Comment



**Alain Laprade** Any idea what that may imply? Sounds like a billing statement.

Like · Reply · 1w



**Albert Dunford** It means that if you access the web portal you won't get a refund as you are agreeing that you have received full value for your registration fee. I don't know about you but a few pdfs, most of which I will never read does not equal a conference with an expo hall.

Like · Reply · 1w



**Albert Dunford**



Like · Reply · 1w



**Sarah Lynch** This is such an outrage! For sure the virtual portal and even if they do a real virtual event it's not of much value for exhibitors. But even for people who were just going to attend this is probably not close to the same value as the in-person event. But if they would at least clearly state their intention that accessing the portal will probably void your possible refund... Disgusting!

Like · Reply · 1w



**Alain Laprade** Despicable act.

Like · Reply · 1w



**Peter Ksiazek** Wow

Like · Reply · 1w



**Clive Harvey** 🙄 This current climate really does prove the points being made about modern day big business.

Long gone are the days of customer service, the customer is always right and life time customer base.

Like · Reply · 1w

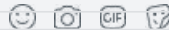


**Michael Delany** Never been to APEC but one of my former coworkers had a billion APEC books. I imagine these are presentations and such. Is it possible to access these?

Like · Reply · 1w



Write a comment...



**John Baillie**

March 20 at 2:42 AM

Hello,

I'm using a Traco TMR6 WIR +/-15V supply in my design and after only about 10hours of up-time the -15V rail is playing up. It goes down to -18V and wanders up to -16V. It was only powering some comparators up to now and the positive and negative rails are loaded to within 20% of each other so I'm scratching my head as to what would cause this. Bulk capacitance at the output is 10uF on each rail. Any ideas as to why this would happen or anyone have the same experience with this part? It's railway grade part and very expensive!

Thanks,

John



2

13 Comments



**John Baillie** UPDATE - low battery on multimeter 🤔😬. Positive voltages are measuring correctly but any negative ones are not.

Like · Reply · 2w



**Ray Ridley** 🗨️ John Baillie been there done that! Not on the last 35 years though. The lesson sticks with you.

Like · Reply · 2w



**Hamish Laird** John Baillie that's a good one!

Like · Reply · 2w

Like · Reply · 2w

**Hamish Laird** Ray Ridley 👍

Like · Reply · 2w

Write a reply...

**Casper Hjort Wilson** What happens if you load the outputs evenly? Sometimes the regulation is only done on the positive rail to GND while the negative is bifilar wound with the positive, so tracking should be optimum - nevertheless, this means the negative rail can drop and it's dependent on the load. Try to make a little bleed (1-10mA) with a resistor and zener from GND to negative output.

Like · Reply · 2w

**John Baillie** Thanks **Casper Hjort Wilson** yeah i tried loading it a bit but turns out it was my multimeter that was giving a false reading due to low battery.

Like · Reply · 2w

**Casper Hjort Wilson** **John Baillie** OK, but also the negative? I thought you still had problems with the negatives even with fresh batteries 😊

Like · Reply · 2w

**John Baillie** No all good

Like · Reply · 2w

Write a reply...

**John Baillie** I was very surprised that a Fluke meter wouldn't automatically refuse to turn on below a certain battery voltage to avoid false readings. Could be very dangerous. I assumed that the low battery indicator was just that, not an indicator that the reading is junk. Lesson learned!

Like · Reply · 2w

**Scott Styles** don't assume that all flukes are built to similar standards. We don't have any of the F19 esque range of meters at work anymore.

Like · Reply · 2w

**Norman Elias** Things are not always what they seem to be.

Like · Reply · 1w

**Ray Ridley** 🤫 This is a secret you learn and don't tell others since it give you a design edge. 😊

Like · Reply · 1w

Write a comment...

**Ray Ridley** Admin · March 24 at 8:18 PM

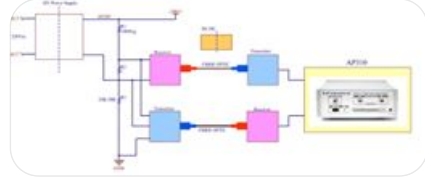
AP310 Frequency Response Analyzer



14 3 Comments

Like Comment

AR Jam Ray Ridley Hi Dr.Ridley Hopefully, I will obtain one of them in future. Is it possible to use fiberoptic interface for frequency response analysis for high voltage power supply applications.Im not sure that fiber optic is good choice. What is the best approach to analyze frequency response for HV power supplies? Thank you 🙏



Like · Reply · 1w · Edited

Ray Ridley Just use the HV differential probes that you can get for the AP. that will take you to 1000 V. If that doesn't work, you can come up with any interface you like to isolate the signals. The AP will measure whatever you present to its terminals. You can even calibrate out the probes with the software.

Like · Reply · 1w

Write a reply...

Brian Feighner I think we are getting one to replace our AP300

Like · Reply · 1w

Write a comment...

Stuart Wood March 25 at 5:54 AM

Dr. Ray Ridley, from your 2018 APEC presentation New High-Frequency Magnetics Circuit Models, how did you calculate the overall resistor value needed at each frequency, on slide 64, step 3? I thought it would have been the Drive Voltage^2.45 \* Duty Cycle divided by power.

2 8 Comments

Like Comment

Stuart Wood Parallel Ladder Network – Calculating Values Step 3 Find overall resistor value needed at each frequency

Like · Reply · 1w

Ray Ridley We have revisited and revised this resistor choice quite a few times since then. The selection of the RL parallel network values is quite intensive math, I left that to a PhD graduate student to solve!

Like · Reply · 1w



assumed, and there is a scale factor involved.

As the duty cycle on the converter changes, the dissipation will go up even as the delta B stays the same. That is one of the good features of the model that we use.

Like · Reply · 1w



**Stuart Wood** My numbers are off by a factor of 1.294 if I remove the duty cycle.

Have you published any more information on this since 2018?

Like · Reply · 1w



**Ray Ridley** It's all encapsulated in our software. To be honest, I no longer remember the algorithm. That was two years ago!

We haven't published any more since then, it just takes too much time and energy to do that. Hopefully we can get back to it.

If you are trying to generate the models for yourself, just be aware it is a substantial amount of work. Three grad students were involved, it's not a 10 minute task.

Like · Reply · 1w



**Stuart Wood** Understood. But we need a model that can be used by engineers in general, that doesn't require proprietary software ( I'm not against proprietary software). Your model looks to be very good.

I can calculate all the values you used on your presentation, except the one in question. Which seems to have a "fudge factor" of 1.294 in it. It's this do to parallel resistor paths lowering the effective resistance at a given frequency?

Like · Reply · 1w



**Ray Ridley** It's not a fudge factor. It's a combination of many things.

If I were still an academic, There would be a dissertation on this, hundreds of equations, and it would get published. Then you would spend weeks studying it and implementing it in your own software.

when you are done, your software would arrive at the point that the original work was done.

Like · Reply · 1w · Edited



**Ray Ridley** I view these topics this way - if you want to use someone's fet, you trust them to give a model. You don't have to go back to fundamentals to derive it for yourself to get a good result in the lab.

Our software is like that. We have over 3900 equations for design at the last count. Do you need to know them all to be able to trust the designs? If so, you would never get any work done. 🤖

Like · Reply · 1w



Write a comment...



**Jean Jacques Girin**

March 24 at 1:28 PM

Hi Guys, I would appreciate some advice. I am looking a designing a isolated dc/dc . Input 9v to 24V / Output 4kv dc 10w max. I looked at flyback and converter using multiplier but I would like to check out Fly Buck. The regulated output will be a 7V. The isolated output will be built using 5 secondary 800V each. Turn ration around 800v/ 7v= 115. The diode voltage Vd 24V x 115V = 2760V, may use two 2kv diodes in series. For the controller TI and ST have few parts, like the L6986(H): 2 A rated 38V. This part is fixed on Time and integrated Mosfets. First impression, look like a lots of turns! Would this work?

2

12 Comments





using 6 o/p wdg's - the transformer design is the critical bit ...

Like · Reply · 1w



**Jean Jacques Girin** I think that you are correct, fly buck would work well for low voltage output. I will look at Flyback again. thanks again

Like · Reply · 1w



**Daniel Pruna** Never heard of fly buck...do you mean isolated buck (Forward converter)?

Like · Reply · 1w



**Bob Gudgel** I think of a Fly Buck as an isolated flyback with turns ratio such that has secondary voltage lower than the input voltage. Isn't that what it is ? I am guessing

Like · Reply · 1w



**Jean Jacques Girin** <https://www.youtube.com/watch?v=WdkazE73MLE>



YOUTUBE.COM

Multi-Output Fly-Buck Solution

Like · Reply · 1w



**Gourahari Nayak** Flybuck is buck converter with coupled output filter inductor for isolated output

Like · Reply · 1w



**Bryce Hesterman Col Johns** As was mentioned, the transformer design is critical. You will want to have several secondary windings with rectified outputs connected in series. This helps keep the diode voltages reasonable and also helps prevent corona. The leakage inductances will be significant, so snubbers will be required.

Like · Reply · 1w



**Colin Tuck** Fly buck is a combined fly back and isolated buck ( fwd conv ) in one - have been around for a few years now ... there are some patents out there ...

Like · Reply · 1w



Write a reply...



**Stuart Wood** Looks at CCFL designs and transformers.

Like · Reply · 1w



**Ray Ridley** As mentioned - it is all about the transformer.

Beware of corona! It will come to say hello to you.

Like · Reply · 1w



**Alex Berestov** I would rather do push-pull forward, may be resonant one, with multiplier at output. Having 5 HV windings with low coupling is questionable for flyback. That said CRT TV utilizes horizontal deflection circuitry for anode voltage. And it's ZCS as Col Johns suggested.

Like · Reply · 1w · Edited



sine wave voltages and several stages of voltage multipliers on the secondary. Consider encapsulating the transformer and high voltage



Federico Rodighiero

March 20 at 5:55 AM

Hello,

I would ask help here because I am struggling with an EMI problem on a Low Voltage 3-phase PMSM drive.

**The fact:**

The problem is in the radiated range, in particular between 30-50Mhz. I was able to find the source of this noise which is ringing during mosfet commutation. More specifically, as can be seen in the picture, I can see this ringing with a DiY HF current probe (see Kenneth Wyatt articles for details) on the single phase of the motor. Furthermore, there is also a similar (maybe the same) ringing on Vgs\_HS during the miller plateau.

**Picture and test description:**

Yellow: out phase voltage, passive probe

Blu: single-phase current HF current probe

Purple: Vgs high side mosfet with 200Mhz Tektronix differential probe

The measurement has been done with only one leg switching with a fixed duty cycle. The configuration is like a buck with and L-R load. The current during the test is around 8A.

**Components used:**

Gate driver: DRV8323

Original mosfet: DMTH6002LPS

Alternative mosfet: TPH1R306P1

**Notes:**

This ringing doesn't change by adding Cgs, Cgd and also the alternative mosfet shows the same issue.

The ringing is the same with different current load (4A,8A and 16A )

Lowering the gate current doesn't solve the problem (it has been changed from 1A to 330mA).

Increasing the layout inductance lower the ringing. I have noted this by replacing the low side shunt with a wire for current measurement.

**Questions:**

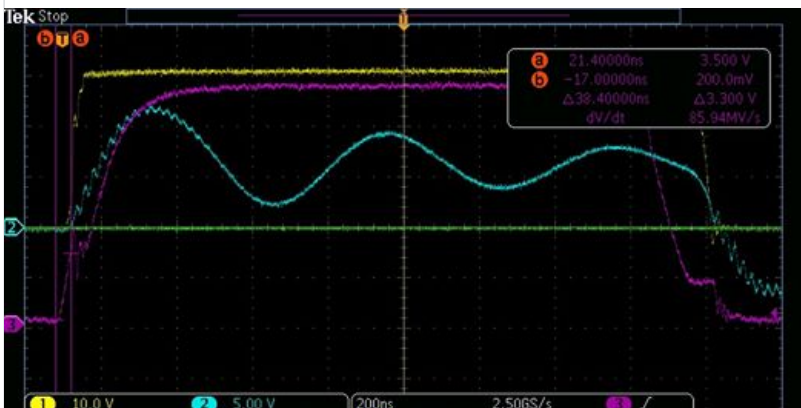
Could this ringing be related to the body diode reverse recovery?

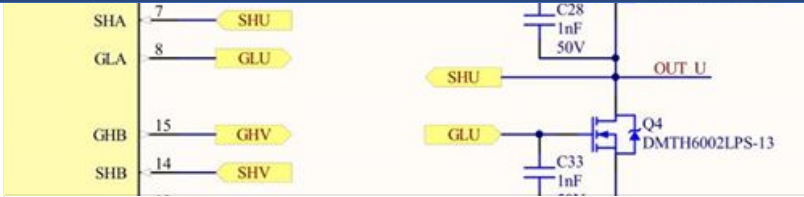
The Vgs ringing is the cause or a consequence?

Could the problem be related to the active drive nature of the gate driver?

What causes this ringing?

Thanks





10 37 Comments

Like Comment

**Long Nguyen** You should consider inductance stray and parastic of Mosfet package. It is the cause for high EMI. Please reduce current loop of Vgs, Vds. So You need add snubber for Vds Mosfet and Capacitor near the bus DC of half brigde.

Like · Reply · 2w

**Long Nguyen** When You use shunt sensor for current sensing, it is increase current loop. So EMI will increase when higher current

Like · Reply · 2w

**Long Nguyen** you should Value of C28 and C33 (about 4.7nF) to decrease Miller effect of switch

Like · Reply · 2w · Edited

**Federico Rodighiero** Thanks, I hoped to avoid the snubber but it will try it. There is already 1uf MLCC near each leg, the layout is very compact and the loops are small. Already tried 10nF con C28 and C33 no improvement. As I said in the notes, the increase of shunt inductance clearly REDUCE the ringing.

Like · Reply · 2w

Write a reply...

**Alain Laprade** **Federico Rodighiero**, if I'm interpreting the information correctly, the ringing continues well beyond the MOSFET plateau region. As Long mentioned above, adding a VDS snubber should be explored. But I have the impression there is an LC resonance unrelated to the switches. I have not done PMSM drive designs, but do recall discussions with peers years ago with resonances related to PMSM interwinding capacitance. I don't have further insight to offer on that topic, but perhaps focusing some debugging effort in that direction might be informative (perhaps a google search on that topic might reveal additional information).

Like · Reply · 2w

**Federico Rodighiero** thanks, this could be a point that I haven't considered. I will try to substitute the motor with an inductor.

Like · Reply · 2w

**Long Nguyen** With motor control, I have tried with the phase current of 120A, very good waveform, very little ringing. As the current increased to 150A and above, it started to deteriorate as you described, but it wasn't too bad

Like · Reply · 2w

**Arief Noor Rahman** 🙏 I am just curious, if blue waveform is phase current, why is it from zero when high side Vgs is off?

Like · Reply · 2w

**Federico Rodighiero** It is a DIY HF current probe as described in Kenneth Wyatt articles. So it is AC coupled.

Like · Reply · 2w



2.5MHz. Far away from the range of 30 - 50 MHz of EMI noise you are trying to troubleshoot.

Usually that high frequency noise is coming from uC, clock frequencies or poor bypassing of chips. Is that a broadband noise? As far as motor drivers are concerned, changing the slew rate, trying spread spectrum and adding snubber helps the case. Last resort is shielding.

[Like](#) · [Reply](#) · 2w



**Hassan Shabbir** just noticed that you are turning it ON and OFF too fast. you can add a series resistor to the gates of the fets and also add a pull down resistor on the gates.

[Like](#) · [Reply](#) · 2w · Edited



**Federico Rodighiero** you are focused on the big oscillation, look at the small one at the beginning on the turn-on. Regarding gate resistor, it is not easy to place resistor due to the layout, I have to cut a track to do it. It is not supposed to be needed because the gate driver is current regulated, so you can set the sink/source current via SPI.

[Like](#) · [Reply](#) · 2w



**Magnus Rosén** Add Vbus el.el. capacitance. Suggest 1mF to 10mF depending on the power source impedance. If long wires to the load/inductor/motor may additional measure be necessary.

[Like](#) · [Reply](#) · 2w



**Federico Rodighiero** there are 200uf polymer capacitor with very low esr near the switching cell. The motor wires are about 20cm.thanks.

[Like](#) · [Reply](#) · 2w



**Magnus Rosén** [Federico Rodighiero](#) Investigate if there are series/parallel resonances. With low rDson fets, low esr dc cap and low res motor you may have an issue. Manifesting in several natural resonance that radiates the 50MHz-ish you struggle with.

[Like](#) · [Reply](#) · 2w



**Broox Le** In this kind of switching arrangement with SH1 low-side sensing resistor and OUT\_U driving the inductive winding, is it better to apply an R-C snubber directly across Q4 drain-source as close as possible, or from drain (OUT\_U) to 0V (power ground)?

[Like](#) · [Reply](#) · 2w



**David Edwards** 🙏. Hello [Long Nguyen](#),

Is your supply voltage about 30 volts?

What is the dead time between the high and low side switch drive?

Do you have gate resistors between the drive IC and MOSFETs?

Is the 50 MHz ringing occurring only on the high side switch transitions?

You stated that the current is measured with a probe on the wire to the motor, not the current sense resistor. Is that correct?

If so, why does the current appear to dip below zero and reverse? (shouldn't the motor winding inductance keep it more or less constant at the time scale of your oscilloscope photo?)

[Like](#) · [Reply](#) · 2w



**Long Nguyen** [David Edwards](#) sorry. The above image is not me

[Like](#) · [Reply](#) · 2w



**David Edwards** 🙏 [Long Nguyen](#) Sorry, I will try again.

[Like](#) · [Reply](#) · 2w



Is your supply voltage about 30 volts?

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[Like](#) · [Reply](#) · 2w



**Federico Rodighiero** yes it is 30V

400nS deadtime, it is not visible but the yellow track is at -0.5V before the turn on, so the Q4 body diode is conducting and we have an hard turn-off of Q4 body diode.

Unfortunately there are no gate resistor. They were not supposed to be needed because the gate driver is current regulated, so you can set the sink/source current via SPI.

No, you can see that it is present also during turn-off.

Correct, SH1 is used for current loop but is not used in this scope measurement.

It is a DIY HF current probe as described in Kenneth Wyatt articles. So it is AC coupled.

thanks

[Like](#) · [Reply](#) · 2w · Edited



**David Edwards** 🍷 . [Federico Rodighiero](#),

Is there ringing when the low side switch turns on or off? (Not the same as when the high side turns on or off.)

[Like](#) · [Reply](#) · 2w



**Federico Rodighiero** [David Edwards](#) the question is clear, there seems to be no ringing on low side turn-on (it is easy because it should be a ZVS). About the turn-off I don't have any picture to verify.

[Like](#) · [Reply](#) · 2w



Write a reply...



**Col Johns** 50MHz is almost certainly diode rev recovery - design and place the largest wattage snubbers you can fit directly across each fet and see if it reduces - if it does you are on the right track.

It may be gate ringing during transition too, adding gate caps can make this worse if the Bus caps are to far away / too high in ESL, and the gate drive is not very low Z ...

[Like](#) · [Reply](#) · 2w · Edited



**Federico Rodighiero** Hello [Col Johns](#), I hoped in your answer.

I have tried only with 10nF parallel to Q4 Cds and it clearly lower the ringing but why ? For sure I will try with and RC snubber but I wanted to learn what is the root of this problem.

There are 200uf polymer capacitor with very low esr/esl near the switching cell. Could you please explain why the bus caps distance (which should means parasitic inductance) can cause this kind of oscillation ?

Thanks

[Like](#) · [Reply](#) · 2w



**Peter Bernard Green** It looks like you don't have a series gate drive resistor. Typically a few Ohms helps to damp ringing.

venkat Karthik The ringing you see in the plateau region of the mosfet is because of the switch node being pulled high ( high side mosfet turning ON). This can be due to the reverse recovery of the low side mosfet body diode or parasitic L-C ringing or both combined ( phase current is into the windings- phase current >0 ). This ringing is quite common. With DRV832x even though it is a current based gate drive I would definitely put a place holder for gate resistor of 1 ohm and increase the Tdrive and decrease the Idrive < 300 mA ( depends on what your control is ). I have worked with trapezoidal 6 - step control. Also always put place holder for R-C snubber across the mosfet ( 0.5 ohm - 1nF). In my experience gate resistor would definitely help with VDS ringing. Put ceramic caps across each phase ( 1-4.7 uF). You will see that the phase (U, V or W) which is closer to the DC bus or battery will have lower ringing on VDS. For RC snubbers, it depends on the Coss of the mosfet (and the battery voltage) and the parasitic inductance of the circuit. Usually, C is chosen to be at least 2 to 3 times bigger than the Coss of the FET at the battery voltage. If the Coss is below 1nF, a few nF for C would be ok.

Like · Reply · 2w

Federico Rodighiero thanks, very useful answer.

Like · Reply · 2w

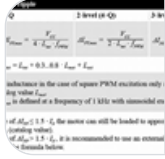
Hüseyin Murat Polater Some motors have high parasitic capacitance related to their windings.you may try to add an inductance around 33u each phase.also you may check Macon motors application note related to minimum motor phase inductances

Like · Reply · 2w

Federico Rodighiero adding 33uF 30A inductor is quite difficult in a compact drive, however, do you have more precise reference for the AN ? thanks

Like · Reply · 2w

Hüseyin Murat Polater <https://support.maxongroup.com/.../360005046213-PWM-power...>



SUPPORT.MAXONGROUP.COM PWM power stage: Current ripple & Motor chokes

Like · Reply · 2w

Federico Rodighiero thanks, the AN is interesting for current feedback problem related to low inductance motor. however, there is not reference to low inductance motor and inter winding capacitance effect on EMI.

Like · Reply · 1w

Hüseyin Murat Polater Federico Rodighiero you may search for motor choke. You will find lots of articles

Like · Reply · 1w

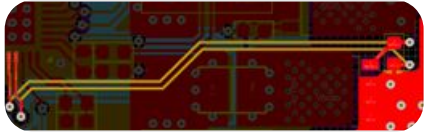
Write a reply...

David Edwards Federico Rodighiero, Does the gate drive route to its own source pin not connected to the other source pins? If so the internal common source inductance is about 0.3nH. If you did a good layout the external loop inductance through the MOSFETs and supply bypass is about 10nH or so. These are what's ringing.

Damp it by connecting a series surface mount RC between drain and gate on each MOSFET. R=10 ohms, C=330pF.

Like · Reply · 2w

is a picture of the HS gate layout.



Like · Reply · 2w

**David Edwards** ☕ · Federico Rodighiero,

As an experiment, perhaps you might try cutting the gate drive's source pin free from the other source pins on the PCB. This way the drive source will have its own bond wire(s) direct to the source on the MOSFET die. If the MOSFET manufacturer designed the number and placement of die landing pads well and placed the bond wires appropriately this should decrease common source inductance to your drive signal (and do so without upsetting the balance of the currents on the die).

You won't know without cutting the PCB (or getting a picture of the die without the epoxy or getting an x-ray picture of the MOSFET). If it doesn't help or is worse, you can always rework the PCB to make the connections again. With the PCB as is the common source inductance might be as high as 1nH to 3nH from the bond wires.

Like · Reply · 2w

**Federico Rodighiero** David Edwards if I have understand well your are purposing a kind of "homemade" kelvin source connection, am I right ?

Like · Reply · 1w

Write a reply... [emojis]

Write a comment... [emojis]

**Arief Noor Rahman** Conversation Starter · March 22 at 8:06 AM

In single phase PFC, how to implement notch filter for output DC voltage ripple filtering in universal 50/60Hz operation?

I am thinking to cascade two second order notch filter with 100Hz center frequency and 120Hz center frequency each.

any alternative design method?

\*I use MCU for my controller, and filter will be implemented by code

Thanks,,,

2 Likes 52 Comments

Like Comment

**李小道** To reject the 100/120Hz ripple for voltage loop? But basically, universal PFC needs to work with 44-66Hz. If you do that way, you will probably need more filters...

Like · Reply · 2w · Edited





There is a reason the loop crossover is kept down around 1 Hz.

Like · Reply · 2w



**Arief Noor Rahman** 🗨️ Yes...it is for output voltage ripple filtering...

I am also aware with the alternative of simply using very low loop crossover...thus 100Hz ripple can be well attenuated

but, in some design reference, they presented to use notch filter, thus they can design with higher loop crossover frequency

Like · Reply · 2w



**Bob White** If you are trying to reduce the ripple voltage at the output of a single phase PFC then add more capacitance.

This is simple physics. You have an energy input that is pulsating at twice the line frequency and an energy output that is more or less constant. There will be a ripple voltage as the power from the mains varies from more or less than needed by the load.

If you want to reduce the ripple by making the power flow from the ac mains more constant then in a single phase input will increase the distortion as the current is no longer sinusoidal. There is no way around that.

Like · Reply · 2w



**Arief Noor Rahman** 🗨️ No...its not to reduce ripple...

but it is to remove the ripple from voltage feedback measurement...so the voltage loop controller doesnt try to compensate for the ripple

Like · Reply · 2w



**Bob White** Then cut the bandwidth of the control loop to a few Hz.

There has been some work in this area by Erickson and Maksimovic. If you have access to IEEE papers see, for example, "Self-tuning digital comb filter for PFC applications". You may also find the references and citations for that paper of interest.

<https://ieeexplore.ieee.org/document/1187510>



IEEEXPLORE.IEEE.ORG

Self-tuning digital comb filter for PFC applications - IEEE...



Like · Reply · 2w · Edited



**Arief Noor Rahman** 🗨️ I actually have another idea by simply calculating the notch filter constant based on real time frequency measurement, since I already employ PLL to detect grid parameter...but I am afraid if it will increase computation load too much

Like · Reply · 2w



IEEE 2002 28th Annual Conference of the Industrial Electronics Society. IECON 02

I HATE the IEEE's naming of conferences and societies so that I cannot tell what I am a member of or not.

Evidently NOT this one !

Bob White, maybe you know the difference between this paper's society and the two industrial societies I am a member of....

IEEE Industrial Electronics Society  
IEEE Industry Applications Society

It used to be, a few years ago that sometimes ieeexplore would screw up and not let me download papers that I KNOW I was supposed to be able to get.

Like · Reply · 2w · Edited



Arief Noor Rahman 🙋 I can help you download...so only this paper?

Like · Reply · 1w



Bob White Arief Noor Rahman Please do not pirate papers from the IEEE or anywhere else for that matter.

Like · Reply · 1w



Arief Noor Rahman 🙋 No worry...i am a student

Like · Reply · 1w



Write a reply...



Arief Noor Rahman 🙋 If anybody is curious about what is notch filter and how it is used in PFC voltage control loop



Like · Reply · 2w



Pablo Roberto Oliva Can you provide the link?

Like · Reply · 2w



Arief Noor Rahman 🙋 <http://www.ti.com/lit/ug/tidue54a/tidue54a.pdf>

Like · Reply · 2w



Andrew Ferencz But ... but ... the voltage ripple has harmonics and your 'fast' loop is going to respond and create more input harmonics. If you are in the digital world you can try to window the sample over a 1/2 cycle .. that puts a notch in the measurement too.

Like · Reply · 2w



Arief Noor Rahman 🙋 Sounds like a nice trick

Like · Reply · 2w



Arief Noor Rahman 🙋 Oops...not so fast, i think that approach may change the voltage loop sampling frequency, of course we can always analyze the loop response if sampling frequency change variably depends on grid frequency



**Hitesh Kumar** Arief Noor Rahman . If you are using digital control then what is the throughput of the ADC you are using?

Like · Reply · 2w



**Andrew Ferencz** Arief Noor Rahman I am more intuitive than pencil and paper mathematician. But if you average over a cycle you can know the relationship between Pin and Pout based on energy storage .. that allows an update 120 times per second. You might even be able to go with 1/4 cycles ...

Like · Reply · 2w



**Arief Noor Rahman** 🗨️ **Hitesh Kumar**, max is 3.75MSPS...but I only use it at 50ksps

Like · Reply · 1w



**Arief Noor Rahman** 🗨️ **Andrew Ferencz**, i have seen similar approach as you mentioned...that method is basically estimating ripple based on input instantaneous power...and use it to cancel the output ripple measurement

But somehow, that approach is not picked by semiconductor companies...so i assume its not as popular approach

Like · Reply · 1w



Write a reply...



**Ray Ridley** 🌟 Well, what a glorious piece of engineering that app note and board is from TI.

Has anyone played with it at all?

How far do you think that board is from something you could actually ship as a product ?

Like · Reply · 2w · Edited



**Manish Bhardwaj** **Ray Ridley** what specific issues do you see ?

Like · Reply · 2w



**Ray Ridley** 🌟 Well, starting with just the temperature ratings. Errors on the top level like that usually conceal many smaller issues below. And TI specifically warns you to do a lot of due diligence before putting such a design into a product. That doesn't mean that people are listening.

I would also bring up the input voltage rating. 265 V is the nominal +10%. Ruggedized testing should go up to 300 V input. All these corners of testing make for a lot of work, more than you can imagine.

I will reiterate: this is an amazing demo board. Years of work invested. But you can't ship it.

Like · Reply · 1w



**Arief Noor Rahman** 🗨️ Well...we normally just take the design idea, not fully copy everything we see...

Like · Reply · 1w



Write a reply...



**Ray Ridley** 🌟 Maybe I'm missing something - the working environment is spec'd at -40 degrees to +85 degrees.

However shutdown temperature is at 75 degrees.

Maybe they meant storage temperature?

Like · Reply · 2w



**Gustavo Finamor** Implement a moving average filter.

Like · Reply · 2w



pass...

Like · Reply · 1w



**Colin Tuck** Speeding up a PFC loop is fraught with interesting side effects - in the old days we had extra bits of non linear control to stop over volts ( load removal ) and undervolts ( load step applied ) - and this really helped to get the best transient performance out of the following down converter ( telecom grade ) - but as mentioned above unless you are sampling every half cycle and using that information intelligently you will create more harmonics - and weird responses for a load pulsating at a freq in the 40 - 240 Hz range ...!

Like · Reply · 1w



**Arief Noor Rahman** Hi Colin, would you mind to share what nonlinear tricks did you use?

Because I have been wondering about how standard boost PFC can deal with sudden load removal...since the converter itself is unidirectional, so it wont be able to just send back the excess bulk capacitor voltage back to the grid

Like · Reply · 1w



**Feyzullah Ertürk** You can play with damping ratio of the notch filter. Don't forget to check how much phase shift the notch filter introduces for the voltage loop. You basically have two limitations, how much dB suppression is needed "around" the double of grid frequency, and how much degree phase delay around the target voltage loop cross-over frequency you can tolerate. Perhaps eventually, these limitations will design you both voltage controller and the notch filter.

Like · Reply · 1w · Edited



**Ray Ridley** This is all fun play, for sure, and makes for happy research. Does the real product world care? Probably not. Does the real product world use the C2000? Not that I have seen.

Hopefully others can chime in and comment.

Like · Reply · 1w



**Arief Noor Rahman** I guess there is a definite reason why they are selling C2000 and still developing new product line based on it

Like · Reply · 1w



**Peter Ksiazek** Ray Ridley c2000 picollo series is used in many telecom rectifiers.

Like · Reply · 1w



**Ray Ridley** Peter Ksiazek ok cool. I just never saw those personally.

Like · Reply · 1w



Write a reply...



**Darrell Hambley** You don't really need to complicate the issue. Do what Bob suggested and lower your bandwidth to a few Hz, like 1/10th the ripple freq which is 1/5th the input freq.

Like · Reply · 1w

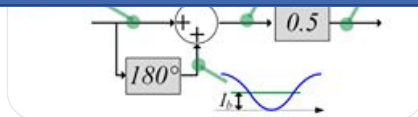


**Colin Tuck** As just mentioned above - the introduction of huge phase shift with a double notch, or 45 - 65 Hz ( Chebychev ) notch filter will cause all sorts of grief unless it is used digitally on a "look behind " basis ...

Like · Reply · 1w



**Adhistira Madhyasta Naradhipa** I am not sure this is the same or different compare to the notch filter if you open up the math. But maybe you can try something like this (The picture is for the current loop).



Like · Reply · 1w



**Arief Noor Rahman** 🗨️ Not really a notch filter...that's a ripple cancelling...

The filter to introduce that phase shift is also sensitive to frequency shifting

Like · Reply · 1w



**Col Johns** A notch filter on the 400V DC bus may not be too disastrous as the volt loop is pretty slow any way ( or should be )

Like · Reply · 1w



**Ray Ridley** 🗨️ These complex filter can get in trouble with transients in the system too. I believe that is part of the reason that simpler approaches are implemented.

Like · Reply · 1w



**Alex Berestov** One may average over half-period. Unitrode did it. The price is half-period delay.

Like · Reply · 1w



**Charlie Elliott** 🗨️ If your design is digitally based and you have a PLL anyhow then there is a really simple and effective way of doing this. Just run your voltage loop twice per mains cycle at exactly the same equivalent angle in each half cycle. Being doing this for 10+ years in grid tied inverters / AFEs!! It works a treat.

Like · Reply · 1w · Edited



**Arief Noor Rahman** 🗨️ I do have a PLL, and that's easy for me to do that, 10+ years means it really works...

so, after that...we just need to make sure that the voltage control loop is stable with 100 and 120 Hz sampling rate...

Thanks [Charlie Elliott](#)

Like · Reply · 1w



**Charlie Elliott** 🗨️ Normally I would consider that tip "secret sauce" but in the current climate I am feeling generous. Yes just set your gains of your voltage loop for low bandwidth. P+I will work a treat. No need for anything fancy although you may need an integral crowbar to prevent gross voltage overshoot if all the load can come off quickly.

Like · Reply · 1w



**Arief Noor Rahman** 🗨️ integral crowbar? is it anti-windup?

anyway, may I ask for another suggestion...in case of sudden loss of input power, is it safe to just turn off all PWM? or do we need to employ a certain turn off procedure?

Like · Reply · 1w



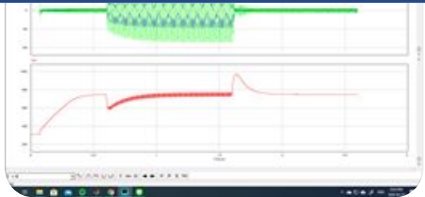
**Charlie Elliott** 🗨️ [Arief Noor Rahman](#) nope a crowbar is separate from antiwindup. In your case as your power stage is 4 quadrant you may not need it if you allow bidirectional power flow.

Like · Reply · 1w



**Arief Noor Rahman** 🗨️ [Charlie Elliott](#), thanks a lot for your suggestion...I have managed to perform the close loop simulation

excellent suggestion!



Like · Reply · 1w · Edited

Write a reply...

Andrew Ferencz Okay - here's an idea that I haven't seen implemented. Maybe it will help somebody get a thesis going. Most PFC's use a transconductance approach - multiply the voltage by a constant to get a current reference. But that has a few issues around surge voltage (big voltage = big current) .. what you really want is a moving power number, Sin^2. That way your current is really power/voltage and you get an nice feedforward term. Now being secluded in my lab I don't know if this ever pursued but with digital controllers - piece of cake.

Like · Reply · 1w

Arief Noor Rahman I am not even implementing it that way... I am using dq-frame theory that is originated from three phase control theory... I prefer this approach because I have started from three phase design before, thus I already mostly already understand well enough... Added benefit is, the control structure I use work for bidirectional power flow, down side is, it must be used with totem pole PFC

Like · Reply · 1w

Andrew Ferencz I just did a totem pole .. critical is a good dead band near zero!!!

Like · Reply · 1w

Arief Noor Rahman I just had a discussion with my friend who recently finished their project on totempole PFC with standard approach...which they need to pay special care near zero crossing... When I disussed with him, I said, in my simulation with dq frame, I just applied unipolar SPWM anf I dont even need to care about zero crossing and I didnt see any distortion... According to my friend, standard control method the distortion and spike also appears in simulation...I hope it really work well in real hardware, because the control code is much much simpler than the common approach

Like · Reply · 1w

John Bailie is feeling silly. March 23 at 12:53 PM

Is it really possible to patent a DC grid?

https://patents.google.com/patent/US20150333512A1/en

PATENTS.GOOGLE.COM US20150333512A1 - Charging and Discharging of DC Microgrid Energy Storage - Google Patents A DC building electrical system includes a DC power consuming device connected to a DC...

You and 4 others 17 Comments



Stuart Wood The patent system at its worst.

Like · Reply · 1w

**Scott Styles** we can't really discuss the patent system w/o swearing and that isn't allowed here....

Like · Reply · 1w



**Alain Laprade** Here's a thought. DC links are frequently used between power grids. Sorry Robert Bosch, we ain't paying up and we're shutting down the grid to your factories. Hoot!

Like · Reply · 1w



**Manuel Escudero Rodríguez** They are targeting Energy Storage Systems feed from an AC grid and supplying a local DC grid, not the DC grid itself.

Like · Reply · 1w



**John Baillie** This sounds like an UPS if you consider the dc link the dc grid

Like · Reply · 1w



**Andrew Ferencz** You can patent a resistor if you know how to write it, pay a lawyer, and accept their feedback.

Like · Reply · 1w



**Simopekka Niskanen** Wow, Edison is back, DC-link!!!

Like · Reply · 1w



**Venkat Karthik** I think Bosch wants to power up all the equipment's from DC ( 380V) <https://www.aeesocal.org/.../95-bosch-dc-power...>

Like · Reply · 1w



**John Baillie** Venkat Karthik thanks for link!

Like · Reply · 1w



**Joanna McLellan** They tried to patent a parasitic capacitor a few years back.

Like · Reply · 1w



**Alex Berestov** Tube cascode connection was patented in 21st century.

DC link is well known in IBM power distribution model, just for instance. Moreover there are a lot of DC circuit breakers on avail. P.S. Everybody heard about patent trolls. Just means competition between two parties and, guess what, not pursue of a factual deed(s).

One 19th century lawyer in Russia was winning cases on a bet, just for fun, just because he was persuasive enough for an ordinary juror.

Like · Reply · 1w · Edited



**John Baillie** Alex Berestov is your comment about dc breakers saying there are lots of them?

Like · Reply · 1w



**Alex Berestov** Yep, I used to use them in hot swap bidir ac-ac.

Like · Reply · 1w



**Alberto Bianco** That's just a patent application, what will come out of the patent examination is yet to be known.

Like · Reply · 1w



**Stuart Wood** Alberto Bianco no that was issued in 2018

Like · Reply · 1w

of first to file, which encourages companies to patent first and sort it out later. This patent is very specific, and with all the dependent claims, very narrow, right down to the emergency lighting load.

Like · Reply · 1w



**Alex Berestov** That's the point. Patent initially was a document about exclusive rights on something. Technical issues to be resolved in a court - priceless. Experts could be biased but jurors could not - they have to know nothing on the matter to be just.

Like · Reply · 1w



Write a comment  
**Frode Sørensen** shared a link.  
March 19 at 12:15 PM

How to decide the air gap for active clamp forward converter transformer?

I am designing my first transformer for this topology, and is right now very puzzled when it comes to the required length of the air gap. I have googled and read a lot of application notes, and did find close to nothing about it. I understand that the gapping is important to avoid core saturation during load steps (see ref below). My questions are what could be an appropriate length of the air gap? How can it be found? Anyone having experience with AC-FW transformer and air gap?

The DCDC specifications are: Vin 18V-32V, Out 5V/12A, f(sw) 400kHz.

Other: Low EMI, and high efficiency is desirable. Controller TI UCC2897A.

Ref. Design Considerations for Active Clamp and Reset Technique

<https://www.ti.com/seclit/ml/slup112/slup112.pdf>

Highlight from this appnote: , transformers for active clamp circuits are usually gapped in order to reduce the magnetizing inductance. If the transformer is not gapped, there is no impact on steady state operation of the active reset circuit, but the soft transition is difficult to achieve and the transformer is more exposed to the possibility of saturation under transient conditions.

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1

35 Comments

Like

Comment



**Youssef Ka** To my knowledge, magnetics design is very customized. It means you need to define your boundaries e.g. the magnetic material, the core shape, winding structure. Then, you can make a mathematical model that include all dimensions you have, so you can adjust the air gap to get the desired magnetizing inductance.

Like · Reply · 2w



**Frode Sørensen** I am not worried about the other design parameters. I have RidleyWorks available for the magnetic design, and have used it for several custom flyback transformers with luck. So I am able to simulate the transformer for different cores and materials.

Like · Reply · 2w



**David Edwards** ☹️ The air gap allows the core to passively reset to a low residual flux (which only requires a small gap). Exact gap length is not critical as long as it is smallish (avoids gap fringing loss and excessive magnetizing current).

Like · Reply · 2w



gap is needed for core reset - core reset simply requires a long enough OFF time for the V.sec to be equal and opposite to reset the soft ferrite to near B=0 ( there will be some remenance ) - the gap is most often used in a fwd converter as an ad-hoc means of reducing flux stair casing - where current mode is not employed ...

Like · Reply · 2w · Edited

**Frode Sørengen** Col Johns My mistake core reset. I know that the gap is not needed for core reset. According to the old unitrode appnote (slup112, see link above) is the air gap in active-clamp forward included because soft transition is difficult to achieve and the transformer is more exposed to the possibility of saturation under transient conditions.

Like · Reply · 2w

**Frode Sørengen** That's good to hear. I did not want any big air-gap that reduces the AL value more than necessary. Because I want to use as the smallest core as possible, and do not want to increase the number of turns due to low AL, or use a larger core.

Like · Reply · 2w

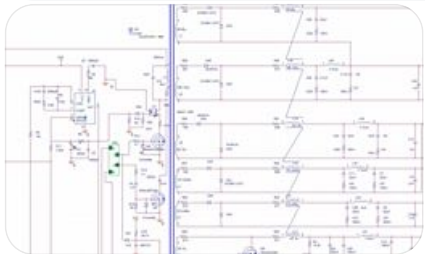
**Chris Merren** Most of those Unitrode articles are based off fantasy.... Some articles are legit...but many of the article talk about things that the author has never built or experienced, since many of these concepts sound great on paper but do not really work in reality.... I have designed and built many Forward Active clamp transformers and can tell you that non of them are gaped and they have worked for over 20 years and are still presently working somewhere in space and other harsh environments... As the other post mentioned, that if your in Current Mode, you should be fine from any stair-casing issue...

Like · Reply · 2w

**Frode Sørengen** Chris Merren 🙌 Fantastic, I am of course using current mode. Basically I have wasted my time about this air-gap thing. But it is always good to have it clarified.

Like · Reply · 2w

**Chris Merren** Frode Sørengen Air-Gap on a Forward Converter will unnecessarily increase the Magnetizing Current... Let me find my design notes... If you were to plot the BH loops during actual run-time of a Current-Mode converter you will see some cool stuff... For example the BH loop looks like a Balloon shape when driven by Square waves... Also you never really start back at the "origin" with Current Mode like the text book mentions... The core will always stair-case to one side and always be on the "verge" of saturating..... But the current Feed-Back loop keeps it from going into saturation....so it rides on the edge of saturation...



Like · Reply · 2w · Edited

**Frode Sørengen** Chris Merren Very good. My experience is that it is relatively little relevant information about active-clamp forward to find, so this is definitively useful. I have spent quite a bit of time understanding this converter since I am in a project where it is possible to use time to learn, something that doesn't happen very often.

Like · Reply · 2w

Write a reply... [emojis]



Air gap for Current mode. Most of the TI ics for active clamp uses Current mode. I had designed active Clamp Forward with Onsemi Voltage mode ics. Unlike Current Mode, Line feed forward becomes crucial to prevent saturation during Transient loads. This reference design document was designed by me over a decade back for Onsemi <https://www.onsemi.com/pub/Collateral/TND331-D.PDF>



TI.COM

Analog, Embedded Processing,  
Semiconductor Company, Texas...



Like · Reply · 2w · Edited



**Frode Sørensen** This contributes well to my understanding of active-clamp forward now

Like · Reply · 2w



**Ray Ridley** 1) Decide the inductance you want for the resonant reset.

2) Gap the core until you read that value

3) Don't look to TI for magnetics advice. No more than you should look to us for semiconductor fab advice.

Voltage-mode or current-mode should not affect the gap decision.

Like · Reply · 2w



**Chris Merren** With the available gaps and the max flux swing to work in, this is not always feasible... Much easier to adjust the capacitor ..

Like · Reply · 1w



**Darrell Hambley** Current mode has nothing to do with it. Neither does "working for 20 years". For a active clamp forward converter, the flux swing from peak flux to residual flux is greater when there is a gap, therefore you can benefit from a larger volt-seconds during reset. This allows you to design with a smaller core area.

Like · Reply · 2w



**Colin Tuck**  $dB/dt = V/N.Ae$  or  $V.dt = dB.N.Ae$

notice there is no dependence on gap ...

gap sets the  $L_{mag}$ , for more flux swing you must go two quadrant resonant fwd operation ...

If you open the gap, the  $L_{mag}$  goes down, for the same applied PWM ( volt.sec ) the current goes up to achieve the same flux as before with the lower current and no gap ...

taking the core out completely, same volt.sec gives same flux - but unlikely a standard circuit can supply the current necessary for this - the assumption is voltage source drive ...

Like · Reply · 1w · Edited



1

^ Hide 13 Replies



**Chris Merren** Agreed..regarding AC flux density... Bsat is not changed with Gap.... The Gap does DECREASE the DC Flux Density in the event you have some residual DC offset...

Like · Reply · 1w



**Colin Tuck** **Chris Merren** Not only Bsat - but Bpk, are you assuming the remanence changes with a gap ( Br ) ? I cannot see any physics based reason for this...(?)

The gap does increase the required H to get to design Bpk.

Like · Reply · 1w



curvature of BH loop prior to Bsat...At the expense of increased H .... Bsat will remain the same.....In real life using the typical ferrite materials found in SMPS. I rarely found it worth that little bit more flux vs increased magnetizing current and increased core loss.... Regarding DC flux density... The bigger the gap the lower the DC flux density.. There are cases where there is always a small DC offset...this offset DC flux sums with the AC flux and can sometimes push it over the edge.... A properly calculated gap can help in those cases..

Like · Reply · 1w · Edited



**Col Johns** how do you get this little bit more flux swing? the Bsat is the same, more flux swing ( more V.sec traversed ) means more hysteresis losses - full stop.

Like · Reply · 1w · Edited



**Chris Merren** Col Johns The curvature or knee under Bsat before you get to the Bsat becomes linearized and a bit straighten out with increased air-gap.. This allows a tiny bit more usable flux swing to be utilized that would otherwise be non-usable....figure another 50 to 100mT at most....if your really squeezed in a tight design....

Like · Reply · 1w · Edited



**Colin Tuck** Chris Merren - only with more core losses - you do not get a free lunch... the hysteresis curve of the actual ferrite does not change - just the overall including the gap - the BH loop is skewed laterally - a given B now requires more H - but traversing a higher B gives more hys losses ... unfortunately...

Like · Reply · 1w · Edited



**Chris Merren** Colin Tuck Yes....agreed, no free lunch... That is why I don't bother gaping in these situations...

Like · Reply · 1w



**Frode Sørensen** I have a feeling I now understand why (usually) not gap active-clamp forward transformers. Of course do the current ripple increase when gap. But I have also been simulated a little with RidleyWorks, I see that core loss is quite "high" if it is "close" to Bsat (0.25T). When lowering a little the core loss decrease quite a bit.

Like · Reply · 1w



**Colin Tuck** Frode Sørensen 100mT at 100kHz is probably running a core at the high end depending on cooling available ...

Like · Reply · 1w



**Chris Merren** Colin Tuck I am not sure what material you are referring to but a typical "run of the mill" Ferrite material for SMPS is 3C92 or 3C96 ...Bsat @100C @10kH around 440mT .... I operate them around 250mT to 300mT ..

Like · Reply · 1w



**Col Johns** Chris Merren at 10kHz that's fine ...

Like · Reply · 1w



**Frode Sørensen** I was simulating with 3C90 operated at 250mT, 400kHz. Lowering to around 200mT helped a lot. Maybe it is also because the switching frequency is a little high. But I prefer to downsize the footprint also.

Like · Reply · 1w




**Col Johns** I would be keen to learn the surface temp of the ferrite after an hour or so at 400kHz at 200mT peak? 400 LFM anyone ..?

Like · Reply · 1w

Write a reply...



**David Edwards** 📖 A forward converter transformer gap lowers the transformer's residual flux level when there is only passive reset. Active reset (if designed right) will reset the core to zero or negative flux values.

Like · Reply · 1w  2

**Col Johns** Really - how exactly does this magic occur...? - the extra reset with a gap that is ...

Like · Reply · 1w · Edited

**Ray Ridley** 🤖 It's magnetics, nobody knows... unless they have been to one of our courses. 😊

Like · Reply · 1w

**Col Johns** **Ray Ridley** - well they may well be put straight at such a course - which is a good thing - there is so much assumed "knowledge" out there that is only tangentially related to physics at best ...






Like · Reply · 1w






**Darrell Hambley** Wow Dave. It's apparent that many people have never seen or, maybe never thought about, the effect of a gap on a BH curve!


Like · Reply · 1w

**Chris Merren** **Darrell Hambley** The best way to learn this concept is to actually build your transformer and plot the BH loops...then incrementally increase GAP and remeasure BH loop ...over and over till yo get to asymptotic Bs<sub>at</sub>..... I did this as a teenager...This way you can visually see the trend in the curves and the concept is the much easier to grasp..Then keep working the equations till you see the mathematical series...It follows 1/coth behavior... Once you have empirical equations worked out, you can then use these equations for some spot on design work...

Like · Reply · 1w · Edited

 Write a reply...    

 Write a comment...    

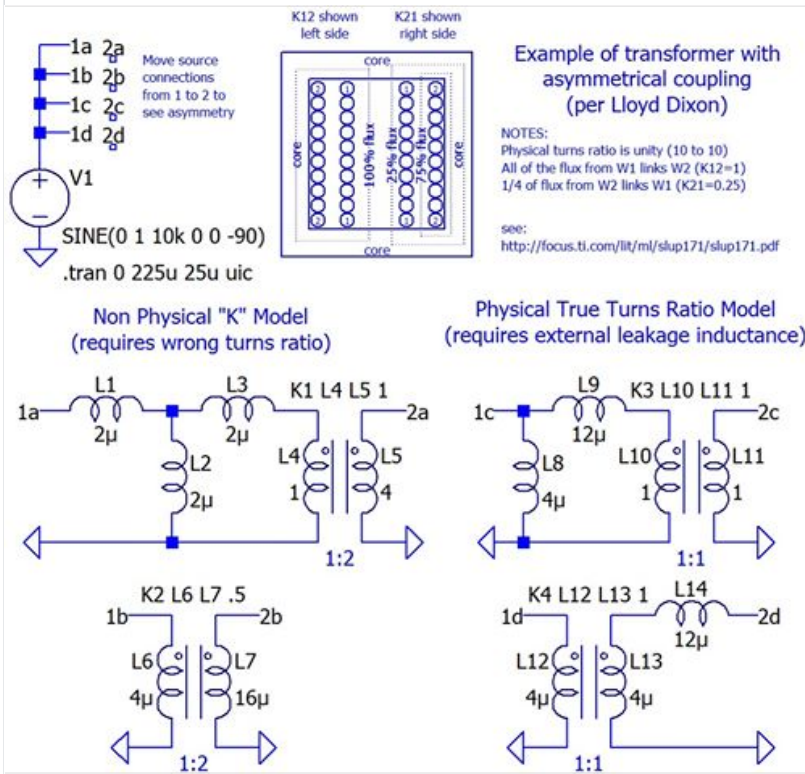
 **David Edwards** Conversation Starter · March 23 at 12:35 AM

**Transformer Asymmetrical Leakage Inductance**

The non-ideal two winding transformer problem has more degrees of freedom than variables, so one can describe the system in multiple ways. In my opinion, it is best (most intuitive) to fix the electrical turns ratio,  $N$ , to be equal to the physical turns ratio. With that assumption there is only one solution, then the coupled portion of the windings should be taken to be perfectly coupled and the leakage portions of the windings should each be represented separately as two entirely non-coupled inductances.

In order to arbitrarily represent the leakage inductance entirely on one or the other side of a two winding transformer, it is generally necessary to adjust  $N$  to a ratio not equal to the physical turns ratio, but doing so obfuscates rather than illuminates the physical/electrical relationships involved.

electrical turns ratio is fixed to the physical turns ratio. However, with some forethought and effort, one can construct a physical transformer with nearly perfect leakage asymmetry such that all of the leakage appears in series with one winding only (again assuming that N in the model is fixed to be equal to the physical turns ratio).



13 10 Comments

Like Comment

**Hamish Laird** David Edwards for three winding and more transformers there is significant meaning and physical effects of where you put the leakage. Really important in thyristor converters.

**Col Johns** Widely separated pri & sec wdgs is a corner case - rarely encountered or intended in a switch mode power circuit ...

**Mike Tommasi** Not so rare

**David Edwards** This effect, less pronounced, is common in center gapped fly back transformers.

**Col Johns** David Edwards only if the pri and sec are widely separated ... most power converters seek good coupling not poor ....

Write a reply...

**Alex Berestov** What about LLC?

**David Edwards** LLC is immaterial to the purpose of my post, which is to demonstrate how asymmetrical leakage inductance may arise with asymmetrical winding structures.

construction.

Like · Reply · 1w

David Edwards 🍷 Col Johns Fair enough.

Like · Reply · 1w

Write a reply...

Kevin Azul



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Ray Ridley Admin · March 24 at 8:17 PM



10

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John Baillie shared a link. March 19 at 6:07 AM

I guess like many others from my generation, the practical education I received at school and university was close to negligible. Thankfully there's Youtube and people spending their time making really helpful videos. This channel isn't about power electronics or even electronics, but has provided me with great tips for those everyday mechanical questions that we have. What else do people value? <https://www.youtube.com/watch?v=bkrUzGooA9k>