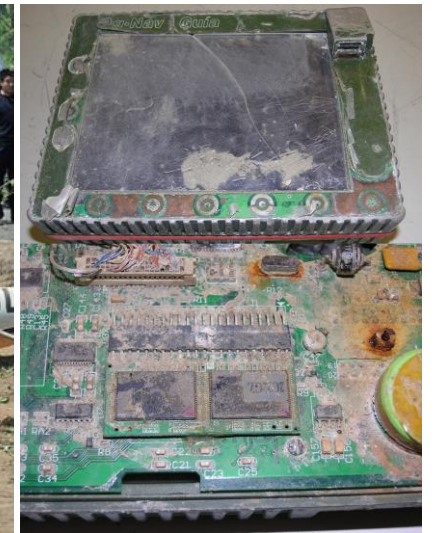
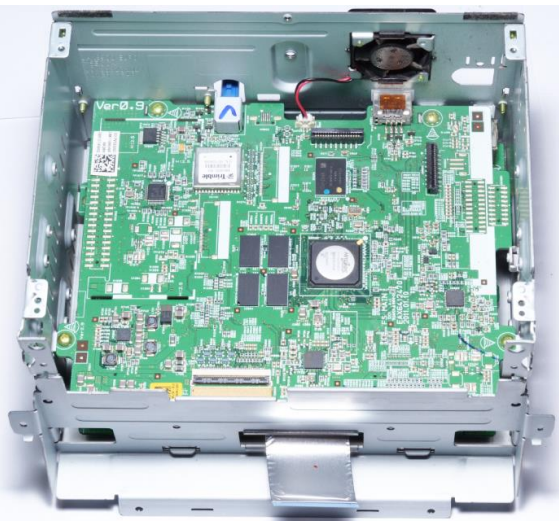
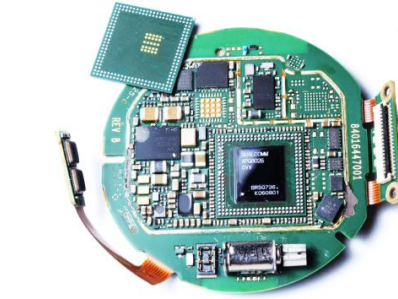
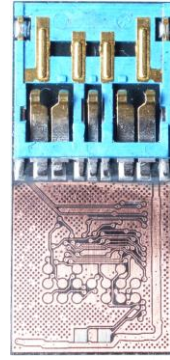
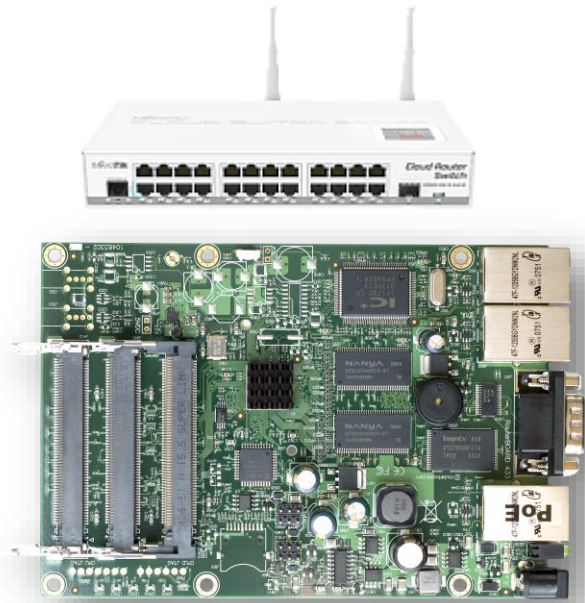


Forensic analysis of flash memory using X-RAY and Logic Analyzer

Rusolut, Poland

EMBEDDED DEVICES



DIGITAL FORENSICS IS FAR BEHIND THE MODERN TECH

- It's not just computer or mobile forensics anymore.
- The digital and IoT evolution is extremely rapid.
- Tons of digital evidence is missed/ignored
- HW vendors are not obliged to cooperate and they usually don't
- Modern hardware is "multi-layered", so multiple vendors involved
- Reverse engineering is by far one of the very few solutions

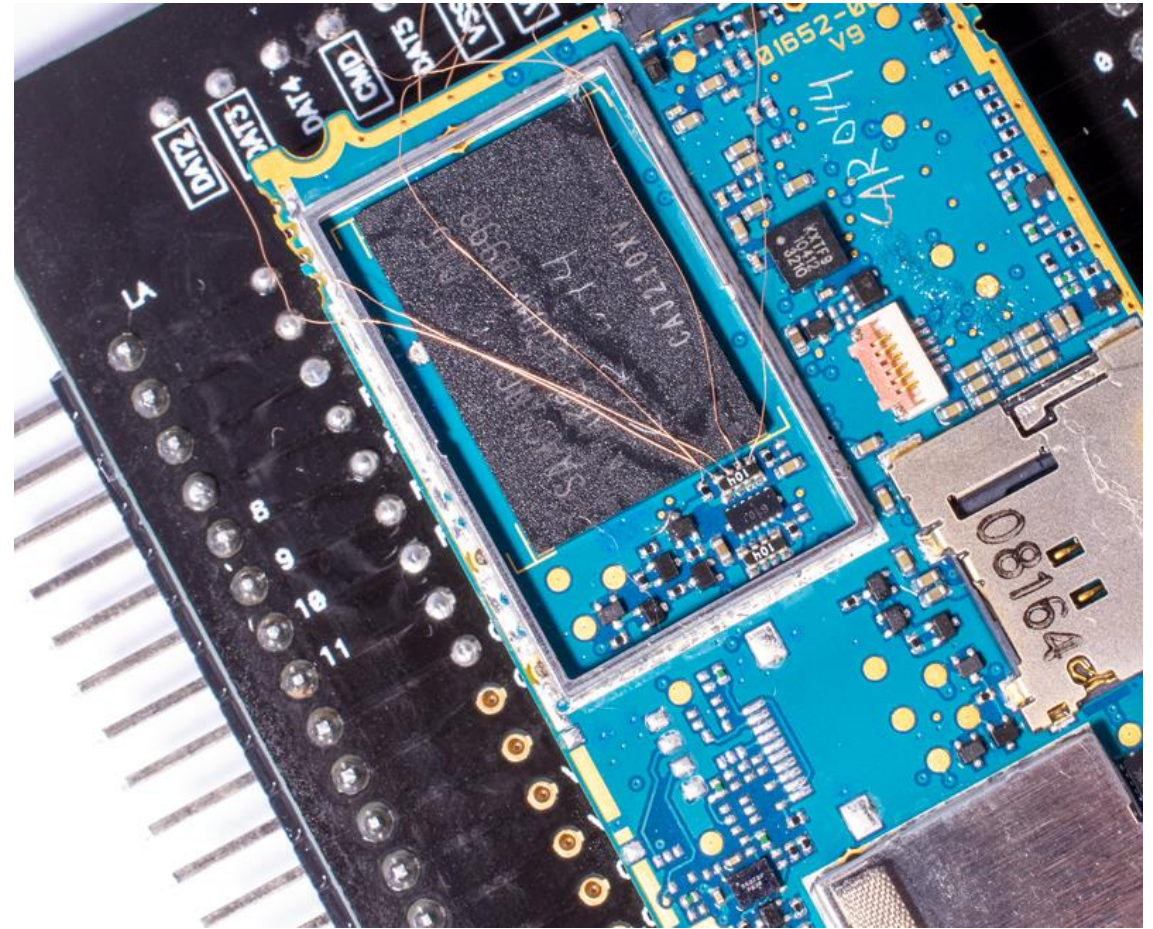
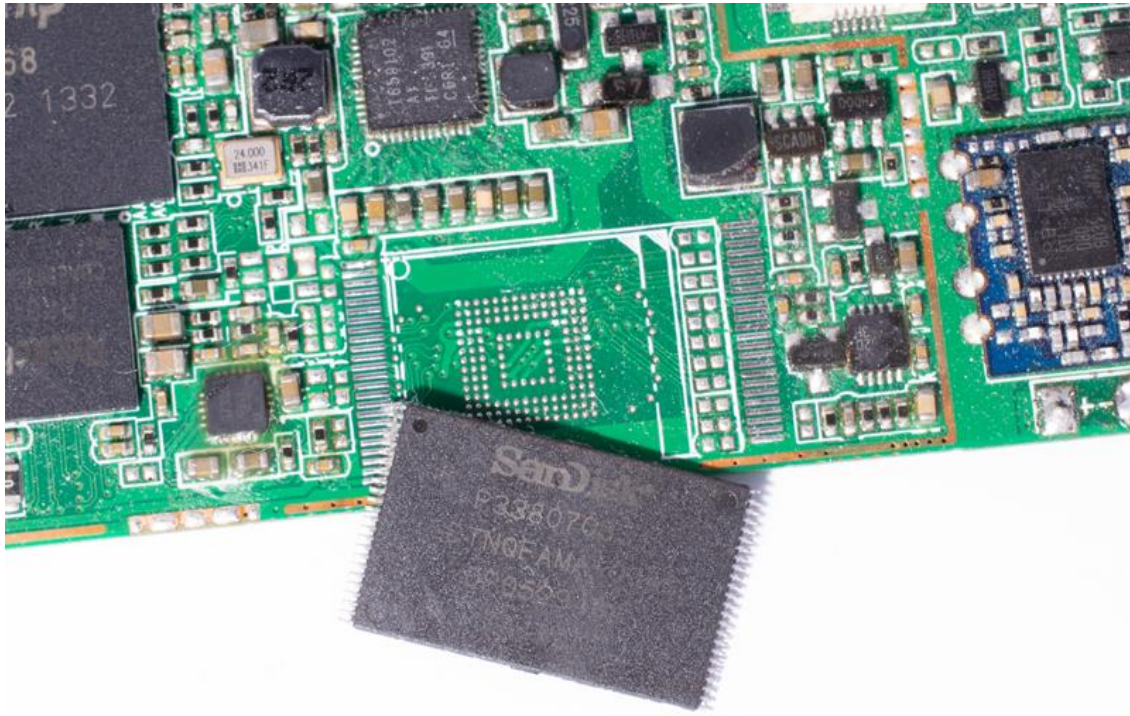
IN MOST EMBEDDED DEVICES DATA STORED IN NON-VOLATILE FLASH MEMORY

- Serial Flash, FeRAM (SPI, I2C interfaces)
- Parallel NOR/NAND flash (CFI interface)
- **NAND flash (NAND interface)**

WHEN DATA EXTRACTION DIRECTLY FROM MEMORY CHIP IS THE ONLY SOLUTION?

- Devices where standard interface isn't working/disabled
- Physically broken devices
- Non-working devices/corrupted FW
- Embedded devices w/o external interface
- Proprietary interface
- Extraction of erased data
- Locked eMMC chips and SD cards

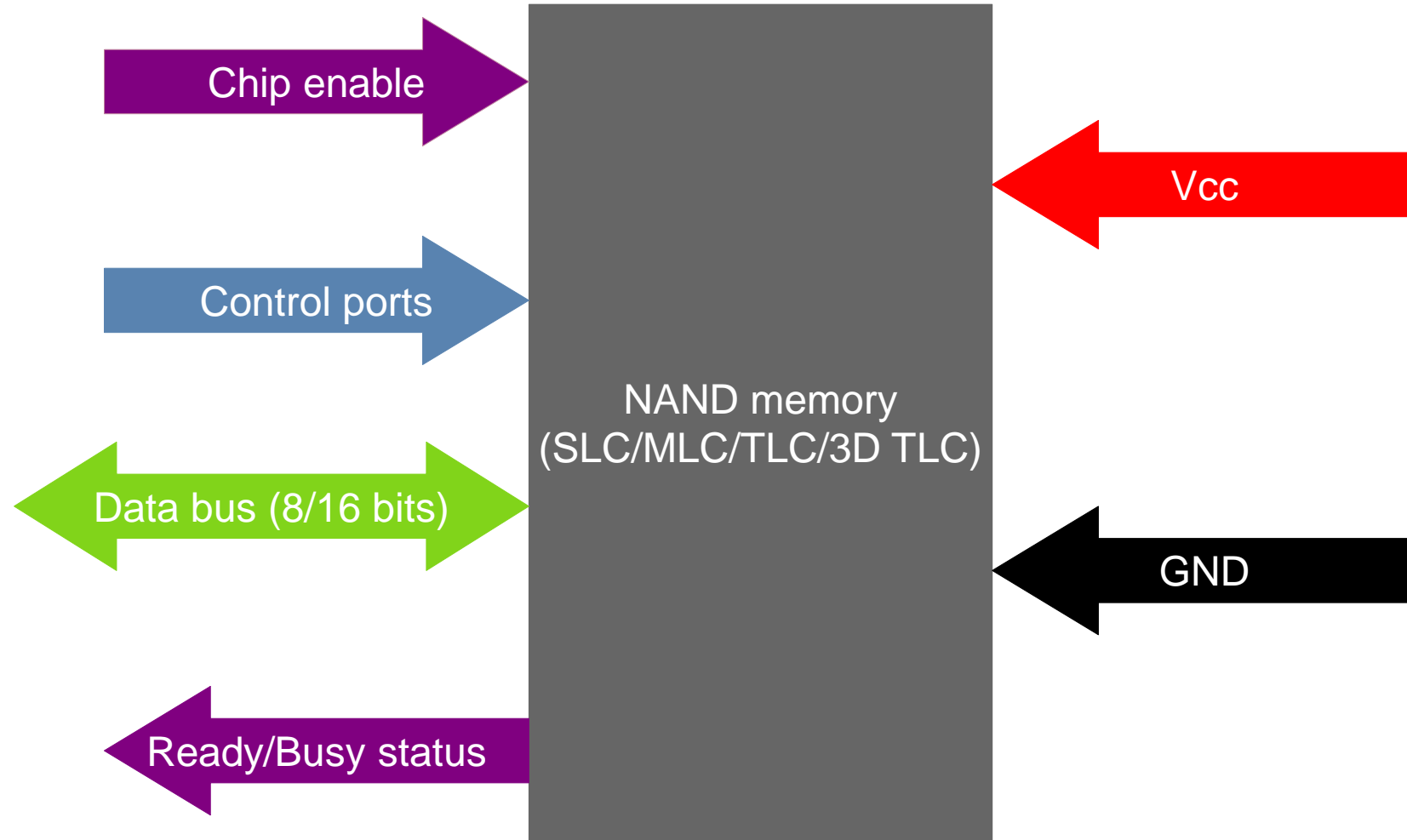
DIRECT FLASH MEMORY ACCESS CHIP-OFF OR ON-CHIP



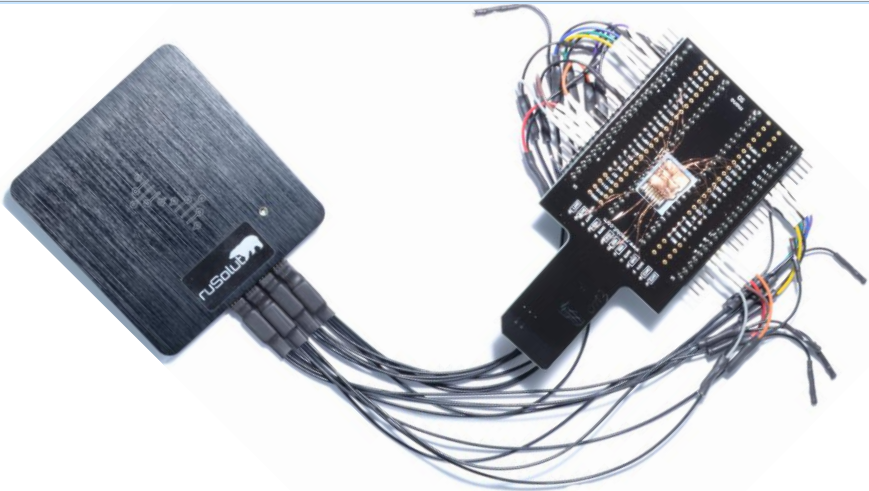
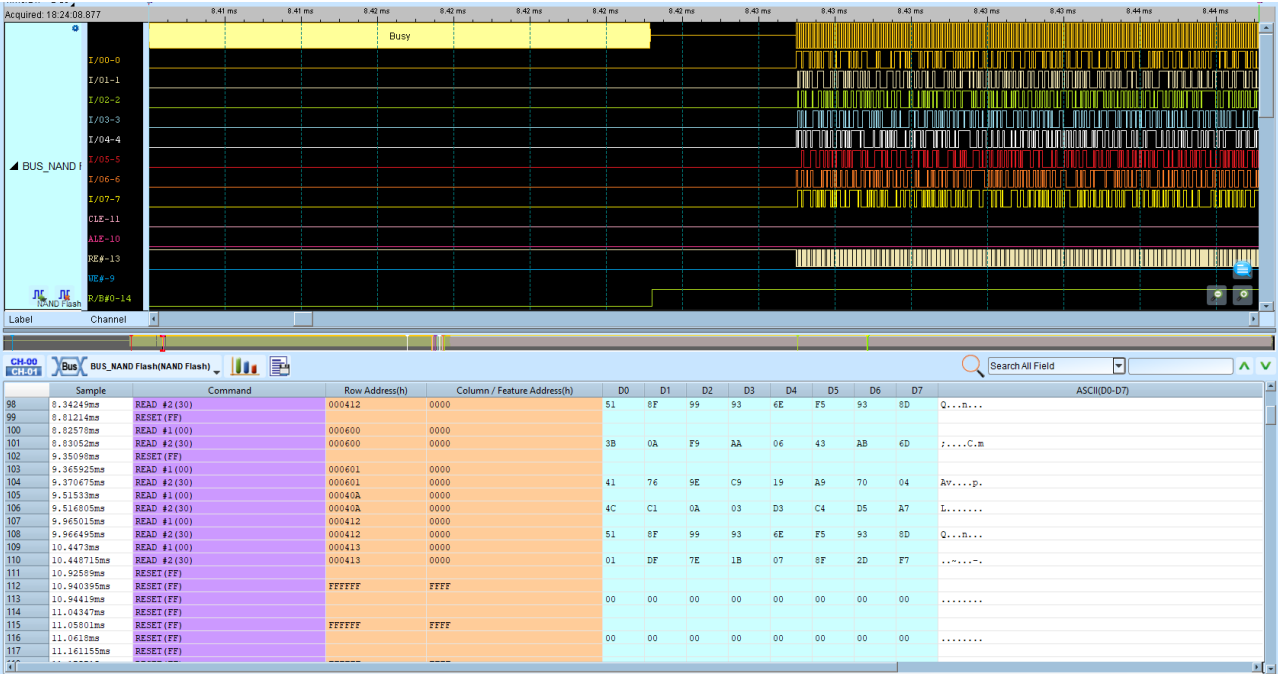
NOT ALL CHIPS ARE SAME
HOW TO READ THEM ALL?



NAND INTERFACE

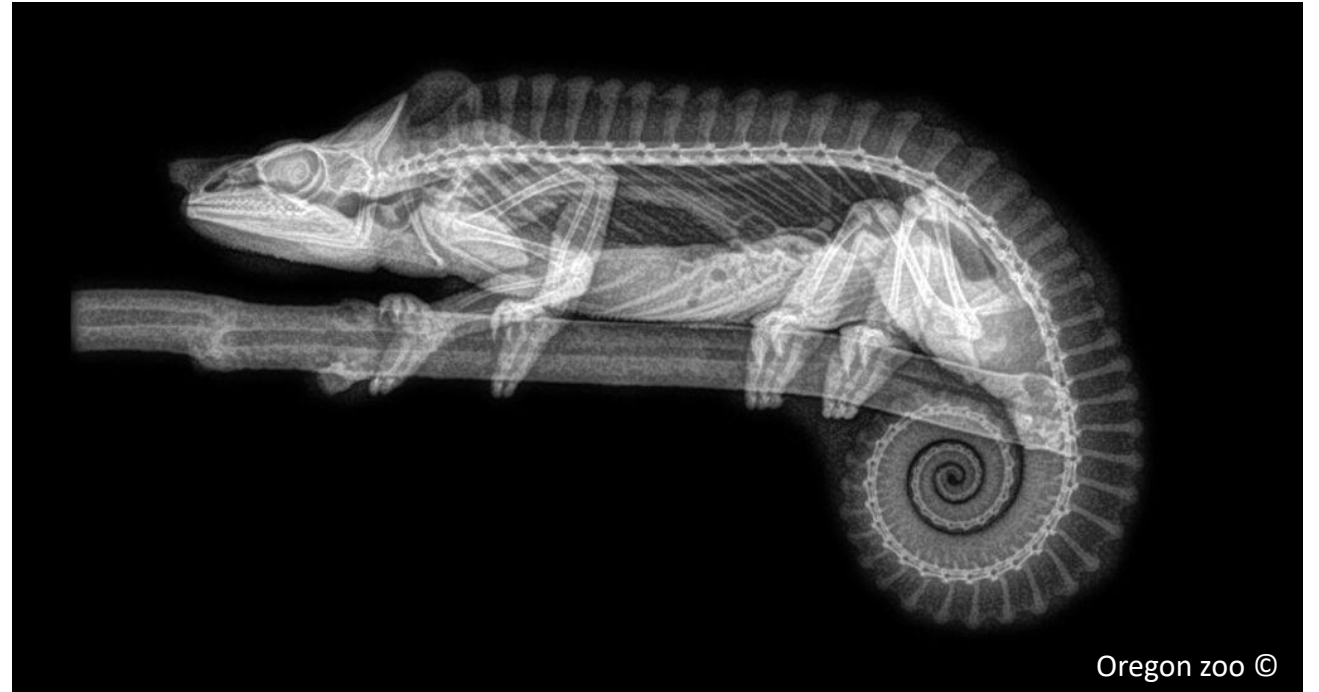


LOGIC ANALYZER & XRAY

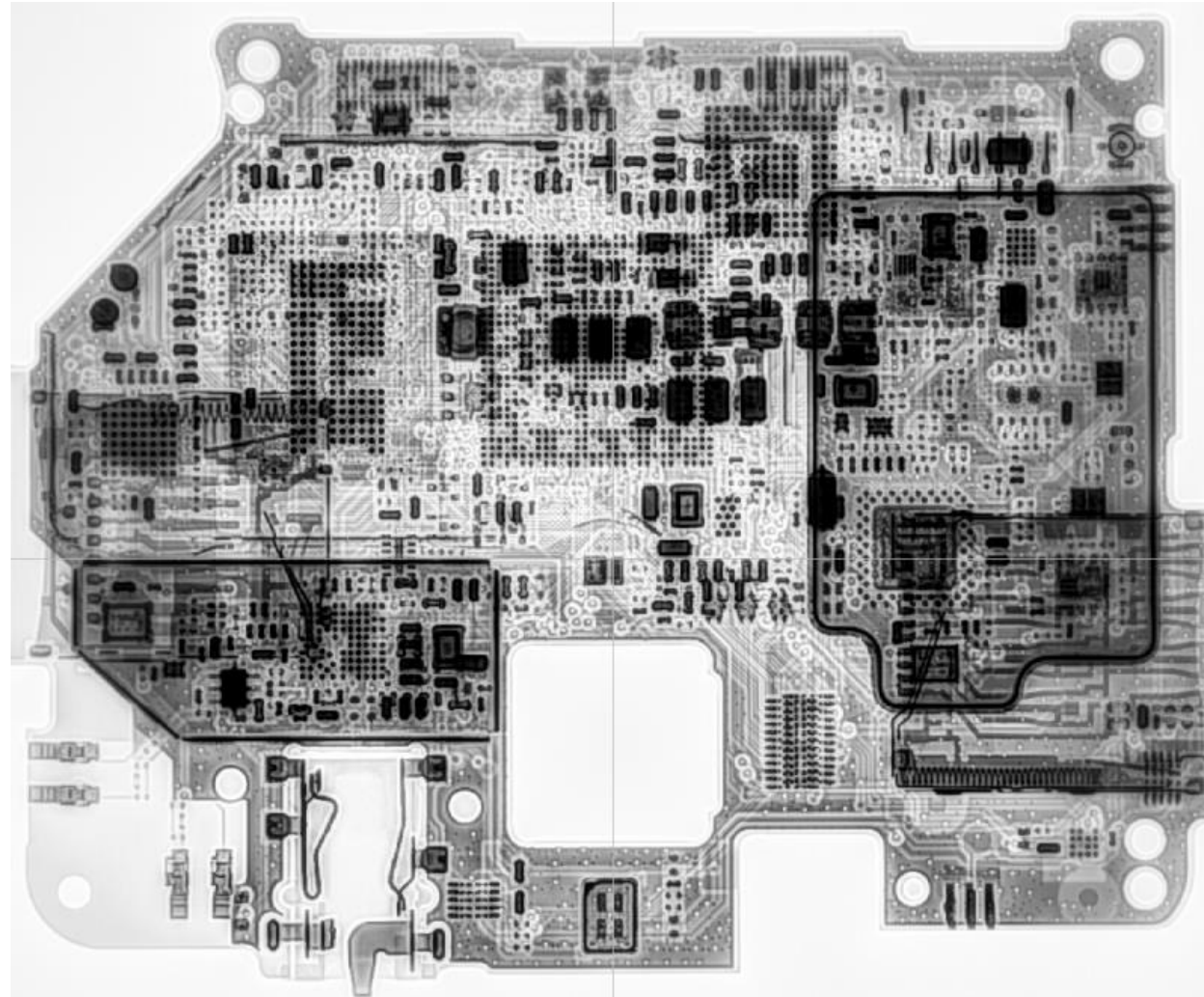


WHAT CAN YOU DO WITH XRAY?

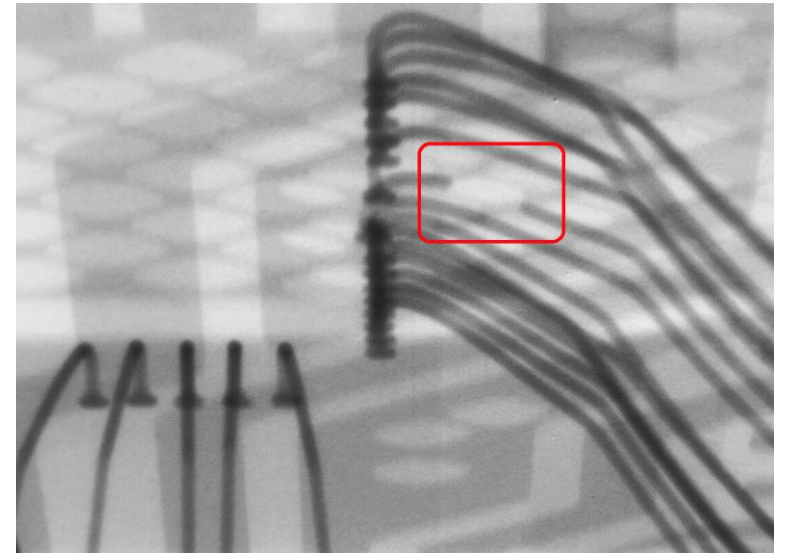
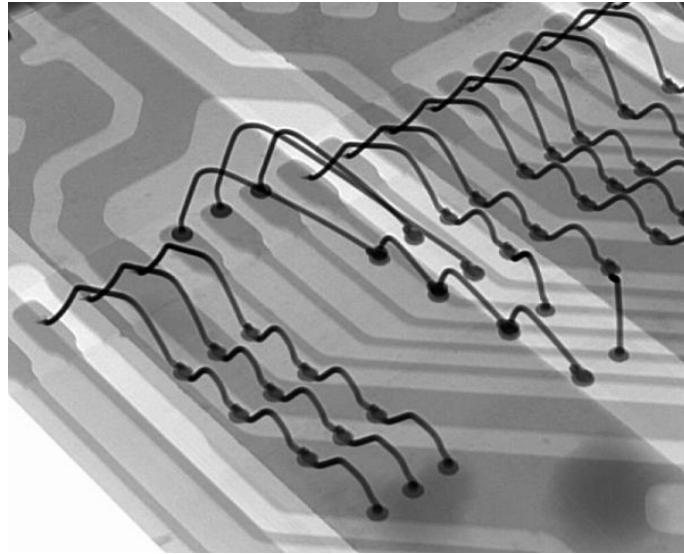
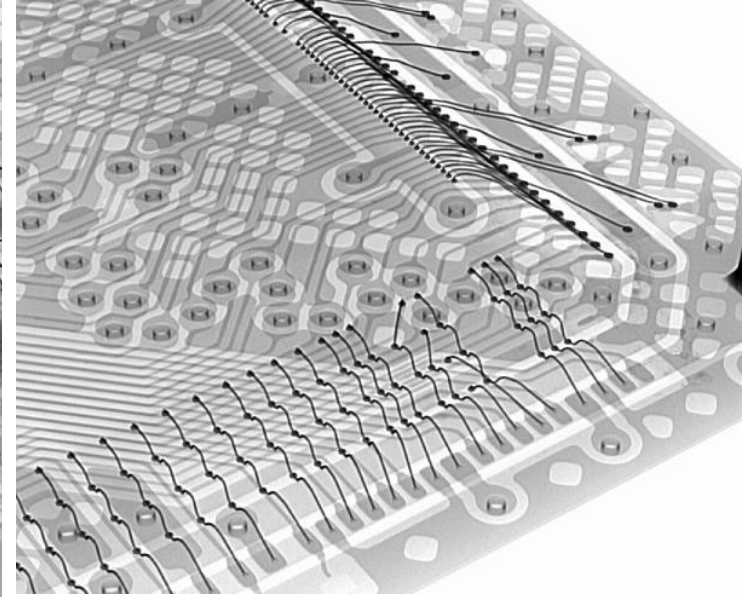
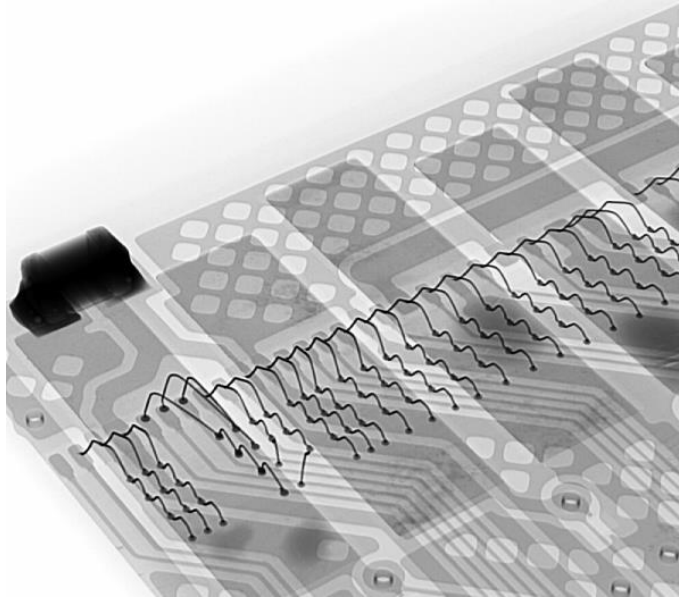
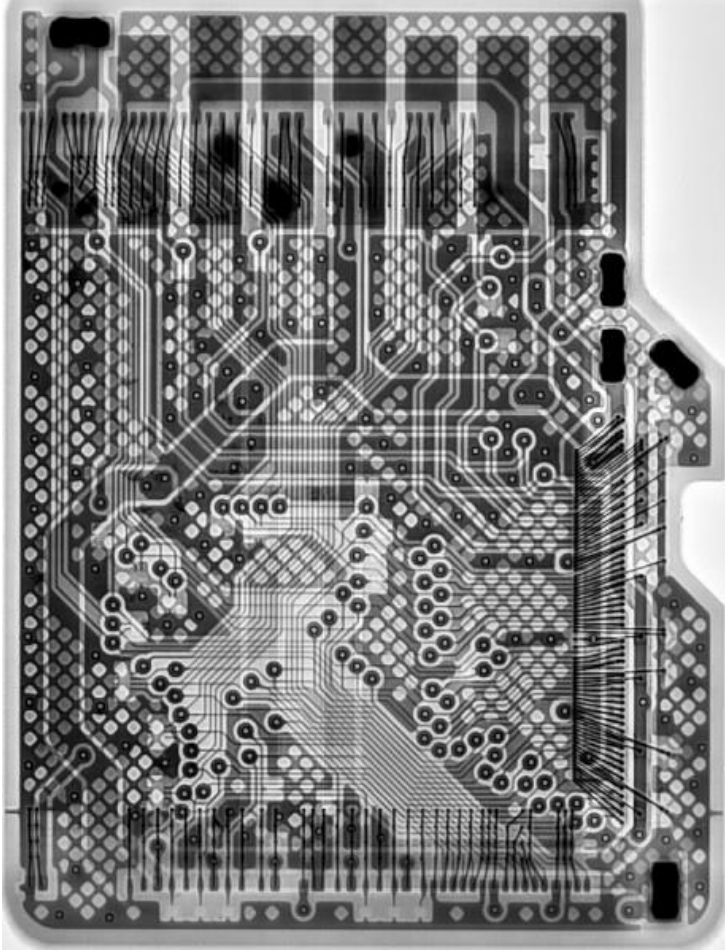
- Structural analysis of device
- Damage assessment
- PCB-to-chip analysis of traces
- **Helps to build flash memory pinout**



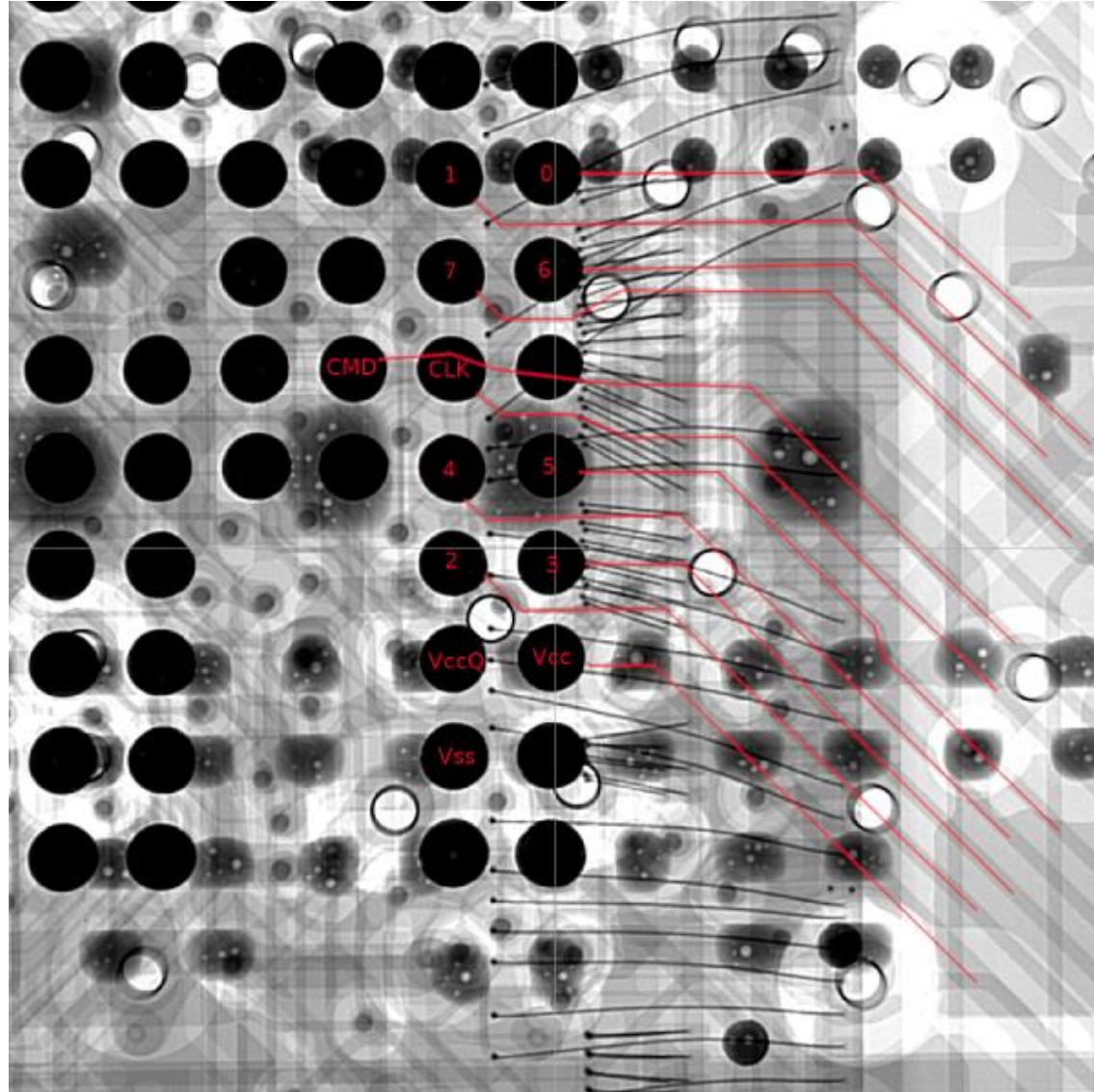
STRUCTURAL ANALYSIS OF DEVICE



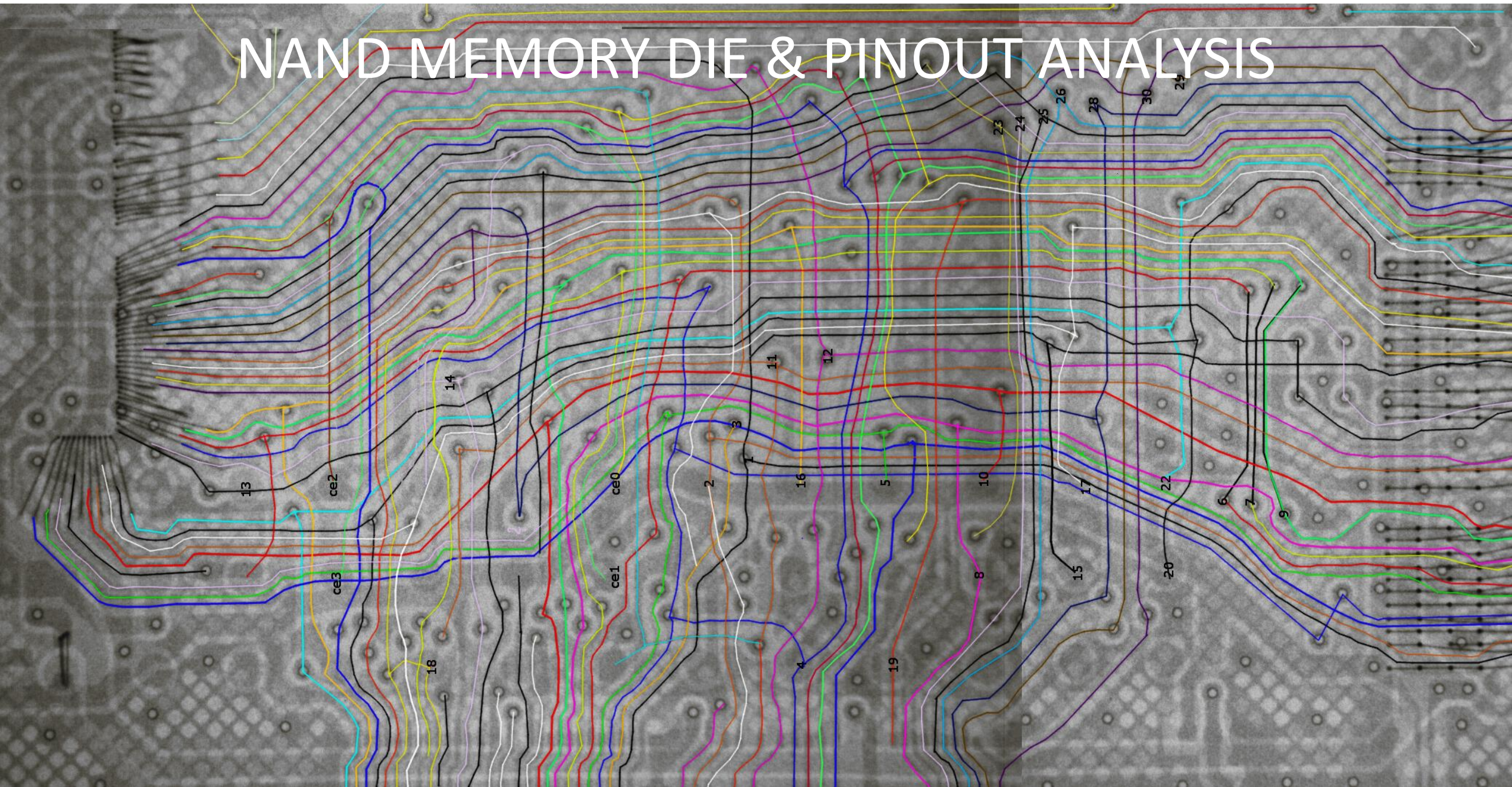
DAMAGE ASSESSMENT



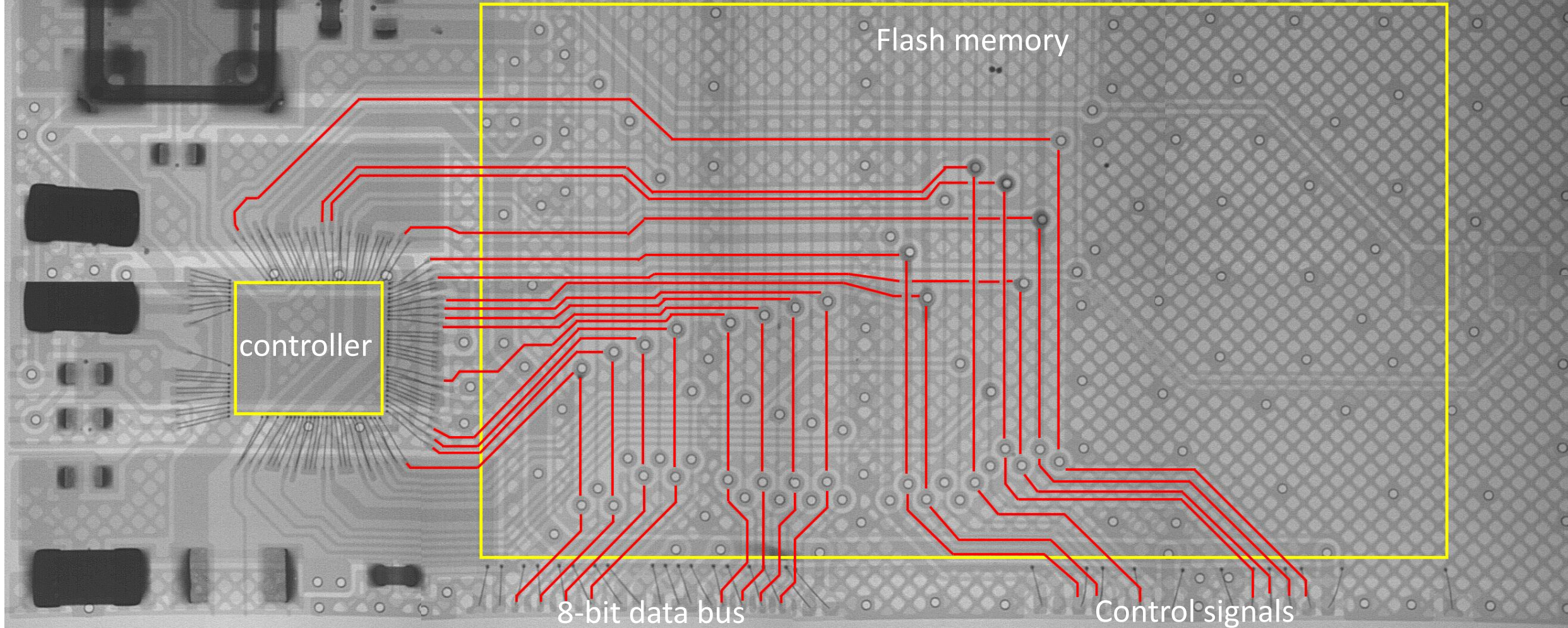
PCB-CHIP ANALYSIS OF MEMORY TRACES



NAND MEMORY DIE & PINOUT ANALYSIS



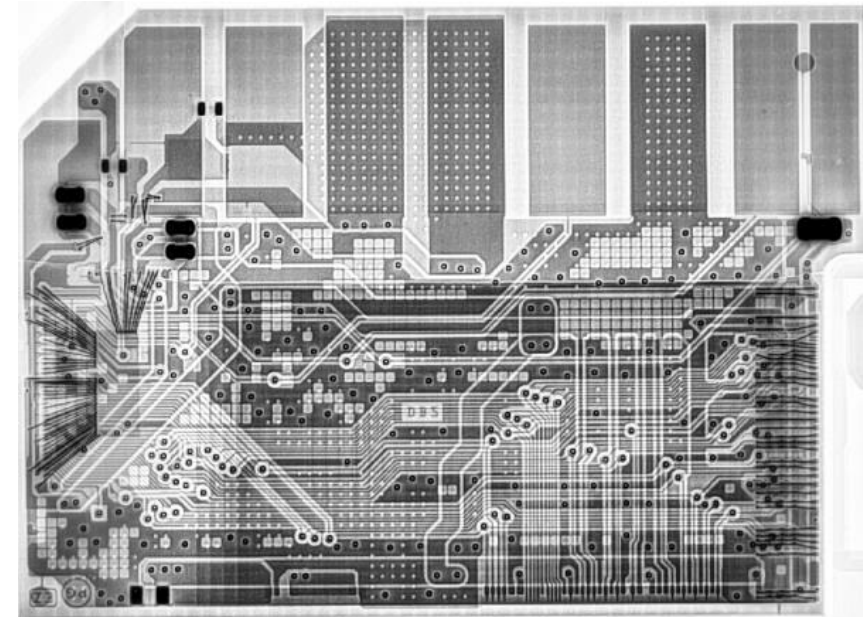
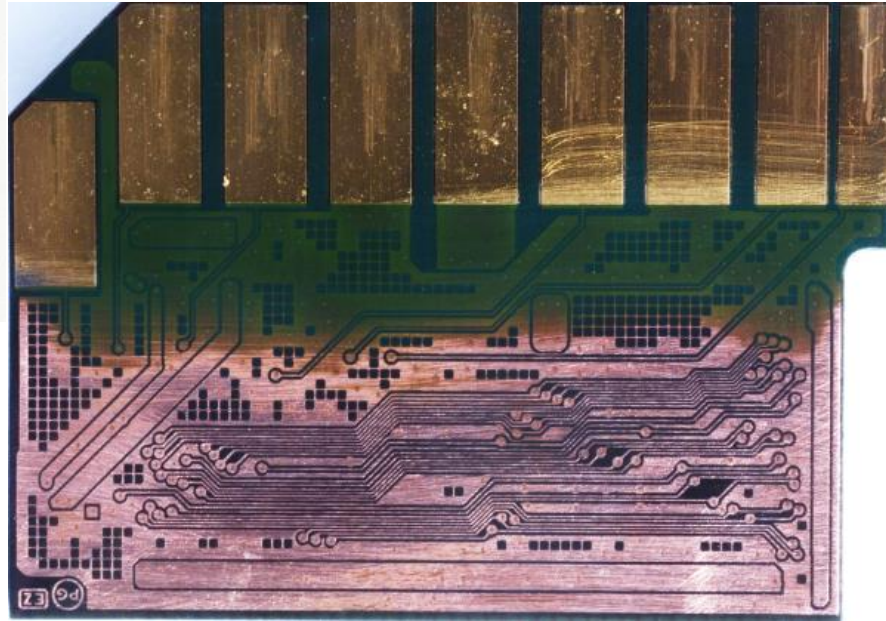
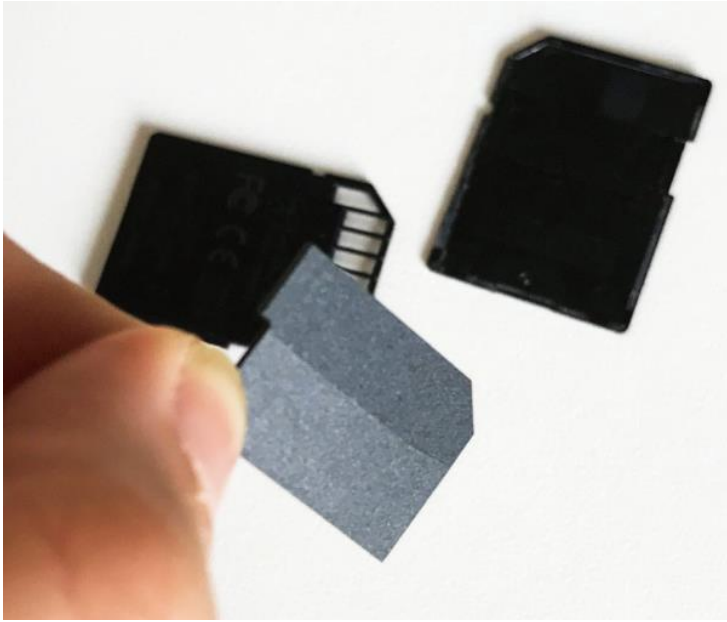
PINOUT ANALYSIS – MONOLITHIC USB FLASH DRIVE WITH CASELESS MEMORY



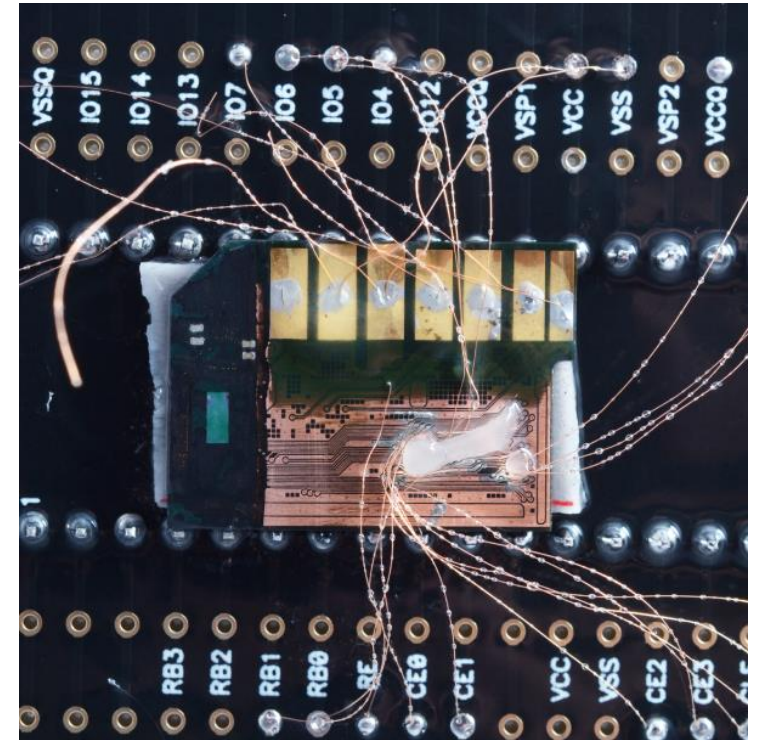
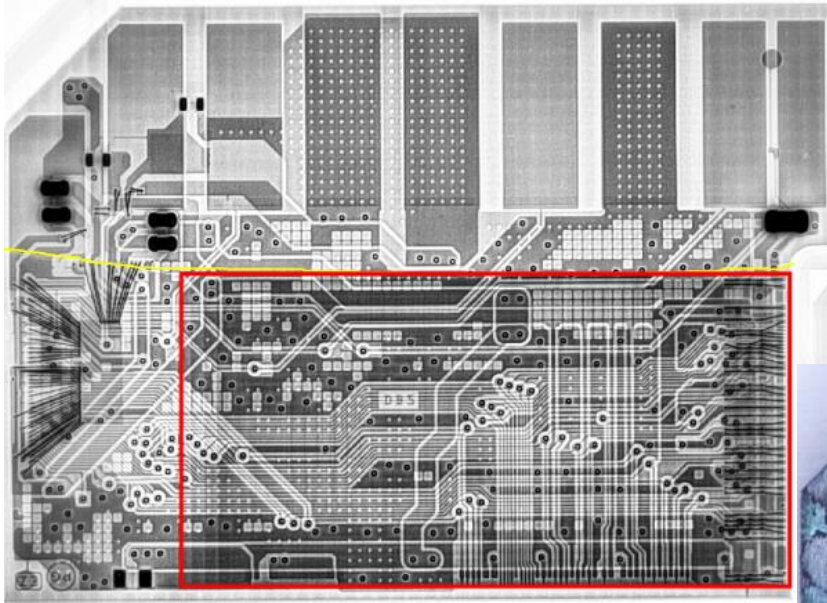
PINOUT ANALYSIS

- Find power lines and GNDs – they are thick
- Find 8 (16) similar tracks – it's data bus
- The rest is control signals. It takes a bit of practise to be able to recognize their order

REAL LIFE CASE



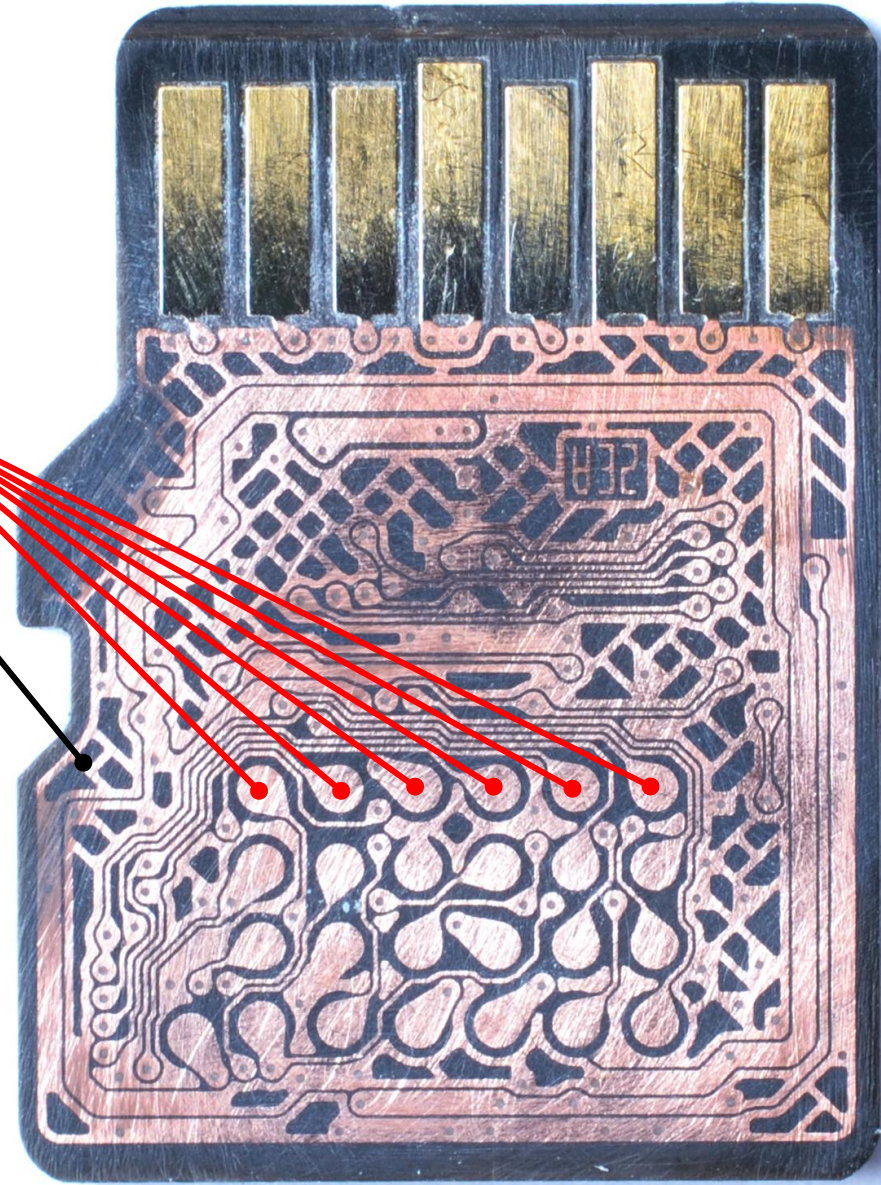
WIRED UP



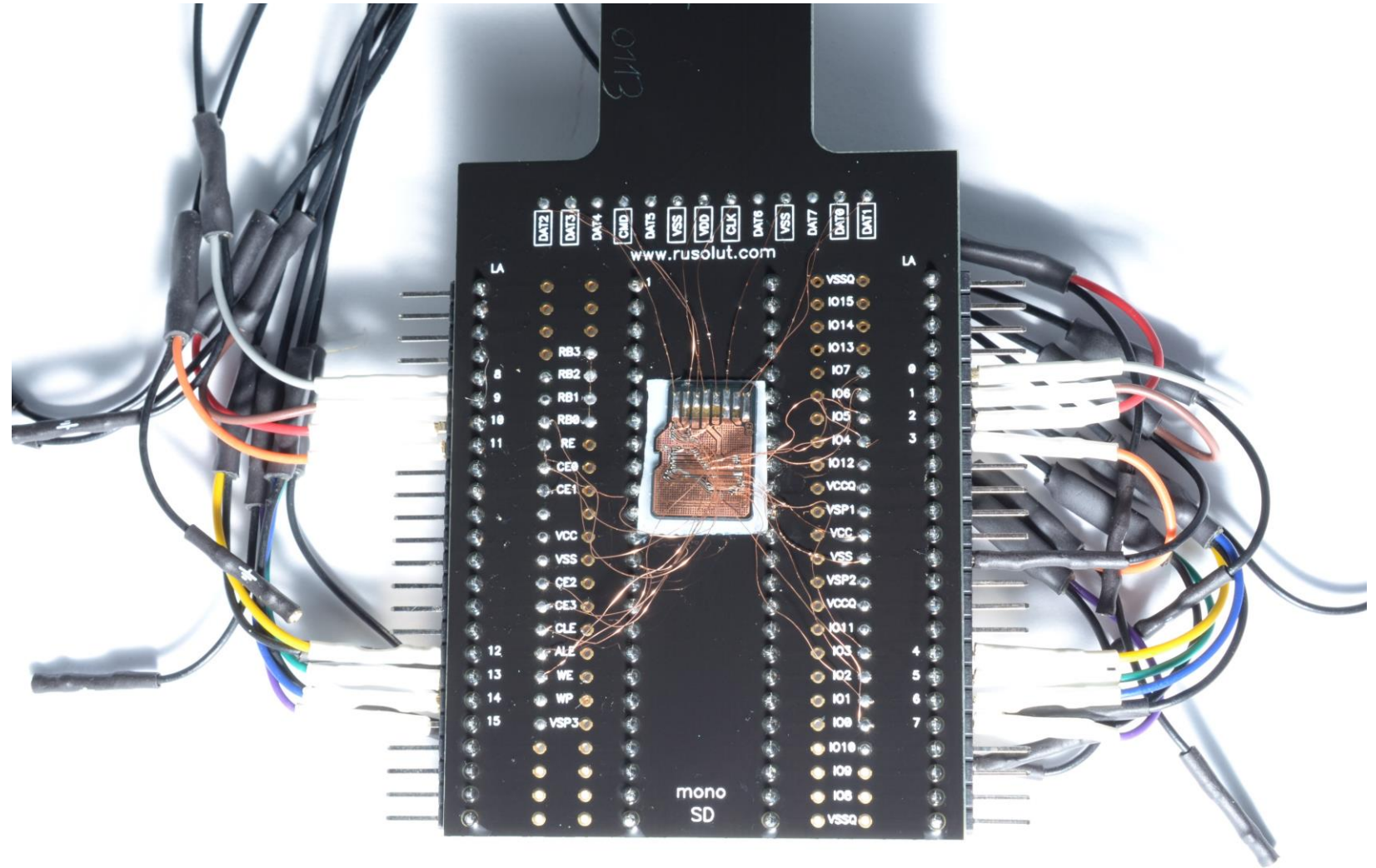
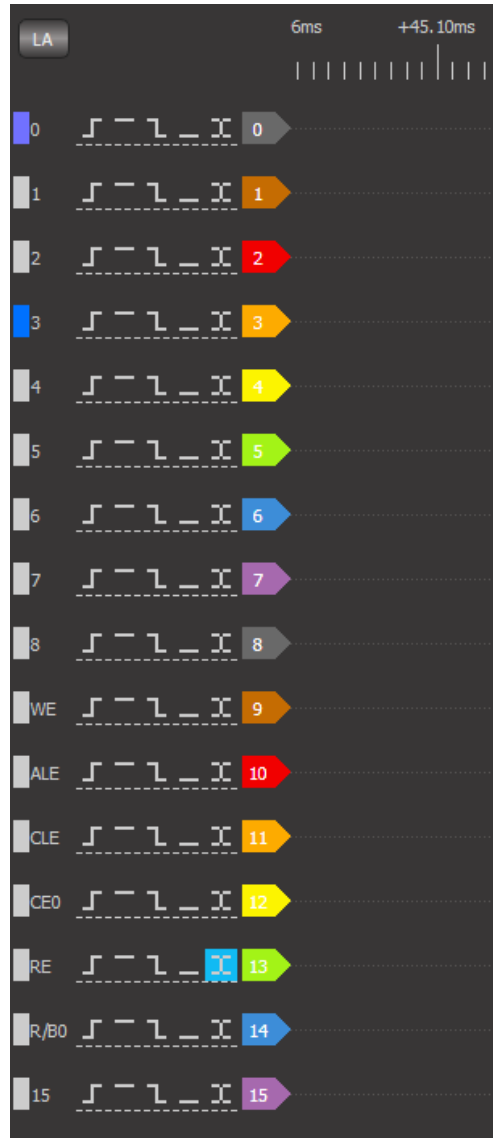
LOGIC ANALYZER, WHY?

- The basic tool for man-in-the-middle signal analysis in the digital data transfer channel
- Unknown pinout of the memory analysis
- Real time data sniffing (passwords, parameters, etc)
- Unknown protocol of communication (commands, register addresses, etc)

DEFINE THE SCOPE OF WORK



INITIAL RANDOM WIRING TO LOGIC ANALYZER



THE BASIC KNOWLEDGE OF INTERFACE IS REQUIRED

IO0...IO7 – Data bus

Vcc/VccQ – power 3,3 ... 1,8 V

Vss/VssQ - Ground

CLE – Command latch enable

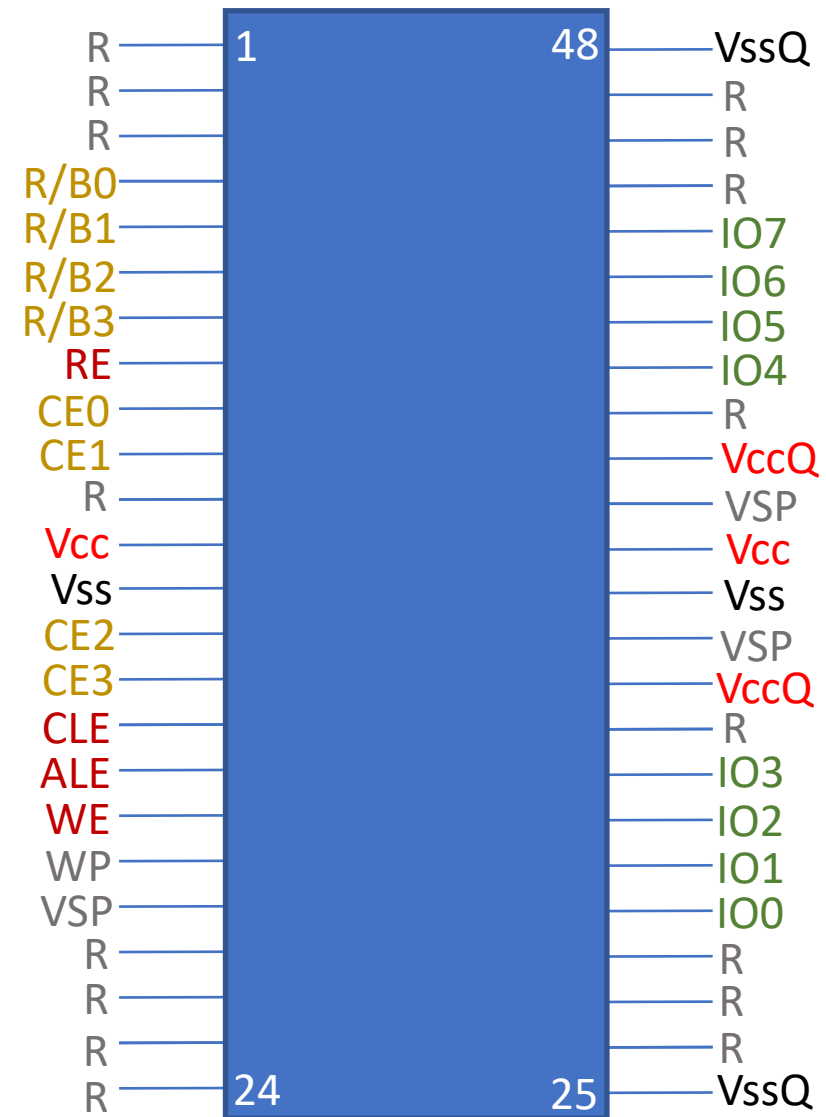
ALE – Address latch enable

RE – Read enable

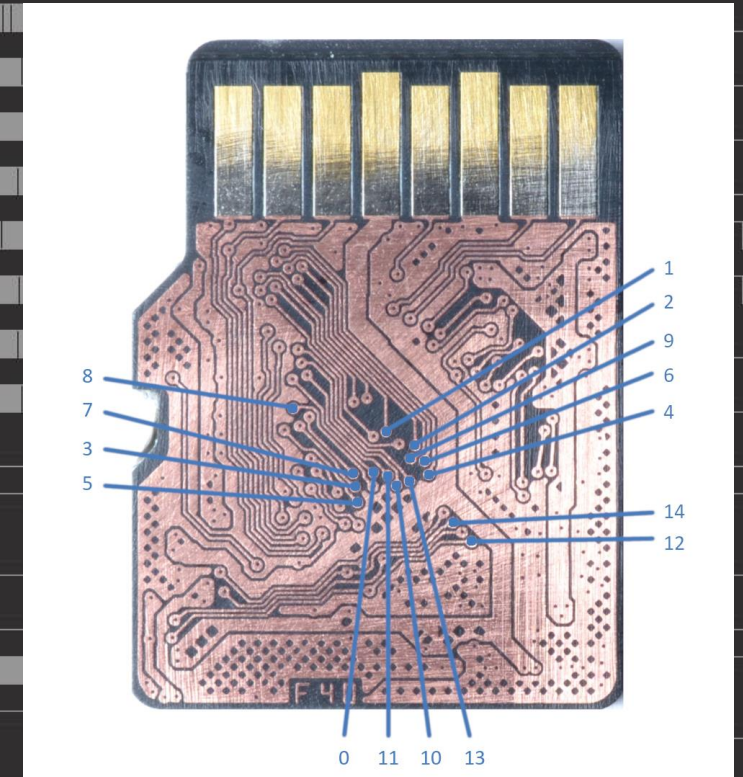
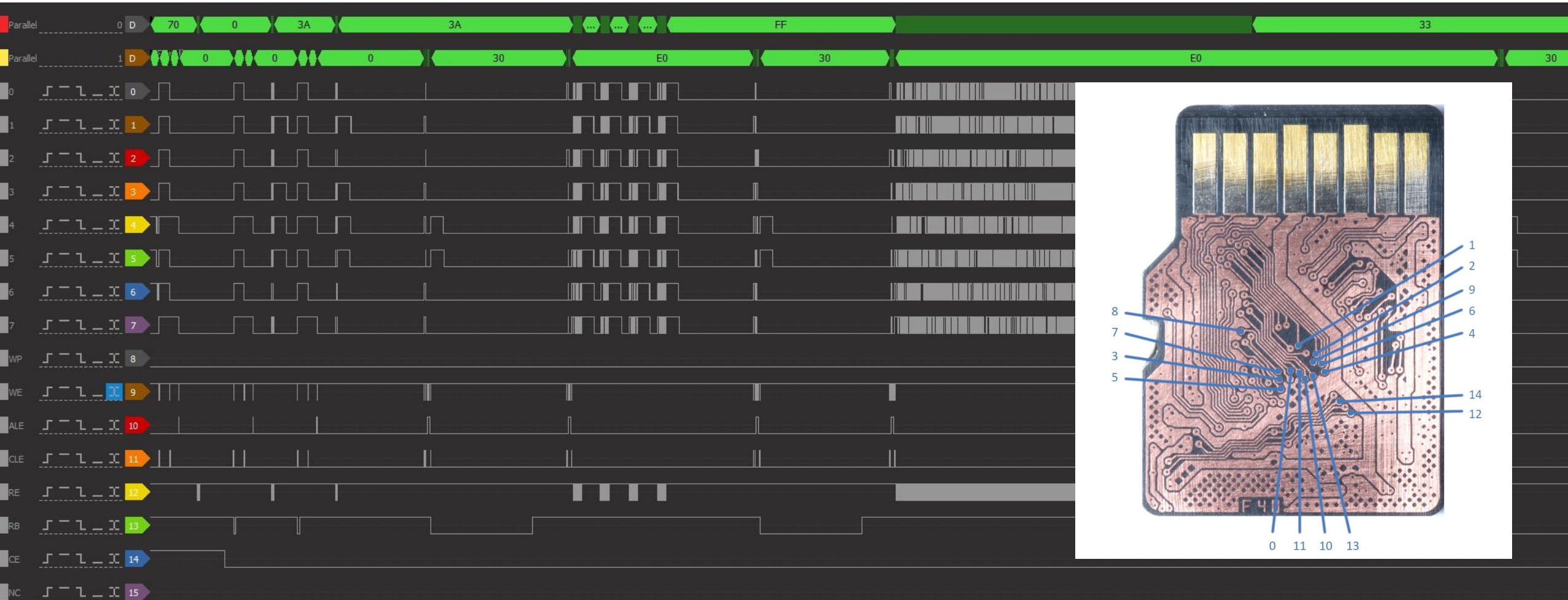
WE – Write enable

R/B0...R/B3 – Ready/Busy status

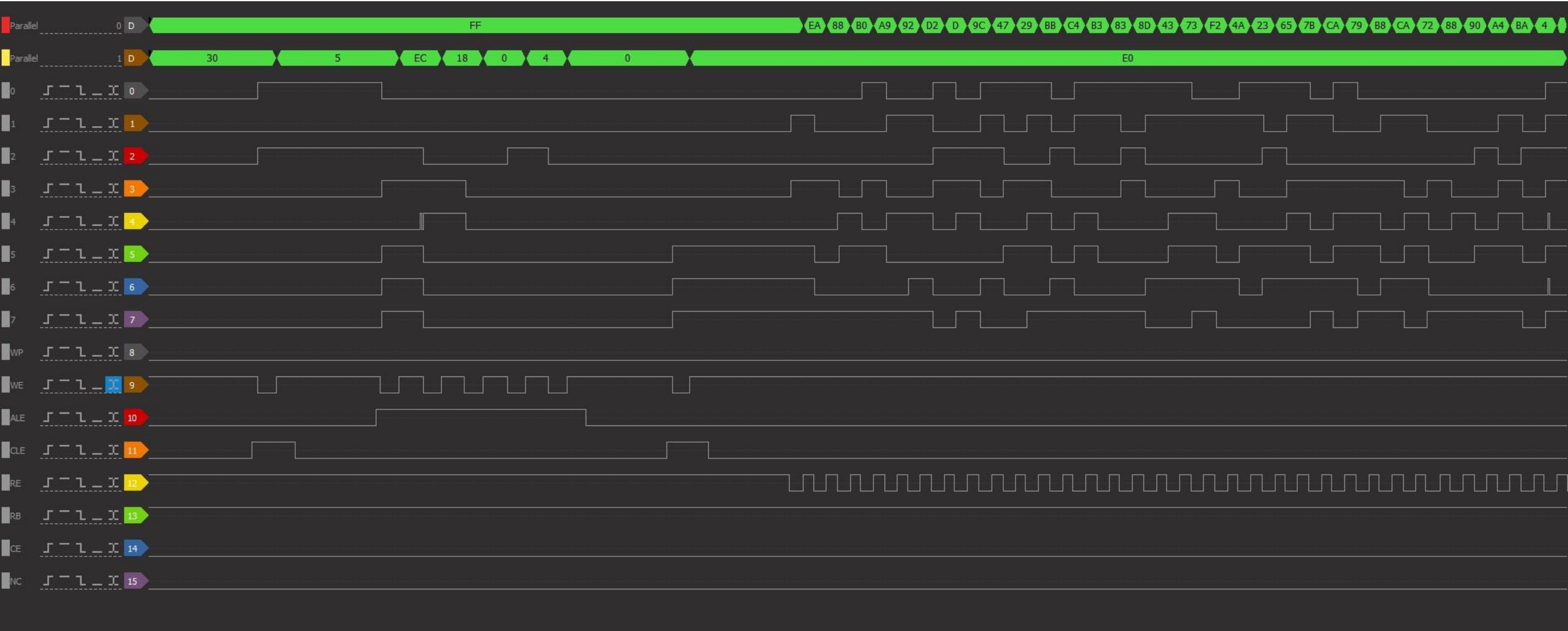
CE0...CE3 – Crystal enable



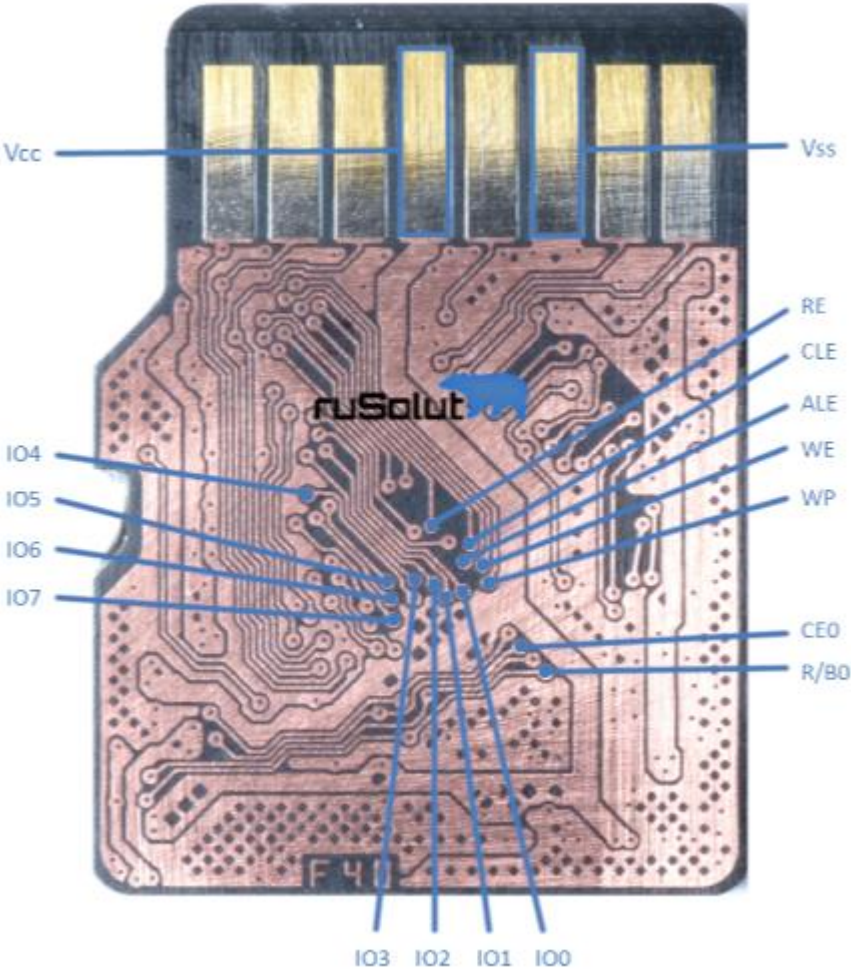
POWER UP YOUR "PATIENT" DEVICE AND READ THE SIGNALS



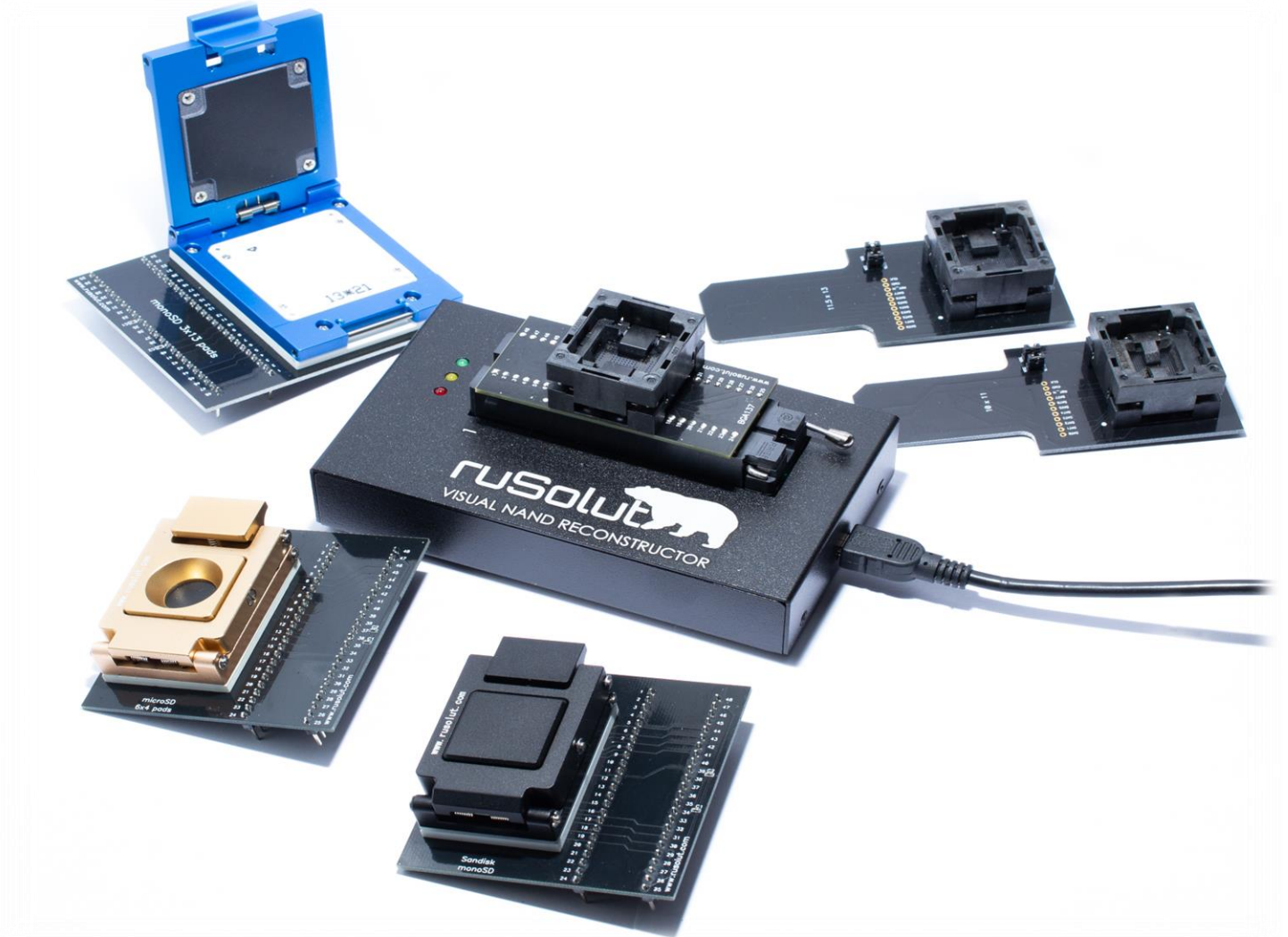
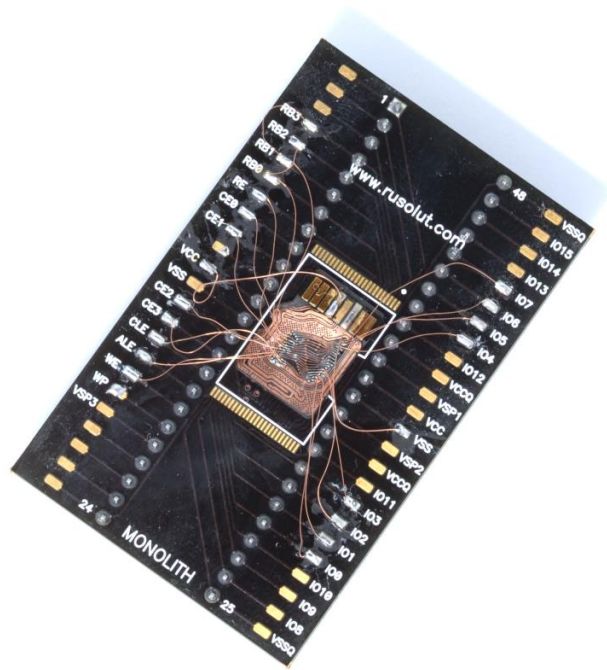
FIND SIGNAL PATTERNS AND IDENTIFY ALL THE SIGNALS OF THE PROTOCOL



PINOUT IS FOUND



ONCE PINOUT IS FOUND - CONNECT DEVICE TO READER



READ THE DUMP, ANALYZE IT AND GET THE DATA

The screenshot displays the Visual NAND R software interface. At the top right, the text "Visual NAND R" is visible. Below the title bar, there are tabs for "Case", "Workspace", and "Plugins". A toolbar contains icons for "Delete", "Copy", "Open images", "Insert area", "Skip area", "Extract area", "Remove bad columns", and "Positi...". Below the toolbar, the "Workspace" tab is active, showing a grid of components. On the left side of the workspace, there is a vertical toolbar with buttons labeled "R", "PI", "BCR", "BCH", "I", "X", "P", "U", "O", and "LI". In the center of the workspace, a "Reader 0" block is connected to four "Phy image" blocks, each labeled "Chip0_0_0", "Chip1_0_0", "Chip2_0_0", and "Chip3_0_0". A red line connects the Reader to the first Phy image block. A dialog box is overlaid on the workspace, titled "Reading dump from reader...". It features a progress indicator showing 15% completion. The dialog also displays the following information: "Chip: Chip0", "Port: 0", and "Crystal: 0". A "Cancel" button is located at the bottom of the dialog.

THANK YOU!

**We have next session tomorrow
with case studies!**

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