SPI 2018
22ND IEEE WORKSHOP ON SIGNAL AND POWER INTEGRITY
BREST, FRANCE
22-25 MAI 2018

Photo by Patricia Le Roux

Dear colleagues and friends,

It is a great privilege to serve as Chair of the 22nd IEEE Workshop on Signal and Power Integrity (SPI2018) and a pleasure to welcome everyone to France and to the city of Brest on the banks of the Atlantic Ocean.

Over the past two decades SPI has evolved into a forum of exchange on all aspects of Signal and Power Integrity covering the latest research topics on design, characterization, modeling, simulation and testing at chip, package, board and system level. The 2018 edition is jointly organized by the Lab-STICC and IMEP-LAHC research laboratories under the patronage of the Université de Bretagne Occidentale, the Ecole Nationale d'Ingénieurs de Brest and the Université de Savoie Mont Blanc.

The SPI Industry Forum, organized and chaired by its founder, Professor Stefano Grivet-Talocia is reaching its third edition and has already gained the reputation of an "event within the event". This special session features talks from the industry and focuses on challenges and problems that have no satisfactory solution yet. The aim is to foster cooperation with academia and tool vendors and help technology advance.

Another important aspect of SPI is its genuinely international nature – participants from thirteen countries are expected to attend this year's edition. The event will feature quality contributions organized in 9 oral sessions and one poster session. Social events were carefully organized in the long standing tradition of the workshop. The gala dinner will be hosted by Océanopolis, one of the largest aquariums in Europe and will be preceded by a guided tour. Cocktails will be served in the exotic atmosphere of tropical reefs.

SPI is also an inclusive event encouraging the participation of PhD. students and young researchers and providing high quality tutorials.

I must express my gratitude to SPI authors for their trust, to our sponsors for their support and to my colleagues from the Local Organizing Committee for their tireless work. I am also grateful to the members of the Standing Committee for their wise guidance.

I wish you all a very successful and enjoyable event!

Mihai Telescu

SPI2018 General Chair

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Tuesday 22 May 2018
14:00-17:30

Modeling and Simulation for Signal and Power Integrity in Mobile Platforms

Dr. Gianni Signorini (Intel Corporation, Germany)
Prof. Stefano Grivet-Talocia (Politecnico di Torino, Italy)

Abstract. This tutorial will cover technological, architectural, modeling and simulation challenges for the Signal and Power Integrity of high-end mobile platforms. On one hand, the latest packaging technologies for mobile applications will be discussed, emphasizing their pros and cons in view of current and expected future system requirements. On the other hand, the architectural challenges will be translated into modeling and simulation challenges, that engineers have to face in their daily work for ensuring system-level signal and power quality. Fast simulation approaches based on reduced-order behavioral models for both interconnects and devices will be discussed in detail. Finally, case studies from real mobile applications will be illustrated.

Part 1: **Signal and Power Integrity Challenges in Mobile System-in-Package and Platforms**
- Package/PCB/SiP Technologies
- Signal Integrity Challenges
- Power Integrity Challenges

Part 2: **Signal and Power Integrity Modeling and Simulation**
- Macromodeling for Passives, Interconnects and Power Delivery
- Macromodels for High-Speed IOs
- Methodologies for Signal Integrity, Power Integrity and RF

Gianni Signorini is a Staff Engineer in the "Chip-Package-Board" team of Intel Communication and Devices Group (iCDG). He is leading the execution and methodology development for Signal and Power Integrity simulations of Intel Mobile Modem solutions. Gianni received his B.Sc. (2010), M.Sc. (2012) and Ph.D. (2016) in Electronic Engineering from the University of Pisa, Italy. He joined Intel in 2011 and he is based in Munich, Germany.

Stefano Grivet-Talocia is a Full Professor of Electrical Engineering with Politecnico di Torino, Italy. From 1994 to 1996 He was with NASA/Goddard Space Flight Center, Greenbelt, MD, USA. His research interests include modeling and simulation of fields, circuits, and their interaction, with emphasis on reduced-order modeling and fast simulation methods. He is Author of more than 160 journal and conference papers. He was a co-founder of academic spinoff company IdemWorks, serving as President until its acquisition by CST in 2016. He was the General Chair of SPI2016 and SPI2017. He is a Fellow of the IEEE.

Wednesday 23 May 2018
9:00-10:00

Unsung Heroes of Scaling – Interconnects in Sub-Nanometer Regime
Dr. Aida Todri-Sanial (CNRS, France)

Abstract: Improving only the transistor performance of the future chip isn't sufficient. Chips, of course, are only one small part of the very large and complex information technology puzzle, albeit a very important one. Thus, to shape the future of the digital world, we also have to look at the bigger picture. Transistors are only as good as the system in which they are embedded. Interconnects play an important role as the operation frequency of today's CPUs is already governed by interconnect delays, and, during operation, most their power is dissipated in the interconnects. This is where current electrical copper (Cu) interconnects will approach their physical limitations and may no longer be able to keep pace with a processor's data throughput. Besides, accelerated technology scaling has aggravated Cu resistivity increase due to electron scattering and even more severely, it introduced electromigration issues. Mass transport along interfaces and grain boundaries in state-of-the-art Cu interconnects is one of the most important issues to be solved for future technology nodes according to the International Roadmap of Semiconductors (ITRS). The research and development on Cu interconnect manufacturing have been carried out for over twenty years. Academics and industry expect view that the replacement of Cu metal for the finest metal tracks might occur in the next 1-3 scaling nodes. This keynote speech will focus on the impact of interconnects on circuits' reliability, power-thermal-signal integrity, and overall energy efficiency. I will discuss why are switching energy of current systems is far from the SNL limit and the role of interconnects. Then, I will provide an overview of novel interconnects materials architectures that have the potential to address the energy efficiency challenge. I will also discuss the three-dimensional integration as a novel design paradigm for integrating more functionality and heterogeneous systems while improving energy efficiency.

Aida Todri-Sanial received the B.S. degree in electrical engineering from Bradley University, IL in 2001, M.S. degree in electrical engineering from Long Beach State University, CA, in 2003 and a Ph.D. degree in electrical and computer engineering from the University of California, Santa Barbara, in 2009. She is currently a Research Scientist for French National Council of Scientific Research (CNRS) attached to LIRMM. Previously, she was an R&D Engineer for Fermi National Accelerator Laboratory, IL. She has also held summer and visiting research positions at Mentor Graphics, Cadence Design Systems, STMicroelectronics and IBM TJ Watson Research Center. Her research interests focus on nanometer-scale issues in high-performance VLSI design with emphasis on power, thermal, signal integrity, and reliability issues as well as on circuits and systems for emerging technologies and nanomaterials. Currently, her research is focused on novel nanomaterials and exploring their physical properties for design of green electronics and bioelectronics applications. She has co-authored more than 100 publications on VLSI design area and emerging technologies. Dr. Todri-Sanial was a recipient of John Bardeen Fellow in Engineering in 2009, ACM Distinguished Speakers 2016-2018 and the CNRS Bronze Medal in 2016. She serves as Technical Program Committee member for ISVLSI, NEWCAS, GLSVLSI, ISQED, EDSSC, and DATE. She is Associated Editor for IEEE Transactions on VLSI, Journal of Microelectronics Reliability and Microelectronics Journal. Dr. Todri-Sanial is Editor-in-Chief for ACM SIGDA Newsletter. http://www.lirmm.fr/~todri

8:00   **Registration Opens**

9:00-9:20   **Opening Ceremony** *(Chair: M. Telescu)*

9:20-10:20   **Keynote Speech**

Unsung Heroes of Scaling – Interconnects in Sub-Nanometer Regime
Aida Todri-Sanial (*CNRS, LIRMM, Montpellier, France***)**

10:20-10:40   **Coffee break. Exhibition Opens**

10:40-11:20   **Session 1: Full Wave Modeling** *(Chair: M. Swaminathan)*
Fast Direct Full-Wave Electromagnetic Analysis of Planar Circuits Embedded in Multilayered Media
A. Menshov (student)[1], V. Okhmatovski[2]
[1]Dept. of ECE, The University of Texas at Austin, United States; [2]Dept. of ECE, University of Manitoba Winnipeg, MB, Canada

14:00-17:30   **Tutorials**

Modeling and Simulation for Signal and Power Integrity in Mobile Platforms

Gianni Signorini[1], Stefano Grivet-Talocia[2]
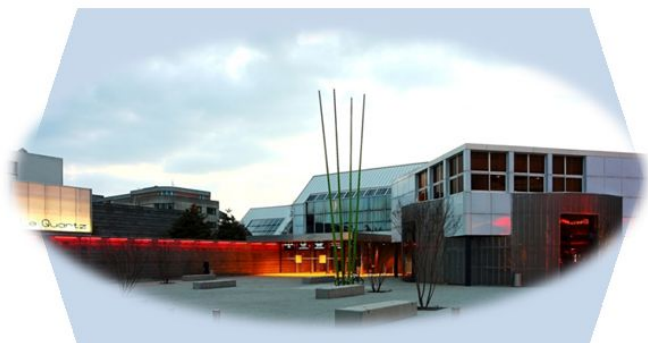**[1]Intel Corporation, Germany**
[2]Politecnico di Torino, Italy

11:00-11:20   A Fully 3-D BIE Evaluation of the Resistance and Inductance of On-Board and On-Chip Interconnects
M. Huynen (student), D. De Zutter, and D. Vande Ginste
Electromagnetics Group/IDLab, Department of Information Technology, Ghent University/Imec, Gent, Belgium

11:20-12:20   **Session 2: Macromodeling** *(Chair: D. Vande Ginste)*

14:00-15:30   **Tutorial part 1**

15:30-16:00   **Coffee break**

11:20-11:40   Multivariate Macromodeling with Stability and Passivity Constraints
A. Zanco (student), S. Grivet-Talocia, T. Bradde, M. De Stefano
Dept. Electronics and Telecommunications, Politecnico di Torino, Italy

16:00-17:30   **Tutorial part 2**

18:30-19:30   **Welcome reception**

11:40-12:00   Reduced-Order Model for Time-Domain Sensitivity Analysis of Active Circuits
B. Nouri and M. Nakhla
Department of Electronics, Carleton University, Ottawa, Canada

12:00-12:20   Circuit Synthesis of Blackbox Macromodels from S-Parameter Representation
J. Schutt-Ainé
Electrical and Computer Engineering. University of Illinois Urbana, USA

12:20-13:40   **Lunch break**

13:40-15:20 **Session 3: Stochastic Analysis & Uncertainty Quantification**
(Chair: B. Nouri and F. Ferranti)

13:40-14:00 Uncertainty Quantification of SiP based Integrated Voltage Regulator
M. Larbi[1], H. M. Torun[1], M. Swaminathan[1], I. S. Stievano[2], F. G. Canavero[2], and P. Besnier[3]
[1]*Center for Co-Design of Chip, Package, System (C3PS), School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, US;* [2]*Dipartimento di Elettronica, Politecnico di Torino, Italy;* [3]*IETR, UMR CNRS 6164 : IETR, INSA de Rennes, France.*

14:00-14:20 Perturbative Statistical Assessment of PCB Differential Interconnects
X. Wu (student)[1], P. Manfredi[2], F. Grassi[1] and D. Vande Ginste[3]
[1]*Dept. of Electronics, Information and Bioengineering, Politecnico di Milano, Italy,* [2]*Dept. of Electronics and Telecommunications, Politecnico di Torino, Italy,* [3] *Dept. of Information Technology, IDLab, Ghent University - imec, Belgium*

14:20-14:40 Modeling of Eye Diagram Height in High-Speed Links via Support Vector Machine
R. Trinchero and F. G. Canavero
EMC Group, Department of Electronics and Telecommunications, Politecnico di Torino, Italy

14:40-15:00 Parameterized Macromodeling of Stochastic Linear Systems for Frequency- and Time-Domain Variability Analysis
Y. Ye (student)[1], D. Spina[1], G. Antonini[2], and T. Dhaene[1]
[1]*IDLab, Department of Information Technology, Ghent University - imec, Belgium;* [2]*UAq EMC Laboratory, Dipartimento di Ingegneria Industriale e dell'Informazione e di Economia, Universita degli Studi dell'Aquila, Italy.*

15:00-15:20 Machine Learning Methodology for Inferring Network S-parameters in the Presence of Variability
X. Ma (student), M. Raginsky, and A. C. Cangellaris
Department of Electrical and Computer Engineering University of Illinois, USA

15:20-17:20 **Poster Session (includes coffee break)**
(Chair: J. Kar and S. Piersanti)

P1 Impact of the Doped Areas Sizes in the Performances of Microwave SPST Switches Integrated in a Silicon Substrate
R. Allanic[1], D. Le Berre[1], Y. Quere[1], C. Quendo[1], D. Chouteau[2], V. Grimal[2], D. Valente[2], J. Billoue[2]
[1]*Lab-STICC, Université de Brest (UBO) UMR CNRS 6285, Brest, France ;*
[2]*Laboratoire GREMAN", Université de Tours, France.*

P2 Eye Diagram Estimation and Equalizer Design Method for PAM4
R.-B. Wu, W-J. Chang (student)
EDAP Laboratory, Graduate Institute of Communication Engineering National Taiwan University, Taipei, Taiwan

P3 Powering a Remote Board and Sensors in an extreme environment - an optical solution
C. Diouf[1], L. Ghisa[1], R. Hamie[1], V. Quintard[1], M. Guegan[1], A. Perennou[1], L. Gautier[2], M. Tardivel[2], S. E. Barbot[2], F. Colas[2]
[1]*Lab-STICC/ ENIB, UMR CNRS 6285 Brest, France,* [2]*IFREMER/RDT Centre de Brest, France*

P4 Evaluation and Comparison of Mounted Inductance for Decoupling Capacitor
B. Goral[1], C. Gautier[1], A. Amedeo[2]
[1]*ENS de Paris-Saclay Cachan, France;* [2]*Thales Communications and Security Cholet, France*

P5 CMOS Integrated 1 GHz Ring Oscillator with Injection-Locked Frequency Divider for Low Power PLL
J. Park (student), S. Chun (student), H. Choi (student), N. Kim
School of ECE, Chungbuk National University Cheong-ju, Korea.

P6   Impedance Measurement in Operating Conditions for PLC Applications

S. Sabo (student)[1], L. Pace (student)[1], J-C. Le Bunetel[3], A-S. Descamps[2], C. Batard[2], N. Idir[1], O. Mahamane

[1]University of Lille France, [2]University of Nantes France; [3]University of Tours, France

P7   Assessment of Coupled Transmission Lines Embedded Between Imperfectly Matched Differential Circuit Stages

G. Mendez-Jeronimo (student), R. Torres-Torres

National Institute of Astrophysics, Optics and Electronics Puebla, Mexico

P8   Analysis of PSIJ in the Presence of both Ground-Bounce and Transmission Media

J. Narayan Tripathi[1], A. Jain (student)[2], M. Marinkovic (student)[2], R. Achar[2]

[1]TD&P, STMicroelectronics, INDIA. [2]Department of Electronics, Carleton University, Ottawa, Canada.

P9   Simulation of Nonuniform Coupled Transmission Lines using approximated S-Parameters Model.

A. Wardzinska, W. Bandurski

Poznan University of Technology, Faculty of Electronics and Telecommunications, Poznań, Poland

Free Evening

8:00   **Registration Opens. Exhibition Opens**

8:40-10:20   **Session 4: Power Delivery Networks**
(Chair: J. Schutt-Ainé and F. Canavero)

8:40-9:00   Power Integrity Challenges of Re-desigining a Mobile SoC with Fully Integrated Voltage Regulator to IoT Applications

Y. F. Shen

Internet of Things Group, Intel Corporation, Chandler, USA

9:00-9:20   An On-Chip Load Model for Off-Chip PDN Analysis Considering Interdependency Between Supply Voltage, Current Profile and Clock Latency

J. Chen (student)[1], T. Kanamoto[2], H. Kando[3], M. Hashimoto[1]

[1]Osaka University Osaka, Japan; [2]Hirosaki University Aomori, Japan; [3]Murata Manufacturing Co., Ltd. Kyoto, Japan

9:20-9:40   A Robust Power Delivery Design Strategy For Platform on DIMM

D. M. García-Mora[1], J. Kar[2], I. Mendez-Soriano[1], H. Morales-Espinosa[1]

[1]Datacenter Package and Power Solutions Intel Guadalajara Design Center Guadalajara, Mexico; [2]Datacenter Package and Power Solutions Intel Corporation Santa Clara, CA, USA.

9:40-10:00   Optimizing Phase Settings of High-Frequency Voltage Regulators for Power Delivery Applications

F. De Jesús Leal-Romo (student)[1], J. L. Silva-Perales[2], C. López-Limón[2], and J. E. Rayas-Sánchez[1]

[1]Department of Electronics, Systems, and Informatics, ITESO, The Jesuit University of Guadalajara Mexico; [2]Intel Corp. Zapopan, Jalisco, Mexico.

10:00-10:20   Optimization of On-Package Decoupling Capacitors Considering System Variables

A. Sanna, G. Graziosi

Back-End Manufacturing and Technology R&D, STMicroelectronics, Agrate Brianza, Italy

10:20-10:40   **Coffee break**

10:40-11:20 **Session 5: Nano, Optical and Wireless Interconnects**
(Chair: H. Grabinski)

10:40-11:00 Integrated Dipole Antennas and Propagation Channel on Siliconin Ka Band for WiNoC Applications
I. El Masri (student), T. Le Gouguec, P-M. Martin, R. Allanic, C. Quendo
Lab-STICC/Université de Brest (UBO) UMR CNRS 6285 BREST, France

11:00-11:20 Electrical properties of a graphene nanoplatelets composite as interposer for electronic packages
A. Maffucci[1], L. Ferrigno[1], M.D. Migliore[1], D. Pinchera[1], F. Schettino[1], F. Micciulla[2], S. Bellucci[2], S. Maksimenko[3], A. Paddubskay[3]
[1,2]D.I.E.I., University of Cassino and Southern Lazio, Cassino, Italy ; [3]Institute for Nuclear Problems, Belarusian State University, Minsk, Belarus

11:20-11:40 A Comparison of Higher-Order Graded-Index MMI-Based Splitters in Thin Glass Sheets for PCB Integration
J-P. Roth, T. Kühler and E. Griese
University of Siegen, Theoretical Electrical Engineering and Photonics H, Siegen, Germany

11:40-12:20 **Session 6: Noise reduction** *(Chair: F. Grassi)*

11:40-12:00 Suppression of Noise from Digital-to-Analog Coupling in Shielding Cavity
H-W. Chan (student) and R-B. Wu
EDAP Laboratory, Graduate Institute of Communication Engineering National Taiwan University, Taipei, Taiwan

12:00-12:20 Miniaturized Wide-and Dual-Band Multilayer Electromagnetic Bandgap For Antenna Isolation and on-Package/PCB Noise Suppression
P. Bantavis (student), M. Le Roy, A. Perennec, R. Lababidi, D. Le Jeune
Lab-STICC, UMR CNRS 6285, Université de Brest (UBO)/ENSTA-Bretagne, Brest, France

12:20-13:40 **Lunch**

13:40-14:40 **Session 7: Equalization techniques**
(Chair: G. Houzet)

13:40-14:00 Direct Prediction of Linear Equalization Coefficients Using Raised Cosine Pulse Shaping in Frequency Domain
T. Wendt (student), T. Reuschel (student) and C. Schuster
Hamburg University of Technology, Institute of Electromagnetic Theory, Hamburg, Germany

14:00-14:20 DDR5 Design Challenges
N. Bhagwath[1], R. Wolff[2], S. Ikeda[3], E. Fujine[4], R. Shibata[4], Y. Sugaya[3], M. Ono[3]
[1]Mentor Graphics, a Siemens Business, Fremont, USA; [2]Micron Technology Boise, USA ; [3]Socionext Yokohama, Japan ; [4]Socionext Kasugai, Japan

14:20-14:40 An Eye Diagram Improvement Method using Simulation Annealing Algorithm
P-J. Li (student) and T-L. Wu
Department of Electrical Engineering and Graduate Institute of Communication Engineering, National Taiwan University, Taipei, Taiwan

14:40-15:00 **Coffee break**

15:00-17:40   **Interactive Industrial Forum**
(Chair: S. Grivet-Talocia)

Michael W. Leddige
Intel, USA
Signal and Power Interactions in Next Generation Platforms

Benoit Goral
Thales, France
Challenges in PDN Design

Hubert Harrer
IBM Germany
Packaging Challenges for High End Servers

Olivier Bayet
STMicroelectronics, France
Power integrity of networking processor at system level

Gianni Signorini
Intel Corporation, Germany
"Chip-Package-Board" Co-Design: a Signal & Power Integrity Perspective

17:40   **Exhibition Closes**

18:00-22:30   **Visit of Océanopolis and Gala dinner**

8:40-9:40   **Session 8: Measurements and characterization**
(Chair: M Le Roy and A. Maffucci)

8:40-9:00   Usage of ESD Detector Circuit for Analyzing Soft Failures in IC cores
T. Ostermann
Institute for Integrated Circuits/Department for Energy-Efficient Analog Circuits and Systems JKU Johannes Kepler University of Linz, Linz, Austria

9:00-9:20   Modelling and Validation of High-Current Surface-Mount Current-Sense Resistor
J. Bačmaga (student)[1], R. Blečić[2], R. Gillon[3], A. Barić[1]
[1]University of Zagreb, Faculty of Electrical Engineering and Computing, Zagreb, Croatia; [2] KU Leuven, ESAT-TELEMIC, Leuven, Belgium; [3]ON Semiconductor, Westerring Oudenaarde, Belgium

9:20-9:40   Fast and Robust RF Characterization Method of Insulators used in High Speed Interconnects Networks
T. Lacrevaz[1], D. Auchère[2], G. Houzet[1], P. Artillan[1], B. Flechet[1], C. Bermond[1], B. Blampey[1]
[1]IMEP-LAHC, UMR CNRS 5130, University Savoie Mont-Blanc, Le Bourget du Lac-France; [2]STMicroelectronics, Grenoble, France

9:40-10:00   In-Depth Characterization of a Dielectric Waveguide for mmW Transmission Line Applications
F. Distler (student), J. Schür and M. Vossiek
Institute of Microwaves and Photonics (LHFT) Friedrich-Alexander-Universitat Erlangen-Nurnberg (FAU) Erlangen, Germany

10:00-10:20   **Coffee break**

10:20-11:20   **Session 9: High Speed links and modeling for SI/PI**
(Chair: U. Arz)

10:20-10:40   Physical Scaling Effects of Differential Crosstalk in Via Arrays up to Frequencies of 100 GHz
K. Scharff (student), D. Dahl, H-D. Brüns, C. Schuster
Institute of Electromagnetic Theory, Hamburg University of Technology, Hamburg, Germany

10:40-11:00   Impact of Chip and Interposer PDN to Eye Diagram in High Speed Channels
F. De Paulis[1], B. Zha[2], S. Piersanti[1], J. Cho[2], R. Cecchetti[1], B. Achkir[3], A. Orlandi[1], J. Fan[2]
[1]University of L'Aquila L'Aquila, Italy; [2] MST EMC Laboratory Missouri University of Science and Technology Rolla, USA; [3] Cisco Systems San Jose, USA

11:00-11:20   Impact of On-Chip Multi-Layered Inductor on Signal and Power Integrity of Underlying Power-Ground Net
A. Tsuchiya[1], A. Hiratsuka (student)[2], T. Inoue[1], K. Kishine[1], H. Onodera[2]
[1]Dept. Electronic Systems Engineering The University of Shiga Prefecture Hikone, Japan; [2]Dept. Communications and Computer Engineering Kyoto University Kyoto, Japan.

11:20-12:00   **Closing Session**

21st IBIS European Summit

13:30   **Sign in, refreshments**

13:45   **Welcome and introductions** *(M. Labonte; SiSoft, USA)*

14:00   IBIS Update
M. Labonte; SiSoft, USA

14:20   IBIS-Compatible Macromodel and Interconnect Simulation Techniques
J. Schutt-Ainé; University of Illinois, Urbana-Champaign, USA

14:50   On Automated Generation of Behavioral Parameterized Macromodels
Part I: Algorithmic Aspects
T. Bradde, S. Grivet-Talocia, M. De Stefano, A. Zanco; Politecnico di Torino, Italy

15:15   On Automated Generation of Behavioral Parameterized Macromodels
Part II: SPICE Equivalents and Applications
M. De Stefano, S. Grivet-Talocia, T. Bradde, A. Zanco; Politecnico di Torino, Italy

15:40   **Break, refreshments**

16:00   IBIS-AMI and Jitter
M. Labonte; SiSoft, USA

16:35   DDR5 Equalization Options with IBIS
A. Muranyi, N. Bhagwath; Mentor, A Siemens Business, USA

17:10   IBIS [Model Selector] Improvement Proposal
M. Schaeder*, B. Ross**; *Zuken, Germany, **Teraspeed Labs, USA

17:30   Open Discussion

17:50   **Closing Remarks** *(M. Labonte; SiSoft, USA)*

17:55   **End of meeting**

18:00   **After meeting Bonus: Walking tour of local history sites**
M. Telescu; UBO, Brest, France

Tuesday, May 22nd, 2018
18:30

Welcome Reception
Le Quartz

Thursday, May 24th, 2018
18:00

Océanopolis Visit
Gala dinner

The conference will be hosted in the Méridienne room of the Conference Center "Le Quartz"

Le Quartz
Square Beethoven, 60 Rue du Château,
29210 Brest, France
http://www.lequartzcongres.fr/
+33 2 98 33 95 00

Brest

Quartz

Océanopolis

Aéroport Brest-Bretagne

SPI 2018		Tuesday May 22nd	Wenesday May 23th	Thursday May 24th	Friday May 25th
08:00	08:20		Registration opens	Registration opens	Registration opens
08:20	08:40		Registration opens	Registration opens	Registration opens
08:40	09:00			Session 4 Power Delivery Networks	Session 8 Measurements & Characterization
09:00	09:20		Openning Session	Session 4 Power Delivery Networks	Session 8 Measurements & Characterization
09:20	09:40		Keynote Unsung Heroes of Scaling–Interconnects in Sub-Nanometer Regime	Session 4 Power Delivery Networks	Session 8 Measurements & Characterization
09:40	10:00		Keynote Unsung Heroes of Scaling–Interconnects in Sub-Nanometer Regime	Session 4 Power Delivery Networks	Session 8 Measurements & Characterization
10:00	10:20		Keynote Unsung Heroes of Scaling–Interconnects in Sub-Nanometer Regime	Session 4 Power Delivery Networks	Coffee break
10:20	10:40		Coffee break	Coffee break	Session 9 High Speed links & modeling for SI/PI
10:40	11:00		Session 1 Full Wave modeling	Session 5 Nano-Optical & Wireless Interconnects	Session 9 High Speed links & modeling for SI/PI
11:00	11:20		Session 1 Full Wave modeling	Session 5 Nano-Optical & Wireless Interconnects	Session 9 High Speed links & modeling for SI/PI
11:20	11:40		Session 2 Macromodeling	Session 5 Nano-Optical & Wireless Interconnects	Closing Session
11:40	12:00		Session 2 Macromodeling	Session 6 Noise reduction	Closing Session
12:00	12:20		Session 2 Macromodeling	Session 6 Noise reduction	
12:20	12:40		Lunch break	Lunch break	
12:40	13:00		Lunch break	Lunch break	
13:00	13:20		Lunch break	Lunch break	
13:20	13:40	Welcome Tutorials	Lunch break	Lunch break	
13:40	14:00	Welcome Tutorials	Session 3 Stochastic Analysis & Uncertainty Quantification	Session 7 Equalization techniques	IBIS welcome Reception
14:00	14:20	14:00 - 15:30 Tutorial Part 1 Modeling and Simulation for Signal and Power Integrity in Mobile Platforms	Session 3 Stochastic Analysis & Uncertainty Quantification	Session 7 Equalization techniques	IBIS European Summit
14:20	14:40	14:00 - 15:30 Tutorial Part 1 Modeling and Simulation for Signal and Power Integrity in Mobile Platforms	Session 3 Stochastic Analysis & Uncertainty Quantification	Session 7 Equalization techniques	IBIS European Summit
14:40	15:00	14:00 - 15:30 Tutorial Part 1 Modeling and Simulation for Signal and Power Integrity in Mobile Platforms	Session 3 Stochastic Analysis & Uncertainty Quantification	Coffee break	IBIS European Summit
15:00	15:20	14:00 - 15:30 Tutorial Part 1 Modeling and Simulation for Signal and Power Integrity in Mobile Platforms	Session 3 Stochastic Analysis & Uncertainty Quantification		IBIS European Summit
15:20	15:40	15:30 - 16:00 Coffee break		Interactive Industrial Forum	IBIS European Summit
15:40	16:00	15:30 - 16:00 Coffee break	Poster Session (includes Coffee break)	Interactive Industrial Forum	IBIS European Summit
16:00	16:20	16:00 - 17:30 Tutorial Part 2 Modeling and Simulation for Signal and Power Integrity in Mobile Platforms	Poster Session (includes Coffee break)	Interactive Industrial Forum	IBIS European Summit
16:20	16:40	16:00 - 17:30 Tutorial Part 2 Modeling and Simulation for Signal and Power Integrity in Mobile Platforms	Poster Session (includes Coffee break)	Interactive Industrial Forum	IBIS European Summit
16:40	17:00	16:00 - 17:30 Tutorial Part 2 Modeling and Simulation for Signal and Power Integrity in Mobile Platforms	Poster Session (includes Coffee break)	Interactive Industrial Forum	IBIS European Summit
17:00	17:20	16:00 - 17:30 Tutorial Part 2 Modeling and Simulation for Signal and Power Integrity in Mobile Platforms	Poster Session (includes Coffee break)	Interactive Industrial Forum	IBIS European Summit
17:20	17:40	16:00 - 17:30 Tutorial Part 2 Modeling and Simulation for Signal and Power Integrity in Mobile Platforms	Poster Session (includes Coffee break)	Interactive Industrial Forum	IBIS European Summit
17:40	18:00				
18:00	18:20				
18:20	18:40				
18:40	19:00	18:30 - 19:30 Welcome reception	Free evening	Gala dinner Oceanpolis	
19:00	22:00	18:30 - 19:30 Welcome reception	Free evening	Gala dinner Oceanpolis	