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Contents

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Conference 10143: Extreme Ultraviolet (EUV) Lithography VIII

Monday - Thursday 27–2 March 2017

Part of Proceedings of SPIE Vol. 10143 Extreme Ultraviolet (EUV) Lithography VIII

10143-1, Session 1

EUVL Readiness for High-Volume Manufacturing *(Keynote Presentation)*

Britt Turkot, Intel Corp. (United States)

No Abstract Available

10143-2, Session 1

Progress in EUV lithography toward manufacturing *(Keynote Presentation)*

Seong-Sue Kim, SAMSUNG Electronics Co., Ltd. (Korea, Republic of)

No Abstract Available

10143-3, Session 2

EUV exposure mechanisms of antimony resists

Michael Murphy, James Passarelli, Jodi Hotalen, Philip Schuler, Jeff Richards, Amrit K. Narasimhan, Gregory H. Denbeaux, Robert L. Brainard, SUNY Polytechnic Institute (United States)

Since 2009, the photoresist community has seen a great deal of interest in EUV photoresists containing metallic elements. This sudden interest in metal-containing resists was inspired by pioneering work of Doug Keszler at the Oregon State University and Chris Ober at Cornell University. Additionally, the realization that capturing more EUV photons will be essential to provide manufacturing capabilities with the necessary photon statistics. Our group has developed a number of EUV resist platforms based on metals that absorb EUV strongly including: cobalt, tin, palladium, bismuth and antimony.

It is the later platform, which is the subject of this paper. We have presented on the properties of penta-coordinate antimony resists of the general form of R3SbX2 which contain olefins. This resist system has demonstrated remarkable sensitivity of Esize = 5.6 mJ/cm2 for 35 nm L/S features (Figure 1A). In previous work, we have proposed an EUV exposure mechanism in which a bond to antimony (Sb-R or Sb-X) breaks homolytically (Initiation) followed by free-radical polymerization (Propagation). This mechanism is supported by several experimental studies including: (1) sensitivity comparison between acrylate and acetate and (2) sensitivity correlation with concentration of olefin functionality.

Despite the studies described above, there are several aspects of EUV exposure mechanism of this platform which we have yet to describe in the open literature. In order to fully realize the lithographic potential of this system we have conducted several detailed experimental studies that we will present at the conference. These studies include an initiator study in which several compounds of the form Ph3SbX2 have been added to an organic diolefin monomer (MM-5). This work shows that the best photosensitivity is achieved when X = Cl or Br, and the worst sensitivity is achieved when X = OAc or I. Additionally, we will conduct experiments focused on determining the extent of polymerization (EUV exposure/GPC), which bonds are formed during exposure (EUV/NMR), and reaction cross-sections with 80 eV electrons (e-beam/MS).

10143-4, Session 2

Nanoparticle photoresist studies for EUV lithography

Hong Xu, Vasiliki Kosma, Jeremy Odent, Cornell Univ. (United States); Kazuki Kasahara, JSR Corp. (Japan); Emmanuel P. Giannelis, Christopher K. Ober, Cornell Univ. (United States)

EUV lithography is one of the most promising candidates for next generation lithography. The main challenge for EUV resists is to satisfy resolution, line-width roughness (LWR) and sensitivity requirements according to the ITRS roadmap. The performance targets require development of entirely new resist platforms. Cornell University has studied metal oxide nanoparticle photoresists for this application. Zirconium oxide nanoparticles with PAG enabling sub 30nm line negative tone patterns at an EUV dose below 5 mJ/cm2, show one of the best EUV sensitivity results ever reported. In this paper, recent progress in nanoparticle photoresists will be described. Discussion regarding new metal core applications and mechanism studies will be included.

Regarding the new metal core study, new metal elements have been applied to nanoparticle resist systems in terms of high EUV absorbance for better lithography performance. In particular new zinc oxide nanoparticles have shown better resolution than zirconium oxide nanoparticles. E-beam and EUV exposure results of these new photoresist will be described.

In a study of the patterning mechanism, (1) ligand exchange, (2) ligand dissociation and (3) condensation reaction are all considered to occur in parallel. However, these plausible mechanisms were investigated in experiments using DUV exposure. Improved mechanistic understanding derived from e-beam and EUV exposures will be discussed.

10143-5, Session 2

Advanced development techniques for metal-based EUV resists

Jodi Hotalen, Michael Murphy, William Earley, SUNY Polytechnic Institute (United States); Daniel A. Freedman, State Univ. of New York at New Paltz (United States); Robert L. Brainard, SUNY Polytechnic Institute (United States)

The first positive-tone MORE resists were oxalate complexes with platinum and palladium centers. The oxalate ligand (C2O42-) is eliminated as carbon dioxide (CO2) during exposure to EUV light. We suspect that the oxalate ligand is the key to achieving a positive-tone organometallic resist. NP1(1) is a cobalt complex that contains oxalate ligands and has similar photochemistry to the platinum and palladium oxalates. Although this resist contains oxalate ligands, previously only negative-tone imaging has been observed. Having some knowledge of the photomechanism and resulting photoproducts, we hypothesized this resist could be converted from negative- to positive-tone imaging through development.

Here, we present lithographic results of several MORE compounds with specialized developers. We introduced a ligand, such as a carboxylic acid, to the developer which resulted in positive-tone imaging with NP1 (1). As the concentration of the developer is increased, the tone of the resist can switch from positive- to negative-tone. Previous negative-tone results with NP1 (1) developed in 2-butanone (MEK) have shown an Emax = 36 mJ/cm2 and a photoresist contrast (γ) of 0.4. Recent results have shown improved sensitivity (Emax = 27mJ/cm2) and contrast (γ = 1.3) of the negative-tone imaging through development in cyclohexanone. This cobalt-oxalate resist system (1) when developed in a solution containing lactic acid, demonstrated negative-tone imaging with fastest photo-speed (Emax = 5 mJ/cm2) and best photoresist contrast (γ = 13.8).

10143-6, Session 3

Exposure kinetics of CAR and non-CAR resists

Roberto Fallica, Yasin Ekinci, Paul Scherrer Institut, ETH Zürich (Switzerland)

The exposure kinetics of photoresists for EUV lithography is of great technological importance for modeling and simulating the material response. Devising and predicting the outcome of a lithographic process demands accurate insight of fundamental properties of photoresists, specifically the amount of light absorbed (?, absorption coefficient at EUV) and the exposure rate (also referred to as the Dill parameter C). However, there is a remarkable lack of accurate data available to lithographers, chiefly owing to difficulties in measuring experimentally these two quantities at EUV.

We have recently developed an experimental setup for the measurement of the absorption coefficient and Dill parameters of photoresists at EUV at the XIL-II beamline of the Swiss Light Source. Both the absorption coefficient ? and the three Dill parameters can be extracted at once [1], with unprecedented accuracy. Furthermore we decoupled the effect of the lithographic sensitivity (from the dose-to-clear measurement) from the sheer optical absorption (?). We thus introduced a new concept, the Chemical Sensitivity CS,which accounts for the contribution of all post-absorption reactions to the formation of the resist image.

We present here an investigation on the role that the chemical sensitivity and the exposure rate jointly play in the exposure kinetics. The exposure rate (described by the Dill parameter C) is widely assumed to affect tfhe variation of the relative acid concentration h (where the reaction is usually modeled as a first order kinetics). When the exposure energy E is equal to the dose-to-clear E0, the relative acid concentration takes a characteristic value h0, the value of which can be extrated from the CS, and tuned, for instance by changing PEB and development conditions.

From the experimental measurement of ? and the Dill parameter C, we estimated the relative acid concentration h0 required to clear PMMA, HSQ and four chemically amplified resists from undisclosed manufacturers. The quantum efficiency at the dose to clear was also extracted from the relative acid concentration divided by the absorbed photons at the dose to clear. The relative acid concentration, which has no physical meaning for PMMA and HSQ, is equal to 1. The CAR have different performance and the threshold acid concentration depends on the specific formulation. Interestingly, a CAR with sensitizer (EUV3+S) attains a higher relative acid concentration at the Dose-to-clear, using a lower dose than its baseline (EUV3). The quantum efficiency is less than 1 for nonchemically amplified resists, and larger than unity for CAR; it is specifically higher in the formulation with added sensitizer (EUV3+S). In conclusion, high performance CAR as the EUV3+S can generate higher acid concentration at a comparably lower dose and with a higher quantum efficiency than its baseline EUV3.

[1] R. Fallica, J. K. Stowers, A. Grenville, A. Frommhold, A. P. G. Robinson, Y. Ekinci, “Dynamic absorption coefficients of chemically amplified resists and nonchemically amplified resists at extreme ultraviolet,” J. Micro/Nanolith. MEMS MOEMS 15(3), 033506 (2016).

[2] C. Mack, Fundamental Principles of Optical Lithography: The Science of Microfabrication, John Wiley & Sons, Ltd. ISBN: 978-0-470-01893-4.

10143-7, Session 3

Correlation of experimentally measured atomic scale properties of EUV photoresist to modeling performance: an exploration

Yudhishthir Kandel, Synopsys, Inc. (United States); Jonathan Chandonait, SUNY Polytechnic Institute (United States); Sajan Marokkey, Lawrence S. Melvin III, Qiliang Yan, Benjamin D. Painter, Synopsys, Inc. (United States); Gregory H. Denbeaux, SUNY Polytechnic Institute (United States)

Extreme ultraviolet(EUV) lithography at 13.5 nm stands at the crossroads of next generation patterning technology for high volume manufacturing of integrated circuits. Photo resist models that form the part of overall pattern transform model for lithography play vital role in supporting this effort. The physics and chemistry of these resists must be understood to enable the construction of accurate models for EUV Optical Proximity Correction (OPC).

In this study, we explore the possibility of improving EUV photo-resist models by directly correlating the parameters obtained from experimentally measured atomic scale physical properties; namely, the effect of cross section of EUV photon with photo acid generators in standard chemically amplified EUV photoresist, and associated electron energy loss events. Atomic scale physical properties will be inferred from the measurements carried out in Electron Resist Interaction Chamber (ERIC). This study will use measured physical parameters to establish relation with lithographically important aspects, such as line edge roughness and CD variations. Experimental exposure results from ASML-NXE 3300 scanners will be used with the same resist for validation and usefulness of the inference and relation described above.

The data gathered from these measurements will be used to construct OPC models of the resist. The accuracy of the models compared with the measured data will be presented.

10143-8, Session 4

Stochastics and the phenomenon of line-edge roughness *(Invited Paper)*

Chris A. Mack, Lithoguru.com (United States)

Extreme Ultraviolet lithography (EUVL) has the potential to enable 15nm half-pitch resolution in semiconductor manufacturing, but faces a number of persistent challenges. One of the most incalcitrant problems is line-edge roughness (LER) caused by fundamental stochastic variations in the lithography process. While this problem has been well known for over a decade, very little progress has been made in reducing LER to desired levels without a large increase in the required exposure dose. The magnitude of the challenge is amplified by the relative lack of “stochastic thinking” in the approaches employed by lithographers, who have successfully applied continuum thinking to lithography problems for 50 years.

This talk will seek to address the “stochastic thinking” gap of the lithography community by providing a tutorial covering the fundamentals of roughness formation:

Characterizing LER with metrology. Measuring roughness with a CD-SEM, then analyzing the data to extract the important parameters of roughness standard deviation, correlation length, and roughness exponent (that is, roughness power as a function of frequency).

How LER affects printed features. Using the parameters of roughness standard deviation, correlation length, and roughness exponent to predict three lithographic outcomes: within-feature variation, feature-to-feature variation (local CDU), and extreme events (shorts and bridges).

Stochastic variations that cause roughness. Explaining the nature of stochastic variations such as photon shot noise, absorption, chemical concentration shot noise, and reaction-diffusion in the resist.

How to reduce roughness. Using our models of stochastic variations, define the best approaches for reducing roughness (including the role of exposure dose, resist formulation, and post-processing).

Future work. What research is needed to fill in the unknowns and complete our understanding of the fundamentals of LER formation?

10143-9, Session 5

Enabling sub-10nm node lithography: presenting the NXE:3400B EUV scanner with improved overlay, imaging, and throughput *(Invited Paper)*

Mark A. van de Kerkhof, Roderik van Es, Hans C. Jasper, Alexander Zdravkov, Fabrizio Evangelista, Egbert Lenderink, Leon Levasier, Derk Brouns, David Ockwell, ASML Netherlands B.V. (Netherlands)

With the introduction of its fifth-generation NXE:3400B scanner, ASML has brought EUV to High-Volume Manufacturing for sub-10nm node lithography. This paper presents lithographic performance results obtained with the NXE:3400B, characterized by an NA of 0.33, a Pupil Fill Ratio (PFR) of 0.2 and throughput capability of 125 wafers per hour (or w/h).

Advances in source power have enabled a further increase of tool productivity requiring an associated increase of stage scan speeds. To maximize the number of yielding die per day a stringent Overlay, Focus, and Critical Dimension (CD) control is required. Tight CD control at improved resolution is obtained through a number of innovations: the NXE:3400B features lower aberration levels and a revolutionary new illumination system, offering improved pupil-fill ratio and larger sigma range. Overlay and Focus are further improved through the use of an improved wafer clamp and improved scanner controls.

The NXE:3400B also offers full support for reticle pellicles.

10143-10, Session 5

Line-edge roughness (LER) performance targets for EUV lithography

Timothy A. Brunner, Xuemei Chen, Allen Gabor, Craig D. Higgins, Lei Sun, GLOBALFOUNDRIES Inc. (United States); Chris A. Mack, LithoGuru.com (United States)

EUV lithography patterns generally have larger stochastic variations and Line Edge Roughness (LER) than patterns made with 193nm lithography, a consequence of the fewer EUV photons. The increased LER of EUV patterns has significant yield implications, and therefore LER performance targets are needed. As EUV lithography goes into full production, there will be increasing pressure to trade-off LER performance for resist sensitivity. The ultimate guidance for this tradeoff will be device yield, but preliminary LER guidelines are needed for early EUV production in the next several years.

Our paper will examine how EUV pattern roughness can cause device failure through rare events, so-called “black swans”. We consider the impact of LER on the yield of simple wiring patterns with 36nm pitch, corresponding to 7nm node logic. This is substantially different than older LER specs which were guided by poly gate electrical considerations. The simple yield model will define a “short” to have an insulator CD less than some prescribed minimum, and an “open” to have a conductor CD less than another prescribed minimum. Experimental CD-SEM data for 36nm pitch gratings produced by an NXE 3300 will be used in the analysis. Data from both resist lines and etched lines will be included. In order to better understand the factors influencing LER, we will also use stochastic resist simulations to generate patterns. We will utilize “image fading” to reduce the image log-slope and thereby controllably increase the LER, so as to modulate the wiring failures. We will then combine LER with CD variations to generate a simple one-layer failure model. This model will allow us to extrapolate our yield estimates to full chip areas, and thereby make predictions of rare “black swan” events. Our analysis will guide preliminary LER performance targets for early manufacturing with EUV lithography, including targets for both the EUV resist material as well as targets for the Image Log-Slope.

10143-11, Session 5

Mix-and-match considerations for EUV insertion in 7nm HVM

Xuemei Chen, Allen Gabor, GLOBALFOUNDRIES Inc. (United States)

In a cost-effective scenario, EUV lithography will be initially deployed for a limited number of critical layers while ArF immersion (ArFi) tools are utilized for others. An optimal mix-match control strategy is crucial for the successful insertion of EUV lithography at 7nm technology node. Besides fundamentally different light sources and illumination systems, there are systematic differences between EUV and ArFi tools in terms of masks, projection optics, alignment and imaging control. These differences lead to systematically different image distortion patterns on wafer layers exposed consecutively with EUV and ArFi tools, resulting in mix-and-match overlay errors, especially at the intra-field level. Consequently, the mix-match overlay control strategy for EUV and ArFi should focus on intra-field control, and fully utilize the higher-order intra-field correction models specifically available for EUV systems. Intra-field sampling plans need to be optimized for accurate estimation of the higher-order correction models, and adequate intra-field measurements are required to characterize the EUV specific intra-field signatures.

In this paper, we attempt to address the challenges in the mix and match of EUV and ArFi tools for 7nm HVM. In particular, we will characterize the image distortion signatures that are systematically different between these tool platforms, and develop intra-field correction and sampling strategies to minimize the mix-and-match overlay errors due to such systematic differences between EUV and ArFi. Sources of intra-field overlay errors that are specific to EUV lithography are evaluated, which include: (1) increased impact from mask nonflatness and thickness nonuniformity due to EUV nontelecentricity and electrostatic reticle chucking, (2) increased pattern-dependent and across-slit position dependent image placement errors, (3) different lens fingerprints, and (4) increased differences in pattern placements between product features and test structures. These dissimilarities and their impacts on on-product overlay are analyzed. Advanced correction and sampling strategies are investigated to minimize the on-product overlay errors between EUV and ArFi for 7nm HVM. Various high-order intrafield scanner correction models and their effectiveness in minimizing mix-and-match on-product overlay are evaluated. We also analyze the impact of intra-field sampling plans in terms of model accuracy and adequacy in capturing EUV specific intra-field signatures. Our analysis suggests that more intra-field measurements and appropriate in-die placement of the metrology targets are required to achieve the mix-and-match on-product overlay control goals for 7nm.

10143-12, Session 5

The future of EUV lithography: enabling Moore’s Law in the next decade

Alberto Pirati, Jan van Schoot, Kars Troost, Rob van Ballegoij, Peter Krabbendam, Judon Stoeldraijer, Erik Loopstra, Jos P. Benschop, Jo Finders, Hans Meiling, Eelco van Setten, ASML Netherlands B.V. (Netherlands); Bernhard Kneer, Bernd Thuering, Winfried Kaiser, Tilmann Heil, Sascha Migura, Carl Zeiss SMT GmbH (Germany)

While EUV systems equipped with a 0.33 Numerical Aperture lenses are readying to start volume manufacturing, ASML and Zeiss are ramping up their development activities on a EUV exposure tool with Numerical Aperture greater than 0.5.

The purpose of this scanner, targeting an ultimate resolution of 8nm, is to extend Moore’s law throughout the next decade.

A novel, anamorphic lens design, has been developed to provide the required Numerical Aperture; this lens will be paired with new, faster stages and more accurate sensors enabling Moore’s law economical requirements,

as well as the tight focus and overlay control needed for future process nodes.

The tighter focus and overlay control budgets, as well as the anamorphic optics, will drive innovations in the imaging and OPC modelling, and possibly in the metrology concepts.

Furthermore, advances in resist and mask technology will be required to image lithography features with less than 10nm resolution.

This paper presents an overview of the target specifications, key technology innovations and infrastructure requirements for the next generation EUV systems.

10143-13, Session 5

SAQP and EUV block patterning of BEOL metal layers on IMEC's iN7 platform

Joost P. Bekaert, Paolo Di Lorenzo, Ming Mao, Stefan Decoster, Stephane Larivière, Joern-Holger Franke, Victor M. Blanco Carballo, Bogumila Kutrzeba Kotowska, Frederic Lazzarino, Emily E. Gallagher, Eric Hendrickx, Philippe Leray, Ryoung-Han Kim, Gregory R. McIntyre, IMEC (Belgium); Paul Colsters, Friso Wittebrood, Joep van Dijk, Mark J. Maslow, Vadim Timoshkov, ASML Netherlands B.V. (Netherlands)

The imec N7 (iN7) platform has been developed to evaluate EUV patterning of advanced logic BEOL layers. Its design is based on a 42 nm first-level metal (M1) pitch, and a 32 nm pitch for the subsequent M2-M3 layers. With these pitches, the iN7 node is an 'aggressive' full-scaled N7, corresponding to foundry N5.

Even in a 1D design style, the 16 nm half-pitch M2 layer is particularly challenging for EUV lithography, because this very dense trench pattern contains several tight tip-to-tip configurations. As an alternative to the EUV direct print of the Metal2 layer, the industry is considering self-aligned quadruple patterning (SAQP) to achieve the dense pitch. Then, to create the tip-to-tip configurations, a Block layer is patterned on top of the SAQP pattern, which creates interruptions in the trenches before etching them into underlying layers. The SAQP pattern itself is obtained from a double spacer process around immersion ArF-based core lithography. To avoid up to 4 block patterning masks when using ArF immersion, the block layer is patterned using EUV and may be one of the first layers to adopt EUV lithography.

In this paper, we report on the imec iN7 SAQP+block litho performance and process integration, targeting 16 nm half-pitch M2 patterning for a 7.5 track logic design. The block layer is exposed on an ASML NXE:3300 EUV-scanner at imec, using optimized illumination conditions and state-of-the-art metal-containing NTD resist. Subsequently, the SAQP and block structures are characterized in a morphological study, assessing pattern fidelity and CD/EPE variability after litho and etch.

The work is an experimental feasibility study of EUV insertion, for SAQP+block M2 patterning on an industry-relevant N5 use-case.

10143-14, Session 5

Modeling EUVL patterning variability for metal layers in 5nm technology node and its effect on electrical resistance

Weimin Gao, Synopsys GmbH (Belgium); Lawrence S. Melvin III, Synopsys, Inc. (United States); Itaru Kamohara, Synopsys GmbH (Germany); Vicky Philipsen, Vincent Wiaux, Eric Hendrickx, Ryoung-Han Kim, IMEC (Belgium)

Recent progress of EUVL in source power, up-time, and resist performance makes EUVL more realistic for industrial adoption within high volume manufacturing. Single layer EUV patterning for metal and via layouts is currently the most likely insertion point of EUVL in production. At the 5nm technology node, as metal lines shrink to 14-18nm and tip-to-tip spaces to 21-24nm, any minor process variation may significantly impact the conductivity between metal layers and directly affect device performance. In patterning process the overlay and CD uniformity are among the typical variations.

EUVL has new processing properties related to the reflective system, incident illumination angle and high photon energy that are new sources of lithography process variation that must be comprehended in processing, modeling and Optical Proximity Correction. Specific EUVL effects include shadowing, strong three dimensional mask effect and stochastic resist effects. EUV scanners also have specific effects including across-slit effects due to aberrations and flare which are typically larger than the corresponding effects in ArF scanners.

We have calibrated models against the experimental patterning data of metal layers at 5nm technology. This includes a rigorous resist model for a state of the art metal resist. The resist was exposed on the NXE:3300 at imec and the calibration included the most recent available information on NXE:3300 scanner and mask. We compare the variability predicted by simulations to that observed on wafer for typical metal geometries. In a next step, we then estimate the impact of the variability on wafer to the conductivity between the different layers. To accomplish this, the process flow will first be essembled with a process emulation tool to construct the actual wafer stack and underlying topography. Then a quantitative estimation of patterning process variations based on experimental data and calibrated lithographic models will be performed. These models will be used to build metal and via contours for analysis. The contour overlap between M1-Via-M2 will be analyzed by an edge placement estimation tool. Finally, a conductivity model will be used to calculate the resistance between M1 and M2.

This approach will allow us to quantify the impact of process variations by investigating the individual contribution of each patterning process variation to the conductivity between metals layers. The metehodology can be used to identify the severity of those process variations and find relevant improvement solutions. In this study, a brief discussion of how M3D EUV OPC can help to improve the patterning fidelity will also be presented. At the end of the paper, the potential benefit of high NA EUVL will be discussed, related to the image performance as well as to the resolution improvement for and beyond the 5nm technology node.

10143-15, Session 6

Actinic review of EUV masks: Performance data and status of the AIMS EUV system

Dirk Hellweg, Sascha Perlitz, Renzo Capelli, Carl Zeiss SMT GmbH (Germany)

The EUV mask infrastructure is of key importance for the successful introduction of EUV lithography into volume production. In particular, for the production of defect free masks, actinic review of potential defect sites is required. Such review can determine whether a defect prints, and if it needs to be repaired or compensated for. It also serves as verification for the repair or compensation process performed with the MeRiT® electron beam repair tool, thereby providing a closed loop mask repair solution. For the realization of actinic mask review, ZEISS and the SUNY POLY SEMATECH EUVL Mask Infrastructure consortium started a development program for an EUV aerial image metrology system, the AIMS™ EUV.

Within this program imaging, measurement and mask handling capabilities have been established on the prototype system and customer measurements are performed on a regular basis.

In this paper, we provide an update on the program and the system qualification status. Achievements from more than one year EMI program participants measurement campaigns on the prototype system will be provided and measurement data on the system's key specifications will be shown.

10143-16, Session 6

Printability and actinic AIMS review of programmed mask blank defects

Erik Verduijn, Pawitter Mangat, Obert R. Wood, Jed H. Rankin, Jaewoong Sohn, Yulu Chen, Francis Goodwin, Harry J. Levinson, GLOBALFOUNDRIES Inc. (United States); Renzo Capelli, Sascha Perlitz, Dirk Hellweg, Carl Zeiss SMT GmbH (Germany); Ravi K. Bonam, Shravan Matham, Nelson M. Felix, Daniel A. Corliss, IBM Corp. (United States)

Pit and bump defects resulting from the manufacturing process of EUV (extreme ultraviolet) mask blank substrates can result in masks with non-repairable, yield-killing wafer printing multilayer defects. In particular for logic back-end-of-line metal layers, a single printing defect on a critical location of the mask may render it unusable. As pitches become tighter with each advancing node, it is more and more likely a defect may print at a critical location. As a result it is important to understand the printing behavior of these defects, and how they may be identified and repaired on mask prior to release to manufacturing.

To study these defects a line-space (56nm, 80nm and 104nm pitch) EUV test mask was made on a blank substrate with etch-defined programmed substrate pits (7nm, 11nm and 15nm depth). The mask defect locations were reviewed with the AIMSTM actinic mask review tool at Carl Zeiss SMT-Oberkochen. This mask was subsequently printed on the NXE:3300 EUV lithography scanner at IBM Research-Albany and the corresponding defect locations on wafer were reviewed by SEM (scanning electron microscopy) on wafer.

We present the imaging behavior of these programmed blank substrate defects on wafer by SEM review and on mask by AIMSTM actinic mask review. We will show which categories of programmed blank substrate defects on this test mask can create wafer printing defects and how they can be mitigated. Furthermore, we show that these wafer printing images correlate very closely to those captured by the AIMSTM tool, which show its capability in predicting the printing aspects of this type of substrate blank defect. Shown below, centered at the defect location at 200nm field of view, the imaging impact of an 11nm mask-blank programmed substrate pit on a 80nm pitch line-space pattern (Left wafer print, right AIMSTM). The bridging impact to the line space pattern can clearly be seen.

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To study these defects a line-space (56nm, 80nm and 104nm pitch) EUV test mask was made on a blank substrate with etch-defined programmed substrate pits (7nm, 11nm and 15nm depth) and bumps (12 nm height). The mask defect locations were reviewed with the AIMS[TM] actinic mask review tool at Carl Zeiss SMT-Oberkochen. This mask was subsequently printed on the NXE:3300 EUV lithography scanner at IBM Research-Albany and the corresponding defect locations on wafer were reviewed by SEM (scanning electron microscopy) on wafer.

We present the imaging behavior of these programmed blank substrate defects on wafer by SEM review and on mask by AIMS[TM] actinic mask review. We will show which categories of programmed blank substrate defects on this test mask can create bridging or severe necking wafer printing defects. Furthermore, we show that these wafer printing images correlate very closely to those captured by the AIMS[TM] tool, which show its capability in predicting the printing aspects of this type of defect.

10143-17, Session 7

Novel membrane solutions for the EUV pellicle: better or not?

Ivan Pollentier, Jae Uk Lee, Marina Timmermans, Christoph Adelmann, Houman Zahedmanesh, Cedric Huyghebaert, Emily E. Gallagher, IMEC (Belgium)

A protective membrane – a pellicle – will be used to prevent yield loss during EUV lithography exposure, just as it was for 193nm lithography. The pellicle must be thin enough to transmit EUV light, yet strong enough to withstand vacuum pumping cycles and handling. Membrane solutions for ~ 80W exposure exist. Our focus is developing a membrane solution for 250W exposure power. The main pellicle challenge is the identification of a membrane material that has very high transmission at EUV wavelengths. Additionally, absorption during lithographic exposure results in high thermal and mechanical load for the pellicle, which can cause yield problems. The current candidates for pellicle membranes such as poly-silicon and silicon nitride cannot withstand 250W power conditions, therefore alternative materials will be required for the future HVM pellicle.

At imec, a variety of novel membrane material options are investigated for the HVM pellicle application. One promising group is based on carbon nanotubes (CNT). In this paper we outline different CNT based process options, and report results on their optical, thermal, and mechanical performance. In addition, we will report on their uniformity and robustness towards scanner application. Finally, the family of CNT-based membrane options will be compared to promising candidates fabricated using conventional film approaches that do not have a CNT layer.

10143-18, Session 7

Impact of noise sources and optical design on defect sensitivity for EUV actinic blank inspection

Yow-Gwo Wang, Univ. of California, Berkeley (United States) and Lawrence Berkeley National Lab. (United States); Andrew R. Neureuther, Univ. of California, Berkeley (United States); Patrick P. Naulleau, Lawrence Berkeley National Lab. (United States)

In this paper, we will discuss the impact of various noise sources: speckle noise, camera noise, and photon shot noise on defect signal-to-noise ratio (SNR) of the dark field actinic blank inspection tool, and also the impact of pixel size and photon density on defect SNR. To figure out what would be the optimum tool design which can have high defect SNR to meet the desired capture rate, and at the same time with a reasonable inspection time and EUV source power requirement.

Therefore, in order to include all these noise sources into consideration, we use a thin mask model which include both the defect and mask roughness profile in generating the aerial image. From the output aerial image, we use pixel binning to mimic the results under various pixel sizes and introduce the shot noise on the same image under various photon density situations. From this image, we can discuss the impact of pixel size and photon density on defect signal and the noise.

For example, we try to understand what would be the impact of photon shot noise and camera noise on defect SNR under fixed photon density (source power) and what would be the minimum photon density for each pixel size to reach target defect SNR (SNR = 13)? The sample defect shown here is a bump phase defect has a height about 0.5 nm and FWHM is 60 nm. The numerical aperture (NA) of the inspection system is 0.25 with a central obscuration equals to 0.4 sigma. As shown in Figure 1, the improvement of defect SNR under fixed photon density is reduced as pixel size increases. The reason is that even more photons and stronger defect signal can be achieved by larger pixel. The increase of photon shot noise compensates the increase of defect SNR, so the defect SNR saturates even with larger

pixel size. Table 1 shows the photon density you need for different pixel size design to reach target defect SNR (SNR = 13). The result shows that as pixel size is larger than 200 nm, the required photon density is saturated at 3 photons/nm2. This means that with a specific EUV source power (photon density), the minimum pixel size for the inspection tool is 200 nm to get the desired defect capture rate. The example shown here indicates the complicated relationship between various noise sources and signal, and its related tool design like pixel size and photon density.

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10143-19, Session 7

High-NA EUV optical testing of exposure and metrology tools

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As exposure and metrology tools extend toward higher numerical apertures, it becomes increasingly difficult to characterize aberrations in the optics via standard interferometric techniques. At the same time, minimizing aberrations becomes increasingly important to ensure that these tools can achieve diffraction-limited performance.

In this paper we compare two non-interferometric wavefront sensors suitable for in-situ high-NA EUV optical testing. The first is the AIS sensor, which has been deployed in both inspection and exposure tools. AIS is a compact, optical test that directly measures a wavefront by probing various parts of the imaging optic pupil and calculating localized wavefront curvature from relative focus shifts. Because the size of the probe is NA-independent, AIS does not suffer from the systematic aberrations and geometric effects that plague interferometric tests such as shearing interferometry and the Hartman test at high NA. When AIS is implemented in exposure tools, a grating-on-grating contrast monitor is placed at the wafer plane to determine best focus. This monitor consists of a scanning grating packaged together with a custom-built high efficiency EUV photodiode.

The second is an image-based technique that uses an iterative algorithm based on simulated annealing to reconstruct a wavefront based on matching aerial images through focus. In this technique, customized illumination is used to probe the pupil at specific points to optimize differences in aberration signatures.

Both AIS and the image-based technique were preformed at the SHARP EUV defect review microscope at the Advanced Light Source at LBL.

10143-20, Session 7

Status of multilayer reflective optics

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The peak reflectance of multilayer reflective optics is generally considered to be the key parameter of an EUVL optical system, but the bandwidth of the multilayers is equally important since it also determines the transmission of the system.

In reality, there are much more factors that determine the optics performance. For instance the figure of the optics, with nm accuracy, and how this is affected by the approximately half micron of multilayer coating on top, and the coating induced stress. But also how the high frequency roughness of the substrates affects the multilayer performance.

Another issue is the reflectance for out of band radiation, both deep UV and infrared light. What can be done to reduce this, and what is the effect on 13.5 nm reflectance?

Furthermore lifetime issues, radiation induced damage, thermal stability, oxidation and cleaning resistance.

In this paper we will present the present status of the multilayer coated optics, including the latest achievements.

10143-21, Session 7

Near normal to grazing incidence scattering: investigating surface structures at PTB

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With EUV lithography (EUVL) steppers for high volume manufacturing (HVM) being available, in-line metrology of surface structures becomes a crucial enabler of process control and yield enhancement. Scatterometry as a photonic non-contact method offers the potential for fast in-line metrology as well as extendability to smaller structures. Grazing incidence small angle X-ray scattering is well established for surface characterization with a high sensitivity but the elongated beam spot size limits the practical applications for relevant metrology field sizes. Rotating the incidence angle closer to normal incidence and simultaneously tuning the incident photons to longer wavelengths (EUV Scatterometry) allows to significantly decrease the sampled spot size but is also coupled with a reduction in information density. This raises the question, what is the minimal measurement data requirement for a reliable surface structure reconstruction.

At this time, we don't deliver a final answer but will present an exploration of the scatterometry parameter space from grazing to near normal incidence in the soft X-ray range (1 -13 nm). Measurements were performed at the PTB synchrotron radiation laboratory using state of the art e beam written silicon gratings as representative samples. We present experimental data as well as simulation results to provide a first insight into optimized measurement schemes for next generation EUV Scatterometry.

10143-22, Session 9

Comparison of state-of-the-art EUV resist platforms toward <13nm resolution for high-volume manufacturing *(Invited Paper)*

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Extreme ultraviolet lithography (EUVL) with 13.5 nm wavelength is the main option for patterning sub-10 nm resolution for future nodes in the semiconductor industry. However, EUV resists are becoming a limiting factor in the pursuit of further shrinkage. EUV allows for higher resolution with its 14x shorter wavelength compared to DUV. On the other hand, with the lower number of photons in a given dose, different absorption and activation mechanisms compared to DUV, and with the need for tighter control of resist blur needed for high resolution, currently used chemically

amplified resists (CARs) reached their limits. The fundamental trade-off relation between resolution, line-edge roughness and sensitivity, the so-called RLS triangle, limits to obtain a sub-16 nm process with acceptable process window. Low absorption, lack of high resolution capacity, high roughness due to photon shot noise (PSN) are major limitations for existing EUV resists. Alternative EUV resist platforms to achieve high performance at high resolution have been studied, however the data is scattered, and it is not straightforward to compare data generated by different tools, at different dates and with different metrology. EUV interference lithography (IL) at the Paul Scherrer Institute (PSI) is a powerful research tool printing high resolution periodic images by the interference of two or more spatially coherent beams through a transmission-diffraction grating mask. As the result of the collaboration between ASML and PSI, we present a comparative study of the high-resolution performance of three state-of-the-art EUV resist platforms: chemically amplified resist (CAR), molecular resist and metal containing non-CAR resist. For good comparison, exposures are done at the same day with the same mask at PSI, and measured with ASML metrology. Resist performance is measured in terms of ultimate printing resolution, line edge roughness (LER), sensitivity (S or exposure dose) and exposure latitude (EL). Comparability with NXE data, the current status, trends, and potential roadblocks for EUV resists are also discussed. The results confirm the feasibility of EUV lithography in high volume manufacturing regarding resist material performance.

10143-23, Session 9

Exploring the readiness of EUV photo materials for patterning advanced technology nodes

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Imec is currently driving the extreme ultraviolet (EUV) photo material development within the imec material and tool supplier hub. EUV baseline processes using the ASML NXE3300 full field scanner tool have been setup for the critical layers of the imec N7 (iN7) BEOL process modules with a resist sensitivity of 40mJ/cm2 and 60mJ/cm2 for metal, block layers and vias layer, respectively. A feasibility study on higher sensitivity resists for HVM has been recently conducted looking at 16nm dense line-space with a dose target of 20mJ/cm2. Such a study reveals that photoresist formulations with a cost-effective resist sensitivity are feasible today. Moreover, recent advances in enhanced underlayers are further offering novel development opportunities to increase the resist sensitivity. However, line width roughness (LWR) and pattern defectivity at nano scale are the major limiting factors of the lithographic process window and further efforts are needed to reach an HVM maturity level.

In this paper we will present the results of the screening for such a class of photo materials and we examine in detail both the lithography and etch patterning results for the best performing photoresists. We also report various routes to mitigate the LWR, line collapse and resist scumming by integrated or post processing solutions.

As metal containing resists are becoming part of the EUV material landscape, we also review the manufacturing aspects of a such class of resists looking at pattern defectivity and metal cross contamination on the process equipment.

We further discuss the fundamental aspects of photo materials from a light-matter interaction standpoint looking at the EUV light absorption and the total electron yield for different photo materials towards a better understanding of the photon efficiency. From a lithographic process standpoint, we also study the resist dissolution properties.

Finally, we will be discussing the implementation aspects of these materials and processes in advanced iN7 patterning modules.

10143-24, Session 9

Metal oxide EUV photoresist performance and fab compatibility readiness

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Inpria is developing directly patternable, metal oxide hardmasks as robust, high-resolution photoresists for EUV lithography. Inpria's resist materials, based on a tin-oxide platform with extremely high absorbance (15-20/μm), are designed to reduce the impact of photon shot noise compared to conventional resists. These metal oxide resists have ~40:1 etch selectivity into a typical carbon underlayer, thereby enabling ultrathin 20nm resist films with minimal pattern collapse. Inpria resists have achieved 13nm half-pitch resolution at 26mJ/cm2 on an ASML NXE:3300B EUV scanner. Newer formulations have achieved 16nm half-pitch at 20mJ/cm2 and a process window over 120nm DOF@11%EL.

We continue to improve photospeed and will provide an update on imaging performance, including process window, RLS, relevant 2D metrics, and LCDU. We also will provide a comprehensive review of the status of progress against key challenges and proposed solutions for integrating Inpria's metal oxide resist into the fab: metal cross-contamination on process equipment, outgassing, defectivity, OPC, etch, and metrology. We bring this together through integration of an Inpria resist as a block layer in IMEC's N7 metal patterning process.

10143-25, Session 9

State-of-the-art EUV materials and processes for the 7nm node and beyond patterned by EUV interference lithography

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Extreme ultraviolet lithography (EUVL, λ = 13.5 nm) being the most likely candidate to manufacture electronic devices for future technology nodes is now predicted to be introduced in high volume manufacturing (HVM) at the 7 nm logic node, at least at critical lithography levels [1]. With this impending introduction, it is clear that excellent resist performance at ultra-high printing resolutions (below 20 nm line/space L/S) is ever more important and pressing. Nonetheless, EUVL has faced many technical challenges towards this paradigm shift to a new lithography wavelength platform. Since the inception of chemically amplified resists (CARs) they have been the base upon which state-of-the art photoresist technology has been developed from. Resist performance as measured in terms of printing resolution (R), line edge roughness (LER), sensitivity (S or exposure dose D) and exposure latitude (EL) needs to be improved but there are well known fundamental trade-off relationships (LRS trade-off) among these parameters that hamper their simultaneous enhancement in CARs. Here, we present a comparative study of the most promising EUVL materials tested by EUV interference lithography (EUV-IL) with the aim of resolving features down to 11 nm half-pitch (HP), while focusing on resist performance at 16 and 13 nm HP as needed for the 7 and 5 nm node, respectively. We show the status of EUV resist development and review the progress. EUV-IL has enabled the characterization and development of new resist materials before commercial EUV exposure tools become available and is therefore a powerful research and development tool. With EUV IL, high resolution

periodic images can be printed by the interference of two or more spatially coherent beams through a transmission-diffraction grating mask [2-3]. For this reason, our experiments have been performed by EUV-IL at Swiss Light Source (SLS) synchrotron facility located at the Paul Scherrer Institute (PSI) [4]. Having the opportunity to test hundreds of EUVL materials from vendors and research partners from all over the world at PSI, we will give a global update on the resist performance for all resist platforms tested in this paper.

10143-26, Session 9

High-volume manufacturing compatible dry development rinse process: patterning and defectivity performance for EUVL

Safak Sayan, Iulian N. Hetel, Danilo De Simone, Geert Vandenberghe, IMEC (Belgium)

There are many knobs available that change the chemical and physical properties of the material to "break" the RLS (Resolution, Sensitivity, Line edge/width roughness) trade-off, however those are not enough today to realize a material to satisfy all requirements at once for 7nm technology and beyond.

DDRP improves the ultimate achievable resolution via pattern collapse mitigation, hence the priority requirements for the EUV photoresist development may be changed with more focus on Sensitivity and LWR. This may potentially provide a new conceptual approach towards EUV PR development for DDRP applications.

In our previous contributions, we have demonstrated pattern collapse (PC) mitigation via DDRP on different EUVL photoresists (including different resist platforms), achieving ultimate resolution (Figure.1) and exposure latitude improvements [1,2]. It was also shown that increasing photoresist thickness can be a viable option towards improving LWR while maintaining reasonable exposure latitude for a given pitch and structure. Selection of photoresist material remains to be crucial for LWR performance of DDRP, the cross-sectional profile being the most critical factor for DDRM LWR performance.

In this contribution, we report patterning and defectivity (both blanket and pattern defects) performance of HVM compatible (all aqueous) dry development rinse material while benchmarking it to previous formulations. We will also report on resolution enhancement on 2-dimensional metal lines (Figure.2).

[1] S. Sayan et al. Proc. of SPIE Vol. 9425 942516-1

[2] S. Sayan et al. Proc. of SPIE Vol. 9776 977610-1

10143-27, Session 9

Sensitivity enhancement of the high-resolution xMT molecular resist for EUV lithography

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EUV lithography (EUVL) is considered to be one of the most promising candidates in replacing photolithographic tools for future semiconductor manufacturing needs. A wide array of new materials have been introduced [1–3], but to date no photoresist has been able to simultaneously meet resolution, linewidth roughness and sensitivity requirements laid out in the International Technology Roadmap for Semiconductors. We are developing a negative tone molecular resist platform, known as xMT, for EUVL application. The xMT resist demonstrates a good combination of photo speed, low line edge roughness (LER) and high-resolution patterning [4]. Here we report our ongoing efforts to optimize the formulation to further improve the performance of this material.

xMT-213 is a three compound negative tone chemically amplified resist with a base molecular resin, an epoxy crosslinker, a photo-acid generator (PAG) and optionally a quencher. Recent work has been undertaken to improve resist purity to SEMI specifications. EUV exposures have been undertaken before and after purification, using the XIL beamline of the Swiss Light source at the Paul Scherrer Institute [5]. High resolution patterning at 14 nm half pitch and 16 nm half pitch showed that the purified formulation, with removed contaminants, was significantly more sensitive than the standard formulation. The dose required for the optimized resist when no quencher is added is 64% that of the standard formulation. The dose required for the optimized resist with quencher is 88% that of the standard formulation. The line edge roughness of the lines is improved by 5–10% using a separately purified quencher in conjunction with the optimized xMT and crosslinker, compared to the standard formulation. The production of resist with less contamination therefore has significant performance benefits.

Additionally we also present enhancements to the base molecular resin itself. One variant, EX1, includes additional functional groups designed to increase sensitivity, whilst another variant, EX2, is designed to stiffen the molecule to reduce line edge roughness. Results are again presented from exposures at PSI. The formulation is non-purified and uses 2.5% quencher addition. The EX1 variant exhibits a significant sensitivity improvement of around 25% with similar LER values as xMT213. The EX2 variant exhibits improved LER values especially at half pitches below 16nm, with a 20% LER improvement at 14nm hp, giving an LER of 2.7nm. Also, 11nm hp lines can be shown using EX2.

[1] Stowers, J. K., et al., Proc. SPIE , 7969, 796915, (2011).

[2] Krysak, M., et al., Proc. SPIE 7972, 79721C (2011).

[3] Cardineau, B., et al., Proc. SPIE 9051, 90511B (2014).

[4] Frommhold, A., et al., Proc. SPIE 9776 (2016).

[5] Päivänranta B., et al., Nanotechnology Vol. 22, 375302 (2011).

10143-28, Session 10

Mechanisms of EUV exposure: electrons, holes, and molecular interactions

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In extreme ultraviolet (EUV) lithography, 92 eV photons are used to expose photoresists. Current EUV photoresists are composed of photoacid generators (PAGs) in polymer matrices. Secondary electrons (2 - 80 eV) created in resists during EUV exposure play large role in acid-production. There are several proposed mechanisms for electron-resist interactions: internal excitation, electron trapping, and hole-initiated chemistry.

Here, we will describe the contributions of electron trapping and hole-initiated chemistry to resist sensitivity. Using a well-established technique of measuring acid-production (or quantum yield) in resists due to EUV exposure with an acid-sensitive dye, we will determine relationships between PAG chemical structures and quantum yields. By applying this same technique to polymers in the absence of PAGs, we will study the acid-generating efficiency of hole-initiated chemistry in phenolic and non-phenolic resists. Cyclic voltammetry and bulk electrolysis will be used to show acid generation upon PAG reduction or polymer oxidation, as well as determine structure-function relations PAGs and polymers and acid generation efficiency.

By analyzing data generated in these studies, we can determine the relative efficiencies of electron trapping and hole-initiated chemistry. Understanding the mechanisms involved in EUV exposure will aid in the development and optimization of chemically amplified and more exotic EUV resists systems.

10143-29, Session 10

EUV resist development for sub-7nm Node

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Extreme ultraviolet (EUV) lithography has been recognized as a promising candidate for the manufacturing of semiconductor devices as LS and CH pattern for 7nm node and beyond. EUV lithography is ready for high volume manufacturing stage. For the high volume manufacturing of semiconductor devices, significant improvement of sensitivity and line edge roughness (LWR) and Local CD Uniformity (LCDU) is required for EUV resist. It is well-known that the key challenge for EUV resist is the simultaneous requirement of ultrahigh resolution (R), low line edge roughness (L) and high sensitivity (S). Especially high sensitivity and good roughness is important for EUV lithography high volume manufacturing.

We are trying to improve sensitivity and LWR/LCDU from many directions. From material side, we found that both sensitivity and LWR/LCDU are simultaneously improved by controlling acid diffusion length and efficiency of acid generation using novel resin and PAG. And optimizing EUV integration is one of the good solution to improve sensitivity and LWR/LCDU. We are challenging to develop new multi-layer materials to improve sensitivity and LWR/LCDU. Our new multi-layer materials are designed for best performance in EUV lithography system. From process side, we found that sensitivity was substantially improved maintaining LWR applying novel type of chemical amplified resist (CAR) and process. EUV lithography evaluation results obtained for new CAR EUV interference lithography. And also metal containing resist is one possibility to break through sensitivity and LWR trade off. In this paper, we will report the recent progress of sensitivity and LWR/LCDU improvement of JSR novel EUV resist and process.

10143-30, Session 10

Driving down defect density in composite EUV patterning film stacks

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Initial readiness of EUV patterning was demonstrated in 2016 with IBM Alliance's 7nm device technology. As the technology matures, further improvement is required in the area of blanket film defectivity, pattern defectivity, CD uniformity, and LWR/LER. As the focus shifts to driving down the 'effective' k1 factor and enabling the second generation of EUV patterning, new techniques and methods must be developed to reduce the overall defectivity, mitigate pattern collapse, and eliminate film-related defects. Also, CD uniformity and LWR/LER must be improved in terms of patterning performance. IBM Corporation and Tokyo Electron Limited (TELTM) are continuously collaborating to develop manufacturing quality processes for EUV.

In this paper, we review the ongoing progress in track based processes (coating, developer, baking) that are required to enable EUV patterning. We will discuss our work for defect mitigation, with a special emphasis on defects related to pattern collapse and film coating processes, as well as the optimization results of CD uniformity and LWR/LER.

10143-31, Session 10

Lithographic stochastics: extrapolating to 7sigma

Robert Bristol, Intel Corp. (United States)

No Abstract Available

10143-32, Session 11

Reducing EUV mask 3D effects by alternative metal absorbers

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Over the recent years EUV lithography has demonstrated the patterning of ever shrinking feature sizes (enabling the N7 technology node and below), while the EUV mask has remained unaltered using a 70nm Ta-based absorber. This has led to experimentally observed Mask 3D (M3D) effects at wafer level, such as best focus shifts through pitch, contrast loss and pitch-dependent telecentricity errors. M3D effects are induced by the interaction between the oblique incident EUV light and the patterned absorber with typical thickness values in the order of several wavelengths. Here we exploit the optical properties of the absorber material of the EUV mask as M3D mitigation strategy.

Using rigorous lithographic simulations we screen potential absorber materials for their optical properties and their optimal thickness for minimum best focus variation through pitch at wafer level. Figure 1 illustrates that metals like Ni and Co have the capacity to minimize M3D effects at significantly smaller absorber thickness compared to the conventional Ta-based absorber. The main cause is the higher extinction coefficient at EUV wavelength of these metals.

In order to validate the rigorous simulation predictions and to test the processing feasibility of the alternative absorber materials in a fast learning cycle we started an experimental route on wafer substrates. In this work we present the film characterization in terms of the composition, crystallinity and roughness obtained by different film analysis techniques. Figure 2 shows the X-ray diffraction analysis performed on Ni films in the range of the lithographic optimized thickness. These spectra indicate micro-crystallinity growth within the Ni film.

Furthermore through EUV reflectometry using a synchrotron source the optical properties of these nanometer-thick Ni and Co films are derived. We also report on our learnings from first patterning tests on these films, including profile information.

Feeding back these experimental results into the rigorous EUV lithography simulator enables us to predict realistic M3D reduction at imaging level by changing the mask absorber material. The complete imaging analysis of alternative absorber materials includes contrast, shadow bias, telecentricity error and best focus for generic building blocks through pitch such as trenches, two-bars and contact holes at numerical aperture (NA) 0.33 using different illumination settings. In addition, the M3D mitigation by absorber material is tested by process window comparison of a foundry N5 specific metal clip, which is extended to future anamorphic high NA EUV lithography.

In conclusion, we present a comprehensive study to reduce M3D effects

by alternative metal absorbers like Ni and Co. The study consists of an experimental part, including characterization and patterning evaluation, as well as imaging predictions with rigorous lithographic simulation at current and future NA.

10143-33, Session 11

Experimental verification of AI decomposition-based source and SRAF placement optimization for horizontal M1 logic two-bar building blocks in 0.33NA EUVL

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The insertion of EUV lithography in 7 nm and beyond technology nodes is likely to coincide with a transition of M1 layer 2D to 1D multi-pitch grating based constructs ensuring a pattern complexity reduction and hence allowing further shrinking. 1D constructs include line/space patterns ranging from the tightest design pitch to semi-isolated focus-sensitive features such as a dark field n-bar (n ≥ 2).

Traditional contrast-aware pupil optimization for a dark field two-bar building block yields a dipole matching its local pitch. We will experimentally verify that this will not work for EUV systems due to its chief-ray-angle-induced symmetry breaking. Under the conditions of maximum contrast the CD Bossungs of the top and bottom trenches of this feature with dimensions of CD1 = CD2 = 16 nm, local pitch = 32 nm and global pitch ≥ 160 nm are severely tilted, leading to a strongly reduced overlapping process window.

We will explain and experimentally verify how pattern fidelity of this feature can be restored by applying aerial image decomposition.

In the first part we will show that symmetrization of the intensity spectrum across the diffraction orders will drive optimal conditions of illumination such that the CD difference between top and bottom trench is lifted and figures of merit such as overlapping process window, contrast, and non-telecentricity will be co-optimized. In particular the balancing between contrast and mask 3D effects can be achieved by introducing asymmetric pupil solutions with illumination bands ensuring large overlapping process windows and balanced intensities across the diffraction orders excluding the necessity of modifying the mask.

In the second part the experimental verification of optimization through aerial image decomposition is being extended to the optimal placement of sub-resolution assist-features (SRAFs). We find that the feature's aerial image condition changes when placing SRAFs in its optimal vicinity and that the impact of the strong first diffraction order on the intensity imbalance is strongly reduced as compared to the case of an isolated two-bar, enabling an overlapping process window enhancement already with more conventional illumination conditions (e.g. symmetric dipole-Y).

We will conclude by discussing the interdependencies between source and SRAF placement optimization for mitigating these mask 3D effects for a range of global pitches of the dark field two-bar from 320 nm down to 96 nm, which might already be a pitch regime resembling dense patterning options likely to be implemented in post 7 nm technology nodes.

10143-34, Session 11

Investigation of alternate mask stacks in EUV lithography

Martin Burkhardt, IBM Thomas J. Watson Research Ctr. (United States)

Initial readiness of EUV patterning was demonstrated in 2016 with IBM Alliance's 7nm device technology. The focus has now shifted to driving the "effective" k1 factor and enabling the second generation of EUV patterning. In order to succeed with such low-k1 lithography at EUV wavelength, we need to be able to print a grating at high contrast similar to ArF immersion tools, where a contrast exceeding 0.95 is achieved routinely. In EUV, high contrast can currently only be achieved using monopole illumination, a technique that does not lend itself to process integration due to removal of wafer side telecentricity and resulting overlay problems. And even with monopoles, the contrast is not as high as can be achieved at ArFi. The case for dipoles is even worse. For dipole illumination, we collect only 0th order light and only one 1st diffracted order for each pole. This means that the final image for horizontal l/s patterns can be approximated by only four sine waves, one TE and one TM wave for each of the poles.

The EUV absorber is not only an attenuator but also a dielectric, so we observe defocus shifts through pitch, and different image location for the two monopole images of the dipole [Shih2015,Burkhardt2015]. This is a result of the fact that the diffraction coefficients are complex valued and aren't close to the real axis in the complex plane, with the 0th order phase set to zero. The difference in magnitude of 0th and 1st diffracted orders gives an indication of the contrast of the image contribution, while the phase difference gives an indication of the location of the resulting image. If we take as an example an absorber consisting of a stack of Al and TaN, which has approximately equal absorption, but very different dielectric index, we can vary the ratio of the two films and see the effect that the variation in dielectric index has on imaging. The spatial difference between the images in the wafer plane is minimized for a pure Al absorber, yet surprisingly the resulting contrast is lower for an Al absorber. This is because contrast can be reduced by other effects, such as reduced reflection and increased absorption of EUV light on index-matched materials such as Al.

The absorber phase effects on imaging has been covered before using a technique to map phase variations onto Zernike polynomials and using aberration theory to correlate the effects with lithographic parameters [Finders2016], which was based on some prior theoretical work [Erdmann2016]. For imaging, both magnitude and phase of the diffracted orders are critical and we believe that using phasor diagrams are very useful and hopefully more intuitive in investigating such phase effects. We use such diagrams to investigate the physical effects of absorber material and thickness choice of the stack.

10143-35, Session 11

Vote-taking for EUV lithography: a radical approach to mitigate mask defects

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Defect-free masks for EUV lithography remains a challenge. Masks for EUV lithography not only require a more complicated film stack comprised of a reflective multilayer coating with 40 bilayers of Mo and Si overcoated with a patterned absorber but also must contend with phase defects due to imperfections in the surface of the mask substrate and with fall-on particles due to the lack of a protective pellicle. Mask patterns with a high reflective pattern density, such as metal masks, are a particularly daunting challenge. Protective thin-film pellicles for EUV lithography have made substantial progress, but will likely cause an undesirable 10 to 20% EUV transmission loss. Even if the mask is perfect when new and pellicle-protected, mask degradation from hydrogen bubbles may grow defects underneath the pellicle. The EUV lithography community is energetically searching for

imaging methods to confidently print defect-free patterns over long production runs.

This paper will propose the EUV application of "Vote-taking Lithography". The idea[1] is to expose N imperfect patterns, each with 1/N the exposure dose, to build up a "perfect" pattern. We expect that the defects in each pattern will be uncorrelated, and so the defective image will tend to be corrected by the "good" patterns from the other masks with no defects. There are strong pros and strong cons to this approach. The pros include:

• Tolerance to small errors from imperfect blanks or absorber patterns

• Same total expose dose as normal mask - avoid EUV-absorbing pellicles

• Potential for reduced mask cost, if high resolution inspection can be avoided

• Reduced mask contribution to LER, assuming no correlation between different masks

• Possible to improve dose uniformity by more averaging, and possible compensation

The cons include:

• Reticle handling and alignment of N masks – currently a large throughput limiter

• Cost of N less perfect masks relative to one perfect mask

Our paper will demonstrate the effectiveness of this idea via lithographic simulation.

[1] Chong-Chen Fu et al., "Elimination Of Mask-Induced Defects With Vote-Taking Lithography", SPIE 633, p. 270 (1986).

10143-36, Session 11

Reticle enhancement techniques toward N5 metal2

Werner Gillijns, Ling Ee Tan, Darko Trivkovic, Victor M. Blanco Carballo, Joost P. Bekaert, Ryoung-Han Kim, Gregory R. McIntyre, IMEC (Belgium)

The imec N7 (iN7) platform has been developed to evaluate EUV patterning performance with design rules equivalent to foundry N5 node. This node has a 42 nm pitch for metal 1 layer and 32 nm pitch for the subsequent metal 2 layer and metal 3 layer and it is considered to be the first node for which industry commonly will insert EUV into production.

This paper will focus on the M2 layer. It has a metal pitch of 32nm and a tip-to-tip of 25nm. Imec is looking at EUV single exposure (SE) as well as SAQP+EUV Block SE as possible candidates. For the 32nm single print a source optimization was performed, while minimizing non-telecentricity, pattern shift and best focus shift. The resulting source was verified on some important features. Following this an OPC model was calibrated and OPC was tuned. For the SAQP+Block option we focus our attention on the SMO, modeling and OPC of the Block layer.

In both cases simulated process windows can be generated and both options can be compared.

10143-37, Session 12

Considerations for pattern placement error correction toward 5nm node

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In previous work, we introduced an attractive pattern correction technique as a post lithography treatment, named "CD-Healing". In this previous work, we demonstrated the effectiveness of post-treatment process for local-CDU improvement, CER (Circle edge roughness) suppression and placement error correction on random hole array imaged with 193-immersion exposure [1]. This paper will attempt to understand the efficacy of post-processing for the correction of placement error on line-cutting pattern fabricated by EUV exposure in 1D layout design.

10143-39, Session 12

Enabling full-field OPC correction via dynamic model generation

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As EUV lithography marches closer to reality for high volume production, its peculiar modeling challenges related to both inter- and intra- field effects has necessitated building OPC infrastructure that operates with field position dependency. One such methodology is a piecewise constant approach where static input models are assigned to specific x-positions within the slit. OPC and simulation can assign the proper static model based on tile-level placement. However, in the realm of 7nm and 5nm feature sizes, small discontinuities in OPC from piecewise constant model changes can cause unacceptable levels of EPE errors. Dynamic Model Generation (DMG) can be shown to effectively avoid these dislocations by providing unique mask and optical models per simulation region, allowing a true continuum of models through field. DMG allows unique models for EMF, apodization, aberrations, etc to vary through the entire field and provides a capability to precisely and accurately model systematic field signatures.

10143-40, Session 12

Rigorous 3D electromagnetic simulation of ultrahigh efficiency EUV contact-hole printing with chromeless phase shift mask

Stuart Sherwin, Lawrence Berkeley National Lab. (United States); Thomas V. Pistor, Panoramic Technology Inc. (United States); Andrew R. Neureuther, Univ. of California, Berkeley (United States); Patrick P. Naulleau, Lawrence Berkeley National Lab. (United States)

Contact-hole layer patterning is expected to be one of the first applications for EUV lithography. Conventional dark field absorber masks, however, are extremely inefficient for these layers, placing even more burden on the already challenging source power demands [1]. To address this concern, a chromeless checkerboard phase-shift mask for 25-nm dense contacts was shown to provide a throughput gain of 8x based on SHARP and 7x based on the Berkeley MET [1]. These promising experimental results warrant both assessment for implementation in practice and rigorous simulations for diagnosing 3D mask effects.

This paper starts from the simplified thin-mask model used to design the original experiment, uses rigorous 3D simulation of etched multilayer masks to fully explain the throughput gains, compares simulation results with experimental SHARP images, and finally explores whether any 3D effects can be leveraged to further optimize the design. As a reference the gain in throughput is calibrated against a simple algebraic model based on ideal thin-mask intensity

for conventional and phase-shifting line space and contact patterns. Systematic simulations with HyperLith are used to characterize the impact of shadowing and etching quality. Data from through focus images of these patterns is used to examine the undesired zero order and image asymmetry through focus as indicators of second order mask performance effects. Layouts are designed for these patterns that compensate for shadowing and EM edge effects.

References:

[1]: Patrick Naulleau, et al., "Ultrahigh efficiency EUV contact-hole printing with chromeless phase shift mask," Proc. SPIE 9984, 99840P (2016)

10143-56, Session PS1

First light at EBL2

Norbert B. Koster, Edwin te Sligte, Freek T. Molkenboer, Alex F. Deutz, Peter van der Walle, Pim M. Muilwijk, Wouter F. W. Mulckhuyse, Bastiaan W. Oostdijck, Christiaan L. Hollemans, Bjorn A. H. Nijland, Peter J. Kerkhof, Michel van Putten, Jeroen Westerhout, TNO (Netherlands)

TNO is building EBL2 as a publicly accessible test facility for EUV lithography related development of photomasks, pellicles, optics, and other components requiring EUV exposure. Recently we finished installation of the source, exposure chamber, handlers and XPS system. We will report on our first results on EUV spot quality and spectrum, and general performance of the system. This includes particle and molecular cleanliness of the handlers and exposure chamber. EBL2 consists of a Beam Line, an XPS system, and sample handling infrastructure. EBL2 accepts a wide range of sample sizes, including EUV masks with or without pellicles. All types of samples will be loaded using a standard dual pod interface. EUV masks returned from EBL2 will retain their NXE compatibility to facilitate wafer printing on scanners after exposure in EBL2. The Beam Line provides high intensity EUV irradiation from a Sn-fueled EUV source from Ushio. EUV intensity, spectrum, and repetition rate are all adjustable. The XPS system has been operational since September 2016 and is able to handle full reticles.

10143-57, Session PS1

RESCAN: An actinic lensless microscope for defect inspection of EUV reticles

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Actinic mask defect inspection is an essential tool for the implementation of EUV Lithography in high volume manufacturing. The main challenges for any mask defect inspection platform are resolution and throughput. The reflective-mode EUV mask scanning lensless imaging microscope (RESCAN) has been developed to provide actinic mask inspection capabilities for defects and patterns with high resolution and high throughput, for node 7 and beyond. The lensless imaging concept allows to overcome the resolution limitations due to the numerical aperture and lens aberrations of conventional actinic mask imaging systems. With the availability of computational power and the refinement of reconstruction algorithms, lensless imaging become a powerful tool to synthesize the complex amplitude of the aerial image field providing us also with extremely valuable information about defects' phase and mask 3D effects. RESCAN is based on Scanning Scattering Contrast Microscopy (SSCM)1, a concept that allows a fast inspection of EUV reticles with arbitrary patterns and makes it possible to detect and classify different types of defects (see figure 1). In SSCM, we compare the measured scattering signal with a reference diffraction pattern, and we infer the presence of defects and some of their characteristics. It is also possible to perform an additional computational step to improve the resolution of the defect map: Using scanning coherent diffraction imaging (SCDI)2, we can reconstruct the complex amplitude of a high-NA, aberration-free aerial image of the defect (see figure 2). We recently upgraded the RESCAN microscope with an ultra-fast modular detector with 1024x512 pixel and a maximum frame rate of 2 kHz. This is a substantial step towards the development of a scanning microscope capable of inspecting a full EUV reticle within a reasonable time. We successfully tested the new detector on several mask samples and we are performing additional scans of programmed defect patterns on reticles with the standard 70-nm Tantalum-based absorber stack. We will present the latest results obtained with the RESCAN tool and illustrate the next upgrades we plan for the improvement of throughput and of defect sensitivity, including the use of an ultra-fast 2kx2k detector array and the introduction of full mask scanning capability.

10143-58, Session PS1

Arc-shaped slit effect of EUV lithography with anamorphic high-NA system in terms of critical dimension variation

In-Seon Kim, Guk-Jin Kim, Hanyang Univ. (Korea, Republic of); Michael Yeung, Fastlitho Inc. (United States); Eytan Barouch, Boston Univ. (United States); Hye-Keun Oh, Hanyang Univ. (Korea, Republic of)

EUV lithography is one of promising technology for 1X nm patterning. EUV lithography has high resolution capability with short wavelength but it has some particular patterning problems which is not appeared at optical lithography. Owing to reflective optics, EUV light incident obliquely at mask and oblique incidence of EUV lithography leads shadow effect and arc-shaped exposure slit. The study of these particular optical problems is required for optical proximity correction (OPC). Arc-shaped exposure slit leads azimuthal angle variation and it involves incident angle variation as a position at exposure slit. Due to incident angle variation at exposure slit, wafer critical dimension (CD) size has non-uniform distribution and the CD variation between slit edge and slit center is different with pattern direction. With understanding of these particular optical problems, lots of EUV OPC studies have been presented with 0.33 conventional NA system. However, suggested high NA system has not only has elliptical shaped mask NA and it has different angle distribution. The incident angle variation as a function of azimuthal angle is different between isomorphic and anamorphic NA system. In case of anamorphic NA system, incident angle distribution is smaller at horizontal direction but it is larger at vertical direction compared with case of isomorphic NA system. These difference makes different arc-shaped slit effect. CD variation as a function of azimuthal angle is different between isomorphic and anamorphic NA system. The study of CD variation in exposure slit is very helpful for optical proximity correction in EUV lithography. In this paper, we will deal with CD variation in exposure slit with anamorphic high NA system

10143-59, Session PS1

A two-step method for fast and reliable EUV mask metrology

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One of the major obstacles in the path to successfully implement extreme ultraviolet (EUV) lithography for future technology nodes remains the realization of a fast and reliable actinic method for the detection of mask defects. In order to meet the stringent requirements for high-volume manufacturing in terms of throughput, a potential mask inspection tool requires a continuously moving sample stage. However, due to the finite exposure time of the imaging sensor, defect identification and imaging using a continuously moving stage are affected by image anisotropies and blurring which have to be handled during data processing. We have devised a two-step process consisting of a primary inspection of the full mask using Scattering Scanning Contrast Microscopy (SSCM) with a subsequent detailed, but slower analysis of those areas where defects were found by Scanning Coherent Diffractive Imaging (SCDI). In the first step, the defect map is generated by comparing the SSCM results to calculated diffraction patterns of a perfect mask. Since SSCM operates purely in the

Fourier domain without the need to reconstruct the aerial image, defects are found in a fast and reliable way, albeit with a location accuracy limited by the spot size of the incident illumination convolved by the continuous stage movement. To reach the final resolution, the aerial image of the area with identified defects is reconstructed via SCDI, where the effects of the continuously moving stage are removed with a suitable algorithm. The effects of continuous sample movement are integrated into the algorithms in both methods. Using our reflective mode EUV mask scanning lensless imaging tool (RESCAN) installed at the new dedicated metrology branch of the XIL-II beamline of the Swiss Light Source, we have been able to reliably detect and classify defects with sizes below 10 nm (on wafer) using EUV multi-layer mask samples with a 70 nm Tantalum absorber featuring periodic as well as non-periodic structures. Here we present our extended SSCM and SCDI algorithms optimized for the defect inspection on a continuously moving sample. Our approach also significantly reduces various experimental errors such as instabilities of the incident illumination, or sample vibration. We believe that our two-step inspection process based on lensless imaging offers a comprehensive solution for actinic mask metrology.

10143-60, Session PS1

Speckle-based aberration recovery in the SHARP EUV mask microscope

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Surface roughness on EUV masks causes speckle when imaged by an extreme ultraviolet (EUV) microscope under sufficient spatial coherence. With the help of a phase-to-intensity transfer function theory [1], direct estimation of aberrations from the spatial spectrum of the speckle intensity is demonstrated using illumination angle diversity on the SHARP actinic inspection tool [2]. The aberration estimation is independent of phase introduced by mask topography, enabling simultaneous estimation of imaging system aberration and mask topography from the actinic inspection tool.

Extreme ultraviolet (EUV) lithography is under aggressive development for semiconductor manufacturing, because it enables smaller features and thus continued scaling. In the EUV regime, the short wavelength (13.5nm) means that even very smooth objects create speckle in the aerial image due to surface roughness at the scale of the wavelength. For reflective surfaces that can be classified as weak phase objects (e.g. EUV lithography masks) a phase-to-intensity transfer function can be defined, which is observed directly in the speckle power spectrum density. This is called the Contrast Transfer Function (CTF) [3], which depends on the system aberrations and the illumination angle. Hence using at least one normal and two oblique illumination angles, the two dimensional aberration function in the imaging system pupil can be recovered from the specular image of a blank mask. Further, by dividing the field of view into smaller regions, the field of view dependent aberrations, such as field curvature and coma can also be extracted. An optimization based framework is presented, that quantifies the first few Zernike coefficients in the system's aberration function. These are subsequently incorporated into the forward model of the system when imaging patterned masks, potentially enabling estimation of mask topography induced phase effects independent of imaging system aberrations.

[1] Gautam Gunjala, Aamod Shanker et. al. "Optical transfer function characterization using a weak diffuser, Proc". SPIE 9713, doi: 10.1117/12.2213271.

[2] Kenneth A. Goldberg et al,"New ways of looking at masks with the SHARP EUV microscope," SPIE 9422 94221A, (2015). DOI 10.1117/12.2175553

[3] J. P. Guigay, "Fourier transform analysis of Fresnel diffraction patterns and in-line holograms," Optik 49, pp. 121–125, 1977

10143-61, Session PS2

Monte Carlo sensitivity analysis of EUV mask reflectivity and its impact on OPC accuracy

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Unlike optical masks which are transmissive optical elements, use of 13.5nm radiation requires a reflective photomask structure --- a multilayer coating consisting of alternating layers of high-Z (wave impedance) and low-Z materials that provide enhanced reflectivity over a narrow wavelength band peaked at the Bragg wavelength. Absorber side wall angle, corner rounding, surface roughness, and various defects affect mask performance, but even seemingly simple parameters like bulk reflectivity on mirror and absorber surfaces can have a profound influence on imaging. For instance, using inaccurate reflectivity values at small and large incident angles would diminish the benefits of source mask co-optimization (SMO) and result in larger than expected pattern shifts.

The goal of our work is to calculate the variation in mask reflectivity due to various sources of inaccuracies using Monte Carlo simulations. Such calculation is necessary as small changes in the thickness and optical properties of the high-Z and low-Z materials can cause substantial variations in reflectivity. This is further complicated by undesirable intermixing between the two materials used to create the reflector. The relation between the standard deviation of mask bulk reflectivity and the standard deviation of most mask parameters are found to be roughly linear, with the slope dependent on the angle of incidence and the polarization. One of the key contributors to mask reflectivity change is identified to be the intermixing layer thickness. We also investigate the impacts on OPC when the wrong mask information is provided, and evaluate the deterioration of overlapping process window. For a hypothetical N7 via layer, the lack of accurate mask information costs 25% of the depth of focus at 5% exposure latitude. Our work would allow the determination of major contributors to mask reflectivity variation, drive experimental efforts of measuring such contributors, provide strategies to optimize mask reflectivity, and quantize the OPC errors due to imperfect mask modeling.

10143-62, Session PS2

A study on EUV reticle surface molecular contamination under different storage conditions in a HVM foundry fab

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The prospect of EUVL (Extreme Ultraviolet Lithography) insertion into HVM (High Volume Manufacturing) has never been this promising. As technology is prepared for "lab to fab" transition, it becomes important to comprehend challenges associated with integrating EUVL infrastructure within existing high volume chip fabrication processes in a foundry fab. The existing 193nm optical lithography process flow for reticle handling and storage in a fab atmosphere is well established and in-fab reticle contamination concerns are mitigated with the reticle pellicle. However EUVL reticle pellicle is still under development and if available, may only provide protection against particles but not molecular contamination. HVM fab atmosphere is known to be contaminated with trace amounts of

AMC's (Atmospheric Molecular Contamination). If such contaminants are organic in nature and get absorbed on the reticle surface, EUV photon cause photo-dissociation resulting into carbon generation which is known to reduce multilayer reflectivity and also degrades exposure uniformity. Chemical diffusion & aggregation of other ions is also reported under the e-beam exposure of an EUV reticle which is known to cause haze issues in optical lithography. Therefore it becomes paramount to mitigate absorbed molecular contaminant concerns on EUVL reticle surface. In this paper, we have studied types of molecular contaminants that are absorbed on an EUVL reticle surface under HVM fab storage & handling conditions. Effect of storage time as well as storage conditions (gas purged vs atmospheric) in different storage pods (Dual pods, RSP, and Reticle Clamshells) is evaluated. Absorption analysis was done both on ruthenium capping layer as well as TaBN absorber. The efficacy of different reticle cleaning processes to remove absorbed contaminant was also evaluated. This paper will detail and discuss results and trends observed from this EUVL reticle contamination study.

10143-63, Session PS2

Optical proximity correction variation considered minimum effect of aberration in extreme-ultraviolet lithography

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In terms of cost and simplification, the extreme ultraviolet (EUV) lithography is essential technology for sub-1X nm pattern. However, various problems which is not identified physically well make difficult to comprehend and predict full chip patterning.

Aberration is one of the issues that is considered as the area of irregular pattern distortion. As technology is developed, allowable precision of lens for imaging distortion is tightened since the wavelength for EUV lithography is an order of magnification smaller than optical lithography. Recently, lens aberration budget was reported as root mean square (RMS) 24 mλ wavefront error (WE) and comes under non-correctable error (NCE) about 26 mλ. Thus, total WE can be ranged from 24 to 50 mλ in situ.

Optical proximity correction (OPC) has been widely used to make a high resolution pattern for various pattern type. OPC was tried to the mask to evaluate whether the pattern distortion from nonideal WE can be compensated or not.

We will show various pattern distortion under various aberrations for various pattern types such as pattern shape, target CD and duty ratio and also provide allowable range of Zernike term for each case. Furthemore, because each aberration affect specific pattern type, pattern distortion and OPCed mask pattern are also different. In this paper, we will discuss the feasibility of EUV lithography under aberration specification of current EUV platform and aberration effect for sub 1X nm variable pattern and the possibilities that aberration can be compensated through proper OPCed mask.

10143-64, Session PS2

The impact of non-uniform wrinkle of multi-stack pellicle in EUV lithography

Guk-Jin Kim, In-Seon Kim, Hanyang Univ. (Korea, Republic of); Michael Yeung, Fastlitho Inc. (United States); Hye-Keun Oh, Hanyang Univ. (Korea, Republic of)

The extreme ultraviolet (EUV) pellicle is required to protect the EUV mask from defects, contaminations and particles during exposure process. The EUV pellicle which has a polysilicon membrane (54 nm thickness) was suggested for high transmission of EUV wavelength. However, the EUV pellicle can be easily deformed during an exposure process, so that the multi-stack pellicle is suggested to minimize the deformation of EUV pellicle. The multi-stack pellicle is a made of polysilicon-based core layer and it is covered with capping layers for the durability of deformation during the exposure process. The EUV pellicles should have over 90 % EUV transmission (after 1 pass) for mass production regardless of pellicle structure. Nevertheless, the EUV pellicle still has the deformation caused by manufacturing, thermal, and mechanical problems even though the multi-stack pellicle is used.

In this study, we investigated the impact of non-uniform wrinkle of EUV pellicle in terms of transmission non-uniformity and critical dimension (CD) variation. Figure 1 shows the transmission non-uniformity for the uniform and non-uniform wrinkle of EUV pellicle. In case of the uniform wrinkle, the transmission non-uniformity (after 2 pass) is periodic as a function of pellicle position, whereas that of the non-uniform wrinkled pellicle depends on the pellicle position due to different local tilt angle as a function of position. This transmission non-uniformity caused by the local tilt angle leads to the CD variation on the wafer. The transmission non-uniformity of non-uniform wrinkled pellicle (Case 1) is smaller than that of uniform wrinkled pellicle for 16 nm half pitch. Figure 2 indicates the transmission non-uniformity of non-uniform wrinkled pellicle (Case 1) when the amplitude of wrinkle is increased from 5 to 30 μm. The non-uniform wrinkled pellicle (Case 1) meets the CD variation of EUV pellicle specification suggested by ASML if the transmission (after 1 pass) of EUV pellicle has changed. However, the transmission non-uniformity of non-uniform wrinkled pellicle (Case 2) is much larger than that of uniform wrinkled pellicle when fixed period and increased amplitude as shown in Fig. 3. Therefore, we need to know the transmission non-uniformity and the CD variation on the wafer caused by deformed EUV pellicle during the exposure process.

10143-89, Session PS2

Image-based pupil plane characterization for anamorphic lithography systems

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In past lithography generations the image resolution has been improved by simultaneously increasing the lens' numerical aperture (NA) and balancing aberrations. Pupil plane characterization has been critical to optimizing high-NA systems, because aberrations are more severe with larger apertures. Increasing NA becomes more difficult in next-generation EUV lithography (EUVL) systems, where the non-zero chief ray angle causes incoming and diffracted energy to overlap if the aperture is too large. The proposed solution to high-NA EUVL is to physically increase the NA in one dimension, and increase the magnification in the other. The well-known Zernike circle polynomials however do not describe the fourteen primary aberrations of these anamorphic optical systems, shown in Figure 1. In this talk, we will examine the properties of the primary anamorphic aberrations and how they impact lithographic processes through analogies to isomorphic aberrations. There is an additional importance in EUVL placed on understanding how pupil variation evolves during system operation. Interferometric methods are the de facto standard of pupil phase metrology but are challenging to implement during tool use. We have previously presented an approach to measure both the pupil amplitude and phase variation of isomorphic EUVL systems from images formed by that system. We will show how this methodology can be adapted to anamorphic optical systems. More specifically, we will present a set of binary metrology targets sensitive to the anamorphic primary aberrations. Pupil variation will be extracted from images using a previously developed statistical approach based on principal component analysis.

10143-65, Session PS3

Recent development status of rinse material for EUV lithography

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Extreme Ultraviolet lithography (EUVL), Directed Self-Assembly (DSA), Electron beam (E-beam) lithography and multi patterning technology of ArF immersion lithography are being investigated for sub-10nm devices and beyond. Especially EUVL is one of the most candidate for high volume manufacturing (HVM) of sub-10nm devices. However, EUVL technology has some challenges for HVM. Resolution, Line width roughness and Sensitivity (RLS) trade-off is concerns for EUVL. Pattern collapse is mentioned as one of root cause of restriction of resist resolution. To improve the resist resolution, rinse material is known to be effective for prevention of pattern collapse and pattern bridging. However, the further improvement of resolution is required. In this study, we investigated the surfactant design and the formulation to improve the resist resolution. LWR and sensitivity with rinse material were also observed.

In addition, defect performance is also one of concern for EUVL. The defect reduction with rinse material was also studied.

As the result, new rinse material with low surface tension and low affinity surfactant for resist was able to achieve better resist resolution, wider process window and higher resist sensitivity than DIW. And also the rinse material exhibited defect reduction. We will discuss lithography performance and defect performance of rinse material.

10143-66, Session PS3

Contribution of EUV photomask CDU on lithographic patterning variability

Zhengqing John Qi, Jed H. Rankin, Lei Sun, Harry J. Levinson, GLOBALFOUNDRIES Inc. (United States)

As extreme ultraviolet lithography (EUVL) pushes the limits of patterning, the associated shrink of mask critical dimensions (CDs) naturally invites greater process variability during mask fabrication. To meet increasing tolerances on optical proximity correction (OPC) model error and wafer CD uniformity (CDU), a detailed understanding of EUV mask contributions on lithographic patterning variability is essential. By isolating various wafer CDU sources (e.g., OPC model error, through-slit 3D mask effects, scanner intrafield variability, and resist stochastic), the intrinsic mask CDU component contributing to patterning variability can be quantified. An evaluation on 2D features, which inherently possess greater process variability than 1D patterns, was preformed through-pitch and CD. The mask-wafer CDU transfer properties through design space is experimentally correlated and quantified to reveal the intrinsic mask contributions on wafer CD fidelity. Strong correlation between mask and wafer CDU was observed across feature type, revealing the intrinsic wafer CDU budgetary consumption attributed to mask CDU. The work here provides a systematic approach for quantifying the mask-wafer variability transfer signature. Key findings provide fundamental guidance on mask CDU budgeting and counsels on potential mask-limiting designs constructs in future technology architectures.

10143-67, Session PS3

EUV process improvement with novel litho track hardware

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Currently, there are many developments in the field of EUV lithography that are helping to move it towards increased HVM feasibility. Targeted improvements in hardware design for advanced lithography are of interest to our group specifically for metrics such as CD uniformity, LWR, and defect density. Of course, our work is focused on EUV process steps that are specifically affected by litho track performance, and consequently, can be improved by litho track design improvement and optimization. In this work we are building on our experience to provide continual improvement for LWR, CDU, and Defects as applied to a standard EUV process by employing novel hardware solutions on our SOKUDO DUO coat develop track system. Although it is preferable to achieve such improvements post-etch process we feel, as many do, that improvements post-patterning are a precursor to improvements after etching. We hereby present our work utilizing the SOKUDO DUO coat develop track system with an ASML NXE:3300 in the IMEC (Leuven, Belgium) cleanroom environment to improve aggressive dense L/S patterns.

10143-68, Session PS3

Impact of EUV SRAF on Bossung tilt

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Mask 3D (M3D) effects remain a significant challenge affecting EUV lithography (EUVL) imaging performance due to the comparable sizes of the mask and the wavelength of the EUV light. To reduce M3D effect, reduced absorber height [1] or a novel multi-layer mirror design [2] have been proposed to reduce the double diffraction between the multilayer mirror and absorber pattern. However, study shows that the different strategies have to be applied to different pattern designs. There is no general solution can be applied to the entire mask design. For sub-resolution assist features (SRAF), we can have custom design for different pattern features to reduce M3D effect locally and improve the process window [3]. Thus we will discuss the possible positive impact of SRAFs on Bossung tilt in this paper, and provide physical insight into the optical mechanisms at play enabling M3D effect mitigation by asymmetric SRAF distribution for EUVL.

In this particular 3D modeling study, we consider an example isolated 2-bar (CD = 16 nm) pattern imaged under delta function dipole illumination as shown in Figure (1). We analyze its scattered order distribution and fit it with the Zernike polynomials to represent the phase distribution in the pupil plane by aberration. The results show that SRAFs (CD = 8 nm) actually introduce stronger effective single pole aberrations in the imaging process as shown in Figure (2). However, the opposite impacts on Bossung tilt from each pole results in an overall improvement for dipole illumination. We also discuss the impact of SRAF position to Bossung tilt and show that the M3D effects lead to the optimal configuration being asymmetric in terms of SRAF offset from the line. Reduced Bossung tilt and a 21% improvement on the overlap process window are achieved by the insertion of asymmetric SRAFs into the 2-bar mask design as shown in Figure (3).

Moreover, we found that the SRAF position on each side will have the different impact on the main feature. As shown in Figure (4), we vary the SRAF position from its ideal asymmetric design and it shows that a slight adjustment on the bottom SRAF can have a huge impact on both features Bossung tilt while the top SRAF can only affect the feature closer to it.

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10143-90, Session PS3

2D self-aligned via patterning strategy with EUV single-exposure in 3nm technology

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Extremely advanced technology node requires higher resolution as well as robustness to process variations (e.g. dose, defocus, mask error, and

overlay). EUV lithography (EUVL) with wavelength of 13.5nm is being addressed in industries for sub-10nm technology node, and 2D self-aligned via (SAV) which is safely formed thanks to self-alignment in both vertical and horizontal directions has been introduced.Material A and hard mask run alternately on Mx and Mx+1 layers. Re-targeted pattern is slightly larger than via design in both directions, so that the via design is always exposed even with variations in lithography and etch processes. Material A and dielectric are eliminated while hard mask is not so that final via hole can be obtained after etch.

Conventional re-targeting, however, does not appropriately consider two vias that are close enough. For instance, if 3nm technology with 24nm metal pitch is assumed, two diagonally located vias could be located closer than minimum center to center distance of EUV hole patterning. Re-targeted patterns end up with a kissing corner, which yields either two single holes or a merged peanut-shape via hole. We cannot avoid EUV double patterning to separate the two vias, otherwise die to die difference is detected as a defect.

We propose a bridged via (BV) to resolve this situation. We insert a bridge pattern (BP) at every kissing corner, so that we can expect only a peanut-shape contour; note that critical margin should be maximized to avoid electrical short. Various shapes and sizes of BP are investigated with a few popular via designs which have kissing corners in actual layout. While a few nm difference of BP shapes is meaningless for EUV source, OPC engine sets evaluation points differently and provides distinguishable solutions, which is meaningful. We demonstrate BV with two high-end OPC techniques: source mask optimization (SMO) and inverse lithography technology (ILT) including EUVL-induced process variations (e.g. flare, resist randomness, and mask 3D effect). We optimize OPC recipe (e.g. fragmentation, mask rule check, and SRAF rules) to forecast 3nm technology requirements.

Pattern matching-based fast ILT flow is proposed to apply BV in full chip level. According to our experiments, ILT is promising for BV in 3nm technology, but runtime is an issue. We first extract some unique via designs to be merged by BP, and build a deck which includes pairs of an extracted via and an ILT result. For a full chip layout, we search for matched patterns in a deck and paste corresponding ILTed patterns. We then run lithography simulation with optimized source to find out some lithography hot spots. The hot spots may be modified by ILT in local region while obtained source is fixed. Proposed method is evaluated with lithography manufacturability check (LMC).

10143-69, Session PS4

A study on enhancing EUV resist sensitivity

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Studies are currently being carried out on developing a method for improving EUV resist sensitivity by enhancing EUV light absorption. The approach applied involves adding metals having high EUV light absorption to the resist polymer to increase secondary electron emission, enhance PAG reactivity, and improve acid generation efficiency [1]. One of our past studies confirmed that adding HfO2 nanoparticles improves EUV resist sensitivity [2].

Our current study investigates a new metal, which exhibits higher EUV light absorption than Hf, to determine whether further improvements in sensitivity can be achieved.

In this time we added ZrO2 to an acrylic-based resist in molar quantities of 0-2 relative to PAG. The resist was then subjected to EUV exposure at the NewSUBARU synchrotron radiation facility for sensitivity measurements and transmittance evaluations. The results show that adding ZrO2 resin further increases sensitivity too.

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10143-70, Session PS4

Impact of acid statistics on EUV local critical dimension uniformity

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Extreme ultraviolet (EUV) lithography provides a solution for industry to continue the shrink at a reasonable cost. However, as the EUV photon density significantly decreases, the resulting noise in the resist makes it challenging to maintaining pattern fidelity. Besides the photon statistic effects, acid diffusion is another major contribution to patterning variations. Local CD uniformity (LCDU) of dense contact holes is a more stable target to monitor the effects of pattern variations than line width roughness of dense lines since contacts holes have substantially wider process window(s) and do not suffer from pattern collapse issues.

In this work, we study the effects of acid deprotection, acid diffusion and acid-base interaction on LCDU by varying the PAG acidity, size, loading, and quencher loading of chemically amplified resist. We found that PAG acidity, PAG anion size and quencher loading have significant influence on controlling LCDU while PAG loading has very limited effects. These EUV experiment results are used to validate the LCDU analytical model which predicts the relationship between shot noise and photon and acid statistics. The learnings of acid impacts on pattern variability will help to better understand the shot noise model and explore the limits of EUV lithography aroused from both photon and chemicals statistics. Furthermore, non-chemically amplified resists which exclude the acid statistics are also evaluated, in order to compare the relative impacts acid statistics.

10143-71, Session PS4

Influence of post exposure bake time on EUV photoresist line-width roughness

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Current EUV photoresists are unable to meet simultaneously the resolution, sensitivity and roughness requirements for advanced technology nodes. For traditional chemically amplified resist (CAR), acid diffusion is intrinsic to the CAR mechanism as it is needed to propagate the deprotection reaction. Reduced acid diffusion length (ADL) is a target for resist manufacturers, because it improves the ultimate resolution that can be achieved.

The ADL is modulated by the type of photoacid generator (PAG), by the amount of quencher in the resist formulation and by the process parameters of the post exposure bake (PEB).

For this study, we investigate the effect of PEB time on the acid diffusion of positive and negative tone development (PTD and NTD, respectively) resists. The resists were coated on 300mm Si wafers, exposed to EUV light by ASML NXE:3300B full field EUV scanner, and subsequently baked at different PEB times from 15s to 240s before development. Using scanning electron microscope (SEM) we follow the evolution of critical dimension (CD) and line width roughness (LWR) for 20nm dense line space patterns as a function of the PEB time for each resist.

By plotting CD and LWR versus PEB time, two different regimes are observed: for short PEB times, the CD and LWR both decrease rapidly, while the second regime is characterized by a slow decrease of CD and small variation of LWR. The first regime indicates that high diffusion and deprotection reaction occurs in the exposed part of the resist, while in the

latter regime the deprotection reaction happens only at the interface of the exposed/unexposed pattern. In this steady state regime, diffusion of the acid is controlled by the remaining quencher in the unexposed region of the resist.

The impact of higher quencher loading, as tested, is an effective way to control lateral acid diffusion. Resists with a low amount of quencher demonstrate a worsening of LWR during the second regime, while high quencher loading help the resist to maintain a stable LWR through PEB time. This stability permits us to use lower dose and longer PEB time to reach the same pattern target. For high quencher loading resist, a PEB of 240s permits a 20% of dose-to-size reduction, while keeping the resolution and LWR constant. This result holds for both PTD and NTD resists tested and opens an interesting pathway for PEB-induced dose reduction.

Additionally, two resists with a different protecting group are tested in order to assess the impact of the deprotection reaction rate on the acid diffusion.

Lastly, we evaluate the effect of PEB time for a non-CAR metal-oxide resist as it is not supposed to be dependent on acid diffusion. This resist also shows a dose reduction of 33% between 60s and 240s PEB, however it has a negative impact on roughness, with 30% LWR increase.

10143-72, Session PS4

Tin-oxo cages for use as photoresists in EUV lithography

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The field of photoresists nowadays faces serious challenges, due to the smaller sizes of the desired features and the transition from Deep UV (193 nm) to Extreme UV lithography (13.5 nm). A promising approach is the use of organometallic resists. The metal atoms that they contain strongly absorb EUV light. For instance, tin (Sn) has an EUV absorption cross section that is about 30 times larger than that of carbon (C).

This work focuses on the synthesis, characterization and photoresist performance of the cage compounds [(BuSn)12O14(OH)6]X2, in which X is a monovalent anion that can be varied. The typical size of the compound (~1.5 nm) makes the cages suitable for patterning at the nanoscale. The compounds are soluble in organic solvents, but turn insoluble upon DUV, e-beam or EUV radiation. In this work we have expanded upon previously published work by a thorough comparison of the three irradiation methods.

Firstly, the structure of the prepared compounds was unequivocally confirmed using 1H NMR, 119Sn NMR, IR/Raman spectroscopy and mass spectroscopy. Chemical changes were observed on material that was exposed to DUV radiation, using IR and Raman spectroscopy. These exposures were carried out in the solid state as well as in solution. The exposures in solution were monitored by UV-Vis spectroscopy, using the strong absorption band of the compound at 220 nm. This absorption decreased upon UV exposure, and this allows us to estimate the quantum yield (QY) of photobleaching. It was found that this quantum yield depends on the concentration, indicating that the photochemical reaction occurs between at least two different molecules. It is very likely that a similar mechanism takes place in the solid state; UV-Vis absorption experiments were also conducted on spin coated layers of the material.

Spin coated layers were also studied using IR and Raman spectroscopy. An interesting region in the IR and Raman spectrum is the C-H stretch region (2900 - 3000 cm-1). A decrease in these bands was observed upon irradiation with DUV light, indicating that organic groups are lost during the exposures.

With AFM, contrast curves were generated. It was found that an EUV dose of only 20 mJ/cm2 is sufficient to induce the changes in solubility. However, for patterning at the nano-scale a higher dose is required, judging from the obtained patterns. Additionally, the sensitivity to e-beam irradiation compared to conventional polymer resists was found to be quite low, meaning that a high dose is required. Apparently, photons are strongly absorbed by the material but capturing the subsequent electron cascade still has low efficiency. If this is improved, the sensitivity of the compound could improve even more. Additionally, it was shown that post-exposure baking, which is often utilized for CARs, is an important process for organometallic resists as well. Apparently, this baking induces additional cross-linking in the material, improving the sensitivity and line-edge roughness.

10143-73, Session PS4

Technology for defectivity and CD uniformity improvement in resist coating and developing process in EUV lithography process

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Extreme ultraviolet lithography (EUVL) technology is getting closer to high volume manufacturing phase every year. In July 2016, the light source power, range of dose in wafer, and so on in ASML NXE:3300 were upgraded at imec, and advance EUV patterning on ASML NXE:3300/ CLEAN TRACKTM LITHIUS ProTM Z- EUV litho cluster is launched, allowing for finer pitch patterns for L/S and CH.

In order to enhance the yield in EUV lithography process, defectivity improvement is required.

Latest technologies and TEL's best known method are demonstrated on 24nm contact hole pattern to achieve defect reduction.

CD uniformity control is also very important factor toward EUVL manufacturing phase. CD variations are composed of several components such as shot to shot CD uniformity, within shot CD uniformity and local CD uniformity. Improvement of each component is studied with process optimization and latest technologies.

This paper include not only result of chemically amplified resist(CAR), but also result of in-organic resist such as metal oxide resist.

10143-74, Session PS4

Measurement of outgassing species generated from EUV resist including metal oxide nanoparticles

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As advanced technology of increasing EUV sensitivity, EUV-resist which includes metal oxide nanoparticles has been developed and evaluated by many researchers. Sensitivity for EUV-light is improved by metal oxide nanoparticles, for example ZrO2 or TeO2, in EUV-resist. This kind of study is important for developing EUV lithography in the future. However, resist including metal oxide nanoparticles has risk of metal pollution and it is fatal for semiconductor fabrication. Therefor analytical methods of metal particles and outgas which are generated from EUV-resist including metal oxide nanoparticles is required.

In this study, we evaluated outgassing species generated from EUV resist including metal oxide nanoparticles during exposure. Especially metal particles which may be scattered from EUV resist during exposure were evaluated by using induced cupping plasma (ICP) analysis which has good sensitivity for metal species. And also we evaluated outgassing species generated from EUV resist by in-situ mass-spectrometry during exposure.

10143-75, Session PS4

xMT molecular EUV resist readiness for high-volume manufacturing (HVM): Introduction and update

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It has been reported that the xMT resist performs well under electron beam lithography at energies ranging between 30 – 100 keV. Initial testing has now demonstrated that the platform shows high sensitivity under 193 nm dry illumination – dose to gel is ~ 2 mJ/cm2. Features with a CD of 80 – 100 nm have been patterned in initial testing, holding out the possibility that xMT can provide a single resist solution to hybrid patterning approaches incorporating 193 nm, EUV and electron beam patterning.

Irresistible Materials (IM) continues to develop its chemically amplified molecular resist, which has demonstrated a strong combination of resolution, sensitivity and line edge roughness using EUV exposure. The IM team is now focusing on wider application and optimization of the xMT platform for production EUV tool use. In this paper we will focus on the results obtaining using the xMT platform specifically for EUV applications.

New EUV photoresist platforms have been required to show that they have suitable outgassing performance in order enable testing on NXE 3100/3300 systems. Outgassing studies utilizing xMT, undertaken on the IMEC outgassing tools, have shown that both cleanable (<2.5 nm) and non-cleanable outgassing are well within spec for the NXE 3300. Recent experimental performance will be shown that demonstrates overlapping process windows for lines and spaces (l/s) and for pillars (for example). We will also show contact hole performance using the xMT platform. As an example, 16.4 nm lines and 25.5 nm pillar have been simultaneously patterned using the Micro Exposure Tool (MET) located at the Lawrence Berkeley National Laboratory. F2X illumination, with a dose of 25.7 mJ/cm2 was used to obtain these results. Resolution has been pushed to MET tool limits – 13 nm and 14 nm hp features at doses of 54.4 and 32.1 mJ/cm2 respectively have been demonstrated. First round exposures using the IMEC NXE 3300 have yielded 19 nm half pitch features. Lines have been obtained down to 16 nm (patterned at a dose of 22 mJ/cm2). It is anticipated that this will improve considerably with further optimization of resist processing for the NXE.

10143-76, Session PS4

Simulation and experimentation of PSCAR (TM) chemistry for complex structures

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Extreme ultraviolet lithography (EUVL, λ = 13.5 nm) continues to be one of the most important candidates for future technology nodes. For the insertion of EUV lithography into device mass production, higher sensitivity of EUV resists is helpful for better cost of ownership of the EUV tool and light source. However, obtaining low sensitivity (S), high resolution (R), and low line edge roughness (L) simultaneously is very difficult. Many previous experiments by lithographers proved the existence of this "RLS trade-off"1-2.This paper furthers the work related to Photosensitized Chemically Amplified ResistTM (PSCAR) TM**, a chemistry which is trying to break the "RLS trade-off" relationship. This chemistry was introduced last year as a new chemically amplified lithographic concept and is accomplished in an in-line track tool with secondary exposure module connected to EUV exposure tool.

PSCAR is a modified CAR which contains a photosensitizer precursor (PP) in addition to other standard CAR components such as a protected polymer, a photo acid generator (PAG) and a quencher. In the PSCAR process, an improved chemical gradient can be realized by dual acid quenching steps with the help of increased quencher concentration. The addition of the PP, as well as other material optimization, offers more degrees of freedom for getting high sensitivity and low LER, but also makes the system more complicated. Thus coupling simulation and experimentation is the most rational approach to optimizing the overall process and for understanding complicated 2-D structures.

In this paper, we will provide additional background into the simulation of PSCAR chemistry, explore the effects of PSCAR chemistry on chemical contrast of complex structures (e.g. T structures, slot contacts, I/D bias for L/S), and explore the sensitivity enhancement levels capable while improving or maintaining lithographic performance. Finally, we will explore modifications of PSCAR chemistry on performance.

10143-77, Session PS4

Envisioning new extreme ultraviolet resists by seeing EUV-resist interactions down to the electron level

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It is well understood that new resists are needed to advance EUV lithography. Nevertheless, a grand challenge to improving EUV resists is "seeing" the photon-induced reactions. The EUV cross-sections and binding energies for atoms are well known. This allows the prediction of photoemission cross-sections and photoemitted energies. However, this is only one important step in the process. Auger emission, molecular fragmentation patterns, and subsequent electron-resist interactions are also critical. Understanding all these steps is crucial to harness all the deposited energy for improved patterning results. We combine beam-line gas phase experiments of the EUV absorption with theoretical studies to gain fundamental understanding of the role of these processes in EUV radiation chemistry.

In this work, we present experimental and theoretical studies of resist analogs using tunable EUV radiation from the Advanced Light Source at Berkeley (ALS). Our equipment allows us to look at electron emission and photo induced fragmentation of resist components EUV irradiated in the gas phase. We study halogenated phenols with fluorine, chlorine, bromine, or iodine functionalization. We confirm that iodine is the highest cross-section absorption, but more importantly, we find that the photoemission is amplified beyond one electron. Results are summarized in Figure 1. With one iodine, the electron emission cross-section is increased relative to that calculated for photoemission alone (photoemission cross-section calculated using CXRO website). This is due to Auger emission. Hence Iodine produces electrons beyond the primary photoemission for multiple electron emission per absorption event. We will discuss these studies and accompanying theoretical work. In addition, we will describe our equipment capabilities which allow both EUV and electronic excitation of gas phase materials with detection of electron emission, low energy electron attachment, and molecular fragmentation. We find that low energy electron attachment is important to consider in resist systems. With this work, we can direct needed advancements in EUV resist design. This includes direction into which elements can "electronically" amplify the resist sensitivity.

10143-78, Session PS4

Optimization of stochastic EUV resist models parameters to mitigate line-edge roughness

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Line-edge roughness (LER) of the EUV-patterned features is one of the current challenges limiting EUV applications[1-3]. This edges roughness is caused by photon shot noise (PSN) in the EUV exposure and also by the stochastic effects of the complex physical and chemical processes occurring during EUV exposure, post exposure bake and development of photoresists. To mitigate the LER effects it is desirable to adjust the parameters of the EUV resist in an optimal way[2].

In this paper, we formulate the optimization problem of reducing LER of a certain feature subject to the constraints dictated by the need to fabricate this feature within certain dimensional specifications, applying at nominal EUV process conditions and several off-nominal conditions. We use a stochastic Monte-Carlo EUV resist model[2], where each run of the model produces a certain specific instance of edge roughness. To account for the infinite variety of possible edge roughness shapes, the optimization algorithm must handle properly the stochastic nature of both the cost function and the constraints, for instance by performing a sufficient number of trials and calculating statistical moments (mean and variance) of the involved quantities.

Several options for optimization algorithms, suitable for the solution of the formulated EUV LER optimization problem, are presented and discussed, along with the results of their tests.

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10143-79, Session PS4

Simulation of secondary electron trajectories in EUV resists

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Secondary electrons play a crucial role in triggering the chemistry which ultimately leads to the formation of solubility contrast in an EUV resist. Modeling the scattering mechanisms by which electrons deliver energy to the photoresist can provide useful insights into the best strategies that might help with optimizing lithographically important parameters, e.g. net secondary electron blur and the acid quantum efficiency. Of particular importance are the mechanisms by which electrons with very low energies (e.g., under 10 eV) scatter in the material. One of the widely studied mechanisms is the excitation of vibrational states. Khakoo et. al. [1] performed gas-phase measurements of vibrational excitation cross-sections for tetrahydrofuran (C4H8O) using electron energy loss spectroscopy with incident electron energies ranging between 2 and 20 eV. The EELS results demonstrate that all the vibrational modes in the material are at energies less than 1 eV, which likely indicates that a single vibrational excitation event will not directly lead to activation of PAGs. However, vibrational excitations can serve as elastic scattering events that can alter electron trajectories, possibly resulting in a chemically significant energy loss event elsewhere in the material. As demonstrated by the differential cross section data for tetrahydrofuran by Khakoo et. al. [1] and for furan (C4H4O) by Hargreaves et. al. [3], the scattering angle of the electron following a vibrational excitation event is a function of both the incident electron energy and the vibration mode being excited.

In this paper, we assess the impact of vibrational excitation mechanisms on the net secondary electron blur and spatial distribution of acid generation events by using a Monte Carlo model for simulation of electron trajectories. The vibrational excitation mean free path and scattering angle are calculated using the angle-dependent differential cross-section data from the literature for materials with chemical compositions similar to a typical chemically amplified resist. The inelastic scattering based energy delivery by electrons in the continuous slowing down approximation is modeled by using the Mermin dielectric function based model for mean free path and oscillator strengths that have been previously reported [2].

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10143-81, Session PS4

Fundamental aspects of new resist process breaking RLS trade-off and photon shot noise

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EUVL is expected to start soon based on the recent advancement of EUVL technology, especially EUV light intensity. However its intensity is not enough yet. The light source intensity and the resist sensitivity are complementary each other. It is expected to enhance EUV resist sensitivity for compensating the low EUV light intensity and also reducing the development/maintenance cost of EUV exposure systems. However, improving the EUV resist sensitivity was challenging owing to two important problems in EUV/EB CAR resists: the simultaneous improvement in resolution, line edge roughness (LER), and sensitivity (so-called RLS trade-off)1 and the dramatic change of pattern formation processes from photochemistry in KrF / ArF photoresists to radiation chemistry in EUV/EB resists, especially acid generation processes2. Based on the resist pattern formation model of EUV CARs including radiation chemistry3, the RLS trade-off has been improved steadily by worldwide efforts. However, the improvement of RLS trade-off based on the standard resist pattern formation model3 has become gradually slow recently. In this regards, it is problematic that the RLS trade-off of EUV resists has not been improved much in recent years. It becomes more difficult to improve the RLS trade-off of EUV resists. Therefore this approach becomes more difficult gradually because this approach is now reaching near physical limit of the model.

Therefore, novel processes and materials of overcoming RLS trade-off such as photosensitized chemically amplified resistTM (PSCARTM) proposed4 in 2013 and explained clearly about the RLS trade-off5 and post exposure delay effects of PSCAR in 20146 by EB exposure are necessary for HVM by EUVL. The preliminary but promising results for RLS trade-off were presented in SPIE Advanced Lithography 20167-9. Moreover future improvement plan of PSCAR was proposed based on the reaction mechanisms and experimental results by EB pattern exposure of PSCAR10 on the pattern degradation of PSCAR observed in previous papers7-9.

Stochastic problems including photon shot noise become more important with increasing as well as RLS trade-off. The present presentation makes clear the fundamental aspects of the new resist processes breaking RLS trade-off and also overcoming photon shot noise problem based on experimental data.

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10143-91, Session PS4

Computational approach on PEB process in EUV resist: multi-scale simulation

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For decades, downsizing has been a key issue for high performance and low cost of semiconductor, and Extreme Ultraviolet Lithography (EUVL) is one of the promising candidates to achieve the goal[1,2]. As a predominant process in EUVL technology on determining resolution and sensitivity, post exposure bake (PEB) has been mainly studied by experimental method, and development of its photoresist (PR) undergoes difficulty because of the lack of unveiled mechanism during the process. Herein, we provide theoretical approach to investigate underlying mechanism on the PEB process in chemical amplified resist (CAR), and it covers three important reactions during the process: acid generation of photo-acid generator (PAG), acid diffusion, and deprotection. First principle calculation (quantum mechanical simulation) was conducted to quantitatively predict activation energy and probability of the chemical reactions, and they were applied to molecular dynamics (MD) simulation for constructing reliable computational model. Then, overall chemical reactions were simulated in the MD unit cell, and final configuration of the PR was used to predict the line edge roughness (LER). The presented multiscale model unifies the phenomena of both quantum and atomic scales during the EUVL process, and it will be helpful to understand critical factors affecting the performance of the EUVL and design the next-generation PR material. References[1] Kozawa, T.; Tagawa, S., Jpn. J. Appl. Phys. 2010, 49 (3R), 030001. [2] Itani, T., Microelectron. Eng. 2009, 86, 207.

10143-82, Session PS5

Development of high-efficient laser amplifiers system toward 40-kW pulsed laser generation for EUV light source utilizing transverse-flow CO_2 laser

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In recent years, an extreme ultraviolet (EUV) lithography technology has become increasingly attracted for high-volume manufacturing. The power of EUV light sources required for exposure tool throughput remains as one of critical and technical challenges. Technologies for the higher-efficiency EUV light source are also demanded. A CO2-laser produced tin plasma (LPP) EUV light source is a promising candidate as the high power light source with the wavelength of 13.5 nm for the EUV lithography. Availability of the high-power pulsed CO2 laser is one of the important key factors for applying the LPP EUV light source to high-volume manufacturing. A 27-kW CO2 laser system is needed for the first generation of high volume manufacture EUV lithography and a 40-kW CO2 laser system is needed for the next one.

We have been developing transverse-flow CO2 laser amplifiers for the LPP EUV light source. In the transverse-flow laser, the direction of the gas flow is perpendicular to optical pass. The transverse-flow CO2 laser is a promising candidate for the EUV light source driver. In principle, transverse-flow CO2 lasers offer a higher gain and a shorter optical path in the amplification system compared with axial-flow CO2 lasers. In addition, a multi-fold optical path is possible in the case of transverse-flow lasers.

A master-oscillator power-amplifier (MOPA) CO2 laser system is constructed for amplification test. The master oscillator emits 4-line, P(18), P(20), P(22), P(24) laser pulses with the repetition frequency of 100 kHz. These lines are neighboring CO2 laser lines in the 10.6 μm band. The pulse duration of the oscillator is 15 ns. Four transverse-flow CO2 lasers are designed and constructed for the amplifiers. The first amplifier has a five-fold optical path and the others have a single path. The electrical input for the discharge of each amplifier is up to 100 kW. The amplification test is carried out at a 100% duty cycle of discharge.

As a result, the output average power of 27.1 kW is demonstrated with the small input power of 20 W using the four transverse-flow CO2 laser amplifiers in cascade. The electrical-to-optical efficiency is 6.8 % which is higher than that of reported data using axial flow amplifiers. In this experiment, the optical power of 23.8 kW is extracted from three single-path amplifiers exited by the electrical power of 300 kW.

The transverse-flow CO2 laser demonstrated highly-efficient high-power laser amplification at 100% duty cycle of discharge. Our calculation reveals that six transverse-flow CO2 laser amplifiers system can generate 40-kW optical power with high efficiency. A lower optical loss is needed for amplifiers in high power laser input. The single-path amplifiers has the minimum optical loss because the light passes through only two windows. We will report our simulation and the latest results in the presentation.

10143-83, Session PS5

Key components technology update of the 250W high-power LPP-EUV light source

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We have been developing CO2-Sn-LPP EUV light source which is the most promising solution as the 13.5nm high power light source for high volume manufacturing which enable sub-10nm critical layer patterning for semiconductor device fabrication. It has unique and original technologies such as; The high power short pulse CO2 laser, the short wavelength solid-state pre-pulse laser, the high stabilized doloplet generator, a laser-droplet shooting control system and the debris mitigation technology with the magnetic field.

In this paper, we show the key components technology update of our 250W CO2-Sn-LPP EUV light source. The high power short pulse CO2 drive laser system composed of higher gain amplifiers realizes a shorter laser pulse with higher output power. We developed multi-line short pulse CO2 laser oscillator and high gain traverse flow CO2 laser amplifier cooperated with Mitsubishi Electric Corporation. More than 20kW of CO2 laser output and 15 nanosecond pulse duration with 100 kHz are achieved. The short wavelength solid-state pre-pulse laser produce high conversion efficiency. The Pre-pulse laser is the solid-state laser with a pulse width of 10ps (FWHM) and a wavelength of 1.06um and its power is a more than 100W.The irradiation of pre-pulse with the duration of 10ps before CO2 laser irradiation makes the high CE of over 4%, and it achieves the high ionization rate of over 99%. The improved droplet generator can create smaller size and stable droplets suitable for longer operation time due to less tin debris generation. ~20 um diameter droplets and position stability of less than +/- 5 was achieved. The improved laser-droplet shooting control system is developed. The system has several shooting control loops for ensuring shooting accuracy of um and ns level between droplets and lasers, which are droplets position control, laser beam axis control and timing. The Magnetic Mitigation system maximize the lifetime of the collector mirror. Very strong magnetic field trap the tin ions and protect the corrector mirror from the degradation of tin debris from the plasma. The laser-droplet shooting control system controls several actuators, laser properties and droplet properties for accurate tin droplets shooting. Shooting error is cause of shorter operation time due to much amount of tin debris generation. The improved metrology system also contributes shooting accuracy and shooting error is decreased.

We are now constructing new high power HVM LPP-EUV source with >25kW CO2 driver laser amplifier system made by Mitsubishi Electric. At the conference we will report the performance of the new system and updated data of old systems.

10143-84, Session PS5

Numerical analysis of particle emission from laser irradiated tin targets for the optimization of the EUV source

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Optimization pre-plasma is critical to obtain high output power from the laser pumped plasma (LPP) extreme ultra-violet (EUV) light source. We investigate fragmentation of tin droplet targets by the pre-pulse laser irradiation. The target is broken up to small particles, which are distributed into the sphere with a radius of few 100 micrometers, resulting in the averaged density of the plasma to be 10-3 solid density, which is suitable for efficient EUV emission by the irradiation of the main CO2 laser pulse.

The laser produced plasma has been investigated using the hydrodynamics simulation assuming uniform distribution of density and temperature. Particle emission from the laser ablation is investigated using the molecular dynamics simulation, however, with which spatial and temporal scale of the model is limited. To investigate the performance of the EUV source, macroscopic methods using statistical approaches may be necessary.

We develop a hydrodynamics model with the equation of state (EOS) of tin, which describes liquid to gas transition, and algorithms for mesh reorganization, to investigate the generation of particles through the evaporation, condensation as well as by shock wave caused by the irradiation of short laser pulse. We use Van-der-waals equation of state to determine the ratio between liquid and gas phase for given temperature and density of the material, assuming thermodynamic equilibrium.

The simulation model is based on the Lagrangian hydrodynamics, in which the mesh is reorganized dynamically according to the distribution of the material, with which gas bubbles in the liquid phase and clusters in gas phase are represented, while the mesh collapse due to the hydrodynamic motion is avoided. We also include the process of liquid to gas transition. If the density and temperature of the cell satisfied the condition of phase transition, the cell is split into several cells to have a correct volume ratio between liquid and gas determined for the group of the cells using the Van-der-waals equation of state, maintaining the conservation of internal energy.

We verify the model through test calculations. Furthermore, we will discuss the physical effect and numerical method to include processes that determine dynamics of the particles, such as surface tension for bubbles and clusters as well as the interaction between the laser and particles.

10143-85, Session PS5

Study of ion-enhanced Sn removal by surface wave plasma for collector cleaning

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A hydrogen plasma cleaning technique to clean Sn off of EUV collector optics is studied in detail. The cleaning process uses hydrogen radicals (formed in the hydrogen plasma) to interact with Sn-coated surfaces, forming SnH4 and being pumped away. This technique has been used to clean a 300mm-diameter stainless steel dummy collector optic, and EUV reflectivity of multilayer mirror samples was restored after cleaning Sn from them, validating the potential of this technology.

This method has the potential to significantly reduce downtime and increase source availability. Thus, an investigation into the fundamental processes governing Sn removal has been performed. These have shown that the Sn etch rates scale with hydrogen ion energy. Incident ions upon the surface impart energy that weakens the Sn-Sn bond allowing the chemical etch by hydrogen to proceed at a faster rate. Due to this our plasma is able to be in a reactive ion etch (RIE) regime. Results showing etch enhancement due to ions in this particular chemistry, including threshold energy, are shown.

A concern for plasma based methods is the implantation of high energy hydrogen ions into the MLM, reducing reflectivity and possibly blistering. With a surface wave plasma (SWP) this concern is alleviated somewhat because of lower ion energies. Surface wave plasmas have lower electron temperatures than conventional sources in the range of 1 to 3 eV. In addition, SWP sources result in plasma densities on the order of 10^11 to 10^12 cm-3, allowing for greater utilization of ion etch enhancement. Experiments measuring plasma parameter profiles over large areas have been conducted and the results from these measurements are presented. These will help demonstrate scalability of SWP cleaning techniques for use in EUV sources.

10143-86, Session PS5

Background pressure effect on EUV source efficiency and produced debris characteristics

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The cost of future computer chips, among other things, will depend on the performance of EUV source and on the duration of the efficient operation of nanolithography devices. While the efficiency of the sources is continuously being improved, their operational cycle is still highly restricted due to optic mirrors degradation as well as necessity of cleaning chamber environment and components.

One of the problems of EUV sources for high volume manufacture regimes is related to the contamination of chamber environment by products of

preceding laser pulse/droplet interactions. Implementation of high, 100 kHz, repetition rate of devices for Sn droplets and laser pulses generation can cause fast accumulation of tin in the chamber in the form of vapor/plasma/clusters.

We simulated possible tin accumulation in the chamber in dependence on laser parameters and mitigation system efficiency. Then, we studied the effect of various pressures of tin vapor on the CO2 laser beam propagation and size, intensity, and efficiency of EUV source produced.

Modeling of source environment consisting from tin droplets and micro-fragments surrounded by vapor cloud with different pressures was performed using the comprehensive HEIGHTS package. The package includes advanced models for various interactions of laser photon with liquid/vapor/plasma, plumes hydrodynamics, and radiation and thermal processes. Predictions for stable source operation were performed based on the frequency of laser and droplets generation systems. Effect of chamber conditions on further fragments/vapor distribution was also analyzed. The maximum source operation frequency and efficiency could be affected and limited by the background environment inherited from source operation.

10143-87, Session PS5

Spatially resolved ion dynamics in two dimensions around a droplet-based laser produced plasma

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At the Applied Laser Plasma Science (ALPS) facility at the Laboratory for Energy Conversion (LEC) at ETH Zurich droplet-based laser produced plasma sources with the application in actinic blank and mask inspection are the main research focus. Laser produced plasma creation is inherently coupled to the formation of debris which can be divided into three main categories which are namely, ions, neutrals and droplet fragments compromising the lifetime of the light source by degrading the highly sensitive EUV optics. This reduced lifetime, therefore substantially influences the cost-of-ownership of the light source.

Key to optimize the debris mitigation strategy is the assessment and quantification of the detrimental plasma debris. A major challenge is associated to the high kinetic energy ions emanating from the laser produced plasma eroding the first bounce collection optics.

The spatial distribution of the ion emission generated from a laser irradiated droplet target is analyzed in detail in the intermediate pressure regime of 2e-2 mbar. The employed instrument is a multiple array of six motorized Langmuir probes. The ion emission is measured in the two dimensional space from 50° to 130° towards the laser axis with distances from the plasma ignition point from 15 mm up to 80 mm. The total ion flux and its attenuation over distance is discussed. Furthermore, the ion kinetic energy based on the time of flight signal is analyzed and the implication on the collection optics is assessed.

By providing fresh targets in the form of micro-meter sized droplets to the droplet irradiation position, a certain variability of the droplet position with respect to the laser focal area is inherent. By actively changing the droplet position with respect to the laser focal area with a control system the influence on ion and EUV propagation direction is studied in this work.

10143-88, Session PS5

Improvement of power, efficiency, and cost-of-ownership in the tin LPP EUV source

Malcolm W. McGeoch, PLEX LLC (United States)

An argon plasma in a magnetic cusp [1,2,3] thermalizes fast tin ions [1] and removes exhaust energy onto a large area beam dump. Demonstrations of plasma stability and particle control [1,2] have shown the magnetic field requirement to be modest and easily achievable with a very compact magnetic circuit. The plasma required for an EUV source power greater than 300W has a pressure of 640Pa and is contained in a cusp magnetic well with a containment B field of only 40mT. Superconducting magnets are not required and the conventional magnet power totals only 4kW. A cusp magnetic circuit of mild steel serves as part of the source chamber wall and has very small fringing fields.

In 2015 [2] we demonstrated stable containment of an argon plasma at the exhaust power, temperature and density required for this application. Without B field containment the same degree of tin ion control would require a large gas number density, necessitating the use of hydrogen for low EUV absorption, with its associated disadvantages of dissociation, tin hydride chemistry and re-cycling concerns. The hydrogen throughput to carry away excess plasma heat is very large and its flow is not directional like the flow of a magnetically-controlled plasma, making scaling of the hydrogen technology very difficult.

Substantially raised EUV source efficiency (40% improvement) is achievable by conforming the cusp magnetic well to the EUV collector optic, allowing a collection solid angle as high as 7 sterad to be achieved. This translates into a laser power as low as 30kW for 500W of EUV power. This is only made possible by the accurate plasma power guidance provided by the magnetic field.

In place of hydrogen, non-reactive argon gas is used, and its flow rate is relatively low. The pumps required for argon recycling are small and may be mounted close to the target chamber, avoiding large duct-work and a remote, high power, and high cost pumping station.

In the argon cusp tin LPP source, the exhaust power is guided precisely onto a ring-shaped beam dump that receives argon ions of energy too low to cause back-sputtering of tin. A typical beam dump heat loading for a 500W EUV source will be 100W cm-2 or less.

This combination of low-stress components, easy argon recycling and high source efficiency makes the further development of this technology very important for HVM.

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10143-41, Session 13

Single exposure EUV patterning of BEOL metal layers on the IMEC iN7 platform *(Invited Paper)*

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Inc. (United States); Paul Rusu, Friso Wittebrood, ASML Netherlands B.V. (Netherlands)

The imec N7 (iN7) platform has been developed to evaluate EUV patterning performance with design rules equivalent to foundry N5 node. This node has a 42 nm pitch for metal 1 layer and 32 nm pitch for the subsequent metal 2 layer and metal 3 layer and it is considered to be the first scaling node at which industry likely will insert EUV into production.

The Imec baseline integration scheme for iN7 node uses 1D design style with Singe Exposure (SE) EUV for metal 1 layer, SE EUV for Via 1 and SAQP plus SE EUV block for metal 2 layer. At the same time the platform also includes metal 1 2D designs and metal 2 SE EUV for evaluation purposes.

This paper will investigate full SE EUV patterning, litho and etch, of most critical BEOL metal layers available in the iN7 platform. The studied cases comprise:

- Metal 1 1D design: 42 nm pith, 24 nm trench width and 24 nm tip to tip
- Metal 1 2D design: 36 nm horizontal and vertical pitch and 18 nm tip to end
- Metal 2 1D design: 32 nm pitch, 16 nm trench width and 30 nm tip to tip

For each of the layers, a source optimization, OPC model calibration and OPC have been performed with Tachyon computational lithography software. Exposures on ASML NXE:3300 0.33NA EUV systems at Imec and at ASML Veldhoven were carried out using the optimized sources.

Logic structures have been measured after litho and after etch. Variability was characterized both with conventional CD-SEM measurements as well as contouring method. After analyzing the patterning of the different layers the impact of variability on potential interconnect reliability was studied using MonteCarlo and electrical simulations.

10143-42, Session 13

Integrated approach to improving local CD uniformity in EUV patterning

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Extreme ultraviolet (EUV) lithography is crucial to enabling technology scaling in pitch and critical dimension (CD) and to enabling complex two dimensional design rules. Currently, one of the key challenges of introducing EUV lithography to high volume manufacturing (HVM) is throughput, which requires high source power and high sensitivity chemically amplified photoresists. An important limiter of high sensitivity chemically amplified resists (CAR) is the effect of stochastic shot noise and resist blur on dose received per feature, especially at the pitches required for 7 nm and 5 nm nodes. These stochastic effects are reflected in via structures as hole-to-hole CD variation or local CD uniformity (LCDU). Here, we demonstrate a synergistic combination of lithography and plasma etch techniques to reduce LCDU post exposure, which allows the use of high sensitivity resists required for the introduction of EUV HVM. Thus, to improve LCDU to a level required by 5 nm node and beyond, EUV lithography and etch processes were combined and co-optimized to enhance LCDU reduction from synergies.

Test wafers were created by depositing an advanced pattern transfer stack on a substrate representative of a 5 nm node target layer. The advanced pattern transfer stack consists of an atomically smooth adhesion layer and two hard masks and was deposited using the Lam VECTOR® product family. These layers are expected to mitigate hole roughness and provide additional outlets for etch to improve LCDU and control hole CD. These wafers were then exposed through an ASML NXE3350B™ EUV scanner using a variety of advanced positive tone EUV CAR. They were finally etched to the target substrate using Lam Flex™ dielectric and Kiyo® conductor etch systems. Metrology methodologies were also investigated to enable repeatable patterning process development and to reflect chip performance and defectivity.

Illumination conditions in EUV lithography were optimized to improve aerial image contrast which is expected to reduce shot noise related effects. It can be seen that the EUV imaging contrast improvement can further reduce post-develop LCDU from 4.1 nm to 3.9 nm and from 2.8 nm to 2.6 nm. In parallel, etch was developed to further reduce LCDU and hole roughness, to control CD, and to transfer these improvements into the final target substrate. At the target substrate, it can be seen that EUV lithography and etch optimizations improve LCDU to 1.6 nm (3-sigma). We also demonstrate that increasing post-develop CD by 1 nm through dose adjustment can enhance the LCDU reduction from etch by 0.3 nm. Similar trends were also observed in different pitches down to 40 nm. The solutions demonstrated here are critical to the introduction of EUV lithography in high volume manufacturing.

10143-43, Session 13

Comprehensive analysis of line-edge and line-width roughness for EUV lithography

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Pattern transfer fidelity is always a major challenge for any lithography process and needs continuous improvement. Lithographic processes in semiconductor industry are primarily driven by optical imaging on photosensitive polymeric material (resists). Quality of pattern transfer can be assessed by quantifying multiple parameters such as, feature size uniformity (CD), placement, roughness, sidewall angles etc. Roughness in features primarily corresponds to variation of line edge or line width and is gaining significance, particularly due to shrinking feature sizes. This has caused downstream processes (Etch, CMP etc.) to re-assess their tolerance levels. A very important aspect of this work is relevance of roughness metrology from pattern formation at resist to subsequent processes.

In this work we present a comprehensive assessment of Line Edge and Line Width Roughness at all lithographic transfer processes. To simulate effect of roughness a pattern was designed with periodic jogs on the edges of lines with varying amplitude and frequency. Figure 1 shows design pattern with programmed jogs in a symmetric and asymmetric fashion to emulate Line edge and Line Width roughness. Figure 1 also shows respective pattern images formed on mask and wafer. Multiple techniques including, Height-Height Correlation, Power Spectral Density Analysis, Variation of roughness as a function of length, will be applied to analyze roughness of these patterns, primarily to define transfer bounds between processes and also to determine any intrinsic contribution of roughness at each step. Multiple imaging conditions, resist materials and metrology methods will also be assessed.

The aim of this study is to determine the optimum technique for assessment of Line edge and Line Width roughness and be relevant across adjacent and downstream pattern transfer processes. This would also lead to roughness bounds which need to be monitored for each process. We will also present a case study which will implement aforementioned methods. Figure 2 shows plots of Line Edge roughness measurements from programmed macros on both mask and wafer. This clearly indicates amplitudes and frequencies with evident response.

10143-44, Session 13

Study on restricting factors of practical k1 limit in 0.33NA EUV lithography

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As we presented in the last conference, it is much difficult to get down the k1 limit of EUV lithography compared to that of optical lithography especially recent immersion lithography. Even though current 0.33NA NXE3300 tool has enhanced aberration characteristics and variable illumination mode than its predecessor, ADT & NXE3100, still there are limitations related with resolution capability of EUV lithography.

First of all, photon shot noise and immature resist performance play an important role in patterning of very fine patterns. As already known, low sensitivity resists have been widely used to reduce shot noise. However, when considering productivity in EUV lithography, high sensitivity resists are inevitable, so it is necessary to increase image contrast by reducing scanner blur like aberration, M3D, stray light et al.

We have investigated the impact of aberration and limitation in illumination pupil fill ratio in EUV. In particular, the aberration sensitivity is different by the illumination conditions, this was intensified when using the particular pupil. Because the lens calibration are conducted with standard illumination condition in NXE3300, it is necessary to consider different aberration sensitivity in accordance with pattern and used pupil condition in EUV lithography. To ensure the process margin of tech node close to limit, a flexpupil with low pupil fill ratio (PFR) than 0.2 were required. Hence in order to avoid through-put loss at this condition, the new concept of the illuminator design is required without light loss. Contamination of collector mirror can affect the patterning also. We will also report about the patterning effect of pupil deformation by degraded collector in low PFR condition.

10143-45, Session 13

New methodologies for lower-K1 EUV OPC and RET optimization

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EUV lithography is viewed as a highly desirable technology for 5nm node patterning cost reduction and process simplicity. However, EUV has several new and complex patterning issues for the low-K1 imaging at 5nm which will need accurate compensation by mask synthesis tools and flows. The main new issues are: long-range flare variation across the chip, feature dependent focus offsets due to high mask topography, asymmetry inducing shadowing effects which vary across the lens, higher image contrast sensitivity and new metallic resist photochemical responses. Many compensation methodologies exist for these issues but full solutions resolving all these many patterning issues will need to be individually customized and optimized for the many different EUV + 193i flows and specific customer needs in 5nm. These solutions must be successfully deployed at low K1 values and must integrate together to create OPC/RET flows which have high quality, are easy to build and fast to deploy. Therefore, the combined requirements of full reticle correction accuracy, process window, flexibility, ease-of-use and speed can be even more challenging than current optical lithography mask synthesis flows.

Advanced computational methods such as ILT and model-based SRAF optimization are well known to have considerable benefits in process window and resolution for low-K1 193 lithography. However, these methods have not been well studied to understand their benefits for lower-K1 EUV lithography where fabs must push EUV resolution, 2D accuracy and process window to their limits. In this paper we review the state of the art in accurate compensation of several of these complex EUV patterning issues. We then investigate where inverse and other advanced computational methods can improve EUV patterning weaknesses vs. traditional OPC/RET. Next we provide a description of new OPC/RET recipes which have been re-architected to address the additional complexity of overlapping EUV resolution, accuracy and integration issues into a quickly programmable full flow solution.

10143-46, Session 13

Ultrathin EUV patterning stack using polymer brush as an adhesion promotion layer

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Initial readiness of EUV patterning was demonstrated in 2016 with IBM Alliance's 7nm device technology. The focus has now shifted to driving the 'effective' k1 factor and enabling the second generation of EUV patterning. In current EUV lithography, thin photoresist is required to mitigate pattern collapse. Etch budgets necessitate the reduction of underlayer thickness as well. Typical spin-on underlayers show high defectivity when reducing thickness to match thinner resist. Inorganic deposited underlayers are lower in defectivity and can potentially enable ultrathin EUV patterning stacks. However, poor resist-inorganic underlayer adhesion severely limits their use. Existing adhesion promotion techniques are found to be either ineffective or negatively affect the etch budget. Here, using a grafted polymer brush adhesion layer we demonstrate an ultrathin EUV patterning stack comprised of inorganic underlayer, polymer brush and resist. We show printing of fine-pitch features with good lithography process window and low defectivity on various inorganic substrates, with significant improvement over existing adhesion promotion techniques. We systematically study the effect of brush composition, molecular weight and deposition time/temperature to optimize grafting and adhesion. We also show process feasibility through pattern transfer from the resist into typical BEOL stacks.

10143-47, Session 14

Compact 2D OPC modeling of a metal oxide EUV resist for a 7nm node BEOL layer

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Inpria has developed a directly patternable metal oxide hard-mask as a high-resolution photoresist for EUV lithography.1 In this contribution, we describe a Tachyon 2D OPC full-chip model for an Inpria resist as applied to an N7 BEOL block mask application.

Some of the key attributes of this negative tone resist are small molecular building blocks, high EUV absorbance, low resist blur, and high etch resistance. At IMEC, the Inpria resist has been selected for use in the N7 BEOL block mask process module where the minimum pitch of the metal 2 and the contacted poly is 32nm and 42nm, respectively. This layer requires a minimum printed pillar CD of 21nm. As the Inpria resist has fundamentally

different properties compared to a traditional chemically amplified resist, its impact on OPC modeling needs to be understood. Some of the potential challenges that need to be addressed are:

• Film thickness and metrology: the Inpria resist is being used at 18nm film thickness, which can result in low SEM contrast. The SEM measurement can also cause resist shrinkage leading to incorrect or misleading results.

• Low Resist Blur: Inpria resist has a much smaller resist blur, and no long range diffusion. This may cause a different pull back or corner rounding than seen with traditional CAR. It also results in an LWR PSD with a significantly shorter correlation length.

• High Etch Resistance: as a metal oxide, the Inpria resist has very high etch resistance which may impact the final etched pattern transfer compared to CAR.

• Negative-tone behavior: the transition from positive tone resists to negative tone materials in 193 nm immersion lithography has required extensive enhancements to full chip compact modeling tools in order to capture non-optical behaviors such as developer loading effects and mechanical shrinkage deformations.2

In order to achieve the needed model accuracy, it is critical to understand how these parameters interact with the OPC model and the resulting resist and etched patterns. A previous study1 reported that a Tachyon compact OPC model for an Inpria formulation achieved an rms error of 0.35 nm. As this model was calibrated using only 1D patterns, we were interested in extending this result to a more challenging 2D patterning use case. We will present encouraging Tachyon calibration and verification results for the IMEC N7 BEOL block mask full-chip model as well as provide an assessment of the degree to which materials, metrology, and process challenges outlined above impact compact model behavior and requirements.

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10143-48, Session 14

Minimizing wafer overlay errors due to EUV mask non-flatness and thickness variations for 7nm production

Xuemei Chen, Christina Turley, Jed H. Rankin, Timothy A. Brunner, Allen Gabor, GLOBALFOUNDRIES Inc. (United States)

EUV mask flatness induced overlay error is a major risk factor for the deployment of EUV lithography into high volume production at 7nm. Mask backside non-flatness and thickness variations, combined with conformal electrostatic chucking and non-telecentric illumination lead to image placement errors on the wafer during EUV exposure. State of the art EUV reticles with a peak-to-valley (P-V) flatness of ~60nm(1) would result in wafer overlay errors of over 1.5nm, exceeding the total overlay budget allocated to masks for 7nm devices. Effective application of mask write compensation (pre-shifting patterns during mask writing to compensate for predicted image placement errors) and scanner higher-order intrafield correction will be necessary for minimizing the on-wafer overlay errors arising from mask non-flatness and thickness variations. In this work, analytical strategies are explored and quantitative approaches are provided to answer the following questions:

1. What is the effective on-product overlay impact from mask non-flatness and thickness variations for typical EUV mask blanks?

A comprehensive characterization of EUV mask blanks with flatness and thickness variations representative of that expected for the 7nm node is performed using Legendre polynomial expansion. Analytical IPD (in-plane distortion) and OPD (out-of-plane distortion) models are developed to translate mask flatness and thickness variations into on-wafer image placement errors. The magnitudes and spatial frequency components of major overlay errors that would need to be reduced with mask compensation or scanner intrafield correction are quantified.

2. What are the quantitative goals for mask write compensation and scanner intrafield correction?

The total mask flatness induced overlay errors are partitioned into global distortions correctable by scanner higher-order intrafield correction, remaining distortions that can be compensated by mask writers, and non-correctable local residual errors. EUV specific high-order intrafield overlay models are utilized to maximize the scanner correction ability. A method to transform the Legendre polynomial representation of mask surfaces into scanner correction polynomial terms is developed. Significance of the remaining distortions (after scanner correction) and feasibility for additional mask write compensation are assessed.

3. What is the minimum overlay impact from mask flatness achievable using the combined compensation strategy? What is a practical EUV mask flatness specification required for 7nm production? What is the optimal correction methodology using the various correction methods?

Various scenarios for combining scanner correction with mask write compensation are analyzed and a strategy for minimizing mask induced overlay errors is proposed for achieving the on-product overlay required at 7nm. The EUV mask flatness and thickness variation requirements are evaluated and a practical mask blank specification is determined that will drive the continuous development of cost effective manufacturing solutions.

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10143-49, Session 14

Single-expose patterning development for EUV lithography

Anuja De Silva, Jefferey C. Shearer, Karen E. Petrillo, Luciana Meli, Joe Lee, Indira Seshadri, Nicole Saulnier, John C. Arnold, Bassem Hamieh, IBM Corp. (United States); Genevieve Beique, GLOBALFOUNDRIES Inc. (United States); Tsuyoshi Furukawa, Lovejeet Singh, Ramakrishnan Ayothi, JSR Micro, Inc. (United States)

Initial readiness of EUV patterning was demonstrated in 2016 with IBM Alliance's 7nm device technology. The focus has now shifted to driving the 'effective' k1 factor and enabling the second generation of EUV patterning. With the substantial cost of EUV exposure there is significant interest in extending the capability to do single exposure patterning with EUV. To enable this, emphasis must be placed on the aspect ratios, adhesion, defectivity control, selectivity, and imaging control of the whole patterning process. Innovations in resist materials and processes must be included to realize the full entitlement of EUV lithography at 0.33NA. In addition, enhancements in the patterning process to enable good defectivity, lithographic process window, and post etch pattern fidelity are also required. Through this work, the fundamental challenges in driving down the effective k1 factor will be highlighted.

10143-50, Session 14

Single-nm resolution approach by applying DDRP and DDRM

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EUV lithography has been desired as the leading technology for single nm half-pitch patterning. However, the source power, masks and resist materials still have critical issues for mass production. Especially in resist materials, RLS trade-off is the key issue. To overcome this issue, we are suggesting Dry development rinse process (DDRP) & materials (DDRM) as the pattern collapse mitigation approach. This DDRM can perform not only as pattern

collapse free materials for fine pitch, but also as the etching hard mask against bottom layer (spin on carbon : SOC). In this paper, we especially propose new approaches to achieve high resolution around hp10nm. The key points of our concepts are 100% water solvent system and PR smoothing. This new DDR technology can be the promising approach for hp10nm level patterning in N7/N5 and beyond.

10143-51, Session 15

Scaling LPP EUV sources to meet high-volume manufacturing requirements

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In this paper, we provide an overview of various challenges and their solutions for scaling laser-produced-plasma (LPP) extreme-ultraviolet (EUV) source performance to enable high volume manufacturing. We will discuss improvements to source architecture that facilitated the increase of EUV power from 100W to >200W, and the technical challenges for power scaling of key source parameters and subsystems. Finally, we will describe current power-scaling research activities and provide a forward looking perspective for LPP EUV sources towards 500W.

10143-52, Session 15

Performance of 250W high-power HVM LPP-EUV source

Hakaru Mizoguchi, Gigaphoton Inc. (Japan)

We have been developing CO2-Sn-LPP EUV light source which is the most promising solution as the 13.5nm high power light source for HVM EUVL. Unique and original technologies such as; combination of pulsed CO2 laser and Sn droplets, dual wavelength laser pulses shooting and mitigation with magnetic field have been developed in Gigaphoton Inc.. The theoretical and experimental data have clearly showed the advantage of our proposed strategy. Based on these data we are developing first practical source for HVM; "GL200E". This data means 250W EUV power will be able to realize around 20kW level pulsed CO2 laser. We have reported engineering data from our resent test such around 43W average clean power, CE=2.0%, with 100kHz operation and other data 1). We have already finished preparation of higher average power CO2 laser more than 20kW at output power cooperate with Mitsubishi electric cooperation2). We achieved 132W with 100kHz, 50% duty cycle operation during 120 hour3). Recently we have demonstrated short term operation at 264 W level open loop operation at proto type #2 system4).

We are now constructing new high power HVM LPP-EUV source with >25kW CO2 driver laser system made by Mitsubishi Electric. At the conference we will report the performance of the new system and updated data of old systems.

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10143-53, Session 15

Further enhancement of LPP sources for more efficient EUV using multiple dual beams on single target

Ahmed Hassanein, Tatyana Sizyuk, Purdue Univ. (United States)

Light sources for extreme ultraviolet (EUV) lithography continued to face challenges in the demanding performance for high volume manufacture. Currently EUV and beyond source developments are focused on dual-pulse laser produced plasma (LPP) using droplets of mass-limited targets. These systems require extensive optimization to enhance the conversion efficiency (CE) and increase components lifetime using experimental and development efforts.

We continued to further enhance our HEIGHTS comprehensive simulation package and CMUXE laboratories to analyze and optimize LPP sources and to make projections and realistic predictions of near future powerful devices. HEIGHTS currently includes 3-D detail description of all physical processes involved in LPP devices. The models continued to be well benchmarked in each interaction physics phase of plasma evolution and EUV production as well as in the integrated LPP systems. We simulated and compared multiple dual laser beams in full 3-D geometry using tin droplets and fragmented targets of tiny droplets distribution. We studied the effect of three incident simultaneous laser beams from multiple directions (with similar total energy in a single dual pulse system) on the CE of these systems. We studied mass dependence, laser parameters effects, atomic and ionic debris generation, and optimization of EUV radiation output. Our enhanced modeling and simulation included all phases of laser target evolution: from laser/droplet interaction, vaporization and fragmentation, ionization, plasma hydrodynamic expansion, thermal and radiation energy redistribution, and EUV photons collection. Modeling results were benchmarked against experimental studies for the in-band photons production and for debris and ions generation.

10143-54, Session 15

High-radiance LDP source for mask inspection and beam line applications

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High-throughput actinic mask inspection tools are needed as EUVL begins to enter into volume production phase. One of the key technologies to realize such inspection tools is a high-radiance EUV source of which radiance is supposed to be as high as 100 W/mm2/sr. Ushio is developing laser-assisted discharge-produced plasma (LDP) sources. Ushio's LDP source is able to provide sufficient radiance as well as cleanliness, stability and reliability. Radiance behind the debris mitigation system was confirmed to be 120 W/mm2/sr at 9 kHz and peak radiance at the plasma was increased to over 200 W/mm2/sr in the recent development which supports high-throughput, high-precision mask inspection in the current and future technology nodes. One of the unique features of Ushio's LDP source is cleanliness. Cleanliness evaluation using both grazing-incidence Ru mirrors and normal-incidence Mo/Si mirrors showed no considerable damage to the mirrors other than smooth sputtering of the surface at the pace of a few nm per Gpulse. In order to prove the system reliability, several long-term tests were performed. Data recorded during the tests was analyzed to assess two-dimensional radiance stability. In addition, several operating parameters were monitored to figure out which contributes to the radiance stability.

The latest model that features a large opening angle was recently developed so that the tool can utilize a large number of debris-free photons behind the debris shield. The model was designed both for beam line application and high-throughput mask inspection application. At the time of publication, the first product is supposed to be in use at the customer site.

10143-55, Session 15

Free-electron laser emission architecture impact on EUV lithography

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Laser-produced plasma (LPP) EUV sources have demonstrated 120 W at customer sites, establishing confidence in EUV lithography as a viable manufacturing technology. However, beyond the 7 nm technology node existing scanner/source technology must enable either higher-NA imaging systems (requiring increased resist dose and providing half-field exposures) or EUV multi-patterning (requiring increased wafer throughput proportional to the number of exposure passes). Both development paths will require a substantial increase in EUV source power to maintain the economic viability of the technology, creating an opportunity for free-electron laser (FEL) EUV sources. FEL-based EUV sources offer an economic, high-power/single-source alternative to LPP EUV sources. Should free-electron lasers become the preferred next generation EUV source, the choice of FEL emission architecture will greatly affect its operational stability and overall capability.

A near-term industrialized FEL is expected to utilize one of the following three existing emission architectures: (1) self-amplified spontaneous emission (SASE), (2) regenerative amplification (RAFEL), or (3) self-seeding (SS-FEL). Model accelerator parameters have been established to use when evaluating the impact of emission architecture on FEL output. Then, variations in the parameter space are applied to assess the potential impact to lithography operations, thereby establishing component sensitivity. The operating range of various accelerator components is discussed based on current accelerator performance demonstrated at various scientific user facilities. Finally, comparison of the performance between the model accelerator parameters and the variation in parameter space provides a means to evaluate the potential emission architectures. A scorecard is presented to facilitate this evaluation and provide a framework for future FEL design and enablement for EUV lithography applications.

Conference 10144: Emerging Patterning Technologies 2017

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10144-1, Session 1

Meta-lens: A new generation of optics for the 21st century *(Keynote Presentation)*

Federico Capasso, Harvard School of Engineering and Applied Sciences (United States)

No Abstract Available

10144-2, Session 1

Applying NIL for device fabrication and challenges in nano-defect management *(Keynote Presentation)*

Tatsuhiko Higashiki, Toshiba Corp. (Japan)

Cost reduction is a critical factor for the fabrication of high performance memory devices and will continue to be a focus for future generations of devices. However, investment costs in pattern shrinking technologies, such as multi-patterning and EUVL have become enormous, and encompass additional etch and deposition systems as well as the infrastructure equipment necessary to support these technologies. The framework surrounding these pattern shrinking technologies has not been able to provide lower-cost semiconductor devices. Therefore, in order to significantly reduce investment cost in lithography, nanoimprint lithography (NIL) technology has aggressively been developed1).

Over the past few years, Toshiba, with the support of Canon, has developed NIL technology for the application of advanced memory devices and succeeded in yielding working devices at dimensions less than 20nm2). We are in the process of verifying the fundamental technologies and the compatibility of NIL to the Si-fab and are now preparing the NIL technology for the production line. To be successful however, we must solve the unique challenges of NIL in defectivity, overlay accuracy, and productivity. Additionally, we have to understand new phenomena in lithography, such as the polymer rearrangement influences on liquid resists, as well as nano-fluidic mechanisms. Potential defect mechanisms such as nano-bubble and metal ion content must also be understood and addressed

The previous incarnation of EIDEC focused on EUVL the development of a supporting infrastructure. However, in June 2016, a new EIDEC consortium was formed and the EIDEC acronym has evolved to represent its new thrust: “Evolving nano process Infrastructure Development Center”. The new EIDEC mission was adopted as a part of a new national program in Japan. The consortium is responsible for addressing various forms of “Nano Defect Management (NDM)” in the pursuit of LSI scaling well below 20nm. This includes both scaling and cost reduction methods in manufacturing, with the purpose of identifying scaling challenges at the nanoscale and developing solutions that enable new manufacturing methods.

For any lithographic approach, nano-scaled defects and particles are quickly becoming one of the main contributors for yield losses. As a result, the challenge will be the management of the nano-scaled defects and particles. NDM will be an enabler that drives to future lithographic solutions and methods. The new EIDEC covers the gamut of semiconductor processes and related concerns regarding defectivity. In lithography, EIDEC’s charter covers all lithographic approaches such as optical, NIL, EUVL and DSA. The intent of NDM is to mitigate the defects and/or particles for all unit processes. The process cycle includes inspection, clarification of root causes, countermeasures, and controls.

As applied to the development of the NIL infrastructure, NDM includes issues such as:

1) Advanced metrology and Inspection: As an example, electron beam inspection for wafer and imprint templates, including multi CD-SEM inspection.

2) Resist and material Innovation: Etching resistance improvement to reduce defects on the template and wafer.

3) Super clean tools and clean room environment: The cycle for mitigating defects and/or particles for all unit processes.

4) Cleaning technology: The process cycle includes inspections, clarification of root causes, countermeasures, and controls.

In this paper, the status of the nanoimprint lithography for high volume manufacturing will be discussed, along with key challenges that must be addressed. The role of EIDEC in identifying these challenges and developing NDM solutions will also be discussed.

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10144-3, Session 1

Security applications for direct-write lithography *(Keynote Presentation)*

Mike Borza, Synopsys Inc. (Canada)

No Abstract Available

10144-4, Session 2

Nanoimprint system development for high-volume semiconductor manufacturing and status of overlay performance *(Invited Paper)*

Yukio Takabayashi, Mitsuru Hiura, Hiroshi Morohoshi, Nobuhiro Kodachi, Tatsuya Hayashi, Atsushi Kimura, Takahiro Yoshida, Kazuhiko Mishima, Yoshio Suzaki, Canon Inc. (Japan); Jin Choi, Canon Nanotechnologies, Inc. (United States)

Nanoimprint Lithography (NIL) is an effective technique for replication of nano-scale features. Jet and Flash Imprint Lithography* (J-FIL*) involves the field-by-field deposition and exposure of a low viscosity resist deposited by Drop-On-Demand inkjet onto the substrate. The patterned mask is lowered into the fluid which then quickly flows into the relief patterns in the mask by capillary action. Following this filling step, the resist is crosslinked under UV radiation, the mask is removed, and leaves a patterned resist on the substrate.

Previous studies have demonstrated J-FIL* resolution better than 10nm, making the technology suitable for the printing of several generations of critical memory levels with a single mask. In addition, resist is applied only where necessary, thereby eliminating material waste. Given that there are no complicated optics in the imprint system, the reduction in the cost of the tool, when combined with simple single level processing and zero waste leads to a cost model that is very compelling for semiconductor memory applications.

There are many other criteria besides resolution that determine whether a particular technology is ready for manufacturing. In 2016, Takashima et al. introduced the FPA-1200NZ2C cluster system designed for high volume manufacturing of semiconductor devices. Described in this work were the advancements made defectivity, throughput and overlay. As of early

2016, tool particle adders were approaching 0.001 pieces per wafer, overall defectivity was approximately 5 defects/cm2, throughput of 17 wafers per hour per station (for an overall system throughput of 68 wafers per hour) was achieved and a mix and match overlay of better than 5nm (mean + 3sigma) was demonstrated.

The purpose of this paper is to update progress made in particle adders, defectivity, throughput and overlay, with an emphasis on the methods used to enhance system overlay.

Nanoimprint lithography requires field by field alignment approach, and Canon has adopted a through the mask (TTM) alignment system with 1nm repeatability. An array of piezo actuators are applied to enable linear corrections. To realize improved overlay results, it was necessary to address wafer chuck flatness issues that introduce distortion, particularly towards the edge of the wafer. By reducing chuck flatness, local deformations were reduced to about 4nm.

In this presentation we discuss the additional improvements needed to the tool, mask and wafer to meet aggressive overlay specifications. This includes both a local heating high order correction method on the tool as well as mask chucks that reduce the added image placement budget for a replica mask to less than 1nm.

Additionally we will address the error factors of NIL alignment which include matching distortion with the underlying device layer, differences between imprint stations, difference between masks, and so on. We will also introduce the application of alignment control for nanoimprint by using a feed-forward methodology based on alignment residual data. This is possible, as Archer measurements on a printed wafer are very well correlated with the imprint TTM data. Finally, we will show Canon's overlay roadmap as well new technologies designed to address higher order distortions correction.

10144-5, Session 2

Study of nanoimprint lithography (NIL) for HVM of memory devices

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A low cost alternative lithographic technology is desired to meet the decreasing feature size of semiconductor devices. Nano-imprint lithography (NIL) is one of the candidates for alternative lithographic technologies. (1)(2)(3) NIL has such advantages as good resolution, critical dimension (CD) uniformity and low line edge roughness (LER). On the other hand, the critical issues of NIL are defectivity, overlay, and throughput. In order to introduce NIL into the HVM, it is necessary to overcome these three challenges simultaneously.(4)-(12) In our previous study, we have reported a dramatic improvement in NIL process defectivity on a pilot line tool, FPA-1100 NZ2. We have described that the NIL process for 2x nm half pitch is getting closer to the target of HVM.(12) In this study, we report the recent evaluation of the NIL process performance to judge the applicability of NIL to memory device fabrications. In detail, the CD uniformity and LER are found to be less than 2nm. The overlay accuracy of the test device is less than 7nm. A defectivity level of below 1pcs./cm2 has been achieved at a throughput of 15 wafers per hour.

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10144-6, Session 2

Improved defectivity and particle in nanoimprint tool for high-volume semiconductor manufacturing

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There are many criteria that determine whether a particular technology is ready for wafer manufacturing. Defectivity and mask life play a significant role relative in meeting the cost of ownership (CoO) requirements in the production of semiconductor devices. NIL, like any lithographic approach requires that defect mechanisms be identified and eliminated in order to consistently yield a device. NIL has defect mechanisms unique to the technology, and they include, liquid phase defects, solid phase defects and particle related defects. Examples of these types of defects have been discussed previously.

Especially, more troublesome are hard particles on either the mask or wafer surface. Hard particles run the chance of creating a permanent defect in the mask, which cannot be corrected through a mask cleaning process. Because of this, hard particles play a significant role in determining the mask life time.

To meet CoO specifications, the replica mask life must be maintained for at least 1000 wafers. If the conservative assumption is made that every hard particle damages the mask, then the number of particle adders must be less than 0.001 pieces per wafer. To achieve this particle specification, an aggressive strategy is needed to remove particles adders from the wafer and mask. Hard particles on a wafer or mask create the possibility of inducing a permanent defect on the mask that can impact device yield and mask life.

In a previous paper Emoto et al., defectivity in the imprint tool was reduced by more than two orders of magnitude. One of the contributors to defectivity were particle generated within the tool. To remedy this issue, new particle reduction methods were introduced, including both the treatment of specific material surfaces and the optimization of an air curtain system to control airflow around both the wafer and mask.

Initially, the air curtain was first tested in a dedicated test stand. Using an accelerated testing procedure, we were able to eliminate all particles on a wafer.

As a result, the air curtain was next applied to the imprint tool and runs of nearly 1000 wafers were performed. Relative to the case without an air curtain, particle adders were reduced by a factor of twenty, achieving a particle adder per wafer pass count of only 0.003 pieces per wafer, close to the targeted specification of 0.001 pieces per wafer.

More recently, an optimized air flow system has been combined with new cleaning protocols, resulting in a particle adder count of only 0.0008 pieces per wafer, which is equivalent to a single particle over 1232 wafers. In this presentation, we will report the details that enabled the path towards achieving mask lifetimes of better than 1000 wafers. We will also discuss additional particle reduction methods, including charge neutralization to further extend mask life. Finally, we will describe how the developed particle reduction technology can be extended to all imprint platforms.

10144-7, Session 2

Progress on throughput and defectivity using jet and flash imprint lithography for high-volume manufacturing

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Nanoimprint lithography techniques are known to possess replication resolution below 5nm. A specific form of imprint lithography known as Jet and Flash Imprint Lithography* (J-FIL*) has been developed for manufacturing advanced CMOS memory. A one step patterning at 15nm half-pitch can be achieved with J-FIL eliminating the need of complicated and expensive Self-Aligned-Quadruple–Patterning. In addition, patterns are not limited to repeating structures such as lines and spaces thereby leading to significant cost savings in patterning. J-FIL involves field-by-field inkjet deposition of a low viscosity resist fluid followed by imprinting with nano-scale precision overlay. A mask with a relief structure is lowered into the fluid which then quickly flows into the relief patterns in the mask by capillary action. Following this filling step, the resist is crosslinked under UV radiation, and then the mask is separated from the substrate leaving a patterned resist on the substrate.

The key to achieving high throughput is the filling step, in which the resist drops must merge together and fill all relief images on the imprint mask. There are several parameters that can impact resist filling. Key parameters include:

- Resist drop volume (smaller is better),
- System controls (which address drop spreading after jetting),
- Design for Imprint or DFI (to accelerate drop spreading)
- Material engineering (to promote wetting between the resist and underlying adhesion layer).

In 2016, we addressed improvements made in drop volume, material engineering, DFI and system controls to enable a 1.50 second filling process for a sub-20nm device like pattern which includes both full fields and edge fields. Figure 1 describes the changes made in the imprint process and the resulting reduction in feature filling.

In this work, we have increased throughput to over 17 wafers per hour, thereby achieving a throughput of 68 wafers per hour for a four station NZ2C cluster tool. The increase in throughput was driven by further improvements to the imprint material and additional reductions in resist drop volume.

Next, customized cleaning processes were applied to the NZ2C wafer imprint tool, and a methodology was established addressing cleaning protocols during tool manufacture, maintenance and operation. The combination of material treatment, air flow optimization and cleaning were then tested on the NZ2C for a simulated run of over 1200 wafers. Only a single particle event was detected over the run, which is equivalent to a particle adder specification of 0.0008 particles per wafer, surpassing the target of a 1000 wafer mask life.

After the implementation of all the particle reduction methods discussed, a test run was done at a throughput of greater than 17 wafers per hour on the FPA-1200NZ2C imprint system across 25 wafers with a minimum half pitch of 30nm to understand whether defect levels on imprinted wafers were also reduced. Figure 2 shows the result of this study. In this figure, the defectivity is shown for every imprint of the run. Inspections were done using a KLA-T 2905 in array mode. After the 25 wafer run, the increase in defectivity was just 1.5/cm2.

Details of both the throughput and defectivity runs will be described. In addition, we will discuss the steps necessary to increase the throughput to 20 wafers per hour while and reducing the defectivity to less than 1 defect/cm2.

*Jet and Flash Imprint Lithography and J-FIL are trademarks of Molecular Imprints Inc.

10144-8, Session 2

Overlay control for nanoimprint lithography

Kazuya Fukuhara, Masato Suzuki, Masaki Mitsuyasu, Takuya Kono, Tetsuro Nakasugi, Toshiba Corp. (Japan); Yong-Hyun Lim, Woo-Yung Jung, SK Hynix, Inc. (Korea, Republic of)

Nanoimprint lithography (NIL) is a promising technique for fine-patterning with a lower cost than other lithography techniques such as EUV or immersion with multi-patterning. The NIL tool for 300mm Si wafer has a simple structure, and does not have large components such as lasers, projection optics, or vacuum chambers. However, NIL has the potential of “single” patterning for both line patterns and hole patterns with a half-pitch of less than 20nm.

It has been pointed out that there are four issues for applying NIL into mass-production [1]. They are defectivity, overlay, throughput, and template infrastructure. As for overlay, NIL employs die-by-die alignment with moire fringe detection [2] and an alignment measurement accuracy of below 1nm [3]. An overlay accuracy of below 5nm [4] has been reported. NIL-to-NIL overlay, that is, NIL overlay on underlayer patterns made by NIL, shows less than 3nm in 3sigma for the overlay residual [5].

An overlay accuracy of less than 3nm will be expected for chip manufacturing in around 2020[6]. In order to qualify for the requirements from the semiconductor industry, more and more enhancements of NIL technology, such as an improvement in the overlay control accuracy for NIL-tool, image placement accuracy improvement for NIL templates and mix & match technique of NIL and other lithography tools such as an immersion exposure tool, are needed.

In this paper we describe the evaluation results of NIL the overlay performance using an up-to-date NIL tool for 300mm wafer, and discuss the potentials of NIL overlay improvement. For NIL tools, alignment accuracy, precision, stability, and overlay correction performance are discussed. For templates, an overlay error originating from the image placement (IP) error of the master/replica template and the active correction of template IP for distortion matching to an underlayer on a wafer will be discussed. As for process control, we will describe the progress of both NIL-to-NIL and NIL-to-immersion distortion matching techniques while considering the overlay error structure analysis (intrashot, intrawafer, wafer-to-wafer, etc.). The relation of the overlay accuracy and the throughput will be also discussed. From these analyses based on actual NIL overlay data, we will discuss the possibility of NIL overlay evolution to realize an on-product overlay of less than 3nm.

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10144-9, Session 3

Nanoimprint of a 3D structure on an optical fiber for light wavefront manipulation *(Invited Paper)*

Keiko Munechika, Giuseppe Calafiore, Alexander Koshelev,

Carlos Pina-Hernandez, Abeam Technologies, Inc. (United States); Frances I. Allen, Univ. of California, Berkeley (United States); Scott D. Dhuey, Simone Sassolini, Edward Wong, Lawrence Berkeley National Lab. (United States); Paul Lum, Univ. of California, Berkeley (United States); Stefano Cabrini, Lawrence Berkeley National Lab. (United States)

Integration of complex photonic structures onto optical fiber facets enables powerful platforms with unprecedented optical functionalities. Conventional nanofabrication technologies, however, do not permit viable integration of complex photonic devices onto optical fibers owing to their low throughput and high cost. In this work, we report the fabrication of three-dimensional structures achieved by direct nanoimprint lithography on the facet of an optical fiber.

Nanoimprint processes and tools were specifically developed to enable a high lithographic accuracy and coaxial alignment of the optical device with respect to the fiber core. To demonstrate the capability of this new approach, a 3D beam splitter has been designed, imprinted and optically characterized. (Figure 1) Scanning electron microscopy and optical measurements confirmed the good lithographic capabilities of the proposed approach as well as the desired optical performance of the imprinted structure.

One of the key advantages of this approach is capability to imprint optical elements comprised of materials with functional properties. In this regard, we also report direct imprinting of Fresnel lens, where the structure itself is made out of a high refractive index (n = 1.68) material. (Figure 2) This lens enables efficient light focusing even inside other media, such as water or an optical adhesive. Measurement of the lens performance in an immersion liquid (n = 1.51) shows a near diffraction limited focal spot of 810 nm in diameter at the 1/e2 intensity level for a wavelength of 660 nm. The inexpensive approach presented here should enable advancements in areas such as integrated optics and sensing, achieving enhanced portability and versatility of fiber optic components.

10144-10, Session 3

Selective surface smoothening of 3D micro-optical elements

Helmut Schift, Robert Kirchner, Nachiappan Chidambaram, Paul Scherrer Institut, ETH Zürich (Switzerland); Mirco Altana, Heptagon Oy (Switzerland)

Optical polymer microlenses are used in various devices, including smartphones. Since they are so small, they have to be processed using novel 3D lithographic methods that build the lenses out of thin layers (e.g. grayscale electron or laser writing). However, this often results in roughness, which has adverse effects for optical applications. If a surface has to be subsequently smoothed out, it must be achieved using a method that only modifies the surface (around 100 nm) and does not change the underlying layers or overall shape. For this a method known as TASTE was developed. It involves selectively changing the material properties of the part of the sample that needs modification, i.e. locally confined in lateral or vertical direction. By use high energy exposure the polymer is modified at a defined depth of the surface by chain scission followed by molecular weight dependent reflow at elevated temperatures. For surface smoothening of microlenses we have found 172 nm UV exposure to be the ideal fit for this application. A lens design with a test micro-lens array (3x3) with concave lenses 50 x 50 um2 (each) and a height of 50 um from tips at the four corners to the central sag was chosen. For optical measurements, the lens array was expanded to a circular array larger than 2 mm in diameter. Lenses were exposed with direct laser writing using 2-photon-polymerization from NanoScribe in their proprietary IP-dip resist. After conversion into PMMA by 2-step copying process using UV and thermal NIL, the PMMA surface was exposed with VUV light and the surface subjected to heat enabling surface confined thermal reflow. This provided high enough damage in a 200 nm thick surface skin layer and negligible etching, which allowed smoothening out up to 100 nm roughness. The original structure (in IP-dip) as well as the PMMA replicas, were optically measured. For testing of structural deformation and surface roughness variation upon post-processing (reflow), additional pyramidal structures with lower height defined but defined steps were created. They enabled to discriminate between desired reduction of roughness (surface confinement) and unwanted collapse of structure (reflow of entire structure) using AFM microscopy. A roughness of 100 nm could be removed while preserving the concave shape with up to 40 um high structures and deep central sags surrounded by high aspect ratio tips between adjacent lenses in array configuration. A significant reduction of straylight was also proven by optical measurement. Such processes can also be used for smoothening mirrors, microfluidic devices or other devices where sub-10 nm roughness is required, or simple for the removal of roughness and cracks from damaged surfaces.

10144-11, Session 3

New 3D structuring process for non-integrated circuit related technologies

Lamia Nouri, Nicolas Possémé, Stéfan Landis, Frédéric Milesi, Frédéric-Xavier Gaillard, Commissariat à l'Énergie Atomique (France)

Fabrication processes that microelectronic developed for Integrated circuit (IC) technologies for decades, do not meet the new emerging structuration's requirements, in particular non-IC related technologies one, such as MEMS/NEMS, Micro-Fluidics, photovoltaics, lenses. Actually complex 3D structuration requires complex lithography patterning approaches such as gray-scale electron beam lithography, laser ablation, focused ion beam lithography, two photon polymerization. It is now challenging to find cheaper and easiest technique to achieve 3D structures.

In this work, we propose a straightforward process to realize 3D structuration, intended for silicon based materials (Si, SiN, SiOCH). This structuration technique is based on nano-imprint lithography (NIL), ion implantation and selective wet etching. In a first step a pattern is performed by lithography on a substrate, then ion implantation is realized through a resist mask in order to create localized modifications in the material, thus the pattern is transferred into the subjacent layer. Finally, after the resist stripping, a selective wet etching is carried out to remove selectively the modified material regarding the non-modified one.

In this paper, we will first present results achieved with simple 2D line array pattern processed either on Silicon or SiOCH samples. This step have been carried out to demonstrate the feasibility of this new structuration process. SEM pictures reveals that "infinite" selectivity between the implanted areas versus the non-implanted one could be achieved. We will show that a key combination between the type of implanted ion species and wet etching chemistries is required to obtain such results.

The mechanisms understanding involved during both implantation and wet etching processes will also be presented through fine characterizations with Photoluminescence, Raman and Secondary Ion Mass Spectrometry (SIMS) for silicon samples, and ellipso-porosimetry and Fourier Transform InfraRed spectroscopy (FTIR) for SiOCH samples. Finally the benefit of this new patterning approach will be presented on 3D patterns structures.

10144-12, Session 3

Development of nanoimprint lithography templates for the contact hole layer application

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Nanoimprint lithography, NIL, is gathering much attention as one of the most potential candidates for the next generation lithography for

semiconductor. This technology needs no pattern data modification for exposure, simpler exposure system, and single step patterning process without any coat/develop truck, and has potential of cost effective patterning rather than very complex optical lithography and/or EUV lithography.

NIL working templates are made by the replication of the EB written high quality master templates. Fabrication of high resolution master templates is one of the most important issues. Since NIL is 1:1 pattern transfer process, master templates have 4 times higher resolution compared with photomasks. Another key is to maintain the quality of the master templates in replication process. NIL process is applied for the template replication and this imprint process determines most of the performance of the replicated templates.

Expectations to the NIL are not only high resolution line and spaces but also the contact hole layer application. Conventional ArF-i lithography has a certain limit in size and pitch for contact hole fabrication. On the other hand, NIL has good pattern fidelity for contact hole fabrication at smaller sizes and pitches compared with conventional optical lithography.

Regarding the tone of the templates for contact hole, there are the possibilities of both tone, the hole template and the pillar template, depending on the processes of the wafer side. We have succeeded to fabricate both types of templates at 2xnm in size.

In this presentation, we will be discussing fabrication or our replica template for the contact hole layer application. Both tone of the template fabrication will be presented as well as the performance of the replica templates. We will also discuss the resolution improvement of the hole master templates by using various e-beam exposure technologies.

10144-13, Session 4

Overview and development of EDA tools for integration of DSA into patterning solutions *(Invited Paper)*

J. Andres Torres, Germain L. Fenger, Daman Khaira, Yuansheng Ma, Yuri Granik, Chris Kapral, Joydeep Mitra, Mentor Graphics Corp. (United States); Polina Krasnova, Mentor Graphics Corp. (Russian Federation)

Directed Self-Assembly is the method by which a self-assembly polymer is forced to follow a desired geometry defined or influenced by a guiding pattern. Such guiding pattern uses surface potentials, confinement or both to achieve polymer configurations that result in circuit-relevant topologies, which can be patterned onto a substrate.

Chemo, and grapho epitaxy of lines and space structures are now routinely inspected at full wafer level to understand the defectivity limits of the materials and their maximum resolution. In the same manner, there is a deeper understanding about the formation of cylinders using grapho-epitaxy processes.

Academia has also contributed by developing methods that help reduce the number of masks in advanced nodes by "combining" DSA-compatible groups, thus reducing the total cost of the process.

From the point of view of EDA, new tools are required when a technology is adopted, and most technologies are adopted when they show a clear cost-benefit over alternative techniques. In addition, years of EDA development have led to the creation of very flexible toolkits that permit rapid prototyping and evaluation of new process alternatives.

With the development of high-chi materials, and by moving away of the well characterized PS-PMMA systems, as well as novel integrations in the substrates that play in tandem with the diblock copolymer systems, it is necessary to assess any new requirements that may or may not need custom tools to support such processes.

Hybrid DSA processes (which contain both chemo and grapho elements), are currently being investigated as possible contenders for sub-5nm process techniques. Because such processes permit the re-distribution of discontinuities in the regular arrays between the substrate and a cut operation, they have the potential to extend the number of applications for DSA.

This paper illustrates the reason as to why some DSA processes can be supported by existing rules and technology, while other processes require the development of highly customized correction tools and models. It also illustrates how developing DSA cannot be done in isolation, and it requires the full collaboration of EDA, Material's suppliers, Manufacturing equipment, Metrology, and electronic manufacturers.

10144-14, Session 4

Free energy modeling of block-copolymer within pillar confinements on DSA lithography

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We perform a systematic study about behavior of asymmetric PS-b-PMMA block copolymers (BCP) within pillar confinement for DSA. In this study, according to brush treatment on pillar surface, self-assembled PMMA cylindrical contact showed various morphologies driven by pillar confinements. Therefore, we firstly show how the perturbation of ordered patterns within irregular distance of pillar can be described in terms of thermodynamics in the array of self-assembled polymer domains.

After pillar guiding preparation, conventional DSA procedure is performed. On the designed DSA pillar guiding scheme, assembled PMMA domain should be located on a triple point area among adjacent three pillars (TPA). In case of small diameter of pillar guide, the period of contacts well match with used BCP period (L0). These represent the existence of contacts is determined by the confinement width, which is given by the physical pillar diameter including the thickness of the surrounding brush layers that form at the surface of the silica pillar. Cheng et al. used a free energy model to understand the behavior of confined block copolymer spheres. The model is applied to the cylinders in our hexagonal confinement and the equation is also modified. We calculate free energy ratio comparing with unperturbed polymer varying pillar diameter, in case of triple point area (TPA) and side area (SA), respectively. Free energy ratio value "1" means ideal phase separation as like on planar substrate without confinements, and higher value means unstable contact generation by pillar perturbation. Therefore, contact engineering caused by incommensurability could be optimized as aspect of pillar diameter. We note that contacts are hardly generated in side area having higher energy. For further engineering to control contacts, we have to increase energy in side area, but at the same time free energy of TP should be maintain "1" as possible.

We have studied how self-assembled BCPs behave within pillar topographic confinement. In our experiments, phase separated PMMA contacts were driven by chemically modified three- dimensional pillar surfaces. In case of neutrally modified pillar surface, the PMMA contacts were perturbed by confinements and the free energy magnitude model compared with unperturbed polymer was applied to understand this phenomenon. Furthermore, the equation was modified so as to utilize two kinds of different confinement width, TPA and SA, respectively. This modeling in hexagonal pillar confinements could be useful for actual DSA engineering, such as a parasitic contact control and the adoption of future guiding scheme.

10144-15, Session 4

Process, design rule, and layout co-optimization for DSA based patterning of sub-10nm Finfet devices

Joydeep Mitra, Andres Torres, Mentor Graphics Corp. (United States); David Z. Pan, The Univ. of Texas at Austin (United States)

There have been extensive research efforts demonstrating the use of DSA to pattern contacts/vias, however, not much work has been done towards the patterning of the most critical Fin layer for fabricating Finfet devices. Self-aligned double patterning (SADP) is the current technology for printing fins at the 16nm/14nm node . Unfortunately, due to the required Mandrel mask in SADP only an even number of fins can be manufactured thus requiring extra trim effort to remove the unnecessary dummy fins. DSA guiding patterns on the other hand natively support both odd and even numbers of fins, thus relaxing the patterning constraints of the trim mask. This paper performs the first comprehensive Monte Carlo simulation based study on Graphoepitaxy based DSA guiding patterns and proposes design guidelines for the fin layer. We further propose layout decomposition algorithms for the DSA guiding pattern and optical trim mask co-optimization.

The key contributions of this paper are as follows:

1. A first patterning methodology leveraging the pitch multiplication property of DSA in manufacturing the fin layer with comparable or better fidelity than SADP but without the even parity constraint of SADP.

2. A first simulation based study and systematic organization of DSA guiding pattern shapes and aspect ratios to optimize the printability of fins and the chemical composition of the DSA process to best target a given fin pitch and CD.

3. A first layout decomposition algorithm for fins using the DSA process based on guidelines obtained from 2 above which partitions fin clusters into optimal groups and then decomposes the resulting groups into guiding pattern and trim masks.

In this paper we begin by optimizing the chemical composition of a given DSA process to match the pitch requirements for a specific 7nm technology followed by an exhaustive simulation driven study of guiding patterns that will best achieve fidelity towards the target design. We then analyze the raw simulation results to obtain a set of guidelines that will map the design onto commensurable guiding patterns. We then provide a layout decomposition algorithm that uses the above mapping to achieve the patterning of the desired target fins. The main contributions of the paper are in the methodology to arrive at an optimal diblock composition subject to a layout decomposition process.

10144-16, Session 4

Advanced fast 3D DSA model development and calibration for design technology co-optimization

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Full chip capable DSA technology has been proposed and demonstrated [1] that can support VLSI SOC Scaling for 7nm node and beyond. Fin patterning for FinFET designs is one of the feasible application where extremely high resolution and immunity to pitch walking is achievable. However, for random logic application, we need to make sure we have a computational tool, especially a fast and accurate 3D DSA model that can enable an early DTCO study and later the development of design manual and PDK.

In this paper we evaluate a fast 3D DSA model that's significantly improved in run time and amenable to area scaling, hence capable for DTCO study. The speed improvement is due to direct minimization of the free energy functional rather than solving the OK model via a modified Cahn-Hilliard equation. Fig. 1 shows a preliminary data set suggesting that the new model exhibits a largely improved scaling characteristic.

The relative commensurability window of a hybrid DSA process for different L/S configurations (a preferred choice for fins patterning) [2] is predicted more reliably by using an improved calibration procedure. The use of various multiplication factors provides a larger calibration space. Fig.2 shows an example set of design constructs that allows different multiplications (hence different guiding strength) in the calibration process and will be tested to verify if a general Arrhenius relation is still valid [3].

This work was partly performed in Synopsys Inc. and various IBM Research and Development Facilities.

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10144-17, Session 4

Engineering the kinetics of DSA toward fast dynamics and low defectivity

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Directed self-assembly (DSA) of block copolymers (BCP) can multiply the resolution of lithography and has been a leading candidate for nanofabrication at advanced nodes. Great progress has been made to achieve the level of ordering, registration and pattern complexity required for semiconductor manufacturing. One of the few remaining roadblocks for DSA is that the number of defects in the BCP structures, although already very small, has not quite met the stringent standard of the industry. Past simulation work on defect annihilation has shown that the defects are highly energetically unfavorable compared to aligned structures and they are likely kinetically trapped. Therefore it is of paramount importance to understand the thermodynamics of DSA so that strategies can be designed to mitigate defect formation and facilitate defect annihilation. Here we investigated the DSA dynamics of polystyrene-block-poly(methyl-methacrylate) (PS-b-PMMA) during thermal annealing on "LiNe Flow" chemically patterned substrates with density multiplication. Both arrested annealing and in-situ AFM imaging were used to capture the evolution of structures through different stages of the annealing process. It was revealed that complex three dimensional structures were nucleated during the early stages of annealing and then became trapped, demonstrating that there exists a complicated thermodynamic landscape between the disordered state and the aligned state. To engineer an optimal landscape for defect-free assembly, DSA parameters such as pattern geometries were systematically explored to study their effects on the dynamic process. Results showed that the DSA conditions had a significant impact on both the evolution of structures and speed of assembly. The optimized dynamic process exhibited no trapped states and the speed of assembly was ~100x faster compared to that of the standard processing conditions.

10144-18, Session 5

Multi-beam mask writer MBM-1000

Hiroshi Matsumoto, Hiroshi Yamashita, Rieko Nishimura, Yasuo Kato, Hideo Inoue, Kenji Otoshi, NuFlare Technology, Inc. (Japan)

We are developing our 1st generation of multi-beam (MB) mask writer MBM-100 for application to N5. It will be released in Q4 2017. This mask writer uses multi-beam optics based on blanking aperture array (BAA), and is designed to handle much larger shot counts than single variable shaped beam (S-VSB) writer, which has been used for producing advanced photomasks in recent decades. Characteristic features in MBM-1000 are 10-nm beam size, 10-bit dose control per pass, and high-speed data path. We use 10-nm beam size not to spoil, and make the most of beam resolution. Shot time resolution of 10-bit is essential to accomplish CD/position control accuracy. Resolution of 10-bit is also advantageous to make dose correction

method simple and robust. MBM-1000 inherits platform and mask transfer system of EBM-9500 with modification for air stage newly introduced.

In this paper, we will introduce design of MBM-1000. Performance of MBM-1000 will be discussed with simulation result on patterning resolution and gray beam writing, along with patterning resolution test. We will report results of patterning tests and tool performance evaluations. Performance of MBM-1000 will be compared with EBM-9000/9500 to discuss how MB and S-VSB mask writes can be efficiently used in production of advanced mask writing and lithography.

10144-19, Session 5

Progress on complementary patterning using plasmon-excited electron beamlets

Zhidong Du, Chen Chen, Liang Pan, Purdue Univ. (United States)

Maskless lithography using parallel electron beamlets is a promising solution for next generation scalable maskless nanolithography. Researchers have focused on this goal but have been unable to find a robust technology to generate and control high-quality electron beamlets with satisfactory brightness and uniformity.

In this work, we will aim to address this challenge by developing a revolutionary surface-plasmon-enhanced-photoemission (SPEP) technology to generate massively-parallel electron beamlets for maskless nanolithography. The new technology is built upon our recent breakthroughs in plasmonic lenses, which will be used to excite and focus surface plasmons to generate massively-parallel electron beamlets through photoemission. Specifically, the proposed SPEP device consists of an array of plasmonic lens and electrostatic micro-lens pairs, each pair independently producing an electron beamlet. During lithography, a spatial optical modulator will dynamically project light onto individual plasmonic lenses to control the switching and brightness of electron beamlets. The photons incident onto each plasmonic lens are concentrated into a diffraction-unlimited spot as localized surface plasmons to excite the local electrons to near their vacuum levels. Meanwhile, the electrostatic micro-lens extracts the excited electrons to form a focused beamlet, which can be rastered across a wafer to perform lithography. Studies showed that surface plasmons can enhance the photoemission by orders of magnitudes. This SPEP technology can scale up the maskless lithography process to write at wafers per hour. In this talk, we will report the mechanism of the strong electron-photon couplings and the locally enhanced photoexcitation, design of a SPEP device, overview of our proof-of-concept study, and demonstrated parallel lithography of 20-50 nm features.

10144-20, Session 5

Simulation analysis of a miniaturized electron optics of the massively parallel electron-beam direct-write (MPEBDW) for multi-column system

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This paper reports a simulation analysis of a miniaturized electron optics for the Massively Parallel Electron Beam Direct-Write (MPEBDW) system. The system consists of a nanocrystalline silicon (nc-Si) electron emitter array (1-3), an active-matrix LSI for driving the electron emitter array (1), a condenser lens array (4) with an anode aperture array, and an einzel type objective lens (see Fig. 1), which have been developed and are evaluated.

Figure 2 (a) shows the present MPEBDW system. A higher throughput Multi-column/Multi-beam system is being developed (Fig.2 (b)). Miniaturization of the column diameter increases the electron beams density, while the field curvature aberration increases. However, the aberration can be compensated by the present MPEBDW electron optics with the coaxial rings structure (1). Moreover, a miniaturized objective lens with multiple lens layers suppresses a coulomb blur and a spherical aberration. Thus, this multi-column scheme can provide an increased number of electron beams without degradation of the writing resolution.

Figures 3(a) and 3(b) indicate a schematic of the miniaturized objective lens and the corresponding electron optics configuration, respectively. The objective lens consists of two electrostatic lenses of 1st Layer (Large) and 2nd Layer (Small). By the 1st Layer, the spacing of arrayed beams from the anode is reduced and electron trajectories included in each beam become parallel. Then, by the 2nd Layer, the beams become parallel and trajectories of each beam are focused on a point.

The characteristics of the objective lens are analyzed using TriComp simulation software. Figure 4 shows calculated equipotential lines and the parallel electron beams trajectories by a Finite Element Method (FEM) taking the coulomb interaction into consideration, where the horizontal axis is a direction of the optical axis, and the vertical axis is a radius of the optics. For the cylindrical coordinates system, only an upper half to the optical axis was calculated. The electron trajectories with a kinetic energy of 10 keV were calculated with the electric potentials as shown in Fig. 4. The mesh size of the triangle element in FEM was 0.2 ?m. The electron trajectories with the distances from the optical axis of 0.5 mm, 1.0 mm, and 1.5 mm at the anode aperture were calculated, where the beam divergence angles were set as ±1 mrad, ±0.3 mrad, and ±0.1 mrad, respectively.

Figure 5 is a magnified image of Fig. 4 within red dashed lines near the focal points. The electron trajectories were intensely affected by a field curvature aberration. Thus a field curvature aberration appears unless the aberration compensation function is introduced. In the electron trajectories from the anode aperture of 0.5 mm, the sizes of the least confusion disks with different beam divergence angles are indicated in Figure 6, where the least confusion disk size corresponds to the focused electron beam size. The beam of 6.5 nm size with ±0.1 mrad beam divergence angle shows that the miniaturized objective lens is suitable for 10 nm order electron beam writing.

10144-21, Session 5

High-resolution direct laser writing

Julia Purtov, Peter Rogin, Leibniz-Institut für Neue Materialien gGmbH (Germany); Elmar Kroner, Robert Bosch GmbH (Germany); Peter de Oliveira, Leibniz-Institut für Neue Materialien gGmbH (Germany)

Flexible design of high precision 3D-crystals interacting with visible wavelengths provides a novel platform for integrated devices applicable in photonics. Current approaches, such as multi-film coatings and various one photon lithography techniques, however, are strongly limited for this purpose. Direct laser writing (DLW) based on a two-photon polymerization appears to be a very promising method, but unfortunately does not provide the vertical resolution needed for structures interacting with visible wavelengths. According to earlier reports, attempts to combine DLW with stimulated emission depletion (STED) did not significantly improve the writing resolution. In this work we demonstrate a new, promising variation of DLW as an alternative to the STED procedure. We demonstrate an easy and very flexible way to generate 3D-photonic crystal structures interacting with visible wavelengths, whose fabrication is facilitated by a threefold improvement of the current direct laser writing resolution. We not only discuss the advantages of the new approach, but also delineate the critical control parameters via simulation and experiments. Moreover, we address the prospect of high resolution direct laser writing (HRDLW) by exemplarily creating optically active structures and structures with free-hanging features smaller than 150 nm. The shape and optical behavior of the structured surfaces were characterized using scanning electron microscopy, UV-Vis measurements and optical microscopy. This easily applicable approach leads to resolution dimension of DLW, applicable not only in optics, but also in various other fields.

10144-22, Session 5

Overlay performance of MAPPER's FLX-1200

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Mapper Lithography has introduced its first product, the FLX–1200, which is installed at CEA-Leti in Grenoble (France). This is a mask less lithography system, based on massively parallel electron-beam writing with high-speed optical data transport for switching the electron beams. This FLX platform is initially targeted for 1 wph performance for 28 nm technology nodes, but can also be used for less demanding imaging. The electron source currently integrated is capable of scaling to 10 wph at the same resolution performance, which will be implemented by gradually upgrading the illumination optics. The system has an optical alignment system enabling mix-and-match with optical 193 nm immersion systems using standard NVSM marks. The tool at CEA-Leti is in-line with a Sokudo Duo clean track. Mapper Lithography and CEA-Leti are working in collaboration to develop turnkey solution for specific applications.

At previous conferences we have presented imaging results including 28nm node resolution, cross wafer CDu of 2.5nm 3 and a throughput of half a wafer per hour, overhead times included. At this conference we will present results regarding the overlay performance of the FLX-1200.

In figure 2 an initial result towards measuring the overlay performance of the FLX-1200 is shown. We have exposed a wafer twice without unloading the wafer in between exposures. In the first exposure half of a dense dot array is exposed. In the second exposure the remainder of the dense dot array is exposed. After development the wafer has been inspected using a CD-SEM at 480 locations distributed over an area of 100mm x 100mm. For each SEM image the shift of the pattern written in the first exposure relative to the pattern written in the second exposure is measured. Cross wafer this shift is 7 nm u+3s in X and 5 nm u+3s in Y. The next step is to evaluate the impact of unloading and loading of the wafer in between exposures. At the conference the latest results will be presented.

10144-28, Session PSTue

PS-b-PMMA/ionic liquid blends: a high-χ drop-in replacement for sub-10 nm lithography

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Directed self-assembly (DSA) of block copolymers (BCPs) is a promising candidate to address grand challenges towards new generations of low-cost, high-resolution nanopatterning technology. Over the past decade, poly(styrene-b-methyl methacrylate) (PS-b-PMMA) has been the most popular block copolymer applied in this area. However, further scaling towards pitches below 20 nm is hindered by its relatively low segregation strength between constituent blocks, characterized by a low Flory-Huggins interaction parameter, ? (? for PS-PMMA ~ 0.038 at r.t). To reach sub-10 nm feature dimensions, many high- ? block copolymer materials and processes are currently being studied. For many such systems, moving to processing strategies that are less manufacturing friendly than thermal annealing with a free surface is required, for example solvent vapor annealing or thermal annealing with a top coat. Here we investigate the DSA of PS-b-PMMA with blended ionic liquid (IL) on chemically-patterned substrates via thermal annealing with a free surface. This materials system is attractive because with low volume fraction IL it exhibits a substantially higher –? than the pure block copolymer, yet the change in surface and interfacial properties are manageable by carefully controlling the composition of poly(styrene-random-methyl methacrylate) brushes and the IL loading ratio using thermal annealing at a free surface, thus making PS-b-PMMA/IL may serve as a high-? drop-in replacement for PS-b-PMMA. In this work, we systematically study the orientation control of PS-b-PMMA/IL blends, and assess the thermodynamics and kinetics of its assembly to provide key results to answer two following questions: 1) Can PS-b-PMMA/IL blends offer a solution for sub-10 nm lithography? 2) What is the impact of ? on interfacial width and line-edge roughness by comparing the assembly of PS-b-PMMA without and with IL addition?

10144-29, Session PSTue

Directed self-assembly of single block copolymer lines in graphoepitaxial guiding patterns made by EUV-IL

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We demonstrate the graphoepitaxial alignment of an 11-nm-half-pitch block copolymer in narrow trenches fabricated by extreme ultraviolet interference lithography (EUV-IL).

The International Technology Roadmap for Semiconductors (ITRS) fancies the directed self-assembly of block copolymers as one of the four next-generation lithography (NGL) techniques capable of achieving the required resolution for upcoming logic nodes1. For the use of block copolymers in such patterning applications it is crucial to make use of guiding patterns that induce long-range order in the structures. Most commonly, chemical and topographical guiding patterns are used to induce long-range order. On the way to the implementation of block copolymers in semiconductor industry, the major issues that are meant to be improved are the relatively large defectivity and line-edge roughness of the structures.2

In this work we focus on improving the line-edge roughness of self-assembled block copolymers by very smooth guiding pattern lines. We present EUV-IL3 as a viable way to fabricate parallel, high-resolution, low-line-edge-roughness guiding patterns for the graphoepitaxial directed self-assembly of block copolymers (figure 1 a)). In particular, we demonstrate the defect-free alignment of an 11-nm-half pitch lamellar PS-b-PMMA block copolymer in silica trenches resulting from an HSQ exposure with an aspect ratio AR > 1. The minimal trench width in which we observed alignment is about 35 nm (figure 1 b)). This leads to the formation of one single block in the middle of the trench holding out the prospect of manufacturing very high aspect ratio nanowires of 11 nm width in silicon from considerably wider trenches. Moreover, we show that the deposition of a neutral brush layer allows it to direct the self-assembly of the block copolymers perpendicular to the pattern (figure 2 a) and b)).

When irradiated by extreme ultraviolet light, HSQ is converted in a silica structure that is exclusively wetted by one of the blocks4. This effect gives rise to the alignment of PS-b-PMMA in HSQ-patterns.

Unlike electron beam lithography which is the most commonly used method

to fabricate guiding patterns in research environments, EUV-IL is a parallel fabrication method. This enables fast prototyping on considerable length scales, because dense patterns with lengths exceeding 400 ?m may be obtained at a single exposure step. Such guiding patterns fabricated by EUV-IL are therefore an excellent base to determine the defectivity of self-assembled block copolymers on statistically significant areas. Beyond that, we anticipate that the fabrication of low-line-edge-roughness guiding patterns is a way to improve the line-edge-roughness of the aligned structures.

10144-30, Session PSTue

Rules-based correction strategies setup on sub-micrometer line and space patterns for 200mm wafer scale SmartNILTM process within an integration process flow

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NanoImprint techniques stick out from other more conventional lithography processes (photolithography, electronic lithography, EUV lithography) by virtue of the fundamental mechanisms that create the structures. With conventional approaches the structures are created through a chemical contrast, whereas a topographic one is formed in the case of NanoImprint thanks to the flow of the resist through the stamp's cavities.

In twenty years, consequent technical developments have been achieved to make the technology more mature. Among a plenty of technology alternatives, the UV-based imprint, using transparent stamp, became the standard technology. Two well established options are now available on the market: the full wafer imprint (the size of the stamp correspond to the size of the wafer to be printed) and the step and flash imprint were a small stamp (i.e. die size) is stepped across the wafer to be processed.

If the step and flash technology has demonstrated its capabilities to address the semiconductor markets with high-requirement levels for alignment capability and defectivity density, the full wafer option seems to be the reference for the emerging and growing markets like LED and Photonics based devices having lower defectivity level requirements. Commercially available types of equipment and resists are cornerstones of this technology and some blocs of a full supply chain (design rules, master manufacturing and repair, in-line metrology, integration solutions) need to be established and qualified to make the technology mature enough to rapidly meet the market's needs.

To accelerate this technology adoption, CEA-Leti and EV Group through their joint program INSPIRE, are currently evaluating the benefits of the NIL technology. Much more than an industrial partnership, the INSPIRE program is designed to demonstrate the cost-of-ownership benefits of this technology for a wide range of application domains and to support the NIL technology take-off :

• by supporting the development of new applications;

• from the feasibility-study stage to the first manufacturing steps;

• by transferring integrated process solutions to their industrial partners, lowering significantly therefore the entry barrier for adoption of NIL for manufacturing novel products.

One of the results obtained within this program so far and detailed in this paper are related to the study of the Critical Dimension Uniformity evolution along the process, and we demonstrated, from quantitative and statistical data, how tiny CD drifts could be monitored after 100 cumulative imprints made with a single soft stamp.

This paper will present also a strategy plan for design corrections adapted to the SmartNILTM process implemented on the HERCULES®NIL equipment with respect to the process conditions, and based on Critical Dimension (CD) uniformity assessment. The work brings focus on sub-micrometer resolution features. SEM characterizations of printed patterns were performed over dedicated points on the master to obtain reference measurements. The as-imprinted and etched wafers were then measured. Repeatability tests were performed over 50 wafers to collect statistics and the CD distribution within a wafer and also wafer to wafer. From the data we are able to derive rules-based correction tables for lines pattern.

10144-31, Session PSTue

Patterning of polymer nanogratings with molecular orientation and characterization with polarized resonant critical dimension small angle x-ray scattering

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Critical dimension small angle X-ray scattering (CDSAXS) is a recently developed variable angle transmission scattering technique that has been shown to be capable of characterizing the three-dimensional shape of periodic nanostructures, such as memory arrays and the buried interfaces of directed self-assembled block copolymer (DSA BCP) lamellae [1]. Information about the structures is extracted by fitting simulated scattering patterns to the experimental ones using an inverse iterative algorithm. In the case of polymer structures, conducting CDSAXS at resonant energies with soft X-rays can enhance the scattering contrast, but also causes the scattering to be influenced by any preferential orientation of the transition dipole moment that is being probed, and thus the preferential molecular orientation.

In this work, to assess how preferential molecular orientation can influence CDSAXS scattering, we fabricate model systems of nanogratings of the polymers PBTTT and P(NDI2OD-T2) with 140 nm pitch using nanoimprint lithography and replica molding. These polymers were selected because they have aromatic rings in their backbones whose orientation can be probed separately from that of the side chains, and whose backbones are known strongly orient. Nanoimprint lithography on thin films oriented as a result of blade-coating results in nanogratings with strong biaxial anisotropy but is challenging with these polymers, which have a high glass transition temperature. Replica molding, which involves putting a soft stamp onto a small volume of polymer solution, does not have temperature restrictions but results in weaker biaxial anisotropy.

We then conduct CDSAXS at the carbon 1s-pi* transition energies with different angles and polarizations and fit the periodic shape of the nanogratings and the orientation of the aromatic rings in the backbones of the polymers. We also use spectroscopic ellipsometry on these samples to aid in fitting the shape and molecular orientation. Finally, we simulate the CDSAXS scattering of DSA BCP lamellae with varying strengths of preferential molecular orientation at the interfaces between domains. By learning more about the influence of polymer orientation on CDSAXS measurements, we hope to more accurately fit DSA BCP lamellae in the future and continue to improve the utility of CDSAXS.

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10144-32, Session PSTue

RLT uniformity improvement utilizing multi-scale NIL process simulation

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1. INTRODUCTION

Technologies for pattern fabrication using nanoimprint lithography (NIL) process are being developed targeting for various devices. Nanoimprint lithography is attractive candidate for its clear pattern transfer characteristics of mold contact patterning with fewer process steps comparing multi-patterning, and so the effect of greatly shortened TAT. To make finer device pattern with NIL, controlling of the residual layer thickness uniformity (RLTU) is the key factor to achieve CDU. RLTU is affected by mainly several factors, and among them, resist drop placement refinement is effective to correct local RLT variation. To optimize resist drop placement, iterative NIL process and measurement is time-consuming, so automated RLT hot-spot prediction and refinement utilizing NIL simulation is needed 1-6).

2. RESIST DROP PLACEMENT

Using jet and flush NIL process, resist drops are dispensed by ink-jet nozzle according to drop placement recipe, which is calculated as follows: considering pattern layout, template cavity depth, outer shape of the chip and other factors, the required resist volume for each local area is calculated, and then the drop number and the position are determined to fulfill the volume. On the substrate, resist drops spread merging each other, filling into the cavity of the template. The resist spreading behavior depends on resist physical properties, template imprinting sequence, pattern layout and depth. After imprinting, UV cure and de-molding, RLTU is measured using optical scatterometry (OCD).

3. NIL PROCESS SIMULATIONS

The template bowing behavior through the imprinting process observed using spread camera, and analyzed by structural simulation. Resist flowing behavior on substrate is calculated using fluid simulation. In the simulation, the issue is that the resist flow behavior specific in the space of the nanometer scale must be considered, but detailed mechanism is unclear. In the smaller sized space under 100 nm, the effect of surface tension of the resist is increased. In addition, in the thinner RLT conditions than 10nm, resist viscosity is observed to increase. To elucidate the mechanism, detailed measurement of resist behavior and characteristics in the finer space is necessary.

4. RLTU IMPROVEMENT UTILIZING NIL SIMULATIONS

An example of NIL compliance check flow is proposed in figure 1. Layout is analyzed with design rule checker (DRC), and hotspot candidate is extracted. And then, each hotspot is examined with NIL process simulation. Critical hotspots are modified in design or process, so NIL friendly design data is provided. For RLTU improvement, RLT hotspot is extracted using NIL simulator, and resist drop arrangement is refined according to the simulation result (Figure 2). Resist un-filling issue is also analyzed and modified simultaneously. In this way, nominal RLTU is achieved without iterative imprinting and measurement. The detailed result will be shown in the presentation.

10144-33, Session PSTue

DSA process window extension via controlled atmospheric conditions through accurate defectivity and roughness measurements

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Directed Self-Assembly (DSA) is today an attractive and credible alternative lithographic technology for semiconductor industry. In the coming years, DSA integration could be a standard complementary step with other lithographic techniques (193nm immersion, e-beam, extreme ultraviolet). The potential of DSA must next be confirmed viable for high volume manufacturing. Developments are especially necessary to transfer this technology on 300mm wafers in order to demonstrate semiconductor fab-compatibility. Key challenges concern block copolymers (BCPs) self-assembly quality (defectivity, roughness, period stability), the DSA process stability and processing times compatible with industrial throughput constraints.

In this paper we highlight the interest of self-assembly annealing step of BCPs under controlled atmospheric conditions. The study is focused on polystyrene-block-poly(methyl methacrylate) (PS-b-PMMA) BCPs materials processed on a new designed annealing chamber, allowing to tune atmospheric conditions, developed on 300mm SOKUDO DUO DSA dedicated track. BCP self-assembly quality (defectivity, roughness, period stability) is particularly investigated and accurately evaluated through dedicated CDSEM images treatment software. Fingerprint DSA configuration is preliminary used as a test vehicle to clearly demonstrate atmospheric conditions effects and understand related chemical and physical mechanisms. BCP defectivity, roughness and natural period are finely extracted through statistics measurements on 300mm-wafers. Thanks to these output parameters we clearly demonstrate the usefulness of efficient metrology for DSA process optimization. We show that with optimized atmospheric annealing conditions DSA process window is improved. This DSA process window extension allows especially to reach self-assembly thermal budgets providing lower defects levels than standard used annealing chambers. Shorter times with low defectivity processes are particularly highlighted. Besides defectivity, BCP period stability appears as a key to control commensurability matters for grapho-epitaxy and chemo-epitaxy DSA processes. Atmospheric conditions effects on lamellar and cylindrical BCP morphologies will be presented as well as first trends on grapho-epitaxy DSA process.

10144-34, Session PSTue

DSA materials in-film defectivity advanced investigation

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Directed Self-Assembly (DSA) is today an attractive and credible alternative lithographic technology for semiconductor industry. In the coming years, DSA integration could be a standard complementary approach with other lithographic techniques (193nm immersion, e-beam, extreme ultraviolet). DSA technology must now be confirmed viable for high volume manufacturing. For that continuous developments are necessary to transfer this technology on 300mm wafers in order to demonstrate semiconductor fab-compatibility. One of the main key challenges concerns the defectivity where the detection limits have to be adapted to the targeted technology nodes.

This paper is focused on the investigation of in-film defectivity for DSA materials using KLA SP5 Inspection tool. 300mm-unpatterned silicon wafers spin-coated with PS-PMMA based DSA materials are used as test vehicles. Various DSA configuration are investigated such as only block copolymers (BCP), only neutral layer (NL) and fingerprint configuration with NL/BCP stack. Different process conditions are varied such as film thickness and temperature in order to benchmark the process conditions to maximize the

defect detection. The defectivity contribution of the different materials is as well evaluated. Thus we demonstrate that sensitivity is improving when film thickness increasing. SP5 film thickness utility also predicts optimal thickness for best sensitivity. Moreover for the best configuration the sensitivity limit is push down to 30 nm.

10144-35, Session PSTue

The use of thermal scanning probe lithography for the directed self-assembly of block copolymers

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Lithography based on the use of self-assembled block copolymers has gathered considerable attention in the last couple of years. In this approach block copolymer patterns are used as etching masks for micro- and nanofabrication processes. Guiding patterns are used to control the orientation of block copolymer domains. The fabrication of high-resolution guiding patterns is necessary for the alignment of small-pitch block copolymers. For the industrially interesting chemoepitaxy approach it is necessary to achieve guiding patterns with minimum widths approximately corresponding to the structure size of the block copolymer half-pitch [1]. For investigations at the laboratory scale and at the initial states of process development, e-beam lithography is the most frequently used method to fabricate these patterns. Due to the proximity effect, e-beam lithography suffers from resolution limitations for the fabrication of high-density and high-resolution guiding patterns. This limitation is going to be critical for the investigation of the chemical epitaxy process of new high-χ materials, where guiding patterns with a sub-10 nm accuracy will be required. We present thermal scanning probe lithography as a viable alternative to e-beam lithography for the fabrication of guiding patterns for an 11-nm-half-pitch lamellar PS-b-PMMA block copolymer. Thermal scanning probe lithography (t-SPL) relies on the evaporation of a polymeric resist when getting in contact with a resistively heated atomic force microscopy tip [2]. Thanks to extremely sharp tips in combination with resist evaporation triggered by a tip-sample contact of microsecond duration, the technique provides high resolution capability and throughput [3]. A possible application of this technique is the 3-D patterning of polymer samples [2]. In this work, we apply t-SPL to achieve the fabrication of 10 nm wide lines with a period multiplication factor of two with respect to the periodicity of the block copolymer. We demonstrate defect free alignment of the block copolymer on the μm2-scale.

Figure 1 shows the overall process consisting of a patterning step using a resist thickness of only 3.5 nm and subsequent oxygen plasma functionalization of an underlying neutral PS-r-PMMA brush followed by the directed self-assembly. Figure 2 shows the resulting 10 nm line pattern and the structure transferred to the brush. In the course of this activation step we observe swelling of the brush layer (see figure 2 b)). This effect may be due to the attachment of functional groups that are responsible for the chemical modification of the exposed areas. The finally achieved block copolymer patterns are depicted in figure 3. In particular, the difference in degree of order of the block copolymers between the patterned and the non-patterned area proves the capability of the patterns to direct the self-assembly of block copolymers (see figure 3 a)). The defect free self-assembly is depicted in an AFM tapping mode image in figure 3 b).

Based on our results we consider t-SPL to be a suitable method for upcoming challenging research activities in the field of chemoepitaxy. The high accuracy and resolution in all three spatial directions makes us believe that t-SPL will play a decisive role in the fabrication of guiding patterns for sub-10 nm block copolymers.

10144-36, Session PSTue

The 300mm evaluation of a 38nm period lamellar PS-b-PMMA for L/S applications with graphoepitaxy

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Directed Self Assembly (DSA) of block-copolymers (BCPs) used as a complementary technique to the 193nm immersion lithography as demonstrated sub-10nm node applications in both via [1] and line/space patterning [2]. In recent years the chemoepitaxy approach as generated a great interest in DSA of PS-b-PMMA diblock copolymer with extensive patterning and etching results [3,4]. We propose however to study the performance of graphoepitaxy which allows DSA with thicker initial BCP layer, higher multiplication factors and stronger orientation control of lamellae. The aim of this work is to use the 300mm pilot line available at LETI and Arkema's advanced materials [5] to evaluate the performances of a standard graphoepitaxy process of a 38nm period lamellar PS-b-PMMA (L38) reported before [6].

Values of CD, roughness and defectivity of PMMA lines are extracted offline from a 300mm statistical CDSEM review (figure 1) and can be used to draw out the process window, function of the CDguide, of this graphoepitaxy process. Interestingly each data behave in an overlapping, discrete "potential well" fashion with clear minima at commensurate CDguide as depicted in figure 2. At these minima, for both a multiplication factor of 4 and 5 lines, we report a mean CD of PMMA lines of 11nm (3=0.9nm), a LWR around 1.9nm (3) and a LER around 3nm (3) after PSD treatment. This is a major improvement over the initial pattern mean LWR evaluated at 5nm after PSD. Regarding defectivity, a 0.009/μm^2 defect rate is obtained for a multiplication factor of 4 lines. Interestingly this is not the case for the multiplication of 5 lines yet (defect rate at 0.19/ μm^2), indicating that further optimization of thermal budget might be needed.

This methodology will thus be applied from now on to determine an optimum DSA process parameters as well as to further illustrate the ability of the BCP to accommodate and improve on a deliberately implemented roughness variation of guiding patterns. Additionally, a novel methodology to finely tune the surface energy of the topographic gratings will be introduced as a solution to improve on the roughness and defectivity performances obtained so far.

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10144-37, Session PSTue

The opportunity and challenge of spin coat based nanoimprint lithography

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Since multi patterning with spacer was introduced in NAND flash memory, multi patterning with spacer has been a promising solution to overcome the resolution limit in most of devices including NAND, DRAM, and logic. However, the increase in costs of multi patterning with spacer would be a serious burden on device manufacturers as the minimum dimensions are getting smaller. Even though Nanoimprint Lithography(NIL) has been considered as a strong candidate in order to avoid cost issue of multi patterning with spacer, there are still negative viewpoints such as template damage from particles between template and wafer, low throughput compared with other candidates, and overlay degradation from stress between template and wafer. Of course, many critical issues of NIL have been dramatically improved for recent several years, but more progress must be made especially in template damage. Particles on wafer must be strictly excluded prior to imprinting, because some particles may cause a significant damage on template. For this reason, added particles within NIL tool have been reduced with persistent effort, and are expected to be controlled within our target in near future. But, particles come from not only NIL tool but also other sources which may be some process steps in mass production. To make things worse, if particles are smaller than the sensitivity of defect inspection tool, it would be very difficult to protect template from tiny particles. Fortunately, our eventual aim is that fine patterns on template must be protected from tiny particles, not that tiny particles must be removed. Therefore, we expect that template can be protected from tiny particles by preventing the contact between template and particles with thick resist. Even though Jet and Flash Imprint Lithography(J-FIL) is known as a novel method for high volume manufacturing, it is very hard to increase resist thickness to the sufficient level without side effects. Instead of dispensing resist droplets, spin coating can be considered to increase resist thickness. By changing resist deposition method from jetting to spin coating in J-FIL, additional improvements in throughput and overlay as well as template damage can be achieved. J-FIL typically consists of 5 main steps: dispensing resist droplets on wafer, lowering template to wafer, resist droplet's spreading along the gap between template and wafer, UV curing, and separation of template from wafer. If we replace dispensing resist droplets at NIL tool with spin coating at spin coater, we can skip dispensing resist droplets and minimize spreading time, thereby achieving improvement in throughput. While wafer stage moves for wafer alignment, there must be some stress between template and wafer which eventually induces overlay degradation within field. Because the stress between template and wafer decreases as resist thickness increases, overlay degradation can be expected to be suppressed as resist thickness increases. Spin-coat-based NIL has a problem such as pattern collapse. Even though only hole patterns can be realized with spin-coat-based NIL in current circumstances, pattern collapse is expected to be overcome through the improvement of resist property.

10144-38, Session PSTue

Inspection and fabrication of nano-imprint stamp using electron and ion dual beam system

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Nano-imprint lithography (NIL) is an emerging high-resolution parallel patterning method, mainly aimed towards fields in which high-end photolithography methods are costly and do not provide sufficient resolution at reasonable throughput. In a top-down approach, a surface pattern of a stamp is replicated into a material by mechanical contact and it is a simple nanolithography process with low cost, high throughput and high resolution. High resolution stamp patterning can currently be performed by electron beam lithography; however at the smallest resolution, the thickness of e-beam resist used for electron beam lithography is very thin and it is hard to get a high aspect ratio pattern by using dry etching for pattern transfer. As a result, such an approach has been that employs electron-beam-assisted deposition to form pattern-transfer hard mask in a direct-write deposit, it is a resistless process can improve the limitation of dry etching selectivity of resist thickness. By scanning the focused electron beam while injecting a suitable organometallic precursor gas around the location of e-beam and just above the substrate, a high-density and high-uniformity hard mask for subsequent etching without use proximity-effect correction techniques. Furthermore, this technique can also directly deposit a metal pattern for interconnect or a dielectric pattern on NIL stamp without the need for separate metal or dielectric deposition, photoresist etch-mask, and etching processes. This approach simplifies the hard-mask creation or even metal or dielectric pattern creation process modules from five or ten of steps to only a single step for NIL stamp fabrication. Therefore, it saves both stamp making and further processing costs. Electron beam assisted deposition to form pattern-transfer hard mask for NIL stamp with gate and interconnection pattern. And focus ion beam can be used direct etch contact and via hole pattern with high aspect ratio on NIL stamp. Helios Nano Lab™ 1200 and Nova Nano Lab™ 600 dual beam system are used in this work for NIL stamp inspection and fabrication. Obduct Eitre® 6 nano-imprint system is used for pattern transfer. Detail process procedure and results will be presented in the SPIE Advanced Lithography 2017 conference.

10144-39, Session PSTue

Model-based guiding pattern synthesis for on-target and robust assembly of via and contact layers using DSA

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DSA has been shown to be a compelling technology for printing the dense-pitched and low critical-dimension (CD) via/contact layer. The graphoepitaxy process investigated here is compatible with traditional MP processes and is amenable to hybrid DSA-MP techniques. The pitch multiplication property of DSA enables the printing of dense contact patterns below the resolvable lithographic pitch using the appropriate molecular composition of two block copolymers and by selecting the correct shapes for the guiding patterns (GP). Since the chemical composition of the diblock copolymer is invariant in a specific DSA process, the accurate synthesis of GPs has now become the key bottleneck in the robust assembly of contacts to accurately match the placement of target contact shapes.

Any method attempting to optimize the shape of a GP for accurate contact assembly needs to have the means to accurately predict the locations of assembled contact shapes given a GP as input. Since it is not practical to embed a full-physics DSA simulator directly into GP synthesis due to its prohibitive runtime, we need to ensure that our GP synthesis framework has the ability to plug-in any compact DSA model which is accurately calibrated against such a DSA simulator or experimental data with significantly faster runtime to enable full-chip simulations. In addition to accurately predicting assembly locations, any compact DSA model that has been integrated into our GP synthesis framework should also be able to evaluate the robustness of an input GP in regards to phase transition characteristics, in other words, there must be a metric to determine not only error placement but also how far a given guiding pattern is from experiencing phase transition, which in this case we define as not achieving the target cylinders. The key contributions of this paper are as follows:

1. We propose the first model-based full-chip GP synthesis framework and optimization algorithm which targets two key objectives for on-target and robust DSA:

a. minimizing placement error (PE) between drawn target and assembled contact shapes;

b. minimizing the sensitivity of placement under guiding pattern variations induced by process fluctuations.

2. We describe an overall mask synthesis flow for DSA which includes DSA compliant contact grouping, GP synthesis, GP mask synthesis and RET, and a verification step that ensures the post-RET printed GPs will still assemble the contacts at the required locations and with the required shapes.

3. We define the characteristics that a DSA compact model should have to satisfy the requirements of a GP synthesis framework. We illustrate the quality of results using a specific calibrated compact model.

4. We define the metric of `Total Interaction Energy' (TIE) that is used to characterize the robustness of a GP in regards to contact phase transformation and shape degradation. We find that with lower TIE the robustness of the GP improves.

We will first describe the overall DSA mask synthesis flow and compact model calibration methodology followed by a formulation of the GP synthesis problem and constraints and describe our GP synthesis algorithm. Next we will provide data based on our compact and Monte Carlo models demonstrating the robust assembly of arbitrary contact patterns by running detailed DSA simulations on our synthesized GPs. We will also provide an independent verification flow which will demonstrate that the post RET printed images of our synthesized GPs will still maintain compliance of assembled contact patterns.

10144-40, Session PSTue

Anti-spacer formation of self-aligned vias for mitigation of edge placement error

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Feature scaling for the 7nm technology node has presented significant challenges in achieving overlay and edge placement error (EPE) requirements for critical back end of line (BEOL) via patterning. Traditional 193nm immersion (193i) lithography-plasma etch (LEx) solutions require multiple memorization processes to deliver the required via density. This increases process variability and cost through additional masks and process steps required. Extreme ultraviolet lithography (EUV) is an alternative to LEx processing, but EUV faces substantial challenges in production readiness. This has prompted the need for additional via patterning solutions.

Anti-spacer technology (AST) can provide an alternative approach for via formation. Utilization of a cross contact, dual damascene process provides via self-alignment in both X and Y directions. EPE is a function of critical dimension (CD), critical dimension uniformity (CDU), line edge and width roughness (LER, LWR). AST process improves EPE window with via memorization occurring at the same plasma etch step, reducing CD variation. CDU and edge roughness are improved with the use of ALD films. Integration of AST via process presents new challenges, namely organic film planarization and plasma etch process selectivity, which must be addressed.

This paper will highlight the overlay improvement provided by AST via patterning. A summary of tool selection, integration challenges, film stack and etch chemistry optimization will be shown to achieve the 7nm technology node targets. AST via will be benchmarked against 193i LEx and EUV patterned vias. With EPE being of paramount importance to 7nm and beyond technology, AST via patterning can provide a unique advantage.

10144-41, Session PSTue

Nanofabrication and process development of dense sub-5nm structures over large areas

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The patterning and transfer of ultra-small features in the nanometer scale on a wide variety of substrate materials have become an important area of research in recent years [1]. The main driver of this field has been the micro- and nano-electronics industry where the transistors keep diminishing in size as predicted by Moore's law [2], although there are signs of this trend slowing down [3]. Nevertheless, this trend has also benefited other scientific and technological areas involving the fabrication of 'nano-devices' for a wide range of applications in sectors such as bio-medical, environment, energy, communications [4] and sensing [5]. As a result, the process development of the patterning and transfer of sub-10 nm or smaller features have become very critical to ensure the realization of nano-scale devices in many scientific and technological areas. In this report, the electron beam lithography process development of sub-5 nm lines on 20 nm thick Hydrogen Silsesquioxane (HSQ) resist is investigated using a 100 kV electron beam acceleration voltage. Previous reports [6-9] involved the process development of isolated and larger line-widths over smaller exposed areas and using different process parameters. The exposed patterns are developed using varying developer temperatures with ultrasonic sample agitation that shows to provide significant improvement on pattern resolution. In addition, lift-off processes are developed and optimized to transfer the patterns on silicon substrates. The influence of several process parameters such as development temperature, exposure current, exposure dose, pattern density and pitch on the line-width is also investigated. Lines with lateral width of 3 nm on a 100 nm pitch over exposed areas as larger as 500 microns x 500 microns have been successfully exposed and the pattern transfer of the periodic lines, bent lines, and nano-pillars on Chromium layer using lift-off have been demonstrated. To the best of the authors' knowledge, the 3 nm dense lines produced are the narrowest line-width exposed using the specific process conditions reported in this work. The process reported to fabricate sub-5 nm lines in this work would be useful in the fabrication of a wide range of nanostructures and devices such a X-ray zone plates, optical slot-waveguides, graphene-base electronic devices and plasmonic devices.

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10144-23, Session 6

Advanced surface affinity control for DSA contact hole shrink application

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DSA patterning is a promising solution for advanced lithography as a complementary technique to standard and future lithographic technologies1 (ArF immersion lithography, multiple e-beam and extreme ultraviolet). Over the past years, important effort related to material development and process optimization enabled major improvements regarding the critical dimension uniformity (CDU), the placement error (PE), the self-assembly defectivity and throughput2,3 (i.e., short bake time). Nevertheless, among the DSA patterning key issues, defect density is still identified as the major challenge for DSA integration since the state of the art values remain at least one to two orders of magnitude higher than the industrial specifications.

One of the most advanced DSA integration process is the contact hole shrink by graphoepitaxy. This well-known approach is suitable for arbitrary pattern generation. Moreover, the pattern-density-related defects encountered (i.e., template filling issues) could be overcome by employing the "DSA Planarization" process developed at CEA-LETI4. Furthermore, by using advanced surface affinity control conjointly with optimized DSA materials, the defectivity level could still be decreased to reach the expected manufacturing performance.

In this work, we focused on the DSA graphoepitaxy process flow dedicated for contact hole applications using polystyrene-b-poly(methyl methacrylate) (PS-b-PMMA) block copolymers. We specifically investigated the selective surface affinity control of a guiding pattern design by ArF immersion lithography in order to achieve better performances on CEA-LETI DSA dedicated 300 mm pilot line. The objective was to control and reduce the residue at the bottom of the cavities by controlling separately the surface affinity of the wall and of the bottom of the guiding pattern cavities. Indeed the controlled of this residue is critical for subsequent DSA pattern transfer into the underlayers. For this purpose, the DSA performances were evaluated as a function of the template surface affinity properties, by using both surface modification and alternative process integration. The surface affinities (wall and bottom) were customized to enhance DSA performances for a PS-b-PMMA block copolymer of intrinsic period 35 nm (cylindrical morphology) by monitoring main key manufacturing parameters: defectivity, CDU and PE. FIB-STEM analyses were conjointly carried out on the optimized wafers to analyze the residual polymer thickness after PMMA removal. The best DSA process performances (100% hole open yield, CDU-3σ = 2.5 nm and PE-3σ = 1.2 nm) were achieved with a reduced polymer residue around 7 nm (cf. figure 1). It was witnessed that the surface affinity control of the guiding pattern is crucial to reduce the residual layer at the bottom of the template. In addition, the DSA-related defectivity monitoring by review-SEM enabled us to optimize the integration process in order to achieve a defect free surface superior to 10000 μm^2 (see figure 2). This result represents more than 6x105 contacts, attesting the progress achieved over the last years and witnessing the maturity of the DSA in the case of CH application.

10144-24, Session 6

Optimization of in-cell DSA performance and out-cell morphology orientation control of the SMARTTM flow

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Directed self-assembly (DSA) of block copolymer (BCP) has been witnessing remarkable progress contributed by the efforts of academia, consortia and the industry for the last five years. DSA technology is now a leading alternative patterning method which has high potential to be accepted by semiconductor industry for N7 and beyond IC chip fabrications. Among the DSA process flows reported thus far, SMARTTM was developed by EMD Performance Materials Corp (EMD). Since its introduction in 2013 [1], SMARTTM flow has attracted extensive studies on its basic performance stability [1, 2], LER/LWR [3-5], pattern etching transfer [3, 4], placement error [6], and defectivity [4-5]. Full 12" wafer SMARTTM DSA patterns with CDU < 0.5nm (3 sigma) [5] and LER < 2nm [4] were achieved, which are comparable to pattern quality generated via multiple patterning process. However, all aforementioned investigations on SMARTTM are primarily focused on its intrinsic DSA performances. For a typical chemoepitaxy DSA flow like SMARTTM [1] and LiNe [7, 8], the last material processing step is the coating and annealing of BCP material. Therefore, BCP film covers entire wafer surface. After BCP annealing, DSA patterns appear in areas where proper pre-patterns were prepared (in-cell). Outside of those areas (out-cell), BCP self-assembly patterns will be formed. For lamellae BCP which is designed for line/space applications, fingerprint pattern with perpendicular morphology orientation or parallel morphology orientation with island and hole defects can be formed in out-cell areas. These out of cell undesired patterns will be transferred into underlying substrates during DSA pattern etch transfer processes complicating integration process and possibly increasing DSA process costs. Good control of the out-cell BCP morphology to be perfectly parallel oriented with respect to the substrate surface without island and hole defects is highly desired. This communication will describe co-optimizations of materials and process to reach well balanced performances of in-cell DSA and out-cell morphology orientation control via SMARTTM flow.

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10144-25, Session 6

Pattern defect reduction and LER improvement of chemo-epitaxy DSA process

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Directed self-assembly (DSA) is one of the candidates for next generation lithography. Over the past few years, many papers and presentation have been reported regarding DSA, and Tokyo Electron Limited (TEL is a registered trademark or a trademark of Tokyo Electron Limited in Japan and /or other countries.) also has presented the evaluation results and the advantages of each1-6.

By some theoretical analysis, it is understand that the pattern defects related with phase separation phenomenon are very rare because of the big free energy gap between with and without defects. However, many defects are observed on actual DSA patterns. One of the possible causes is that the system is not reached well to the equilibrium state. Therefore, the kinetic types of defect are remained. In this case, higher anneal temperature or longer anneal time may remove the defects faster. Other possibility generate defects, especially single bridge type of defect, may be related with the thermal fluctuation. In case of low chi number of BCP (block co-polymer), for example PS-b-PMMA (poly styrene – poly methyl methacrylate), interfacial length between two domains is relatively wide, therefore, the risk of bridge type of defect is existed especially with high temperature anneal condition. In this case, optimizing the quench step may reduce the risk. On the other hand, many type of defect observed on actual DSA patterns are related with chemical and physical guide errors. For example, guide pitch

and pin width not matched with BCP original pitch, BCP thickness, not optimized surface affinity at neutral and PS or PMMA pin area, and defects of guide patterns. If those conditions are prepared for DSA process, many types of defects will be generated and it is very difficult to remove them even by longer or higher anneal conditions because the equilibrium state is changed by them. Especially, chemical epitaxy process has many steps to prepare the chemical guide for BCP, therefore, each step have to be carefully optimized to remove the defect causes.

In this report, we will report the latest defect number of DSA pattern and which process step generate the defects by experimental and simulated results.

Another challenge of DSA patterns is how to improve the Line Edge Roughness (LER). In general, LER of DSA lines are related with the interfacial length between two domains. In case of PS-b-PMMA, the length is predicted 3nm, and, approximately 2~2.5nm LER is observed by experimentation. On the other hand, high volume manufacturing request for LER is going smaller, <2nm. Therefore, the LER have to be improved from original LER number generated by BCP own. One of the possible methods is improving the LER during the etch transfer step. Now, we are investigating the many types of etching condition and comparing the LER.

10144-26, Session 7

Wide-range directed self-assembly lithography enabling wider range of applicable pattern size for both hexagonal multi-hole and line/space

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1. INTRODUCTION

To make various pattern sizes on hexagonal multi-hole layout and on line/space layout for semiconductor device applications, two cost-effective lithography technologies (conventional immersion lithography and directed self-assembly lithography (DSA) [1][2]) are tried. In the case of conventional immersion lithography, it is difficult to make small patterns (CD of less than 60nm, pitch of less than 100nm) without any double patterning technology under small size-variation condition because of optical resolution limit. On the other hand, in the case of DSA, it is really difficult to make not only smaller patterns (CD of less than 15nm, pitch of less than 30nm) because of self-assembling limit which depends on block copolymer material but also middle patterns (CD of more than 40nm, pitch of more than 70nm) because of synthesis issues of block copolymer having large molecular weight and elongation of annealing process time for phase separation. This paper describes wide-range directed self-assembly lithography (WDSA) which enables not only narrow but also wide patterns. Small holes (CD of 10nm, pitch of 20nm) and wide holes (CD of 50nm, pitch of 100nm) are obtained as hexagonal multi-hole patterns using newly developed block copolymer which supports wide-range size. Also sub-15nm line/space pattern having half-pitch (hp) of 12nm is confirmed and selective metalizing process is applied to improve dry etching stability with WDSA.

2. WIDE-RANGE DIRECTED SELF-ASSEMBLY LITHOGRAPHY (WDSA)

Applicable range of patterning pitch size of three lithography technologies (conventional immersion lithography, DSA and WDSA) is evaluated. Conventional immersion can support wider pitch of over 100nm and DSA covers pitch from 30nm to 60nm. It is found that the applicable range which can be patterned by DSA is extremely narrow. On the other hand, WDSA can apply wider range from a pitch of less than 10nm to that of more than 100nm. Main technical point of WDSA is new concept of block copolymer material. The block copolymer for realizing WDSA has a new molecular structure which enables wider range of pitch for phase separation by shorter annealing process time and it can be made with higher molecular weight by easy synthesis process. WDSA process is exactly same as DSA process. The new block copolymer for WDSA is coated on a normal substrate having a guide pattern. Self-assembling pattern is made through annealing process and development process. SEM pictures of hexagonal multi-holes by WDSA are shown. CD from 10nm to 50nm and pitch from 20nm to 100nm were successfully patterned. This results show WDSA can cover wider range than conventional immersion and DSA.

3. METALIZING PROCESS

One technical issue of DSA is dry etching resistance because of poor etching stability of DSA material. One block of the new block copolymer for WDSA is easily metalized by infiltration synthesis process and its metal content percentage becomes higher than that of conventional DSA. SEM pictures of hp12nm L/S pattern created by self-assembling on both of before metalized and after metalized through RIE process are shown. The results show dry etching resistance was markedly improved by metalizing process.

4. CONCLUSION

Wide–range directed self-assembly (WDSA) using a new block copolymer can support wider patterning range than conventional lithography technologies and CD from 10nm to 50nm and pitch from 20nm to 100nm were successfully patterned. It is also confirmed that dry etching resistance was markedly improved by metalizing process.

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10144-27, Session 7

Extremely broad processing window for directed self-assembly of block copolymer films on atomically-thin graphene chemical patterns

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Directed self-assembly of block copolymers is a scalable method to fabricate well-ordered patterns over the wafer scale with feature sizes below the resolution of conventional lithography. Typically, lithographically-defined prepatterns with varying chemical contrast are used to rationally guide the assembly of block copolymers. The directed self-assembly to obtain accurate registration and alignment is largely influenced by the assembly kinetics. Furthermore, a considerably broad processing window is favored for industrial manufacturing. Using an atomically-thin layer of graphene on germanium, after two simple processing steps, we create a novel chemical pattern to direct the assembly of polystyrene-block-poly(methyl methacrylate). Continuous monolayer graphene films are grown directly on germanium wafers via CVD or can be transferred from metal surface to arbitrary substrates. The wetting behavior of the block copolymer domains on graphene and germanium is further verified with a hole/island experiment. At 190°C, PS has lower surface energy than PMMA, so it is energetically favored to wet the free surface. Thus, from the morphology of the self-assembled films, the surface affinity of graphene and germanium toward each block copolymer domain can be determined. We observed that the graphene surface is preferential to PS domains, while the germanium surface is slightly preferential to PMMA domains after brief plasma treatment. This new chemical pattern allows for assembly on a wide range of guiding periods and along designed 90° bending structures. Faster assembly kinetics has been observed on graphene/germanium chemical patterns than on conventional chemical patterns based on polymer mats and brushes. We also achieve density multiplication by a factor of 12 (not limited to), greatly enhancing the pattern resolution. These templates offer an exciting alternative to traditional chemical patterns composed of polymer mats and brushes, as they provide faster assembly kinetics and broaden the processing window, while also offering an inert, mechanically and chemically robust, and uniform template with well-defined and sharp material interface.

Recently we have down scaled the fast assembly to sub-7nm features from newly synthesized triblock copolymers with both thermal annealing and solvent annealing. The direct synthesis of the graphene chemical pattern on a target substrate is desirable for wafer-scale assembly of block copolymers because (1) CVD is an inherently scalable process, yielding uniform continuous graphene films over large areas that are only limited in extent by the size of the substrate or the size of the reaction chamber, and (2) direct growth yields relatively pristine graphene films, providing a clean, highly reproducible template on which to conduct directed assembly. Chemical contrast may be alternatively patterned by exposing the sample to chemical or plasma treatment, by forming a self-assembled monolayer, or by depositing a second two-dimensional atomic layer (e.g. by lateral growth, van der Waals epitaxy, or stacking). These graphene-based chemical patterns may enable the directed self-assembly of ultranarrow block copolymer domains for manufacturing of high resolution features, both in the semiconductor electronics industry and in high density magnetic media. This work also opens the door for directed assembly studies on chemical patterns based on the large library of two-dimensional materials.

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10145-1, Session 1

Advancing measurement science at NIST to enable atom-scale technology *(Keynote Presentation)*

Richard M. Silver, National Institute of Standards and Technology (United States)

No Abstract Available

10145-2, Session 1

Metrology challenges for in-line process control *(Keynote Presentation)*

Philippe Leray, IMEC (Belgium)

No Abstract Available

10145-3, Session 2

Electrical test prediction using hybrid metrology and machine learning

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Electrical test measurement in the back-end of line (BEOL) is crucial for wafer and die sorting as well as comparing intended process splits. Any in-line, nondestructive technique in the process flow to accurately predict these measurements can significantly improve mean-time-to-detect (MTTD) of defects and improve cycle times for yield and process learning. Measuring after BEOL metallization is commonly done for process control and learning, particularly with scatterometry (also called OCD (optical critical dimension)), which can solve for multiple profile parameters such as metal line height or sidewall angle and does so within patterned regions. This gives scatterometry an advantage over inline microscopy-based techniques, which provide top-down information, since such techniques can be insensitive to sidewall variations hidden under the metal fill of the trench. But when faced with correlation to electrical test measurements that are specific to the BEOL processing, both techniques face the additional challenge of sampling. Microscopy-based techniques are sampling-limited by their small probe size, while scatterometry is traditionally limited (for microprocessors) to scribe targets that mimic device groundrules but are not necessarily designed to be electrically testable.

A solution to this sampling challenge lies in a fast reference-based machine learning capability that allows for OCD measurement directly on the electrically-testable structures, even when they are not OCD-compatible, as well as the standard OCD targets in the scribe. By incorporating such direct OCD measurements, correlation to, and therefore prediction of, resistance of BEOL electrical test structures is significantly improved. Improvements in prediction capability for multiple types of in-die electrically-testable device structures is demonstrated. To further improve the quality of the prediction to the electrical resistance measurements, hybrid metrology using the OCD measurements as well as X-ray metrology (XPS and XRF) is used. Hybrid metrology is the practice of combining measurements from multiple equipment types in order to enable or improve the measurement of one or more critical parameters. Here, the XPS and XRF measurements are used to detect and quantify barrier layer changes that can have second-order effects on the electrical resistance of the test structures. By accounting for such effects with the aid of the X-ray-based measurements, further improvement in the OCD correlation to electrical test measurements is achieved. Using both types of solution—incorporation of fast reference-based machine learning on both OCD-compatible and non-OCD-compatible test structures, and hybrid metrology combining OCD with XPS and XRF technology—improvement in BEOL cycle time learning is accomplished through improved prediction capability.

10145-4, Session 2

Patterning control strategies for minimum edge placement error in logic devices

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Since the 20-nm node, multiple patterning schemes are being used by chipmakers to create the small features of semiconductor devices. Meanwhile the factories are preparing for the shipment of 10-nm node devices, and at the same time the R&D crews have started the development of the 5-nm node. Along with the device shrink, the patterning performance requirements, characterized with edge placement error (EPE), have become very tight. EPE refers to the relative displacement of the edges of two features from their target positions. In order to assure a low EPE of the final pattern, the process variability caused by every individual process step must be understood and minimized. The error contributors of especially deposition, lithography and etch need to be considered here. At these advanced nodes we expect that both EUV and ArF lithography steps, and consequently also the systematic pattern placement differences between these two technologies must be minimized.

In this paper we will discuss our holistic patterning approach to understand and minimize the EPE of the final pattern. Using experimental data of a 7-nm logic patterning process based on Self-Aligned-Quadruple-Patterning (SAQP) using ArF lithography, combined with line cut exposures using 0.33 NA EUV lithography, we construct the EPE error budget and evaluate the main error components. The hybrid metrology method to determine EPE is discussed. It will be shown that ArF to EUV overlay, CDU from the individual process steps, and local CD and placement of the individual patterns, are the important contributors. Based on the error budget, we developed a holistic optimization strategy for each individual step and for the final pattern. Solutions include overlay and CD metrology based on angle resolved scatterometry, scanner actuator control to enable high order overlay corrections and computational lithography optimization to minimize imaging induced pattern placement errors of devices and metrology targets.

10145-5, Session 2

Hybrid scatterometry measurement for BEOL process control

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Scaling of interconnect design rules in advanced nodes has been accompanied by an increasing demand on inline metrology to enable control

of back-end-of-line (BEOL) processing. Dielectric hard mask layer thickness control to enable consistent etching of BEOL trenches is one challenge that has emerged due to thin copper layers in advanced technology nodes. Traditionally, measurements of film deposition thickness have relied on 1-dimensional (1D) film pads. Such film pads typically have copper blocks in their design, intended to minimize or eliminate any optical signal from below the films of interest. The reduction of this copper thickness and CMP dishing effects has resulted in a portion of the signal coming from layers below the copper. To avoid this metrology noise, and to measure structures that are more representative of product, measuring structures that have patterned copper gratings underneath is proposed using scatterometry, a diffraction based optical measurement technique using Rigorous Coupled Wave Analysis (RCWA), where light diffracted from a periodic structure is used to characterize the details of profile.

Scatterometry measurements on 3D structures have been shown to demonstrate strong correlation to electrical resistance parameters for BEOL Etch and CMP processes. However, there is significant modeling complexity in such 3D scatterometry models, in particlar due to complexity of front-end-of-line (FEOL) and middle-of-line (MOL) structures. The accompanying measurement noise associated with such structures can contribute significant measurement error. To address the measurement noise of the 3D structures and the impact of incoming process variation, a hybrid scatterometry technique is proposed that utilizes key information from the structure to significantly reduce the measurement uncertainty of the scatterometry measurement. Hybrid metrology combines measurements from two or more metrology techniques to enable or improve the measurement of a critical parameter.

In this work, the hybrid scatterometry technique is evaluated for measurement of a dielectric hard mask layer thickness and a dielectric trench etch application, both measured on a 3D BEOL structure shown in Figure 1. With this method, significant measurement noise reduction is achieved for M2 layer hard mask thickness measurements as compared to both 1D film pad and conventional scatterometry measurements as shown Figure 2. Figure 3 illustrates the improvement obtained in inline measurements of the hard mask film thickness through comparison of the conventional scatterometry and hybrid scatterometry method for two different metal layer modules (M2 and M3). For these applications, the within-wafer standard deviation for the hybrid scatterometry technique on the 3D structure is two to four times smaller than that of the conventional scatterometry model. Figure 4 compares measurements of the M2 layer hard mask and M2 dielectric etch trench depth in both standard process of record (POR) and 3 DoE configurations chosen intentionally to introduce metrology uncertainty into the model.

The data obtained from the hybrid scatterometry technique demonstrates the capability for robust characterization of the measurement parameter of interest without impact from parameter correlation from the incoming process DoE conditions. The paper demonstrates the flexibility of the technique for monitoring of 7nm and 14nm BEOL processes.

10145-6, Session 2

The coming of age of the first hybrid metrology software platform dedicated to nanotechnologies

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The development and integration of new materials and structures at the nanoscale require multiple parallel characterizations in order to control mostly physico-chemical properties as a function of applications. Among all properties, we can list physical properties such as: size, shape, specific surface area, aspect ratio, agglomeration/aggregation state, size distribution, surface morphology/topography, structure (including crystallinity and defect structure), solubility and chemical properties such as: structural formula/molecular structure, composition (including degree of purity, known impurities or additives), phase identity, surface chemistry (composition, charge, tension, reactive sites, physical structure, photocatalytic properties, zeta potential), hydrophilicity/lipophilicity. Depending on the final material formulation (aerosol, powder, nanostructuration…) and the industrial application (semiconductor, cosmetics, chemistry, automotive…), a fleet of complementary characterization equipments must be used in synergy for accurate process tuning and high production yield. The synergy between equipment so-called hybrid metrology consists in using the strength of each technique in order to reduce the global uncertainty for better and faster process control. The only way to succeed doing this exercise is to use data fusion methodology.

In this paper, we will introduce the work that has been done to create the first generic hybrid metrology software platform dedicated to nanotechnologies process control. The first part will be dedicated to process flow modeling that is related to a fleet of metrology tools. The second part will introduce the concept of entity model which describes the various parameters that have to be extracted. The entity model is fed with data analysis as a function of the application (automatic analysis or semi-automated analysis). The final part will introduce two ways of doing data fusion on real data coming from imaging (SEM, TEM, AFM) and non-imaging techniques (SAXS). First approach is dedicated to high level fusion which is the art of combining various populations of results from homogeneous or heterogeneous tools, taking into account precision and repeatability of each of them to obtain a new more accurate result. The second approach is dedicated to deep level fusion which is the art of combining raw data from various tools in order to create a new raw data. We will introduce a new concept of virtual tool creator based on deep level fusion. As a conclusion we will discuss the implementation of hybrid metrology in semiconductor environment for advanced process control

10145-7, Session 2

Hybrid methodology for on-product focus control using CD and diffraction-based focus marks

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The semiconductor industry's current standard of focus setup and control can be improved by the implementation of diffraction-based focus (DBF) marks and their applications. Determining best focus per scanner/reticle/device/layer (SRDL) combination is currently done by exposing a focus/energy matrix (FEM) wafer and examining CD features. The drawback of this process of record (POR) method is that the accuracy is greatly influenced by inter- and intra-field effects, focus step size, and machine accuracy. However, DBF marks do not suffer from these drawbacks because they are measured on product and close to the CD features. Experiments confirm that when comparing Bossung curves on each scanner, the wafer-to-wafer variation is much lower using DBF.

The setup time and accuracy of new SRDL combinations can also be greatly improved using DBF. DBF uses an asymmetry signal which is translated directly to focus values and is independent of any focus settings of the scanner. After accurately determining the best focus using DBF on only one SRDL combination, the focus setting can be applied to all other combinations and scanners will be matched. This method is illustrated in Fig.1; instead of exposing a FEM for each SRDL combination, best focus only needs to be determined once. Experiments using five different machine/reticle combinations show that Bossung tops can be matched two times more accurately compared to POR. Experiments also show a linear relation between energy and shift in Bossung top; both DBF and CD are sensitive to energy variation. When correcting for energy differences, the Bossung top scanner-to-scanner matching is six times more accurate than POR. A

method using DBF for scanner best focus matching saves up to 8 hours of CD-SEM and manpower setup time per SRDL combination. When a scanner needs to be requalified, the same DBF focus setup method can be used, reducing the scanner downtime.

Experiments have shown that DBF marks are sensitive to lens aberrations and energy variation. Although the impact on the readout accuracy in realistic cases is quite small, the typical machine-to-machine errors are comparable in size to the machine-to-machine matching accuracy. Combining DBF focus control and/or monitoring with the POR CD APC readouts (a so-called hybrid mode) will result in a robust strategy. Because DBF targets can be read out at a much higher rate through sparse integrated metrology and are more focus-sensitive, the focus feedback loop can catch high frequency variations and correct them. CDs can then be measured at a lower frequency to verify if the corrections DBF are correct. Offline dense DBF measurements can capture low frequency changes like intrafield and low-order interfield shapes. Experiments also showed diffraction-based overlay (DBO) targets are not influenced by focus offsets.

10145-8, Session 3

Impact of stochastic process variations on overlay mark fidelity at the 5nm node *(Invited Paper)*

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Accurate and precise edge placement in advanced semiconductor manufacturing relies on overlay metrology from proxies or targets in order to disposition and control the lithographic process. The impact of manufacturing processes on target noise and overlay mark fidelity has been characterized in the past , but such experimental characterization has not provided a quantitative link to basic lithographic quantities such as line edge roughness.

Two pending technology transitions currently underway will likely elevate the relative importance of overlay mark fidelity. Firstly, the transition from high order wafer level models to CPE (correction per exposure) models, drastically reduces the ratio of correctables to number of sites from which the model terms are determined. This necessarily means that the impact of any stochastic variations at each individual measurement site will have significantly higher impact on the model correctables. Secondly, the insertion of EUV on a small but critical number of layers is predicted to have an overall negative impact on lithographic line edge roughness. The combination of these two effects will potentially conspire to inject significant random noise into the lithographic overlay control loop which, for the 5 nm node has exceedingly tight requirements.

In this publication the authors will investigate both theoretically and experimentally the link between line edge roughness, target noise, overlay mark fidelity and their impact on model correctables. Based on previous work , a model will be presented to explain how any given edge of a printed feature could have a mean position that varies stochastically (i.e., randomly, following a normal distribution) due to lithography stochastic variation. The amount of variation is a function of the magnitude of the LER (more accurately, all the statistical properties of the LER) and the length of the feature edge. These quantities will be analytically linked to target noise and overlay mark fidelity, and ultimately the impact on overlay model residuals and the model terms themselves will be estimated for both optical and e-beam based overlay metrology. The model results will be compared with experimental results from wafers manufactured at IMEC on both EUV and ArF lithographic processes developed for 7 and 5 nm nodes

10145-9, Session 3

A complete methodology towards accuracy and lot-to-lot robustness in on-product overlay metrology using flexible wavelength selection

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The optical coupling between gratings in diffraction-based overlay triggers a swing-curve like response of the target's signal contrast and overlay sensitivity through measurement wavelengths and polarizations. This means there are distinct measurement recipes (wavelength and polarization combinations) for a given target where signal contrast and overlay sensitivity are located at the optimal parts of the swing-curve that can provide accurate and robust measurements. Some of these optimal recipes can be the ideal choices of settings for production. The user has to stay away from the non-optimal recipe choices (that are located on the undesirable parts of the swing-curve) to avoid possibilities to make overlay measurement error that can be sometimes (depending on the amount of asymmetry and stack) in the order of several "nm". To accurately identify these optimum operating areas of the swing-curve during an experimental setup, one needs to have full-flexibility in wavelength and polarization choices.

In this technical publication, a diffraction-based overlay measurement tool with many choices of wavelengths and polarizations is utilized on advanced production stacks to study swing-curves. Results show that depending on the stack and the presence of asymmetry, the swing behavior can significantly vary and a solid procedure is needed to identify a recipe during setup that is robust against variations in stack and grating asymmetry. An approach is discussed on how to use this knowledge of swing-curve to identify recipe that is not only accurate at setup, but also robust over the wafer, and wafer-to-wafer. KPIs are reported in run-time to ensure the quality / accuracy of the reading (basically acting as an error bar to overlay measurement).

10145-10, Session 3

Reaching for the true overlay in advanced nodes

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Traditionally, the total measurement uncertainty (TMU) of overlay metrology focuses on dynamic precision, tool-induced-shift, and matching, while rarely examining inaccuracy. However, some researchers have recently shown that measurement inaccuracy can still be large despite optimized small TMU. Moreover, this inaccuracy can consume a significant portion of the overlay budget in the advanced nodes. In addition to qualifying the overlay error of inline wafers, overlay metrology is also used for improving on-product overlay as it provides overlay error correction feedback to the lithography scanner. The accuracy of the correction terms as a result depends directly upon the measurement accuracy. As such, enhanced overlay accuracy will improve the overlay performance of reworked wafers, or subsequently exposed wafers.

We have previously shown that the segmented Blossom targets are more prone to asymmetry-induced inaccuracy than unsegmented targets [1]. Since target segmentation is inevitable for SADP and SAQP patterning processes, their resulting overlay performance leaves a lot to be desired. In our quest to reach for the true overlay, this paper reports our investigations on accuracy enhancement techniques for image-based targets, such as redundancy and asymmetry-calibration, and on the use of simulation-optimized scatterometry-based targets.

[1] Chiew-seng Koay, Nelson Felix, Bassem Hamieh, Scott Halle, Chumeng Zheng, Stuart Sieg, "Assessments of image-based and scatterometry-based overlay targets," Proc. SPIE 9778 (2016)

10145-11, Session 3

Image-based overlay measurements improvements of 28nm FDSOI CMOS front-end critical steps

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Technology shrinkage leads to tight specifications in advanced semiconductor industries. For several years metrology for lithography has been a key technology to address this challenge and to improve yield. More specifically overlay metrology is the object of a special attention and efforts from tool suppliers and semiconductor manufactures.

This work is focused on Image Based Overlay (IBO) metrology of 28 nm FDSOI CMOS front-end critical steps (gate and contact). With Overlay specifications below 10 nm, the inaccuracy of the measurement is critical and needs to be as low as possible. In this study we show specific cases where target designs need to be optimized in order to minimize process effects (CMP, etch, deposition...) that could lead to overlay measurement errors. Another discussed aspect of the metrology target is the device-like design in order to control and correct overlay errors leading to yield losses. Methodologies to optimize overlay metrology recipes are also presented. If the process effects cannot be removed entirely by target design optimization, recipe parameters have to be carefully chosen and controlled to illuminate the influence of the target imperfection on measured overlay. With target asymmetry being one of the main contributors to those residual overlay measurement errors the Qmerit accuracy flag can be used to quantify the measurement error and recipe parameters can be set accordingly in order to minimize the target asymmetry impact. Reference technique measurements (CD-SEM) were used to check accuracy of the optimized overlay measurements.

10145-12, Session 3

Higher order intra-field alignment for intra-wafer lens and reticle heating control

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Prior to exposure, each wafer is aligned by the alignment system. Because the alignment takes some time, the number of alignment marks that are measured is limited so that the throughput impact to the exposure tool remains limited. However, in order to get more accurate overlay performance, tool vendors decrease the measurement time of the alignment marks, allowing more marks to be measured per wafer.

The alignment system typically measures a selected set of alignment marks across the wafer to correct for the placement error of the wafer on the exposure stage and the wafer deformation. Usually, the wafer alignment does not correct for intra-field effects present in the layer to which it aligns. However, even after exposure tool calibration for lens and reticle heating, residual heating effects still remain that are usually not well controlled.

In an experiment, we exposed a set of wafers with special reticles containing a large number of alignment marks. This allows us to measure several marks per field, so that intra-field effects across the wafer can be determined for each wafer.

Different reticles have been used with different pattern densities, so that lens heating and reticle heating show different behavior per wafer. Some of the wafers have been exposed with higher dose than usual, so that the heating effects are larger. As a result, we will demonstrate the dose dependency of the heating effects.

In addition, overlay simulations have been performed with dedicated higher order intra-field overlay models to compensate for across wafer lens and reticle heating. With these simulations we quantify the improvement potential that can be achieved with higher order intra-field alignment.

10145-13, Session 3

High-volume manufacturing device overlay process control

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Advancing technology nodes in semiconductor manufacturing require smaller process margins. Overlay control is one of the key parameters to control due the tight requirements and strong correlation to yield. Overlay control based on ADI (after develop inspection) metrology of optical targets has been the primary basis for run-to-run (R2R) process control for many years, and has included significant enhancements in precision, accuracy, and throughput. Scanning electron microscopes (SEMs) have been used at AEI (after etch inspection) to provide supplemental overlay data to R2R process control systems on a limited basis due to throughput and lack of material transparency. In previous work [1] we described one such scenario where optical overlay metrology is performed on metrology targets on a high frequency basis including every lot (or most lots) at ADI. SEM based AEI metrology is performed on-device in-die as-etched on an infrequent basis. The difference between ADI and AEI overlay is often referred to as non-zero overlay (NZO), referring to the offset imposed on the ADI R2R control loop based on the infrequent AEI updates. Hybrid control schemes of this type have been in use for many process nodes: what is new is the relative size of the NZO as compared to the overlay spec, and the need to find more comprehensive solutions to characterize and control the variability of NZO. This investigation includes analysis of NZO sampling and modeling requirements to achieve control for the 1x nm processing node, in addition we investigate the temporal frequency and control aspects as well as trade-offs between SEM throughput and accuracy for the overlay use-case.

[1] Device overlay method for high volume manufacturing, Honggoo Lee, et. al., SPIE Volume 9778: Metrology, Inspection, and Process Control for Microlithography XXX, June 2016

10145-14, Session 3

In-depth analysis of indirect overlay method and applying in production environment

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Overlay measurements are done for verification of the exposure and for creating process corrections for the next lots. For leading edge technologies, the overlay of one layer is often critical to several other layers. As throughput of the overlay measurement tools in high volume environment is limited, it is desirable to avoid unnecessary measurements. Another concern can be that in-transparent stacks do not allow measuring all critical overlay relations directly.

We developed different types of methods for calculation of the overlay relation between two different layers that have no direct overlay measurement. This calculation, called indirect overlay, is based on measurements between each of these layers and other layers.

In the simplest situation a third overlay measurement can be derived from two other existing direct measurements. In addition, in case of in-transparent layers, it may be necessary to take more overlay measurements from different layers taken into account to estimate the indirect overlay.

In this paper, we use two methods to calculate indirect overlay for different sets of data, from both FEOL and BEOL processes. We consider and qualify the impact of sampling plans, different TIS settings, the distance of targets

and the number of dependent layers on the reliability of results.

It is not trivial to assess the quality of the method. We compare the accuracy of direct and indirect overlay using statistical numbers as TMU (total measurement uncertainty). By correlation analysis, we qualify the systematic and varying part of the differences between the direct and indirect overlay for the individual model parameters and the dispositioning criterion. We also present a set of tuning knobs to increase the accuracy of the indirect overlay method.

To verify the performance of indirect overlay calculation in a productive scenario, the performance has been compared on high volume data. For one specific case, all three overlay relations have been measured. All of them are critical to each other. Applying the method of indirect overlay calculation on two of the measured overlay relations the third relation was calculated and compared to the direct overlay measurement.

During further analysis the data are used to generate optimal process corrections based on the indirect overlay result. With our own run-to-run simulation the predicted overlay performance of the indirect overlay relation can be optimized. Based on the indirect overlay and the direct overlay measurement we generate a weighted feedback to improve the overlay performance for indirect overlay relation.

10145-15, Session 4

Metrology capabilities and needs for 7nm and 5nm logic nodes *(Invited Paper)*

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As the industry progresses down the ITRS [1], device dimensions shrink and device architectures increase in 3D complexity, and incorporate new materials. To enable efficient process development and yield ramp to successful production, demonstrated metrology capability must be realized at the forefront; such new critical in-line metrology will be needed to not only keep pace with these changes, but to provide process developers with the information necessary to accurately and efficiently evaluate the structural results of their work and to aid them in understanding their paths to profitable yields.

FinFETs continue to pose 3D metrology challenges,[2][3][4] and these challenges will continue to increase as fins evolve into nanowires. Multi-patterning is now commonly used in many different process steps, where alignment/overlay and complex periodicities add many complications.[5][6] Furthermore, small dimensions and volumes of the resulting features cause low signal-to-noise ratios. And not only are the patterns shrinking, but films become thinner [7] and smaller defects become yield detractors.[8]

This paper will provide an update to previous works [2][4] to our view of the future for in-line high volume manufacturing (HVM) metrology for the semiconductor industry, concentrating on logic technology. First, we will take a broad view of the needs of patterned defect, critical dimensional (CD/3D), overlay and films metrology, and present the extensive list of applications for which metrology solutions are needed. We will then update the industry's progress towards addressing gating technical limits of the most important of these metrology solutions, highlighting key metrology technology gaps requiring industry attention and investment.

[1] The International Technology Roadmap for Semiconductors (San Jose: Semiconductor Industry Association, 2016); available from the Internet: http://member.itrs.net.

[2] B. Bunday, T. Germer, V. Vartanian, A Cordes, A. Cepler & C. Settens. "Gaps Analysis for CD Metrology Beyond the 22 nm Node", Proc. SPIE, v8681, pp 86813B (2013).

[3] Benjamin Bunday, Aron Cepler, Aaron Cordes, and Abraham Arceo, "CD-SEM metrology for sub-10 nm width features", Metrology, Inspection, and Process Control for Microlithography XXVIII, Proc., SPIE Vol. 9050, 90500T (2014).

[4] Bunday, Benjamin. "HVM Metrology Challenges towards the 5 nm Node", Proc. SPIE 9778, 97780E (2016).

[5] D. F. Sunday, S. List, J. S. Chawla, and R. J. Kline. "Determining the shape and periodicity of nanostructures using small-angle X-ray scattering". J. Appl. Cryst., v. 48 (2015). doi:10.1107/S1600576715013369 .

[6] P. Dasari, et al. "Metrology characterization of spacer double patterning by scatterometry". Proc. SPIE, v7971, pp 797111 (2011).

[7] Benjamin Bunday & Richard Matyi. "X-Ray Metrology Needs", OSA Workshop, Washington, DC, October 2014.

[8] Matt Malloy, Brad Thiel, Benjamin D. Bunday, et al., "Massively parallel E-beam inspection: enabling next-generation patterned defect inspection for wafer and mask manufacturing", Proceedings of SPIE Vol. 9423, 942319 (2015).

10145-16, Session 4

Variability study with CD-SEM metrology for STT-MRAM: Correlation analysis between physical dimensions and electrical property of the memory element

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Emerging non-volatile memory devices are being studied extensively. Among them, STT-MRAM (Spin Transfer Torque-Magnetic Random Access Memory) is considered one of the promising candidates owing to its low power consumption, low latency, and excellent endurance. The memory element of a STT-MRAM device is an MTJ (Magnetic Tunnel Junction) pillar, which consists of an ultrathin MgO layer sandwiched by two ferromagnetic layers. The MgO layer has high or low tunneling resistance depending on the magnetization polarity of the ferromagnetic layers. This resistance difference is used as a memory bit. One disadvantage of STT-MRAM is its narrow resistance window which is typically about 2. Thus, cell-to-cell resistance uniformity is critical to ensure the memory reliability. Since the resistance of the MgO layer is ideally inversely proportional to its area, physical area control is essential. It is equally important to evaluate the area-independent variability of the resistance, as it affects the operable memory window. For this reason, correlation study between area and resistance of STT-MRAM cells was performed.

The physical area of the memory element was measured by CD-SEM. However, a direct measurement of the MTJ pillars after etching was not possible because in-situ encapsulation is required to avoid damage to the MTJ. Thus, measurements were performed after hard mask etching and after encapsulation. The area difference due to the step difference was corrected by utilizing the results of a dummy wafer which was measured at all steps, namely, after hard mask etching, after MTJ etching, and after encapsulation. The offset between physical dimension of the MgO layer and measured value was also calibrated. 852 pillars with different sizes (60-100 nm in design) were tested for statistical analysis. The calibrated area was compared with the conductance of the same pillar, which is the inverse of the measured resistance at low resistance state. The variation of MgO thickness across a wafer due to in-process variations was taken into consideration in the analysis.

The conductance of the measured pillars showed obvious linear correlation to their area besides some shorted pillars. Thus, the conductance was affected by the area variability of MTJ pillars as expected. Efficient size control should be effective in improving cell-to-cell conductance uniformity. Meanwhile, the conductance of the shorted pillars was proportional to the square root of the area. This suggests that a leakage occurred along the sidewalls of the pillar. In addition, the area-irrelevant conductance variability can be quantified by subtracting the component linear to the area. The conductance spread of the normal pillars defined by the interquartile range was 14% of the median conductance when the area-induced variability was not corrected, while the spread was 9% when it was corrected. Such an analysis should be useful for the investigation of the variability causes.

In summary, correlation analysis between physical size and resistance of STT-MRAM pillars was performed. The result indicates that the resistance variability can be reduced by size control. It was also concluded that this approach is useful for the failure analysis and the quantification of the size-independent resistance variability.

10145-17, Session 4

Designed tools for analysis of lithography patterns and nanostructures

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Nanobjects and nanostructures that can be found in semiconductor industry as well as in other industries exhibit advanced structures and complex patterns. Unfortunately, most of the measurements are currently performed manually, leading to an important source of improvement to obtain an accurate process control by reducing the variation on the measurements due to the different users. To satisfy such a demand, it is required the develop robust algorithms to perform automatic, accurate and fast metrological measurements. This smart tool requires the development of a new platform. The algorithms behind are based on computer vision and machine learning.

We have developed a smart tool oriented towards the detection of nanoscale features and extraction of significative dimensions for characterization of processes such as size, shape, roughness, critical dimension (CD) among others.

This tool is available in 2 levels: semiautomatic and automatic. We present some application using these approaches that we have developed. The main advantage for users is the high accuracy on the measurements, facilitating the analysis of high amount of images.

For the semiautomatic approach we present the measurement of Carbon Nano Tubes (CNT), where the user places a box over the CNT to measure automatically the internal and external diameter, as well as the number of walls. Another demonstrative approach is the measurement of contours in a pattern such as the case of lithography. By taking advantage of the smart tool, the user places control points close to the border of the pattern. Then, the profile is identified automatically with accurate and precise results, which could include intricate and complex designs. This approach was evaluated in VLSI patterns from which after 45 000 repetitions and placing randomly the points at maximum 10 pixels distance from the true profile, we measured its position and CD. The measurements at 3 sigma were 1.20 pixels in the position and 0.24 pixels for the CD. With the captured profile, we can measure differences with respect to a predefined model. This pattern can be searched for in a set of images and used to extract quantitative information for quality control of the processes.

As an example of the automatic identification we present the measurement of free surface block copolymer, lamellae and cylindrical, oriented to extract the CD, the periods, the defects, orientations, roughness among others. This information allows a complete characterization of the process which is fundamental for characterization and decision making.

To go further, the user can use the semiautomatic tools to create a database. An example is for the VLSI patterns, the database is created using the semiautomatic profile extraction. Combining the automatic period extraction and the database, we can analyze automatically and accurately VLSI images for calibration of microscopes.

We will present the performance of this smart tool in applications to semiconductor industry and a discussion of these applications, mainly the accuracy and precision of the results and the flexibility of adaptation to a wide process variations.

10145-18, Session 4

Required metrology and inspection for nanoimprint lithography

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Nanoimprint lithography (NIL) is regarded as one of the candidates for next-generation lithography (NGL) toward single-nanometer manufacturing. Among the wide variety of imprint methods, Jet and Flash imprint (J-FIL) is the most suitable for IC manufacturing for which high productivity and high yield are required. In J-FIL, resist is selectively applied by an inkjet to an imprinting field whose size is almost the same as that of an exposure field of a conventional optical scanner (~26mm x 33mm), and then a patterned mask (template) is directly contacted to the field under UV exposure. This resist apply and imprint process is carried out from field to field with step and repeat, which is similar to a conventional stepper or scanner.

From the viewpoint of metrology and inspection, there are some challenges inherent in NIL, which are not necessary for conventional optical lithography.

One is template inspection in which 1X quartz mask pattern has to be inspected. Compared with conventional 4X reticle inspection, much more resolution and sensitivity are required. An electron beam (EB) inspection tool is one of the candidates because it is the only tool that can resolve the template pattern whose size is less than 30 nm. We also have developed an optical based inspection tool. Its throughput and damage-less inspection are attractive for the supposed scheme of template management in high volume manufacturing (HVM).

The metrology for residual layer thickness (RLT) of resist pattern imprinted on a wafer is quite important. Because the RLT is the only control knob for critical dimension (CD) of NIL, nondestructive metrology followed by an RLT control method is needed. In the last SPIE advanced lithography conference, we proposed a scatterometry-based RLT control with the optimization of drop pattern of inkjet. Since then we have verified the RLT control for various layers and improved to the required level for HVM.

In this paper, we clarify the requirements in the metrology and inspection for NIL and show the solution that we have developed.

10145-85, Session 4

High-throughput electrical characterization for robust overlay lithography control

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Realizing sensitive, high throughput and robust overlay measurement is a challenge in current 14nm and advanced upcoming nodes with transition to 300mm and upcoming 450mm semiconductor manufacturing, where slight deviation from overlay has significant impact on reliability and yield1). Exponentially increasing number of critical masks in multi-patterning litho-etch, litho-etch (LELE) and subsequent LELELE semiconductor processes require tighter overlay specification2). Here, we will show limitations of current image- and diffraction- based overlay measurement to meet these stringent processing requirements due to sensitivity, throughput and low contrast3). We demonstrate show a new electrical measurement based technique where resistance is measured for a macro with intentional

misalignment between two layers. Overlay is quantified by a parabolic fitting model to resistance where minima and inflection points extracted characterize overlay control and process window, respectively. Analyses using transmission electron microscopy show good correlation between actual overlay performance and overlay obtained from fitting. Additionally, correlation of electrical based overlay control to existing image- and diffraction- based techniques will be discussed with focus on challenges of integrating electrical measurement based approach in semiconductor manufacturing from Back End of Line (BEOL) perspective. Our findings open up a new pathway for accessing simultaneous overlay as well as process window and margins from a robust, high throughput and electrical measurement approach.

10145-113, Session 4

Sub-wavelength transmission and reflection mode tabletop imaging with 13nm illumination via ptychography CDI

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We demonstrate reflection and transmission-mode imaging of extended samples using 13nm illumination produced by tabletop high harmonic generation through ptychographic coherent diffraction imaging (CDI). We achieve the first sub-wavelength resolution EUV imaging (0.9?) in a transmission geometry, with the highest spatial resolution using any 13.5nm illumination source to date. We also present the first reflection-mode image obtained on a tabletop using 12.7nm light, as well as the first 12.7nm reflection-mode image using any source, of an extended sample not fabricated on a multilayer mirror.

10145-21, Session 5

Application of actinic mask review system for the preparation of HVM EUV lithography with defect free mask

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Recently, readiness of the EUV infrastructure for the high volume manufacturing has been accelerated. At this point of time, providing a defect free EUV mask is very important to lead the EUV lithography into HVM. In order to produce a defect free mask, special metrology tools are required due to the difference in mask structures between EUV and ArF lithography. Current DUV and e-beam inspection tools may not catch real defects in EUV mask because the lights of corresponding wavelengths cannot penetrate multi-layers. Therefore, the actinic review system is essential to provide defect free EUV masks. The AIMSTM EUV can be one of the solutions but it is still being developed and a HVM tool is not available.

Previously, we introduced an EUV mask defect review system (EMDRS) which had been developed in SAMUSNG. The EMDRS has been continuously updated and used in various EUV related studies. It consists of a stand-alone coherence EUV source and a simple EUV optics including scanning stages, a zone plate lens, and an X-ray detector. The scanning based imaging system in the EMDRS provides aerial images. During the mask process in the FAB, the EMDRS is being utilized for the applications such as repair verification as well as studies on the defect printability, mask defect avoid technique, and line width roughness (LWR). In this paper, we introduce our recent works regarding practical applications at 1xnm half pitch line and space patterns with improved aerial imaging systems. According to the studies, we hope to find potential issues which can be happened during mask production and also improve each unit process to guarantee high quality EUV masks.

10145-22, Session 5

Toward a stand-alone high-throughput EUV actinic photomask metrology tool

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With EUV based lithography scanners being introduced for high volume manufacturing in the very near future, the need for a stand alone metrology tool for EUV photomasks is imminent and urgent. We have identified lensless optical metrology methods (Scanning Scattering Contrast Microscopy1 and Scanning Coherent Diffraction Imaging2) as viable and versatile methods for defect identification and characterization (both amplitude and phase) on photomasks. These techniques exploit the coherence of the illuminating probe and potentially meet the industry set targeted specifications of resolution, sensitivity and throughput for a photomask metrology tool. Evolving a stand-alone tool (RESCAN) based on these techniques critically hinges on the availability of (1) an intense coherent source for EUV with a small footprint and (2) a high frame rate pixel detector with extended dynamic range and high quantum efficiency for EUV. We present two in-house projects at Paul Scherrer Institute addressing the development of these major components for RESCAN – COSAMI and JUNGFRAU. COSAMI (COmpact Source for Actinic Mask Inspection), is a high-brightness table-top EUV source based on accelerator technology optimized for EUV metrology with a footprint of 5 x 10 m2. JUNGFRAU3, a silicon hybrid pixel detector, developed in-house and prototyped for EUV at the Paul Scherrer Institut, would form the imaging sensor for RESCAN. With a frame rate in excess of 2000 Hz and a demonstrated extended dynamic range of 106 92 eV photons this sensor solution is adapted specifically for the lensless EUV actinic metrology. We will present the conceptual design and targeted specifications for the former and provide recent results in the characterization and application of the latter. We believe that these ongoing source and sensor programs in conjunction with the aforementioned Fourier domain techniques, will bridge the gap for the need of an effective actinic metrology solution for defect identification and analysis in the EUV and pave way towards integrating a comprehensive tool.

10145-23, Session 6

Patterned wafer geometry grouping for improved overlay control

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As ground rules shrink, advanced technology nodes in semiconductor manufacturing demand smaller process margins and hence require improved process control. Overlay control has become one of the most critical parameters due to the shrinking tolerances and strong correlation to yield. Process-induced overlay errors from outside the litho cell have become a significant contributor to the error budget including non-uniform wafer stress. Previous studies have shown the correlation between process-induced stress and overlay and the opportunity for improvement in

process control [1, 2], including the use of patterned wafer geometry (PWG) metrology reduce stress-induced overlay signatures by monitoring and improving non-litho process steps or by compensation for these signatures by feed-forward corrections to the litho cell [3,4]. Key challenges of volume semiconductor manufacturing are how to improve not only the magnitude of these signatures, but also the wafer to wafer variability. Standard advanced process control (APC) techniques provide a single set of control parameters for all wafers in a lot, and thereby only provide aggregate corrections on a per chuck basis. This work involves a novel technique of using PWG metrology to provide improved litho-control by wafer-level grouping based on incoming process induced overlay. For the case of VNAND wafer stress is particularly high, and in the case of DRAM the overlay specs are extremely tight. We investigate the correlation between PWG metrology based wafer groups to overlay based groups under varying process conditions. We describe several control schemes based on wafer grouping, demonstrate process improvement in a volume manufacturing environment, and compare the results to other control techniques. We show that wafer-geometry measurements of in-process wafers, with novel algorithms, can be used effectively to reduce process-induced overlay errors from non-lithographic sources.

[1] Characterization and mitigation of overlay error on silicon wafers with nonuniform stress, T. Brunner, et. al., SPIE Volume 9052: Optical Microlithography XXVII, April 2014.

[2] Patterned wafer geometry (PWG) metrology for improving process-induced overlay and focus problems, Timothy A. Brunner, et. al., SPIE Volume 9780: Optical Microlithography XXIX, March 2016.

[3] Improvement of process control using wafer geometry for enhanced manufacturability of advanced semiconductor devices, Honggoo Lee, et. al., SPIE Volume 9424: Metrology, Inspection, and Process Control for Microlithography XXIX, April 2015.

[4] Lithography overlay control improvement using patterned wafer geometry for sub-22nm technology nodes, Joel Peterson, et. al., SPIE Volume 9424: Metrology, Inspection, and Process Control for Microlithography XXIX, April 2015.

10145-24, Session 6

Wafer-shape metrics based foundry lithography

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Wafer shape variability has been reported as a significant detractor of foundry manufacturing yield and specially of its lithographic process. Both in-plane displacement (IPD, distortion) and topography residuals (planarity) have been correlated to advanced lithography performance. The first directly impacts overlay, the second focus and critical dimension. Wafer shape metrology has been adopted in Research and Development to characterize wafer shape and in some cases minimize the variability of wafer shape due to process fluctuations. This has shown the importance of wafer shape control in thermal annealing, deposition and Chemical-Mechanical Planarization (CMP). However, this has not been sufficient to prevent wafer shape variability to become one of the main overlay and critical dimension budget components in high volume manufacturing. Advanced manufacturing lithography faces then 2 challenges. Firstly, the R&D wafer shape metrologies available do not have the density and speed required to cover statistically large volume of advanced material. Secondly, if a high density and high speed wafer shape metrology was available, robust metrics do not exist enabling the Statistical Process Controls (SPC) or Advanced Process Controls (APC) necessary to compensate for the lot to lot and wafer to wafer variability of wafer shape.

In this work, we report the adoption of CGS (Coherent Gradient Sensing) interferometry into high volume foundry manufacturing to overcome these challenges. Leveraging this high density 3D metrology, we characterized its In-plane distortion as well as its topography capabilities applied to the full flow of an advanced foundry manufacturing. When a relationship between the interferometry measurable and the traditional 2D metrology and inspection solutions are established then large volume of advanced material can be statistically characterized and correlated to the lithographic and yield performances. This allows the fingerprinting of process flow sections and the ranking of variabilities within that section, both required to locate and prioritize the possible points of application for statistical process control of wafer shape metrics. Having achieved this important milestone, wafer shape metrics must be optimized and tested for robustness before release into manufacturing; a fundamental validation of the inherent CGS technology capabilities for patterned wafer shape metrology.

We will show that the CGS interferometry not only achieve high degree of correlation with the traditional 2D metrology and inspection solutions used in foundry manufacturing but also that its high density and speed allows rapid statistical characterization of the critical wafer shape variabilities of the manufacturing process flow. Furthermore, we show that the wafer shape metrics robustness supports statistical process control (SPC) leading to lithography performance improvements. We also present how these SPC capabilities can be extended into future advanced process control (APC) solutions.

10145-25, Session 6

Application of patterned wafer geometry (PWG) to enhance overlay budget

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As overlay requirements are getting more stringent, monitoring and characterizing process effects on overlay becomes more important. Advances in metrology are providing new solution to measure the geometry of in-process wafers very quickly, which is PWG (patterned wafer geometry). It has been established that process-induced overlay can be estimated by measuring PWG. There are two kind approaches to reduce process-induced overlay error. One is the modification and optimization of related process that has major contribution in wafer geometry. The other is the feed forward application to adjust the expose tool parameters for compensating geometry related overlay error, and separate exposure based on the wafer grouping that has similar geometry-induced overlay fingerprint in the lot. In this paper, we describe an assessment of various process effects on overlay and the possible methods to release them. Moreover, we demonstrates how to increase matching rates between PWG and overlay data for more effective wafer grouping.

10145-26, Session 6

Topography based wafer clustering for wafer level overlay correction

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Non-linear overlay deformation is a well-known problem in today´s leading edge semiconductor processing. A significant root cause for the non-linear overlay deformation is the non-uniformity of stress across the wafer, caused by non-uniform deposition thickness, non-uniform high temperature processes, high-aspect etch ratio, and so forth.

In case the resulting non-linear deformation is constant, or at least slowly drifting, it can be compensated by higher order process corrections and field-by-field corrections that are based on feedback from previous wafers. However, as overlay budgets shrink, the remaining wafer-to-wafer variation becomes an issue.

It is well known that the non-uniform stress in the wafer not only causes the in-plane overlay deformation, but also deformation in the direction perpendicular to the wafer. Several metrology equipment vendors offer solutions to measure the topography profile of the wafer in great

detail. Because the perpendicular deformation is related to the in-plane deformation, analysis of the topography profile of the wafers can be used to enhance overlay corrections, using a clustering analysis.

In this case study, clustering is used on the topography profile data to sort each wafer into groups. Using the context information from the clustering, overlay feedback is computed on a wafer level basis, based on previous wafers from the same cluster only. The evaluation of the approach is done with a run-to-run simulation, which allows optimization of the method and evaluation of the on-product overlay performance improvement.

The simulation results are compared to experimental results, to verify the benefit of true wafer level control. In the analysis, different wafer zones are distinguished to characterize the improvement potential for the different zones.

10145-27, Session 7

In-line e-beam metrology and defect inspection: tactical and strategic applications on a single platform *(Invited Paper)*

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At SPIE 2013 in Metrology, Inspection, and Process Control for Microlithography an invited paper was published titled “In-line E-beam wafer metrology and defect inspection: the end of an era for image-based critical dimensional metrology? New life for defect inspection”. Three years have passed and numerous developments have occurred as predicted in this paper. The development of Ebeam tools that can concurrently handle metrology and defect applications is one of the primary developments. In this paper, the capabilities of these new Ebeam tools and their current use cases will be discussed in the areas of Critical Dimension Uniformity (CDU), In-die overlay, Hot spot and Physical defect inspection. Emphasis will be placed on use cases where “massive” CDU data is collected in order to increase yield learning for manufacturing (14nm) and decrease cycles of learning for development (7nm). Additionally, some of the other subject material from the previous publication will also be discussed such as the current state of Ebeam critical dimension image fidelity and decreasing physical defect detection capabilities. Lastly, future directions and opportunities for In-line Ebeam will be discussed.

10145-28, Session 7

Smart sampling for process control

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Engineers are continually faced with decisions about how much data they can collect. In this work, we present a statistically-based smart sampling methodology which can be used to target data collection and ensure that the risk to the product is clearly understood. Smart sampling combines knowledge of the distribution of control statistics with knowledge of their run length distributions to balance the need for information against the ability to respond to anomalies.

We define and explore three characteristics that any sampling plan deemed “smart” must explicitly address:

* control errors * that are associated with basing decisions on sample data, * jeopardy * that is associated with the inability to know the true state of the process, and the * switching mechanism * that controls the dynamic response to the latest information about the process.

We show how the interplay of these characteristics can be exploited to comprehend the merits of a smart sampling plan. Practical examples of optical inspection and defectivity control are presented and explained.

Balancing capacity and quality drives the argument for smart sampling. The desire is to sustain a stable process with low intensity sampling and contain an unstable process with a high intensity sampling. The latest process data should be used to indicate when to switch between sampling modes.

We consider the control errors * false hold * and * false release * where the expression * hold * means quarantine the lot, adjust, etc., and * release * means allow the lot to move, do not adjust, etc., as the context dictates.

False holds are caused by a lack of specificity; false releases are caused by a lack of sensitivity.

For example, a highly specific defect control system will not be misled by benign artifacts and a highly sensitive control system will detect and respond to the defects that are added at a process step.

We consider two kinds of jeopardy: the amount of material processed between false holds (J0) and the amount of material processed between false releases (J1). A sampling plan is not acceptable if the jeopardy that it entails exceeds the ability of the control system to respond appropriately.

The expected value of J0 is ARL0. If ARL0 is too short, the system will be overwhelmed with false alarms and needlessly consume resources.

The expected value of J1 is ARL1. If ARL1 is too long, the amount of material that is processed between the onset of a critical change and its detection will overwhelm the containment capacity of the system.

An ideal control system has infinitely long ARL0 and zero ARL1.

The switching mechanism controls which sampling mode to use based on the latest information available. Smart sampling plans operate in at least two different modes; low intensity and high intensity. High intensity modes may have larger sample sizes, higher frequencies of sampling, or both. Additionally, high intensity modes may consume more expensive resources than a lower intensity mode. When sampling is smart, a stable and capable process will be sustained more economically because a low intensity mode will be running most of the time.

10145-29, Session 7

A new method for wafer quality monitoring using semiconductor process big data

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As the semiconductor industry meets shorter life cycle of new design rule nodes, advanced wafer inspection and metrology techniques are required for the fast driving of process qualification. With an ever increasing number of metrology and inspection steps it becomes more critical to focus on in-situ metrology in order to develop robust processes providing sustainable device yields. Traditionally, metrology of process-driven defectivity is focused on investigating pattern abnormality primarily in the form of particle defects, miss-alignment of each process layers or CD (Critical Dimensions) changes. Conventional semiconductor metrology methods such as optical critical dimension (OCD), CD-SEM (CD-Scanning Electromagnetic Microscopy), bright and dark field optical inspection, and spectroscopic thickness measurement have been effectively used for wafer quality assessment during the production processes. Even destructive method for example transmission electron microscopy (TEM) measurement has been used to visualize under layer profile. However those methodologies generate production loss increasing number of process steps and destructive treatment of the real products. Thus the need of in-situ process monitoring methodology without additional measurement steps has been requested increasingly. In addition finding main cause of the failure during the process should be advanced by in-situ monitoring.

We now propose a new analysis and monitoring methodology PLAM (Process Log Analysis Metrology) using process big data for the detection of process defectivity especially applicable in semiconductor lithography processes. The research includes development of statistical main cause analysis methodology and monitoring system. Exclusively in this research the process big data includes process log, optically emitted spectrum, fault detection and classification data, measurement data, electrical die sort

failure analysis data and etc. Process logs and classification data are usually generated during lithography process and spectrum data are generated by plasma reaction of target material during the etch process. Those data are generated in huge amount, ie. big data, for example more than 5Tera bytes per day in one production line. To analyze the big data it is essential to extract desired data easily and rearrange the data structure in appropriate manner for the analysis convenience. Practically this kind of data handling burden engineers taking more than a month just for data pre-processing. To solve the big data handling problem in pre-processing stage we developed automated data collecting and arranging system which is able to handle large amount of data very effectively. The system has been proved that it provides effective data pre-processing method reducing preparation time from more than 2 month to less than 5 days. Also systematic analysis approach provides fast and concrete generation of result from cumbersome big data. As one of the application we analyzed process big data generated in lithography coating process to verify the process key parameters of specific functional failure using the developed system. It is also proven that the analyzed parameters work as key factor of the defect occurrence showing good correlation with final chip failure result. This study will provide new big data analysis methodology in semiconductor process as well as in-situ quality monitoring technique in various applications.

10145-30, Session 7

Combined process window monitoring for critical features

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After critical lithography steps, overlay and CD are measured on a selected set of wafers and locations on the wafer. The measurement result is used to judge if the wafers will have good yield, i.e. if they continue their journey through the line, or need to be re-worked. Traditionally, a certain overlay metric is applied per X/Y-direction, to verify if overlay is within specification across the wafer. Additionally, it is checked whether the CD measurement results fulfill a given specification.

From a design point of view, however, just overlay errors or CD deviations only are not sufficient to cause electrical failures. Electrical failure is usually based on a more complex interaction between CD deviations and overlay errors of different layers and the exact nature of this interaction depends on the specific design and process integration.

Therefore, in order to avoid yield impact, the traditional single parameter control limits must take into account maximum possible variations of the other parameters. But this would lead to an extremely small process window for the individual measurable parameter. Because this is not feasible for high volume production (HVM), specifications are typically relaxed to an acceptable working point, whilst some yield loss is taken into account.

An alternative method is to include realistic design constraints of the most critical parameters for the affected layers. This allows the calculation of a combined process window, so that the results of the different measurement steps are not judged individually, but in a combined way. We illustrate this with a simple scenario consisting of a contact that requires a minimum distance to the neighboring underlying metal line: the minimum distance is determined by the CD deviation of the metal line and the contact, but also by the bi-directional overlay error between both layers.

We evaluate this combined process control for a HVM use case, and show that a better relation between the combined measurement results and resulting electrical performance can be achieved compared to the traditional approach. In addition, this can be used to relax process constraints, which reduces the rework rate significantly.

10145-31, Session 7

Computational overlay metrology with adaptive data analytics

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With photolithography as the fundamental patterning step in the modern nanofabrication process, every wafer within a semiconductor facility will pass through a lithographic apparatus multiple times. With more then 20,000 sensors producing more then 700GB of data per day across multiple subsystems, the combination of a light source and lithographic apparatus provide a massive amount of information for data analytics. This paper will describe how data collected before the wafer is exposed can be used to predict small process dependent wafer-to-wafer changes in overlay.

As wafers move through a lithographic apparatus they will have their positions measured with wafer alignment and leveling metrology. This occurs after the wafer is clamped onto the wafer stage and just before exposure. The intention is to characterize any unique wafer-to-wafer deviations. Deviations can come from several sources; error from wafer placement onto the exposure stage, how the prior level's process has shaped the wafer surface, or if there is contamination on the backside of the wafer. Because the wafer has to be clamped onto the exposure stage, any contamination or non-uniformities between the two can affect the wafers surface topography. As a real world application, the physical models that control the wafer-to-wafer adjustments of the lithographic apparatus use the alignment and leveling metrology to consistently present each wafer to the exposure side image plain.

After the wafer is exposed and leaves the lithography apparatus, a select number of wafers will receive some form of overlay metrology. Using advanced techniques in data analytics this paper describes how a the addition of a adaptive model on top of the standard physical model can be used to pickup on the portion of pre exposure metrology that can reliably be correlated to post exposure metrology. The result is a full wafer prediction for every wafer within a lot. With data from a High Volume Manufacturing (HVM) semiconductor facility, the author's outline how a full lot of predicted overlay metrology can be used to improve feedback process control, be use for fault detection and (when the wafer receives measure side metrology within the lithographic apparatus) how real time predictions can be use for feed forward control during exposure.

10145-32, Session 7

Surface topography analysis and performance on post-CMP images

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Surface topography on post-CMP processing can be measured with white light interference microscopy to determine the planarity. Results are used to avoid under or over polishing and to decrease dishing. The numerical output of the surface topography is the RMS (root-mean-square) of the height. Beyond RMS, the topography image is visually examined and not further quantified. Subjective comparisons of the height maps are used to determine optimum CMP process conditions. While visual comparison of height maps can determine excursions, it's only through manual inspection of the images. In this work we describe methods of quantifying post-CMP

surface topography characteristics that are used in other technical fields such as geography and facial-recognition. The topography image is divided into small surface patches of 7x7 pixels. Each surface patch is fitted to an analytic surface equation, in this case a third order polynomial, from which the gradient, directional derivatives, and other characteristics are calculated. Based on the characteristics, the surface patch is labeled as peak, ridge, flat, saddle, ravine, pit or hillside. The number of each label and thus the associated histogram is then used as a quantified characteristic of the surface topography, and could be used as a parameter for SPC (statistical process control) charting. In addition, the gradient for each surface patch is calculated, so the average, maximum, and other characteristics of the gradient distribution can be used for SPC. Repeatability measurements indicate high confidence where individual labels can be lower than 2% relative standard deviation. When the histogram is considered, an associated chi-squared value can be defined from which to compare other measurements. The chi-squared value of the histogram is a very sensitive and quantifiable parameter to determine the within wafer and wafer-to-wafer topography non-uniformity. As for the gradient histogram distribution, the chi-squared could again be calculated and used as yet another quantifiable parameter for SPC. In this work we measured the post Cu CMP of a die designed for 14nm technology. A region of interest (ROI) known to be indicative of the CMP processing is chosen for the topography analysis. The ROI, of size 1800 x 2500 pixels where each pixel represents 2um, was repeatably measured. We show the sensitivity based on measurements and the comparison between center and edge die measurements. The topography measurements and surface patch analysis were applied to hundreds of images representing the periodic process qualification runs required to control and verify CMP performance and tool matching. The analysis is shown to be sensitive to process conditions that vary in polishing time, type of slurry, CMP tool manufacturer, and CMP pad lifetime.

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10145-33, Session 7

Advanced in-production hotspot prediction and monitoring with micro-topography

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At 28nm technology node and below, hot spot prediction and process window control across production wafers have become increasingly critical to prevent hotspots from becoming yield limiting defects. We previously established proof of concept for a systematic approach to identify most critical pattern locations, i.e. hotspots, in a reticle layout by computational lithography and combine process window characteristics of these patterns with across-wafer process variation data to predict where hotspots may become yield impacting defects.[1]

The current paper establishes the impact of micro-topography and its correlation with hotspot best focus variations across a production chip layout. Detailed topography measurements are obtained from an offline tool [2], and pattern-dependent BF shifts are determined from lihto simulation that includes mask-3D effects are used for this purpose. (Fig.1)

We also establish hotspot metrology and defect verification by SEM image contour extraction and contour analysis. This enables detection of catastrophic defects as well as quantitative characterization of pattern variability, i.e. local and global CD uniformity, across a wafer to establish hotspot defect and variability maps.

Finally we combine defect prediction and verification capabilities for process monitoring by on-product, guided hotspot metrology, i.e. with sampling locations being determined from the defect prediction model. The paper will demonstrate that across-wafer signatures after etch can be predicted, and process drifts over time could be effectively detected by guided hotspot metrology.

10145-34, Session 8

Global minimization line-edge roughness analysis of top down SEM images *(Invited Paper)*

Barton G. Lane, Tokyo Electron America, Inc. (United States); Chris A. Mack, Lithoguru.com (United States); Nasim Eibagi, Peter Ventzek, Tokyo Electron America, Inc. (United States)

We propose here a method for the line-edge roughness (LER) analysis of top down SEM images. In this method the edges of a set of adjacent parallel photoresist or etched lines and spaces imaged, from above using an SEM in a single frame, are fit to a set of straight lines with the following constraints: the lines are parallel to one another, the pitch (the distance between successive left or right edge lines) is the same for all the lines and the CD (the distance between left and right edge lines) is the same for all pairs of adjacent left and right side lines. These constraints represent the best estimate as to the location of the ideal line edges. The constraints of parallelism, pitch, and CD limit the number of free fitting parameters to 4 for an image, in contrast to a conventional fitting procedure which fits straight lines independently to each detected edge which can have 4n parameters if there are n photoresist lines to be fit. Hence the estimate of the line edge roughness defined as the normalized sum of the squares of the differences between the detected line edges from the estimated ideal line edges is greater for the constrained method relative to the unconstrained method. The constrained method can be viewed as answering the question: “Is the photoresist line edge in the right place?” while the unconstrained, line by line fitting method answers the question: “Is the photoresist line edge straight?”.

The constrained method in addition yields some interesting insights into the physical nature of both the short and long wavelength (low and high frequency) roughness. We find that the average displacement of each measured line edge from the expected location varies smoothly from adjacent line to adjacent line. This can be an indication of either instrumental aberration in the SEM or due to a long wavelength perturbation with a wave vector with components perpendicular to the photoresist line.

We examine these issues more quantitatively for this method versus the conventional line by line method by creating multiple realizations of synthetic images of sets of line edges such as would be generated by a top down SEM. We can control the shape and overall amplitude of the power spectral density function of the underlying processes generating the line edge roughness, the spatial coherence of the roughness between lines, as well as introducing synthetic SEM image aberrations. From these studies we can estimate how many images are required to be averaged in order to detect SEM aberrations of a given magnitude and how well the aberration can be subtracted out. We can also estimate how well the method estimates the long wavelength (low frequency) roughness and the degree of correlation between the long wavelength roughness on neighboring lines.

10145-35, Session 8

Level crossing methodology applied to line-edge roughness characterization *(Invited Paper)*

Chris A. Mack, Lithoguru.com (United States); Timothy A. Brunner, Xuemei Chen, Lei Sun, GLOBALFOUNDRIES Inc. (United States)

Line-edge and linewidth roughness is generally characterized using power spectral densities or height-height correlation functions to obtain not only the standard deviation of the roughness but also the correlation length and the roughness exponent. Unfortunately, each of these complementary approaches have their limitations. Alternate methods for estimating the correlation length in particular could be very valuable.

In time-series analysis one common technique for assessing statistical properties of the time series is to count the density of level crossings. This approach begins by defining as a random variable the number of times a series crosses the level a over a series length L (Figure 1). We shall ask, what is the expect number of level crossings given a knowledge of the statistical behavior of the rough feature? For the case of a roughness exponent of 0.5, the solution is known analytically. For other values of the roughness exponent, the expected number of level crossings can be simulated. An interesting property of the zero crossing rate (a = 0) is that it is independent of the magnitude of the roughness while still dependent on the correlation length. Thus, measuring the number of zero crossings provides a method for estimating the correlation length that is decoupled from the magnitude of the roughness and thus potentially dependent only on the photoresist (and not the quality of the aerial image).

In this paper, the level-crossing method will be introduced and developed theoretically. Using this theoretical development as a basis, experimental measurements of the level crossing rate will be combined with traditional power spectral density measurements to better estimate correlation length and roughness exponent. The (potential) usefulness of this technique as a standard LER analysis tool will be assessed.

10145-36, Session 8

Multitaper and multisegment spectral estimation of line-edge roughness

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Line-edge roughness has an important impact on the quality of semiconductor device performance, and power spectrum estimates are useful tools in characterizing it. One way to reduce the variance of the estimate is to take measurements of many lines and average a classical power spectrum estimate from each one. However, critical-dimension scanning electron microscopy causes sample damage during repeated measurements and critical-dimension atomic force microscopy is slow and has other disadvantages which affect measurement. To alleviate these problems we propose techniques which simultaneously reduce data requirements and variance over current approaches at the price of computational complexity. The multitaper method has widespread application including neuroscience, climate studies, and nuclear test-ban treaty verification. Previous papers have discussed the use of data windowing functions or tapers to reduce spectral leakage. Multitaper spectral analysis uses an orthogonal collection of tapers on a finite sample of data to obtain a set of statistically independent spectral estimates.

The overall spectrum estimate is either an average or a weighted average of the individual estimates. We choose the Slepian sequences as tapers because they protect against broadband leakage. The Welch method is a simpler but less effective way to reuse data. Just as there is a good parametric approximation to the error bars for the spectrum estimate calculated by averaging a given number of singly-tapered spectrum estimates, there are generalizations to these later methods and resampling techniques for other noise models if needed.

For our experiments we follow Mack's approach to use the Thorsos method to simulate random rough lines which follow a Gaussian distribution with an underlying Palasantzas spectral model with parameters specified in a paper by Verduin, Kruit and Hagen. Each simulated line initially has four thousand ninety-six points with a distance of one nanometer between successive points. The input to a spectrum estimator is the middle half of the points corrupted by additive white Gaussian noise. For the experiments using the periodogram and the single Welch window every spectrum estimate comes from the average of twenty-six lines; we consider the ninety-five percent confidence intervals based on a chi-squared distribution with fifty-two degrees of freedom. We do one thousand experiments per technique. We report the average length of a confidence interval over all frequency points and the fraction of instances where the true value of the spectrum at a frequency fell within the confidence interval of the estimate at that frequency. We also report the same experiments for the low-, middle-, and high-frequency regions specified in a recent paper by Levi et al. For the multitaper experiments we produce one spectrum estimate with six tapers per line and average over fourteen lines; we initially consider one hundred sixty-eight degrees of freedom and subsequently lower this by twenty or thirty to match the coverage of the first two techniques in the low-frequency range. We also report results on Welch multisegment estimates with three or seven segments per line and average over fourteen lines to obtain one spectrum estimate.

10145-37, Session 8

An OCD perspective of line edge and line width roughness metrology

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Metrology of nanoscale patterns is always challenging with multiple challenges that range from measurement noise, metrology errors, probe size etc. Optical Metrology has gained a lot of significance in the semiconductor industry due to its fast turn around and reliable accuracy. Apart from monitoring critical dimension, thickness of films, there are multiple parameters that can be extracted from Optical Metrology models3. Sidewall angles, material compositions etc., can also be modelled to acceptable accuracy. Line edge and Line Width roughness are much sought of metrology following critical dimension and its uniformity, although there has not been much development in modelling them with optical metrology. Scanning Electron Microscopy is still used as a standard metrology technique for assessment of Line Edge and Line Width roughness. In this work we present an assessment of Optical Metrology and its ability to model roughness from a set of programmed structures to simulate both Line edge and Line width roughness at multiple amplitudes and frequencies. Figure 1 shows design pattern with programmed jogs in a symmetric and asymmetric fashion to emulate Line edge and Line Width roughness.

10145-38, Session 9

Enabling CD SEM metrology for 5nm technology node and beyond *(Invited Paper)*

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The CD SEM (Critical Dimension Scanning Electron Microscope) is the main tool used to estimate Critical Dimension (CD) in semiconductor manufacturing nowadays, but, as all metrology tools, it will face considerable challenges to keep up with the requirements of the future metrology nodes. The root causes of these challenges are not uniquely related to the shrinking CD values, as one might expect, but to the increase in complexity of the devices in terms of morphology and chemical composition as well. In fact, complicated three-dimensional device architectures, high aspect ratio features, and wide variety of materials are some of the unavoidable features of the future metrology nodes. This means that beside an improvement in resolution, it is critical to develop a CD SEM metrology that is capable to satisfy the specific needs of the devices of the nodes to come, needs that sometimes will have to be addressed through dramatic changes in approach with respect to traditional CD SEM metrology.

In this paper we report on the development of advanced CD SEM metrology at imec on a variety of device platform and processes, for both logic and memories. We discuss newly developed approaches for standard, III-V, and germanium FinFETs, for lateral and vertical nanowires, for via in trench, 3D NAND, STT RAM, and ReRAM. Applications for both front-end of line (FEOL) and back-end of line (BEOL) are developed. In terms of process, S/D Epi, SAQP, DSA, and EUVL have been used. The work reported here has been performed on Hitachi CG5000 and CG6300.

In terms of logic, we discuss here the S/D epi defect classification, the metrology optimization for STI Ge FINs, the defectivity of III-V STI FINs, gate measurements on and off FINs, metrology for vertical and horizontal NWs. With respect to memory, we discuss the development of more in-depth algorithms for pillar measurements, the STT RAM statistical CD analysis and its comparison to electrical performance, ReRAM metrology for OxRam and VMCO with comparison with electrical performance, 3D NAND ONO thickness measurements (see Fig. 1). In addition, we report on 3D morphological reconstruction using CD SEM in conjunction with FIB, on optimized BKM development methodologies, on CD SEM overlay.

The large variety of results reported here gives a clear overview of the creative effort put in place to ensure that the critical potential of CD SEM metrology tools is fully enabled for the 5nm node and beyond.

10145-39, Session 9

Framework for SEM contour analysis

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EM images provide valuable information about patterning capabilities of available lithographic tools and processes. Geometrical properties such as Critical Dimension (CD) that can be extracted from them are used to calibrate OPC models, thus making OPC more robust and reliable. However, complex 2-dimensionnal patterns currently do not have appropriate metrology tools to inspect them as it is possible to do with any simple 1D pattern.

In this article we present a full framework for SEM image analysis. It has been proven to be fast, reliable and robust for all types of structures, especially 2D structures. The framework we will describe is composed of a series of innovative solutions that each respond to specific needs of the different steps involved in SEM image treatment. We will describe each of these solutions in the present article and provide support for our findings with images from our datasets.

Firstly, it is important to understand how the aforementioned solutions can be implemented to achieve the sought after image analysis and the role each of them plays in the overall treatment process. These solutions in greater detail are :

1) A new filter for noise reduction, which is more efficient than existing filters in terms of both computationnal cost and edge extraction accuracy.

2) An algorithm to detect bottom and top parts of a SEM images without prior assumptions. A direct consequence is the automatic detection of inner and outer contours.

3) The use of topological skeleton as a shape descriptor to measure geometrical information. It allows a robust and accurate measurement of geometrical characteristics even for complex 2 dimensional patterns which replace CD-SEM measurements.

4) The use of phylogeny to classify SEM images. A closer look at the principles used in this field may allow to develop innovative solutions for organizing image analysis results, that is based on the possibility to classify SEM images and to sort them based on their geometrical proximity.

10145-40, Session 9

Robust 2D versus 1D patterns process variability assessment using CD-SEM contours extraction offline metrology

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In advanced core and derivative technology nodes more aggressive design rules are required leading to complex designed features. These features bring more challenges to chips manufacturing processes, in particular lithography and etching steps. To improve and optimize these design rules, designers need to rely on process assumptions based on engineers' knowledge of their processes. Today, these process assumptions must be fed with information from more complex structures: corner rounding, tip-to-tip, tip-to-line, line end shortening, pattern distortion, etc.

Metrology needs also to evolve so that process engineers are able to measure 2D features to quantify their process variability on silicon. Today process variability is mostly addressed through the analysis of in-line monitoring features which are often designed to support robust measurements and as a consequence are not always very representative of critical design rules. In parallel, the process window of the whole design is assessed using Focus Exposure Matrix (FEM) wafers and/or Process Window Qualification (PWQ) that are measured on some features, characterized in defectivity and brought to yield measurements. FEM and PWQ do not provide variability information, but only confirmation of a dose and focus set point along with a dose and focus range (sometimes combined with overlay, etch setups or any other modulator) that will be associated with a CD range of a reference feature that will be used to set in-line specifications to monitor and secure the process using standard SPC indicators. How does the dispersion of monitoring features correlate to the dispersion of complex features?

CD-SEM metrology is challenged when it comes to measure complex features found in patterning hotspots (like tip to tip, tip to side, necking, bridging ...) in high quantity with a good robustness. Recipe creation becomes difficult and time consuming, multiple questions come to mind like what to measure and how to place measurement boxes? There is a wealth of information inside CD-SEM pictures that are discarded when engineers are setting their measurement boxes inside the measurement recipes.

Today metrology analysis tools provided by CD-SEM suppliers allow us to extract SEM contours of a feature and convert them into a GDS format where dimensional data can be performed. The CD-SEM takes pictures, the measurement and the choice of what needs to be measured is done offline and can be retuned anytime without using a CD-SEM tool anymore. Most of the time this is used for OPC model creation but barely for process variability analysis at nominal process conditions.

We showed in a previous paper (Translation of lithography variability into after etch performance: monitoring of a "golden hotspot", J. Finders et al, European Mask and Lithography Conference 2016, Dresden) that it is possible to study lithography to etch transfer behavior of a hotspot by using SEM contours extraction combined with an algorithm to realize

measurements through contours data. The goal of the current paper is to go forward with this methodology to quantify and compare process variability of different features, either 1D or 2D. The work is done using a 28 nm CMOS process at metal 1 level, both after develop and after etch inspections.

10145-41, Session 9

CD-SEM distortion quantification for EPE metrology and contour analysis

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To quantify relative and local placement of features, SEM is the metrology tool of choice. The SEM platform is the only metrology able to make a compromise between throughput and local information in the measurement.

Traditional CD-SEM applications perform measurements on a short length scale compared to the field of view (FOV). For local placement one needs information on different length scales ranging from near traditional sizes to extending over the full FOV. This introduces an error factor in these measurements in the form of SEM distortions. There are 2 flavors of distortions that introduce an error. Global which can be described by rotation, magnification errors, skew and shear. Secondly there are local, more random shaped effects. This paper proposes a way of describing the distortions allowing assessment of their impact on the application which relies on local placement information.

Traditional CD measurements are hardly impacted, as the effects average out on the length scale of interest when the feature is much smaller than the SEM FOV. In other applications the distortions are in the tolerance budget for large features. When performing measurements to support contour based OPC or relative placement within a layer or in multiple patterning, all information is extracted related to a position within a single FOV. A wrongly reported position by SEM will introduce a possible error in the data. These measurements are impacted by both the global as the local distortions.

Method to derive and quantify distortions

When dealing with distortions there are several factors to take into account:

1. System to system variability, even SEMs of the same brand and model could have different distortion profiles.

2. Short time scale stability, meaning a timespan up to the time needed for move and acquire.

3. Long time scale stability, would be visible as drift in distortions over multiple measurements.

4. Imaging setting variability, changing voltage, beam current, magnification etc. could impact the fingerprint of the distortions.

In our initial studies on the fingerprint of distortions we kept factors 1 and 4 constant. We limited the number of points used within a single acquisition to limit the impact of long term stability. We assumed the short time scale effect would be small enough to perform measurements above noise level.

By using a contour based measurement we could determine the offsets from the expected positions based on mask design. For this assessment we used a feature array with a semi dense slot array in the FOV. We excluded mask error by sampling strategy. First details on method and result are shown in Figure 1 & 2. The delta between expected position and found position is represented as a vector and can be used both visualize as well as describe the distortions. In our experiment on a limited set of features a mean length of error was found of 1.6 nm.

In the paper we will address stability of the distortions over the factors described above.

Application and outlook

Once the contribution by SEM distortions is known, a budget of the SEM contribution to model error can be derived. This is also applicable to budgeting EPE including metrology error.

If SEM distortion contribution is exceeding budget, a vector based description allows offline correction of SEM data and possibly extends into online correction.

10145-42, Session 10

Assessing the wavelength extensibility of optical patterned defect inspection

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A core principle of optical patterned defect inspection is that with decreased dimensions, “killer” pattered defects will scatter far less light. Multiple papers have been published with simulated and experimental demonstrations of such decreases over several semiconductor manufacturing nodes. However, less attention has been directed to the effects of the illumination wavelength on defect detectability. Comparisons have been made in the literature between the scattering off deep-subwavelength-sized defects and the scattering off spheres, the latter of which can be analytically solved using Mie’s Theory. This theory reduces to the Rayleigh approximation, for a particle with diameter d << λ, the inspection wavelength. For the Rayleigh approximation the scattered intensity I scales as I d^6 / λ^4. Using this approximation, simple reductions of wavelength hold promise for increases in detectability, and state-of the art techniques now use wavelengths as short as 190 nm.

This paper examines these potential scattering gains from using shorter, vacuum ultra-violet (VUV) wavelengths, weighted against the significant challenges of VUV microscopy. First, optical engineering requirements of the VUV are reviewed and fundamental physical limitations considered. Second, we seek to validate the Rayleigh approximation as a predictor of defect detectability. Third, rigorous three-dimensional electromagnetic modeling of light scattering from conventional 3-D layouts are performed at several wavelengths to quantify how defect inspection can be extended by using smaller wavelengths.

As shown in Fig. 1 [see Supplemental], simulated differential images for orthogonal bridge directions (“Bx”,”By”) are shown for two VUV wavelengths (122 nm, 157 nm) and for 193 nm as a benchmark. Using a recent SEMATECH Intentional Defect Array as a basis, we have combined optical constants from the literature with publicly disclosed geometrical cross-sectional information on current manufacturing processes (scaled down to 8 nm CDs) as inputs to our in-house finite-difference time-domain (FDTD) Maxwell’s equations solver. Qualitatively, the data demonstrate an increase in defect detectability as the wavelength decreases.

Beyond these preliminary data, additional emphasis will be placed on the wavelength dependence of the wafer noise due to line-edge roughness (LER). Defect metrics for quantifying gains with wavelength scaling are to be defined that harness increases in the scattered intensities while accounting for the reduction in scattering volume with wavelength. Optimizations in linear polarization, incident angle, and focus position for defect inspection are to be considered for each wavelength.

10145-43, Session 10

Anamorphic approach for developing hi-efficiency illumination system to inspect defects on semiconductor wafers

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In order to effectively inspect fine defects on the wafer using optical method, extreme performances of the objective lens and illumination system are inevitable. Resolution of the objective (OBJ) can be simply described by an Airy disk (Z) as Z=1.22λ/2NA and be improved with a higher NA

(Numerical Aperture) of objective and a shorter wavelength. Illumination systems that this study focused on cos underestimated relative to the OBJ are evaluated by brightness, uniformity and concentration efficiency of beam intensity.

There are well known two types of conventional illuminations, Abbe and Köhler. When using these systems in dark field without consideration of anamorphic optics, some issues appear such as asymmetric and non-uniform. This is because the beam shape on the illumination area has difference magnification of aspect ratio according to incident angle. These cause the efficiency of illumination to decrease. Therefore an illumination system which is designed with consideration of anamorphic optics is required.

This study intends to design illuminations which are optimized with anamorphic optics. Three types of dark field illumination namely, Far-field Areal Illumination (FAI), Near-field Areal Illumination (NAI) and Linear Illumination (LI), are evaluated.

First, the FAI is designed to illuminate an objective plane inclined at 30 and 15° to the horizontal and it is suitable for a NA 0.85 objective using UV (Ultra Violet) wavelength of 354.7nm. The light source is an Nd:YAG laser connected to random fiber bundle arrayed hexagonally as homogenizer. The FAI is designed with a right-angle prism to meet certain conditions on the objective surface. To form a 1:1 aspect ratio on an objective plane after illuminating, the beam shape's aspect ratio should be 1:2 for an incident angle of 30° and 1:4 for an incident angle 15°.

Second, the NAI uses the same light source as FAI and it is suitable for a NA 1.13 objective lens using a SIL (Solid Immersion Lens). In near-field illumination using an SIL, there is not enough back focal length to directly illuminate the objective plane because the interval between SIL and the objective plane is filled with a 0.1mm thick immersion. Therefore the NAI is designed to illuminate the objective plane through the side of SIL also to avoid interference between SIL and the other lenses. To meet these conditions, it is composed of a right-angle prism to control aspect ratio. To improve efficiency of light source and compensate for key stone distortion caused by the side of SIL, the random fiber bundle is shaped in the form of an anamorphic trapezoid.

Third, the LI is suitable for a NA 0.46 objective lens using 365nm UV wavelength. The light source is comprised of 6 LED chips arrayed linearly. It shows Lambertian type radiation and its bandwidth is 350~370nm. It uses cylindrical lens to form a linear beam shape. We produced a proto-type to test an illumination performance. We are going to use homogenizer and bandpass filter to enhance the performance.

10145-44, Session 10

Rapid Nano 4: Inspection tool for sub-20 nm particle detection: experimental results

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The Rapid Nano is a particle inspection system developed by TNO for the particle cleanliness qualification of EUV reticle handling equipment [2]. The detection principle of this system is dark-field microscopy. The performance of the system has been improved via model-based design. Through our model of the scattering process we identified two key components to improving the inspection sensitivity [3]. The first component is to illuminate the substrate from multiple azimuth angles. This illumination mode averages out the variance in the background scattering, allowing for a lower detection threshold to be used. This illumination mode is first implemented in the predecessor of Rapid Nano 4, the Rapid Nano 3 [4].

The second component to improve the sensitivity is to decrease the wavelength of illumination. A shorter wavelength increases the total scattering and reduces the background scattering relative to the defect signal. A new Rapid Nano inspection system (RN4) showed first results in the end of 2016, which combines the multi-azimuth illumination mode with a 193 nm source. This system will have a sub 20 nm LSE sensitivity, in-line with the requirements of the ITRS roadmap for defects on EUV masks (Figure 1). Model predictions and measured results are shown in Table 1.

The Rapid Nano inspection system uses the principle of dark-field imaging, in which an area of a substrate is imaged on a camera (Figure 2). Previous generations of the Rapid Nano system used commercially available optics for the imaging step. In the DUV wavelength regime diffraction limited imaging over a large field is more challenging and suitable optics were not available off-the-shelf. Therefore TNO designed and fabricated an objective lens specifically for the Rapid Nano 4 inspection system.

Other challenges in changing the illumination to the DUV include handling the high peak power of the pulsed laser source and the lifetime of the optics. The design of the Rapid Nano 4 and first measurement results comparing it to the model predictions will be presented.

10145-45, Session 10

1.5nm fabrication of test patterns for characterization of metrological systems

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The semiconductor industry is moving toward a half-pitch of 11 nm and 7 nm. The required metrology equipment should be at least one order of magnitude more accurate than that. The characterization of metrology systems requires test patterns that are one order of magnitude smaller than the measured features. Test patterns with linewidths down to 1.5 nm were fabricated. The test patterns contain alternating lines of silicon and tungsten silicide that provide good contrast in images. The size of the test sample was approximately 6x6 microns and involved hundreds of lines, each according to its designed width.

The test sample was designed in such a way that the distribution of linewidths appears to be random at any location and any magnification. This pseudo-random test pattern is used to characterize metrological equipment. The power spectral density of such a test pattern is inherently flat, down to the minimum size of lines. Metrology systems add a cut-off of the spectra at high frequencies; the shape of the cut-off characterizes the system in its entire dynamic range, describing the loss of sensitivity as the linewidth decreases. This method is widely used to characterize optical systems, and has allowed optical systems to be perfected down to their diffraction limit. There were attempts to use the spectral method to characterize nanometrology systems such as SEMs, but the absence of natural samples with known spatial frequencies was a common problem. The system characterization includes the imaging of a pseudo-random test sample and image analysis by a developed software to automatically extract the power spectral density and the contrast transfer function of the nano-imaging system.

10145-46, Session 10

Fabrication of metrology test structures with helium ion-beam direct write

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As the transistor critical dimension continues to shrink, lithography is confronted with challenging issues in various aspects. Patterning imperfection is one of the significant factors that influence the device performance and functionality, including wire and contact shorting or opening and line width variation, making metrology resolution and accuracy increasingly critical as well. Besides conventional optical and electron microscopy, even newer approaches such as optical scatterometry and AFM are facing significant challenges in sub 20 nm technologies. International Technology Roadmap for Semiconductors (ITRS) indicates that rapid introduction of the complicate 3D structures urges the requirements of accurate metrology and test structures to measure full profiles and improve defect detection. Therefore, metrology and inspection methods with a higher resolution for complicate structures are required. The fabrication of high-resolution test structures is an important step to the successful development of the needed metrology solutions. Although conventional lithography processes such as electron beam direct-write (EBDW) lithography can be utilized to fabricate the test structures, it can encounter significant process and resolution difficulties at advanced technology nodes due to severe forward and backward electron scattering. Helium ion beam direct-write (HIBDW) is a promising alternative for its advantages that include smaller focusing spot, less proximity effects, and hence potentially higher resolution and better patterning fidelity. In this work, we investigate the feasibility and potential advantage of utilizing HIBDW, in particular in the form of direct helium ion milling, for such applications. The capability of patterning control is demonstrated with high resolution and low process complexity, indicating its potential in metrology test structures fabrication. Several test patterns have been designed and fabricated, including a 6T-SRAM cell gate layer direct milling with programmed imperfection on a 50 nm gold-on-glass substrate. A further investigation on sub 10 nm structures and different materials such as programmed LER and chromium-on-glass substrates will be conducted.

10145-47, Session 11

High-NA optical CD metrology on small In-cell targets, enabling improved higher order dose control and process control for logic

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In advanced semiconductor production the Critical Dimension of the lines and contact holes at different process steps are controlled using dense CD metrology in combination with feedback control systems to lithography tools and other patterning tool systems in the FAB. Tighter CD control can be achieved using high order dose correction on the Lithography patterning tool and/or increased capability of tracks and etchers to control the wafer fingerprint. To allow the CD measurements to fully cover the intra-field and inter-field variations, it is required to use densely placed small targets or measurements in the device itself. Historically the metrology tool used is CD-SEM. An alternative is Optical CD (OCD) metrology. OCD provides additional information on profile and stack, which makes it very suited for monitoring and control of deposition and etch tooling. In addition it offers higher throughput and a better TMU then CD-SEM. State-of-the-art OCD metrology requires targets with repetitive structures. These targets are typically 40x40μm2 or 25x25μm2, an area which is available in the scribe lanes only, prohibiting the dense intra-field metrology required to capture the full reticle fingerprint and process fingerprints variations at the edge of the wafer.

High-NA optical CD metrology offers the capability to overcome this traditional limitation of Optical CD systems. It has been demonstrated that target sizes down to 12.5x12.5μm2 are feasible (see ref. [1]). By a further reduction of the spot size, enabled by the high-NA of the system, target sizes well below 10x10μm2 can be measured accurately and precise.

We will show the capability of this system to measure CD and other parameters of interest using small targets or in-cell targets down to 5x5μm2. Additionally we will quantify the improvement potential enabled by very dense and frequent metrology using higher order dose corrections at different steps in the process on multiple advanced production layers.

[1] Hugo Cramer, et al, "Intra-field patterning control using high-speed and small-target optical metrology of CD and focus", Proc. SPIE 9424, Metrology, Inspection, and Process Control for Microlithography XXIX, 94241F (2015); doi: 10.1117/12.2085957

10145-48, Session 11

Complex metrology on 3D structures using multi-channel OCD

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Device scaling has not only driven the use of more complex structures, in terms of both geometry and materials, and tighter groundrules, but also the need to move away from unpatterned measurement sites to patterned ones, especially for very thin film layers that have a high thickness dependence on structure geometry or wafer pattern factor. This transition of thin film thickness measurement is required not only because of the inability of unpatterned site thicknesses to properly track those of patterned or device sites, but also in some cases of increasing occurrence of unpatterned sites leading to defectivity issues and yield loss. Thus, transition away from such unpatterned sites can become more of a necessity than of preference, so that such sites can be removed from future mask designs. Although 2-dimensional (2D) sites often are found sufficient for process monitoring and control of very thin film thickness, sometimes 3D sites are needed. The measurement of film thicknesses only a few atoms thick on complex 3D sites, however, is very challenging. Apart from measuring thin films on 3D sites, there is also a critical need to measure parameters on 3D sites which are weak and less sensitive for OCD (Optical Critical Dimension) metrology, with high accuracy and precision. The OCD metrology, or scatterometry, is an optical technique for measuring detailed profile information on patterned structures. Important device characteristics are controlled by such parameters and confidence in the metrology read-out is of utmost importance. Thus, state-of-the-art, and even newly developed, methods are needed to address such metrology challenges. This work describes how more channels of information improve the precision and accuracy of weak, non-sensitive and complex parameters of interest.

This work describes the approach used to measure various parameters on complex 3D structures, including the ultra-thin high-K gate dielectric of advanced devices. In-line X-Ray Photoelectron Spectroscopy (XPS) was used as reference measurement for thin film thickness and composition, and also used to improve the measurement quality of the high-K thickness by decoupling the signal of this parameter from other parameters. Furthermore, the use of the additional channels from the OCD system greatly increases optical sensitivity to the high-K film thickness. In this paper we describe the methodology and detail the results that demonstrate the improvement of using the new channels of OCD information on 3D structures. Figure 1 shows the 3D structure that has the high-K film deposited and measured. The structure replicates the actual device at the specific process step. Figure 2 shows the improvement of within wafer variability (here, associated with improved measurement precision) of the high-K thickness when the new channels of information are used. We will also show how accuracy

and precision of measuring other complex and difficult parameters on 3D structures (besides film thickness) is improved by using new channels combined with state-of-the-art newly developed methods.

10145-49, Session 11

Optical metrology strategies for inline 7nm CMOS logic product control

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CMOS logic devices in the 10nm and beyond technology nodes have been enabled by two major process innovations, multiple patterning and 3D geometry. But these changes have required ever-tightening limits on process control and with this a smaller metrology budget. In addition, optical metrology techniques are being heavily impacted by processing on prior layers and needs to be accounted for in models. Inline film thickness measurements on planar targets also no longer correlate well to device performance.

A solution for 10nm node that we reported previously is a “film on grating” (FoG) measurement technique using spectroscopic ellipsometry (SE) that can enable sub-Angstrom level precision for multi-layer film thickness measurement on topographies that closely approximate the device structure. FoG follows the industry trends to measure what matters and provides thickness measurement data from patterned structures that has much stronger correlation to actual device performance. In this paper, we further explore the use of this methodology for 7nm node devices and process flow. It is observed that high resolution and accurate discernment of the process splits has been enabled by our FOG technique. We will show that the use of multiple measurement subsystems combined with advanced algorithms are critical in enabling the measurement resolution required to support 7nm process requirements. These measurement subsystems include a rotating polarizer/rotating compensator SE with high signal/noise combined with a laser-driven spectroscopic reflectometer (LDSR).

We also explore the impact of deviations in the film stack that can appreciably alter the device performance. One of the key device performance metrics that we will investigate is the leakage current, which is highly sensitive to the equivalent oxide thickness (EOT) - a 1Å shift in EOT can change leakage current by an order of magnitude. Conventionally, the reference value for EOT is obtained by electrical testing of the device after it has been built up till the first metallization level. This means that several process steps are conducted after the HK deposition over multiple weeks on the product wafer prior to learning if the EOT is within acceptable limits. Multiple week learning cycles is not acceptable in a high volume manufacturing setting. Since the introduction of HK dielectrics at 32nm node, it has been observed that the physical thickness of the high-k dielectric does not correlate well to the EOT. However, measuring both the thickness and the bandgap of the HK dielectric permits excellent correlation with EOT determined by electrical testing of the device. The ability to predict the EOT effectively will greatly accelerate learning cycles during process development and can enable real time product control on existing inline metrology tools.

The bandgap of HfO2 based dielectrics is typically in the 5.5 - 6.5eV range, requiring any optical measurement technique to employ a probing wavelength range of 190 - 225nm. In this paper we will describe the capability of spectroscopic ellipsometry (SE) to measure the gate dielectric bandgap and material defects. We will also demonstrate that these gate stack material defects and bandgap measured by SE can reliably track process variations not captured by conventional in-line film thickness measurements. The deep UV wavelength range required to measure the HK bandgap also requires very high signal-to-noise ratio (SNR) in order to precisely and accurately track the bandgap. We will show that laser-sustained plasma source (LSPS) afford the high SNR deep UV radiation required to discern the shift in the bandgap of the gate dielectric before and after deposition of the metal gate, which is not possible using ellipsometers based on conventional arc lamps.

10145-50, Session 11

Evaluating the effect of modeling errors for isolated finite 3D targets

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Optical 3-D nanostructure metrology utilizes a model-based metrology approach to determine critical dimensions (CDs) that are well below the inspection wavelength. More specifically, the CDs are determined by varying the input parameters for a physical model until the simulations agree with the actual measurements within acceptable error bounds. Since systematic errors caused by using inaccurate or overly simplified models directly influence the fitting of the model data to the measurement data, a comprehensive knowledge of possible sources of systematic errors is crucial to obtaining reliable results.

As in most applications, establishing a reasonable balance between model accuracy and time-efficiency is a complicated task. A well-established simplification is to model the intrinsically finite 3-D nanostructures as either periodic or infinite in one direction, reducing the computational expensive 3-D simulations to usually less complex 2-D problems. The effects of this simplification become more apparent with decreasing lengths of the structures. In this presentation we investigate these effects, and will report experimental set-ups, such as the used illumination numerical apertures and focal ranges, that can increase the validity of the 2-D approach.

We found that the introduced modeling errors strongly depend on the focus height, and that the approximation turns out the be better if we restrict the focal range. This also holds true for the second modeling error we investigated, errors due to the presence of line edge and line width roughness (LEWR). Similar to previous findings, we have observed that LEWR leads to a systematic bias in the simulated data. In scatterometry, an analytical expression for the influence of LEWR similar to a Debye Waller damping factor on the measured orders can be derived, and accounting for this effect leads to a modification of the model function that not only depends on the critical dimensions but also on the magnitude of the roughness. For finite arrayed structures however, such an analytical expression cannot be given. Nevertheless, a reevaluation of the used focal range can lead to a reduction of the influence of errors due to LEWR on the estimated CDs.

10145-51, Session 11

Scatterometry control for multiple electron-beam lithography

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In the past few years, several different alternative patterning strategies have been investigated. Some examples are Extreme Ultraviolet Lithography (EUVL), Directed Self-Assembly (DSA), Nanoimprint Lithography (NIL), Sidewall Image Transfer (SIT) and e-beam lithography. Each of these alternatives present their own specific advantages and challenges, many of which differ from the ones encountered with traditional optical lithography. While the industry has developed approaches to evaluate, monitor and control optical lithography processes, methods for the more recent alternative patterning strategies are still being developed. Example challenges among the alternative strategies include pitch walking for the SIT

method, residual resist underneath the pattern for NIL, and beam variation for e-beam lithography. Each of these challenges demands a metrology or inspection technique capable of meeting the specified requirements for monitoring and control. For e-beam lithography, beam variation can consist of changes or differences in beam dose and beam registration. In order to monitor and eventually control such variations, a non-destructive, high throughput, precise, and accurate metrology method is required.

Although scatterometry is commonly used in semiconductor development and manufacturing for measuring periodic structures that are often complex, it has also been shown to successfully measure patterning variation levels of non-periodic structures. This ability to detect undesired, non-periodic patterning variations across large regions (tens of microns across) makes scatterometry appealing for the detection of local patterning variability within a large array of e-beam-patterned structures.

The present work evaluates methodologies for monitoring e-beam dose and placement through the use of scatterometry measurements of innovative target designs. The targets are designed to mimic dose and registration variation in multiple e-beam lithography so that such variation can be monitored and minimized. The multiple e-beam tool used to expose the wafers is based at CEA-LETI and operates so that each electron beam patterns a stripe that is 2 microns wide. The film stack of the wafers used in this work consisted of patterned e-beam resist on top of an anti-reflective coating and a hard mask (Figure 1).

The scatterometry target array designed for this work is shown in Figure 2; controlled variations are induced inside the targets. The target array consists of four sections (VS, AS, VD, and AD) and has built-in DOE conditions: the rows (0 – 7) indicate the number of beams affected, while the columns indicate the magnitude of the shift in nm (for dose, the magnitude is converted to the equivalent change in nm). Figure 3 shows measured spectral variation for three of the targets within the VD array, where dose shift is varied. As expected, the spectral shift increases with the size of the dose shift and with the increase in the number of beams affected by the dose shift. Figure 4 displays measured “effective CD” values from each of the targets in the VD array, indicating that interpretation of the spectra also provides results that are sensitive to total dose change (magnitude of shift and number of beams). Top-down CD-SEM images, shown in Figure 5, qualitatively show that the CD of the resist lines decreases as the magnitude of the dose shift increases from 0 (Std_Ref) to 10 nm. In the paper, quantitative comparisons between the CD-SEM and scatterometry measurement will be shown. In conclusion, scatterometry is found to effectively measure local beam variations on the described targets, with the goal of multiple e-beam lithography monitoring and control.

10145-52, Session 11

Advanced optical modeling of TiN metal hard mask for scatterometric critical dimension metrology

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Titanium nitride (TiN) is widely utilized metal in semiconductor manufacturing. It has variety of applications such as gate material, metal hard mask, and diffusion barrier. Properties of TiN depend on its structure and composition. For instance, stoichiometric crystalline TiN is a good conductor and used as a diffusion barrier material, whereas amorphous or nitrogen deficient TiN is a very good insulator. In this paper we focus on optical properties and their relation to material characteristic of TiN hard mask , for advanced in-line production control in first metal levels of 22 nm FD SOI technology. Typical optical process control structure is illustrated in Figure 1. Optical dimensions such as the TiN thickness and middle CDs (critical dimensions) as well as ILD (interlayer dielectric) undercut need to be well controlled. We demonstrate that set up of accurate optical model for such stacks is non-trivial task due to the presence of highly absorbing film, namely TiN. Optical properties of thin-metal films vary with deposition conditions, surface oxidation/roughness and film thicknesses.

Furthermore, due to its high absorption TiN layer strongly affects the determined thicknesses of dielectric layers underneath. On the other hand, an accurate modeling might bring additional information related to important material parameters such as stress or resistance. Our findings are applicable to lower technology nodes where TiN is widely utilized as well. Also, proposed modeling methodology can be applied for TiN metal films in diffusion barrier and metal gate applications.

In order to model optical properties, TiN with various thicknesses has been deposited on ~1000 Å SiO2 grown on 300 mm Si wafer (Figure 3). Thin oxide was used for interference enhancement. Figure 4 shows obtained optical properties of TiN films with lower thicknesses and two different deposition conditions. Multi-oscillator Tauc-Lorentz model was used to fit the data. Thickness dependence of the optical properties (n&k’s) is clearly visible for both deposition conditions. Furthermore, extinction coefficient (k) clearly increases with thickness especially in red and near-infrared parts of the spectra (600-1000 nm). This area is related to Drude absorption. The Drude model describes ideal model of material resistance. Drude resistance can be indirectly link to film resistance. Thin metals show significant deviation form bulk optical properties up to 100 Å.4,5 However, in the control range of 125-225 Å we still observe thickness dependence that affects model output as shown in Figure 5. According to literature , the metal films transform into more granular form (tens of angstrom range) with decreasing thickness, therefore, their behavior deviates from bulk material. The optical conductivity depends on the capacitive coupling of the islands and thus increases with frequency. Below some thickness threshold, called percolation threshold, one can observe the metal-insulator transition (metallic behavior disappears). This results in abrupt decrease in real part of dielectric function due to Drude absorption. Different metals have different percolation threshold, for instance, for titanium it is equal to 25 Å.5, In practice, the optical properties of TiN need to be linked with specific process conditions, i.e., by using metal deposition zone diagram discussed in literature.2 Apart from thickness dependence on optical properties, two other factors influence TiN dispersion: surface oxidation/roughness and variability due to process conditions as also demonstrated in Figure 4. The surface roughness of metal films can be described using effective medium approximation (EMA).4 In this paper we discuss the TiN model that utilizes alloy model constructed with optical properties obtained for different thicknesses and additional EMA layer that approximate TiN roughness. We show that this approach significantly improves quality of scatterometric model. We discuss alternative metrics of model quality briefly described in Figure 6. We review Active Parameter Isolation (API) approach which further improves model accuracy and repeatability. Furthermore, we investigate the links between optical properties of TiN and fundamental manufacturing problems related to TiN hard mask technology such as mechanical stress.

10145-53, Session 11

Advanced applications of scatterometry based optical metrology

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This report is an overview of applications and benefits of using optical scatterometry for characterizing defects such as pitch-walking, overlay and fin-bending as well as characterizing patterned nano-structures of the gate-all-around nanowire devices (as seen in Fig. 1) for 7nm process technology. Currently, the optical scatterometry is based on conventional spectroscopic ellipsometry and spectroscopic reflectometry measurements, but generalized ellipsometry or Mueller matrix spectroscopic ellipsometry data provides important, additional information about complex structures that exhibit anisotropy and depolarization effects. In addition the symmetry-antisymmetry properties associated with Mueller matrix (MM) provide an excellent means of measuring and understanding any asymmetry present in the structure. The useful additional information as

well as symmetry-antisymmetry properties of MM elements is used to characterize fin-bending (as seen in Fig. 2), overlay defects (as seen in Fig. 3) and design improvements in the OCD test structures (as seen in Fig. 4), utilizing Nanometrics' ATOM® Target Design Suite, are used to boost OCD's sensitivity to pitch-walking.

10145-71, Session PWed

Overlay degradation induced by film stress

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The semiconductor industry has continually sought the approaches to produce memory devices with increased memory cells per memory die. One way to meet the increasing storage capacity demand and reduce bit cost of NAND flash memories is 3D stacked vertical flash cell array. In constructing 3D NAND flash memories, increasing the number of stacked layers to allow more memory cell number per unit area necessitates high aspect ratio etching processes accordingly thick and unique etching hard-mask scheme is indispensable. However, the ever increasingly thick requirement on etching hard-mask has made the film stress control extremely important for maintaining good process qualities. The residual film stress alters the wafer shape accordingly several process impacts have been readily observed across wafer, such as wafer chucking error on scanner, film stack peeling, materials coating/baking defects, critical dimension (CD) non-uniformity and overlay degradation.

This work investigates the overlay and residual order performance indicator (ROPI) degradation coupling with increasingly thick demand of C-contained etching hard-masks. Various C-contained hard-masks grown by chemical vapor deposition (CVD) method under different stage temperatures, chemicals combinations, radio frequency powers and chamber pressures were carried out. And -340Mpa to +80Mpa film stress with different film thicknesses were generated for the overlay performance study. The results revealed the overlay degradation doesn't directly correlate with convex or concave wafer shapes but film stress while increasing the C-contained hard-mask thickness will worsen the overlay performance and ROPI strongly. High-stress film was also observed to enhance the scanner chucking difference and lead to more serious wafer to wafer overlay variation. To reduce the overlay impact from ever increasingly thick etching hard-mask, optimizing the film stress of C-contained hard-mask is the most effective way, and high order wafer alignment and high order overlay compensation are also helpful.

10145-72, Session PWed

Normal and oblique incidence scatterometry for 2D/3D isolation mounts with RCWA and PML

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Scatterometry is capable of measuring the critical dimension and profile measurements of grating structures. It is possible to get down to approximately 8nm with high precision in semiconductor manufacturing process control. The quality of the measurement results depends on the setting groove model parameters, and the algorithms used by the analysis software. So, we develop the simulator to test the efficient parameter settings to raise the scatterometry's performance. In the Microlithography papers in 2004-2008, we completed the 3D-FDTD analysis of the arbitrary shapes for isotropic and anisotropic mediums. In Microlithography 2010-2012, we developed the scatterometry simulation software that has the spectroscopy calculation and optimization algorithm systems. We calculated the spectroscopy using the Rigorous Coupled Wave Analysis that provides a method for calculating the diffraction of electromagnetic waves by periodic grating structures. The Conjugate Gradient and the Binary-Coded Genetic Algorithm methods were used to automatically search data that matches the given spectrums. In 2013, we sped up the scatterometry simulation for the 3D RCWA by using the GPU and the CUda LApack. The 2D scatterometry simulator was improved by using a Real-Coded GA. In Microlithography 2014-2016, we examined the sensitivity of scatterometry for the 2D and 3D isolation mounts on the substrate by applying the Perfectly Matching Layer in the RCWA using normal and oblique incident beams. The RCWA is usually used for the period grooves and the scatterometry is now used for measuring the period groove shapes. However, by using the PML to absorb the outgoing waves from the interior of a period computational region for RCWA, we can analyze the scatterometry for the isolation mounts. We analyzed the reflectance from the silicon and resist single mount and the silicon double mounts on the silicon substrate by changing the mount's length, width and height for the single mount and the mount positions for the double mounts.

In this paper, we continue to examine the scatterometry's sensitivity for the 2D and 3D isolation mounts by changing the incident beam angles and applying the PML in the RCWA. We analyze the reflectance from the silicon/resist single mount on the silicon substrate and the several silicon/resist mounts on the silicon substrate by changing the mount's length, width, height and mount's positions for the several mounts. Here, the scatterometry characteristic is also examined for the trapezoidal shape mounts. First, we investigate the spot beam width dependences of reflectance. We also show the propagation properties of the electromagnetic fields propagating for the isolation mounts on the substrate. Then, we examine the reflectance for the TE and TM waves by changing the wavelengths and incident angles. And we examine the dependences between the incident angle and the sensitivity for finding small mount shape changes. Finally, the scatterometry simulator is developed for the isolation mounts using the Real-Coded Genetic Algorithm. The RCGA is used to automatically search the data which resembles the given spectrum and to get better fitting mount figures. Then, we understand the scatterometry observation is possible in several microns beam widths.

10145-73, Session PWed

Failure analysis metrology of semiconductor device using inline conductive AFM

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For the enhancement of yield, the amount of defects should be reduced and be detected at the early stage in fabrication steps. Specially, the detection and diagnosis of invisible defects such as junction leakage, crystal defect, and gate leakage, become a key factor for the yield of DRAM manufacturing. Currently, the most common method for non-destructive physical failure analysis in the semiconductor industry including DRAM is passive voltage contrast (PVC) method. This PVC method can easily perceive the leakage or abnormal contact with high resistance in DRAM structure. However, as the fabrication process of DRAM goes much finer to a nano-scale, the manufacturing parameters take extreme small values. Therefore, the PVC inspection is not enough sensitive to diagnose the failures in ultra-fine DRAM structures. We introduce the first in-line C-AFM system for surface resistive failure analysis in DRAM device fabrication. Specially, we focused on the self-aligned contact (SAC) process in DRAM fabrication, because the failure of SAC process is one of dominant factors which induce the degradation of yield performance and is the physically invisible defects in DRAM structures. We successfully suggested the accurate pass mark for resistive-failure screening in the fabrication of SAC structures and established that the cause of SAC failures is the bottom silicon oxide layer. Through the accurate pass mark for the SAC process configured by the in-line C-AFM analyses, we secured a good potential method for preventing the yield loss caused by failures in DRAM fabrication.

10145-74, Session PWed

Adaptive filtering schemes for data estimation in process control for microlithography

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In recent years, data processing is an important topic in control systems and advanced control technology for microlithography, and has become more and more complicated. The main purpose of the proposed Kalman-based scheme is to suppress noise, preserve data details, and have low computational complexity. The Kalman filtering, also known as linear quadratic estimation (LQE), is an efficient recursive filtering algorithm that estimates the internal state of a linear dynamic system from a series of noisy measurements. Additionally, it is used in a wide range of engineering and econometric applications from radar and computer vision to estimation of structural macroeconomic models. In this paper, we use an adaptive Kalman-based filtering scheme to tracking the dynamic (non-stationary) channel. The development of the Kalman-based scheme is addressed under the full channel state information (CSI). The Kalman-based recursive scheme plays an important role on the time-varying (t.v.) data estimation and analysis based on the minimum mean square error (MMSE) criterion in order to seize out the best data estimation. The best data estimation means that low data error rate and good performance. Simulation results demonstrate the superior data error rate of the Kalman-based technique for the multiple-input multiple-output channel model, and compare to the really full-information data channel.

10145-75, Session PWed

Scanning electron microscope automatic defect classification of process induced defects

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With the integration of high speed Scanning Electron Microscope (SEM) based Automated Defect Redetection (ADR) in both high volume semiconductor manufacturing and Research and Development, the need for reliable SEM Automated Defect Classification (ADC) has grown tremendously in the past few years.

In many high volume manufacturing facilities and research and development operations, defect inspection is performed on E-Beam, Bright Field or Dark field defect inspection equipment. A text file is created by the defect inspection tool. The defect inspection result file contains a list of the inspection anomalies detected during the inspection tools examination of each structure, contained in each die, of the wafer. The text file created based on the inspection results of the inspection tool is imported into the Defect Review Scanning Electron Microscope (DRSEM). Following the defect inspection result file import, the DRSEM automatically moves the wafer to each defect die coordinate and performs ADR. During ADR the DRSEM may operate in a reference mode, capturing a SEM image at the exact position of the anomalies die coordinates and capturing a SEM image of a reference die at the same exact in-die coordinates. A reference image is created based on the Reference Die minus the Defect Die. The exact coordinates of the defect are calculated based on the calculated defect position and a high magnification SEM image is captured. The captured SEM images are process through either DRSEM ADC binning, exporting to a Yield Analysis System (YAS), or a combination of both. Process Engineers, Yield Analysis Engineers or Failure Analysis Engineers will manually review the captured images to insure that either the YAS defect binning is accurately classifying the defects or that the DRSEM defect binning is accurately classifying the defects.

This paper is an exploration of the feasibility of using the Hitachi RS6000 Defect Review SEM to perform Automatic Defect Classification with the objective of the total automated classification accuracy being greater than human based defect classification binning when the defects do not require multiple process step knowledge for accurate classification.

The integration of DRSEM ADC has the potential to improve the response time between defect detection and defect classification. Faster defect classification will allow for rapid response to yield anomalies that will reduce the die yield.

10145-76, Session PWed

Process resilient overlay target designs for advanced memory manufacturer

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In recent years, lithographic printability of overlay metrology targets for memory applications has emerged as a significant issue. Lithographic illumination conditions such as extreme dipole, required to achieve the tightest possible pitches in DRAM pose a significant process window challenge to the metrology target design. Furthermore, the design is also required to track scanner aberration induced pattern placement errors of the device structure. Previous work, has shown that the above requirements have driven a design optimization methodology which needs to be tailored for every lithographic and integration scheme, in particular self-aligned double and quadruple patterning methods. In this publication we will report on the results of a new target design technique and show some example target structures which, while achieving the requirements specified above, address a further critical design criterion – that of process resilience.

Process resilience is defined as the ability of a metrology structure to minimize the process induced bias in the wafer center to edge dependence of the modeled overlay terms and model residuals. The center to edge metric is selected since overlay control at the wafer edge is one of most challenging problems faced in DRAM HVM today. In a nutshell, process resilient target designs are achieved by reducing the minimum open space in the target structure in order to be compatible with advanced CMP and etch manufacturing design rules.

Additionally, this publication will explore the sensor architectural changes required to maintain metrology performance while measuring process resilient target structures. In particular, the reduced open space on process resilient targets results in a concomitant contrast reduction. Therefore we will report on the effect of new metrology sensor capabilities, specifically polarized illumination, extended spectral range and increased light source brightness on metrology performance in measurements of these new target design structures when implemented on the tightest pitch alignment schemes of advanced design rule DRAM layers.

10145-77, Session PWed

Asymmetry overlay correction for lithography processes

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Overlay control for semiconductor devices is getting tighter in recent years. In the past, we may only concern the whether the overlay are in spec or not. However, the spec we concerned was the same for both X and Y directions. To achieve the tighter spec in the future, we may consider the asymmetry specs for X and Y directions separately for some specific layers,

such as CONT layer. For example, if the spec of X direction is tighter than Y direction, we can lose the precision of overlay from Y direction to let overlay from X direction more precise. Theoretically, the common overlay models such as HOPC or iHOPC set X and Y directions independently. To reach the goal of loss overly from one direction to preserve the overlay from the other direction, we consider the full map measurement overlay historical data. From these data, we can analyze the data to find which overlay targets are more important to X direction, and we can set these corresponding targets as the new measurement locations. This is one concept of "asymmetry" since the chosen measurement locations can provide more precisely correction for the overlay of specific direction. On the other hand, we use the in spec ratio (ISR) index for all measurement overlay targets on wafer to replace the traditional mean plus 3 sigma (M3S) index, since we have the budgets of both X and Y directions. The in spec ratio is defined as ratio that the residuals of X and Y directions fill the corresponding budgets, simultaneously. Since our goal is to maximize the ISR, the traditional M3S optimization algorithm can be replaced by ISR optimization with different overlay specs. That is the reason we call "asymmetry overlay correction".

10145-78, Session PWed

A hybrid overlay technique using computational prediction and measured data to accurately determine process corrections with reduced sampling

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Reducing overlay error via an accurate APC feedback system is one of the main challenges in high volume production of the current and future nodes in the semiconductor industry. The overlay feedback system directly affects the number of dies meeting overlay specification and the number of layers requiring dedicated exposure tools through the fabrication flow. Increasing the former number and reducing the latter number is beneficial for the overall efficiency and yield of the fabrication process.

An overlay feedback system requires accurate determination of the overlay error, or fingerprint, on exposed wafers in order to determine corrections to be automatically and dynamically applied to the exposure of future wafers. Since current and future nodes require correction per exposure (CPE), the resolution of the overlay fingerprint must be high enough to accommodate CPE in the overlay feedback system, or overlay control module (OCM). Determining a high resolution fingerprint from measured data requires extremely dense overlay sampling that takes a significant amount of measurement time. For static corrections this is acceptable, but in an automated dynamic correction system this method creates extreme bottlenecks for the throughput of said system as new lots have to wait until the previous lot is measured.

One solution is using a less dense overlay sampling scheme and employing computationally up-sampled data to a dense fingerprint. That method uses a global fingerprint model over the entire wafer; measured localized overlay errors are therefore not always represented in its up-sampled output. This paper will discuss a hybrid system shown in Fig. 1 that combines a computationally up-sampled fingerprint with the measured data to more accurately capture the actual fingerprint, including local overlay errors. Such a hybrid system is shown to result in reduced modelled residuals while determining the fingerprint, and better on-product overlay performance.

10145-79, Session PWed

Monitoring of 450mm copper seeding and plating process via SSIS haze

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This study explores the feasibility of utilizing the high throughput, non-destructive surface scanning inspection system (SSIS) to monitor the quality of the copper seeding and electroplating process on 450mm wafers. Currently copper grain size and surface quality is measured by atomic force microscope (AFM). While the AFM provides high resolution information down to 1 μm2, it is highly time intensive with the inspection of a single wafer taking up to 20 minutes. The SSIS in this study provides fast full wafer surface roughness information in 450μm x 450μm blocks.

This paper will also investigate the advantages of identifying wafer level process variation of the copper film deposition with the SSIS versus sampled points of AFM inspection. With full wafer surface roughness information it may be possible to find a commonality between the quality of the copper electroplating process and the haze information of the copper seeding wafer.

10145-80, Session PWed

Application of advanced diffraction based optical metrology overlay capabilities for high-volume manufacturing

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On-product overlay requirements are becoming more challenging with every next technology node due to the continued decrease of the device dimensions and process tolerances. Therefore, current and future technology nodes require demanding metrology capabilities such as target designs that are robust towards process variations and high overlay measurement density (e.g. for higher order process corrections) to enable advanced process control solutions. The impact of advanced control solutions based on YieldStar overlay data is being presented in this paper.

Multi patterning techniques are applied for critical layers and leading to additional overlay measurement demands. The use of 1D process steps results in the need of overlay measurements relative to more than one layer. Dealing with the increased number of overlay measurements while keeping the high measurement density and metrology accuracy at the same time presents a challenge for high volume manufacturing (HVM). These challenges are addressed by the capability to measure multi-layer targets with the recently introduced YieldStar metrology tool, YS350. On-product overlay results of such multi-layers and standard targets are presented including measurement stability performance.

10145-81, Session PWed

EPE analysis of sub-N10 BEOL structures with Coventor's SEMulator3D

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Semiconductor process modeling software has become an indispensable tool for developing new integration approaches. Visualization of complex 3D structures and budget analysis on film thickness, CD and etch budgets allow process integrators to create flows before any physical wafers are run. Once early data is available from real wafers, the virtual process flow can incorporate observed effects and be used to make more specific comparisons. Coventor's SEMulator3D® process modeling software is used along with observed data on imec's iN10 BEOL M1-M2 process to make several comparisons. SEMulator3D is run in a batch mode to simulate running hundreds of virtual wafers and compares the effects of running with different overlay schemes, differences between EUV and DUV and between different design approaches. Edge placement errors(EPE) leading to device characteristic changes are modeled for different patterning schemes.

In the figure 1, below, we show the estimated yield by running Monte-Carlo simulations on the same clip by two different patterning approaches, AL1 (where M1B, M1C, V0A and V0B align to M1A) and AL2 (where M1A, M1B, M1C align to M0). In figure 2 we use a screen limit of 70% to determine whether a contact fails or not. Trends are different depending on alignment schemes and circuit design. Kerf structure is less sensitive than logic structure (logic structure fails more often). Considering alignment schemes is also not trivial. In this specific case the AL2 scheme fails more frequently than the scheme at any yield limit. We can also use this to back-calculate the spec limits which must be met to have a yield greater than 99%.

Furthermore, by using the resistance/capacitance modeling capability of SEMulator3D, predictions on eventual electrical behavior are also made. Parametric yields and limited yields are used to compare the different process/design approaches, as is typically done in evaluating real wafer data.

10145-82, Session PWed

Verification methodology of retarget value accuracy using pattern library

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We must ensure the targeting accuracy of pattern for semiconductor implementation of good quality. If metal contact pattern which has target size of same width distributed in Chip is measured width size, its result actually has various values. At this time, we compensate retarget value that pattern with the same target has the same size. Likewise, compensating retarget value is to find out what factors influence to targeting and each factor needs a process which identifies how much compensation requires. To extract each factor in main chip is so difficult. Because, in main chip various factors are mixed in pattern. Therefore, it is difficult to figure out whether the factor has an influence or not about one factor and it is also difficult to extract accurate retarget value about the factor. Thus, we have created Pattern Library which one factor can separate from mixed factors and made pattern group to show an influence of only one factor.

Our experiments were conducted in 6 steps. Step1: Pattern library conception, we expect to affect width size targeting of metal contact pattern Here, we have considered six different factors. Next, after selecting a single factor and fixing the rest of environments, we create pattern group to split application values on the factor. The remaining factors also make pattern group to split in the same way.< Fig.1> Step2: Pattern library implementation, we produce reticle applied pattern library planned in Step1, and it has be patterning in real wafer. Step3: Measuring set-up of pattern. We used NGR(Nano Geometry Research) as a tool to compare size that has pattern in wafer and layout designed pattern library. NGR is a tool machine used Data Based Matching System which offers massive data. We must prepare GDS file to use matching and set measurement area. Step4: Pattern measurement using NGR, we measure width size of split group contact based on GDS in wafer carried out pattern library. Step5: Data processing, we calculate between skew value extracted width target size and measured size of each split pattern. By this result, we are able to find out that width size of contact is how close to the target.< Fig.2> Step6: Verification and outcome, we determine which factors influence targeting, if one factor affects, we have to identify any trends visible. We can present retarget value by making Rule table integrated factors that affect targeting based on this result.< Fig.3>

Our experiment find out length size and contact to contact space are the reasons to affect width size targeting of contact and according to this, we can suggest retarget value in section. Our experiment method gives it possible to accurately grasp the effects of each factor independently by creating pattern library and separating one by one that mixed in main chip. Also, as mentioned above, we were able to enhance completeness and accuracy of the results analyzed lots of data through using NGR tool. Through this experiment, we not only enhance accuracy of retarget value but also expect to propose a direction of weak layout.

10145-83, Session PWed

Enhanced 28nm FDSOI diffraction based overlay metrology based on holistic metrology qualification

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Continuous tightening of overlay control budget in semiconductor industry drives the need for improved overlay metrology capabilities. In this context, measurement accuracy needs to be address. In the first part this study shows that Diffraction Based Overlay metrology accuracy can be improved with a dedicated methodology. This methodology involves the use of target design simulation software in order to maximize stack sensitivity and to minimize processes non uniformities impacts on measurement. It will be shown that accurate stack settings (n, k, thicknesses etc ...) are critical. Simulation results are compared to experimental results. In the second part this study focuses on Holistic Metrology Qualification methodology that allows selecting the best on-wafer target. The methodology is explained and discussed. It is demonstrated that HMQ helps to reduce target asymmetry impact on uncertainty measurement and to select primary recipe parameters (wavelength, polarization, etc...). Finally CD-SEM measurements were used to validate methodology results.

10145-84, Session PWed

New alignment mark design structures for higher diffraction order wafer quality enhancement

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In IC manufacturing process, wafer alignment is one important characteristic to ensure the accurate alignment and reduce the overlay between different layers. In some wafer process, special opaque film stacks with strong absorption of detective light was selected for very high etch resistance purpose, which resulting in seldom diffraction light. As a result, no alignment mark is detectable to scanner. Thus, one important parameter during wafer alignment is the diffraction light power, especially the higher odd-order diffraction light power, which gives more accurate for alignment. Process engineers usually use wafer quality (WQ), the normalized diffraction light power, to characterize and compare different wafer alignment strategies. Normally, larger WQ of diffraction light gives more robust of alignment. So, it is recommended to optimize the thickness of film stacks and structures to achieve a higher WQ of high odd-order diffraction light.

Right now, the widely used wafer alignment marks are ASML AH53 and AH74 in industry. We optimized and designed new alignment marks based on these two structures to enhance the odd-order diffraction light WQ. The

structures of each grating period of AH53 and AH74 are seen in Fig. 1(A) and Fig.1(B). As comparison, the new designed alignment structures of one grating period are plotted in Fig.1(C) and Fig.1(D). New alignment marks have obviously WQ improvement of odd-order diffraction light.

In order to quickly calculate the WQ of different film stacks and alignment mark structures, we wrote a WQ calculation software as seen in Fig.2. Fourier optics is used for the physical model as it has relative accuracy when the minimum width of alignment mark is larger than or similar with the detective wavelength. Using the software, we calculate WQ of a simple bare silicon wafer stack. All alignment marks and 0th to 7th WQs are shown in the interface. The result shows new alignment marks have higher odd-order WQ, especially AMM7_2 which has more than 50% improvement of 7th WQ comparing with AH74.

The purpose of the new designed alignment marks is applied these structures to real optical alignment. User defined alignment mark can be accept of ASML SMASH alignment system, but a self reference interferometer should be used. That is, mark type configuration file should be defined and added into the system to ensure each diffraction order light can be determined separately. At present, we are writing the mark type configuration file. The experimental results will be shown in the text soon after. Moreover, we believe these new designed structures can improve the wafer alignment performance of some key layers or special film stack applications.

10145-86, Session PWed

High-throughput and dense sampling metrology for process control

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No Abstract Available.

10145-87, Session PWed

Efficient hybrid metrology for focus, CD, and overlay

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Since the introduction of multi-patterning techniques in semiconductor industry, metrology has become more and more of a burden. With multiple patterning techniques such as Litho-Etch-Litho-Etch and Sidewall assisted double patterning the number of processing steps has increased enormously and therefore so have the amount of metrology steps needed for both control as well as yield monitoring. The amounts of metrology needed is increasing node over node as more and more layers need multiple patterning steps as well as more patterning steps per layer. In addition to this there is the need for guided defect inspection, which in itself requires substantially denser focus, overlay, and CD metrology as before. Metrology efficiency will therefore be crucial to the next semiconductor nodes.

ASML's emulated wafer concept offers a highly efficient method for hybrid metrology of focus, CD, and overlay. In this concept metrology is combined with scanner sensor data in order to get to predictions of on-product performance. The principle underlying the method is to isolate and estimate individual root-causes which are then combined to predict the on-product performance. The goal is to use all information available to avoid ever increasing amounts of off-line metrology.

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10145-88, Session PWed

CDC-ratio prediction using OPC model for WLCDU improvement in memory devices

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The WLCDU (Wafer Level CD Uniformity) of semiconductor devices become more important than ever because of the small technology node. Local Intra-field CDU variation on wafers can be arisen from various reasons, but the main reason is mask CD uniformity. As a result of this, CDC (Critical Dimension Control) technology has been adopted for several years to improve WLCDU by making partially scattered pixles in the mask. However, it is still difficult to decide how much attenuation should be applied into the quartz to meet the CD target without additional fabrication of the test reticles. Because measuring mask CD uniformity before and after CDC can not reflect WLCD change from CDC process, in other words, the defect density of CDC and wafer CD change from it, which is CDCR, is not constant. The applied blurring in the mask and its effect on wafer CD are varied according to the illumination condition of scanners and photo-resist on wafers.

In this work, we used OPC model for predicting the relationship between the applied amount of attenuation and WLCD change. OPC model can be a good link between defect density of the mask and wafer CD drift, because it include informations about illumination conditions of a scanner and photo resist on wafers. To prove our theory, we compared our simulated results with the data from 1x DRAM and NAND Flash devices using half tone PSM (Phase-Shift Mask) in both case of dark tone and clear tone.

10145-89, Session PWed

Reducing the overlay metrology sensitivity on perturbations of the measurement stack

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Overlay metrology setup today is done in a continuously changing landscape of process steps. In order to be able to cover the full process window many different types of target designs are evaluated. Default methods of overlay metrology setup consist of single-wafer optimization, evaluating the performance of all available metrology targets. Without the availability of external reference data or multi-wafer measurements it is difficult to predict the metrology accuracy and robustness against process variations which naturally occur from wafer-to-wafer and lot-to-lot.

In this paper, we will outline the capabilities of the Holistic Metrology Qualification (HMQ) setup flow, in particular with respect to overlay metrology accuracy and process robustness. The significance of robustness and its impact on overlay measurements will be discussed

using multiple examples. Improvements of the overlay metrology setup flow are incorporating an overlay sensitivity check on perturbations of the measurement stack such as grating imbalance. This measurement error caused by process asymmetry coming from slight stack variations across the target, in the order of nm, is dependent on the metrology target environment. The micro-scale variation can cause errors in the overlay calculation in the order of nanometers in case the recipe and target have not been selected properly.

An extensive analysis on Key Performance Indicators (KPIs) from HMQ recipe optimizations was performed on uDBO targets on product wafers from variety of layers and devices. The top key parameters (preset) for recipe/target combination accuracy and process robustness performance ranking were identified, which can be applied for a wide range of applications, independent of layers and devices.

10145-90, Session PWed

Further study on overlay AEI-ADI shift on contact layer of advanced technology node

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As semiconductor integrated circuit industry has been driven into advanced technology node (28nm, 14nm, etc.), the device CD (Critical Dimension) is getting smaller, therefore the overlay budget control is more and more tightened and crucial for device performance and yield guarantee. Understanding overlay AEI-ADI (AEI: After Etch Inspection; ADI: After Develop Inspection) shift is extremely important, because it is the basis for using overlay ADI result to control lithographic process into final satisfactory AEI outcome. In our previous 2016 SPIE paper: Study on Overlay AEI-ADI Shift on Contact Layer of Advanced Technology Node (Proc. of SPIE Vol. 9778 97782C-1), we studied an OVL (Overlay) AEI-ADI shift issue and did series of experiments and analysis, then finally provided a model of "stress-induced PR tilt" (PR: Photo resist). As a continued effort in the study, recently, we have some new findings, as follows: In some other cases, even after eliminating stress issue on hard mask deposition, the overall OVL AEI-ADI shift map (Figure 2 in our previous SPIE paper mentioned above) and OVL AEI-ADI shift intra-shot map (Figure 3 in our previous SPIE paper mentioned above) still exists. For these cases, an experiment split of enlarging the exposure sigma at photo stage, the overall upper-right-directional ADI-AEI shift vanishes. The center-edge difference of the OVL AEI-ADI shift intra-shot map is also gone. This single experiment split indicates that there could exists some residual coma that induces the PR profile asymmetry (PR tilt) which could finally lead to the AEI-ADI OVL shift. We did more experiments and simulations to verify the role of coma in inducing the unwanted PR profile. We also explain how the intra-shot center-edge difference (Figure 3 in our previous SPIE paper mentioned above) is caused under the residual coma. The results of our study will be presented and discussed in this paper.

10145-93, Session PWed

MFIG: a vacuum-contamination sensor for yield enhancement

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To produce high-end products, clean vacuum is often required. Even small amounts of high-mass molecules can reduce product yield. For example, a sub-monolayer of contaminant molecules can affect atomic-layer-deposition by obstructing full surface-coverage by the ALD precursor. The resulting pinholes in the ALD layer may cause early failure of the final product. The challenge is to timely detect the presence of relevant contaminants. Here is where MFIG can help. The mass-filtered ion gauge sensor (MFIG) continuously and selectively monitors the presence of high-mass contaminant molecules with a sensitivity down to 10E-13 mbar at total pressures up to 10E-5 mbar.

TNO's development of MFIG started in 2007, when experts realized that IC manufacturing with EUV needs extremely clean vacuum, while existing sensors are either too slow, expensive or insensitive for real-time monitoring of vacuum cleanliness. The promising results of a "quick-and-clean" test were well-received at the AVS fall meeting in 2008. Hence TNO incubated the concept in an EU project, in which both instrumentation was improved and application requirements were clarified by interacting with the consortium partners. In 2015 TNO has been awarded an NanoNextNL valorization grant to further mature the instrumentation for sensitivity selectivity and cost, as well as to collect field test data to validate MFIG's value in realistic usage conditions.

This contribution presents laboratory and field-test data to demonstrate the capabilities of the latest MFIG sensor in continuously and selectively detecting high-mass contaminant molecules in (U)HV vacuum.

10145-94, Session PWed

CD uniformity control for thick resist process

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In order to meet the increasing storage capacity demand and reduce bit cost of NAND flash memories, 3D stacked flash cell array has been proposed. In constructing 3D NAND flash memories, the higher bit number per area is achieved by increasing the number of stacked layers. Thus the so-called "staircase" patterning to form electrical connection between memory cells and word lines has become one of the primarily critical processes in 3D device manufacture. To provide controllable CD with good CD uniformity involving thick photo-resist has also been of particular concern for staircase patterning.

The study on CD uniformity improvement has been widely conducted with relatively thinner resist associated with resolution limit dimension but thick resist coupling with wider dimension. This study explores CD to exposure dose sensitivity, within-wafer CDU and line edge roughness associated with photo-resist pattern profile of microns thick resist processing. Several critical parameters including exposure focus, exposure dose, baking conditions, pattern size and development recipe, were found to strongly correlate with the thick photo-resist profile accordingly affecting the CD uniformity control. To minimize the within-wafer CD variation, the slightly tapered resist profile is proposed through well tailoring the exposure focus and dose. Great improvements on ADI and AEI CD uniformity as well as line edge roughness were achieved through the photo resist profile optimization.

10145-95, Session PWed

Traceable measurement and pitch analysis of a laser focused Cr nano-grating

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The laser focused atomic deposition offers a novel method to fabricate pitch standards for the calibration of scanning probe microscopes (SPMs), because the nano-grating is directly traceable to the standing laser wavelength. Highly parallel and uniform Cr nano-grating covers a millimeter-sized area with pitches at nano-scale, which satisfies the length calibration application at trans-scales in micro-metrology and nano-metrology. When the collimated Cr atoms with laser cooling pass through a near-resonant laser light, an induced dipole force on the Cr atoms interacts with the laser to impose a force toward the nodes or antinodes of the standing wave. As a result, the deposited periodic nano-grating has a high accuracy with half of the laser wavelength, which is ideal for the application of a

length calibration standard for SPMs. A Cr nano-grating sample made by laser focused atomic deposition (Sample No.TJ070113) was measured by the Traceable atomic force microscope (T-AFM) at National Institute of Standards and Technology (NIST). As a traditional method to evaluate the 1D nano-gratings, the gravity center (GC) method extracts the gravity center of each nanostructure. Compared to the Fourier transform methods which may contain a theoretical calculation error because of spectrum broadening, the GC data evaluation analysis is real and reliable because the results are based on the real structure profiles measured by the scanning probes. Based on the pitch analysis study with GC method, it's obvious that the Cr nano-gratings have a highly parallel structure with an accurate and uniform mean pitch. Half of the wavelength (λ/2) is 212.775 nm, while the mean pitch of sample No.TJ070113 is 212.76±0.01 nm at 10μm scale. At 5μm and 20μm scale, the mean pitches are 212.74±0.03 nm and 212.73±0.01 nm, respectively; and the relative uncertainty of the measurements is better than 1.5x10-4. The mean pitch at 5~20μm scale range demonstrates a high uniform and parallel characteristics, which indicates that laser focused Cr nano-gratings are very suitable to be reference standards for length calibration for scanning probe microscopes.

10145-96, Session PWed

Enhanced methodology of focus control and monitoring on scanner tool

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In this paper, Diffraction Based Focus (DBF) metrology enabling accurate, fast, and non-destructive focus acquisition, has been successfully utilized for focus monitoring/control of TWINSCAN NXT immersion scanners. The optimal DBF target with minimized dose crosstalk, dynamic precision, set-get residual, and lens aberration sensitivity was obtained by the possibility of DBF target selection. By exploiting this new measurement target design, >50% improvement in run-to-run mean focus stability has been demonstrated compared to the previous BaseLiner strategy on Zebra target. Matching <5nm across multiple NXT immersion scanners has been achieved with the new methodology of set baseline reference control. This baseline technique, with either conventional BaseLiner low numerical aperture (NA) mode or advanced illumination high NA mode (NA=1.35), has also been evaluated to have consistent performance. This enhanced methodology of focus control and monitoring on multiple illumination conditions, opens an avenue to significantly reduce Focus-Exposure Matrix (FEM) wafer exposure for new product/layer best focus (BF) setup.

10145-97, Session PWed

Wafer-shape based in-plane distortion predictions using Superfast 4G metrology

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With the latest scanners performing at the sub-2-nm overlay level, the On-Product-Overlay (OPO) budget is more and more determined by non-lithography contributors. Examples of these process-induced overlay errors can be etching, thin film deposition, Chemical-Mechanical Planarization (CMP) and thermal annealing. These processes have in common that they could lead to stress (changes) in the thin films on top of the silicon wafers. Variations in these film stresses can result in significant non-linear wafer grid distortions that can be as high as 20 nm and cannot be corrected for by linear alignment. The ASML solution for correcting these higher-order Lot-to-Lot (L2L) and Wafer-to-Wafer (W2W) overlay variations is Higher Order Wafer Alignment (HOWA). Currently, HOWA models are successfully applied in high volume manufacturing (HVM) at several customers to reduce process-induced W2W overlay variation levels down to 0.5-nm. However, these performance levels can only be met when certain preconditions are fulfilled. Firstly, the wafer alignment markers should not be damaged by etching and/or CMP. Secondly, the application of these polynomial-based models is effective for correcting global wafer grid distortions whereas their correction capability might fail when local grid distortions play a role, for instance as a result of non-uniform wafer processing.

In order to overcome the issues mentioned above, we have investigated the possibility to perform overlay corrections based on wafer-shape metrology using the Superfast 4G system. Thin film stress and variations in there will typically have an impact on the unclamped shape of the wafers. When a relationship between the wafer shape and the in-plane distortion (IPD) after clamping is established then feed-forward overlay control can be enabled. To this end, we have set up a controlled experiment using scanner calibration wafers. These are bare silicon wafers with a large number of alignment markers etched with a well-defined depth into the silicon. By conformal, homogeneous deposition of nitride, umbrella- and bowl-shaped wafers have been created. On some splits, additional dry etching is applied to remove the nitride again from the edge fields to create local stress changes. The wafers are measured on the scanner using the SMASH alignment system before and after wafer processing, and by subtracting the two alignment fingerprints measured, the process-induced grid distortion can be isolated from scanner and wafer contributions. Similarly, the processing-induced wafer shape change is obtained by Superfast 4G measurements.

We will show that homogeneous nitride deposition results in a unique grid distortion fingerprint in the wafer edge region. From the measured wafer shape change and by taking into account the wafer table design, we are able to explain and predict this edge distortion fingerprint. Furthermore, we show that removal of the nitride deposited on the edge fields leads to localized grid distortions in the inner fields. Using an advanced distortion feed-forward model, we are able to accurately predict the measured in-plane distortion from the wafer shape measurements. From this we conclude that wafer-shape based overlay corrections are a promising method for reducing process-induced overlay errors.

10145-98, Session PWed

Monitoring of multi-patterning processes in production environment

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In leading edge semiconductor industry using multi patterning processes (e.g. QADP) became popular in the last years. The main reason is that with multi patterning the shrinking ground rules can be supported in an effective way. The goal is to have a good uniformity of the created pattern over the wafer.

One concern is that the different involved lithography steps, trim steps, deposition steps and etch steps are interacting. For instance, on the one hand, the initial lithography steps can be almost perfect. But a variation in the CD after the trim process will cause a variation in the CD after the spacer deposition. That leads to a non-uniformity effect in the created pattern. There are spacer sensitive and lithography sensitive CD lines and spaces.

Monitoring and controlling the individual CD parameters is not sufficient to ensure a stable process for multi patterning. New key performance indicators (KPI) have to be defined, for instance imbalance metrics, which take all contributions into account.

Therefor we are presenting a new way to define and monitor KPI's, based on the CD data. We enable the setup of process specific KPI's, using detailed measurement data and combining them. To get more sensitivity in the KPI, we also use historical data and combine them with the current data. That compensates effects of measurement uncertainty and removes noise.

The method is applied in a real production environment to establish a very efficient and reliable monitoring. We were able to discover clear trends over the time, excursions and signatures over the wafer surface that could not be detected with traditional metrics.

10145-99, Session PWed

Process control using adaptive matrix-form affine projection filtering algorithm

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Data processing means process post-treatment and data analysis technology effectively. In recent years, there are more requirements in data processing, and had become more and more complicated. The sensors in wireless sensor networks (WSNs) contain one antenna element in each single device. To effectively lower the power consumption of each sensor node, the cooperative wireless sensor networks have been proposed. The virtual antenna array composed by WSNs nodes constructs a virtual multiple-input multiple-output (VMIMO) system which can reduce significantly the transmission power consumption between the nodes and achieve the transmission quality and data rate in MIMO system. A VMIMO architecture allows cooperatively data exchange among each node in a sensor network. In order to solve the problems caused by VMIMO, we use a method of set-membership filtering (SMF) design in the Affine Projection adaptive algorithms to improve the convergence rate and alleviate the complexity of the scalar-form Affine Projection. Simulation results show that the SMF is able to reduce the computational complexity effectively and achieves a better system performance.

10145-100, Session PWed

Improved multi-beam laser interference lithography system by vibration analysis model

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Laser interference lithography (LIL) is a fabrication process for patterning micro or nano structures. Because the advantages of maskless, simple optical setup, low cost, infinite depth of focus, and large area patterning in single exposure, LIL is one of the most suitable technique to fabricate periodic structure such as gratings, nanowires, and photonic crystals.

Our lab has developed a multi-beam LIL system and successfully fabricated 2D period structures. However, due to the working principle, LIL system is very sensitive to the light source and the vibration. When there is a vibration source in the exposure environment, the standing wave distribution on the substrate will be affected by the vibration and move in a certain angle. As a result, Moire fringe defects occur on the exposure result.

In the environment, there not be avoided vibration, such as fan of laser cooling, fan filter unit of clean room, those rotational speed are about 1000-3000rpm estimation 17-50 Hz. that need to maintain ideal laboratory and experiment.

In order to eliminate the effect of the vibration, this paper use the software ANSYS to analyze the resonant frequencies of our LIL system. Therefore, we need to design new multi-beam LIL system to raise the value of resonant frequencies. On the original LIL multi-beam LIL system, the first and second modes of resonant frequency are about 28Hz, 60Hz respectively. Both these two resonant frequencies are low and could exist in the exposure environment. The first mode resonant frequency caused the system bending back and forth. And the second mode resonant frequency caused the system rotating in horizontal direction. Both these vibrations might cause the Morie fringe defect.

On the ANSYS simulation result of the improved LIL system, the result shows that significant improvement of the resonant frequency. The first mode resonant frequency is about 84 Hz and the second mode is about 135 Hz. Which is much higher than the original design. And the bending and rotating effect is reduced. A “X” shape support can further improve the system. But we chose the tilt support due to the convenience of system setup and adjustment.

This paper design a new LIL system to improve the multi-beam LIL system in our lab. We used the ANSYS software to analyze the resonant frequencies of the LIL system. The new design of the LIL system has higher resonant frequencies and successfully eliminate the bending and rotating effect of the resonant frequencies. As a result, the new LIL system can fabricated large area and defects free period structures.

10145-101, Session PWed

Numerical investigation of measurement characteristics of through-focus scanning optical microscopy (TSOM) measures under focused Gaussian beam illumination

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We investigate a method for enhancing the capability of inspection and metrology of a through-focusing optical microscope (TSOM) with Fourier modal method (FMM), also referred to as Rigorous Coupled-Wave Analysis (RCWA), based numerical modeling. Our main finding is that the use of tightly-focused Gaussian beam can effectively enhance the major measures of TSOM as optical intensity range (OIR), metric value (MV), and mean square difference (MSD) from a few to hundreds times. Possible performance enhancement for conventional target structures is quantified for various illuminating Guassian-beam conditions.

10145-102, Session PWed

A pattern-based method to automate mask inspection files

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Mask inspection is a critical step in the mask manufacturing process in order to ensure all dimensions printed are within the needed tolerances. In addition to the mask quality, there is a significant amount of manpower needed when the preparation and debugging of this process are not automated. As a time-critical part of the manufacturing process we wish to 1) reduce the data preparation cycle time, 2) minimize the amount of manual/human error in naming and measuring the various locations, 3) reduce the risk of wrong/missing CD locations, and 4) reduce the amount of manpower needed overall.

By utilizing a novel pattern search technology with the ability to measure and report match region scanline (edge) measurements, we can create a flow to find, measure and mark all metrology locations of interest and provide this automated report to the mask shop for inspection. A digital library is created based on the technology product and node which contains the test patterns to be measured. This paper will discuss how these digital libraries will be generated and then utilized.

We will also review and example pattern and how the reporting structure to the mask shop can be processed. This entire process can now be fully automated.

10145-104, Session PWed

SAQP pitch walk metrology using single target metrology

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Self aligned quadruple patterning (SAQP) processes have found widespread acceptance in advanced technology nodes to drive device scaling beyond the resolution limitations of immersion scanners. In these processes one lithographically defined line feature is split into a total of 4 final line features. Of the four spaces generated in this process two tend to be equivalent as they are derived from the first spacer deposition. The remaining three independent spaces are commonly labelled as α, β and γ. α, β and γ are controlled by multiple process steps including the initial lithographic patterning process, the two mandrel and spacer etches as well as the two spacer depositions.

Scatterometry has been the preferred metrology approach, however is restricted to repetitive arrays. In these arrays independent measurements, in particular of alpha and gamma, are not possible due to degeneracy of the standard array targets : a target where α is equal to some value x and γ is equal to some value y generates the same spectrum as a target where α = y and γ = x. In order to lift this degeneracy either multiple targets are required or modifications to the target design have to be made which may not necessarily reflect actual layout geometries present in the product.

In this work we present a single target approach which lifts the degeneracies commonly encountered while using product relevant layout geometries.

We will first describe the metrology approach which includes the previously described SRM (signal response metrology) combined with reference data derived from CD SEM data. The performance of the methodology is shown in figures 1-3. In these figures the optically determined values for alpha, beta and gamma are compared to the CD SEM reference data. The variations are achieved using controlled process experiments varying Mandrel CD and Spacer deposition thicknesses.

Correlation between CDSEM reference data (x-axis) and OCD values extracted using the methodology described in this paper:

10145-105, Session PWed

Projection lens testing with Moiré effect

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The manuscript describes the application of Moiré effect for testing of a lithographic projection stepper lens. As confirmed experimentally, the arrangement presented allows measuring magnification, distortion, field curvature and telecentricity of the lens and can be used for its fine tuning. The method is based on two matched two-dimensional gratings (arrays of pinholes) whose feature size is comparable with critical dimension of the projection system and whose position errors are two orders of magnitude smaller. The first grating is positioned before the lens (in the “object” plane) and illuminated with a Köhler illumination system. The second grating is placed in a conjugated (“image”) plane and can be translated both laterally (in X and Y) and axially (in Z).

In the presented theoretical analysis of the Moiré fringe forming, local intensity after the second mask is considered as a periodic function of lateral shift between the gratings. Variation of the transmission profile and its contrast due to diffraction effects, aberrations and defocus is analyzed.

Visual interpretation of Moiré fringe pattern allows quick diagnostics of placement errors of the projection system (i.e., combined distortion and magnification error). If placement errors exceed the critical dimension and the masks are aligned by rotation, one could tell the magnitude of these errors from the number of fringes and, based on their shape, relative contributions of magnification and distortion.

Lateral scanning schemes can be applied for measuring of smaller magnitude errors with accuracy up to a few tens of nm. One approach is similar to the phase shifting method in interferometry, where the mask is translated in a few steps and local position error is extracted from the phase of periodic intensity variation. Another approach treats the second mask as a sampling tool for simultaneous scanning of multiple PSFs created by pinholes of the first mask. In this case, placement error manifests itself as a PSF shift. We present the results of both reconstruction methods and analyze measurement errors caused by aberrations and defocus. Measured distortion pattern is confirmed by wafer tests.

It is also shown how the measurement of field curvature and telecentricity of the projection lens can be accomplished by three-dimensional scanning. Field curvature is measured based on variation of Moiré fringe contrast with focus, and telecentricity based on change of distortion with focus. Experimental results presented is in a good agreement with those obtained from the lens design and interferometric measurements.

10145-106, Session PWed

Photolithography enhanced APC for semiconductor manufacturing

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Advanced Process Control (APC) is not a new thing especially in Photolithography for semiconductor fabrication process to achieve good Cpk and less rework. In general, measurement result of Critical Dimensions (CD) and Overlay are automatically feedback to optimize the process condition for the next material in order to get the result of CD and Overlay more on target. APC tends to be complicated especially in a mix-and-match manufacturing with multiple products and multiple tools.

In this paper, an enhanced APC is introduced, which utilizes exponentially weighted moving average (EWMA), delta subtraction, and time retard factor as the key control elements. Additional groupings and offset function to cater for mix-and-match is built into the system. The result of this enhanced APC is discussed.

10145-107, Session PWed

Detection of distorted wafer using stepper alignment control

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Cycles of high temperature thermal process in furnace and rapid thermal processing during wafer fabrication will subject wafer to extreme thermal stress. Due to wafer substrate thermal endurance marginality, unintentional warpage of the wafer may happen intermittently which is unrecoverable after thermal process, this will cause patterned wafer to be permanently distorted. Distorted wafer will cause subsequent Photolithography patterning process misalignment and low yield. Marginally misaligned chip is not able to be screened out during standard functionality test, which may result in field failure.

In this paper, phenomena of wafer distortion are studied and solutions are discussed. Most importantly, a method of 100% inline detection of distorted wafer using Nikon Stepper/ Scanner alignment result control is demonstrated. With this detection, all problematic wafers can be screened out and scrapped to achieve 0 ppm.

10145-109, Session PWed

Advanced carbon nanotube (CNT) tips for CD-AFM metrology

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Critical dimension atomic force microscopes (CD-AFMs) use flared tips and two-dimensional sensing and control of the tip-sample interaction to enable scanning of features with near-vertical or even reentrant sidewalls. As the feature sizes in leading-edge manufacturing have approached the 10 nm level, the need for ever smaller tips has been a challenge for CD-AFM metrology.

Most CD-AFM tips in common use are made of silicon, high density carbon, or a combination of these two. Carbon nanotubes (CNT) have been the subject of experimentation and there are some in use.

Small tips generally pose greater challenges of flexibility and durability than larger tips, and while CNT tips exhibit greater wear resistance and lower compliance than silicon tips, CNT tips remain more difficult and expensive to fabricate than those made of silicon. And since the alignment angle of the CNT is critical for sidewall imaging, the application of CNT tips for CD-AFM has been even more challenging than for conventional AFM.

The Korea Research Institute of Science and Standards (KRISS) has invested considerable effort in the development of a CNT tip fabrication system with very precise control over the CNT alignment.[1] Since the National Institute of Standards and Technology (NIST) has experience in the calibration and characterization of CD-AFM instruments, KRISS and NIST have been collaborating to evaluate the performance of advanced CNT tips for CD-AFM metrology.[1] One of our goals in this collaboration is to push toward CNT tips with 20 nm trench capability. This is challenging in any case but is especially challenging for features of any significant aspect ratio.

Even trenches in the 50 nm range can be challenging to image with most presently available tips. This is particularly true for height/width aspect ratios greater than 2:1. Beyond the challenges due to the geometrical size of a CD-AFM tip, there are challenges due to the flexibility and tip position control: All methods of CD-AFM tip position control induce an effective tip width that may be larger than the actual geometrical tip width, and this concern is potentially greater when using very narrow and high-compliance tips.

Presently, we are exploring the limits of CNT tips fabricated at KRISS, and evaluating their metrology performance using CD-AFM at NIST. Examples of approximately 30 nm multi-walled CNT tips are shown in Fig. 1 and Fig 2. These tips exhibit narrow widths, but have larger edge heights than would be typically be desirable. We continue to work on more advanced tips – including some with a Pt ball grown at the end of the CNT. Our paper will report on the latest progress.

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10145-110, Session PWed

Precise design-based defect characterization and root cause analysis

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As semiconductor manufacturing continues its march towards more advanced technology nodes, it becomes increasingly crucial to identify and characterize design weak points using a combination of inline inspection data and the physical layout (or design). Although inline inspection data and physical design have been used for this purpose over the past few years, the employed methodologies have been somewhat crude, relying greatly on statistical techniques to signal excursions. For example, defect location error that is inherent to inspection tools prevents them from reporting the true locations of defects.

Therefore, common operations such as background-based binning that are designed to identify patterns that fail with high frequency cannot reliably identify specific weak patterns. They can only identify a set of possible weak patterns, but within these sets there are many perfectly good patterns.At the same time, characterizing the failure rate of a known weak pattern on design based on inline inspection data also has a lot of fuzziness due to the coordinate uncertainty. SEM Review comes to the rescue by capturing high resolution images of the regions surrounding the reported defect locations, but SEM images are reviewed by human operators and the weak patterns revealed in those images must be manually identified and classified. Compounding the problem is the fact that a single Review SEM image may contain multiple defective patterns and several of those patterns might not appear defective to the human eye.

In this paper, we describe a significantly improved methodology that brings advanced computer image processing and design-overlay techniques to better address the challenges posed by today's advanced technology nodes. Specifically, new software techniques allow the computer to analyze Review SEM images in detail, to overlay those images with reference design to detect every defect that might be present in generically pre-identified potential failing design locations(including several classes of defects that human operators will typically miss), and to get the exact defect location on design, and to compare those defective patterns against a library of known patterns, and to classify all defective patterns as either new or known.By applying the computer to these tasks, we automate the entire process from defective pattern identification to pattern classification with high accuracy, and we can perform this operation on masse during R&D, ramp, and volume production phases.

By adopting the methodology, whenever there is a specific weak pattern identified, we subsequently run a series of characterization operations to ultimately arrive at the root cause. These characterization operations can include (a)searching all pre-existing Review SEM images for the presence of the specific weak pattern to determine whether there is any spatial (within die or within wafer) or temporal (within any particular date range) correlation and (b) Understanding the failure rate of the specificweak pattern at the same time to prioritize the urgency to fix the problem , (c) comparing the weak pattern against an OPC Verification report or a PWQ/FEM result to assess the likelihood of it being a litho-sensitive pattern, etc. Cyclically, after resolving the specific weak pattern, it will be categorized as known pattern, and the engineer can move forwards to discovering the new weak pattern.

10145-111, Session PWed

TurboShape focus and dose metrology: from computational target design to experimental validation of metrology performance

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The semiconductor industry has made significant improvements to the achievable resolution of the lithography patterning, however this impressive success comes at the cost of losing the process window (PW) of the devices. In particular, the inverse proportionality to the square of numerical aperture (NA) in depth of focus (DOF) is a major challenge, especially in an advanced high NA immersion lithography, raising the importance of process

control in semiconductor manufacturing. As a result, real-time monitoring capability to detect process variations on production wafers is emerging as a new industry requirement. To meet such a request, the new technique called signal response metrology (SRM) has been recently introduced and it has been received a wide attention due to its potential to improve accuracy and robustness to process variation for focus and dose monitoring with a simple measurement recipe can be made by hours [1,2]. Note that the SRM is now named as TurboShape.

One fundamental requirement that never change for any different process monitoring techniques is to utilize targets those provide at least some sensitivity to focus and dose variation within a tight range of interest although the amount of required sensitivity varies depending on different types of metrology techniques. Although TurboShape (i.e., SRM) technique enables to use the measurement on real device for certain critical layers those typically have relatively small overlap process window, measuring the device signal is not always the best solution due to the different focus and dose sensitivities depending on the design of different critical layers and corresponding illuminations. As a result, one needs to design optimal focus and dose monitoring targets when the device does not provide strong enough signal sensitive to process variation.

In the conference, we will present a novel framework for the computational TurboShape target design method which enables the design of robust metrology targets that maximize focus and dose sensitivities. In particular, we will show the detailed analysis of target performance based on using resist profile as well as corresponding Scatterometry signal response, as shown in figures 1 and 2, respectively. We have validated our computational target design framework for particularly the logic metal 1 layer which uses LELELE process with flex-ray illumination. Both computational and experimental results will be discussed.

10145-114, Session PWed

Spectral tunability matters

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In recent years overlay metrology accuracy has significantly improved as additional spectral configurations were introduced. Looking forward to future process nodes raises the question whether there is real value in wavelength tunability over multiple dense, but constant, wavelengths. In this paper experimental results from an overlay tool with a tunable light source as well as comprehensive theory and simulations will be presented. The areas covered as part of this investigation include: The optimal accuracy of the first wafer, the optimal accuracy for cases of high variations within lot and within wafer process, and finding and tracking this optimal setup. The conclusion of this analysis is that tunability is not just a small step down the road; it provides a whole new set of capabilities. Full development and implementation of these capabilities may be the enabler for process control in future process nodes.

10145-54, Session 12

SEM image prediction based on modeling of electron-solid interaction

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Metrology and inspection technology is key in the advancement of device manufacturing. Accurate monitoring of CDs provides useful feedback to the fabrication tools, and sensitive defect detection helps locate the root cause for device failure and leads to a quick yield ramp.

In e-beam metrology and inspection using SEM, a lot of breakthroughs have been proposed to improve imaging capabilities that could be applicable to ever-shrinking semiconductor devices. When a new device structure is introduced, the typical process development procedure is to understand what the SEM image of this device will look like. During this procedure, the limitations of the imaging tool for this particular target can be understood. Then, the working conditions of the tool are optimized. If the image quality is not satisfactory, then the tool manufacturers are required to develop a new tool or a new functionalities. It requires a relatively long time to address the imaging problems.

One of the successful approaches that enables metrology for new generation devices which we are currently pursuing is SEM image simulations based on physical modeling. Accurate modeling is essential to estimate the SEM image contrast of new devices prior to the acceptance of a new wafer processing. Thus, reliable simulation technology enables imaging capabilities and process development to be performed in parallel.

Monte Carlo simulation is the traditional solution for reliable SEM image simulators. Many research groups have proven that advanced physical modeling based on Monte Carlo approaches reproduces the signal generation in SEM well. The non-uniform nature of materials, however, has not been taken into account in Monte Carlo codes so far. In fact, the crystalline structure of materials has not yet been considered, and the shape/density modification during e-beam irradiation has not been modeled. Another challenge is accurately simulating the contrast when there is a difference in the detection efficiency. While certain tool functions, such as detector properties, can be predicted, the effect of the specimen charging is the most difficult task to predict.

In this paper, we demonstrate several case studies of the SEM image simulation solving these tasks. The crystalline effect of the specimen is modeled by examining the difference in the amount of backscattered electrons (BSEs) that are generated depending on the crystal orientation. This is called grain contrast. Grain contrast is the result of electrons channeling through the crystal, where the electrons feel various scattering forces when moving along specific crystalline directions. This effect has been implemented in the Monte Carlo software, resulting in a realistic grain contrast.

Specimen damage is also accounted for in the simulation by assuming that the volume loss is correlated to the energy loss in the materials calculated in Monte Carlo. Volume loss driven by the electron energy loss in the specimen is one of the possible reasons of the phenomena, and other mechanisms would be worth considering for more realistic reproductions.

Image changes due to specimen charging in SEM is a long lasting problem. We have successfully reproduced typical charging artifacts in SEM by proper modeling algorithms of charging and adjusting the parameters of the materials.

10145-55, Session 12

Depth measurement technique for extreme deep holes using back-scattered electron images with high-accelerating voltage SEM

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The design structure of NAND flash memory has shifted from planar 2D to vertical 3D to increase bit density and reduce bit cost. 3D NAND devices have cell strings positioned vertically in 3-?m-thick channel holes etched through the whole film stack. The etching of these extreme deep channel holes is one of the most challenging and critical processes. Non-destructive depth monitoring of the holes is necessary for the control of the process.

In this study, we developed a novel depth measurement technique for extreme deep holes that uses scanning electron microscope (SEM), widely used for monitoring the process of semiconductor manufacturing. To gather information from the bottom surface of the holes, we used high accelerating voltage SEM (HV-SEM) at an accelerating voltage over 15 kV. The intensity of the bottom surface in the back-scattered electron (BSE) image that is generated from HV-SEM depends on the depth. The high-energy electrons

irradiating the bottom surface are back-scattered to a certain extent and lose their energy while traveling in the solid surrounding the hole. The BSE image intensity is determined by the number of electrons ejected from the solid by the backscattering process. The intensity is lower for deep holes as the electrons need to travel a longer distance in the solid, resulting in fewer electrons ejected from the solid.

We modeled the relationship between the hole depth and the BSE image intensity in the following steps. First, we expressed the distance travelled by the BSEs in the hole depth by assuming that they has been randomly scattered in the solid. Then, we expressed the BSE image intensity in the distance travelled on the basis of the energy attenuation of electrons. Using this model, the hole depth was measured using the BSE image intensity at the bottom surface. This proposed technique, using only a top-view image generated from HV-SEM, enables fast, non-destructive depth measurements.

We evaluated the performance of the proposed technique for deep holes in simulations and experiments. The results show the sensitivity of the technique is sufficient for depth monitoring.

10145-56, Session 12

SEM-based overlay measurement between via patterns and buried M1 patterns using high-voltage SEM

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As semiconductor device pattern has been shrinking continuously, overlay control at each layer becomes one of the most important issues for semiconductor manufacturers.

Recently, SEM based overlay has been used for reference and optimization of optical overlay for both Image Based Overlay(IBO) and Diffraction Based Overlay(DBO) at AEI (After Etch Inspection) steps.

However, feedback to lithography equipment at AEI steps is already too late to make any corrections. Overlay measurement at ADI(After Development Inspection) steps has a benefit of enabling resist rework.

Thus, SEM based overlay at ADI steps has become necessary as a reference for optical overlay.

For accurate overlay measurement, measured patterns should have features similar with actual devices.

SEM overlay patterns can be the same pattern sizes as actual patterns and much smaller compared to optical overlay patterns.

In the last SPIE, we presented evaluation results to measure overlay between M1A and M1B using high voltage SEM and showed good correlation with optical overlay.

This time, overlay at via step was evaluated in the same manner.

V0 patterns are fabricated using LELE process. V0A hard mask pattern exists under V0B resist pattern. There is a trench structure of M1 in the lowest layer (M1A). Two overlay measurements, 1) between V0B resist layer and V0A buried layer, 2) between V0B resist layer and buried bottom M1 layer, were carried out. The results show good correlation with the intercept 1nm and NRE 2nm below. Measurement variation associated with local CDU was analyzed for Via patterns.

The effectiveness of overlay measurements using high voltage SEM was also shown for Via steps.

10145-57, Session 12

High-precision CD measurement using energy-filtering SEM techniques

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Semiconductor logic and memory devices are being switched from a 2D planar structure to a 3D structure. Forming these complex structures requires sophisticated process control and metrology to enable the creation of high-aspect-ratio (HAR) structures. Since in CD-SEM metrology, the number of secondary electrons (SEs) at the top of a HAR structure is much larger than that at the bottom of the structure, the value measured using CD-SEM reflects the dimensional change of the top surface instead of reflecting that of the bottom face. Thus, the SEs emitted from the top surface should be removed to improve measurement precision for the bottom face. The energy spectra of SEs emitted from the top surface of HAR structures formed with insulation layers are different from those of SEs that have escaped from the bottom face [1]. Thus, SEs emitted from the top surface can be removed by using an energy filter (EF), which is known as voltage contrast (VC) SEM imaging.

Examples of bottom edges emphasized using a retarding field EF [2] are shown. Voltages VEF (<0) and VR (<0) were respectively applied to the EF and the sample, and ?V was VR?VEF. As ?V increased, the low-energy SEs were reflected at the EF, and the contrast between the bottom edge and hard mask increased. The VC images are useful for extracting edges from the HAR structure, but the images are sensitive to variations in wafer potential.

VC images obtained from four measurement points using a conventional EF are shown. The wafer potential at each point was different, resulting in different quality VC images. Since CD-SEM metrology requires precise EF voltage control when using VC images, we developed an EF voltage correction method to be used at each measurement point. The VC images obtained using the newly developed EF are also shown. The image quality of the images was consistent at every measurement point.

The relationship between the variation in the measured values and that of the wafer potential for the HAR hole pattern is shown. The conventional EF showed a positive correlation between the variations, indicating that the measured values were affected by the wafer potential fluctuations. On the other hand, there was no correlation between the variations with the newly developed EF. Consequently, bottom-edge measurement, independent of the wafer potential fluctuations, was achieved by using the newly developed EF.

In summary, VC images obtained using a newly developed EF were used to measure the bottom face of HAR structures. The EF incorporates a correction method for wafer potential fluctuations and thus improved the stability of the images of HAR structures. Our developed technique is effective for CD-SEM metrology using VC images.

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10145-58, Session 12

SEM imaging capability for advanced nano-structures and its application to metrology

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For over 30 years, scanning electron microscopy (SEM) imaging has

been supporting the R&D, yield management, and process controls in semiconductor device manufacturing. Originally, the application of SEM in microelectronics imaging came along with its basic principle of secondary electron contrast, where the signal intensity is enhanced at the structure edges, called edge contrast. This fact was eventually applied to the critical dimension measurement of the device structures, making a substantial contribution to the dominated CD-SEM installation for metrology.

Several challenges were recognized soon after the first introduction of CD-SEM in major chip makers. Technology solely depending on the edge contrast was not capable of detecting the material interfaces or the sub-surface structures. This problem was solved by using energy filtering, or energy-selective imaging, rejecting low energy secondary electrons and highlighting the high energy back-scattered electrons that are sensitive to the material composition, and the local geometry of the target. Now the energy filter capability becomes a standard feature in major in-line SEM tools working for the metrology and inspection.

Complexity of the semiconductor device structures, however, goes forward further so that the energy selective imaging as well as the traditional secondary electron imaging would become insufficient to monitor the dimension or to pick the defects in the most advanced nano-scale devices.

In this paper, we propose an effective approach to obtain proper SEM contrast at a point of interest in semiconductor devices, by optimizing the primary electron energy and detector window for signal energy and emission angle.

Emission angle of the signal electron carries the information of the local geometry. In the deep structure like the capacitor bottom in DRAM or the trench of stacked NAND memory, only the high angle signal can escape from the bottom to be detected by SEM. Therefore the angular selection is essential to enhance the contrast of the bottom images created by the very weak signal and, on the other hand, suppress the strong background signal from the other area. The trajectory of the low energy signal electrons may be affected by the local charging, making the angular selection difficult. In such cases, combining energy filtering with angular selection becomes effective.

Energy of the impinging electron is another important parameter. This enables the depth profiling of the target structure. Basically the selection of the beam energy is the trade-off between the information volume and the depth resolution. By comparing the low and high probe energy images, the surface residue can be located, and the sub-surface void embedded in the inter-layer dielectrics can also be found.

In summary, the SEM contrast improvement by optimizing the primary electron energy and detector window is presented. The approach would be applied in metrology and inspection for next generation nano-devices. In signal detection, the realization of the energy-angular selective imaging is a key to challenging metrology.

10145-59, Session 12

3D SEM characterization of advanced sidewall patterning process

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Sidewall image transfer has become a key enabler of future design shrink. It is consisted of several process steps that multiply the number of lithography backbone patterns in a self-aligned form, shrinking pattern and pitch sizes.

The quality of the image transfer process depends on the characteristics of the sidewall pattern morphology. Rectangular Sidewalls with a flat top and vertical edges will result with symmetrical and uniform etched image. On the other hand, Facet top, bent sidewalls, sloped edges or foot, may distort the etched image.

In this paper we present a description of the 3DSEM metrology technique used, simulation results, and demonstrate three dimensional characterization of Sidewalls pattern fabricated with different etch recipes:

o Top Facet measurements vs cross section images

o Edge slop and foot characterization

10145-60, Session 13

Pattern centric design based sensitive patterns and process monitor in manufacturing

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When design rule is mitigating to smaller dimension, process variation requirement is tighter than ever and challenges the limits of device yield. Masks, lithography, etching and other processes have to meet very tight specifications in order to keep defect and CD within the margins of the process window. Conventionally, Inspection and metrology equipments are utilized to monitor and control wafer quality in-line. In high throughput optical inspection, nuisance and review-classification become a tedious labor intensive job in manufacturing. Certain high-resolution SEM images are taken to validate defects after optical inspection. These high resolution SEM images catch not only optical inspection highlighted point, also its surrounding patterns. However, this pattern information is not well utilized in conventional quality control method. Using this complementary design based pattern monitor not only monitors and analyzes the variation of patterns sensitivity but also reduce nuisance and highlight defective patterns or killer defects. After grouping in either single or multiple layers, systematic defects can be identified quickly in this flow.

In this paper, we applied design based pattern monitor in different layers to monitor process variation impacts on all kinds of patterns. First, the contour of high resolutions SEM image is extracted and aligned to design with offset adjustment and fine alignment [1]. Second, specified pattern rules can be applied on design clip area, the same size as SEM image, and form POI (pattern of interest) areas. Third, the discrepancy of contour and design measurement at different pattern types in measurement blocks. Fourth, defective patterns are reported by discrepancy detection criteria and pattern grouping [4]. Meanwhile, reported pattern defects are ranked by number and severity by discrepancy. In this step, process sensitive high repeatable systematic defects can be identified quickly

Through this design based process pattern monitor method, most of optical inspection nuisances can be filtered out at contour to design discrepancy measurement. Daily analysis results are stored at database as reference to compare with incoming data. Defective pattern library contains existing and known systematic defect patterns which help to catch and identify new pattern defects or process impacts. On the other hand, this defect pattern library provides extra valuable information for mask, pattern and defects verification, inspection care area generation, further OPC fix and process enhancement & investigation.

10145-61, Session 13

The use of computational inspection to identify process window limiting hotspots and predict sub-15nm defects with high capture rate

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As critical dimensions for advanced 2D DUV patterning continue to shrink,

the exact process window is increasingly difficult to determine. The defect size criteria shrink with the patterning critical dimensions and are well below the resolution of current optical inspection tools. As a result, it is more challenging for traditional bright field inspection tools to accurately discover the hot spots that define the process window. In this study, we use a novel computational method to identify the depth-of-focus (DOF) limiting features of a 10nm node mask with 2D metal structures (single exposure of multiple LE) and compare the results with those obtained by a traditional process window qualification (PWQ) method based on utilizing a focus modulated wafer and bright field inspection to detect hot spot defects. By determining the DOF for Hot Spot candidates from both techniques on a CD-SEM we compare which provides more critical locations and better describes the process window.

The computational work was done with a Tachyon litho-resist model that was also used to conduct the optical proximity correction (OPC) before mask tape-out. The detection of hot spots was done with the Lithography Manufacturability Check (LMC) software and can employ the same detectors as the established LMC product to verify the simulated pattern integrity. Simulations through the process window are done to locate the hot spots with the smallest depth-of-focus. The main failure mechanism observed on this layout with modulation out of focus is necking (pinching).

We plot the actual depth-of-focus measured after-litho and after-etch-and-clean and conclude that the computational method finds more critical features than found with bright field Inspection in a PWQ work flow.

We explore the monitoring of systematic defects occurring at these hot spot locations by using a prediction model that combines focus measurements with the collected process window information. The focus measurements are done with a YieldStar on diffraction based focus targets which are placed in the scribe-lanes of the test mask. Fast measurement allowed dense sampling up to 25 points per field, which is combined with scanner data that relates to non-correctable focus errors for high resolution and accurate focus prediction on the test wafer.

Defect prediction is verified with CD-SEM on a wafer with induced focus defects. Because of the focus offset this wafer shows a high number of process window limiting locations to be out of specification. The measurement is compared with the prediction by showing feature size for these locations. The capture rate and nuisance rate are determined to be ~80% and ~30% respectively.

We conclude that for the focus sensitive hotspots considered, the computational technique is an improvement over the traditional method for hot spot discovery and monitoring.

To show the general applicability of the method we extend it to bridging hot spots in an LELELE application, again identified with LMC-based software. An overlapping process window for overlay can be shown with the most critical hot spots in the layout closest to nominal (no overlay error) condition. We show experimentally that these locations are indeed limiting by comparing with the process of record. An HVM monitoring flow can be envisioned where overlay measurements are also input to the defect prediction algorithm.

We suggest extending the method to include defects that are related to inter-layer placement errors.

10145-62, Session 14

CD-SEM metrology and OPC modeling for 2D patterning in advanced technology nodes *(Invited Paper)*

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In the course of assessing OPC compact modeling capabilities and future requirements, we chose to investigate the interface between CD-SEM metrology methods and OPC modeling in some detail. Two linked observations motivated our study:

1) OPC modeling is, in principle, agnostic of metrology methods and best practice implementation.

2) Metrology teams across the industry use a wide variety of equipment, hardware settings, and image/data analysis methods to generate the large volumes of CD-SEM measurement data that are required for OPC in advanced technology nodes.

Initial analyses led to the conclusion that many independent best practice metrology choices based on systematic study as well as accumulated institutional knowledge and experience can be reasonably made. Furthermore, these choices can result in substantial variations in measurement of otherwise identical model calibration and verification patterns.

We will describe several experimental 2D test cases (i.e., metal, via/cut layers) that examine how systematic changes in metrology practice impact both the metrology data itself and the resulting full chip compact model behavior. Assessment of specific methodology choices will include:

• CD-SEM hardware configurations and settings: these may range from SEM beam conditions (voltage, current, etc.,) to magnification, to frame integration optimizations that balance signal-to-noise vs. resist damage.

• Image and measurement optimization: these may include choice of smoothing filters for noise suppression, threshold settings, etc.

• Pattern measurement methodologies: these may include sampling strategies, CD- and contour- based approaches, and various strategies to optimize the measurement of complex 2D shapes.

In addition, we will present conceptual frameworks and experimental methods that allow practitioners of OPC metrology to assess impacts of metrology best practice choices on model behavior.

Finally, we will also assess requirements posed by node scaling on OPC model accuracy, and evaluate potential consequences for CD-SEM metrology capabilities and practices.

10145-63, Session 14

Analytical linescan model for SEM metrology of 2D patterns

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A critical dimension (CD) scanning electron microscope (SEM) converts a measured linescan into a single dimension number. To better understand how the linescan relates to the actual dimensions of the feature being measured, it is important to understand how the systematic response of the SEM measurement tool to wafer structures impacts the shape of the resulting linescan. Rigorous 3D Monte Carlo simulations of SEM linescans can be extremely valuable for this purpose, but they are often too computationally expensive for day-to-day use. Thus, one approach will be to develop a simplified, analytical linescan model (ALM) that will be more computationally appropriate to the task of analyzing linescans. This analytical linescan expression will then be fit to the rigorous Monte Carlo simulations to both validate and calibrate its use.

In this work, JMONSEL simulation [1,2] is used to better understand how various SEM parameters, beam size/shape, and sample profile influence the linescan (Figure 1). In our previous studies [3-5], an analytical linescan model was developed for trapezoidal features of varying height, width, pitch, and sidewall angle, including top corner rounding and bottom footing. This model was shown to fit JMONSEL simulations extremely well (Figure 2) for silicon and PMMA features on a silicon wafer (or on BARC for the case of photoresist) over a range of dimensions and shapes. In this study, the linescan model will be extended to two-dimensional patterns such as contact holes and tip-to-tip line-end patterns. The result will be a calibrated

linescan model that could prove very useful for better analyzing and interpreting experimental linescans. Additionally, features as small as 5 nm in width will be explored to understand applicability of such models to the smallest upcoming features of interest.

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10145-64, Session 14

High-throughput multi-beam SEM: quantitative analysis of imaging capabilities at IMEC-N10 logic node

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The continuous shrink of semiconductor patterns imposes many challenges on the fabrication of semiconductor devices, not only on the patterning process itself but also on the inspection of the patterns. As critical patterning defect sizes shrink along with the target pattern size, the required sensitivity and signal-to-noise ratio is becoming increasingly difficult to achieve with current optical inspection techniques. SEM-based inspection technologies can resolve the relevant patterns and defects, but have not been able to achieve the throughput requirements for screening large areas yet. This barrier has been overcome in 2014 with the introduction of multi-beam scanning electron microscopes [1].

The details of the setup of the multi-beam electron microscope have been described in detail elsewhere [1]. We describe the basic principle of operation in Figure 1: Multiple primary beams (depicted blue in the left image) are scanned in a single column in parallel over a sample (right image); one detector per secondary electron beam (green in the left image) enables parallel detection of all beams, thus circumventing the detector bandwidth limitation. The distribution of the current over a large volume inside the column enables maintaining high resolution at high total current. The multi-beam SEM has been demonstrated qualitatively to image wafer patterns [2] and lithography masks [3]. A first quantitative evaluation of critical dimensions (CD) yielded values similar to a CD-SEM [4].

In this paper, we apply the multi-beam SEM to the inspection of patterns on separated chips of a semiconductor wafer suited for process window characterization at the imec-N10 logic node, and analyze its imaging properties in a systematic and quantitative way. We investigate the impact of imaging parameters on quantitative metrics extracted from the images, e.g., CD repeatability and relative defect count. We demonstrate that the multi-beam SEM is able to image the relevant patterns at this technology node, track their variations as the focus and dose conditions of the lithography scanner are varied, and consistently find defects which will limit the process window for the lithography application. Example images taken with the multi-beam SEM can be seen in Figure 2.

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10145-65, Session 14

SEM review color imaging in detection of gate to source/drain short in 14nm finFET device

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The introduction of finFET has contributed tremendously in making scaling beyond 20nm a reality. However, the complexity of these 3D high performance transistors generate inherent new defects that are difficult to detect and this heightens concerns over device quality and reliability at future technology nodes. New methods and approaches are thus needed to effectively detect and monitor this new class of defects. Color imaging in Scanning Electron Microscopy (SEM) is not a new phenomenon. However, its use in inline SEM based defect review in the semiconductor industry is relatively new. In this work SEM color imaging is used to enhance SEM review redetection of a buried defect, Gate to Source/Drain short in 14nm finFET device. Defect sites on the wafer are flagged as defect events by Bright Field (BF) defect inspection tools. The review tool uses SEM optics to redetect the defect event using a combination of very high electron landing energies in excess of 5 keV and high beam current of about 3,000 pA to confirm the existence of the defect. The defect signal is further processed through a color coder by the SEM review equipment to create a "false" color image to enhance defect redetection and help to accurately classify defect.

10145-66, Session 15

Materials characterization for process integration of multi-channel gate all around (GAA) devices

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Multi-channel Gate all around (GAA) semiconductor devices march closer to becoming a reality in production as their maturity in development continues. From this development, an understanding of what physical parameters affecting the device has emerged. The importance of material property characterization relative to that of other physical parameters has continued to increase for GAA architecture when compared to its relative importance in earlier architectures. Among these materials properties are the concentration of Ge in SiGe channels and the strain in these channels and related films. But because these properties can be altered by many different

process steps, each one adding its own variation to these parameters, their characterization and control at multiple steps in the process flow is crucial.

This paper investigates the characterization of strain and Ge concentration, and the relationships between these properties, in the PFET SiGe channel material at the earliest stages of processing for GAA devices. Grown on a bulk Si substrate, multiple pairs of thin SiGe/Si layers that eventually form the basis of the PFET channel are measured and characterized in this study. The detailed relationships between these material properties at each step, and how these properties change as a function of process step, are presented. Multiple measurement techniques, both in-line and laboratory-based, are used to measure these properties. In-line X-Ray Photoelectron Spectroscopy (XPS), Low Energy X-Ray Fluorescence (LE-XRF), and off-line Secondary Ion Mass Spectrometry (SIMS) are used to characterize Ge content, while in-line High Resolution X-Ray Diffraction (HRXRD) and off-line Nanobeam Diffraction (NBD) are used to characterize strain. Because both patterned and unpatterned structures were investigated, scatterometry (also called optical critical dimension, or OCD) was used to provide valuable geometrical metrology needed to better calibrate some of the Ge concentration measurements and provide better insight into the relationships between Ge concentration and strain.

10145-67, Session 15

3D-profile measurement of advanced semiconductor features by using FIB as reference metrology

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A novel method of sub-nanometer uncertainty for the 3D-profile measurement and LWR (Line Width Roughness) measurement by using FIB (Focused Ion Beam) processing, and TEM (Transmission Electron Microscope) and CD-SEM (Critical Dimension Scanning Electron Microscope) images measurement is proposed to standardize 3D-profile measurement through reference metrology. The proposed method has been validated for profile of Si-line and photoresist features in our previous investigations. In this article, we apply the methodology to line profile measurements and roughness measurement of advanced-FinFET (Fin-shaped Field-Effect Transistor) features. The FinFET features are sliced as thin specimens of 100 nm thickness by FIB micro sampling system. Cross-sectional images of the specimens are obtained then by TEM. LWR is estimated from the edges sharpness on TEM images. Moreover, we demonstrate a novel on-wafer 3D-profile metrology as “FIB-to-CDSEM method” with FIB slope cut and CD-SEM measuring. Using the method, a few micrometer wide on a wafer is coated and cut by 45 degree slope using FIB tool. Then, the wafer is transferred to CD-SEM to measure the cross section image by top down CD-SEM measurement. We apply FIB-to-CDSEM method to FinFET feature. 3D-profile and 3D-profile parameters such as top line width and side wall angles of FinFET feature are evaluated. The 3D-profile parameters also are measured by TEM images as reference metrology.

10145-68, Session 15

Molecular dynamics and dynamic Monte-Carlo simulation of irradiation damage with focused ion beams

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Focused ion beam (FIB) has become one of important tools for micro- and nanostructuring of samples such as milling, deposition and imaging. However, the surface is still damaged on the nanometer scale by implanted projectile ions and recoiled material atoms. It is important to investigate each kind of the damages quantitatively. This report presents our dynamic Monte-Carlo (MC) simulation code to simulate morphological and compositional change of a multi-layered sample and our molecular dynamics (MD) simulation code to simulate dose-dependent changes in backscattering-ion (BI)/secondary-electron (SE) yields of a crystalline sample.

In order to calculate the BI yield, ion trajectories were pursued by solving kinetic equation of motion in a small cell of the sample with periodic boundaries conditions of the sides of the cell, according to the classical MD scheme [1]. Forces were calculated from the analytical differentiation of empirical bond-order potentials for solid-state atoms and the Ziegler-Biersack-Littmark potentials for ion-atom interactions. The ions were assumed to lose energy continuously in the trajectory from electronic interaction of Lindhard-Scharff type. The SE yield was simply calculated through a semi-empirical scheme, assuming that the number of internal SEs produced along the ion trajectory is proportional to the electronic energy loss, the SEs decay exponentially toward the top surface of the cell, and the transmission probability through the surface potential barrier is 0.5.

In the dynamic MC code [2,3], assuming ion beams with the profile of Gaussian type, three dimensional material changes in the sample arise from the deposition of implanted ions and the collisional mixing of implanted atoms and different material atoms. The principle of the material changes is based on the assumption that each pseudo-projectile represents a differential dose of the ions and the surface layer is divided into many cells of constant thickness. After ion bombardment, implantation, sputtering and atomic relocation cause removal or deposition of constituent atoms in different cells. Local depletions or excess densities in each cell are allowed to relax by adjusting cell thickness. The incremental surface recession, or thickness increase, is calculated from the difference in integrated cell thickness before and after bombardment.

Recent progress of the codes for research to simulate Mo/Si layers deformation and intermixing in EUV lithography mask repair using FIB and crystalline orientation effect on the BI an SE yields related to the channeling contrast in scanning ion microscopes, are presented.

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10145-69, Session 15

Measurement of beam-induced damage during CDSAXS measurement of photoresists

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New critical dimension metrology methods such as critical dimension small angle X-ray scattering (CDSAXS) are being developed to meet the measurement challenges of next generation devices. Two key requirements for any new CD metrology method are non-destructiveness and the measurement speed. We will report on a study of beam damage and scattering strength of two model photoresist systems, HSQ and PMMA. We also will report on the status and initial results from NIST’s upgraded lab CDSAXS system.

50 nm pitch line gratings were fabricated in HSQ and PMMA films using EUV interference lithography at the Swiss Light Source. The lines were about 30 nm tall and 20-30 nm wide. The 17 keV CDSAXS exposure time was varied from 0.1 s to 60 s to determine the minimum X-ray exposure required to obtain a satisfactory fit. Normal incident measurements separated by a blanket X-ray exposure were repeated to measure the decrease in

scattering intensity with X-ray dose. The PMMA scattering signal was found to decrease by about 80 % before stabilizing at around 15 % of the original scattering intensity. The HSQ scattering signal decreased much less and stabilized at about 80 % of the original scattering intensity. We also conducted a series of variable-angle CDSAXS measurements as a function of blanket X-ray exposure to determine how the shape of the photoresist lines changed during X-ray exposure. For PMMA, we found the line width to remain constant and the line height to decrease from 25 nm to 10 nm during the exposure series. The exposures that damaged the samples corresponded to several hours of exposure to the synchrotron beam in a 100 μm spot and were much longer than what was required to characterize the line gratings. Smaller targets result in a larger dose and could potentially damage the resist in the time required to make a CDSAXS measurement. The large differences in beam damage between PMMA and HSQ show that resist damage from CDSAXS will depend on the particular resist chemistries and target size.

10145-108, Session 15

Application of advanced hybrid metrology method to nanoimprint lithography

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Alternative lithography solutions have made significant advances in recent years, still offering a variety of choices within the semiconductor lithography community. In order for these advancements to be fully utilized, lithography methods also need innovative metrology solutions to address their unique challenges. Once such metrology solutions are in place, the lithography is much closer to being fully adopted. Nanoimprint lithography (NIL) is one alternative lithography solution that is being pursued by the industry. A metrology-related problem specific to NIL is the measurement of the residual layer thickness (RLT), as knowledge of this is key to the monitoring and control of the NIL process and subsequent patterning. Scatterometry is used to measure the RLT due to its ability to measure profile features non-destructively with high throughput. But because scatterometry is sensitive to features unrelated to the parameter of interest, complex geometries throughout the film stack can make the measurement challenging. New methods to reduce the impact of such complex geometries on the measurement parameters of interest are therefore needed. Because of the use of NIL for 3DNAND development, the measurement of the RLT with complex structures underneath becomes necessary. This paper describes the results from a new hybrid metrology method that can combine key information from these complex geometries with scatterometry measurements to reduce the impact on the RLT measurement due to the layers beneath the resist. By reducing this impact, scatterometry measurement noise and cross-correlation of parameters is reduced, resulting in better precision and accuracy in the RLT measurement.

Results verifying the measurement quality of the RLT on complex 3DNAND structures using this new hybrid method are presented. In this paper, we call the locations where the complex structures are measured the target structure or target film stack (fig. 1), which are on the target wafers. This structure, or film stack, consists of the NIL pattern over several film layers and a complex under-layer 3DNAND pattern. In order to verify the hybrid measurements of the target wafers, we compare such measurements using two approaches: comparison to reference measurements collected from the same target wafers, and comparison to standard scatterometry measurements collected from "proxy" wafers. The reference metrology used includes both XSEM (cross-sectional scanning electron microscopy) measurements of the RLT and the CD (critical dimension) of the resist, as well as CDSEM measurements of the resist CD. Although the resist CD is not as important to measure for NIL as the RLT, verifying it as well as the RLT increases confidence in the hybrid method.

In the second comparative approach, we take advantage of the fact that the NIL process is insensitive to the underlayers, whether simple or complex, as long as planarity is achieved before the NIL. Due to the complexity of the target film stack, accurate and precise measurements of the RLT are difficult to obtain using standard scatterometry (also called OCD, or Optical Critical Dimension, metrology). However, the hybrid method solves this problem by taking advantage of key aspects of the complex structure in order to reduce their effect on the measurement of the RLT. The second approach verifies this by comparing measurements on the target wafer using the hybrid method to standard OCD measurements on a proxy wafer, which contains the proxy structure, or proxy film stack (fig. 1). The proxy wafer only contains the NIL patterned resist plus a couple other layers identical to the target wafer, but not the complex under-layer pattern, thus making standard OCD a straightforward method to measure the RLT. Because of the insensitivity of the NIL process to the underlayers, target structures and proxy structures processed using the same NIL conditions should have nominally the same RLT. This concept is similar to the commonly used idea of "sister" wafers, which are wafers that are nominally identical in an experiment. The term "proxy" is instead used in this case to indicate that the wafers are not even nominally identical (one contains the complex under-layer pattern, the other does not), but the relevant aspects of the wafers (the NIL resist on top) are still nominally identical.

10145-112, Session 15

Connected component analysis of review-SEM images for sub-10nm node process verification

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With the continuous shrink of device features, especially below 10 nm, optical inspection of individual features is becoming more and more challenging [1]. Hot spots detected by optical inspection need to be always verified by a review-SEM to localize the exact point of failure. Historically, Review-SEM's have been used for classification of defects into different bins depending on type e.g. particles / pattern fails (bridge / opens), residues, etc. Recent advances have seen incorporation of design for design assisted auto classification. However, still a vast amount of information is lost due to almost non-existent methods for specific feature quantification on review SEM images. This is particularly important in understanding pattern fidelities at 7nm and beyond nodes. In this paper we show that by extracting various kinds of feature measurements from review-SEM images, acquired with KLA-Tencor EDR7110 platform, we can get valuable insight into process capabilities in order to augment

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10146-1, Session 1

"How" can selective area atomic layer deposition extend patterning beyond the 7nm node? *(Keynote Presentation)*

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Atomic layer deposition has played an important role in manufacturing in semiconductor microelectronics for on the order of a decade, even though the antecedent of ALD dates to the 1970's. There are additional opportunities for ALD to contribute that depend on the development of ALD processes that are substrate composition dependent, which exhibit selectivity, i.e., growth on material A, with no growth occurring on material B. Over the past several years a number of groups have been pursing different approaches to developing selective area ALD processes. In this presentation we will present a short overview of ALD, comparing and contrasting it to other deposition techniques, with an eye on factors that might produce selectivity. We will also present a summary of the work conducted to date, identifying the strengths and weaknesses of these approaches concerning their ability to contribute to selfaligned patterning at the 5 nm node and beyond.

10146-2, Session 1

DSA patterning options for logics and memory applications *(Keynote Presentation)*

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Directed self-assembly (DSA) of block copolymers (BCPs) has drawn great attention in logics, hard disk drive, and memory applications due to its material-controlled patterning capability, including density multiplication and defect/feature size rectification. Recent studies on 193i/High Volume Manufacturing (HVM) compatibility, defectivity, and device demonstration of DSA further reinforce its role as a potential candidate for lithography extension rather than merely a lab-scale nanofabrication method.[1-3] Lately, many research groups have illustrated structures for specific applications using a variety of chemoepitaxy and graphoepitaxy DSA processes, such as sub-30nm pitch line/space array for FinFET, hexagonal array of holes for DRAM, elongated holes/bars for vias/contacts, and posts for memory applications. In this paper, we will discuss the advantages and challenges of several potential DSA applications in logics and memory field. Furthermore, we will summarize the critical gaps that still remain open and identify areas where the DSA community can work together. Each topic will be discussed in details in a separate talk in this conference.

Using chemoepitaxy DSA for fin patterning provides inherent control in both pitch and CD uniformity while its technological counterparts may have excellent control in only one of the two but not both. However, as pattern density increases, two major challenges arise: pattern transfer fidelity and customization. To address these two issues, a HVM-compatible integration scheme with an ultra-thin film stack will be demonstrated. Challenges of pursuing Si Fin formation and integrated FinFET devices, as well as further pitch scaling using this new stack will be discussed. The preliminary study of using DSA combined with alternating-color hard mask approach to overcome the overlay limit will also be investigated. (AL17-AL104-79)

Graphoepitaxy DSA for via/contact formation provides CD rectification and potential reductions in total lithography process steps. In this work we will focus on studying the CD rectification effect using guiding patterns generated by EUV. Sub-60nm pitch via-chain test structures are fabricated and tested in order to understand the behavior of local CDU structurally and electrically. The surface modification process, pattern transfer process, and materials involved to enable such a tight-pitch design will be further discussed. (AL17-AL104-36, AL17-AL104-77)

Phase change material (PCM)-based memory cells have shown promise as an enabler for low power, high density memory. However, phase change chalcogenide alloys are prone to processing damage such as from plasma etch, wet clean, encapsulation and annealing. Two methods of patterning of PCM device structures have been achieved using directed self-assembly (DSA): the formation of a high aspect ratio pore designed for atomic layer deposition of etch damage-free PCM, and pillar formation by image reversal and plasma etch transfer into a PCM film. We demonstrate significant CD reduction of a lithographically defined hole by dry etch shrink and DSA and subsequent pattern transfer into a high aspect ratio pore or pillar structure with appropriate hard mask selection and design of the plasma etching process. (AL17-AL107-6)

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10146-3, Session 2

A numeric model for the imaging mechanism of metal oxide EUV resists *(Invited Paper)*

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Metal-containing resist systems, including metal oxide (MOx), organic-inorganic hybrid, and nanoparticle based compositions, are promising alternative imaging materials for EUV lithography. When compared to traditional organic chemically amplified resists (CAR), such new materials offer the potential for improved sensitivity to EUV radiation (by virtue of stronger intrinsic absorption), improved pattern fidelity (due to diminished diffusion-based image blur), simplified processing protocols (enabled by the robust refractory metal oxide etch barriers formed upon patterning), and reduced pattern collapse (a consequence of relaxed thickness requirements).

Inpria MOx resists, designed to undergo photo-induced metal oxide condensation following EUV exposure, have realized many of these performance and integration advantages. However, compared to CAR systems, whose chemistry, physics and processing characteristics have been studied in depth over three decades, the chemical and physical mechanisms underpinning the lithographic imaging of these newly developed materials are not widely understood. In order to elucidate these mechanisms each step of the lithographic process for an archetypal Inpria MOx resist is examined: (a) absorption of EUV radiation, (b) radiation-induced chemical reactions, (c) condensation of radiation products to form a latent image, and (d) development of the latent image to form a relief image. Based on experimental measurements, a quantitative representation of the chemical and physical state of the MOx resist film is described as it evolves through each step in the lithographic process. Lithographic performance parameters are predicted and compared directly with experimental results.

Treatment of the resist film at the scale of individual molecules explicitly accounts for statistical effects in photon absorption, secondary electron generation, and the chemical reactions that follow. Following EUV exposure, reactive MOx species may have more than one reactive site available for condensation. Propagation of the condensation chemistry, and its variation with the degree of photolysis of the film, is demonstrated to play a key role in governing lithographic properties.

While this model employs a specific resist material as an initial example, the overall imaging model may be applied more broadly to other resist systems exhibiting photo-induced MOx condensation.

10146-4, Session 2

Reactivity of metal-oxalate EUV resists as a function of the central metal

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Extreme Ultraviolet light (EUV, ?=13.5 nm) is the likely subsequent technology for high volume manufacturing for the microelectronics industry. Traditional EUV photoresists have been composed of organic compounds which are moderately transparent to EUV. Resist stochastics and sensitivity can be improved by increasing the number of photons absorbed. Molecular organometallic resists are metal containing resists aimed at improving EUV absorption. This work focuses on studying the role of the metal center (Metal = Co, Fe, Cr) in an oxalate complex by comparing the number of absorbed photons and the photoelectron reactivity in each compound. This series of compounds is well-suited for this study because the only change in structure is the central metal—all the ligands remain the same.

Previous work has shown that sensitivity improves with increasing theoretical EUV optical density using the CXRO website and assuming the film density remains constant (Figure 1).1,2 Presumably, the darker central metal causes the molecule to absorb more photons. Consequently, more photoelectrons are generated, but it is uncertain if the electron reactivity changes between the different compounds. We will determine whether the metal is changing the EUV optical density as expected, and if there is any correlation between the different compounds in terms of electron reactivity.

In the study presented here, the EUV absorption coefficients are determined experimentally by measuring the transmission through a resist coated on a silicon nitride membrane using an Energetiq (EQ-10M) plasma source. Additionally, the photochemistry is evaluated and compared prior to development by monitoring outgassing reaction products. This particular resist platform eliminates oxalate ligands when exposed to electrons or EUV photons resulting in a solubility difference between the exposed and unexposed regions. In the process, carbon dioxide is produced and is monitored using mass spectrometry, where quantitative values are obtained using a calibration technique.

10146-5, Session 2

Studying the photoreaction mechanism of tin-oxo cage photoresist using hard x-ray photoelectron spectroscopy

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Molecular inorganic photoresists are considered for Extreme UltraViolet Lithography (EUVL) for sub 10 nm features instead of organic polymers due to their stronger photon absorption and smaller building block size, which potentially allow high resolution and low line edge roughness. However, the chemical reaction mechanisms of this kind of photoresist during the photolithography process are still unclear. In this study, we will discuss the mechanism of the photochemistry of a potential negative tone inorganic EUV photoresist: molecular tin-oxo cages ([(RSn)12O14(OH)6]X2)(R = organic group; X = anion) that contain strongly absorbing Sn atoms, making these materials potentially very sensitive to EUV photons.

We use spectroscopic methods to obtain insight into the radiation induced chemical and solubility changes. Synchrotron radiation based hard X-ray photoelectron spectroscopy (HAXPES) which has a high photon energy range from 1.7 keV to 9 keV can ionize a large range of core level electrons from the sample well below the surface. Thus, the bulk electronic properties of the sample can be characterized with high energy resolution. HAXPES was used to investigate the structure of the molecules and chemical oxidation state changes of the atoms in the photoresist. Tin cage photoresists were prepared on conductive substrates as fresh samples. Exposed samples were prepared by using fresh samples pre-exposed to a 225 nm DUV laser. HAXPES spectra were recorded using 2 keV photon energy. Different chemical oxidation states and concentrations of the atoms and atom types in the fresh and exposed photoresists were obtained from the HAXPES spectrum, as shown in Figure 1.

The composition of the fresh tin-oxo cages was confirmed to match the theoretical formulation. After DUV exposure, Sn-carbon bond cleavage and binding energy shift of core level electrons from different atoms were observed. Other spectroscopy techniques such as UV-vis and IR were also used to obtain more information about the chemical changes inside the materials. Results from the fresh and exposed photoresist samples are compared and presented. We believe that once we understand the chemical reaction mechanisms of the Tin oxo cages photoresists, we can think of rational strategies to improve the sensitivity and resolution of these and related inorganic EUV photoresists. Such improvements are urgently needed to meet the demands of the semiconductor industry.

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10146-6, Session 3

Fundamentals of EUV resist-inorganic hardmask interactions *(Invited Paper)*

Dario L. Goldfarb, Martin Glodde, IBM Thomas J. Watson Research Ctr. (United States); Anuja De Silva, Indira Sheshadri, Nelson M. Felix, IBM Research - Albany Nanotech (United States)

Initial readiness of EUV patterning was demonstrated in 2016 with IBM Alliance's 7nm device technology. The focus has now shifted to driving the 'effective' k1 factor and enabling the second generation of EUV patterning. High resolution EUV patterning is currently limited by EUV resist thickness and pattern collapse, thus impacting the faithful image transfer into the underlying stack. Such limitation requires the investigation of improved hardmasks (HMs) as etch transfer layers for EUV patterning. Ultrathin (<5nm) inorganic HMs can provide higher etch selectivity, lower post-etch LWR, improved defectivity and wet strippability compared to spin-on hybrid HMs (e.g SiARC), however such novel layers can induce resist adhesion failure and resist residue. Therefore, a fundamental understanding of EUV resist-inorganic HM interactions is needed in order to optimize the EUV resist interfacial behavior. In this paper, novel materials and processing techniques are introduced to characterize and improve the EUV resist-inorganic HM interface. A number of alternative adhesion promoters specifically tailored for ultrathin inorganic HMs (aSi, LTO, TiOx) are presented and the mitigation of resist delamination is exemplified for the cases of positive-tone and negative-tone development (PTD, NTD). Additionally, original wafer priming hardware for the deposition of such novel adhesion promoters is unveiled. Separately, HM surface interactions with specific EUV resist components are evaluated for an open-source experimental resist formulation dissected into its individual additives using EUV contrast curves as an effective characterization method to determine post-development residue formation. The learning acquired in this work can be directly applied to the engineering of EUV resist materials and processes specifically designed to work on such novel HMs.

10146-7, Session 3

Photoelectron scattering and acid release in EUV lithography: a simulation study

John J. Biafore, KLA-Tencor Texas (United States)

Abstract

BACKGROUND: The ionizing wavelength in extreme ultraviolet (EUV) resist exposure leads to photoelectron scattering and uncertainty in the resulting acid image, producing line-edge roughness (LER) and poor CD uniformity of the printed features.

GOALS: Try to determine how photoelectron and acid exposure blur effects affect EUV lithography and how they might be better controlled. Try to determine whether or not, and if so under what conditions, high resist quantum yields are beneficial to EUV lithography.

METHODS: Using a stochastic resist simulator, we study the effects of resist properties upon photoelectric scattering, the uncertainty in the acid release and the properties of the after-development photoresist image in high NA EUV lithography. Uncertainty in the release of acids is the fundamental cause of LER and the ultimate limiter of optical lithography technology.

10146-8, Session 5

Modeling and simulation of low-energy electron scattering in organic and inorganic EUV photoresists *(Invited Paper)*

Alessandro Vaglio Pret, Trey Graves, David Blankenship, John J. Biafore, KLA-Tencor Texas (United States)

Alternative photoresist platforms are being developed with the goal of meeting Resolution, Roughness and Sensitivity requirements for EUV lithography. Metal-based materials appear promising due to the high etch resistance, high absorption, and high resolution shown under 13.5nm synchrotron exposures . However, the exposure mechanism of these materials is quite different from that of organic CARs.

In this paper we use the optical data previously collected at the Elettra facility to modify the physical model of electron scattering in PROLITHTM to describe both organic and inorganic materials. Specifically, the new model can be used to approximate the inelastic and elastic mean-free paths and the stopping power at very low kinetic energy.

The new model allows a direct comparison of the exposure mechanisms in different resist platforms: in particular, it is now possible to estimate the intrinsic resist uncertainty by evaluating electron and acid shot noise and spatial blurring, while forcing the Photon Shot Noise (PSN) contribution to uncertainty to zero .

A comparison between an organic CAR and a metal-based photoresist revealed how the denser nature of the latter and the higher effective atomic number Zeff help containing the electron scattering in a much closer radius around the absorption event. The consequent electron-reaction (acid generation for organic PAG-containing CAR, ligand dissociation for the metal-based photoresist) reflects the electron shot noise of the different platforms: the final exposure radial blur for the organic material is almost 3 times larger than the metal-based photoresist.

10146-9, Session 5

Difference in EUV photoresist design towards reduction of LWR and minimization

Jing Jiang, Danilo De Simone, Geert Vandenberghe, IMEC (Belgium)

Pattern fidelity of EUV lithography is crucial for especially for small and dense features, as small variation can affect device performance and even cause short or open circuit. For 1D features, dense lines and contact holes are the most common features for active, metal and contact layer, therefore line width roughness (LWR) and local critical dimension uniformity (LCDU) are important targets to quantify the variations. Both targets are greatly influence by the photon and acid shot noise, while LWR is also affected by other mechanical issues of resist like pattern collapse.

In this study, we systematically study the influence of different chemically amplified resist components on LWR and LCDU, like polymer, PAG and quencher type and concentrations in order to understand the relative influence of deprotection, acid diffusion, and base neutralization on pattern fidelity. Based on these fundamental understanding, we optimized resist sensitivity and LWR/LCDU performance.

However, conventional methods to approach higher resolution or to decrease LWR/CDU by sacrificing the dose are not sustainable. In order to continue to improve resist performance, we introduce a new component – metal salt sensitizer- into the resist system. We are able to achieve 35% dose reduction by increasing EUV absorption, maintaining LWR. We believe adding metal sensitizer gives us a new way to challenge the RLS tradeoff.

10146-11, Session 5

Separating the optical and resist contributions to line-edge roughness in EUV lithography using stochastic simulations

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KLA-Tencor Texas (United States); Harry J. Levinson, Todd Bailey, GLOBALFOUNDRIES Inc. (United States)

Minimization and control of line-edge roughness (LER) and contact-edge roughness (CER) is one of the current challenges limiting EUV line and hole printability1-3. One significant contributor to feature roughness and CD variability in EUV is photon shot noise (PSN); others are the physical and chemical processes in photoresists. Different approaches are available to mitigate each of these contributions and to facilitate this mitigation, it is important to assess the magnitude of each of these contributions separately from others.

In this paper, we present and test several computational approaches based on either explicit utilization of the Poisson statistics of PSN2 or direct Monte Carlo simulation of photon absorption in resist to estimate the contribution of PSN to LER. We also discuss another approach to separate the optical and resist contributions based on Monte Carlo stochastic simulations of certain ad hoc patterns by varying the incident dose within a wide range.

The simulation results indicate approximately similar magnitude of contribution from PSN and resist stochastic to edge variation for a sufficiently optimized high dose EUV resist.

We also present a systematic resist parameter optimization method and demonstrate several examples of its application.

An understanding of the role of various resist parameters and stochastic mechanisms would benefit LER mitigation efforts in EUV lithography.

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10146-12, Session 5

An investigation on "nano-swelling" phenomenon during resist dissolution using in situ high-speed atomic force microscopy

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Lithographic technology target sizes are becoming much smaller than the basic components of typical resist materials. It is thus a natural trend to pursue alternative / non-conventional materials in achieving these nano-patterning goals. The optimization of resist processes and introduction of alternative ones are also being actively advanced as it plays a significant role in extending the limits of present resist materials. Resist development (or dissolution) into the developer solution is a key step in the resist process that has been a constant topic of interest. This is because the dissolution process is where physical realization of resist nano-patterns first occurs. If clearly understood, such information can provide potentially significant pointers in insuring high quality nano-patterns. However, the dissolution process has both chemical and mechanical reactions which complicate analyses, and in effect makes it difficult to appreciate just how these nano-patterns are formed.

The authors have in recent years proposed and reported on the use of an in-liquid high-speed atomic force microscope (HS-AFM) which allows the in situ analysis of resist dissolution. This has led to the establishment of a method in determining the "dissolution unit size" of resist polymers during dissolution which is viewed as a potentially effective metric for improving resist material composition. In the application of this method for extreme ultraviolet (EUV) resists, certain materials were found to have a tendency to "swell" during dissolution. It is noteworthy that such swelling behaviors occur in the nano-scale regions, as opposed to the bulk film swelling (millimeter-scale) reported in other dissolution analysis methods. Thus the term "nano-swelling" was applied. This "nano-swelling" phenomenon was especially true for positive-tone chemically amplified resists where the exposed areas (spaces between line patterns) were observed to exhibit swelling behavior just before dissolution in conventional aqueous alkali-based developer solutions (aq. tetramethylammonium hydroxide or aq. TMAH).

Specifically, the existence of "nano-swelling" was observed in experiments using model EUV resists based on polyhydroxystyrene (PHS) and a hybrid PHS-methacrylate polymers, in comparison to typical EUV resists. Figure 1 show a part of the in situ dissolution analysis results; HS-AFM scanned images for the (a) PHS-based, (b) hybrid, and (c) typical EUV resist materials with 32-nm isolated line pattern (upper section), 32-nm half pitch lines and spaces (hp L/S) patterns (middle section) and a cross-section analysis of the 32-nm hp L/S image showing the magnitude of "nano-swelling", in terms of maximum swelling value (bottom section). These results were obtained during dissolution in aq. TMAH developer, at optimal HS-AFM measurement conditions (image size: 1000?1000 nm, resolution: 400?400 pixels, speed: 2 s/image). As shown in the figure, it is clear that compared to the PHS-base model EUV resist, the hybrid and typical EUV resist materials exhibit "nano-swelling" at ~15nm and ~7nm, respectively.

During the conference, the results of an investigation of the cause of this "nano-swelling" phenomenon and their effect on nano-pattern formation quality will be reported. This will be done through additional experiments utilizing varied of material components and resist process conditions.

10146-82, Session 5

Embedded top-coat for reducing the effect out of band radiation in EUV lithography

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Extreme ultraviolet lithography (EUVL) is the most promising next-generation lithography candidate for device manufacturing at the sub-20nm half-pitch node [1]. However, in order for EUV to enter production, several challenges remain to be addressed. For example, out-of-band (OOB) photons emitted by the EUV source along with the desired EUV wavelengths can significantly deteriorate lithographic patterning performance. Conventional EUV photoresists have evolved from materials designed for lithography at 193 nm and 248 nm, whilst the wavelength of out-of-band radiation is generally from 150-400 nm. Hence if OOB light generated from plasma source reaches the wafer plane, and the resist is sensitive to that light, then contrast and LER will be reduced, resulting in degraded imaging performance [2, 3].

Recently, several studies have addressed these problems by developing an OOB protection layer or topcoat (OBPL) [1, 4, 5]. However, the application of a separate OOB protection layer has certain restrictions, for example the topcoat must not mix with the resist, and it must be removable during the development process. Furthermore, the extra processing step for coating of the separate OBPL on the photoresist is not desirable. Therefore, we have developed an embedded topcoat with the ability to absorb out-of-band radiation for EUV lithography photoresists. One of the main characteristics of the topcoat polymer is that it possesses low surface energy. In order to promote the formation of a top-layer via phase separation from the photoresist, the polymer bears surface-active moieties such as fluorinated groups. The introduction of such species as single moieties or as polymeric segments has been investigated in this study. In addition, another important characteristic of the embedded polymer is that it has absorbance across the range of OOB wavelengths. In order to absorb such wavelength photons, the polymeric top-coat includes deep ultraviolet (DUV) absorbers such as benzene, anthracene or naphthalene groups. In addition, the embedded

topcoat polymer has a solubility switching unit. In order to ensure that the topcoat can dissolve in the alkaline solution during the development step, the polymer contains solubilizer units, which can improve the solubility and the compatibility of the topcoat polymer in alkaline solution after irradiation.

In this study we describe the design of a surface-active polymer, which is able to undergo phase segregation from a photoresist matrix to form a topcoat. The variety of surface agents (fluorinated, hydrocarbon, etc.) and quantity required to provide the most effective phase separation from the photoresist has been investigated. The phase segregation has been confirmed through TOF-SIMS, XPS and AM-FM viscoelastic characterization. Besides, the absorbance of DUV radiation of embedded topcoat was characterized by ellipsometry. Finally, the lithographic performance of a resist containing the embedded topcoat was evaluated using EBL exposure.

10146-13, Session 6

Challenges and progress in low defectivity for advanced ArF and EUV lithography processes using surface localized material technology

Michihiro Shirakawa, Hideaki Tsubaki, Hajime Furutani, Wataru Nihashi, Naohiro Tango, Kazuhiro Marumo, Kei Yamamoto, Hidenori Takahashi, Akiyoshi Goto, Mitsuhiro Fujita, FUJIFILM Corp. (Japan)

Extreme ultraviolet lithography (EUVL) is one of the most promising candidates for high volume manufacturing of next generation lithography (NGL). On the other hand, ArF lithography process still occupies an important position for NGL due to the delay of EUVL by difficulties in developing exposure tool, mask, and resist materials. Materials for both EUV and ArF lithography are, therefore, necessary toward 10 nm node generation and beyond.

The main challenge in ArF lithography is to reduce cost of ownership (CoO) because increase in multi-patterning process is generally required to obtain fine pattern. As a consequence, industry strongly requires ArF lithography process with a fast scan speed scanner and low defectivity material for CoO. Negative-tone imaging (NTI) process, which involves an organic solvent developer and conventional resist, can be applied as a novel method to simultaneously satisfy both fast scan speed and low defectivity requirements because hydrophobic character to achieve a good scan speed followability is suitable for dissolving material without defectivity. However, there is also great demand to apply positive-tone imaging (PTI) process for NGL using both ArF and EUV. Requirements of fast scan speed and low defectivity have to be solved even in case of PTI where hydrophobic character is not good for defectivity reduction.

We described herein novel immersion additive technology to satisfy both high scan speed and low defectivity requirements. A key technology for fast scan speed was to increase surface localization ability of immersion additive to obtain followability to immersion water by increasing hydrophobicity of film surface. On the other hand, a tradeoff relationship was observed between followability to water and defectivity because hydrophobicity was not good for developer wettability and affinity which are both related to low defectivity. Breakthrough technology to improve defectivity and resolution simultaneously was reforming properties of film surface from hydrophobic to hydrophilic after alkaline development process because properties after development process should be only associated with defectivity, not fast scan speed.

The materials with high polarity change function were explored to EUV PTI process to achieve low defectivity with good lithography performances.

10146-14, Session 6

A chemically amplified resist without catalyst

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Chemically amplified resists (CARs) are now in widespread and general use for efficient production of high resolution patterns by optical, x-ray and photolithographic exposure. The basis of the CAR design is a gain process, in which a small amount of photochemically-generated acid catalyzes a large number of deprotection reactions that change the solubility of a resin. However, the diffusion of the acid during the post-exposure baking step also leads to image bias and line-edge roughness (LER). These obstacles are intrinsically linked to the CAR design and have been described by the so-called “triangle of death” and quantified on the basis of Wallow’s “Z-factor”. In such systems, high gain (sensitivity) requires efficient diffusion, but this also inevitably causes bias and blur. For low-intensity light sources, like those found in EUV lithography, these issues become exacerbated and limit the use of the traditional CAR resist design.

The goal of the work described here was to devise a system that achieves gain without utilizing photoacid catalysts. The inherent instability of so-called “unzipping” polymers was exploited to facilitate a solubility switch upon exposure to radiation that does not involve diffusion, but provides resist formulations with contrast and sensitivity comparable to that of CARs. In this design, the polymer is a dissolution inhibitor for an etch resistant matrix resin, but once depolymerized, the exposed regions become soluble in developer. A single exposure event can initiate depolymerization of a polymer chain back to monomer, which involves breaking many bonds and provides the gain. Herein, the development of a resist based on a new, self-immolative, aromatizing polyester is presented. This carefully designed polyester was synthesized by two different routes and then blended with Novolac. The formulation acts as a positive-tone resist. Upon e-beam exposure, this catalyst-free CAR demonstrates a lower dose-to-clear than commonly used e-beam resists like PMMA and ZEP and may serve as a model for the design of a new family of resist materials.

10146-15, Session 6

Photosensitized chemically amplified resist (PSCAR (TM)) 2.0 for high-throughput and high-resolution EUV lithography

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Akihiro Oshima, Seiichi Tagawa, Osaka Univ. (Japan)

In order to lower the cost of ownership of EUV lithography, high sensitivity EUV resists, enabling high throughput of EUV scanners are being sought intensively. The concept that utilizes a Photosensitized Chemically Amplified Resist (TM) (PSCAR (TM)) is a promising solution for achieving increased resist sensitivity while maintaining other high performance characteristics of the material (i.e., resolution, line edge roughness (LER), exposure latitude). PSCAR uses a UV flood exposure after EUV exposure and selective absorption to meet these goals. The preliminary but promising results have been discussed in previous papers1-6.

PSCAR is trying to break the resolution, line-edge-roughness, and sensitivity trade-off (RLS trade-off) relationships that limit the ultimate lithographic performance of standard chemically amplified resists (CAR). PSCAR utilizes an area-selective photosensitization mechanism to generate more acid at the pattern exposed areas during a UV flood exposure. The photosensitizer which is generated in the pattern exposed area by photo acid catalytic reaction absorbs the flood exposure light selectively and generates more acid in this area only. Because of the extra photo acid quenching step in the PSCAR process, an improved photosensitizer (PS) distribution profile can be achieved so that the final acid image contrast is better than the original EUV pattern exposed image resulting in a superior resolution and LER.

Material development and flood exposure techniques are the key elements of PSCAR technology for semiconductor mass fabrication. This talk will review the collaborative efforts on the improvement of PSCAR technology. Also, this paper introduces a new concept for PSCAR ("PSCAR 2.0") to enhance resist sensitivity and latent image contrast using a new type of chemistry that works with flood exposure.

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10146-16, Session 6

Double-deprotected chemically amplified photoresists (DD-CAMP): higher-order lithography

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As the industry moves to narrower line widths, reaching LER goals is becoming increasingly difficult.1-4 Additionally, as EUV has been late to market, a number of researchers have developed double exposure processes that require non-linear responses to light.5-7

Here, we present a completely new design for chemically amplified resists called Double-Deprotected Chemically Amplified Photoresists (DD-CAMP). This approach utilizes chemical deprotection kinetics which have higher-order dependence upon acid concentration. These higher-order kinetics should create sharper chemical contrasts, and therefore, print images with better LER than would be possible with first-order CAMP resists. Conceptually, the DD-CAMP monomers consist of a carboxylic acid protected with a blocking group consisting of a trigger and a body. The removal of this blocking group requires two acid-catalyzed steps to produce the polymer-bound carboxylic acid (CA). The first step "pulls the trigger", thereby weakening the bond between the body and the carboxylic acid. The second acid-catalyzed step removes the blocking group. When the relative rates of these two deprotection steps are properly balanced, the rate of deprotection of these blocking groups is proportional to the concentration of acid to the 1.8 power: d[(P)CO2H]/dt ? [H+]1.8. Figure 2 shows that the concentration of carboxylic acid (% product) is proportional to catalytic acid to the power of 1.84.

This higher-order dependence allows this system to yield a sharper chemical contrast at the line edge than typically provided by the aerial image. We have also shown improved LER of our DD-CAMP resists over control.

10146-17, Session 6

Patterning with metal-oxide EUV photoresist: process simplification, resist smoothening, trim, shrink and selective strip

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Inpria's metal-oxide photoresist (PR) serves as a thin spin-on patternable hard mask for EUV lithography. Compared to traditional organic photoresists, the ultrathin metal-oxide photoresist (~12nm after development) effectively mitigates pattern collapse. Because of the high etch resistance of the metal-oxide resist, this may open up significant scope for more aggressive etches, new chemistries, and novel integration schemes.

We have previously shown that metal-oxide PR can be successfully used to pattern the block layer for the imec 7-nm technology node1 and advantageously replace a multiple patterning approach, which significantly reduces the process complexity and effectively decreases the cost. We also demonstrated the formation of 16nm half pitch 1:1 line/space with EUV single print2, which corresponds to a metal 2 layer for the imec 7-nm technology node.

In this paper, we will explore new etch chemistries in order to develop the etch processes for

- Patterning transfer – process simplification
- LWR smoothening

- Resist line trimming
- Trench Shrinking
- Dry selective strip

All these learnings will be needed to implement the metal-oxide PR into the 7nm-technology node and beyond.

The initial results for the trim and shrink process are demonstrated for 16nm HP line/space in the figure below.

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10146-18, Session 7

Unexpected impact of RIE gases on lithographic films *(Invited Paper)*

Martin Glodde, Robert L. Bruce, Marinus J. P. Hopstaken, Michael R. Saccomanno, IBM Thomas J. Watson Research Ctr. (United States); Nelson M. Felix, Karen E. Petrillo, IBM R&D Lithography Enablement (United States); Bill Price, IBM Thomas J. Watson Research Ctr. (United States)

Successful pattern transfer from the photoresist into the substrate depends on robust layers of lithographic films. Typically, an alternating sequence of inorganic (most often Si containing) and organic hardmask materials is used. Pattern transfer occurs then by using RIE chemistry that is selective to one particular layer (such as: flurorinated RIE for Si HM). The impact of these RIE gases onto the layers acting as hardmask for the layer to be etched is typically neglected, except for known sputtering effects.

We found that components of the RIE gases can penetrate deep into the “inert” layers and significantly modify them. For example, nitrogen used as component to etch spin-on carbon layers was found to travel up to 70 nm deep into Si HM materials and create layers with different material properties within this film. The question is being raised and discussed to which extent this atom implantation may impact the pattern transfer of the ever shrinking features.

More Explanations:

On paper, RIE gases are treated as if they are inert to all lithographic films that they are not supposed to etch (besides some sputtering).

The main message will be that we have data showing this is not the case but that in opposite, the RIE gases can penetrate deeply into the films and modify them significantly. Examples are shown, such as N implantation into Si substrates but also SIMS data of various other RIE gases into various substrates.

Examples of potential impact: will an a-Si or SiO2 layer implanted with N now etch more like SiN?

Layers within the film become more relevant if the overall size of the film shrinks. This is of general interest for the lithographic community and shows our leadership in researching this.

10146-19, Session 7

Exploration of a low-temperature PEALD technology used to trim, clean, smooth and re-shape both ArF and EUV photoresists targeting patterning requirements for the 5nm technology node and below

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Year after year, the semiconductor industry overcomes a tremendous amount of technical challenges to satisfy Moore’s law. Through innovative device architectures, smart design, new integration and patterning concepts, better tools and new materials, the industry has successfully reached the 7-nm technology node. Both design and patterning options are identified and the High Volume Manufacturing (HVM) readiness is expected end of 2018. Today, the industry is preparing for the 5-nm technology node (N5) while research centers start identifying and exploring the different patterning options for the 3-nm technology node. The former targets a Metal 2 Pitch (M2P) of 32-nm and a Contacted Poly Pitch (CPP) of 42-nm while the latter aims for a M2P of 24-nm and a CPP of 32-nm. At such tight metal pitches and in view of the continuous progress in EUV source power, a single print EUV lithography is considered as a potential patterning option for N5 to pattern critical Back-End-Of-Line (BEOL) layers such as block, via and eventually unidirectional metal lines. Going one node further down and considering only a full EUV flow, pitch splitting techniques such as Spacer Assisted Double Patterning (SADP) or double Litho-Etch (LE) must be inserted to assist EUV lithography and meet final pitch requirement for both metal and block layers. However, at such dimensions EUV lithography will add extra components to the inherent patterning complexity of the aforementioned pitch splitting techniques. Without the emergence of improved EUV photoresist (PR) design that meets requirements for resolution, line edge roughness and sensitivity, we can expect a very limited available PR budget for pattern transfer (between 12-nm and 30-nm), an increase of the bottom PR scum and finally a degradation of the PR roughness that will contribute to the total CD variation and consume an important part of the overall Edge Placement Error (EPE) budget. Hence, actual patterning methods used to smooth and transfer down the PR pattern must be significantly improved and new solutions must be explored to enable the emergence of advanced technologies.

In this work, we exploit the advantages of a low temperature Plasma-Enhanced Atomic Layer Deposition (PEALD) technology such as an excellent uniformity across wafer and a high process control. We divert the technique from its original goal and used it to trim, clean, smooth and re-shape both ArF and EUV PR patterns that could subsequently receive an in-situ spacer deposition required to build up an SADP grating. Different process conditions (gas, power, pressure) are evaluated on both blanket and patterned wafers. Trim and etch rates, stress, surface roughness and chemical modification of the PR are characterized using ellipsometry, Fourier transform infrared spectroscopy and atomic force microscopy. The PR line roughness is measured from top down SEM imaging and the different contributors to the roughness determined from a Power Spectral Density (PSD) analysis. Moreover, we evaluate the formation of a cost-effective EUV SADP grating and we study how patterns and roughness are transferred down into the metal hard mask.

10146-20, Session 7

High-aspect ratio silicon structures by using displacement Talbot lithography and Bosch etching

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The resolution of a standard contact/proximity photolithography tool is typically limited to ~0.5-0.6 micrometers. However, the precise control of the linewidth and uniformity becomes challenging for gratings with pitches in the range of 1-2 micrometers, especially for wafers which are thinner than about 300 micrometers. Any surface inhomogeneity or defects present on the wafer or the mask surfaces can lead to noticeable linewidth variations.

We utilized the newly developed Displacement Talbot lithography (DTL) [1] technology to pattern gratings with a pitch of 1.2 micrometers. The method is non-contact, which makes it essentially insensitive to surface planarity and enables exposures with very high linewidth uniformity on thin and even slightly deformed wafers. In the DTL lithography the illumination of a phase mask with periodic structures with a parallel beam of light forms a Talbot pattern and the substrate is scanned during exposure by one Talbot in the direction of the illumination. The details of the principle of DTL have been published elsewhere [1]. After development of the resist layer, the pattern is transferred into an underlying antireflective coating by reactive ion etching (RIE) in oxygen and then further into Cr hard mask by RIE in a Cl2 based process. Finally, high aspect ratio structures are etched into the Si substrate using SF6/C4F8 based Bosch process. We achieved uniform gratings over complete 4”-wafer areas with pitches down to 1.2 micrometer and structure heights up to 30 micrometers.

Our results demonstrate the creation of uniform, large-area, small-pitch gratings at an affordable cost with the use of the DTL technology. Such gratings are key components that enable construction of compact systems for phase contrast X-ray imaging [2] with wide-ranging applications in medicine, biology and material science.

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10146-21, Session 8

Modeling of NTD resist shrinkage

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Recent chemically amplified resist used in Negative Tone Development processes exhibit a significant amount of resist shrinkage during post-exposure-bake (PEB). A detailed analysis of experimental results can be found in reference [Küchler et al, SPIE Adv.Litho, 2017]. These resists show up to ~ 25% height loss during PEB in the exposed regions. In particular, it has also been demonstrated that the shrinkage during PEB can have a strong impact on both, the CDs and the resist profile shapes which are formed after the final development step. We therefore highlighted the necessity to augment physical modeling of the PEB process step for these NTD photoresists.

To account for the shrinkage process during PEB in lithography simulations we start with the following modeling assumptions: Microscopically, the tendency for shrinkage is due to the collapse of free volume which is left behind by the volatile and evaporating byproduct of the acid-catalyzed de-protection reaction during PEB. However, this tendency for shrinkage will not only induce a (vertical) resist height loss but causes also lateral displacements inside the resist. This yields distorted 3D profiles of all the species that are typically tracked during PEB simulations. In particular, the local degree of protection after PEB will be distorted, which determines the solubility during the final development simulation step. A deformed degree of protection will then lead to tilted sidewall angles of resist profiles and changed CDs. These effects are strongly pitch-dependent and must be accounted for in a physical simulation approach as well as in OPC modeling.

In this work we first describe our simulation framework which accounts for mechanical deformation during PEB. We simulate the mechanical deformation applying a lattice-spring network, modeling an isotropic but possibly heterogeneous elastic material the properties of which may locally vary. Using exemplary simulations, we determine the impact of the main effects which are captured by our model.

In order to validate our simulation approach, the simulated effect of shrinkage-induced mechanical deformations during PEB on CD signatures and on resist profiles is compared with experimental data.

10146-22, Session 8

A novel methodology for litho-to-etch pattern fidelity correction for SADP process

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For 28 nm node semiconductor devices and beyond, more aggressive resolution enhancement techniques (RETs) such as source-mask co-optimization (SMO), litho-etch-litho-etch (LELE) and self-aligned double patterning (SADP) process are utilized for the low k1 factor lithography processes. In SADP process, the pattern fidelity is extremely critical since a slight photoresist (PR) top-loss or profile roughness may also impact the later core trim process due to its sensitivity to environment. During the subsequent sidewall formation and core removal processes, the core trim profile weakness may be enhanced and induces serious defects that affect the final electrical performance. To predict PR top-loss, a rigorous lithography simulation can provide a reference to modify mask layouts; but it takes much longer run time and not capable of full-field mask data preparation.

In this paper, firstly we brought out an algorithm which utilizes multi-intensity levels from conventional aerial image simulation to assess the physical profile through lithography to core trim etch steps. Subsequently, a novel correction method was utilized to improve the post-etch pattern fidelity without suffering litho. process window. The results not only matched PR top-loss in rigorous litho. simulation, but also agreed with post-etch wafer data. Furthermore, this methodology can also be incorporated with OPC and post-OPC verification to improve core trim profile and final pattern fidelity at early stage.

10146-10, Session PS1

Chemical changes in hybrid photoresists before and after exposure by in situ NEXAFS analysis

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Tracking the chemical changes that occur in a photoresist after exposure is

considerably challenging even in the simplest molecules. The main difficulty lies in the delay between the exposure and the characterization of the material, which usually needs to be done using different instrumentations and vacuum environments. The near edge X-ray absorption fine structure (NEXAFS) spectroscopy is a powerful technique to investigate the chemical changes in resist materials before and after exposure: in PMMA, it clarified the exposure mechanism both qualitatively (which carbon bond change) and quantitatively (how many)[1]. NEXAFS is as well useful for extreme ultraviolet (EUV) lithography photoresists[2] featuring an organic or organometallic core.

In this work we analyzed the chemical changes occurring in EUV photoresists synthesized from organically modified precursors and transition metal alkoxides by sol-gel route [3]. Some of these systems containing Zr and Ti [3, 4, 5] and produced into liquid solution, were drop-cast onto semitransparent silicon nitride membranes to be characterized by NEXAFS. The experiments were conducted at the PolLux beamline of the Swiss Light Source, featuring a STXM (scanning transmission X-ray microscopy) which combines the spatially resolved microscopy and the NEXAFS spectroscopy at once[6] and it is especially suited for the study of radiation damage in photosensitive organic thin films by in situ exposure.

The absorption spectra were acquired in the proximity of the carbon (≈ 272 eV) and oxygen (≈ 525 eV) edges before and after the exposure. To the purpose of the exposure, the beam energy was set to 500 eV, which is much higher than the carbon edge energy and thus exposing the material by generation of thermal secondary electron, in a similar way as the EUV light (91.9 eV) does. By varying the exposure dose, the peak shift revealed the changes in the chemical environment of carbon and thus the change in chemical configuration (consistently with complementary analysis by Fourier transform infrared spectroscopy). It was found that the exposure induced a progressive photodegradation of some organic groups with increasing dose; hydrolysis and condensation reactions of residual alkoxy groups of transition metal and organically modified precursors were also promoted.

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10146-52, Session PS1

Chemically amplified i-line positive resist for next-generation flat panel display

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Traditional diazonaphthoquinone (DNQ) positive photoresists are widely used for TFT-LCD array process. Current LTPS technology has more than 600ppi resolution is required for small or middle-sized TFT liquid crystal display panels. One of the ways to enhance resolution is to apply i-line single exposure system instead of traditional g/h/i- broadband exposure system. We have been developing i-line chemically amplified photoresist ECA 200 series for the next generation flat panel display (FPD). ECA 200 consists of three components: a phenol resin, a photo acid generator and dissolution enhancer. We applied three different types of dissolution enhancers to our resist materials. As a result, we achieved higher sensitivity, higher resolution, less footing of the resist profile and reduced standing wave effect compared with traditional DNQ photoresists. In addition, we have developed another photoresist that does not need post exposure bake (PEB) process. This resist has a great advantage at most of current panel plants without PEB process.

10146-53, Session PS1

High-resolution, high-throughput, CMOS-compatible electron-beam patterning

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Two electron-beam lithographic processes were developed, which employ chemically amplified resists that are used in optical lithography: one positive tone 193-nm photoresist, and one negative tone i-line photoresist. Using established optical resists in electron-beam lithography addresses two limitations of conventional scanning electron beam lithography (SEBL): (1) low areal throughput and (2) limited compatibility with traditional microfabrication infrastructure.

Due to high costs, state-of-the-art tooling (i.e. 193-nm immersion) and masks can be impractical for low-volume device fabrication, whether for microelectronic, microelectromechanical, or microphotonic applications. SEBL with shorter exposure times and compatibility with the traditional microfabrication infrastructure is an enabler of wafer-scale maskless patterning techniques, which can mitigate the high costs of advanced lithography.

Tennant observed that areal throughput (At) relates to resolution (R) via a power law as At?R^5 [Tennant, Nanotechnology Ch.4 1999]. This relationship predicts extremely long write times or low throughput for writing nanoscale features with SEBL, which can render the technique impractical for large area, wafer-scale patterning. However, since areal throughput depends inversely on the exposure time (t), which in turn varies linearly with resist dose (Do), t?Do, increasing the resist sensitivity will proportionally reduce the exposure time, assuming similar SEBL writing strategies. Thus, using chemically amplified photoresists, which are also sensitive to e-beam exposure, can increase areal throughput relative to e-beam specific resists, such as PMMA or HSQ.

For the chemically amplified photoresists under investigation, dense lines were developed at exposure doses as low as 50 ?C/cm2. The photoresists were stable under vacuum (10-6 Torr), and withstood long write times (2-3 days). The changes in critical dimensions due to post-exposure bake (PEB) delays were repeatable and small at rates of ~1-2 nm/hr. For the 193-nm methacrylate-based positive resist (JSR ARF1682J-30), with 3:1 PGMEA:resist dilution, sub-40-nm half-pitches were consistently demonstrated (30-nm half-pitch minimum). This resolution is comparable to the state of the art for 193-nm lithography. For the melamine resin-based negative resist (AZ nLOF2020), with a 6:1 PGMEA:resist dilution, sub-60-nm features were demonstrated, which are among the smallest features reported for this resist.

Conventional SEBL patterning may involve metals, lift-off processes, or resist materials with relatively poor etch resistance, which can limit their use in and effectiveness with state-of-the-art microfabrication facilities and processes. We have demonstrated both imaging and patterning by using resist materials with an established compatibility with the existing advanced CMOS microfabrication infrastructure. Using a tri-layer resist stack (Brewer Science Optistack) and the positive photoresist, nanoscale features were etched reproducibly into crystalline and polysilicon, silicon nitride, and silicon dioxide without evidence of beam distortion due to charging.

The aforementioned photoresist processes, which combine SEBL exposure with optical resist processes, can overcome the practical and economic

limitations of the two disciplines. Furthermore, it opens the possibility for true hybrid e-beam/optical lithography in many applications.

10146-54, Session PS1

Nanoimprint lithography using gas permeable template

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Dilution solvents and cracked gasses generated from resist materials cause transcriptional defects on template materials in nanoimprint lithography. This study aimed to create the novel gas permeable nanoimprint template materials to prevent transcriptional defects by dilution solvents and cracked gasses from nanopatterning materials. A biomass based template was investigated in thermal and UV nanoimprint lithography, instead of the conventionally template such as quartz, PMDS, DLC, block copolymers, and polymers. The line patterning results using the biomass based gas permeable template in nanoimprint lithography were better to reduce the line pattern failure as compared with that of quartz based template as the standard reference. Gas transmission coefficient, light transmission rate, and hardness in cellulose nanofibers were evaluated for transparent template materials with thermal cross-link urethane groups. The proposed nanoimprint lithography using biomass based template with gas-permeable and gaseous adsorption is one of the most promising processes ready to be investigated for mass-production of nano device applications.

10146-55, Session PS1

Development of novel purifiers with appropriate functional groups based on solvent polarirties

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The ongoing efforts by Integrated Device Manufacturers (IDMs) to improve defectivity on ever shrinking technology nodes and changes of device structure has put pressure on OEMs to reduce metal contamination in photo chemicals. Traditional methods of metals reduction such as distillation, ion-exchange resins service or water-washing processes are increasingly insufficient, particularly for high viscosity polymer solutions. Weak-polar solvents like PGMEA (Propylene Glycol Monomethyl Ether Acetate) or Cyclohexanone has recently been used to dissolve the more hydrophobic photo-resist polymers where current purification technology is inadequate.

In this paper two novel surface modifications were investigated to see their effects on metal removal and to understand the mechanism. The experiments yielded effective purification methods for metal reduction, focusing on solvent polarities based on Hansen Solubility Parameters, and developing optimal purification strategies.

10146-56, Session PS1

Effects of phenolic compound addition to fractionated Novolak-based resists to improve resolution capability(2)

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Novolac resists have been widely used in IC production and are still used in the production of flat panel displays (FPDs) and MEMS. However, with the advent of high-definition products, FPDs increasingly face requirements for finer dimensions. These trends have generated requirements for higher sensitivity, higher resolution, and wider process margin for novolac resists. Using a lithography simulator with the goal of improving the performance of novolac resists, we examined various approaches to improving resist materials. This report discusses efforts to improve resolution and sensitivity using more than before, it is higher.fractionated novolac resins and adding low molecular weight phenol resins.

10146-57, Session PS1

Study for new hardmask process scheme

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Hardmask scheme is one of the key process for the low k process, Actually hardmask scheme has an impact on the patterning and process control such as defect, alignment and OVL. Specially ACL hardmask has OVL issue by bad alignment signal. Therefore, we need new hardmask scheme for OVL improvement. And we can find good candidate scheme, but new scheme has demerits for DCD-FCD skew. And we are trying to study new hardmask scheme to find out how to overcome to skew issue in this paper.

10146-58, Session PS1

Pattern optimizing verification of self-align quadruple patterning

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Through the continuous scaling, complicacy of patterning schemes and increasing costs are considered problematic especially in the case of the application of grid design rule including double patterning. Though the double patterning techniques are still effective for pattern scaling [1], [2]. The double patterning will be essential techniques for EUV application for the future. We reported that the controllability of critical dimensions (CDs) and line edge roughness (LER) is most important factor for the pattern placement in line and space patterns [3]. The CDs and roughness can be controlled to use carbon cores. In this conference, we will discussed the pattern placement control techniques in self-aligned quadruple patterning (SAQP) and introduce newly abbreviated SAQP scheme based on the core of carbon materials.

10146-59, Session PS1

Optimize of shrink process with X-Y CD bias on hole pattern

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We will report cut mask pattern additional process such as smoothing and shrink etch .

This paper focused on X-Y CD bias and comparison of EUV and 193-immersion process.

10146-60, Session PS1

Hole placement error correction for N7 logic and beyond

Kenichi Oyama, Masatoshi Yamato, Kyohei Koike, Syouhei Yamauchi, Arisa Hara, Sakurako Natori, Hidedami Yaegashi, Tokyo Electron Ltd. (Japan)

The continuously down-scaling of FinFET is driving by the self-aligned multiple patterning techniques. Depending on such periodical grid scaling, logic critical design rule has been accelerated to unidirectional design layout. Nowadays Fin, Gate and Metal layers are based on grating with cutting/blocking scheme in N14 and beyond. On the other hand, immersions based pitch splitting of contact hole, via and cutmask are required multiple lithography and etching passes like LEx. Overlay control among multiple exposed patterns become tight and tough, basically the pattern placement in single exposure imaging is made on the assumption of correctly placement. However it's widely known that current immersion NTD resist profile has an asymmetry tapered shape in narrow pitch case. According to our estimation in each resist slice level (Fig.1), resist surface region has a smaller placement error compared with bottom region and its lithographic factors shows a wider process margin in terms of EL and MEEF. Basically thin film resist process might be suitable in this view point, however thinner resist process has happen many concerns by resist process issue. So that background, we'd like to discuss about newly top surface imaging process with tone reverse (Fig.2). In addition, we will talk about not only immersion resist but also EUV resist extendibility.

10146-61, Session PS1

Defectivity reduction for sub-20nm lithography nodes through improved concept design of track dispense hardware

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With the continually shrinking dimensions within the semiconductor industry, the need to reduce on wafer defects is more evident now, than ever. By improving the interaction between the delivery system of photolithography equipment and process chemicals; significant reduction to the amount of particles added on the wafers can lead to increased yield, productivity and overall equipment utilization.

Samsung Austin Semiconductor (SAS) tested a valve that provided an optimized flow path within the valve. With less interruption, the flow proves to be more laminar through the defect reduction dispense valve. Two tests were conducted on a state of the art coat and develop system for high volume manufacturing of sub 20nm technology nodes. One test consisted of SAS's comparison of valve performance, Type 1, standard versus improved defect reduction valve; using the same photolithography chemical. Second test consisted of SAS's valve, Type 2, standard versus improved defect reduction valve using same negative tone developer (NTD) chemical. Utilizing an advanced scanning metrology tool with sub 30nm defect resolution capability, the improved Type 1 and Type 2 valves showed a statistically significant reduction in particles over the conventional standard valves.

Initial testing of Type 1 valves showed an overall decrease of 10 to 15% for back end of line defects of interest on patterned wafers when utilizing the improved valve. In the second experiment, a more than 50% reduction in defects of interest was observed on patterned wafers when using Type 2 improved valve versus standard valve for the negative tone developer chemical. In conclusion, improved designs of both Type 1 and Type 2 valves enabled reducing baseline defect levels for both of the tested photolithography chemicals. Upon completion of the improved defect reduction valve evaluation, further testing will continue using other chemicals within the immersion fleet.

10146-62, Session PS1

Pattern collapse solution for asymmetric pattern

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Smaller and smaller feature size is unavoidable in advanced technology nodes. One of the most critical issues associate with small feature size is pattern collapse, and more serious pattern collapse can be easily observed especially in asymmetric pitch environment due to unbalanced surface tension during development rinse step. The pattern collapse would kill product yield in the worse condition.

This work investigates the approaches of enlarging asymmetric pattern collapse window, such as adjusting photo-resist aspect ratio, applying surfactant during development rinse, and altering underlying anti-reflection coating and hard-mask combinations to tailor the photo-resist bottom profile as well as decreasing developer permeation into photo-resist interface. Pattern sizing to resist unbalanced surface tension was also explored in the asymmetric pattern region. Two novel layout methods to mitigate asymmetric dummy pattern collapse were demonstrated and both methods were confirmed to have higher immunity against pattern collapse in asymmetric environment.

10146-83, Session PS1

New processes associated with electron-beam lithography for ultra-small resonators

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High density ultrahigh resolution patterning with desired shape and size is a crucial requirement in nanotechnology and its applications. Electron beam lithography (EBL) is the most widely used lithography tool in these aspects. However, achieving cost-effective patterning with sub-10-nm critical dimension has been challenging due to the inherent tradeoff between resolution and throughput. Here, we present cost-effective new processes associate with EBL technique, which include optimized resist selection and processing as well as sonicated cold development process. With the new processes, we demonstrate sub-10-nm diameter metal dots at a pitch of ~34 nm and sub-10 nm wide metal lines. With the same processes, we can make U-shape split ring resonator array of different metals with resonator size as small as 60 nm and V-shape SRRs with arm length as short as 50 nm. By reducing the size and arm length of the split ring resonators with the reliable and cost-effect processes, magnetic and electrical resonance across visible and UV range are demonstrated and ultrasensitive biochemical sensors made of such resonator arrays are realized.

10146-63, Session PS2

Design and synthesis of sub-10nm DSA materials

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Following the Moore' s Law, 193 nm multi patterning technology is approaching its resolution limits. As a competing technology, EUVL is getting more mature and widely considered as the next generation litho technology for 7 nm and 5 nm nodes. However, EUV optic system is high cost with low throughput that may limit its applications.

While pure optic resolution is facing big physical and economical challenge, people now look for assistant chemical approaches for sub-10 nm litho. Chemical trimming, chemical shrinking and copolymer lithography have attracted more and more attention. [1-5]

Some phase separating block copolymers are directed to self-assembled

(DSA) into alternative lines, and then form litho patterns through selective etch. Due to its low cost and high potential, the DSA technology has been investigated world wide. [6-11]

Our research interest is to design and synthesize optimal DSA materials with finest intrinsic phase separation resolution, and shortest assembling time. In this study, some block copolymers with low PDI were synthesized through anionic polymerization. The polymer annealing process was carried out without a guiding template, so that only random phase separation structures were observed by Small-Angle X-ray Scattering (SAXS).

The SAXS spectra confirmed the resulted lamella or hexagonal structures with sub-10 nm half-pitch. The smallest lamella structure is repeating at 10 nm or less, and the smallest hexagonal cylindrical structure is repeating at about 15 nm pitch. The assembly time is less than 5 min.

By changing the elemental ratio or the block segment ratio in the copolymers, different lamella phase separation pitches were obtained. These block copolymers show the potential as DSA material with high intrinsic resolution for sub-10 nm and beyond nodes.

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10146-64, Session PS2

Large-scale fabrication of ordered nanostructures based on directed self-assembly of block copolymers on topographically patterned surface

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Block copolymers (BCPs) that consist of two or more chemically distinct polymers covalently linked together at their ends can self-assemble into various well-ordered nanostructures including sphere, cylinder, and lamellae. However, they inevitably meet many defects like dislocation and grain boundary which are regarded as practical limits for potential applications on flat surface during their phase separation. Therefore, these defects are one of the biggest challenges that should be overcome for their direct use. So far there exist several important efforts such as graphoepitaxy, epitaxial growth, e-beam lithography and so on in order to achieve long-rage ordering of nanostructures of the block copolymers. But, it is also known that these approaches reported previously show some critical drawbacks including requirements of complicated multi-step process, expensive templates, etc. In present study, it is investigated the directed self-assembly (DSA) of block copolymers guided by uniaxially oriented nanostripes of poly(tetrafluoro ethylene) (PTFE) produced by rubbing on substrates. As the PTFE bar is mechanically rubbed on various surfaces which are heated at near melting point of PTFE, unique and aligned nanostripes of PTFE having ~ 20 nm of amplitude and ~ 200 nm of pitch are generated in large area because of its unusual physical properties of low friction coefficient and high wear rate. It is noted that the dimension of the nanostripes also can be controlled by applying force and temperatures. Then, polystyrene-block-poly(2-vinylpyridine) copolymers (PS-b-P2VP) are directly spin-coated on the substrates containing well-aligned nanostripes of PTFE on their surfaces and subsequently solvent-annealed in organic vapor to induce the self-assembly of the block copolymers. By adjusting film thickness, types of solvents and solvent-annealing time, extremely ordered P2VP cylinders of S2VP which are oriented perpendicular or parallel to the surface are fabricated in large area because of the guiding effect of the underlying nanostripes of PTFE. In addition, the BCP thin films on the nanostripes are utilized as templates to produce inorganic nano-dot (Si, Au and Pt) on ITO substrate for use in other applications like organic light-emitting diode (OLED).

10146-65, Session PS2

Spatial control of nanostructures on nanoporous templates fabricated by block copolymer based lithography

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In this study, we demonstrate a unique method to localize well-defined nanostructures in large area using nanoporous templates. Cylinder-forming polystyrene-block-poly(2-vinyl pyridine) copolymer (S2VP) is spin-coated on a thin layer of poly(vinyl alcohol) (PVA). To induce phase separation, the thin films of block copolymers (BCPs) are solvent-annealed in vapor of tetrahydrofuran (THF) which is a good solvent for both blocks. As immersed in ethanol that is a selective solvent for P2VP blocks, the surface of BCP thin films is reconstructed and well-ordered nanopores are generated over the whole surface area. Then, the nanopores are successfully transferred to the underlying PVA layer by oxygen plasma treatment. The well-ordered nanopores on PVA can play a role as versatile templates to localize uniform spherical BCP micelles due to surface energy difference and topographical contrast during simple spin-coating process. In addition, well-ordered array of quantum-dots (QDs) having hydrophobic surface is obtained by using nanoporous PVA templates. Interestingly, it is found that their population in a pore with diameter of about 80 nm can be precisely controlled by adjusting the concentrations or the size of QDs. The use of this QDs array can be expanded to various potential applications including QD-LED. As the QDs have been selectively arranged in hexagonally packed nanopores with regular separation distance of about 100 nm, it is possible to generate extremely high density QDs arrays, which is necessary for fabrication of a high resolution colour display based on nano-pixels. The selective arrangements of BCP micelles and QDs are characterized by using scanning electron microscopy (SEM) and atomic force microscopy (AFM). The optical properties of QDs arrays with various diameters are also investigated by UV-Vis spectroscopy.

10146-66, Session PS2

DSA process window expansion with novel DSA track hardware

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PS-b-PMMA block copolymer is a well-known DSA material, and there are many DSA patterning methods that make effective the use of such 1st generation materials. Consequently, this variety of patterning methods opens a wide array of possibilities for DSA application. Last year, during the inaugural International DSA Symposium, researchers and lithographers concurred on common key issues for DSA patterning methods such as: defect density, LWR, placement error, etc. Defect density was specifically expressed as the biggest obstacle for new processes.

Coat-Develop track systems contribute to the DSA pattern fabrication and also influence the DSA pattern performances. In this study, defectivity was investigated using an atmosphere-controlled chamber on the SOKUDO DUO track. As an initial step for expanding the DSA process window, fingerprint patterns were used for various atmospheric conditions during DSA self-assembly annealing. In this study, we will demonstrate an improved DSA process window, and then we will discuss the mechanism for this atmospheric effect.

10146-67, Session PS2

Orientation control of silicon containing block-co-polymer with resolution beyond 10nm

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Directed Self-Assembly (DSA) process is one of the attractive processes for creating the very fine pitch pattern. In this technology, block-co-polymer is the key material to achieve a fine patterning. Many reports are published with Polystyrene-b-Polymethylmethacrylate (PS-b-PMMA) for DSA applications. But it is difficult to achieve the resolution below 10 nm with PS-b-PMMA because of its low chi value. Etching transfer of PS-b-PMMA is also the key issue due to the low etching selectivity between PS and PMMA during dry etching process.

In this report, block-co-polymers that include a Si-containing monomer and an organic monomer were synthesized by living anionic polymerization to supply a high resolution and a high etching contrast. These polymers with a low polydispersity demonstrated lamella morphology that can be oriented by thermal annealing with a neutral surface treatment. The effects of underlayer and top-coat materials were investigated to control the block-co-polymer orientation. These block-co-polymers also achieve a high dry etching contrast.

10146-68, Session PS2

Development of mass production technology for block copolymer lithographic materials

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Directed self-assembly (DSA) is an essential technology for next generation lithography in the field of semiconductor to achieve the nano scale patterning and cost effective patterning. Half pitch (hp) less than 10nm is getting possible to combine DSA lithography technology with various conventional lithography technologies. In DSA lithography process, the pattern is formed using the features that block copolymers (BCPs) form self-assembled structure, so-called microphase-separated structure. The domain spacing of the microphase-separated structure by BCP self-assembly depends on the molecular weight of the polymer (degree of polymerization), which can be controlled by the living anionic polymerization technique. The domain size and resolution of pattern are closely related to the chain dimension of the block copolymers. The next generation target for the micro patterning using BCPs is to form the microphase-separated structure with the hp less than 10 nm. Moreover not only synthesizing copolymer by living anionic polymerization in experimental lab scale, but industrial process for high volume manufacturing is required.

We produced various BCPs: these are polystyrene(PS)-polymethylmethacrylate(PMMA) and poly(4-trimethylsilylstyrene) (PTMSS)-poly(4-hydroxystyrene)(PHOS) system as very strong segregated components (high-χ) and multiblock type of those copolymers which form the microphase-separated structure pattern using living anionic polymerizing method by which the size of polymer can be precisely controled. In addition, we were able to observe alternating lamellar structures which were formed by our various BCPs using small angle X-ray scattering (SAXS) and scanning electron microscope (SEM).

Generally, living anionic polymerization is the most suitable method to control molecular weight of polymer which influenced the size of hp, but it is difficult to maintain stable polymerization because polymerization must be carried out under high-level clean environment. Therefore it is difficult method for mass production. However, we have successfully developed new apparatus for high volume manufacturing including our original technologies such as purification of monomer, high purity wetted parts, and mechanical technology for high vacuum etc. In should be noted that our new apparatus has capacity to synthesize 3kg per batch, and it can be easily scaled up. We have succeeded in high volume manufacturing BCPs for DSA materials using this apparatus.

In this study, we could get results of various evaluations and discuss the possibility of adaptation to semiconductor process using high-? BCPs with microphase-separated structure. And we have discussed about the performance of our new apparatus for high volume manufacturing comparing with some conventional living anionic polymerization processes. In addition we report automatic polymerization apparatus.

10146-69, Session PS2

Influence of processes and materials toward DSA LiNe flow defect mitigation

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In the past years, Directed Self-Assembly (DSA) has been widely explored as a complimentary technique to extend the limits of optical lithography. For line and space patterns obtained with lamellar–phase block copolymers (BCP) using the LiNe flow, efforts have been focused on understanding the origin of DSA–specific defects, as a means to annihilate them and to achieve a low-defect patterning route for the industry. This includes a detailed characterization of the BCP material and the processing conditions, as well as the use of the most advanced optical inspection tools to capture the defects relevant for DSA flows. In this work, we describe our efforts towards improving defect levels, particularly of dislocations and 1–period bridges. We investigated the impact of the dimensions of the guiding stripe and evaluated different approaches to improve on the kinetics of the assembly process to annihilate defects more effectively. Finally, PS-b-PMMA materials with different quality were compared and results are discussed.

10146-70, Session PS2

How do high chi BCP chemical types and process conditions contribute to surface roughness

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Polystyrene (PS) is one of the major components utilized in the synthesis of block copolymer (BCP) formulations. The ability to chemically tune and

modify this polymer has resulted in functionally enhanced polystyrene to improve the performance of directed self-assembly (DSA) materials. The major objective of our study is to characterize and quantify these modified-PS variations to determine the contributions of process conditions as a function of surface roughness. A variety of annealing temperatures (180°C – 260°C) and annealing times (5 min to 20 min) were investigated. An array of plasma etch recipe gas selections (O2 and ArO2) have been studied to determine the effect of multiple monomer additions on the final polystyrene quality after etch. Reference standard PS is compared directly to multiple distinct choices of modified-PS having monomer additions to the baseline polystyrene. Brewer Science provides a complete library of BCPs utilizing L0 values measuring from 28 nm to high ? results with L0 values as low as 12-14 nm with excellent photolithographic capabilities. To accomplish these high ? materials, Brewer Science developed and synthesized specific monomer types to enhance the PS. In addition to high ? properties, Brewer Science's BCP materials have a significant advantage in that no topcoat or solvent annealing is required for alignment of BCPs in guide structures. Understanding the interactions of process anneal temperature, time, and etch processes to the roughness component of enhanced polystyrene has an impact on the photolithography quality metric of edge roughness. One of the most essential lithography criteria to improve is line edge roughness (LER). We believe understanding the direct influence of variations in process condition selections will further improve this metric.

10146-71, Session PS2

Control of interface energies for implementing directed self-assembly of block copolymers in a 300mm CMOS processing line

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Directed Self-Assembly (DSA) of Block Copolymers (BCP) is becoming a well-established method with high potential of gaining industrial relevance. It allows patterning surfaces with high resolution and throughput, and it also offers process simplification compared with alternative approaches [1, 2]. One of the methods to guide the BCPs alignment is chemical epitaxy, which consists in creating chemical patterns on a surface with areas that present larger affinity to one of the two blocks of the BCP [3]. Therefore, by properly tuning the chemical affinity between the surfaces, highly oriented and ordered structures can be achieved.

In this communication, we present a chemo-epitaxy DSA process implemented at 300 mm scale at LETI's block copolymer pilot line. The overall process to create chemical pre-patterns is depicted in figure 1. In the first step of the process, a polystyrene (PS) based brush is grafted on the top of a 300 mm wafer. Then, the chemical pre-patterns are prepared by using e-beam lithography followed by O2 plasma exposure in order to chemically modify the brush. Finally, the resist is stripped by using different solvents and the BCP (lamellar PS-b-PMMA with different chain lengths, L0 = 22- 38 nm) is self-assembled. Multiplication factors ranging from 2L0 to 5L0 have been obtained for PS-PMMA block copolymers and for block copolymers blends.

The mechanism of the lamellar PS-b-PMMA block copolymer alignment is evaluated through the differences of surface free-energy of each copolymer segment and the confining boundary (γSA and γSB), which is the main driving force in chemical epitaxy process. This is experimentally defined by determining the contact angle between PS and PMMA in an homopolymer blend, which has been previously processed in the same way as the block copolymer. In this way, the difference of surface free-energy is estimated by using Young's equation [$\Delta\gamma = \gamma SA - \gamma SB = \gamma AB \cdot \cos(\text{ØAB})$] where γSA and γSB are the interface tensions between homopolymers A and B with the substrate. ØAB is the contact angle between A and B homopolymers, which is obtained from de-wetting experiments. The surface free-energy between the species is determined at each step of the process in order to evaluate the effects of the different chemical treatments (development and resist stripping) in both, modified and un-modified areas. We have analyzed how each process changes its surface free-energy, and so the guiding properties of the chemical patterns. By properly tuning these interactions, aligned L/S patterns are accomplished with density multiplication factors up to 5L0.

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10146-72, Session PS3

Study on thick film spin-on carbon hardmask

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A thick spin-on carbon (SOC) material is designed to overcome inherent problems of amorphous deposited carbon layer (ACL) and thick photoresist. For ACL in use of semiconductor production process, especially when film thickness from sub-micrometer up to few micrometers is required, not only its inherent low transparency at long wavelength light often causes alignment problems with under layers, but also considerable variation of film thickness within a wafer can also cause patterning problems. To avoid these issues, a thick SOC is designed with monomers of high transparency and good solubility at the same time. In comparison with photoresist, the SOC has good etch resistance and high thermal stability, and it provides wide process window of decreased film thickness and increased thermal budget up to 400° after processes such as high temperature deposition of SiON. In order to find key factors along with good solubility to achieve thick uniform film, surface tension and viscosity of surfactant and relationship with coated film will be carefully observed.

10146-73, Session PS3

Study of flowability effect on self-planarization performance at SOC materials

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The importance of self-aligned double patterning (SADP) process using immersion-ArF lithography is ever increasing as the node of semiconductor becomes smaller. However, in SADP process, thickness bias across the pattern is varied to a large extent since a spin-on carbon (SOC) layer needs

to be applied to another pre-patterned SOC layer. In that case, depth-of-focus (DOF) margin becomes smaller which leads to poor reproducibility which is critical in mass production. In order to overcome the deterioration in planarity at SADP process, we studied self-planarizable SOC hardmask material. We successfully controlled the flowability of polymers to achieve desirable level of planarization performance across various underlying substrate pattern topography.

10146-74, Session PS3

Novel spin on planarization technology by photo cross-link SOC (P-SOC)

Takafumi Endo, Nissan Chemical Industries, Ltd. (Japan)

Recently, very fine patterning like less than hp20nm is fabricated by multiple patterning with ArF immersion technology. In this case, it is necessary to use under layer materials which can planarize substrates having hole, trench and topography in order to obtain enough focus margin in lithography step.

Especially, SOC (Spin-on-Carbon) materials are required good via filling performance and high planarization on the topography substrates. Conventional SOC materials which contain polymer and thermal cross-linker are applied thermal curing system by baking process. However, this kind of thermal cure system is difficult to achieve the good planarization because polymer reflow was prohibited by viscosity increasing and causing the film shrinkage during baking.

Therefore, we newly developed photo curing SOC(P-SOC) system which can be cross-link by using UV light. The process flow is coating P-SOC, reflow bake then apply UV exposure. This new system has capability to cross-link by only UV exposure, not by thermal curing. So, the P-SOC achieved high planarization and good via filling performance because they can occur enough reflow without viscosity increasing by reflow bake step and almost no film shrink during reflow bake and photo curing step. This paper describes the design and effect of the P-SOC for the high planarity under layer targeting N5 generation.

10146-75, Session PS3

Development of high-heat resistant polyphenols applied to the spin-on carbon hardmask

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In this paper, we reported on new polyphenols synthesized by the condensation of the combination of phenols and aldehydes. The phenols were 4,4'-biphenol, 2,6-dihydroxynaphthalene and 2,7-dihydroxynaphthalene. The aldehydes were 4-phenylbenzaldehyde and 4,4'-biphenyldicarboxaldehyde. And we evaluated basic properties necessary for the Spin-On Carbon Hardmask. We compared the properties of these compounds, and we investigated the relationship of the structure and the properties.

New polyphenol, NF0A98 was synthesized by the condensation of 2,6-dihydroxynaphthalene and 4,4'-biphenyldicarboxaldehyde. Another new polyphenol, NF7A78 was synthesized by the condensation of 4,4'-biphenol and 4,4'-biphenyldicarboxaldehyde. NF0A98 and NF7A78 showed superior solubility for the coating solvents like PGMEA or PGME, and also showed good heat resistance.

NF0197 synthesized by the condensation of 2,6-dihydroxynaphthalene and 4-phenylbenzaldehyde, showed 5wt% solubility in PGME, and the slightly weight loss until 400 degree Celsius. NF0127 synthesized by the condensation of 2,7-dihydroxynaphthalene and 4-phenylbenzaldehyde, showed less than 2wt% solubility in PGME, and the slightly weight loss until 350 degree Celsius. NF0A28 synthesized by the condensation of 2,7-dihydroxynaphthalene and 4,4'-biphenyldialdehyde, showed 5wt% solubility in PGME, and the slightly weight loss until 450 degree Celsius. NF7177 synthesized by the condensation of 4,4'-biphenol and 4-phenylbenzaldehyde, showed more than 30wt% solubility in PGME, and the slightly weight loss until 400 degree Celsius.

And NF0A98 showed 20wt% solubility in PGME, and the slightly weight loss until 460 degree Celsius. NF7A78 showed more than 30wt% solubility in PGME, and the slightly weight loss until 400 degree Celsius.

So we recognized, in solubility, 4,4'-biphenol was the best raw material of the phenols for polyphenol, and 2,6-dihydroxynaphthalene was better raw material for polyphenol than 2,7-dihydroxynaphthalene. On the other hand, 4,4'-biphenyldialdehyde was better raw material of the aldehydes for polyphenol than 4-phenylbenzaldehyde, in solubility.

As for heat resistance, 2,6-dihydroxynaphthalene was the best raw material of the phenols for polyphenol, 2,7-dihydroxynaphthalene was better raw material for polyphenol than 4,4'-biphenol. But we think that NF7177 and NF7A78 can be crosslinking by heating, so the heat resistance of the polyphenols using 4,4'-biphenol might be improved by optimizing heating condition. On the other hand, 4,4'-biphenyldialdehyde was better raw material of the aldehydes for polyphenol than 4-phenylbenzaldehyde, also in heat resistance.

These materials are low molecular weight of less than 1000, so we expected having a good planarization and gap filling. We are evaluating the performance of the planarization and gap filling.

10146-76, Session PS3

Factors analysis on the physical properties of the low-temperature SOC of memory cell characteristics

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In recent year, it became a critical issue that thermal effect affects the operating of memory cell of integrated semiconductor. As thermal time increases during heat process, thermal stability drops down resulting the degradation of cell operation. Therefore, low temperature process to suppress thermal effect is highly demanded.

In this paper, we introduced LT-SOC (low temperature SOC) to minimize thermal effect. LT-SOC has low temperature cross Linker and it is important to have the capabilities of solubility, coating, pliability, gap-fill, etch resistance and heat tolerance. We verified that the characteristics of hardmask stack and photoresist keep stable with LT-SOC. Moreover, etch selectivity and final pattern profile after etch has been confirmed. It would be expected that cell operation characteristics and electrical properties of memory devices are improved with novel LT-SOC process.

10146-77, Session PS3

Novel silicon hardmask design for collapse margin improvement

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As the critical pitch and critical dimension (CD) continue to shrink, the line collapse margin has become more and more important. For the 20-nm logic node and beyond, due to the resist resolution limit, negative-tone development (NTD) has become a possible approach. Un-like positive tone development (PTD), NTD pattern is formed by removing the unexposed resist with solvent and preserving the exposed resist. The latter is made possible by making the exposed resist more polar, more hydrophilic, and less soluble to the NTD solvent. Due to the resist polarity switch in the

exposure area, the polarity mismatch between the resist polymer and the Silicon hardmask (Si-HM) can sometimes cause pattern collapse.

In this paper, we introduce a new floatable polymer to the Si-HM to reduce polarity mismatch. The additive polymer contains acid-labile group for polarity switch when contacted to acid in the exposure area. Comparing to conventional Si-HM, the floatable additive approach improved the collapse margin by 7 nm

10146-78, Session PS4

Metal reduction at bulk chemical filtration

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Metal impurities are one of the major concerns that potentially deteriorates electronic performance of the semiconductor device[1] In our previous SPIE paper[2], we have demonstrated that Nylon 6,6 filtration is effective in removing metal impurities in organic solvents at point-of-use filtration and found that the removal efficiency depends on the hydrophobicity (octanol water partition coefficient, LogP) of the organic solvent. Also, we have identified that the metal is removed by means of partitioning to the water layer formed on the hydrophilic Nylon 6,6 membrane, similarly to the hydrophilic interaction chromatography, which precedes in mechanism identification on the hydrophilic interactions in organic solvents[3,4]. In bulk filtration at chemical suppliers, typical flow rate per unit filtration area is faster than that in the point-of-use filtration. This may adversely impact the metal removal efficiency. In the current work, we studied metal reduction at a condition in bulk filtration.

Figure 1 shows the test stand used for the metal challenge test on Nylon 6,6 filter in organic solvent. Using the test stand, electronics grade cyclohexanone spiked with each 1 ppb of multiple metals was passed through a Pall 5 nm rated Nylon 6,6 filter, varying flow rate, which include the conditions of both point-of-use and bulk filtration. A result is shown in Figure 2. Removal efficiency for some metals descended depending on the flow rate, while other metals maintained efficiency. For details, removal efficiency of Ca, Cd and Cr was reduced to 80% and for Na, K, Fe, Ag and W was decreased to <40% at a flow rate of bulk filtration. Removal efficiency of Li, Mg, Mn, Co, Ni, Cu, Zn and Pb maintained the same at high efficiency (>90%) regardless of the flow rate. Based on the result, flow rate is found to be one of the key factors for reducing specific kinds of metal impurities in cyclohexanone. Especially Na, K, Fe, Ag and W seem to exhibit weaker interactions to Nylon 6,6 membrane. To further reduce these kinds of metals in bulk filtration, flow rate slower than the typical one is recommended.

In the previous study[2], it was found that removal efficiency of the metals by Nylon 6,6 filter is strongly dependent on the LogP of the organic solvents. It can be expected that the solvent LogP impact the above flow rate dependence of the metal removal efficiency. Different LogP solvents and also filter rating will be explored and discussed in the presentation.

10146-79, Session PS4

Structure property relationship of filtration membranes for negative-tone development (NTD) applications

Lisa Xiao, Rao Varanasi, Michael Mesawich, Eric Shiu, Pall Corp. (United States)

While the negative tone development (NTD) process has become an attractive extension to the most advanced lithography applications, NTD in organic solvents has presented a new set of challenges for contamination control and filtration at both point-of-use and bulk uses. This paper focuses on studying the structure-property relationship of different types of polymeric membranes; such as polytetrafluoroethylene (PTFE), Polyethylene (PE) and Nylon membranes and their interactions with NTD organic solvents. Results, expressed in terms of rinse-up, particle removal efficiency, and chemical compatibility, for membranes of different chemistries, structures and pore sizes, are presented.

10146-80, Session PS4

Continuous improvements of defectivity rates in immersion photolithography via functionalized membranes in point-of-use photochemical filtration

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While the lithography community awaits EUV maturity, the need to extend immersion lithography for multiple patterning schemes continues to grow. In this scenario, continuous defectivity reduction at each patterning step is becoming more and more critical.

Specific "killer-defects", such as micro-line-bridges are one of the key challenges in photolithography's advanced applications. These defects generate from several sources and are very difficult to eliminate. Point-of-use filtration (POU) plays a crucial role on the mitigation, or elimination, of such defects.

Previous studies have demonstrated how the contribution of POU filtration could not be studied independently from photoresists design and track hardware settings. Specifically, we investigated how an effective combination of optimized photoresist, filtration rate, filtration pressure, membrane and device cleaning, single and multilayer filter membranes at optimized pore size could modulate the occurrence of such defects [1, 2 and 3]. The beneficial impact of an asymmetrical filter pore-size-distribution across the membrane thickness on fast filter priming, high retention and high flow was also demonstrated under actual production condition [4].

However, the ultimate desired behavior for POU filtration is the selective retention of defect precursor molecules contained in commercially available photoresist. This optimal behavior can be achieved via customized membrane functionalization. Membrane functionalization provides additional non-sieving interactions which combined with efficient size exclusion can selectively capture certain defect precursors.

The goal of this study is to provide a comprehensive assessment of different functionalization schemes applied on an asymmetric ultra-high molecular weight polyethylene (UPE) membrane of 1nm pore size. Filter priming and startup performance has been studied on bare silicon wafers down to the 26 nm particle size. Defectivity transferred in a 45 nm line 55 nm space (45L/55S) pattern, created through 193 nm immersion (193i) lithography with a positive tone chemically amplified resist (PT-CAR), has been evaluated on organic under-layer coated wafers. Lithography performance, such as critical dimensions (CD), line width roughness (LWR) and line edge roughness (LER) is also assessed via scanning electron microscopy (SEM).

10146-81, Session PS4

Advanced lithographic filtration and contamination control for 14nm node and beyond semiconductor processes

Rao Varanasi, Patrick Connor, Michael Mesawich, Pall Corp. (United States); Archita Sengupta, Intel Corp. (United States)

New challenges and opportunities in process and design innovations continue to emerge in parallel to ever shrinking semiconductor device geometries and technology scaling beyond 14 nm. While Moore's Law is driving the scale reduction, the industry is facing ever-increasing process sensitivity and complexity as well as integration challenges of new materials and the need for unprecedented purity at process maturity. Today, the industry is redefining the on-wafer defect tolerance. The "total" wafer environment contamination characterization and control are essential for yield enhancement with regards to incoming defects to ensure the success

of the latest technology nodes. Due to the increasing number of new materials, device architectures, and cleaning formulations, the severity of killer defects is potentially rising and can remain undetectable without early intervention safeguards in place.

Filtration technology plays a key role and must keep up with not only defect scaling, but with the need for overall cleaner performance. Metals, particulates, fibrous defects, residue defects in the photoresist dispense system have been significant yield detractor for Intel IC manufacturing processes for years and have had a strong impact on various optical photolithography steps (immersion 193/dry 193nm) at some of the most sensitive areas for process defects. In addition, the baseline tolerance of such "wet particle defects" on wafers has been noticeably reduced for <=14nm Nodes. This demand accompanies requirement of significantly cleaner materials from all aspects. Optimized filtration is needed to meet "Paradigm Shift in Defect Tolerance", to remove of <10nm Metals/Particles/Organics/NVR from Chemicals. Filters should "retain", and should neither "react" with process chemistry, nor "add" any of these contaminants. Control must be in place with respect to filter cleanliness, retention rating, nature of filter media/design, filtration rate, and controlled filtration pressure drop versus flux.

This paper explores the performance of a variety of filters utilizing different media meeting the stated goal of retention, without reaction or addition of contaminant. The various filters studied each possess unique characteristics in terms of particle removal, gel retention, flow characteristics and thermal and chemical stability, providing a suite of optimized solutions for the broad array of lithographic applications.

10146-23, Session 9

Nano-defect management in directed self-assembly of block copolymers *(Invited Paper)*

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Directed self-assembly (DSA) of block copolymers (BCPs) has been expected to become one of the most promising next generation lithography candidates for sub-15 nm line patterning and sub-20 nm contact hole patterning. In order to provide the DSA lithography to practical use in advanced semiconductor device manufacturing, defect mitigation in the DSA materials and processes is the primary challenge. We need to clarify the defect generation mechanism using in-situ measurement of self-assembling processes of BCPs in cooperation with modeling approaches to attain the DSA defect mitigation.

In this work, we thus employed in-situ atomic force microscope (AFM) and grazing-incidence small angle X-ray scattering (GI-SAXS) and investigated development of surface morphology as well as internal structure during annealing processes.

Figure 1 shows series of the AFM images of PMAPOSS-b-PTFEMA films during annealing processes. The images clearly show that vitrified sponge-like structure without long-range order in as-spun film transforms into lamellar structure and that the long range order of the lamellar structure increases with annealing temperature. It is well-known that ordering processes of BCPs from disordered state in bulk progress via nucleation and growth. In contrary to the case of bulk, the observed processes seem to be spinodal decomposition. This is because the structure in as-spun film is not the concentration fluctuation of disordered state but the vitrified sponge-like structure. The annealing processes induce order-order transition from non-equilibrium ordered-state to the lamellar structure. The surface tension assists the transition and directs the orientation.

Figure 2 shows scattering patterns of (a) vicinity of film top and (b) whole sample of the GI-SAXS. We can find vertically oriented lamellar structure in the vicinity of film top while horizontally oriented lamellar structures in the vicinity of film bottom, indicating that the GI-SAXS measurement can clarify the variation of the morphologies in depth direction and that the surface tension affects the orientation of the lamellar structure. Finally a combination of the time development data in the in-situ AFM and the GI-SAXS is used to develop a kinetic modeling for prediction of dynamical change in three-dimensional nano-structures.

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10146-24, Session 9

Directed self-assembly enabled fully self-aligned via processing

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Until recent years, dimensional scaling allowed for the fabrication of smaller and faster devices with increasing capacity. Currently, the limited area and the high density of the features in such devices have made self-aligned contacts/vias (SAC or SAV) a standard technique to overcome the decreasing distance between electrically functional elements in integrated circuits. In SAV schemes, the use of hard masks to define the effective transferred patterns allows for more relaxed via patterning conditions and overlay requirements. In this work, we explore a DSA-based fully self-aligned vias (FSAV) flow to further improve on traditional SAV processes. We use directed self-assembly (DSA) of block copolymers (BCP) to generate topographic features between the metal lines, which in combination with SAV, extend the benefits of this method to both X-Y directions, while maximizing the distance between the contacts and the adjacent not-connected metal lines to avoid potential shorts, as shown in Figure 1. In order to achieve this, patterned metal and/or dielectric lines are selectively functionalized using homopolymer brushes, to form a 1:1 chemical nano-pattern of specific surface energy, such that, when a BCP layer is coated and annealed on these samples, each block will align to the metal (or dielectric) lines underneath, as shown on Figure 2. We subsequently use one of the blocks as a template to generate topographic features between the metal lines. In addition, different hard masks are characterized to find the optimal material for the current scheme. Finally, we define the design rules for integration of the proposed flow into electrical devices.

10146-25, Session 9

Electrical study of DSA shrink process and CD rectification effect at sub-60nm using EUV test vehicle

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Directed self-assembly (DSA) of block copolymers (BCPs) provides material-controlled CD uniformity and process simplicity, which is very critical for advanced nodes applications.[1] DSA of lamella-forming BCP has become a promising candidate for forming self-aligned via (SAV), which requires the DSA process to support structures from circular via to lines and spaces. [2] The basic process flow is similar to general graphoepitaxy

method. [3] Combined with EUV, DSA shrink with PS-philic sidewall process has been applied to enable sub 60nm pitch dense vias. The top down images taken at different process stages are shown in Figure 1 (left). The LCDU of minor axis was improved by 30% after DSA Shrink process. Meanwhile, a large CD reduction in the major axis was observed for this particular process. (Figure 1, right)

To further study the integrity and the benefits of the DSA process, via-chain test structures were fabricated using DSA and baseline process for via formation while metal layer processes remain the same. [4,5] Both dense, i.e. center-to-center (c2c) distance below 60nm, and isolated, i.e. c2c > 400 nm, via-chain structures were investigated. We compared several DSA Via shrink processes and a DSA control process, in which GP was directly transferred to the bottom OPL without DSA shrink, as shown in Fig. 2. The DSA control resulted in larger CD than other cases, thus, shorted the dense via chains. However, this group showed slightly better yield in iso via-chains. The two DSA shrink processes compared here are mainly for aspect ratio, CD uniformity, and placement control. We demonstrated that an initial DSA shrink process may create more circular vias than the GP and then lose the benefits from SAV process. Similar effect was observed if the placement accuracy of the DSA vias were affected by the DSA and pattern transfer. We also explored the electrical current distribution of different experimental conditions as an indicator of the local CDU and compared to the structural learning. Furthermore, the challenges and strategies applied to improve local CD uniformity and current distribution will be discussed.

10146-26, Session 10

Dual brush process for selective surface modification in graphoepitaxy directed self-assembly

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Graphoepitaxy directed self-assembly is a potential solution for patterning contact holes with pitches beyond the reach of a single lithographic exposure. In this process, lithography is used to create a topographic pre-pattern consisting of trench-like templates in which a cylindrical block copolymer is deposited and allowed to phase separate before the minority block is removed, resulting in one or multiple sub-resolution holes within each template. Earlier research shows selective control of the interfacial energy at the bottom and sidewall of the template is crucial. Conventionally, this is done by surface-specific chemical attachment of an end-functionalized polymer brush prior to block copolymer coating. In this work, a dual brush process is implemented, in which two brushes with distinct end-groups are consecutively grafted to the pre-pattern to achieve fully independent modification of the bottom and sidewall surface of the template. As a result, this approach is more effective in controlling the interfacial interactions than single brush methods. Therefore, a considerably larger process window for doublets (two-hole features in elliptical templates) with a sidewall surface affinity for the majority block can be achieved.

10146-27, Session 10

Use of ALD sequential infiltration synthesis to improve the pattern transfer on directed self-assembly high-X PS-b-PLA bock copolymers

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Directed self-assembly of block copolymers is considered one of the candidates to fulfill the requirements of the next technological nodes [1,2]. Polymer domains are aligned by using a chemical and/or a topographical pre-pattern in which preferential surfaces to one of the two blocks or neutral wetting areas are created. In particular, polystyrene-block-polymetylmethacrylate (PS-b-PMMA) has been extensively studied during the last years showing strong capabilities to define periodic nanostructures. However, the relatively low Flory-Huggins parameter and, the resulting low segregation strength of PS-b-PMMA systems, limit their achievable resolution to around 11 nm [3]. The application of block copolymer on sub-10 nm technologies requires the development of the new block copolymer generation known as high- block copolymers. Additionally, an important requirement for their integration on the lithography roadmap is the capability of selectively remove one of the two blocks. The etch contrast between the two domains is typically low due to their organic chemistry. In this sense, selective sequential infiltration synthesis by ALD into one of the blocks can be used in order to incorporate an inorganic material. The formed organic/inorganic blend sustains better the plasma etching to remove the non-infiltrated organic block.

In this contribution, we show the use of high- polystyrene-b-polylactide acid (PS-b-PLA) lamellar block copolymer for line/space applications. PS-b-PLA has a larger Flory-Huggins parameter (=0.218 at room temperature[4]) compared with PS-b-PMMA, allowing the size reduction of the self-assembled domains. The method to control the orientation of the polymer domains is similar to the one typically used for PS-b-PMMA. Chemical contrast and the subsequent alignment of the polymer domains are achieved by the definition of a chemical pre-pattern on a random copolymer PS-r-PMMA (48% of PS) (figure 1). The polymer brush is grafted on the substrate and then locally modified by the combination of e-beam lithography and soft oxygen plasma. Afterwards, the PS-b-PLA block copolymer is spin-coated and thermally annealed on the chemically pre-patterned substrate. A chemical contrast is observed between the modified and unmodified stripes. While, the lamellar domains are oriented perpendicular to the substrate on unmodified areas, PLA domains are strongly attracted to the O2 modified surfaces inducing a parallel orientation to the substrate. Additionally, the wetting behavior of the polymer domains is also studied through the difference of surface free energy between the substrate and each polymer block. The energy estimated by the Young's equation [$\Delta\gamma = \gamma SA - \gamma SB = \gamma AB \cdot \cos(\O AB)$], where γSA and γSB are the interface tensions between homo-polymers A and B with the substrate, and ØAB is the contact angle between A and B homo-polymers which is obtained in de-wetting experiments.

Finally, sequential infiltration synthesis is used to selectively infiltrate alumina (Al3O2) on PLA domains (figure 2). A selective infiltration is achieved because the precursor molecules react with the carbonyl (C=O) groups that are only present in the PLA block. After five cycles of SIS, the SIS modified PLA domains become more resistant to O2 plasma etching than PS enabling the PS etching without using other kind of hard-masks.

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10146-28, Session 11

Topcoat-free strategies for orientation control of all-organic high-χ block copolymers

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Directed self-assembly (DSA) of block copolymers (BCP) is a promising candidate for extending the patterning capability of conventional lithography. While PS-b-PMMA is the most widely used block copolymer for DSA, the minimum half-pitch of this BCP is limited to ~10nm because of the low interaction parameter (chi) between PS and PMMA blocks. Higher-chi BCPs (e.g. PS-b-PEO, PS-b-P2VP, PS-b-PTMSS, etc.) capable of smaller natural period, the Lo, are expected to be necessary for patterning for sub-10nm IC (integrated circuit) devices. But due to the increased mismatch in the surface energies of the two blocks of high-chi BCP, only the lower surface energy block is present at the polymer-air interface, rendering the thin-film undesirable for lithographic applications. Previously, we had discussed a formulation-based approach in which a surface active polymer (SAP) was added as an additive to enable perpendicular orientation control of polycarbonate-containing high-chi BCPs (Figure 1) using a coat and a short thermal annealing step on neutral underlayer modified substrates (Gen. 1 BCP).

To further improve the robustness of the BCP material and make it more integration-friendly for DSA processing, an additive free high-chi BCP platform (Gen. 2 BCP, Figure 2) that forms vertically oriented features upon thermal annealing on a wide range on underlayer compositions was developed. In this talk, the development and performance of Gen 2. BCP platform will be discussed. Specifically, the thin-film characterization by AFM and GISAXS to confirm perpendicular orientation, and the effect of thermal annealing conditions and underlayer composition on self-assembly behavior of the lamellae forming BCPs will be detailed. Next, the DSA, etch, and pattern transfer of the Gen. 2 BCP will be highlighted. Finally, the advantages and the limitations of Gen. 1 and Gen. 2 high-chi BCPs will be compared with respect to sub-20 nm pitch patterning.

10146-29, Session 11

Directed self-assembly of high-χ block copolymers without the need for topcoat or solvent annealing

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Poly(styrene-b-methyl methacrylate) (PS-b-PMMA) is the current benchmark block copolymer (BCP) material for direct self-assembly (DSA) patterning, which stands out by its simple requirement of thermal annealing alone to obtain vertically orientated polymer micro-domains for pattering. However, PS-b-PMMA is known to have a scale limit of obtainable features of around 11 nm due to its low ? value. In order to gain sub?10 nm features, high-? block copolymers are desired, but most of the ones reported in literature require topcoat or solvent annealing to get vertical orientation for DSA pattering. With the motivation to simplify DSA processing, we have developed high-? block copolymers that do not need topcoat or solvent annealing to get vertical orientation and can produce pattern features as small as 5 nm. Lamellae-forming high-? block copolymers with a L0 range of 10-20 nm (5-10 nm line/space features) and cylinder-forming high-? block copolymers with 4-10 nm cylinders (vertical holes or rods) have been successfully prepared and their orientation controlled by simple thermal annealing for a short time (≤10 min) have been demonstrated. Pattern development by dry etching and DSA performance of these high-? block copolymers has also shown great promise.

The high-? block copolymers are di-block copolymers with organic polymer blocks, e.g., PS and PMMA analogues, which can be easily synthesized by two-step controlled radical polymerization reactions. These block copolymers have polydispersity index (PDI) of no more than 1.15 as characterized by gel permeation chromatography (GPC). We have successfully prepared a family of lamellae-forming and also cylinder-forming high-? block copolymers. A L0 range of 10-20 nm with 1-2-nm intervals has been obtained by lamellae-forming block copolymers, which show 5-10 nm line-space features. A size range of 4-10-nm cylinder structures, e.g. holes or rods, has also been obtained by cylinder-forming block copolymers. Orientation control of these block copolymers can be realized by thermal annealing alone. For example, a thin layer of block copolymer is spin coated onto a substrate that is pre-coated with a selected neutral layer, and then baked on a hot plate at typical 140-200 °C for 5-10 minutes. Success of vertical orientation control is confirmed by scanning electron microscopy (SEM) after a short time etch of removing the sacrificial polymer block, e.g., line-space features (i.e. fingerprint) can be seen in the lamellae block copolymer, and hexagonally packed holes/rods can be seen in cylinder block copolymers. Studies on patter transfer by dry etch and DSA alignment of the high-? block copolymers is still ongoing, and preliminary results will be summarized and presented later.

10146-30, Session 11

Directed self-assembly of 5nm block copolymer lamellae

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The relentless drive for high-resolution patterning materials has promoted the development of new, high-? block copolymers (BCPs) for lithography(1). In particular, lamellar BCPs capable of forming perpendicular 5 nm features in thin films are highly sought after, because the feature sizes naturally produced by these materials rival the resolution of combined litho/multiple patterning processes operating at their absolute technological boundaries. By pushing the limits of chemical incompatibility between polymer blocks, we have recently demonstrated the self-assembly of 5 nm line/space patterns in thin films using poly(5-vinyl-1,3-benzodioxole-block-pentamethyldisilylstyrene) (PVBD-b-PDSS, L0 = 10 nm). When incorporated into a hybrid chemo-/grapho- epitaxy directed self-assembly (DSA) process, highly ordered 5 nm BCP lamellae were produced in thin films using thermal annealing. Nanoimprint lithography (NIL) provided thin guidestripes for BCP alignment, and systematic variation of the height of the NIL guidestripes demonstrated that topography plays an important role in promoting defect-free self-assembly. Cross-sectional analysis revealed key process parameters responsible for promoting vertical through-film structures. Sophisticated etching techniques have been developed to enable the full development and pattern transfer of these very small BCP patterns into an underlying substrate. These results represent a significant advancement for demanding patterning applications such as fabricating high-density NIL templates for bit-patterned media.

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10146-31, Session 11

A track process for solvent annealing of high chi BCPs

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Directed Self Assembly (DSA) is a promising technology for complementary patterning in future nodes. Several polymeric systems have been proposed in the literature, with the most currently studied being a block copolymer (BCP) from Polystyrene (PS) and Poly(methyl methacrylate) (PMMA). The phase separation for the PS-b-PMMA BCP is primarily achieved by thermal annealing. In some cases, thermal anneal times required in a track process exceed most standard process for high volume manufacturing.

There have been new BCPs proposed that can be induced to phase separate using solvent vapor instead of heat. Solvent annealing times are traditionally thought to be longer than thermal annealing. In this study, we investigated the feasibility of performing solvent annealing in a 300 mm track. High chi BCPs were prepared and evaluated based on their ability to form fingerprint structures. Annealing times, temperature and solvent composition were the primary variables in the study.

10146-32, Session 11

Liquid crystals for sub-5nm nanopatterning

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The directed self-assembly of block copolymers is an exciting technology that promises to push the resolution limit of optical lithography by aligning micro-phase separated block copolymers in guiding structures. Poly(dimethylsiloxane)-containing block copolymers are particularly useful due to their high etch contrast, which allows pattern transfer into an underlying layer. Further downscaling of feature sizes is however difficult with block copolymers as the immiscibility based self-assembly runs out of steam beyond 10 nanometers, where micro-phase separation no longer occurs. In addition, defects are stabilized by a lower thermodynamic driving force for micro-phase separation at shorter block lengths, even though the industry tolerance for defects is extremely low (< 0.01 cm2).

The strategy to prepare sub 5m features by the self-assembly of liquid crystals is regarded as the ultimate step for high-?, low-N materials,1 but it has never been demonstrated. We have recently developed monodisperse oligo(dimethylsiloxane) liquid crystals for nanopatterning applications. [2] These novel materials form ordered phases on the order of several nanometers due to their molecular design, multiple times smaller than block copolymers, and at inherently low defectivities. The anisotropic nature of the materials allows for additional alignment techniques such as, for example, photo-alignment. We also demonstrate that the features can be easily aligned within lithographic guiding structures. Highly ordered patterns were obtained at feature sizes multiple times smaller than previously reported, without the need for additional annealing. In this talk, we will discuss the possibilities that these liquid crystalline materials can provide for nanopatterning, and highlight the remaining challenges in utilizing these novel materials as self-assembled resists.

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10146-33, Session 11

Hemicellulose block copolymers made from woods for wide-range directed self-assembly lithography enabling wider range of applicable patterning size

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An importance of green chemistry is growing up because of the serious global warming problem in the world. Disappointingly the semiconductor industries pay little attention to that. Hemicellulose made from plants is one of the green chemicals. Xylan is one of hemicellulose family and a component of plant cell wall from hard woods. It shows higher hydrophilic property. This paper describes new sustainable hemicellulose high chi block copolymer using xylan and its wider range of patterning size results on directed self-assembly for semiconductor application.

Xylan has many hydroxy groups in one molecule . It means that xylan block copolymer has a potential for high chi block copolymer. Generally, it is too difficult to create smaller size and larger size phase separation on DSA lithography. Xylan block copolymer is promised not only smaller size separation but also larger size separation with less placement errors, shorter annealing time and low defect density thanks to its strong phase separation property.

Experimental results using xylan block copolymers of 20nm hexagonal separated holes in hole guides, 5.4nm L/S patterns in trench guides, 41nm hexagonal holes on post guides will be reported.

10146-34, Session 12

Optimized phase field models in confinement: fast and accurate simulations of directed self-assembly

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To design processes that effectively use directed self-assembly (DSA), we would like to have a complete picture of stable and defective polymer configurations. Field-theoretic simulations are an effective way to gain knowledge about these configurations and predict defect populations. Using these simulations, we can easily vary design parameters such as prepattern dimensions, wetting conditions and polymer composition and observe their effects on pattern formation.

All successful simulation models strike some balance of computational speed and accuracy. The simplest models, phase field models such as the Ohta-Kawasaki (OK) model, are fast and usually qualitatively accurate. On the other extreme, when thermal fluctuations are important to polymer behavior, an expensive method such as complex Langevin sampling is required to produce accurate results. For many applications, the appropriate model lies between these two extremes, such as self-consistent field theory (SCFT) or the similar theoretically informed coarse grain (TICG) model.

We previously developed a more accurate phase field model by drawing information from SCFT. This optimized phase field (OPF) model is just as fast as the OK model, but makes better predictions of domain spacing and defect formation energies (and thus of defect populations) in the bulk. We now extend this model to confined templates with chemoepitaxy and/or graphoepitaxy guiding patterns.

To complete this extension, we resolve several issues typical of phase field models including the OK model. Using a field variable transformation, we prevent the model from describing nonphysical volume fractions (outside

the range 0-1). We then use the masking method to define walls that confine the polymer and interact with polymer at the boundary. This strategy, also employed in SCFT, allows us to define walls with any geometry by including them in the simulation.

Figure 1 shows two simple defects for a PS-PMMA diblock copolymer in lateral confinement computed by the OPF model. Defect formation energies are comparable to the values calculated by SCFT, but the OPF calculation can be completed much faster than SCFT. This increase in performance makes the OPF model well-suited to rapid prototyping of complex DSA templates.

In this study, we will report on a newfound capability to conduct DSA simulations in large, complex templates with an accuracy comparable to the SCFT standard, but up to two orders of magnitude faster.

10146-35, Session 12

Estimation of effects of thermal fluctuations in graphoepitaxy DSA of cylinder-forming block copolymers

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Thermal fluctuations of the block copolymer (BCP) molecules during the annealing step of DSA process result in roughness of the edges formed in DSA lithography. In a particular case of DSA lithography with cylinder-forming BCPs used to pattern vias of the integrated circuits, the effects of thermal fluctuations are manifested as variations in the placement and diameter of vias. Such variations, driven by thermal fluctuations, lead to alignment and CD errors for these vias, and the need to estimate and mitigate such effects has been understood in the industry [1-3].

The effects of thermal fluctuations in graphoepitaxy DSA are studied using simulations based on the self-consistent field theory (SCFT) model. The method [1-2] based on using an external potential field to displace or deform the DSA cylinder is employed to study the dependencies of the fluctuations of the position and the size of the DSA cylinder on the confinement well diameter. Similarly to previously published[2] experimental and simulated results, a minimum in dependencies of standard deviations of a DSA cylinder placement and a DSA cylinder diameter on the diameter of a confinement well is observed. An explanation to local minima of these dependencies is proposed.

A drawback of the approach[1-2] to the estimation of the thermal fluctuation effects is that it requires conducting multiple SCFT simulations sampling the different magnitudes of displacements or deformations of DSA features by artificially applied external potential field. Depending on the required accuracy and the complexity of the DSA result, such multiple simulations may take a long time to complete. An alternative method is presented and discussed in this paper. This method uses a family of perturbations in SCFT potential fields, resulting in a displacement or deformation of a DSA cylinder. The use of the proposed method does not require solutions of multiple SCFT problems, resulting in a significantly faster execution times, compared to the method[1-2].

A comparison of the results of both methods is presented, followed by a discussion of the variations of these methods and their advantages and disadvantages.

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10146-36, Session 12

Suppression of thermal fluctuation placement errors in linear arrays of block copolymer cylinders

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Directed self-assembly (DSA) of block copolymers has attracted much interest for its use as a low-cost, high-throughput patterning tool to supplement existing lithographic techniques, and especially for its ability to easily pattern vertical interconnect accesses (VIAs). Assembling multiple cylinders in a single template has obvious advantages for feature density increase. However, denser patterning comes at a cost, due to more abundant defect modes and increased susceptibility to placement errors due to thermal fluctuations. Linear arrays of cylinders have been shown to contain collective excitations, leading to unbounded positional variance away from their equilibrium locations in a manner analogous to a one-dimensional crystal. In order to reduce this positional uncertainty, we introduce chemically selective stripes on the substrate of the system. These chemoepitaxially patterned regions create an energetic preference for the equilibrium configuration of the system, "pinning" the VIAs in place.

In this study, we use three-dimensional self-consistent field theory (SCFT) simulations and Complex Langevin (CL) sampling to investigate the effects of thermal fluctuations on cylinder positions in linear arrays of VIAs with preferentially striped substrates. We interrogate the relationship between stripe interaction strength and positional variance, compare the magnitude of reduction with a Landau-Peierls analysis on a simplified system, and propose a predictive model for placement error in similarly chemopatterned systems. Since the cylinders are flexible, we propose a maximum system height for linear arrays with acceptably low placement error.

10146-37, Session 12

Evaluating structure in thin BCP films with soft x-rays

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The semiconductor industry is evaluating a variety of approaches for the cost efficient production of future processing and memory generations. Amongst the technologies being explored are multiple patterning steps, extreme ultraviolet (EUV) lithography, multiple-beam electron beam lithography and the directed self-assembly (DSA) of block copolymers (BCPs). BCP DSA utilizes a chemical or topographical template to induce long range order in a thin film of BCP which enhances the resolution of the original pattern.

The characterization of buried structure within a DSA BCP film is challenging due to the lack of contrast between the organic materials. Critical-dimension small angle x-ray scattering (CDSAXS) measurements were performed on DSA BCP films, using soft X-rays to tune the contrast, in order to understand the relationship between template structure and film morphology.1 The results of these measurements show that as the width of the guiding stripe widens the arrangement of the BCP on the guiding stripe inverts, shifting from the A block being centered on the guiding stripe to the B block being centered on the guiding stripe. The initial results of integration of mean field

simulations into the analysis of scattering data will also be discussed.

In addition to examining the BCP structure with CDSAXS, soft X-ray reflectivity2 measurements were performed on BCP to better understand the relationship between interface width for systems with alternative architectures (triblocks) and additives (polymers/ionic liquids). The addition of a selectively associating additive increases the interaction parameter between the two blocks, resulting in the reduction of the interface width and access to smaller pitches. The use of soft X-ray reflectivity allows the evaluation of the distribution of the additive.

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10146-38, Session 12

Lamellar orientation of block copolymer using polarity switch of Nitrophenyl self-assembled monolayer (SAM) induced by electron beam

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The combination of top-down and bottom-up approaches to nanopatterning has become an interesting research focus area. Recently, directed self-assembly (DSA) of block copolymers has abstracted significant research attentions as a promising nanolithography to surmount the fundamental limitations of conventional lithography. Controlling the surface chemistry of specific regions to locally change the orientation of block copolymer domains is very valuable by top-down lithography. In particular, EB lithography is suitable for the modification of substrate surface. The neutral wettability to the polystyrene-block-poly(methyl methacrylate) (PS-b-PMMA) block copolymers on modified surfaces such as random styrene-methacrylate copolymer films (PS-r-PMMA) or self-assembled monolayers (SAMs) has been studied to induce perpendicular orientation. However, current methods for achieving their patterned substrate template are generally complex. In this study, we investigated whether DSA of PS-b-PMMA films could be performed using lithographic modification of SAMs, such as the conversion of the NO2 group to an NH2 group induced by EB irradiation.

SAMs layers were spin-coated on a substrate, and then irradiated with EB to produce a patterned SAM layer. Then, PS-b-PMMA block copolymer was spin-coated from propylene glycol mono methyl ether acetate (PGMEA) solutions onto the patterned SAM layer coated substrates after EB irradiation. Subsequently, they were annealed at various temperatures in a vacuum for a sufficiently long time. The annealed film was also treated with an oxygen reactive ion etching (RIE) process. The resulting morphology was recorded using field emission-scanning electron microscopy (FE-SEM).

Lamellar orientation of the PS-b-PMMA block copolymer could be performed using the change of SAMs such as the conversion of the NO2 group to an NH2 group induced by EB irradiation. The resulting chemical patterns provide neutral surface layers for lamella orientation of PS-b-PMMA domains. To our knowledge, this is the first example of creation of a neutral layer using the reductive treatment of EB irradiation, and this work provides insights on tuning the neutral layer and the vertical orientation conditions for appropriate irradiation dose and annealing temperature. Though the main obstacle for this process is controlling the alignment of the domains to accomplish DSA, this method can greatly simplify block copolymer DSA processes as compared to the multi-step fabrication procedures currently used.

10146-39, Session 12

DSA via hole shrink for advanced node applications

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In recent years major advancements have been made in the directed self-assembly (DSA) of block copolymers (BCPs). DSA is a promising complementary patterning technique for future node integrated circuit (IC) device manufacturing and is seriously considered for the 7 nm node and beyond. One of the most straightforward approaches for implementation of DSA is via patterning by graphoepitaxy. In this approach, the guiding pattern dictates the location and pitch of the resulting hole structures while the material properties of the BCPs control the feature size and uniformity. As device node is smaller, the influence of defects and CD variation of the pattern to the yield in manufacturing is more significant. Here, we show strategies how to improve defectivity and CDU performance in DSA by controlling the surface property of the template and the self-assembly of BCPs. We developed polymer brush materials to selectively modify the bottom of the template hole and the surface between the holes to be neutral to both of the BCP blocks and the sidewall to be preferential to either of the BCP blocks. Applying these new materials & process reduces missing vias, creates a uniform coating and results in a decrease in defect density. Additionally, we established different processes (e.g. increase of grafting density of the brush materials or tuning the selectivity of the sidewalls) to promote the phase separation of BCP leading to higher overall shrink amount and better CDU

10146-40, Session 13

Development of Ti containing hardmasks through PEALD deposition

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With evolving of complex integration schemes, tri layer patterning with a solvent strippable hardmask can have a variety of applications. Spin on metal hardmasks have been the key enabler for selective removal through wets when active areas need to be protected from dry etch damage. As spin on metal hardmasks require a dedicated track to prevent metal contamination and are limited to scaling down thickness without comprising on defectivity, there has been a need for a deposited hardmask solution. This paper presents a systematic study on developing a PEALD deposited Ti containing hardmasks for patterning applications. Due to deposition techniques, low film defectivity is attained at thickness in the <50A range. We demonstrate lithography process window, profile and defectivity evaluation for a tri layer scheme patterned with PEALD based Ti hardmask and its performance under dry and wet strip conditions. Comparable structural and electrical performance is shown for a deposited vs a spin on metal hardmask.

10146-41, Session 13

Investigation on hard mask integration

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As the node size shrinks, it requires thin photoresist (PR) and hardmask layers to keep the same aspect ratio for the fine pattern manufacturing. There are two possible hardmask integration schemes for spin-on-hardmask (SOH) application: quad-layer and tri-layer systems. Quad-layer system has PR / bottom anti-reflective coating (BARC) / silicon oxynitride (SiON) / amorphous-carbon-layer (ACL) or SOH and tri-layer system has PR / Si-rich anti-reflective coating (Si-ARC) / SOH. Due to the different structure and process between quad- and tri- layer system, each system needs specific chemical and physical properties of the hardmask. We have studied the properties of the hardmask and proposed the adequate SOH candidates for quad- and tri- layer applications and hard mask integration.

10146-42, Session 13

Novel gap filling BARC with high chemical resistance

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In the recent of the semiconductor manufacturing process, variety of properties?(narrow gap-filling and planarity etc.) are required to organic BARC in addition to the conventional requirements. Moreover, SC-1 resistance is also needed because BARC is often used as a wet etching mask when TiN processing. But conventional BARC which include crosslinker doesn't have enough SC-1 resistance, and we found that it is also difficult to obtain good gap-filling and good planarity because of outgassing and film shrinkage derived from the crosslinker.

In this study, we have developed the new self-crosslinking BARC with new crosslinking system. The new crosslinking system shows low outgassing and film shrinkage because of not including crosslinker. So, novel BARC has better gap filling property and planarity and over 3 times higher SC-1 resistance than that of conventional BARC. Moreover, by adding the low molecular weight additive which has high adhesive unit to substrate, the novel BARC has over 10 times higher SC-1 resistance than that of conventional BARC.

And this novel BARC can be applied both ArF & KrF lithography process because of broad absorbance, high etching rate, chemical resistance (SC-1, SC-2, DHF, and others) and good film thickness uniformity.

In this paper, we will discuss the detail of new self-crosslinking BARC in excellent total performance and our approach to achieve high chemical resistance.

10146-43, Session 13

CMOS patterning over high-aspect ratio topographies for N10/N7 using spin-on carbon hardmasks

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The ever-decreasing gate pitch required to facilitate advanced CMOS technology nodes coupled with the need for taller dummy gate stacks will result in much higher aspect ratios at N10/N7 than are found within current CMOS architectures. At these nodes standard lithography approaches will no longer be adequate to handle patterning requirements: the current generation of BARC materials is unable to properly gapfill such high aspect ratio topographies, leading to voids that will affect the litho performance. Furthermore, the light from exposure tools is not even able to fully penetrate the gaps between such dense structures in order to expose photoresist in all areas, potentially causing serious scumming issues. Alternative approaches and materials will therefore be required both in order to gapfill high aspect ratio topographies, as well as to maintain acceptable patterning performance in both litho and etch while still remaining compatible with the underlying CMOS device structures.

We have demonstrated proof-of-principle implementations of trilayer spin-on carbon (SOC)/spin-on glass (SOG) patterning schemes as a replacement for BARC, and have created strategies that can selectively remove the SOG layer after hardmask opening while still maintaining the integrity of the underlying CMOS devices. For applications where wet etching is allowable, a dedicated HF-resistant SOC material can be utilized which allows the SOG layer to be wet etched before a subsequent SOC dry etch removal, without any damage to gates or fins. In applications where the wet etching of SOG is not feasible, for example within implantation blocking layers where the fins to be implanted are covered only by a thin oxide cap that would be damaged in such a process, we have developed a novel patterning scheme based on the coating of a second SOC material after hardmask open, with a partial etchback to allow for SOG removal while protecting the device architecture underneath. Utilizing this approach we have demonstrated that an equivalent electrical performance can be obtained from CMOS devices at N14 dimensions where both NMOS and PMOS extension and halo implants were performed with a trilayer implant mask in place of a standard photoresist implant mask.

10146-44, Session 13

Development of the Inkjet-enabled adaptive planarization process

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Planarization is a critical unit step in the lithography process because it enables patterning of surfaces with versatile pattern density without compromising on the stringent planarity and depth-of-focus requirements. In addition to nanoscale pattern density variation, parasitics such as pre-existing wafer topography, can corrupt the desired process output after planarization. The topography of any surface can be classified in three broad categories, depending upon the amplitude and spatial wavelength of the same [1], [2]: (i) nominal shape, (ii) nanotopography and (iii) roughness. The nominal shape is given by the largest spatial wavelengths, typically > 20mm. For spatial length scales of ~1-20mm, height variations at this spatial wavelength range are classified as nanotopography. Roughness usually has lower spatial wavelengths. While the nominal shape of a substrate surface is usually decided by the nature of wafer preparation and the tooling and chucking infrastructure used in the same, roughness is usually mitigated by standard polishing techniques. It is the intermediate nanotopography that is probably the most critical surface topography parameter. This is because most traditional polishing techniques cannot selectively address pre-existing substrate topography, without introducing a parasitic signature at the scale of nanotopography. Moreover, fields with pattern density variation typically also have length scales that are commensurate with nanotopography. It is thus instructive to summarize existing planarization technology to understand current limitations.

Spin on Glass and Etch back is one technique used for micron scale device manufacturing [3]. As the name implies, a glass dielectric is spin-coated on the substrate followed by etching in a chemistry that ensures equal etching rates for both the sacrificial glass and the underlying film or substrate material. Photoresists may also be used instead of glass. However, the global planarity that can be achieved by this technique is limited. Also, planarization over a large isolated topographical feature has been studied

for the reverse-tone Jet-and-Flash Imprint Lithography process, also known as JFIL-R [4]. This relies on surface tension and capillary effects to smoothen a spin-coated Si containing film that can be etched to obtain a smooth profile.

To meet the stringent requirement of planarity in submicron device technologies Chemical Mechanical Planarization (CMP) is the most widely used planarization technology [5], [6]. It uses a combination of abrasive laden chemical slurry and a mechanical pad for achieving planar profiles. The biggest concern with CMP is the dependence of material removal rate on the pattern density of material, leading to the formation of a step between the high density and low-density. The step shows up as a long-range thickness variation in the planarized film, similar in scale to pre-existing substrate topography that should have been polished away. Preventive techniques like dummy fill and patterned resist can be used to reduce the variation in pattern density. These techniques increase the complexity of the planarization process and significantly limit the device design flexibility.

Contact Planarization (CP) has also been reported as an alternative to the CMP processing [7], [8]. A substrate is spin coated with a photo curable material and pre baked to remove residual solvent. An ultra-flat surface or an optical flat is pressed on the spin-coated wafer. The material is forced to reflow. Pressure is used to spread out material evenly and achieve global planarization. The substrate is then exposed to UV radiation to harden the photo curable material. Although attractive, this process is not adaptive as it does not account for differences in surface topography of the wafer and the optical flat, nor can it address all the parasitics that arise during the process itself. The optical flat leads to undesirable planarization of even the substrate nominal shape and nanotopography, which corrupts the final film thickness profile. Hence, it becomes extremely difficult to eliminate this signature to a desirable extent without introducing other parasitic signatures. An example of this is shown in Figure 1.

In this paper, a novel adaptive planarization process has been presented that potentially addresses the problems associated with planarization of varying pattern density, even in the presence of pre-existing substrate topography [9]. This process is called Inkjet-enabled Adaptive Planarization (IAP). The IAP process uses an inverse optimization scheme, built around a validated fluid mechanics-based forward model [10], that takes the pre-existing substrate topography and pattern layout as inputs. It then generates an inkjet drop pattern with a material distribution that is correlated with the desired planarization film profile. This allows a contiguous film to be formed with the desired thickness variation to cater to the topography and any parasitic signatures caused by the pattern layout. This film is formed by the coercing action of a compliant superstrate, which forces the drops to spread and merge and eliminates any bubble trapping. Then, the film is cured using blanket UV exposure and the superstrate separated to reveal the desired planarized film. The use of an inverse optimization algorithm allows substrate topography to be addressed adaptively. In other words, the algorithm can generate a drop pattern that does not disturb the pre-existing substrate topography substantially, but only caters to the pattern density variation. This process has potential advantages over other planarization techniques because of its adaptive nature. Hence, the IAP process can cater to substrates of varying topographies and pattern densities by changing the inkjetted material distribution, without any changes in hardware. The IAP process can also address pre-existing substrate topography selectively by conforming to the nominal shape while planarizing over the pattern layout. A schematic of the IAP process is shown in Figure 2.

The goal of this paper is to present some preliminary results from the IAP process. A test pattern layout has been generated with the help of photolithography, and is shown in Figure 3. For the purpose of this trial, the nanoscale features have not been patterned, as it is expected that the planarization process will be blind to their presence. Thus, areas with nanoscale patterns have been patterned as a single feature of SiO2 with height equal to 100 nm. These features are adjacent to pattern-less areas, thus marking a drastic change in pattern density. As can be seen in Figure 4, the smallest length scale across which pattern density changes, is 70 microns. The goal of the IAP process is to be able to planarize this pattern with a film that conforms to pre-existing substrate topography. The targeted planarity of the film is 95% 3sigma, while the targeted film thickness at the tallest feature is less than 30 nm. In another trial, the inverse tone of the same layout will also be tested. This pattern has features of height equal to 100 nm where the previous pattern did not. The targeted metrics for the inverse layout are the same as the nominal layout.

10146-45, Session 13

Development of a robust reverse tone pattern transfer process

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High resolution imaging is typically followed by a pattern transfer process in order to define nanoscale features for both memory and logic devices. It is common for the most critical levels to apply a multilayer resist stack consisting of an imaging resist, a hardmask and an underlying organic layer.

Even with the application of a multilayer stack, critical dimension uniformity (CDU) errors can arise from a variety of sources including imperfect resist profiles, resist footing, line edge roughness and excursions in topography.

All advanced lithographic methods must control these sources of error. As an example, Jet and Flash Imprint Lithography* (J-FIL*) involves field-by-field inkjet deposition of a low viscosity resist fluid followed by imprinting with nano-scale precision overlay. A mask with a relief structure is lowered into the fluid which then quickly flows into the relief patterns in the mask by capillary action. Although the volume of resist is tailored specifically for the relief pattern on a mask, small excursions in the residual layer thickness (RLT) of a few nanometers must be controlled to prevent CDU errors that occur after the removal of the residual layer.1 Imprinting over topography can add additional variation in the RLT that can impact both CD mean and CDU.

J-FIL is also utilized for mask replication, in which an imprint resist is used to pattern a thin chromium film that then acts as a hardmask to transfer the pattern into the fused silica substrate. In this case, RLT errors can also impact CDU on the replica mask. Additionally, it is possible that the imprinted resist film may be insufficient to hold to up to the chlorine-based etched used to pattern the chromium layer.

One method for minimizing the CDU error is to apply a reverse tone process (RTP). A common process that has been developed involves the formation of a lithographic pattern on a spin-on carbon film, followed by a blanket coating of a hardmask material such as a PECVD oxide or spin on glass. The blanket oxide is then back etched to expose the imaging resist, at which point the remaining underlying organic films can be removed with a selective and anisotropic oxygen based etch.

The above approach is very effective for reversing the tone of nanoscale features where the hardmask film is able to effectively planarize the pattern. For larger features, however, in the areas where the planarization properties are poor, the hardmask is lost during pattern transfer, and the process fails.

To overcome this failure, we introduce a new RTP stack and robust transfer process that is relatively insensitive to both underlying topography and feature size. The approach is shown schematically in Figure 1. In this example, after the patterning of the resist, an ALD layer, such as silicon dioxide is applied to conformally cover all features. Next a protective resist film is placed over the ALD layer. In the example, the resist is shown to planarize both nanoscale and micron scale features (which is possible to do using an imprint tool to apply the resist), but perfect planarization is not required, as long as enough protective resist remains during the pattern transfer sequence.

The transfer is accomplished by first etching back the protective resist to expose the ALD film and then etching back the ALD to expose the top of the resist features. The printed resist can then be etched at this point, along with any underlying materials.

Examples of the RTP process used to invert of the pattern of a replica mask are shown in Figures 2, 3 and 4. Figure 2a shows the ALD conformally deposited over the resist pattern followed by a planarized resist film deposited using an imprint tool. Figure 2b is an SEM cross section of the patterned glass and Figure 2c shows a top down SEM of 19nm lines and spaces in the glass. Figure 3 shows an area with much larger features. Figure 3a depicts the original resist pattern and Figure 3b shows the pattern after tone reversal.

Details of this process will be discussed along with process limitations. The extension of the RTP to wafer processing will also be described.

1. Cynthia B. Brooks, Dwayne L. LaBrake, Niyaz Khusnatdinov, Proc. of SPIE Vol. 6921 69211K-2

*Jet and Flash Imprint Lithography and J-FIL are trademarks of Molecular Imprints Inc.

10146-46, Session 14

Pattern uniformity control in integrated structures

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Amid the ongoing miniaturization of semiconductor devices, multi-patterning techniques like litho-etch (LE) and self-aligned multi-patterning (SAMP) have been introduced to mass production. Edge placement error (EPE) control has been identified as critical for improvements in patterning precision in density scaling [1-5]. It is important to clearly distinguish single layer EPE [6] from multi-layer EPE [7]. In a previous paper, we proposed that interactive pattern fidelity error (IPFE) should be an indicator for the multi-layer EPE. IPFE is a value which combines overlay, CD average and CD variation. When IPFE becomes larger than a threshold value (half of line CD), the relationship between each pattern deviates from the allowable state, which may impact negatively the yield. To control the IPFE, all manufacturing equipment, from the lithography process to the etching process, need to be controlled carefully and CD and its variation should be strictly controlled from the wafer level to the pattern level. In this paper, we will report the IPFE simulation and real data results which shows the acceptable variations for each processes.

10146-47, Session 14

Advanced hole patterning technology using soft spacer materials

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A continuing goal in integrated circuit industry is to increase density of features within patterned masks. One pathway being used by the device manufacturers for patterning beyond the ~80nm pitch limitation of 193 immersion lithography is the self-aligned spacer double patterning (SADP). Two orthogonal line space patterns with subsequent SADP can be used for contact holes multiplication. However, a combination of two immersion exposures, two spacer deposition processes, and two etch processes to reach the desired dimensions makes this process expensive and complicated. One alternative technique for contact hole multiplication is the use of an array of pillar patterns. Pillars, imaged with 193 immersion photolithography, can be uniformly deposited with spacer materials until a hole is formed in the center of 4 pillars. Selective removal of the pillar core gives a reversal of phases, a contact hole where there was once a pillar. However, the highly conformal nature of conventional spacer materials causes a problem with this application. The new holes, formed between 4 pillars, by this method have a tendency to be imperfect and not circular. To improve the contact hole circularity, this paper presents the use of both conventional spacer material and soft spacer materials. Application of soft spacer materials can be achieved by an existing coating track without additional cost burden to the device manufacturers.

10146-48, Session 14

Line end shortening and iso-dense etch bias improvement by ALD spacer shrink process

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Driven by “Moore’s Law” the semiconductor industry has adopted more aggressive node scaling, hitting the CD limitation of conventional photolithography. Multiple patterning employing etch shrink extends the scaling of hardmask open CD (HCD) to sub-50nm regime. The etch shrink has offered a substantial CD reduction from post-litho to post-etch, allowing the sub-20nm half-pitch patterning by interleaving multiple conventionally printed patterns. A plasma-assisted shrink process has been being primarily used in the back-end-of-line (BEOL), it forms a polymer film on all exposed surfaces during post-litho etch to eventually achieve a shrunk hardmask open CD for contacts and trenches [1]. A downside of this shrink is the line end shortening (LES) and significant iso-dense bias (IDB) on one- and two-dimensional (1D & 2D) structures post etch which we believe to be caused by the pattern density loading during reactive ion etching (RIE). The LES, also known as line end pullback, can cause problems including via opens if under corrected or metal shorts if overcorrected. And the IDB erodes space margin and leads to short defects. Therefore an optimized shrink process is highly desired.

In this presentation, we demonstrate improvement on LES and IDB by applying a novel atomic layer deposition (ALD) spacer shrink process [2], which replaced the plasma-assisted shrink step during etch. This process employs ALD to form spacers on sidewalls of PR post BARC etch to effectively “fatten” the PR, therefore shrinking the size of pattern to be transferred to underneath layer through etch. We investigated the IDB of 1D (isolated & dense trenches) and LES of 2D (tip-to-tip, tip-to-side) structures at M1 interconnect layer with sub-20nm minimum half-pitch. We will prove the patterning performance improvement by comparing data that were collected from one baseline wafer and the other wafer with ALD spacer. On each wafer we measure five dice and over 200 targets (post-litho and post-etch). Based on the experiment, we observed an overall LES through pitch improvement and up to 8nm LES reduction for the smallest pitch by using ALD spacer process. We also identified a 5nm IDB reduction through pitch post etch. In addition to that the spacer process offers capability of stronger CD shrinking therefore enhances the photolithography process marginality, the common process window (PW) extended by over 10nm by increasing post-litho CD target while keeping post-etch CD unchanged. In contrast to these improvements, we will also discuss potential drawbacks including line width roughness (LWR) degrading and defectivity induced by ALD spacer. In summary the ALD shrink process is proved capable of offering low LES and IDB for hardmask opening, which is one of the key to precise CD control in multiple patterning process.

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10146-49, Session 14

Improvement of patterning performance in complex layout mask

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These days, Spacer Patterning Technology (SPT) and Double Patterning Technology (DPT) are widely used to reduce chip size in semiconductor device. In our study, we use Double Patterning Tech. (DPT), our masks have repeated horizontal line and space patterns and no directional ramdom-

shaped patterns simultaneously. Both X, Y directions of the patterns are critical, only limited illumination optics can be used, and have problems need to be improved : the shortage of EL margin, DOF margin, and LWR.

In this paper, we have approached for the imporvement of there problems by controlling any of the experiment parameters, such as Cr pattern size in reticle, layout, and photoresist, and also investigated the correlation of these parameters with patterning performance.

10146-50, Session 14

Nanofabrication of flexible MoS2 biosensor to detect lower-concentrated area of biological molecules

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Two dimensional layered transition metal dichalcogenides (TMDC) materials have the growing potential to upstage graphene in the next generation of biosensors in detecting lower-concentrated areas of biomolecules. The current gold-standard detection method is the enzyme-linked immunosorbent assay (ELISA), an immunological assay technique that makes use of an enzyme bonded to a particular antibody or antigen. However, this technique is not only bulky, labor-intensive, and time extensive, but more importantly, the ELISA has relatively low detection limits of only 600 femtomolar (fM). In this work, for the first time, we present a novel flexible, sensitive MoS2 (molybdenum disulfide) biosensor, as shown in Figure 1, composed of few-layer of MoS2 as the channel material, and flexible polyimide as the substrate. In order to nano-fabricate this flexible biosensor, we mechanically transferred a few layers of MoS2 onto the flexible substrate polyimide and photolithography to create a patterning on the surface, and as a result, we were able to create a transistor that used MoS2 as its conductance channel. We successfully fabricated this MoS2 biosensor onto a flexible polyimide substrate. Furthermore, the fabricated flexible MoS2 biosensor can be utilized for quantifying the time-dependent reaction kinetics of streptavidin-biotin binding. Figure 2 shows the transfer characteristics of flexible MoS2 biosensors measured under different concentrations of streptavidin. The flexible MoS2 biosensor could illustrate a faster detection time in matters of minutes, and higher sensitivity with detection limits as low as 10 fM. Time versus equilibrium constants will be presented in details.

10147-1, Session 1

Technology Development: the "In Between" *(Keynote Presentation)*

David M. Fried, Coventor, Inc. (United States)

Semiconductor research continues to uncover fascinating innovations, and semiconductor manufacturing continues to outlive the predictions. However, technology development, the "in between" timeframe, is changing drastically right now due to process complexity, physical and financial constraints, and a general lack of options for the future. Transiting through this part of the technology lifetime quickly and efficiently is essential to success in an increasingly competitive electronics industry.

Technology development is challenged to take device technology from singular demonstrations to integrated multi-billion transistor products. Rarely is one research concept enough to drive an entire new product, so several aspects of advanced research must be combined into development projects. The resulting technology also has to satisfy cost and market pressures rarely examined in research. This presentation will focus on a few novel technology development capabilities and methodologies that can enable rapid acceleration of semiconductor concepts to manufacturable products.

10147-2, Session 1

Optical 3D nano-fabrication: top-down and bottom-up approaches *(Keynote Presentation)*

Satoshi Kawata, Osaka Univ (Japan)

While nanotechnology has a great potential for fabricating advanced nano-devices and materials that found the applications in sciences, industries, and medicine, it is limited to the surface modification technology. E-beam, ion-beam, light-beam lithography and scanning probe microscopes modify the surface of substrate or film by deposition, etching, oxidization, or modification. Nanotech devices now available are all basically in two dimensions, such as nano-electronic circuits, high-density data-storage, liquid-crystal displays, and MEMS/ NEMS. Here, I discuss the methods of 3D fabrication in nano-scale. Two-photon process has been successfully combined with photo-polymerization for drawing micro- and nano-machines in 3D with a tightly focused laser beam [1]. It has been applied to photo-isomerization for multi-layer rewritable optical data-storage [2]. Metallic metamaterials have been drawn with two-photon photo-reduction [3]. However, direct leaser-beam drawing consumes time for fabrication a large-scale 3D complex structures. We have developed a completely different method of 3D fabrication, that is the use of evolutional fabrication of the structures or self-growing method. Fiber structures have been self-grown in polymerizable resin [4]. Coupling and branching of waveguides between many fibers and a single fiber were fabricated, based on the nonlinear Schrödinger equations. A recent work on the self-growth of metallic metamaterials will be also shown [5]. Fractal 3D nano-structures of silver with self-similarity have been grown in silver-ion solution with plasmonic heating of metallic nano-seeds [5].

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10147-3, Session 2

EPE improvement thru self-alignment VIA multi-color material integration *(Invited Paper)*

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As the industry marches on onto the 5nm node and beyond, scaling has slowed down, with all major IDMs & foundries predicting a 3-4 year cadence for scaling. A major reason for this slowdown is not the technical challenge of making features smaller, but effective control of variation that creeps in to the fabrication process. That variability manifests itself as edge placement error (EPE), which has a direct impact on wafer yield. Simply defined as the variance between design intent vs. actual on-wafer results, EPE is one of the foremost challenges being faced by the industry at the advanced node for both logic and memory. This is especially critical at three stages: the front end of line (FEOL) STI patterning; middle of line (MOL) contact patterning; and back end of line (BEOL) trench patterning where the desired tight pitch demands EPE control beyond the capability of 193i multi-patterning or even EUV single pattern. In order to mitigate this EPE challenge, we are proposing self-alignment of blocks & cuts thru a multi-color materials integration concept. This approach, termed as "Self-aligned block or Cut (SAB or SACut)", simply trades off the un-manageable overlay requirement into a more manageable etch selectivity challenge, by having multiple materials filled in every other trench or line.

In this paper we will introduce self-alignment based block and cut strategies using multi-color materials integration and show implementation for FEOL STI cut, MOL gate contact patterning and BEOL trench block patterning. We will present a breakdown of the key unit process challenges that needed to be resolved for enabling the self-alignment such as: (a) material selection of multi-color approach; (b) planarization of spin on materials; (c) void-free gap fill for high aspect ratio features; and last but not the least, (c) etch selectivity of etching one material with respect to all other materials exposed. Further, we will present a comparison of our new self-alignment approach with standard approaches where we will articulate the advantages in terms of EPE relaxation and mask number reduction, thru process and TCAD simulation and validation on silicon on a N7 vehicle. We will conclude our talk with a brief snapshot of the future direction of our EPE improvement strategies and our view on the future of patterning beyond 5nm node for the industry.

10147-4, Session 2

In-design and signoff lithography physical analysis for 7/5nm

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At advanced nodes, definition of design rules and process options must be tightly optimized to deliver the best tradeoff performance, power, area and manufacturability. However, design implementation platforms don't typically have access to process information and process teams don't have design knowledge. This challenge in particularly strong for fabless design houses that need to work with their foundry partners on Design-Technology-Co-Optimization (DTCO).

Joining forces, ASML, IMEC and Cadence Design Systems developed an In-design and signoff lithography physical analysis well suited for 7/5nm and below. As a demonstrator of this capability, we have integrated the Tachyon OPC engine used by IMEC 7/5nm process into Cadence's Litho Physical Analyzer (LPA) to perform lithography checks and to leverage LPA integration in both custom and digital design platform, as well as standalone signoff.

Depending upon the end application, LPA can be launched either from place & route or custom layout or standalone. LPA processes first the design database to identify hierarchy, decompose the layout for coloring and apply pattern matching to identify location requiring simulation. The layout is then passed to the Tachyon OPC tool to perform optical process correction and model-based litho verification that is validated on Silicon. The hotspots and contours are processed by LPA for generation of hotspot markers, for fixing guidelines, and for providing all this information to the design environment. Fixes can be in the design, in the coloring, in the OPC, or ultimately in the process technology.

The flow has been developed and demonstrated to work on IMEC 7nm, and can be ported to smaller or larger technologies. The paper will present the result of this In-design and signoff lithography physical analysis flow, how DTCO and design teams can add manufacturability to Power Performance and Area (PPA).

10147-5, Session 2

Using heuristic optimization setting SRAF rules

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Sub-resolution assisted features (SRAF) have been widely used to improve the printing margin for isolated and semi-isolated designs in the advanced semiconductor technology nodes. Rule based SRAF (RBSRAF) and model based SRAF (MBSRAF) are two common methods to generate SRAF in the optical correction process. As for RBSRAF, an empirical method is used to extract SRAF placement rules for a group of designs from either the silicon wafer data or lithography simulation data. It is challenging for this empirical method to generate complete and optimized SRAF rules due to the lack of interactive cycles of optimization, incomplete parameter space coverage, long cycle time and high cost. In MBSRAF, the pixel based inverse lithographic simulation contour (gradient map) is used as a guide for SRAF insertion. Theoretically, MBSRAF should be an ideal way to set proper SRAFs for a full chip design. However, there are two fundamental issues preventing us from obtaining the maximum SRAF benefit. The exact contour-like MBSRAF solution is too complicated for mask manufacturing. Some kind of simplification has to be used to make it more manufacturable. During this simplification process, some important information may get lost. More importantly, MBSRAF is blind to SRAF printing possibility because SRAF printing information is difficult to be included in the mathematically inverse calculation. Very often, either excessive or insufficient SRAFs are generated initially. Then some of them may be reduced or removed during subsequent clean-up process (SRAF printing avoidance check, i.e. SPA). The worst scenario is to remove the critical first SRAF. This leads to poor printing margin for some key designs. Moreover, MBSRAF solution is strongly dependent on the matrices used in the gradient map generation. When the matrices are not directly related to the printing performance on silicon wafers, the SRAF solution is not always optimized for real world performance. As for MBSRAF, the worst could happen as SRAFs are generated where they are not required while SRAFs are not generated or removed where they are desperately needed.

In this paper, a heuristic optimization approach has been developed to optimize SRAF placement rules for advanced technology nodes. In this optimization process, an intelligent cost-function is constructed with matrices which are directly related to wafer imaging process margin and SRAF printing performance. Through multiple cycles of mathematical optimization, several SRAF placement parameters such as SRAF width, length, location and so on are optimized to derive a set of SRAF placement rules which produce a superior imaging process margin and avoid SRAF printing. Then, the optimized SRAF rules can be implemented in the RBSRAF manner instead of MBSRAF to give engineers better control. RBSRAF can be tailored for a specific design and also can be used in hybrid mode with MBSRAF. The optimized RBSRAF has demonstrated more than 30% DOF improvement, superior SRAF printing avoidance, and significant run-time reduction.

10147-6, Session 2

The impact of lower light source bandwidth on sub-10nm process node features

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Over the years, Lithography Engineers continue to focus on CD control, overlay and process capability to meet current node requirements for yield and device performance. Use of ArFi lithography for advanced process nodes demands challenging patterning budget improvements in the range of 1/10 nm especially for interconnect layers.(1) Previous experimental and simulation based investigations into the effects of light source bandwidth on imaging performance have provided the foundation for this work.(2-6) The goal from the light source manufacturer is to further enable capability and reduce variation through a number of parameters.(7-10)

In this study, the Authors focus on the increase in image contrast that Source Mask Optimization (SMO) and OPC models deliver when using 200 fm light source E95 bandwidth. Using test constructs that follow current N7 / N5 ground rules and multiple pattern deconstruction rules, improvements in Exposure Latitude (EL), Critical Dimension (CD) and Mask Error Enhancement Factor (MEEF) performance are observed when SMO and OPC are optimized for 200 fm light source bandwidth when compared with the standard 300 fm bandwidth. New SMO-OPC flows will be proposed that users can follow to maximize process benefit. The predicted responses will be compared with the experimental on wafer responses of 7 nm features to lower light source bandwidth.

10147-7, Session 3

Computational phase microscopy for mask metrology *(Invited Paper)*

Laura Waller, Univ. of California, Berkeley (United States)

This talk will describe computational imaging methods for phase retrieval of mask effects, such as electromagnetic edge effects. Our experimental setups employ illumination-side or detection-side coding of angle (Fourier) space with simple hardware. The result is high-resolution intensity and phase images for quantifying mask edge effects. We describe methods for illumination coding Gigapixel microscopy in commercial microscopes and extend our methods to 3D imaging and algorithmic self-calibration. Through an end-to-end design of both the optical system and the computational algorithms, we achieve metrology modalities that are accurate, simple and flexible.

10147-8, Session 3

Process margin improvement through finger-print removal based on scanner leveling data

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The next generation technology and emerging memory devices require gradually tighter lithographic focus control on imaging critical layers. Especially in case of BEOL process, big PDO (Process Dependent Offset) from large intra-field topography steps affects the process margin directly. There are couple of scanner options to reduce PDO, such as AGILE which provides several benefits. However, for certain use cases the AGILE sensor may not be the optimal solution.

In this paper, we introduce the concept and development background of iFPC (intra-field Finger Print Correction). iFPC is a scanner option that removes the generic 3D fingerprint seen in the leveling data so that both process dependency and actual wafer topography are not followed during wafer exposure.

In addition, we compare the degree of process margin improvement when applying iFPC compared to that of AGILE on a critical layer. The achieved results demonstrate that by applying iFPC it is possible to gain an additional 10% DoF. In other words, on this use case our feasibility suggests that by removing the generic 3D fingerprint seen in the leveling data, it is possible to achieve a better focus performance than when trying to follow the topography during scanning.

In conclusion, we found another good way to improve the process margin through this comparative experiment. Therefore, our next step will be to setup the methodology to select the use cases where iFPC is the optimal solution.

10147-9, Session 3

Scanner-to-scanner CD analysis and control in an HVM environment

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As the pattern sizes shrink, scanner-to-scanner CD variations are increasingly becoming a critical issue for HVM products.

This paper shows that scanner-tuning can allow for a tight control of critical feature dimensions between scanners when an accurate root cause analysis is carried out as input for the ?CD matching per feature and per source of the issue.

At Samsung HVM fab, the root causes of CD mismatch between multiple ArFi scanners (XT4 1950Hi, NXT 1960Bi, NXT 1950i) were successfully identified and ranked with the help of a methodology (Proximity Matching Budget Breakdown or ProMA BB) developed by ASML, which allows identifying the key contributors to scanner-to-scanner CD variation of selected critical features.

ProMa BB results help to identify what combination of scanner control parameters should be optimized to compensate CD of critical patterns while helping to avoid undesirable cross-compensation (e.g., tuning the source pupil to correct for aberrations-driven DCD).

The paper will show accuracy between predicted and measured CD mismatch of better than 0.2nm per feature for the reviewed cases.

The critical out-of-spec feature CD variations were tuned within specifications by adjusting scanner parameters (pupil illumination, focus, lens aberration).

This budget breakdown method was proposed for HVM implementation at Samsung in combination with other ASML fab applications: Patter Matcher Full Chip (PMFC), Image Tuner and FlexWave.

10147-10, Session 3

Reduction and control of intrafield focus variation on 7nm technology

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With each technology node, overall focus budgets have become increasingly tighter in order to meet the necessary product requirements. Wafer topography, scanner leveling and dynamics are just a few of the contributors to the overall focus budget . In this paper we demonstrate multiple solutions for intrafield focus variation improvement through calibration reticle to production reticle curvature matching. Additionally we will demonstrate intrafield focus uniformity improvement results obtained from newly developed scanner software functionality allowing to match scanner intrafield focus set-up to be tailored towards actual product-reticle-population intrafield characteristics.

Tool focus calibrations and setups are required periodically to maintain optimal performance. Any variation in this setup from the optimal state of production can impact the calibration model. Here, we quantify the impact of the calibration reticle's X curvature on baseliner. Through this we note a 63.3% improvement in intrafield focus range when matching X curvature to production reticle shape. Impact on lens aberrations are also analyzed and minimal astigmatism impact is observed. The intrafield focus uniformity solutions proposed in this study provide a methodology to further reduce process variation on current and future technology nodes.

10147-11, Session 3

450mm status for high-volume manufacturing

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The Global 450mm Consortium (G450C), which is located at the SUNY Poly campus in Albany, NY was created to develop and evaluate a manufacturing tool set for 450mm wafers. The Lithography cell at G450C consists of a Nikon NSR-S650D 193nm immersion scanner and a SCREEN DT-4000 Sokudo DUO track. The Lithography cell was installed and qualified in 2015, and with over a year of tool availability we have been able to perform extensive testing on the system to determine the equipment readiness for volume manufacturing.

For the purposes of this paper we are focusing on the Edge Placement Error

(EPE) contributors of Critical Dimension Uniformity (CDU) and Overlay. We will show the initial results as well as the improvements that have been made since tool acceptance. The 450mm results will be compared to 300mm tools in production today, as well as against the seven nanometer node (N7) expected requirements. Lastly, we plan to demonstrate the Nikon scanner's ability for focus control on stressed or bowed wafers, which are characteristic of large silicon substrates.

This paper will showcase the current 450mm lithography performance for CDU on both line/space and contact hole patterns. We will demonstrate the process window for line/space and contact hole features on multiple resists specially formulated for 450mm. We will also show data from both Opaque MolySi On Glass (OMOG) vs. Alternating Phase Shifting Mask (APSM). Both Post Exposure Bake (PEB) tuning on the SCREEN track as well as CDU Master Corrections from the Nikon Litho Turnkey Solution software suite will be utilized for performance improvements on 450mm wafers. The G450C goal is to drive across wafer CDU results to less than 1nm 3 using a 1.5mm edge exclusion. In addition to our test masks, G450C is currently designing a three layer mask set and with the availability of this mask we plan to gather "on product" CDU performance on a Back End Of Line (BEOL) metal stack.

In the current reality of high volume manufacturing, multi-patterning is used to achieve the required Critical Dimension (CD) and pitch combination. The largest contributor to EPE is scanner overlay performance. We will demonstrate the Single Machine Overlay (SMO) performance as well as some Mix and Match Overlay (MMO) results. The lithography cell at G450C is the only 450mm linked lithography cell in the world. In order to create MMO wafers we were required to expose the first print at the Nikon factory in Japan and etch them at G450C to generate an align-to layer. G450C is currently designing a three layer mask set, and with the availability of this mask we plan to gather On Product Overlay (OPO) performance on a BEOL metal stack.

As the wafers' size scales, so do some of the process effects including film stress and wafer bow. The current G450C BEOL integrated process has measured wafer bow of up to 400um. We will demonstrate how the S650D measures the wafer topography and adjusts the exposure to compensate for wafer bow.

10147-12, Session 3

Will conventional E95% spectral indicator last long forever?

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Fifteen years has passed since ArF lithography technology transitioned to mass production. At first the node size was 130nm, however, now we are discussing one-digit nm node. This node size is one-fifteenth compared to that in the initial generation. It is obvious that generations have steadily changed.

Meanwhile, ArF projection optics has been designed with higher NA. Moreover, much higher NA or effectively short wavelength have been achieved by introducing the immersion lithography technology which injects immersion media between the light emission side of optics and the wafer surface.

Now that ten years has passed since the immersion lithography technology transitioned to mass production, the requirements for the light source have become much more demanding. This is because E95%, a typical parameter for the light source, which reduces the CD variation and influences the optical characteristics, has been required to be much shorter along with advanced node.

The spectrum characteristics of the conventional KrF 248nm-light source were defined with full-width at half maximum (FWHM). After entering ArF era, E95% was defined as more stringent parameter. This new parameter is closely linked to line narrowing and node transition. This E95% is a parameter to define optics monochromaticity and recognized as equivalent to quantified chromatic aberration.

More specifically, it is desired to reduce the chromatic aberration ideally down to zero to maximize the contrast by suppressing blur images. Provided that the blur images are caused by not only chromatic aberration but also the convoluted effect of spherical aberration, residual errors of lithography optics system and other defocus elements. In line with this we should take persistent challenges to reduce errors in designing and manufacturing lithography optics systems and drive the chromatic aberration closer to zero.

The contrast we discuss in the lithography optics systems strongly correlate to resolution, and thus it is well known that OPC bias is linear with respect to E95% when the resolution is fixed. Although this OPC bias and E95% have been firmly linear with each other, it has also been revealed that the trend of the linearity with much shorter E95% deviates from the conventional trend and shows an inflection point in the near future.

We systematically analyze the trend that linearity error tends to be greater than the conventional distribution and suggest solutions to the issue.

This systematic analysis includes:

1. Measurement errors and distribution in measuring E95% as the spectrum width

2. Correlation between raw measured spectrum intensity data and E95%

3. Linearity comparison in behaviors between when E95% is approximated by i) +/-2 sigma of, ii)+/-3 sigma of normal spectrum distribution, and iii) by another approximation.

Based on these studies, we identify the roles of the light source to contribute to 7nm-node mass production by defining the spectrum and its requirements for lithography performance.

10147-13, Session 4

Molecular force modeling of lithography *(Invited Paper)*

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Figure 1 shows that the most important factor in lithography is foot contrast. Low contrast leaves a large region (CAT) where resist solubility is uncertain (chaotic area), which causes unresolvable patterns, LER/LWR issues, and pattern collapse (collapse may be due to affinity imbalance).

Figure 2 shows examples of a CAT plot for two stacks of low optical reflectivity and high optical foot contrast. Low reflectivity gives higher CAT, and is further deteriorated as the image approaches the forbidden pitch, while a high foot contrast stack keeps good CAT value across all pitches. Experimental results agree well with the calculations, which will be included in the full paper.

Figure 3 is a CAT contour map versus resist and Si-HM thickness for a L/P=40/100 nm pattern. Additional CAT plots will be included in the full paper.

10147-14, Session 4

Experimental characterization of NTD resist shrinkage

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Simulation of NTD resist has become a challenge for physical resist modeling. Traditionally, resist modeling was mainly restricted to reaction-diffusion models for PEB and standard development rate models for simulating the pattern formation during the final development step. With some minor extensions this simulation approach sufficed to predict resist CDs and resist profile shapes that were in very good agreement with experimental data. For the latest NTD resists this situation has changed.

One major experimental observation is that, in contrast to PTD resists, resist shrinkage is strongly impacting the CDs and resist profile shapes. Therefore, the shrinkage process has to be accounted for in a physical resist model. Our modeling assumption is: The resist shrinkage during PEB is caused by the collapse of free volume left behind the evaporating byproduct of the acid-catalyzed deprotection reaction during PEB. This will not only cause a vertical resist height loss in the exposed regions but also a lateral deformation in the resist material. We further assume that the shrinkage happens already during the PEB and that any further mechanical deformation processes that will possibly happen afterwards can be neglected.

In order to validate our model assumptions, we performed and analyzed 4 experiments. The first experiment is aimed at characterizing the tensile stress in resist after PEB which would be the driving force for any mechanical post PEB deformation. We measured the bow of a resist-coated and flood-exposed wafer before and after PEB. Since the change of wafer bow can be related to the remaining tensile stress after PEB, and since we see that there is no significant change in wafer bow we confirm the model assumption to exclude stress induced mechanical deformations after PEB. In a second experiment we aim to validate the existence of lateral mechanical deformation and quantify the upper limit of volumetric shrinkage. To make the lateral shrinkage visible we pattern a wafer with NTD resist using a PTD developer so that unexposed resist remains on wafer. Then we flood expose the wafer and perform an additional PEB to cause maximum deprotection of the remaining patterns. Resist profiles before and after the second PEB are compared to quantify the resulting volumetric shrinkage. A third experiment delivered development rate monitor data. These data show the apparent development rate to be systematically z-dependent: The development rate is higher at the top of the resist than at the bottom. We discuss how this effect can be interpreted to be a consequence of both the shrinkage during PEB and caused by thin film effects. The fourth experiment aims to quantitatively validate the recently implemented shrinkage model by characterizing the pattern dependent shrinkage directly after PEB. The deformation caused resist surface modulation is measured with an AFM and compared to post PEB simulation results.

10147-15, Session 4

Investigation of 3D photoresist profile effect in self-aligned patterning through virtual fabrication

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In modern integrated circuits, self-aligned double patterning (SADP) and self-aligned quadruple patterning (SAQP) techniques are used in various critical points of processing. Due to various deposition and etch steps that are involved in these, understanding the effects of photoresist profile on the final structure requires modeling of the lithography as well as entire downstream process integration schemes. Line edge roughness (LER) and photoresist's sidewall profile are two of these effects. As device feature sizes continue to decrease, both gain increasing importance to ensure tight process control of critical dimensions (CD). Previous studies of the impact of resist profile on CD control rely on the traditional build-and-test approach, where cross-sectional SEM imaging of the resist profile and CD metrology data are collected on processed test wafers. This is not only costly but also time-consuming.

In this study, the effects of photoresist sidewall profile and LER on two representative integration schemes were studied through 3D virtual fabrication: Front-End of Line (FEOL) Fin formation and Back-End of Line (BEOL) Metal line definition. Both of these processes use self-aligned double patterning (SADP) in pattern definition and affect the circuit performance through MOSFET channel shape and parasitic capacitance respectively. In both cases, we imposed LER and sidewall roughness on the photoresist that defines the mandrel at the initial step of the SADP flow using SEMulator3D. The LER followed a Gaussian correlation function for a number of amplitude and correlation length values. The sidewall profile emulated the bulb-shaped pattern that is reported in experimental works. The taper angle and roughness amplitude of this shape were varied to isolate its components.

In the case of silicon fin formation, it was observed that sidewall roughness leads to increased tapering of the mandrel, which in turn results in thinner spacer width. Since spacer thickness is the main modulator for fin width CD, resist sidewall profile is shown to have a strong impact on the final fin profile. Furthermore, a systematic study of taper and roughness components of the photoresist sidewall profile revealed that both components have a significant effect on the mandrel tapering independently. The tapering is at its highest, however, when the two components are both present. Consequently, fin width shows a strong dependence on these two components of photoresist sidewall profile. Our study showed that in order to control fin shape and CD variation, utmost attention should be placed on not only LER but also resist sidewall profile, requiring tighter exposure/development controls.

In the case of metal line definition, the photoresist on the second copper interconnect level (M2) was imposed with LER and a sidewall profile. The intricate damascene process with subsequent etch-block level and vias with litho-etch litho-etch (LELE) scheme revealed implications on interconnect reliability through capacitance extraction of the final structure. Random variation effects on metal lines are found to cause strong variation in parasitic capacitance values, as well as shorts and opens that jeopardize the yield.

In conclusion, the effect of resist sidewall profile on SADP process has been systematically studied in two integration schemes through 3D virtual fabrication: FEOL fin formation and BEOL metal line definition. In each of these cases, we have found direct evidence of resist sidewall profile impact on variability degradation in CD and electrical performance. Special care should be placed on controlling resist profile through optimization of exposure and development schemes.

10147-16, Session 5

Reducing the impact of etch-induced pattern asymmetry on overlay by using combined lithography and etch tool corrections

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With shrinking design rules, the overall patterning requirements are getting aggressively tighter and tighter. For the 5-nm node and beyond, on-product overlay below 2.5nm is required. Achieving such performance levels will not only need optimization of scanner performance but a holistic tuning of all process steps.

In previous work, it has been shown that process-induced pattern asymmetry has significant impact on overlay performance and can be partially compensated by applying high-order scanner corrections or optimizing metrology targets. Today, we present the reduction of process asymmetry in a tunable etch system and demonstrate the related on-product overlay improvement combined with scanner corrections.

In our work we utilize etch tools (Lam Kiyo® conductor etch systems) with proprietary edge tuning technology that can be used to reduce the etch-related asymmetry at the wafer edge. In combination to this unique method, we evaluate the impact of high order corrections per exposure field to compensate for process asymmetry at the wafer edge with a state-of-the-art 1.35 NA immersion scanner (NXT:1970Ci).

The study is done on dedicated test wafers with 10-nm logic node design. We use angle-resolved scatterometry (YieldStar® S-250), atomic force microscopy, and SEM cross-sections to characterize process asymmetry. We present experimental investigation of the effect of etch tuning and scanner corrections on the process asymmetry and the resulting overlay. In particular, we present results showing a reduction of side-wall angle

asymmetry by 4 degrees at wafer radius 146mm which is equal to a reduction of pattern shift of 1.5nm for a hard mask thickness of 40nm.

Results show that asymmetry can be addressed by both, litho compensation and etch tuning, and bring on-product overlay down to the required level. We discuss the benefit of the correction techniques especially for thick hard mask layers (the pattern shift scales linear with hard mask thickness) and evaluate a combined correction scenario, where preventive etch tuning and feed-back based scanner corrections are used. We conclude that a holistic tuning of all process steps will be required to fulfill overlay requirements of future nodes.

10147-17, Session 5

Optimal structure sampling for etch model calibration

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Optical Proximity Correction is widely used in the industry to enable a robust lithographic process. With the help of very accurate optical and resist models, the profiles printed in the photoresist can be finely predicted. However for a successful patterning it is also necessary to be able to simulate precisely the contours transferred in the substrate after etching of the photoresist. An etch model usually starts from a litho contour to compute at each point the litho-etch bias that is strongly dependent of the structure geometry and its environment.

Available OPC Lithographic models are mainly based on rigorous physics (at least for the optical part) whereas current available OPC etch models[1,2] are fully empirical. Indeed the etch physic is very complex and typical etch processes include many steps. Furthermore OPC models need to be fast to run on full chip. Thus etch models are typically made of a set of arbitrary basis functions or kernels adjusted to fit at best experimental data. As a consequence etch models can be very unstable (risk of overfitting the data) because often blindly relying on the judicious choice of the experimental data (sampling plan) and the kernels (model form) ruling the model calibration.

This work proposes a flow to select objectively optimal and minimal number of structures to serve for any etch model calibration. The objective is to use all the information available within a structure assuming a calibration with SEM contours. In addition the goal is to improve the stability of etch models by defining new efficient kernels adapted to the geometries sensitive to the etch effects.

The approach consists in starting from a huge layout containing many design configurations –typically a test chip or a set of exhaustive test patterns- and applying two sequential rounds of pattern selection (see Fig 1.). The first step is a quick pre-selection of patterns based on design topology and deal with the design space. The second step is a fine selection of the patterns based on etch relevant parameters (etch space).

The etch parameters are derived at any point along the lithographic simulated contour of a given structures by evaluating a set of specific kernels described in Fig.2. Then the etch signature of any structure is mapped in the kernel parameter space (etch space) as illustrated in Fig.3. Finally a specific clustering method provides an automated way to select the best structures in the etch space avoiding redundancy and maximizing the coverage.

The methods was specifically applied to a contact layer containing many different geometries and helped to improve the etch model stability by selecting the appropriate calibration structures and using SEM contour as input for the experimental data

10147-18, Session 5

Interlayer verification methodology for multi-patterning processes

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Various multi-patterning processes with accompanying design methodologies have been deployed to address patterning challenges associated with ArFi or/and alternate solutions such as EUV, DSA, Nanoimprint and so on. From our recent experience, process variability prediction through compact models is sometimes limited to those multi-patterning processes used to compose single final target. We may call those sequential processes as representative module for design target layer which is not clearly derived from single litho-etch process but derived from the interaction between various layers. Key challenges for extend multiple pattering are managing design and tolerance variation in multiple pattering steps with proper restrictions, and visualizing interlayer errors (w/ bridge & pinch and overlap) with final target layer against alternate layer is important for process/design engineers with preserving accuracy.

We will demonstrate verification flows for different process modules to verify the failure mechanisms and to aid in visualization then judge the area for improvement with existing model based solution. Then we will also try to investigate possible area for development upon prediction residual to handle from compact model (VEB) as those errors are accumulated from multiple process effects into final CD measurement from design target layers. This may lead to new dimension of modeling solution upon quantified process effects we've never considered because those signatures were lumped between processes to processes.

10147-19, Session 6

Accurate lithography simulation model based on convolutional neural networks

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Lithography simulation is widely used in DFM application such as model based OPC and hotspot detection. It requires simulation accuracy which is measured by the difference between measured wafer CD and simulated CD. Resist model is one of key factors to decide simulation accuracy and several methods have been proposed. Variable threshold model (VTM) is a resist model used in OPC [1]. VTM uses different threshold to calculate simulated CD for different patterns. The threshold is calculated from values of aerial image features such as slope and intensity of the respective aerial image. Form of the features and coefficients of the VTM are optimized using training data which is a set of aerial image of mask patterns and their ideal threshold determined empirically. However, it is difficult to determine appropriate features and the simulation accuracy has an issue for extrapolation, which means insufficient accuracy for unknown patterns which are not included in the training data [2]. This paper proposes a new method of VTM to determine appropriate aerial image features automatically and improve simulation accuracy for training data and non-training data using Convolutional Neural Networks (CNN) architecture. CNN architecture consists of two layers, feature extraction layer and fully-connected layer. In the feature extraction layer, convolution and max pooling are used alternately to extract proper aerial image features. In the fully-connected layer, a threshold value is calculated from the extracted features using neural networks. The convolution kernels and parameters of neural networks are optimized on training data, which consists of aerial images and their ideal thresholds determined empirically as same as conventional VTM. We conducted experiments on contact hole patterns and the results show CNN model can achieve much better performance to calculate CD of the patterns including extrapolation than conventional method.

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10147-20, Session 6

Full chip hierarchical inverse lithography: A solution with perfect symmetry

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Inverse lithography technology (ILT) is among the most studied areas in computational lithography. Several methods like level sets, total variation, and pixelated masks have been proven to produce effective results. However, these methods have not gained traction in manufacturing flows due to two major problems. First, the complexity of the masks creates challenges in manufacturing and inspection. Second, the lack of symmetry in the solution breaks the hierarchy of the designs and forces users to flatten their designs. Flattening the designs increases computation time which makes it impossible to run already slow ILT solutions on a full chip scale. Mask complexity problem has been addressed by introducing mask constraints into the solutions, however the lack of symmetry issue has not been addressed in any of the solutions that we know of.

In this paper we introduce an ILT solution that maintains perfect symmetry with manageable mask complexity. The solution is applicable to full chip hierarchical designs with reasonable turnaround times. In this solution we divide the ILT problem into three steps and strictly maintain symmetry in each of these steps.

a. Optimize an ideal gray scale mask that provides the largest process window.

b. Seed the ideal mask with polygons that match the gray scale mask as much as possible.

c. Grow these seeds in a separate optimization flow to find the best polygonized mask.

At the end of the optimization we generate a mask that perfectly maintains the symmetry properties of the illumination. To our best knowledge this is the first ILT solution that can be used hierarchically on a full chip scale. A sample result is shown in Figure 1.

10147-21, Session 6

Source defect impact on pattern shift

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Most pattern shift analysis discussions focus on the OPC model and model components that form the pattern contours, but the source itself is considered as a constant input. In reality, the source may have defects and/or contaminations that may impact the image formation and possibly introduce asymmetrical pattern formation behavior. Initial studies have quantified the impact of source defects on wafer CDs in the presence of OPC. The studies have found that when source defects are present in the OPC model CD variation, NILS impact, MEEF impact, and patter shifts may occur. Empirical studies and data have shown that the severity of defects are proportional to the impact on final pattern formation. However, it should also be noted that Proximity correction schemes have been found to be a robust ally in countering the aforementioned defects in imaging.

This study will continue to evolve to better understand the interaction between source defects and pattern shift during mask synthesis by focusing on following two defect schemes and quantifying their effects on pattern shift. First, this study will focus primarily on introducing defects on all source pixels at a rate of +/- 6%, this test aims to quantify the effects on pattern uniformity while assuming defects in source manufacturing. Second, followed by introduction of catastrophic pixel failure for pixels that are below a given intensity. This will help to better understand the limitation of scanner systems that may not be able to 100% represent the source pixels that been created during an aggressive SMO session. Detailed analysis and studies will be conducted to quantify the source defects impact on pattern formation.

The software methodology used to execute these studies will also be presented in detail. The tools and software used along with any underlying assumptions will be clearly presented to maximize learning that can be beneficial to end users.

10147-23, Session 6

Automated detection and classification of printing SRAFs using machine learning algorithms

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SRAF printing is a critical yield detractor and known issue in OPC technology. SRAF print avoidance models are used to determine where undesirable printing occurs but lack robustness and are unreliable for detection of all cases. Classification of printing SRAFs is a subjective and manual task where many engineering hours are lost in manually classifying images. In this work we demonstrate a reliable way to accurately classify risk of SRAF printing. We show prediction success rate of over 99.98% where only one image under-predicted (we define under-prediction as the case where our classifier predicts there is no printing SRAF but the SEM image shows printing SRAF). Under-prediction in a model is a key defect generator as it means the model is unable to remove the SRAF shape in the OPC iteration before mask build. We demonstrate the use in practice of our methodology to accurately auto-classify and filter images with SRAF printing on wafer. We demonstrate a scalable solution to improve the quality and reliability of SRAF print avoidance models and reduce the risk of printing SRAF by removing manual & subjective image classification.

10147-73, Session 6

Image contrast enhancement of multiple patterning features through lower light source bandwidth

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DUV immersion lithography (ArFi) continues to be the primary lithographic method for semiconductor manufacturers. Use of ArFi lithography requires patterning budget improvements in the range of 1/10 nm especially for interconnect layers [1]; for advanced process technology nodes, every Angstrom counts. Previous investigations into the effects of light source bandwidth on imaging performance have provided the foundation for this work [2-9]. This study will focus on the increase in image contrast that 200 fm light source E95 bandwidth enables on Self-Aligned Double Patterning (SADP) features. The impact of 200 fm E95 bandwidth on the CD and Edge Placement Error (EPE) performance of core (grating) and block features will be assessed using an imec 7 nm process node test vehicle. The on wafer experimental results will be compared with the simulation predicted responses of 7 nm features to lower light source bandwidth [10].

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10147-24, Session 7

Decomposition of the TCC using non-coherent kernels for faster calculation of lithographic images *(Invited Paper)*

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To our knowledge all OPC codes achieve practical compute times at full-chip scale by approximating partially coherent images as sums of coherent images, a methodology known variously as OCA, SOCS, or OCS. Though many refinements have been made to the OCA methodology since its introduction in the mid-'90s, the basic approach of decomposing the partially coherent Hopkins kernel (aka the TCC or Transmission Cross-Coefficient) as a sum of coherent systems has remained the state of the art for two decades.

Here we derive and demonstrate a new form of image decomposition that is designed to closely match those portions of the TCC which are most recalcitrant to coherent decomposition, thus providing a significantly improved speed/accuracy tradeoff. We refer to our new decomposition systems as "loxicoherent".

While coherent systems employ a single convolution kernel, each loxicoherent system uses at least two distinct kernels. As with standard coherent systems, compute time with loxicoherent systems is proportional (with some overhead) to the number of kernel convolutions. Tests with 1D patterns show that for a given kernel-count budget in the typical e.g. 10-100 range, image calculation error can routinely be reduced by at least 5X if loxicoherent systems are used in the decomposition. Loxicoherent systems likewise enable a given worst-case accuracy target to be achieved with at least 3X fewer kernels. Our new method has not been tested in 2D, but from theoretical arguments we expect the speed/accuracy tradeoff to remain far superior to that of standard OCA, though not by as large a margin as with 1D patterns.

Standard OCA kernels correspond to the pupils of coherent imaging systems. The output of a coherent system is linear in amplitude, whereas loxicoherent systems have a more complex structure that is entirely nonlinear even in the lowest-order term. The structure of loxicoherent systems will be explained in detail, and they will be shown to be well-suited for extraction of any near-Toeplitz components present in the TCC. Such components have an eigenvalue spectrum that decays very slowly, and so are difficult to capture with OCA.

We further show that TCCs for lithographic systems in fact contain strong Toeplitz-like components that arise from slope discontinuities associated with the sharp aperture of the projection lens. Asymptotically, the uncaptured TCC becomes dominated by such discontinuities, and under idealized assumptions the fractional portion of the remaining un-mapped TCC that each new OCA kernel is able to extract becomes arbitrarily small, in the limit where a very large number of kernels has already been extracted. In contrast, a single loxicoherent system is able to capture the entire remainder in this idealized limit. While these behaviors apply in an asymptotic regime that can never be fully realized, qualitatively similar behavior is seen with practical kernel counts.

The rich structure of loxicoherent systems makes them useful for matching recalcitrant portions of the TCC, but their increased complexity also makes them difficult to determine optimally in the general case. However, the largest practical benefit arises in the special case where the loxicoherent system must fit the TCC remainder left uncaptured by a typical set of OCA coherent kernels. In this special case a fast analytic method for choosing optimal loxicoherent kernels compares very favorably to brute-force numerical optimization. We further show that a loxicoherent system kernel which is least-squares optimal can be rigorously obtained under general conditions, analogous to choosing a TCC eigenfunction as the least-squares optimal (lone) kernel of a coherent system. However, this rigorous method only optimizes a single kernel in the loxicoherent system, and optimization of all constituent kernels is necessary to obtain full advantage from the loxicoherent structure. In many cases of practical importance it proves possible to determine all constituent kernels by combining quasi-analytic calculations with fast (linear) least-squares fits. Under general conditions a homotopy algorithm has been found to reliably produce an accurate and complete set of kernels, but tests have thus far been limited to 1D.

Loxicoherent systems can improve accuracy during ILT as well as OPC. By using adjoint differentiation the gradient of a cost function or Augmented Lagrangian can be calculated with the same FFT-gated near-linear area scaling that the forward intensity calculation exhibits.

10147-25, Session 7

Resist 3D aware mask solution with ILT for resist failure hotspot repair

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Traditional segment-based model-based OPC methods have been the mainstream mask layout optimization techniques in volume production for memory and embedded memory devices for many device generations. These techniques have been continually optimized over time to meet the ever increasing difficulties of memory and logic low-K1 patterning processes. These difficulties include the need for OPC and RET methods to work with increasingly coherent source patterns. More coherent sources have stronger local intensity variations that can occur in the X, Y and Z directions due to interference effects. The difficulties also include the need to pattern new negative tone photoresist materials which can suffer from increased resist top-loss and significantly non-vertical developed profiles. Therefore, the control of the resist CD through process window in the vertical direction is becoming increasingly important with each process node.

New inverse methods such as model-based SRAF placement, model-based SRAF optimization and full main feature + assist feature ILT are well known to have considerable benefits in finding flexible mask pattern solutions to improve process window and improve 2D CD control. In this paper, we describe and present results for a methodology to extend ILT's process window improving capabilities in order to co-optimize patterning variations in all three dimensions for 3D resist CD control. These improvements can be seen to reduce the risk of patterning failure at the bottom and top of critical resist features which a normal proximity correction, focused on only the middle of the resist film, would not be aware of. Ideally, mask optimization would use a full rigorous TCAD resist model to guide the correction at multiple heights in the resist. However, TCAD models are significantly slower than compact models in simulations and ILT already has high computational

requirements. Therefore, we have generated rigorously-tuned compact models fitted to the TCAD model resist profile data. We will show the significant process window improvements obtained with this new resist 3D aware ILT methodology.

10147-26, Session 7

Enhanced OPC recipe coverage and early hotspot detection through automated layout generation and analysis

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State-of-the-art OPC recipes for production semiconductor manufacturing are finely tuned, often artfully crafted parameter sets that are designed to achieve design fidelity and maximum process window across the enormous variety of patterns in a given design level. In the typical technology lifecycle, the process for creating a recipe is iterative. In the initial stages, very little to no “real” design content is available for testing. Therefore, an engineer may start with the recipe from a previous node, adjust it based on known ground rules and a few test patterns and/or scaled designs, and then wait to refine based on hardware results. As the technology matures, more design content becomes available to refine the keyword, but it becomes more difficult to make major changes without significantly impacting the overall technology scope and schedule. The dearth of early design information is a major risk factor: unforeseen patterning difficulties (e.g. due to holes in ground rules) are costly when caught late.

To mitigate this risk, we propose an automated flow that is capable of producing large-scale realistic design content, and then optimizing the OPC recipe parameters to maximize the process window for this layout. The flow was tested with a triple-patterned 10nm node 1X metal level. First design-rule clean layouts were produced with a tool called Layout Schema Generator (LSG). Next, the OPC recipe was optimized on these layouts, with a resulting reduction in the number of hotspots. For experimental validation, the layouts were placed on a test mask, and the predicted hotspots were compared with hardware data.

10147-27, Session 8

3D printed complex microoptics: A new paradigm in optics manufacturing *(Invited Paper)*

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We demonstrate a fundamental paradigm shift in microoptics manufacturing. Using femtosecond two-photon 3D printing with 100 nm spatial resolution, the time from lens design and structural assembly layout to manufacturing and optical testing can be reduced to less than 24 hours. Even complex microscope objectives with multiple aspherical and non rotationally symmetric freeform surfaces can be manufactured. We demonstrate diffraction limited performance and MTF measurements across a large field of view of such systems that can be as small as only 100 μm in diameter, directly fabricated onto the ends of optical fiber tips. Other applications such as phase shapers or miniaturized illumination systems are also presented.

10147-28, Session 8

A physical model for laser direct-write lithography

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Laser Direct Write Lithography (LDWL) involves scanning a focused laser beam over a photoresist material. This maskless patterning technique provides a simple fabrication method for arbitrary three-dimensional structures and has a resolution in the order of hundred nanometers. We present a simulation approach that includes most resist and optical effects in experimental LDWL literature (Fischer, Wegener 2013; Xing et al. 2007). We compare three laser write schemes, namely: single photon absorption (SPA), two photon absorption (TPA), and stimulated emission depletion (STED) lithography.

Simulation method: The simulation flow implemented in our work is divided into four stages: bulk image, exposure, dark polymerization, and development. The bulk image computation involves light reflection, propagation, focusing, and linear absorption in the resist. The bulk image computation result is the 3D intensity distribution in the resist. Typical LDWL processes employ negative-tone photopolymers. The absorbed intensity in these materials triggers exposure reactions, leading to generation of photoradicals and an increase in temperature. The photoradicals subsequently initiate polymerization reaction to form polymers, which serve as inhibitors for the development process. By applying a fast marching algorithm for the development process, we computed the developer arrival time (DART), which corresponds to the fabricated structure. The following flowchart summarizes the effects covered in our model.

Using the developed methodology, we computed the three-dimensional polymerization profile for three laser write processes: single photon absorption (SPA), two photon absorption (TPA), and stimulation emission depletion (STED) lithography. The polymerization profile for a single exposed position (voxel) determines the smallest features that can be fabricated for a given fabrication process.

The simulation result (Figure 2) demonstrates the limited capabilities of SPA for the fabrication of 3D patterns. It is mainly used for the patterning of thin (planar) resist layers. In contrast to that, TPA and STED provide better resolution and also a 3D localization of the polymerization profile. STED lithography leads to the best resolution of the three fabrication schemes.

Several examples will demonstrate the application of the developed modeling approach for the investigation of LDWL in the fabrication of 2D and 3D patterns.

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10147-29, Session 8

Large-area high aspect-ratio plasmonic interference lithography utilizing single high-k mode

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Plasmonic lithography has shown the potential to break the diffraction limit, by exploiting the small wavelength of the surface plasmon polaritons (SPPs). Though the feature size of the patterns can be subwavelength, it generally suffers from the low contrast and the shallow pattern depth due to the evanescent wave nature, which seriously limit its practicality. In this work, by using a plasmonic nanolithography approach, high aspect ratio subwavelength patterns with pitch equal to one-half the period of the photomasks, and half-pitch about 1/6 of the wavelength were achieved with uniformity in cm areas.

The diagram of the proposed system consists of the mask and the substrate to be exposed. During exposure, the mask is in conformal contact with PR layer on the substrate to ensure the near field wave coupling. The mask is on a glass substrate, composed of an one-dimensional (1-D) Al grating with 22 nm thickness, 245 nm period and 50% duty cycle, followed by a 40 nm poly methyl methacrylate (PMMA) spacer and a 10 nm Al layer underneath. The substrate is a polyethylene terephthalate (PET) sheet coated with 15 nm Al, 44 nm SiO2 and 100 nm photoresist (PR) layer. 405 nm wavelength TM polarized light is incident on the grating mask, and harmonic modes are excited with the extra momentums provided by the grating. The first order wave couples to the SPPs at the Al/PMMA interface and form a strong high-k resonance. The thin Al film blocks the direct incident light, but transmits the resonance. Therefore, uniform subwavelength patterns can be imaged on the photoresist, producing uniform patterns by single mode interference. To generate high aspect-ratio patterns, we made the PR layer part of an optical waveguide, which significantly improves the propagation depth of the pattern.

Large-area sub-wavelength periodic structures were obtained with approximately 55 nm linewidth, which is less than 1/6 of the light wavelength. The period of the pattern is 122.5 nm, which is 1/2 of the grating mask, and the aspect ratio is around 2:1, significantly improved over previously reported results.

To study the impact of the resist thickness, PR with thickness of 200 nm was also tested aiming for even higher aspect ratio patterns. The approach described above is general and can be applied to other wavelengths. For example, by using 193nm illumination, half-pitch down to 13 nm can be achieved. In addition, other than simple 1-D grating, two-dimensional (2-D) structures can be generated by multiple exposures in experiment. The design criteria can also be applied in the non-contact waveguide lithography systems.

10147-30, Session 8

Analyses of line-edge roughness in plasmonic lithography

Gaofeng Liang, Xi Chen, L. Jay Guo, Univ. of Michigan (United States)

Plasmonics based photolithography has been able to achieve pattern size beyond the typical diffraction limit by exploiting the surface plasmon (SP) [1]. However, film roughness is inevitable in practical fabrication, and can strongly impact the performance of the lithography. In our work, exemplary lithography systems including superlens and hyperbolic metamaterial (HMM) based approaches are considered, where the effects of films roughness and the defects on the mask are analyzed systematically.

For the superlens system, a chromium (Cr) mask with thickness of 50 nm and period of 90 nm on glass substrate, is placed above the superlens with a poly-methyl-methacrylate (PMMA) spacer layer. A silver (Ag) film with thickness of 20 nm transmits the transverse magnetic (TM) polarized light with wavelength 365 nm the photoresist (PR) film with thickness of 40 nm. A reflector composed of an Ag film with thickness of 50 nm is added at the bottom of the PR. For the HMM system, Cr mask is used with period of 360 nm and the multi-layer structure is composed with 9 layers of 15 nm thick aluminum (Al) and 30 nm thick silicon dioxide (SiO2) films. The PR is also 40 nm and reflector film is an Al film with thickness of 50 nm.

The broad optical transfer function (OTF) of the smooth Ag enables the evanescent waves of wide wave vector range to pass through [2]. While the OTF of HMM shows that only ±2nd order diffraction waves with the wave vector about 2k_0 can pass through [3]. Different degrees of roughness are introduced on the films and the photomask, and the performance of the two systems in terms of the intensity, pattern uniformity and line edge roughness are compared. As the roughness of the films grows, the OTF of the superlens degrades dramatically, while the OTF of the HMM maintains, as shown Figure 1 and 2. Accordingly, the field distribution of the HMM system is less affected by the film roughness, thereby can still produce high quality periodic patterns. By properly choosing the period of the mask, the desired transmission order coincides with the peak of the OTF function. Therefore, the light of desired spatial frequency transmits maximally, while the other diffraction orders induced by the rough surfaces is relatively suppressed, leading to a pattern with better uniformity. On the other hand, the superlens case does not offer such a utility because of the broad transmission function in OTF. But superlens can image arbitrary patterns; while the drawback is that line-edge roughness of the mask will also be imaged onto the photoresist. Therefore, the impact of a single defect on the mask pattern is much greater than that of the HMM approach.

In addition, the waveguide lithography system consists of aluminum (Al) layers acting as a filter shows similar behavior compared with that of the HMM system. Though the structure is almost identical to the superlens structure, but the thin metal film serves a very different function in this case, which confirms the distinctive advantage of the frequency selective scheme. Meanwhile, our simulation shows Al can be a good superlens at 193 nm, which indicates that the same metal can function differently in different schemes or wavelengths.

10147-31, Session 8

Neuroelectronic device process development and challenge

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We investigated the fabrication of small neuroelectronic device consisting of four shanks with 16 electrodes per shank for simultaneous neurochemical and brain activity monitoring. The 16 electrodes on each shank have a separation distance of 100 microns. Each shank has a width of 40 microns with separation distance of 7750 microns. This design eliminates single-site recording with limited individual conductors and permits rapid characterization of multiple neurons simultaneously at multiple brain depth/sites, consequently providing ground-breaking capabilities for parsing neurochemical release and brain activity. The device is fabricated on (100) silicon substrate and is fully integrated with electrode, interconnect and bond pad fabricated on one chip. Gold rectangular pyramid electrodes are selected as the recording electrodes to enhance the non-invasiveness associated with heating and minimizing surrounding biological tissue damage. The gold electrodes are deposited on the etched silicon substrate with 200 nm LTO sacrificial layer. Each electrode has top area of 6 um x 60 um and depth of 750 um. The interconnects provide electrical connection between electrodes and bond pads and are sandwiched between thin polyimide layers to prevent them from breaking while maintaining the flexibility. Final bond pads and electrodes are all passivated with polyimide to provide mechanical support. Upon device release, the recording electrodes are exposed to directly contact brain structure, and the exposed bond pads are soldered on the circuit board to transport signals to the measurement instrument. The entire process involves 5 photomasks. Process development and integration challenges will be reviewed and discussed in the paper.

10147-22, Session PSWed

Machine learning-based 3D resist model

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Accurate prediction of resist profile is important in lithographic hotspot verification. Non-ideal resist profiles due to low image contrast and small depth of focus, e.g. footing, T-topping, and top-loss (Figure 1), affect etch resistance and post-etch results. A standard resist prediction relies on 2D resist model, and a contour image at pre-determined resist height is estimated, which cannot distinguish between ideal and non-ideal profiles shown in Figure 1. Rigorous simulation of resist profile in full-chip level is computationally very expensive. Alternative straightforward approach is to build individual 2D models at some different image heights. However, the relevant image heights need to be predetermined by engineers themselves; furthermore, the individual 2D models may deviate from each other during the separate calibration processes, which may result in abrupt change of 2D contours at the adjacent heights.

Our approach to 3D resist model is illustrated in Figure 2. At particular location of a layout, a number of parameters (e.g. local densities and optical kernel signals) are extracted by scanning nearby mask patterns. These parameters are submitted to an artificial neural network (ANN), which outputs predicted height of remaining resist after a lithography process. Optimizing ANN so that the difference between predicted- and actual-resist height is minimized is important. This is performed by refining predicted resist height by comparing it to actual resist height that is obtained by a rigorous simulation; the process is repeated for each layout position and using a number of sample layout patterns. The final ANN corresponds to our 3D resist model. Due to discontinuity of the predicted resist heights, an image processing such as interpolation is subsequently required to reconstruct resist profile.

Accuracy and efficiency of our approach are determined by the parameters that are chosen and the structure of ANN that are employed. A few parameter sets, e.g. local densities (Figure 3(a)), optical kernel signals (Figure 3(b)), and their combinations, are tried and their impact on accuracy and efficiency are assessed. ANN structure is optimized by varying the numbers of layers and nodes and assessing the corresponding accuracy achieved from the structure.

A number of applications of 3D resist model are considered including lithographic hotspot detection, assist feature printing detection, and resist profile-aware mask optimization. Our approaches are implemented on top of Proteus, and compared to conventional methods that Proteus supports using conventional 2D resist model.

10147-48, Session PSWed

Improving the topography performance of ion implantation resist

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As the lithography process enters 1X nm node and beyond, the CMOS device evolves from planar structure to three dimensional structure, such as Fin-FET. By utilizing a specific 3D physical structure, Fin-FET outperforms the traditional planar device in short channel effect, sub-threshold slope, random dopant fluctuation, and high-speed performance. However, the wafer topography structures, including shallow trench isolation and poly gate, will cause a severe degradation of the resist profile and great critical dimension variation. Traditional bottom anti-reflective coating can alleviate this issue, however it requires etch process to open, which may cause plasma induced substrate damage. The developable bottom anti-reflective coating (DBARC) seems as the promising solution for ion implantation layer lithography. But issues like photo-speed and proximity matching between the resist and DBARC, and issues associated with developing may lead to process failure.

With the purpose of reducing the wafer topography effects without adding an additional coating, a novel method is proposed in this paper. Herein various parameters that may have impact on the resist topography are investigated firstly. By utilizing the rigorous simulation algorithm in PROLITH, the density, height, and corner rounding of the fin structures, the height and corner rounding of the gates are analyzed in detail. It is shown that the wafer topography effects are not sensitive to the dimensional parameters of fins, and only the height of poly has a significant effect on wafer topography. Then the relationship between the wafer topography and the material of poly is investigated from the theoretical point of view. From the Fresnel formula, it had been demonstrated that if the refractive index of resist is smaller than that of poly, there is a half-wave loss when the light transmits from the resist to poly. Hence, the intensity of resist image between two gates can be so weak that the developer cannot completely remove the resist. But the intensity will be improved when the refractive index of poly is decreased to a value smaller than that of resist. Therefore, a novel method with increasing the thickness of the oxide on the edge of the gate is proposed to improve the performance of wafer topography. After verification with rigorous simulation, the intensity of resist image is positively related to the thickness of the oxide on the edge of the gate. At last, we choose a typical Fin-FET structure as an example to discuss the possibility of improving the resist topography by only optimizing the resist parameters. In the simulations, the bright field mask and positive resist is used, and 248 nm lithography is applied to expose the mask of ion implantation layer. Due to the wafer topography, the resist between the gates cannot be developed completely before the resist parameters optimization. The simulation results show that although the optimized resist is not suitable for other pattern, the resist profile of ion implantation layer can be largely improved.

10147-49, Session PSWed

Quasi sinusoidal single-order diffractions with hexagonal aperture gratings

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Spectral measurement plays a central role in nearly all aspects of modern optical science and engineering. Spectrum unscrambling only needs the first order diffraction of the traditional black-white grating, and unwanted higher order diffraction always overlaps the first one, which greatly degrade precision of analysis. It's known that sinusoidal transmission gratings only have 0th and +1st/-1st order diffractions, but they are more difficult to fabricate than the black-white structure. The high order diffractions can become evanescent waves with a grating period in the range of the wavelength. Unfortunately, for short wavelengths less than 100 nm, it's difficult to scale the grating period down to the wavelength size by the current nanofabrication technology. Therefore, it has been a goal to design the black-white structure much larger than the wavelength with the suppression of high order diffractions.

In this letter, triggered by photon sieves, we propose the quasi sinusoidal single-order diffractions with hexagonal holes. The key idea is to make the hexagonal holes follow the rectangle array, leading to dominant +1st/-1st diffraction orders on the observation line. Such structure has great advantages from X-rays to far infrared wavelengths. The location distribution of holes according to some statistical law results in a desired diffraction pattern. Moreover, the membrane with holes is easy to freely stand and this will benefit the fabrication, and lead to more stable free standing structure. We numerically and experimentally demonstrate the diffraction pattern of the quasi-periodic hole array with only 0th and +1st/-1st orders. Compared with the previous schemes, the single-order diffraction grating with binary transmittance value of 0 and 1 based on this kind of transmission function, which is larger than the value of 6.25% for ideal sinusoidal amplitude grating.

This new type of single optical element with the capabilities of quasi-single order diffraction named hexagonal aperture gratings (HAGs), consists of a series of periodically arranged hexagonal apertures. Such structure can help to suppress 2N order diffractions over the whole plane (N is integer). Since the HAGs have the periodic distribution along the x axe, resulting in a significant effect of suppressing 3N order diffractions. Finally, we obtain a single order diffraction which suppresses 2N and 3N orders efficiently. The

key of the HAGs is designed to improve the first order diffraction efficiency.

The numerical results that the high-order diffraction can be suppressed significantly and similar to the ideal case, and the corresponding absolute diffraction efficiency of higher orders is less than 0.0111%. In addition, the absolute diffraction efficiency of±1st orders, ±5th orders and±7th are 6.94%, 0.044%, 0.00676%, respectively.

Both numerical solution and experimental results demonstrate the diffraction efficiency of the HAGs. The high-order diffraction of the HAGs is effectively suppressed and merges into the noise, which confirms the validity of HAGs. Furthermore, the minimum linewidth of the HAG is 4?m, which offers credible opportunities for scaling the grating down to the x-ray region. The new design offers an idea of single-order diffraction and benefit in fabrication. This would be of great significance to the practical application of optical micro- and nanostructure fabrication.

10147-51, Session PSWed

Eliminate the vibration defect for laser interference lithography using an optical chopper system

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Laser interference lithography (LIL) is a maskless lithography technique with many advantage such as simple optical design, inexpensive, infinite depth of focus, and large area patterning with single exposure. Compare to the tradition optical lithography, LIL is very suitable for applications which need period nanostructure, such as grating, light-emitting diode (LED), photonic crystals, and etc. There are two types of LIL systems: Lloyd's mirror interference system and multi-beam interference system. Our lab have developed both system and successfully fabricated 2D and 3D nanostructure.

However, due to the principle of LIL, the exposure result is very sensitive to the light source and the environment vibration. Defects which perpendicular to the grating occurs when the LIL system is effect by the environment vibration. The reason that cause this defect is Moiré fringe. When the period structure is fabricated in an environment with vibration source, the grating structure will have a small angle rotational vibration and the Moiré fringe defect is formed.

In order to eliminate the Moiré fringe defect, this paper developed a new LIL system with chopper and accelerometer. The sensor can measure the vibration frequency. And by setting the chopper frequency equal to the vibration frequency, the Moiré fringe defect can be eliminate.

In this paper, we use a piezo stage to generate a stable vibration with tunable frequency. In this way, we can produce a repeatable Moiré fringe defect. By setting the chopper frequency equal to the stage frequency, the Moiré fringe defect can be eliminate. And we successfully fabricated large area period structure without any vibration defects. The period structure is 420nm pitch and the area is 20x20 mm2.

10147-53, Session PSWed

The pattern-matching based OPC approach for preemptively fixing the weak points

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The optical proximity correction (OPC) systematically adds the bias with respect to the designs to the mask, correcting the proximity effects associated with sub-wavelength features. Due to the complex nature of main features of the circuits, even a carefully tuned OPC recipe can yield thousands of weak points for each tape-out. Some of these weak points require manual fixings which might demand considerable amount of effects from engineers. It has been found that for different tape-outs, the resulting OPC patterns that require manual fixings share quite a lot commonalities or are even the same. Repeatedly performing manual fixings for the same type of weak points for different tape-outs presents a waste of human efforts. We therefore constructed a pattern library for these types of weak points. At the very of beginning of an OPC recipe, the design patterns of these types of weak points are used to scan the whole chip and find the same or similar patterns. Then, the pre-calculated OPC and SB (scattering bar) layers are pasted to the relevant positions. The pasted pattern will be kept fixed and serve as boundary condition for the subsequent model-based OPC. The final resulting OPC layer will be free of those types of weak points that require manual fixings.

10147-54, Session PSWed

RET solution optimization for extremely low-k1 metal process

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With technology shrinks, optical lithography is push towards lower k1 factor and often suffers trade-off in image contrast and depth of focus (DOF) for resolution. Various resolution enhancement technologies (RET) are adopted to help us move on, like immersion lithography, multi-patterning process, source mask optimization (SMO) and so on. Multi-patterning technology do help on getting higher k1 factor for lithography process, but for single patterning process, metal layer with extremely low-k1 process is remained as the most challengeable layer. Traditionally, RET will apply strong off-axis source, sub-resolution assistant feature (SRAF) and advanced optical proximity correction (OPC) for this layer. But we found there were gaps between the design rules and production chip designs, which caused our RET solution developed from design rules could not fulfill the process request of real chip design. We also found that target changes had remarkable impact on final RET result. To deliver a sophisticated solution and ensure process-window (PW), OPC engineers will play a more important role than ever before. Besides analyzing the information provided by process engineers, OPC engineers need to explore the possibility of co-optimizing each member of RET family.

This paper demonstrates a serial of DOE for RET optimization on full chip level. The results show significant improvement for full chip OPC quality by simulation. We also correlates simulation and wafer result and proves the effectivity of RET optimization methodology for this super low-k1 process.

10147-55, Session PSWed

Lithography and OPC friendly triple patterning decomposition method for via

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ArF immersion lithography is still a key candidate below 10nm node. Many challenges should be overcome when CD shrinks to such a tiny size. In the whole manufacturing flow, triple patterning (TP) is an important process. TP decomposition is used to decompose customers' layout into three individual masks. Each of the decomposed masks can be imaged in a single exposure.

The chief purpose of the decomposition is to make the decomposed masks fulfill the design rules. However, rare research is focused on the influence of decomposition result on the other processes, such as lithography, OPC (Optical Proximity correction), etch, etc. Thus, a decomposition result that is unfriendly to other processes may happen. Forbidden pitch is an obvious factor that should be considered in the decomposition process. Forbidden pitch can reduce image contrast and then lead to a reduction of the process window. It is also difficult to add SBARs and correct the optical

proximity effect for forbidden pitch. Because pitches of the decomposed patterns can be changed in the decomposition process, if the forbidden pitch were eliminated in the decomposition process, it make other process easier. However, the general TP tool didn't fulfill this target. As illustrated in the following Fig. 1, pitches that are smaller than the minimum pitch of single exposure violate design rules, in other words, sub design rules appear. Sub design rules are certainly be eliminated after the pattern decomposition. However, forbidden pitch is larger than the minimum pitch of single exposure, and they may be decomposed into two different masks or in the same mask randomly, as shown in Fig. 1(a). What's more, if the forbidden pitch is treated the same as sub design rules, it may make the decomposition result confused.

In this paper, we provide a lithography and OPC friendly triple patterning decomposition method. The decomposition is classified into critical decomposition and optional decompositions. The critical decomposition is applied for pitches which are smaller than the minimum pitch of single exposure. The optional decomposition is firstly applied for pitches which are in the range of forbidden pitch, and then applied for pitches in the other ranges. The critical decomposition is assigned the highest priority, and the optional decomposition for the forbidden pitch is assigned the second highest priority, the decomposition for other pitches are assigned lower priorities, as shown in Fig. 1 (b). The TP tool firstly decomposes patterns with the highest priority, then it decomposes patterns with the second highest priority, finally it decompose patterns with other priorities. This method can decompose patterns with forbidden pitch as far as possible. By utilizing TP tool from Mentor graphics, we test the proposed method in a VIA layer layout. The number of forbidden pitch in the decomposed masks is calculated to evaluate the effect of TP result. And the process window for the proposed method is calculated and compared to the general TP method. The results shows the number of forbidden pitch is reduced and the window of process is enlarged. In addition, the proposed method can be easily extended to suitable for other multiple patterning (MP) process, for example, quadruple patterning (QP) process. And the idea of assigning different priorities in the decomposition can be also used for process optimization further.

10147-56, Session PSWed

3 key parameter correlations on the cutting-edge DUV light source

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Compromising higher performance and cost advantage simultaneously discovered to immersion lithography tool. These are mandatory key parameters which are currently required for the lithography technology in manufacturing cutting-edge technology nodes. Now that more than 10 years have passed since the immersion lithography technology was applied to mass productions, this is a new trend which has deviated from conventional trend of shorter wavelength and higher NA. In consequence, requirements meeting several parameters to satisfy demand which is the other end of higher performance. In another background, rare gases such as Neon and Helium have been at risks for running out or short supply lately and now utilities have emerged as an important parameter. More specifically, it is important to optimize 3 key parameters which are performance improvement, longer module life providing improved uptime and lowered cost, and low utility usage for the DUV light source. At the same time we need to recognize it is possible that there is a discrepancy between single parameter optimization and common parameter optimization in some cases.

For the performance of the DUV light source, it is a challenge to improve spectral performance called E95% which influences the optical performance with lithography technology. By improving E95%, we can also improve and stabilize contrast as part of printing performance as well as enhance the CD characteristics. At the same time, obtaining a stable light source power can be a parameter to stabilize CD characteristics and improve yields. Performance-driven parameters we obtain from the light source contributing to CD characteristics, Chambers which are modules integrated into light sources and Line narrowing optics, are strongly correlated to the gases and electricity usage. For instance, when light source oscillates with lean gas condition, there should be a variation in the output energy, and also the chamber electrodes are to be worn. Nevertheless we can obtain instantaneous line narrowing spectral performance hence CD characteristics may improve in contrast. More specifically, these 3 parameters, i.e. performance, module life & cost, and utility usage, strong relations to one another.?We should measure and understand each sensitivity and correlation. In addition to that, it is also important to identify to which level of performance parameter the module life/cost and utility usage parameter optimization should be comparable.

Leveling performance parameters can systematically define additional process latitude given to applications of lithography process, and consequently this should enhance the general versatility such as reduction in cost and utility usage. We believe that such improvements in the general versatility should surely play a significant role to make higher performance coexist with commoditization, which are opposing requirements each other for long-lasted immersion lithography technology.

10147-57, Session PSWed

The ultra-violet partial coherence modulation transfer function for lithography

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The critical dimension(CD) is main factor to determine the line width of semiconductor equipment fabricating ability for the smallest line width of produced electronic components. Modulation transfer function(MTF) has been popularly used to evaluation the optical system, due to the contrast of each line-pair in dimension analytically, however, while the light source is coherent or near coherent for the small dimension near the optical diffraction limit, the MTF is hard to achieve consistently.

The study of ultra-violet partial coherence modulation transfer function is to calculate the 1-D and 2-D the line with an optical design program, to estimate the MTF near the size of diffraction limit. It provides fabricating parameter for a 1-to-1 TSV lithographic system. By applying partial coherence analysis, the optimized relative numerical aperture (RNA) has found. As the system is built, the optimized performance should be expected.

10147-58, Session PSWed

Constructing freeform source through the combination of neural network and binary ant colony optimization

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Source Optimization is one of key techniques to enhance the process window in ArF 193-nm immersion lithography process. This study proposes a source optimization algorithm with the use of metaheuristic based binary ant colony source optimization (ACO) and artificial neural network (ANN). The purpose of this study is to form the optimal freeform source improving the process window of the critical patterns and maintaining the quality of the aerial image. The source plane is pixelated and divided into 12 sectors. Each pixel source is arranged in order and the binary ant colony algorithm is applied on each pixel sequentially to form an optimal freeform source shape. The decision to turn-on or turn-off the pixel is based on the probability depending on the pheromones concentration on the searching path. The high pheromone concentration on the path indicates the effective pixel on minimizing the objective function. In this study, the improvement of depth of focus, contrast and the quality of aerial image are the main objects in the optimization process. A set of the input data for training the ANN in this research includes the pattern edge contours resulted from the various process conditions with respect to each searching agent in each iteration.

The trained ANN selects sectors with effective pixel sources illuminating the target pattern to enhance the aerial image quality and improve the process window. The proposed ANN determines the searching priority in the ACO and the weighting for each sector on source plane. The weighting is used to determine the probability of the pixel source on the sector. The smaller weightings indicate the less effect of the source point on the improvement of process windows and the aerial image quality. The combination of the ACO and ANN methods can decrease the searching space and speed up the convergence of the binary ACO. We use PROLITHTM from KLA-Tencor to calculate the aerial image when using the optimized freeform source. There are two parameters for evaluating the lithography process performance: pattern error and edge placement error. The pattern error is used to evaluate the quality of aerial image and the edge placement error is used to evaluate the deviation of critical pattern edge contours resulted from various process conditions. The developed algorithm will be tested using the 17 clips of 1D line/space pattern with various linewidth, pitch and line orientation. The testing pattern includes nine horizontal line features and eight vertical line features. The minimum linewidth is 40nm with the pitch 80nm and the maximum linewidth is 120nm with the pitch 500nm. An optimized freeform source will be constructed for these 17 clips simultaneously. The imaging performance for these 17 clips will be presented.

10147-59, Session PSWed

Development of the next-generation ArF excimer laser with ultra-narrow stable spectral bandwidth for multiple patterning immersion lithography

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Multiple patterning ArF immersion lithography has been expected as the promising technology to satisfy tighter leading edge device requirements. In cutting edge exposure condition, the improvement of device yield and the reduction of operational costs are demanded. In order to satisfy their demands, we carry out some developments to improve spectral bandwidth performance of light source without helium usage. Narrower spectral bandwidth will improve device yield and stable spectral bandwidth will reduce CD variation. Helium free operation will reduce costs of operation and will reduce impact of difficulty to obtain rare resource, helium gas.

Laser beam of the high duty cycle operation heats purge gas up in the Line Narrowing Module (LNM). Heat distribution leads to refractive index variation and brings distortion of wavefront, which broadens a spectral bandwidth. Helium gas purge has usually employed because the refractive index variation of helium gas is approximately ten times more insensitive to temperature rises than that of nitrogen gas. However, since the price of helium gas is in inflation due to increasing worldwide demands of helium gas, using nitrogen gas as alternative purge gas of helium gas has been desired.

Newly developed ingenious LNM configuration enables thermal wavefront deformation of laser beam to reduce without depending on purge gas, which allows spectral bandwidth to become narrower than that of previous LNM and which realizes helium free operation. Ultra-narrow spectral bandwidth in which E95 reaches 0.20pm will help improvement of device yield. Helium free operation will be useful for the reduction of operational costs and the increasing continuity of high volume manufacturing independent of helium gas shortage.

In our laser system, a spectral bandwidth is controlled by adjusting the wavefront of a laser beam using a two-lens optical system within a resonator. At the beginning of oscillation, the spectral bandwidth has large deviation from target because of thermal relaxation happened during the period of wafer exchange operation. An actuator drives lens system, and there is a long time to return spectral bandwidth to target because the driving speed of current actuator has relatively low speed, which limits the stability of spectral bandwidth. Therefore, we adopt very fast actuator with thirty times faster speed than that of old actuator and adopt new control method in order to utilize the fast speed. The fast actuator and the new control method improve stability of spectral bandwidth, which realizes typically E95 5fm shot average and which will contribute to further reduction of CD variation.

These developments will be upgradable for our ArF excimer laser, GT64A. In the presentation, the latest development status will be shown.

10147-60, Session PSWed

Excimer laser gas usage reduction technology for semiconductor manufacturing

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ArF and KrF excimer lasers are widely used as a light source for the lithography process of semiconductor manufacturing. The excimer lasers consume laser gas mixture in a discharge chamber as laser media, and more than 96% of the gas mixture is Neon. Recently Neon supply and demand balance became critical situation; the price has risen last year due to the instability of politics and economy in Ukraine. Although neon price decreased now, its price is still higher than two years ago.

Gigaphoton has released gas consumption reduction, called Total Gas Management (TGM) series, as part of the green activities. Conventional gas consumption reduction option (eTGM) achieved 50% gas consumption reductions from the former gas control option (sTGM) by optimizing the laser gas control. In order to reduce gas consumption further, Gigaphoton has been developing new gas management option hTGM that employs a gas recycle system. The degraded laser gas mixture, that causes the decrease of the laser power, contains small amounts of impurity such as fluoride compounds and rare gas molecules itself do not change. In hTGM option the gas recycles system purifies used gas so that laser can use it repeatedly. We started field evaluation of KrF gas recycle system. The KrF gas recycle system was connected to five KrF laser systems and achieved 85% of the gas recycling ratio, keeping laser performance within their specifications.

In the case of ArF laser, the laser performance is much more sensitive to the impurity than that of KrF. Furthermore, several ppm orders Xenon gas is added to the ArF excimer laser gas to maintain the laser performance, and control of the Xenon concentration is important. In spite of the difficulties of managing ArF laser gas mixture, we achieved more than 50% of the ArF gas recycling ratio. We will continue to improve these gas recycling systems to increase the gas recycling ratio.

10147-61, Session PSWed

The thermal aberration analysis of a lithography projection lens

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In optical lithography tools, thermal aberration of a projection lens, which is caused by lens heating, leads to degradation of imaging quality. Besides of in-line feedforward compensation technology [1], the thermal aberration can be reduced by optimizing projection lens design. Thermal aberration analysis of a projection lens benefits the optimization of projection lens design. In this paper, thermal aberration analysis methods using physical model and simplified model are compared. Physical model of lens heating provides accurate thermal aberration analysis, but it is unable to analyze

the contribution of an element of the lens to thermal aberration which is significant for thermal optimization. Simplified model [2] supports thermal analysis of an element of a lens. However, only the deformation of lens surface and the variance of refractive index are considered in the simplified model. The thermal aberration analysis, in this paper, shows not only the deformation of lens surface, the variance of refractive index but also the change of optical path should be considered in thermal aberration analysis. On the basis of the analysis, a strategy for optimizing projection lens design is proposed, as shown in Fig.1. The strategy can be used to optimize thermal behavior of a lithography projection lens.

10147-62, Session PSWed

Application of optical similarity in OPC model calibration

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The computational models used for optical proximity correction (OPC) describe process steps in lithographic wafer patterning. The ability to calibrate OPC models accurately and efficiently is desired to minimize the lithography process development time. The model calibration process involves tuning of the model parameters using critical dimension (CD) data measured on the wafer to minimize the error between the measured and simulated critical feature dimensions. One important aspect of model calibration is the selection of the features that are measured. The feature patterns used for model calibration usually include combinations relatively simples features such as lines and spaces or end-to-end configurations of varying sizes and pitches. However, it is imperative to obtain good model accuracy on complex geometries encountered in full chip designs. Hence model accuracy is usually verified on complex feature geometries. Since lithographic process development often involves multiple cycles, usually with accompanying OPC changes, it is sometimes desired to determine if the mask changes are significant enough to require model recalibration or not.

In this paper, we introduce the concept optical similarity between features that is derived from the description of the optical intensity used in OPC models. The optical intensity computation designed for efficient full-chip applications involves the decomposition of the optical system transfer functions into eigenfunctions, or optical kernels, via the sum-of-coherent-systems (SOCS) approximation. The optical similarity analysis is based on comparing contributions from the different optical kernels to the overall intensity. Two features are considered similar if their relative intensity contributions from the different optical kernels are similar. Optical similarity is applied to selecting features for calibration from a larger set of features. It is also applied to understanding whether changes to the calibration pattern resulting from OPC changes would be significant enough to require model recalibration. Additionally, a systematic approach to apply relative weights to different calibration features in order to improve model fit on complex verification data is presented.

10147-63, Session PSWed

Compact modeling for the negative tone development processes

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When the negative tone development (NTD) process was introduced into photolithography, it brought fidelity improvement with it. However, the NTD process behaves in a manner that is not readily comprehended by the computational techniques used to create high speed photolithography models for use in the Optical Proximity Correction process. These effects are mechanical in nature and are not governed by the diffraction phenomena used to create high speed process models. This study will discuss an attempt to utilize the high speed OPC model methods to deliver an accurate representation of the NTD process.

This paper will study a compact modeling flow for NTD processes. The flow works to emulate first principle modeling techniques for NTD in an OPC model. This is accomplished through a combination of the new mechanical methods and traditional Dill's parameters. It also reduces the data volume required to generate the OPC model.

The models generated using this method accurately represent NTD SEM image contours. The results will be demonstrated and discussed.

10147-64, Session PSWed

Addressing optical proximity correction (OPC) challenges from highly nonlinear OPC models

Stephen Jang, Synopsys, Inc. (United States)

Model-based optical proximity correction (MB-OPC) has been widely applied in the advanced lithography process today. As k1 factor decreases and circuit design complexity increases, various advanced OPC modeling techniques have been employed to better simulate the lithography processes, such as mask3D (M3D), negative tone development (NTD) modeling techniques, etc., which as a result bring many challenges to MB-OPC in controlling edge placement error (EPE) and critical dimension (CD) while maintaining non-aggressive mask correction where possible for mask-rule check (MRC) compliance and better yield. In this paper we will discuss about the symptoms to these MB-OPC challenges, and show our integration of inverse lithography technology (ILT) with OPC as the solution to these challenges.

10147-65, Session PSWed

Alignment solutions on FBEOL layers using ASML scanners

Pavan K. Samudrala, GLOBALFOUNDRIES Inc. (United States)

Wafers at FBEOL layers traditionally have higher stress and larger alignment signal variability. ASML's ATHENA based scanners, commonly used to expose FBEOL layers, have large spot size (~700um). Hence ATHENA captures the signal from larger area compared to the alignment marks which are typically ~40μm wide. This results in higher noise in the alignment signal and if the surrounding areas contain periodic product structures, they interfere with the alignment signal causing either alignment rejects or in some cases- misalignment. SMASH alignment sensors with smaller spot size (~40μm) have been used to reduce mark/wafer rejects. However, due to the process variability, the alignment issues still persist. For example, the aluminum grain size, alignment mark trench deposition uniformity, alignment mark asymmetry and variation in stack thicknesses all contribute to the alignment signal variability even within a single wafer. Here, we propose a solution using SMASH sensor that involves designing a new alignment marks to ensure conformal coating. We also present new techniques and controls during the coarse wafer alignment (COWA) including tighter controls for wafer parameters, longer scan lengths on alignment marks and weighted light source between Far Infra-Red laser (FIR) and Near infra-red (NIR) for the alignment. All the above mentioned techniques, when implemented, have reduced the wafer alignment reject rate from around 25% to less than 1%. Future work includes mark validation based on the signal response from the various laser colors. We also explore monitoring the process using alignment parameters.

10147-66, Session PSWed

Novel methodology to optimize wafer alignment to enhance 14nm on product overlay

Pavan K. Samudrala, GLOBALFOUNDRIES Inc. (United States)

With continuous shrink in feature dimensions, overlay tolerance for fabrication of transistors is getting more stringent. Achieving good overlay is extremely critical in getting good yield in HVM environment. It is widely understood that good alignment during exposure is critical for better on product overlay [1]. Conventional methods to choose alignment marks on ASML scanners are based on comparing alignment key performance indicators (KPIs) including signal quality, grid repeatability, etc. It is possible that even with good alignment KPIs, OPO is still impacted. In this paper, we propose aspects that need to be monitored to choose proper alignment marks. Holistic Metrology Qualification (HMQ), Ideal overlay/APC parameter signatures are used to determine and validate wafer alignment. HMQ analysis enables us to determine best alignment strategy between multiple strategies/marks based on overlay measurements. Analysis includes examining wafer to wafer OPO variation which is key indicator for alignment robustness. Varying overlay parameters within lot would indicate either huge process instability (which rarely is the case) or alignment mark signal instability. It is possible that alignment marks depending on their segmentation can be very differently impacted with the process. Ideal overlay/APC signature stability indicates healthy process and wafer alignment. Having similar APC signatures at corresponding layers would mean that there is no major process or alignment issue. APC overlay feed forward corrections for those layers can be implemented reducing rework and improve yield.

10147-68, Session PSWed

Process of opto-mechanical design and assembly for reflective mirror subsystem of lithographic projection lens

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Considering the system performance of the projection lens, not only surface quality of the optics shall be concerned, misalignment between each optics and the wavefront distortion contributed by the mounting stress and gravity are also the factors degraded the optical performance. This article introduces the opto-mechanical design and stress-free assembly process of the reflective mirror subsystem with 300 mm in outer diameter of an I-line lithographic projection lens.

The flexure with mounting position pass through the center gravity of the mirror can be adopted as supporting mechanism to prevent the gravity distortion. The distortion due to temperature difference can be avoided by adopting CLERACREAM®-Z glass ceramic and INVAR for material of reflective mirror and supporting flexure respectively. The adjustment mechanism of the mirror subsystem integrates the concepts of Kinematic and exact constraint to provide six degrees of freedom (6DoF) of posture adjustment of the mirror. Furthermore, the assembly process of the flexure which minimizes the mounting stress on the mirror is presented.

In the end of this article, interferometric performance test of the reflective mirror after opto-mechanical assembly compared with the measurement result in manufacturing stage is also presented. With the proposed opto-mechanical design and stress-free mounting process of the mirror, the surface distortion contributed by the amount of mounting stress and gravity effect is less than P-V 0.02 wave @632.8 nm.

10147-69, Session PSWed

Efficient hybrid sub-resolution assist feature insertion flow for contact hole

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Contact layer is known as the most critical layer at 45 nm node or below due to the limited DOF caused by hyper NA illumination. Sub-Resolution Assist Feature (SRAF) application is one of the most common and powerful technique to improve process window. In recent years, model based approach using Inverse Lithography Technology (ILT) already shows its ability to optimize location and size of the SRAF. The performance also comes with drawbacks such as high resource requirement and usually takes much longer computational runtime compared to rule based approach. The shortcoming makes it an infeasible approach for full-chip and mass production. In this paper, a model assisted rule based SRAF insertion flow is demonstrated with simulation and wafer result which shows comparable performance with model based approach without impacting runtime. This hybrid flow includes two steps:

In the first step, a comprehensive SRAF rule is formed by extracting that from model based algorithm. The main rule was obtained by studying of pitch and dimension of SRAF generated by model based approach at a single contact. For a layout consisted by multiple contacts, SRAF was inserted simply by stacking of SRAF of each individual contact hole. Sub-rules were also established which define operations include exclusion, merge and separation for SRAF conflict with each other.

In the second step, rule generated SRAF in the previous step is modified by model based printing fix function during OPC process to prevent it from printing. A physical model is utilized to check the printability of SRAF. Prior to this work, printing threshold was determined by judging SEM image of evaluated contacts. Several types of test-patterns were designed and inspected carefully to make determination of margin between print and not print. For the threshold calculation, 10% of exposure dose is also taken in account to ensure the window of exposure latitude is sufficient.

In our examples on 40 nm design, hybrid and model based SRAF were compared. The result illustrates that most “location” and “size” of the SRAF generated by the two approach were similar, which means the behavior of model based SRAF generation could be accurately caught by the simple rule at most contact patterns. SRAF performance is too evaluated by comparing simulation and wafer-data between the two approaches. In order to confirm the feasibility of this hybrid flow for full chip production, TAT of the each flow is presented for layouts with various sizes. From all the observation of this work, we conclude that model based approach could be greatly simplified by the hybrid flow and make it an efficient method to insert SRAF for contact layer.

10147-70, Session PSWed

Advanced application of pattern-aware OPC

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For advanced technology nodes, it’s critical to address yield issues caused by process specific layout patterns with limited process window. RETs such as Model-Based Sub-Resolution Assist Feature (MB-SRAF) are introduced to guarantee high lithographic margin, but these techniques come with long runtime, especially when applied full-chip. There’s also lack of integrated solution to easily identify, define comprehensive patterns and apply different controls and/or constraints over these patterns through different stages of OPC/RET process.

In this paper, we introduce a flow that applies advanced RET such as MBSRAF or specific local corrections to layouts with critical and yield

limiting patterns. We also introduce in-process pattern match based on Cadence topological Squish pattern. Overall, this new flow of Pattern-Aware OPC (PA-OPC) achieves better margin for hotspots, without sacrificing turnaround time and is able to handle more complex patterns and environment than traditional methods. We demonstrate the benefit of the new flow with fine-grained process window control over different patterns.

10147-71, Session PSWed

Assessment of light source bandwidth impacts on image contrast enhancement using process window discovery

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The performance requirements of advanced semiconductor technology nodes necessitate the use of complex processing methods that push patterning beyond the physical limits of DUV immersion lithography (ArFi). Specifically, aggressive process window (PW) and yield specifications put tight requirements on scanner imaging performance.

In this study, the light source E95 bandwidth impact on Metal layer features from an imec 10 nm node (N10) logic-type test vehicle was investigated using KLA-Tencor's fixed focus offset conditions and Process window Discovery (PWD) methodology [1]. These PWD findings supplement the traditional analysis methods reported previously [2-3] and provide more detail on where the process window truly lies as a function of E95 bandwidth. The results will demonstrate how PWD results can assist in the identification of effects of E95 bandwidth on non-obvious lithographic features that may limit common process window, and can provide input for the optimal E95 bandwidth that should be used for a process.

10147-72, Session PSWed

Advances in DUV light source sustainability

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All DUV light sources have components that require specific types of gas (i.e. neon, helium, nitrogen) in order to function properly and Cymer continues to address several areas of sustainability within the semiconductor industry. In this paper, efforts to reduce and/or eliminate neon and helium gas consumption will be discussed.

The neon supply crisis in 2015 triggered an intensive effort by the lithography light source suppliers to find ways to minimize the use of neon, a main component in the DUV photolithography light sources. Cymer has delivered a multi-part support program to reduce natural resource usage, decrease overall cost of operation, and ensure that chipmaker's business continuity risk is minimized.

Methods used to minimize the use of neon for 248 nm photolithography are described that offer significant relief from supply constraints and reduction of business continuity risk for chipmakers. The main reason for ongoing neon use in these light sources is to periodically purge the discharge chambers from byproduct build-up and provide a supply of fluorine as it is consumed over time. Improvements in the software algorithms that manage sequencing of gas functions were used to optimize and reduce the overall neon consumption, with the positive side-effect of increasing system availability due to fewer gas management events. Results from extensive testing will compare key stability performance metrics before and after implementation.

In addition, techniques to capture the neon effluent and re-purify it offline or within the semiconductor fabs have been pursued. For example, Cymer has developed a neon recycling system for ArF light sources that resides within the chipmaker's fab. Cymer has partnered with a global gas supplier to develop a system capable of capturing, recycling and delivering >90% of the total neon gas required by multiple ArF light sources through automated operation, including online analysis. The neon recycle system has shown excellent results as demonstrated by a quantitative analysis of facility-supplied gas versus the recycled neon in ArF light source performance.

Similarly, DUV light sources have historically used helium as a purge gas in the critical line narrowing module (LNM) to achieve stable wavelength and bandwidth control. Helium has a low coefficient of index of refraction change vs. temperature relative to nitrogen and provides efficient cooling and purging of critical optics in the LNM. Previous work demonstrated how helium consumption can be reduced and still achieves stable performance under all operating conditions1. In this paper, results of eliminating the use of helium will be described. Test results using nitrogen in a helium-compatible LNM show that some light source specifications are not met under certain operating conditions. Higher thermal load conditions lead to thermal lensing near the optics, as nitrogen's index of refraction experiences a significant change with temperature compared to helium. As such, redesigned LNMs that allow for optimal nitrogen flow have been developed and tested. Initial factory data shows that, using these redesigned LNMs, nitrogen is a viable substitute for helium.

10147-74, Session PSWed

Study of aging behaviour on 193nm phase-shift masks

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Chrome migration or aging phenomenon is known for 193nm binary photomasks since a few years. 193nm irradiations and time generate an oxide growth on chrome sidewalls and then cause a non-uniform increase of critical dimensions (CD). If not prevented or detected early enough, wafer fabs are likely to face process drifts, defectivity issues and even lower yield on wafers in the worst cases. Fortunately, some solutions have been put in place in the industry. A standard cleaning and repel service at the maskshop has been demonstrated as efficient to remove the grown materials and get the mask CD back on target. Some detection methods have been already described in literature, such as wafer CD intrafield monitoring (ACLV), giving reliable results but also consuming additional SEM time with less precision than direct reticle measurement. Another approach is to monitor the CD uniformity directly on the photomask, concurrently with defect inspection for regular requalification to production for wafer fabs. This enables ultimately to trigger the preventive cleanings rather than on predefined thresholds.

However, may the 193nm Phase Shift Masks (PSM) be impacted too? In other words, should wafer fabs pay attention to this form of aging? Indeed, some publications report a growth of SiO2, leading to the development of a high duration MoSi (modification of MoSi composition). This study will characterize the aging behavior on a 193nm PSM contact hole layer, 40nm logic technology node.

During this study, the aging phenomenon has been accelerated with the use of a test bench, to reach a CD increase up to 11nm after a cumulated exposure dose of 10kJ/cm? (equivalent to exposures of >32,000 wafers 300mm). Two dice were compared, one kept as reference without any exposure, whereas the other die was aged on the accelerated test bench. Exhaustive characterization has been performed, with CD measurements on the mask and on wafers, evaluation of lithography process windows for usual patterns and most critical features (Optical Proximity Correction

hotspots). It appears that despite a consistent CD increase on the mask, the impact on wafer can be neglected, at least at this amount of exposures. Aerial CD were also analyzed through a Zeiss WLCD to enable a prediction of wafer impact.

An advanced inspection tool (KLA-Tencor X5.2 model) has been challenged as an inline monitoring method to detect the aging degradation on PSM. The Intensity Critical Dimension Uniformity option (iCDU) was firstly developed to provide feed-forward CDU maps for scanners intrafield corrections, from arrayed dense structures on memory masks. Due to layout complexity and differing feature types, CDU monitoring on logic masks used to pose unique challenges.

CDU monitoring on logic masks is now available, the latest Delta-Die and Delta-Time options gives all the needed information, as shown in this paper. In this study, iCDU has demonstrated its ability to catch a slight degradation of CD uniformity.

In the end, this study shows evidences that standard cleanings used in maskshops cannot recover the mask back to its original CD. Finally, Transmission Electron Microscopy (TEM) was used to confirm the chemical nature of the grown material on sidewalls. TEM cuts provide a comparison between a production mask (aging over many years in production) and the test mask (accelerated aging on a test bench).

10147-75, Session PSWed

Image acquisition and motion positioning system design based on the projection lens wavefront aberration measurement

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Projection lens is an important part of the lithography. The wave aberration is the key index, which directly affects the critical dimension. The main methods of wavefront aberration detection are shear interferometry, Shack- Hartmann diffraction interferometry method and point diffraction interferometry. One shearing interference method can realize the nanometer precision. This method needs high precise motion positioning and high signal-to-noise ratio of image acquisition system. a kind of image acquisition and motor positioning control system based on shear interference was designed and realized the high precision motion position of shear grating and shearing interference fringes of synchronization acquisition. a method of improving the shearing interference image imaging quality was proposed to improve the detection precision of the wave aberration, the simulation and experiment show that wave aberration precision can reach 10 nm; At the same time, through optimizing software algorithm, greatly improve the detection time and work efficiency.

10147-76, Session PSWed

Photolithography stepper defocus reduction using in-tool ionizer

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Particle hot spot defocus is a high occurrence event or defect in Photolithography manufacturing process. Defocus on pattern can cause yield lost and increase ppm of field failure due to marginal distorted pattern. Stepper manufacturer design is not effective in removing the charge from a wafer inside the equipment, especially wafer backside with an insulating oxide layer. Electrical field that the charge creates will continue to attract any charged particle having an opposite polarity during contacted or gripped, and brought to wafer holder during step-and-repeat exposure process, which can cause defocus during wafer exposure, and affecting subsequent wafers if the particle is not removed from wafer holder.

In this paper, particle causing hot spot defocus in Photolithography process is studied; a new in-tool ionizer is experimented and installed inside the equipment, which significantly reduce the occurrence of particle hot spot defocus over a period of time. Design and experimental result of the ionizer is discussed. Using the in-tool ionizer on all otherequipments shows a significant reduction of particle defocus overall.

10147-77, Session PSWed

Stepper lens heading control for semiconductor manufacturing

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I-line Stepper which is using UV light as the light source is used in semiconductor fabrication process, where productivity is crucial for today's semiconductor manufacturing. During wafer step-and-repeat exposure process, Stepper lens is heated up by UV light inevitably. Stepper tool manufacturer has built-in various lens and chamber environment control systems to respond and correct the heated lens, in order to allow continuity on wafer patterning process. Lens heating will cause focus drift and image distortion, especially for high transmission reticle where lens heating rate is much faster due to large area of exposure. Affected material will result in bad Critical Dimension and Overlay, which leads to low yield and increased ppm.

In this paper, i-line Stepper lens heating is studied and solutions are discussed. More importantly, a new Stepper lens heating control method using Stepper chamber pressure monitoring is demonstrated. As a result, the manufacturing process is more effective with higher productivity.

10147-78, Session PSWed

Automated stepper recipe creation system for operation efficiency improvement and error reduction

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Photolithography imaging tools used in semiconductor fabrication requires substantial amount of unique recipes to allow transfer of designed patterns onto the wafer during exposure. Every reticle from any mask-set of a newproduct will require a specific recipe for this purpose. The recipes creation process is a lengthy and time consuming feat as it involves significant amount of precise manualdata entryinto the tool process parameter for every single recipe besides manual data preparation prior to recipe creation. A single product with 25 photo layers typically requires 8-10 man-hours to complete including the tedious recipes auditing (checking). For a semiconductor foundry with more than 500 new reticles tape-outs per month, new recipes creation will compel substantial amount of workload and deplete man-hours significantly and the probability of inadvertent human errors also increases with the number of new recipes. This paper will introduce an automated photolithography imaging tools (steppers and scanners) recipe creation system that shortens the data preparation and recipe creation time. It has been demonstrated that recipe creation and audit time has improved by more than 97% with the introduction of automated recipe creation system. More importantly, the automated system has achieved 100% recipe standardization on critical process parameters. The automated system has also accomplished a remarkable 0ppm misprocess related scrap due to wrong recipe setup and lowered photo rework rateever since the implementation of the automated recipe creation system.

10147-32, Session 9

Exposure source error and model source error impact on optical proximity correction

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Initial studies have quantified the impact of source error on wafer CDs in the presence of OPC. The studies have found that when a 100% emitting source error is introduced into the OPC model, the corrected mask is minimally impacted through process when small errors are introduced on the source. However, as slightly larger errors are placed on the source used in the OPC mode, catastrophic failures are found. When the same errors are introduced to the exposure source when the mask is corrected with a perfect source, there is a significant through process CD variation in the system but there are no clearly catastrophic failures.

This study will continue beyond the initial work to better understand the interaction between source errors and OPC. In this case partial transmission and zero transmission errors will be introduced into the study. The initial study found a CD bias and extra CD variation when the error was located in the transmissive area for the source error case. These effects are thought to be due to scattered background illumination and pattern shift respectively. These effects were not as readily observed in the mask error case. This study will look at the interaction of different error in the source during both exposure and OPC generation to better understand the effects of source errors on the final pattern.

A resulting analysis of study will be presented. The analysis should explain if scattered background illumination and pattern shift are the mechanisms of the source effects. This can be concluded if the same effects can be generated in the mask error case using various source errors. The software methodology used to execute these studies will also be presented in detail.

10147-33, Session 9

Effective use of aerial image metrology for calibration of OPC models

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The appropriate representation of the photomask in the simulation of wafer lithography processes has been shown to be of vital importance for 14-nm and below1. This task is difficult, however since accurate optical metrology and physical metrology of the three-dimensional mask structure is not always available. OPC models for wafer patterning comprise representations of the mask, the optics, and the photoresist process. The traditional calibration of these models has involved empirical tuning of model parameters to CD-SEM data from printed photoresist patterns. Such a flow necessarily convolves the resist effects and it has been difficult to reliably obtain mask and optical parameters which are most representative of physical reality due to aliasing effects. In this work, we have undertaken to decouple the mask model from the photoresist process by use of the ZEISS Wafer-Level CD (WLCD) tool based upon aerial image metrology. By measuring the OPC test pattern mask with WLCD, the mask parameters in the OPC model can be tuned directly without interference of resist effects. This work utilized a 10-nm node metal mask, and we will demonstrate that the use of such a flow leads to the most predictive overall OPC models, and that the mask parameters resulting from this flow more closely match the expected physical values. More specifically, the mask corner rounding, sidewall angle, and bias values were tuned to the WLCD data instead of the wafer CD SEM data, and resulted in improved predictive capability of the model. Furthermore, other mask variables not traditionally tuned can be verified or tuned by matching simulation to aerial image metrology.

10147-34, Session 9

Accurate characterization of 2D etch bias by capturing surrounding effects from resist and trench areas

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The extension of optical lithography to 7 nm node and beyond relies heavily on multiple litho-etch patterning technologies. The etch processes in multiple patterning often require progressively large bias differences between litho and etch as the target features become smaller. Moreover, since this litho-etch bias has strong pattern dependency, it must be taken into consideration during the Optical Proximity Correction (OPC) processes. Traditionally, two approaches are used to compensate etch biases: rule-based retargeting and model-based retargeting. The rule-based approach has a turn-around-time advantage but now has challenges meeting the increasingly tighter critical dimension (CD) requirements using a reasonable etch-bias table, especially for complex 2D patterns. Alternatively, model-based retargeting can meet these CD requirements by capturing the etch process physics with high accuracy, including the etch bias variability that arises from both patterning proximity effects and etch chamber non-uniformity.

This paper's work will focus on the etch bias variability due to patterning proximity effects. It assumes that an After-Development-Inspection (ADI) model has been well calibrated and the subsequent etch model is based on the ADI model contour. In the past, image processing with low-pass filters has been used to approximate the etch effects in pattern areas. In this work, such approximations are replaced in favor of strict geometric methods to capture the effects of neighboring pattern areas. To assess the etch bias for a specific point on the ADI contour, we compute the total areas of surrounding resist and trench regions that can contribute to these etch proximity effects. The local resist area is defined as the resist region enclosed by the resist-trench interfaces surrounding the ADI point (white in Figure), while the local trench area is defined as the trench region enclosed by these interfaces (red in Figure). Ambit parameters are used to define the required area used in the model. The correlation between these areas and the etch bias values gives rise to a mathematical form within the etch model that can be used for OPC applications. A set of wafer data is used to explore and calibrate this etch model. It is known that etch bias behavior for simple pitch patterns can be well described with the resist widths and trench widths alone, so we first build the etch bias correlation with resist/trench areas for a certain number of pitch patterns. The correlation is then applied to 2D patterns. It is found that by tuning the ambit parameters, a similar etch correlation to the pitch structures can be found for complex 2D patterns. Based on the whole wafer dataset, we found that the accuracy of such an etch model form is improved over traditional image-based models.

10147-35, Session 9

Design grid optimization for OPC of silicon photonics

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The layout design for silicon photonics can be complicated and usually have edges with arbitrary angles. The critical dimension can be less than 100 nm, requiring the layouts to be OPCed in order to have large enough process windows for high volume manufacturing. However, the well-established CMOS-orientated IC industry OPC tools for advanced nodes can only handle Manhattan designs in which the Manhattan style polygons with edges of 0°, 90° or 45° to the reference direction. Silicon photonics layouts need to be

discretized in order to use the existing OPC tools. From optical performance point of view, the design grid is expected to be as small as possible and it is usually from 1 nm to 5 nm. However, the design grid has never been optimized based on the OPC performance.

In this paper, we demonstrate the impacts of design grid on the OPC performance. Design grid for silicon photonics is not always the smaller the better anymore. Our study shows that small 2D designs require large design grids while smooth curves with large radius require small design grids.

We proposed a novel design-based discretization algorithm to convert a non-Manhattan style layout to an OPC-friendly Manhattan style layout. Simulation results show that the pattern fidelity is optimized for both small 2D patterns and smooth curves.

10147-36, Session 9

Si-photonics waveguides manufacturability using advanced RET solutions

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Si-Photonics is the technology in which data is transferred by photons (i. e. light). On a Photonic Integrated Circuit (PIC), light is processed and routed on a chip by means of optical waveguides. The Si-Photonics waveguides functionality is determined by its geometrical design which is commonly curved, skewed and non-manhattan. That is why printing fidelity is very challenging on photonics patterns.

In this paper, we present two different Optical Proximity Correction (OPC) flows for Si-Photonics patterning. The first flow is regular model based OPC and the second one is based on Inverse Lithography Technology (ILT). The first OPC flow needs first to Manhattanize the input layout while the ILT flow does support skewed edges input by tool design and does not need any manhattanization before OPC. We will compare these two flows on various Si-Photonics waveguides from lithography quality, run time and MRC compliance of mask output. We will observe that ILT flow gives the best Edge Placement Error (EPE) and the lowest corrugation along the Si-Photonics waveguides. The ILT flows also takes into account the mask rules so that the generated mask is mask rule check (MRC) compliant. We will also discuss the silicon wafer data where Si-Photonics devices are printed within the two different OPC flows at process window conditions. Finally, for both OPC flows, we will present the total OPC run time which is acceptable in an industrial environment.

10147-37, Session 10

Overlay statistics for multiple exposure patterning measurement, disposition, and feedback

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Multiple exposure patterning is now a main-stream method used in the manufacturing of modern integrated circuits. However, the overlay statistics of these multiple exposure schemes has not been well understood. Splitting levels into multiple exposures (2x, 3x, etc. patterning) has a quantifiable effect on how overlay metrology relates to overlay process assumptions and capability. In addition, overlay metrology strategies involving measuring a current level back to a level exposed with multiple exposures can also misrepresent the true overlay error. In this paper we look statistically at the effect of multiple exposures on:

• OL metrology: Through theoretical and experimental means, we show that grouped overlay metrology of multiple exposures underestimates the true overlay error. This is due to the point-by-point averaging of layers that have been split into multiple exposures. Fortunately, the ratio between metrology and true overlay can be exactly calculated.

• process assumptions and ground-rule calculations: Process assumptions typically take into account the combined population of multi-patterned components. Understanding how these process assumptions relate to the capability of simple single level to single level overlay is desirable. This paper takes a new approach to calculating these relationships by going back to image-placement error and using population statisitics. This is different than former methods discussed in the literature that look at “2nd order” overlay calculations. We show that base process capability needs to be tighter than process assumptions with the specific amount of tightening directly related to the mean shifts between multi-patterned layers. Because of this, mean overlay specifications have to be set appropriately at prior levels to match process assumptions. As an example, if a contact layer is split into two exposures, the mean translation error between the two exposures needs to be minimized for good metal to contact overlay. This paper will describe the exact controls needed based on the new statistical understanding.

KEY RESULTS:

- Through theoretical and experimental means, we show that grouped overlay metrology of multiple exposures underestimates the true overlay error. This is due to the point-by-point averaging of layers that have been split into multiple exposures.

- We show that base process capability needs to be tighter than process assumptions with the specific amount of tightening directly related to the mean shifts between multi-patterned layers.

- As an example, if a contact layer is split into two exposures, the mean translation error between the two exposures needs to be minimized for good metal to contact overlay.

KEY CONCLUSIONS:

- The ratio between metrology and true overlay can be exactly calculated for a layer measuring back to a prior level patterned with multiple exposure.

- Mean overlay specifications have to be set appropriately at prior levels to enable process assumptions to be met.

- Former methods discussed in the literature that look at “2nd order” overlay calculations and RSS errors are not appropriate for estimating OL error between a current layer and a prior layer exposed with multiple exposure. Instead, this paper describes a new and statistically correct approach to calculating these relationships by going back to image-placement error and using population statistics.

10147-38, Session 10

Experimental verification of on-product overlay improvement by intra-lot overlay control using metrology based grouping

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For the sub-20 nm DRAM nodes, wafer-to-wafer (W2W) variation is one of the major contributors to on-product overlay (OPO). One way to reduce the W2W variation is by applying overlay corrections on wafer level on top of per lot / per chuck corrections. These overlay corrections are typically based on prior measurements of the OPO on the wafers in question. Measuring OPO on every wafer is not preferred due to the resulting metrology cost increase. Hence, wafers are typically assigned to a limited amount of groups, which are in turn assigned one common correction set for all the wafers within a particular group. The common corrections are obtained from measuring a limited amount of wafers from the respective groups.

In previous investigations, this wafer grouping was deduced from the processing context (e.g. etch chamber, CMP pad, etc.) [1]. However, in a high-volume manufacturing (HVM) situation, this approach is less suited

due to the complex processing infrastructure and the need for profound knowledge on the impact of wafer processing on the overlay fingerprint variation.

In this paper, we present results obtained from a different approach, where the wafer grouping is deduced from metrology data that is available prior to the exposure of the lot. Aim of this approach is to balance overlay control and OPO metrology effort. For this purpose, software tooling was provided and utilized in order to execute the necessary mathematical operations and output the results obtained from these operations. We experimentally demonstrated the benefit of our approach on one of the critical layers of a sub-20 nm DRAM product of SK hynix. The experiment was executed in a rework scenario, which involves exposing and measuring OPO on selected send-ahead (SAHD) wafers, their subsequent rework, and re-exposure of the full lot using per-group corrections. While the grouping in this particular case was determined based on wafer shape measurements [2], the per group corrections were determined from the OPO measurements of the aforementioned SAHD wafers and subsequently applied to the full lot (including the reworked SAHD wafers) on a NXT-1970 scanner [3, 4]. (The corrections were applied via a newly available interface allowing per wafer corrections to be applied to a lot).

The obtained results show a considerable reduction of OPO by 28% and a reduction of W2W variation by 45%. Simulations performed on additional lots and for 3 additional layers confirm the validity of our results.

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10147-39, Session 10

Scanner overlay matching: monitoring and control for 14nm and beyond production in HVM fab

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Overlay matching and control across various tools is a constantly evolving task in high volume manufacturing (HVM) fabs. Current nodes require overlay specifications as small as 3.5nm (1). In this paper we explore overlay contributions remaining after tool to tool matching to the same reference. Multiple contributors are investigated including reticle alignment methods, varying wafer clamping fingerprints across tools and illumination source difference in the control mechanisms between tool control and production.

In a HVM fab, the overlay component of tool matching cannot be fully controlled through automated process corrections (APC), overlay sampling and model correction without residual uncorrected tool to tool mismatching. The purpose of this study is to estimate the overlay penalty on product, by using "product like" test wafers (2). Production lots are processed utilizing multiple Scanner types, for example, PARIS and TIS reticle alignment tools which can result in an overlay delta. An analysis is done to determine the overlay effects of these alignment differences. Variations in wafer clamping fingerprints are observed across all scanners, we propose in this paper different detection methodologies including residual alignment fingerprint monitoring and analysis of on tool qualification wafers. We explore tool to tool as well as time to time delta matching on tool qualification wafers. These monitors provide the frame work to trigger necessary Scanner set-up prior to production impact. We also discuss potential solutions such as BMMO control. Lastly, tool matching using baseliner is generally run using a single illumination setting while production wafers are exposed utilizing multiple, this paper examines the potential overlay impact from this difference. In order to optimize on product overlay (OPO) through production sampling and APC model it is essential to first understand and monitor the varying overlay contributors post tool matching

10147-40, Session 10

FinFET-induced anisotropy in printing of implantation shapes

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In advanced technological nodes, the photoresist absorbs light, which is reflected by underlying topography during optical lithography of implantation layers. Bottom anti-reflective coating (BARC) helps to suppress the reflections, but BARC removal may damage transistors, not to mention its relatively high cost. Therefore BARC is usually not used, and topography modeling becomes obligatory for printing implantation shapes on target. Furthermore, presence of Fin Field Effect Transistors (FinFET) makes modeling of non-uniform substrate reflections exceptionally challenging.

In real designs, the same implantation shape may be found in a vertical or in a rotated horizontal orientation. This creates two types of relationships between the critical dimension (CD) and FinFET, namely parallel to and perpendicular to the fins. The measurement data shows that CDs differ between these two orientations. It is unexpected as the fin periodicity and size are well below the resolution limit of a 248 nm DUV scanner.

We developed a Rigorous Optical Topography simulator that has been applied to analyze this effect in order to reveal physical reasons for this difference. Numerical experiments show that the shape orientation may introduce CD differences of up to 45 nm with a 248 nm illumination for 14 nm technology. These differences are highly dependent on the enclosure (distance between implant shape and active area). We discovered the major cause of the differences: in the parallel orientation the shape is facing solid sidewalls of the fins, while the perpendicular oriented shape "sees" perforated sidewalls of the fin structure, which reflect much less energy.

Meticulously stated numerical experiments helped us to thoroughly understand anisotropic behavior of CD measurements. This allowed us to more accurately account for FinFET-related topography effects in the compact implantation model for optical proximity corrections (OPC).

10147-41, Session 11

On-product overlay improvement with an enhanced alignment system

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The final lithography accuracy is determined by what is known as the "on-product" performance, which includes product wafer-related errors and long-term stability. It is evident that on-product performance improvement is absolutely imperative now, and will become even more crucial in coming years. Today, the cutting-edge Nikon NSR-S631E immersion lithography

scanner is demonstrating high performance at a number of manufacturing facilities worldwide. In order to meet customers' future requirements, Nikon has developed the next-generation lithography system focusing on wafer alignment advancements to improve on-product performance.

3D NAND is being commercially mass produced by multiple companies. 3D NAND technology incorporates the basic concepts that production capacity of dies is increased by vertical stacking, so the number of layer stacks will continue to increase at a rapid rate. Therefore, wafer grid error caused by film stress is greater and mark shape error by CMP planarization process is larger. Wafer warpage including convex, concave and saddle shape signatures are increased, which drives wafer grid error. Our next challenge is on-product overlay improvement utilizing accurate wafer grid modeling. In order to balance high precision and optimal productivity, Nikon has developed a next-generation wafer alignment system.

Accurate stage motion and high precision wafer measurement are key technologies for on-product overlay improvement. Precise stage position measurement and excellent hardware mechanics, as well as an advanced control system are needed to ensure accurate stage motion. In addition, high precision alignment mark measurement and accurate wafer grid modeling are also necessary for accurate wafer measurement. Accurate wafer grid modeling becomes a central focus for these factors. Wafer alignment using linear grid fitting is not sufficient for process wafers having non-linear distortion, so Nikon emphasized improvement of high order wafer grid measurement and modeling. Various wafer processes (for example, thermal oxidization, annealing, etching, ion doping and CMP process) cause non-linear grid distortion. Wafer grid varies not only layer by layer and lot by lot, but also wafer by wafer. Therefore, the enhanced wafer alignment system needs real-time measurement of grid changes between wafers.

This newly developed wafer alignment system will help customers achieve their aggressive next-generation manufacturing accuracy and productivity requirements. In this presentation, we will introduce the details of the new wafer measurement system and provide supporting performance data.

10147-42, Session 11

Reticle heating feed-forward control (RHC2) on NXT:1980Di immersion scanner for enhanced on-product overlay

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Scanners in High-Volume-Manufacturing conditions will experience a large range of reticles that vary in reticle transmission and reticle diffraction characteristics. Especially under full production loads reticles will heat up due to the exposure light-load and experience thermo-mechanical deformations. The resulting reticle pattern distortion can be partially translated in a deteriorated overall system overlay.

Due to the geometry of the reticle and exposure fields, these reticle thermal effects are in general barrel-shape distortions that can be well corrected with the available set of lens manipulators. Nevertheless node-over-node the residual overlay errors associated with thermo-mechanical reticle deformation needs further reduction since it contributes to the total on-product overlay performance. To reduce overlay caused by reticle temperature drift, NXT:1980Di includes an active cooling mechanism suppressing the reticle temperature changes during exposure significantly. Even though the reticle temperature excursions are well suppressed, residual intra-wafer overlay drift effect can still be observed.

Before exposure of a wafer, reticle deformation is measured by reticle align using in-line alignment / image sensors (TIS or PARIS). This is enabled by adding more alignment markers around the circumference of the image field on the reticle. The measured reticle deformations are then fed to the system control network and dynamically corrected for by making use of the available manipulators in the scanner and the projection lens. Wafer-by-wafer reticle distortion measurements are performed to accurately capture the transient dynamics present in reticle heating during normal production lots. A new version of Reticle Heating Feed-forward Control (RHC2) is introduced that uses reticle-heating-induced deformation measurements over time and exposure sequence information to calibrate reticle-deformation-prediction-models. These models are based on thermo-mechanical models that emulate reticle deformation under various exposure conditions and are applied in-line to the exposures to reduce intra-wafer overlay drift effects.

In this paper we report on the latest reticle heating control strategies and present distortion and overlay performance under high thermal load conditions.

10147-43, Session 11

Next-generation DUV light source technologies for 10 and 7nm nodes

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Multi-patterning techniques with ArF immersion lithography continue to be extended into the 10 and 7 nm nodes. With increasingly challenging process control requirements (CD, Overlay, Edge Placement Error), the lithography and patterning tools need to find ways to minimize variation and maintain process margin to achieve high yields. This paper will describe new advances in light source technologies that can regain imaging margins by optimizing light source bandwidth settings in concert with OPC retargeting to take advantage of the contrast improvements afforded by lower bandwidth. In addition to simulation studies reported previously, on-wafer measurements were collected showing the progressive improvements gained with lowering bandwidth on an existing mask as well as reoptimizing a mask to leverage this lower bandwidth setting. To fully leverage this capability, further improvements in bandwidth stability are going to be featured on a new ArF light source along with an integrated solution that allows the bandwidth target to be commanded by scanner recipe. This will allow lithographers to optimize layers that need further improvements in patterning by using lower bandwidth while continuing to run existing layers with standard, 300 fm bandwidth targets. With the introduction of a new DUV light source, this paper will also describe improvements that continue to reduce running costs in an effort to counteract the escalating costs of multi-patterning lithography.

10147-44, Session 11

The ArF laser for the next-generation multiple-patterning immersion lithography supporting green operations and leading edge processes

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Multiple patterning ArF immersion lithography has been expected as the promising technology to meet tighter leading edge device requirements. The most important features of the next generation lasers are the reduction of operational costs, the prevention against rare resource shortage to support green operations and the improvement of device yield in multiple-patterning lithography. The short supply of rare gases used in laser operations is becoming a critical issue for high volume manufacturing (HVM). In basic laser capabilities, lower E95 bandwidth enhances image contrast and tighter E95 bandwidth stability is the key to improve larger focus budgets for a leading edge processes. The new ArF excimer laser, GT64A has been developed to meet the needs such as the reduction of rare resource usage and device yield enhancement.

The unique property of rare gases such as neon and helium has caused a

crisis of global supply and inflation. The semiconductor industry has recently experienced severe shortage of these gases. Neon accounts for more than 96% of excimer gas for discharge in ArF excimer lasers. The sophisticated gas control algorithm has already succeeded to reduce by 50% of neon gas usage. The new developing neon gas recycling system will further enable to refine pure neon gases of 50% from the exhausted gas, which continuously discarded to remove impurities generated during the electrical discharge, without the impact on laser performance. Helium has been employed to purge within the line narrowing module (LNM) due to the low refractive index variation with temperature rises in laser shooting. Helium purging in LNM enables lower E95 bandwidth than that with the purge of nitrogen whose refractive index variation is approximately ten times more sensitive to temperature rises than that of helium. A new designed LNM enables to achieve lower E95 bandwidth than that with helium purge, even with nitrogen purge. These eco-technologies strongly support green operations and the reduction of operation costs in chipmakers.

The new LNM further makes it possible to be E95 bandwidth of 0.20pm, even with full duty cycle operations and nitrogen purge. The large improvement is accomplished by the ingenious design, which enables heat effect in laser shooting at optical elements and mechanical components to be lower. This will improve image contrast and enhance exposure latitude. E95 bandwidth is controlled by adjusting the wavefront of a laser beam using a movable lens with optical system within a resonator. A high speed actuator equipped the movable lens enables E95 bandwidth stability to be less variation. The improvement in spectral bandwidth stability contributes to the further reduction of CD variation. These new technologies on E95 bandwidth will be effective to enhance yield.

These optional functions in GT64A offer lower operational costs and higher device yield for chipmakers. In the presentation, the latest development status on GT64A will be discussed.

10147-45, Session 11

Layout independent levelling (LIL) on NXT:1980Di immersion scanner for enhanced productivity

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ASML's 300mm scanner-systems build on the TWINSCAN (XT/NXT) platform and yield high productivity levels for dry as well as immersion litho-scanners. NXT:1980Di immersion scanners yields productivity levels as high as 275wph while maintaining the overlay accuracy. The TWINSCAN scanner concept uses a double stage, where the wafer alignment and levelling metrology is performed in parallel to the wafer exposures. Under normal High-Volume-Manufacturing operation the system design for the measure and expose sequences is balanced and about equal time is spend for wafers during the expose and measure cycles.

In case customer layers demand a large number of alignment scans, the measure sequence can become limiting for the net productivity of the scanner tool. A reduction of scanner measure actions is hence required to support optimal productivity.

The NXT:1980Di can be equipped with a new levelling mode that results in a significant reduction of the time that is spent on measuring the wafer focus height map. Current leveling strategies have been designed to follow the layout of the exposure layouts/field, resulting in additional levelling scans (@ measure side) for layouts with reduced X-field dimensions.

In the new levelling mode the focus height map is measured employing the full width of the level sensor and thereby minimizing the number of levelling scans. Furthermore the levelling measurement actions have become independent of the customer field layout. This mode of Layout Independent Levelling (LIL) enables a reduction of leveling time resulting in additional productivity for measure cycle limited exposure jobs, or can be employed to enhance the number of alignment scans for jobs that are exposure limited, potentially yielding better alignment and subsequent better overlay. In this paper we describe the implementation of the LIL-method in the TWINSCAN platform design. We will report on the focus / levelling performance for both test as well as customer product wafers, and will present a productivity outlook on the performance gain for a selected set of exposure use-cases.

10147-46, Session 12

Immersion lithography scanner resolution performance demonstration on 450mm substrates

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The Global 450mm Consortium (G450C) located at the SUNY Poly campus in Albany NY is now in its 5th year of developing and evaluating manufacturing 450mm tool sets. The charter for G450C is to partner with equipment manufacturers and develop a 450mm high volume manufacturing (HVM) equipment set. The G450C lithography department received the only linked lithography cell in the world in 2015. This cluster includes a Nikon NSR-S650D 193nm immersion scanner and a SCREEN DT-4000 Sokudo DUO track. The lithography link completed the acceptance testing in Q4 2015 and was released for wafer process development. This paper focuses on how the lithography cell resolution performance has progressed from tool acceptance to current day. We will determine the maturity of the equipment in regards to the technology requirement for ten nanometer and seven nanometer node (N10 and N7). Initial data will be shown, as well as the iterative and final data following process and equipment improvements that have been implemented.

With multi-patterning being the primary driver for resolution enhancement in today's HVM factories Critical Dimension Uniformity (CDU) is one of the key indicators when evaluating Edge Placement Error (EPE), the cumulative sum of all error in the lithography process. We will demonstrate both line/space and contact hole CDU performance as well as process window performance using multiple masks and resist processes. The CDU performance shows significant improvement after three main factors were implemented: these factors are carefully selected photoresist, track process optimization and Nikon Litho Turnkey Solution CDU Master application. We will also demonstrate process window improvements and provide comparison between resists and masks. The 450mm photoresists are specially formulated to meet the thickness and spin requirements of 450mm processing. It will be demonstrated that with the implementation of optimized photoresist, PEB tuning, and CDU Master correction that CDU results of <1nm 3? may be able to be achieved on 450mm wafers. The final 450mm CDU results for contact hole and line/space patterns will be compared to 300mm production tools as well as the N7 and N10 expected requirements.

Besides traditional Alternating Phase Shifting Mask (APSM), G450C litho also utilizes thin Opaque MolySi On Glass Mask (OMOG). Process window comparisons will be evaluated on both mask technologies for all of the resist processes. The strengths and weaknesses of each process will be highlighted using 450mm substrates.

At last, combining photoresist selection and OMOG mask lessons learned, the G450C lithography department has developed a process in preparation for a new HVM style test mask set. In addition to our OMOG and APSM test masks G450C is currently designing a three layer mask set and with the availability of this mask we plan to gather "on product" CDU performance on a Back End Of Line (BEOL) metal stack. This mask set will have resist-

based OPC modeling based on the resolution data collected in these experiments. Nikon will also provide source optimization models to further improve the across wafer CDU performance on this test mask set.

10147-47, Session 12

Computational scanner wafer mark alignment

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In the process nodes of 10nm and below, the patterning complexity, along with the processing and materials required, has resulted in a need to optimize wafer alignment mark simulation capabilities in order to achieve the required precision and accuracy of wafer alignment performance.

In this paper, building on earlier results, we will introduce functionality to co-optimize the alignment marks and recipes for improved performance and robustness.

ASML's Design for Control (D4C) application for wafer alignment mark design has been extended to support computation prediction of alignment mark performance for the latest alignment sensor on the Twinscan NXT:1980Di platform and beyond. New simulation functionality will also be introduced which will enable aberration sensitivity matching between the alignment mark and the device cell, the design of more robust alignment marks, and extend simulation capabilities for the design of wafer alignment capture marks and the recommendation of alignment recipe settings.

Wafer alignment contributes to on-product overlay performance. Wafer alignment mark performance can be influenced by process asymmetries or optically absorbing layers (detectability). Both of these effects can be improved by selecting an optimal wafer alignment mark for a given product layer. Figure 1 shows how overlay performance as seen on a YieldStar (YS) can be influenced by wafer alignment mark choice based on the measured mark performance. Wafer alignment contribution to overlay wafer to wafer variation (W2W) has been evaluated on YieldStar overlay measurements by selecting different wafer alignment marks for wafer alignment where smaller wafer to wafer variation number indicates smaller contribution to overall overlay performance. This performance correlates with difference in readings between alignment sensor colors (color to color) that is also D4C-Alignment Key Performance Indicator (KPI). Figure 1 also shows that the strength of the alignment mark signal, or so called wafer quality (WQ) does not have a direct correlation with overlay performance.

Figure 2 shows that computationally predicted wafer alignment mark performance correlate to overlay measurements. Therefore a D4C-Alignment computational solution for wafer alignment mark design can be used to improve the overlay performance. Figure 2 shows the D4C-Alignment simulated Key Performance Indicator (KPI), which estimates the difference between readings for different alignment sensor colors and can be used to improve on-product overlay by selecting proper wafer alignment mark. Overlay was estimated on measurements done on YieldStar (YS), evaluating the use of different alignment marks. For each mark, the D4C-Alignment Key Performance Indicator (KPI) was calculated and then the value of this KPI was plotted against the impact of potential use of the mark for wafer alignment. The measured overlay performance after potential use of a mark for wafer alignment correlates to D4C-Alignment prediction which shows that D4C-Alignment can be used to influence overlay performance.

This simulation capability of D4C-Alignment function will be further explored towards applications using latest alignment sensor capabilities as well as new capabilities like aberration sensitivity prediction, mark robustness and mark design for Coarse Wafer Alignment (COWA) capture. New applications will allow use of a computational solution together with latest sensor to improve overall on-product overlay performance further.

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10148-2, Session 1

Low track height standard-cells enable high-placement density and low-BEOL cost in N5 *(Invited Paper)*

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Making standards cells smaller by lowering the cell height from 7.5 tracks to 6 tracks for the same set of ground rules is an efficient way to reduce area for high density digital IP blocks without increasing wafer cost. Denser cells however also imply a higher pin density and possible more routing congestion because of that. In Place and Route phase, this limits the cell density (a.k.a. utilization) that can be reached without design rule violations. This study shows that 6-track cells (192nm high) and smart routing results in up to 60% lower area than 7.5-track cells in N5 technology.

Standard cells have been created for 7.5T and 6T cells in N5 technology (poly pitch 42nm, metal pitch 32nm). The cells use a first horizontal routing layer (Mint) and vertical M1 for 1D intra-cell routing as much as possible.

Place and route was performed on an opencores LDPC decoder. Various cell architectures and place and route optimizations are used to scale down the cell area and improve density. Most are not process optimizations, but optimized cell architectures and routing methods:

• Open M1: M1 is removed as much as possible. This allows the router to use M1 for inter-cell routing in dense areas.

• Routing in Mint: With open M1 the router can also use Mint to extend pins to access nearby free M1 tracks in congested areas.

• Outbound rail: The 7.5T cells have inbound VDD/VSS rails in Mint for easy supply tapping. Moving the Mint rail outbound and shared between cells is required to enable lower track height cells.

• Vertical Power distribution network (PDN): in 6T cells too many horizontal tracks would be consumed by the wide M2 rail. Mint is used instead combined with a vertical PDN in M1.

• Self-Aligned Gate Contact allows to contact the gate on top of active fins. Any Mint track then can contact a gate, reducing cell area considerably.

• Partially landing Mint Via trench: In 6T cells, a continuous Via trench underneath the Mint rail is used. This via partially lands on M0A to relax tip-to-tip requirements.

• Relaxed M2 pitch: When pin access is handled in Mint and M1, this allows for a relaxed M2 pitch (48nm) with cheaper double patterning.

To avoid horizontal routing layer congestion with the smaller cells, the 6T cells depend on the vertical PDN and open M1 to improve routability and pin access. Already in 7.5T cells, open M1 and vertical PDN help to improve routable utilization from 50% with closed M1 to 85% maximum. Moving to 6T cells, the combination of reduced cell area and high 85% utilization of result in a 60% area reduction vs the original 7.5T cells.

We have shown that combining 6-track cells and smart routing results in up to 60% lower area than 7.5-track cells in N5 technology. Open M1 and vertical PDN are main area boosters for any cell architecture, boosting utilization from 50% to 85% already for the 7.5T cells.

10148-3, Session 1

Pattern-based optimization of self-aligned double patterning (SADP)-compliant layout designs for sub-20nm metal routing

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Pattern-based methodologies for optimizing Self-Aligned Double Patterning (SADP)-compliant layout designs are developed based on identifying lithography hotspots and replacing them with pre-characterized, manufacturing-friendly fixing solutions. Self-aligned double patterning is one of the multi-patterning techniques used in volume production for sub-20nm technology nodes. In order to leverage the full benefits of the SADP manufacturing process, drawn layout designs are mapped to SADP-compliant mask layers through line-cut decomposition, a technique that requires the drawn designs to be decomposable into uni-directional, one-dimensional mandrel/non-mandrel features and cut features. Line-cut decomposition introduces a design and manufacturing co-optimization challenge for the routed metal layers. On the design side, the unlimited usage of cut mask features is preferred because cuts reduce the amount of excess metal area and excess parasitic capacitance, which may negatively affect circuit performance, such as timing. Yet, on the manufacturing side, the limited usage of cut mask features is preferred because the printing of contact-like cut masks that are used to form the line ends of dense pitch metal lines pose a significant lithographic challenge.

An automated pattern-based matching and replacement methodology optimizes metal routing and improves cut mask manufacturability. By identifying cut mask topologies in SADP decomposed layout designs and opportunistically replacing them with consistent predetermined fixes on the cut mask, the number of unique cut mask patterns and lithography hotspots are reduced. This proposed methodology requires a topology-based library of lithography hotspots to be built a priori, in which each topology is associated with a predetermined fixing solution. A pattern matching engine then searches for matching topologies from the library in the SADP decomposed layout designs. If a match were found, the engine would replace the existing hotspot with the predetermined fixing solution. These fixings are opportunistic because only the design rule check-clean replacements are preserved. In addition, pattern-based insertions of cut features can be used to remove the excess metal area generated by the rule-based, line-cut decomposition algorithm, thereby mitigating layout-induced circuit performance degradation.

The methodology was demonstrated on a sub-20nm SADP decomposed routed block with an area of 280 x 1800 um2 on the metal 2 layer. The SADP-compliant, rule-based line-cut decomposition algorithm reduced the number of uniquely drawn metal 2 line end patterns by ~60%-70%. The number of unique line end pattern instances was further reduced by ~10-15% through pattern replacement, such that the cut features become more manufacturing-friendly, as demonstrated by a reduction in lithographic simulation hotspots. Conservative, DRC-compliant pattern-based opportunistic insertions of cut features removed ~6-10% of the excess metal area generated by the rule-based, line-cut decomposition algorithm.

10148-4, Session 2

Pattern-based analytics to estimate and track yield risk of designs down to 7nm *(Invited Paper)*

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At advanced technology nodes, physical design verification with patterns is essential to co-optimize design and process for improved yields [1, 2].

Conventional design verification flows restrict the use of known yield-limiting patterns (made available by the foundry). However, a design may also pose some new geometric constructs or patterns which are previously unknown to the foundry.

In order to verify such candidate patterns the test chip program is conventionally leveraged to validate design constructs (patterns) on silicon. Other verification methods such as process model-based simulations are also used.

To evaluate these new patterns for possible addition to verification flows it is important to identify and track them for yield risk.

The methodology to identify and track patterns begins with deconstructing designs into patterns. One of the pattern representations used in this work is shown in Figure 1. Keeping track of the patterns across multiple designs and process technology nodes requires a database [3]. Dynamic analyses are performed over this large database of patterns to reduce the set and define patterns of interest (POI) as shown by the schematic flow in figure 2. Such analyses are done to effectively sample the known design space (pattern database) with patterns which pose high risk of being yield detractors. This is done by first characterizing patterns with attributes such as:

• critical dimensions (like width, space, enclosure etc.) which are like design rules but applied over pattern database (examples shown by gauges in figure 3).

• native properties (like complexity, pattern density etc.) which are computed with pattern topologies and/or scanline delta ranges as a whole (example shown in figure 3).

• pattern association property to describe its membership with design groups where such groups can be defined by design IPs, products, technology nodes, process design kits (PDK), critical nets etc. In figure 3, an example design is marked by regions annotated with such associations like the region with different router settings.

Pattern attributes are used to devise analytical methods for mining patterns of interest (POI) [4]. Now, these shortlisted set of patterns can be used in verification flows. This work continues the effort to establish the methodology for full chip high performance topological pattern analysis and the applications of this methodology towards analyzing design styles [5]. Case studies described in this work will include:

• Topological pattern analyses to study variations and coverage of design space by patterns across technology nodes. Here, complexity defined with the number of scanlines over the pattern is used as a metric to make such observations. Specifically, this paper will extend the prior analysis to include 7nm design styles.

• Tracking patterns to study design evolution for a product. Here, metrics including critical dimensions, native pattern properties and pattern association are used to identify and track patterns of interest.

• Router techfile changes lead to new topologies which may pose added risk. Metrics such as critical area for island shapes, line-end counts, pattern density and complexity are used to track such patterns.

10148-5, Session 2

Redundant via insertion in self-aligned double patterning

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Redundant via (RV) insertion is a common practice to enhance via yield and reliability. It is performed through a graph formulation, with the goal of inserting as many RVs as possible while ensuring the manufacturability. Consider a layout shown in Figure 1(a), where the RV candidates for each via are identified. We introduce a conflict graph in which a vertex represents an RV candidate. An edge is created for a pair of vertices if they are from the same via. We also generate an edge between two vertices if their corresponding RV candidates are physically overlapped. The RV insertion problem can now be reduced to the maximum independent set (MIS) problem on the conflict graph; the MIS corresponds to RV candidates of the maximum number without any conflict.

Self-aligned double patterning (SADP) process, however, brings a new challenge to RV insertion owing to the cuts generated for via manufacturing. Figure 2 depicts how an RV insertion affects cut mask generation of SADP process. Once we insert an RV at v, the M3 wire w has to be extended toward its non-preferred direction, and thus an additional rectangle-shaped cut must be formed. The additional cut is then merged with the pre-existing metal cut, and finally grows into an L-shaped cut; we call this kind of cuts RVL cuts, and they are patterned by litho-etch-litho-etch (LELE) process. As such, when we insert an RV in SADP process, an RVL cut is always created on either metal layer connected by the via.

Since RVL cuts are not considered during cut mask optimization, they may end up with cut conflicts with other cuts resulting in the reduced number of available RV candidates. Therefore, there is no valid RV candidate that ensures cut manufacturability in SADP. The conflict graph now has no vertex (see Figure 3(b)), so we cannot insert an RV for the example layout.

In this paper, we propose an RV insertion method for SADP process that effectively removes the cut conflict caused by the RVL cuts, and thereby increases the number of RVs to be inserted. The proposed method consists of two steps: the identification of RV candidates with mergeable RVL cuts and the graph-based RV insertion. We notice that there are some chances to merge an RVL cut with its neighboring cuts so that the cut conflict is resolved. Therefore, given a design after detailed routing and its RV candidates, we first check each RV candidate whether the corresponding RVL cut is mergeable with neighboring cuts or not, as shown in Figure 5(a). We then formulate a conflict graph only with the RV candidates having mergeable RVL cuts (Figure 5(b)), and insert RVs by solving the MIS problem.

Our method will be applied on a set of test circuits after detailed routing using an industrial SADP process. The effectiveness of the proposed approach in the increase of the number of RVs will be demonstrated by comparing to the conventional RV insertion method without consideration of cut mask conflicts.

10148-6, Session 2

Imbalance aware lithography hotspot detection: A deep learning approach

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As circuit feature size shrinks down to 20nm, lithographic defect (hotspot) caused by light diffraction during manufacturing procedure has become a serious factor that affects manufacture yield. Hotspot detection at post-OPC stage is imperative to check potential circuit failures when transferring designed patterns into silicon wafer.

Many studies have been carried for lithography hotspot detection. The state-of-the-art methods include lithographic simulation, pattern matching and recently prevailing machine learning techniques. Lithographic simulation is able to generate fabrication result accurately, but it suffers from great runtime consumption. Although pattern matching provides speedup in comparison with lithographic simulation, it is merely applicable to detect already known or similar patterns and has poor hotspot recognition rate on unknown patterns. On the other hand, machine learning as an emerging technique has been able to achieve reasonable good result for hotspot detection with lower time consumption. In a machine learning flow, raw data should be preprocessed in feature extraction stage, before feeding into the learning machine engine. Feature representation of original data directly affects prediction performance. In the case of VLSI layout, conventional density based and recently proposed concentric circle area sampling (CCAS) take advantages of layout properties and lithography process thus have made considerable improvements on hotspot detection accuracy.

However, with circuit feature size reducing to several nanometres, layout patterns have become more complicated, hence manual feature extraction will miss important information loss when predicting potential error in ultra large scale integrated circuit mask. Convolution neural networks (CNN) have been proved capable of extracting accurate image representations and performing accurate classification task. However, such technique cannot be directly applied for layout defect prediction with the following reasons:

• Layout dataset for hotspot detection is highly imbalanced as defects are always the minority, therefore ordinary training is not reliable.

• Layout pattern varies with technology nodes, foundries and layers, etc. Training large neural network is quite time consuming even with high performance GPUs. Thus, it is hard to build individual models for different layout pattern types.

To address these concerns, in this paper first we upsample minority hotspots of the layout benchmark suit, and then we use preprocessed layouts as training set and feed them into a 3-stage CNN. In order to yield robust feature map and CNN model, inspired by research in human recognition area (e.g. [15]), we combine all benchmark suits together to keep diversity of the training data. Particularly, with robustness, the trained model can be easily transferred to different layout patterns through fine-tune. 16 Our CNN architecture is implemented on Caffe and consists of three convolution stages for different level feature abstraction and two full-connected layers for prediction, as shown in Fig. 1. Each convolution stage includes a convolution layer for feature extraction, a ReLU layer to induce nonlinearity to the network and a pooling layer to keep the feature invariant to minor changes of the input. Mini-batch gradient descent is applied to update neuron weights. Pre-training of the combined layout benchmark takes 8000 iterations to converge, while individual category fine-tuning converges within 1000 iterations.

The proposed hotspot detection framework is verified in ICCAD-2012 benchmark suite. Details of results are shown in Table 1(see attached pdf), where the proposed deep learning model can achieve overall accuracy of 97%. Test results show that our model can achieve comparable or better results in comparison with state-of-the-art hotspot prediction works.

10148-7, Session 2

Optimization of complex high-dimensional layout configurations for IC physical designs using graph search, data analytics, and machine learning *(Invited Paper)*

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Integrated circuit (IC) manufacturing yield is the result of complex high dimensional layout configurations interacting with process parameters, materials, tool settings, and truly random events. When yield-limiting layout configurations enter the IC fabrication plant (FAB), engineers observe problems in simulation, in physical defects, or in electrical failures of the IC devices. They prioritize high frequency problems and then attempt to isolate the cause of each problem through hypothesis. Remedies include modifying the layout configuration through retargeting, adjusting the optical proximity correction (OPC) recipe, or adjusting the manufacturing process to add manufacturing margin. Further observations determine whether the changes demonstrate an improvement, validating or invalidating the hypothesis. In this way, yield is iteratively improved through accumulation of experimental changes over several years, in response to detected failures.

An underlying core issue is that our industry has not been able to fully characterize design variation, i.e. the intrinsic entropy of a design. FAB engineers do observe correlations between layout configurations, manufacturing process, physical defects and electrical device failures, so they intuitively understand the role that design variation plays, but they do not have the tools to address design variation due to the quantity and complexity of these variations. Through our data analytics, we now know that a typical new design has millions of layout configurations that the FAB engineer has never seen before, and that some of these configurations are problems. Knowing the disposition of each and every design variation: problematic or not, seen before or not, etc. is the key to optimizing design and manufacturing process for yield.

To analyze and quantify design variability, which are the source of the yield-limiting layout configurations, we present a method to systematically characterize the space of all possible configurations. All potential design variations are part of this space, and therefore, the coverage of this space by any given design layout can be computed. Coverage can be compared between designs, for example, test chip vs. product, or product A vs. product B to quantify key coverage differences. Furthermore, the configurations for which there is a lack of coverage can also be computed. These “missing” configurations are used to systematically drive data acquisition, resulting in complete characterization of the entire configuration space.

The configuration space is represented by a graph, with nodes representing configurations, and edges linking related configurations. Observational data for each configuration, such as simulation, metrology, defect, and failure data can be further annotated onto each node. Graph search and machine learning algorithms are applied to the graph to identify and eliminate yield-limiting configurations. As a result, integrated circuit designs can be effectively optimized for manufacturing yield.

10148-8, Session 3

Cost effective solution using inverse lithography OPC for DRAM random contact layer

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Many different advanced devices and design layers currently employ double patterning technology (DPT) as a means to overcome lithographic and OPC limitations at low k1 values. Certainly device layers with k1 value below 0.25 require DPT or other pitch splitting methodologies. DPT has also been used to improve patterning of certain device layers with k1 values slightly above 0.25, due to the difficulty of achieving sufficient pattern fidelity. Unfortunately, this broad adoption of DPT also came with a significant increase in patterning process cost. In this paper, we discuss the development of a single patterning technology process using an integrated Inverse Lithography Technology (ILT) flow for mask synthesis. The new single pattering technology flow will reduce the manufacturing cost for a full chip random contact layer in a memory device by replacing the more expensive DPT process with ILT flow, while also maintaining good lithographic production quality and manufacturable OPC/RET production metrics.

This new integrated flow consisted of applying ILT opc to the difficult core region and rule based assist features (RBAFs) opc to the peripheral region of a DRAM contact layer. Comparisons of wafer results between the ILT process and the non-ILT process showed the lithographic benefits of ILT and its ability to enable a robust single patterning process for this low-k1 device layer. Advanced modeling with a negative tone develop (NTD) process achieved the accuracy levels needed for ILT to control feature shapes through dose and focus. Details of these afore mentioned results will be described in the paper.

10148-9, Session 3

SOCS-based post-layout optimization for multiple patterns with light interference prediction

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As technology node shrinks down, hotspots which are patterning failure on wafer after etching process become an inevitable problem. The main cause of such hotspots is low contrast of optical image.

In this paper, we propose SOCS based post-layout optimization for multiple patterns with light Interference prediction, which can improve the image contrast of hotspots.

Due to the linearity of the coherent systems, we can individually evaluate the direction to good light interference relative position between every two patterns in layout based on waveform of dominant SOCS kernels. This algorithm is similar to an "interference map" which is used to place sub-resolution assist feature (SRAF). If one pattern is shifted to a better light interference relative position, it is a better relative position for some patterns, but it is not a better relative position for other patterns in some cases. Therefore, we select the direction to the position where is the best relative position for the majority of patterns. Then we simultaneously move all patterns a little bit to the selected direction. We iterate this manner until all patters stop moving. In our presentation, we will discuss the details and effectiveness of our method with experimental results.

10148-10, Session 4

Directed self-assembly (DSA) of Lamella-type of copolymers in self-aligned via (SAV) application from design to patterning

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Directed self-assembly (DSA) of block copolymer (BCP) is a promising alternative technology to extend optical lithography with fewer patterning steps for 5nm technology and below. It uses the phase separation of block copolymer e.g. lamellar or cylindrical copolymer, and provides resolution enhancement with topological (grapho-epitaxy) or chemical (chemo-epitaxy) pre-patterned surface.

In the past few years, we have been trying to understand the interactions among DSA material, design, and patterning using grapho-epitaxy with cylindrical copolymers for conventional square vias. In this paper, we will focus on investigating the same using grapho-epitaxy of lamella-type copolymers for self-aligned via (SAV) applications. The SAV process has been widely used to enable transfers in via patterns through etch with enhanced Via-to-Metal time-dependent-dielectric-breakdown (TDDB) performance. Unlike the conventional square vias, the design for SAV is of rectangular shape.

First, we study various guiding pattern shapes to form SAV with lamella-type copolymers, and then calculate and compare the template error enhancement factor (TEEF) with Monte Carlo Simulations assuming different sidewall wettings ps-wetting vs. pmma-wetting. Next, we investigate the DSA-aware grouping and decomposition schemes by using GLOBALFOUNDRIES 5nm SAV designs on post placement-routing layouts at different utilizations ranging from 60% up to 100%. We will try to understand the necessary DSA-aware design rules to maximize the design utilization (thus more scaling) and mask number reduction. Finally, we demonstrate a complete DSA manufacturing flow for lamella including DSA synthesis, OPC, and DSA verification with Mentor Graphics's compact model. We will compare the pros and cons of using lamella and cylinder BCP for via layer in terms of design rules, TEEF and patterning.

10148-11, Session 4

Efficient DSA and DP hybrid lithography conflict detection and guiding template assignment

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In recent years, directed self-assembly (DSA) has demonstrated tremendous potential to reduce cost for multiple patterning with fewer masks, especially for via patterning. DSA is considered as the one of next generation lithography candidates or complementary lithography techniques to extend 193i lithography further for the sub-7 nm nodes. In DSA aware design, via decomposition and DSA guiding template assignment should be done simultaneously in order to obtain the optimal result. In addition, for standard cells, the DSA aware decomposition conflict can occur if DSA constraints are not considered during design stage. Therefore, DSA aware conflict detection for standard cells is important. Unfortunately, due to the limited DSA patterns and other DSA constraints, DSA guiding template assignment and decomposition are more difficult than conventional multiple patterning decomposition. There is no polynomial-time method to obtain the optimal solution because the problem is NP-complete.

In this work, we first analyze the cost of DSA patterns with different shapes and sizes. The cost of DSA patterns with the same size is measured as the average placement error between target and simulated contacts. We then propose a graph-based approach to reduce the problem size and solve the problem more efficiently without affecting the optimality of the final result. First, a DSA conflict/grouping graph of the via layer is constructed based on DSA constraints and design rules: DSA minimum distance, maximum distance and minimum same-mask spacing for the guiding template mask. Targeting DSA with double patterning for guiding templates on via layer, we can convert the problem to the constrained minimum cost edge bipartization problem. Edges of the DSA conflict/grouping graph can be deleted to indicate whether the corresponding vias are grouped or conflicted. The final graph should be a bipartite graph so that the vias can be patterned by DSA with double patterning for guiding templates. The problem is constrained due to the DSA constraints: forbidden patterns, maximum grouping size, and etc. The conflict/grouping graph are first trimmed to eliminate branches and nodes that have no impact on the DSA grouping and guiding template decomposition. Then based on the planarity properties of the conflict/grouping graph, two different ILP formulations are proposed which significantly reduce both the variables and constraints compared to previous work.

We first test our proposed method on a scaled 7 nm standard cell library and several clips with different sizes extracted from a fully routed industrial processor for 7 nm nodes. The standard cell library consists of 132 cells. In order to check the impact of the minimum lithography distance on the final result, we perform tests with the enumerated minimum lithography distance. The experimental results show that the total number of DSA conflicts and DSA groups of the standard cells increase significantly with the growth of the minimum lithography distance. We then perform experiments on different size clips to analyze and compare the performance between a previous ILP formulation and our formulation. The results demonstrate that we can achieve 50% reduction in both the number of variables and constraints compared to previous work, and a 50X speed up in the final runtime.

10148-12, Session 4

Technology path-finding for directed self-assembly for via layers

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Directed Self Assembly (DSA) is a very promising patterning technology

for the sub-7nm technology nodes, especially for via/contact layers. In the Graphoepitaxy type of DSA, a complementary lithography technique is used to print the guiding templates, where the Block Copolymer (BCP) phase-separates into regular structures. Accordingly, the design-friendliness of a DSA-based technology is affected by several factors: the complementary lithography technique, the legal guiding templates, the number of masks/exposures used to print the templates, the related design rules, the forbidden patterns (hotspots) and the characteristics of the BCP. Thus, foundries have a huge number of choices to make for a future DSA-based technology, affecting the design-friendliness and the cost of the technology.

In this paper, we propose a framework for DSA technology path-finding, for via layers, to be used by the foundry during Design and Technology Co-optimization (DTCO). The framework optimally evaluates a DSA-based technology where an arbitrary lithography technique is used to print the guiding templates, possibly using several masks/exposures and provides a design-friendliness metric.

To the best of our knowledge, this is the first optimal and general framework to be proposed for evaluation of any DSA-based technology (using any complementary lithography technique), that can have multiple masks/exposures to print the guiding templates. The framework manifests correct-by-construction methods to avoid DSA templates that create technology-specific hotspots. The evaluation is performed by using the input technology specifications to formulate an Integer Linear Programming Problem (ILP) to choose the DSA groups and do the mask assignment in the way that minimizes the number of conflicts.

Several novel technologies are evaluated using the proposed framework, including DSA+EUV, DSA+SADP and DSA+E-beam. For example, one study showed that one mask in a DSA+EUV technology can replace three masks in a DSA+193i technology, if non-manhattan guiding templates are allowed. Another study shows that to be able to use SADP to print the guiding templates, correct by construction design methods should be used, in order to prevent the existence of three layout patterns that are not manufacturable in SADP.

10148-13, Session 4

Density driven placement of sub-DSA resolution assistant features (SDRAFs)

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In the pursuit of alternatives to traditional optical lithography, block copolymer directed self-assembly (DSA) has emerged as a low-cost, high-throughput option. DSA uses small topographical templates to contain the block copolymer and create small clusters of holes useful for patterning vias. However, issues of defectivity have hampered DSA's viability for large-scale patterning. Recent studies have shown polymer fill level to be a crucial factor in defectivity, as template overfill can result in malformed DSA structures and poor LCDU after etching. The inherent density variations in via layouts, though, make regions of overfilled templates nearly inevitable, as templates in less dense regions will contain more polymer. For this reason, it is previously demonstrated the use of sub-DSA resolution assist features (SDRAFs) as a method of evening out template density. The SDRAFs divert excess polymer from the overfilled via templates but are themselves too small to form transferrable DSA patterns. Thus, we can populate low-density regions with SDRAFs to make a given layout more uniformly dense and reduce template overfill. However, excess SDRAFs may increase the manufacture variation and print unexpected holes. As a result, minimizing the number of SDRAFs inserted is desirable.

In this work, we propose a method for SDRAF placement in random logic via layouts using a greedy algorithm. To start, we set basic design rules for minimum pitch on a single mask and minimum resist thickness between features: 95 nm and 45 nm, respectively, for 193 nm immersion. Based on experimental data, we also set the maximum CD of the SDRAFs to be 40 nm for a PS-wetting flow using a PS-b-PMMA block copolymer of L0 = 37 nm.

We test our SDRAF placement on the via 2-3 layer of a Cortex M0 processor scaled from a 32 x 32 nm grid to a 24 x 24 nm grid to fit with the specifications of the 5 nm node. We measure the effectiveness of the SDRAF placement by dividing the layout into overlapping windows set at the size of the DSA interaction range, defined as the length over which the polymer reflows during thermal anneal (~500 nm). Within each window, a measurement of density is calculated by summing the total area occupied by the templates (both SDRAF and via templates) and dividing by the area of the window.

The SDRAF placement algorithm follows a greedy scheme, which iteratively inserts an SDRAF into areas with the highest priority. The priority is determined based on the total demand for SDRAFs of all nearby DSA templates within a window frame. Based on experimental results, we are able to efficiently place SDRAFs to uniform the local density with neglectable variations by using the minimum number of insertions without violating any design rules.

This SDRAF placement scheme gives a path to integrating SDRAFs into random logic via layouts and to mitigating the effects of template overfill due to density non-uniformity. This investigation of SDRAF placement sheds light on the DSA density variation problem and suggests future paths to mass deployment of DSA.

10148-32, Session PSWed

Low-track height standard-cell design in N5 using scaling boosters

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The 7.5-Track architecture employs metal layer called MINT which is laid horizontally below M1 and above front end of line (FEOL). MINT optimally connects the FEOL layers and enables efficient connection to the BEOL routing layer in the standard-cells. With M2/MINT pitch of 32 nm, 7.5-Track standard-cell height is 240 nm. This allows 3fins for each device at max. A templates based technique is used to build the 7.5-Track standard-cells. Where basic

templates are first defined. The vertical connections are completed in M1 and the horizontal routing inside the standard-cells is performed with the help of MINT. In the NAND gate the gate contact is performed in such a way that the M0G on the adjacent gates are faced in opposite direction and then a dummy gate is used for isolation. This leads to higher dummy poly count within the cell with 3 fins.

The 6.5-Track standard-cell architecture has 5 MINT routing tracks compared with 7.5-Track, which is a reduction of two signal routing tracks, since the ground rules are kept equal. Here the VDD/VSS track is moved to MINT level and M2 is freed for high level signal routing. The routing resource reduction is combated by introducing a scaling booster

at the gate contact level. This is achieved by using fully Self-Aligned Gate Contact 3 (SAGC) scheme. With the help of this technique the contact can be made over the active region. The SAGC significantly increases the gate contact placement options, thereby reducing the demand on the insertion of dummy poly gates compared with 7.5-Track architecture.

Track reduction is an effective knob for area reduction. In terms of no. of poly used to complete the cell, the 6.5 and 6-Track have the same number of poly used in the cells. This means that the 6-track cell library has advantage of half a track in the area. It is seen that the SAGC give the first largest reduction in size by increasing the gate contact flexibility shown in both 6.5 and 6-track library cells. The buried rail in 6-Tracks further helps in the reduction of area compared with 7.5-track cell architectures. Overall, the 6.5 and 6-Track have an area reduction of 40% and 45% w.r.t. a 7.5-track, respectively.

The use of scaling boosters such as using MINT and intermediate middle of line metal, self-aligned gate contact (SAGC) and buried rail leads to a cell library with significant area gains up to 45% for N5 node.

10148-33, Session PSWed

Line-edge quality optimization of electron-beam resist for high-throughput character projection exposure utilizing atomic force microscope analysis

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Electron beam lithography (EBL) for direct wafer writing (EBDW) is expected to provide a low-cost solution for advanced semiconductor fabrication with high-resolution lithography. However, EBDW is not suitable for high-volume production due to its low throughput characteristics even with high-speed EBDW methods such as the variable shaped beam (VSB) method.

In VLSI Design and Education Center, the University of Tokyo, we are running an open-use nanotechnology research facility including class 1, 10, and 1000 clean rooms for universities, research institutes, and companies in Japan. In this facility, EBL tools are attracting many users for both mask fabrication and direct wafer/chip writing, both of which do not expect very-high throughput like high-volume production level but moderately-high throughput for users' convenience and better efficiency of the shred tool usage. Our EBL tools from ADVANTEST support both VSB method and character projection (CP) method, which is suitable for regular, repeated shapes like standard-cell logics and memory arrays. However, most VDEC users are aiming for non-VLSI applications like photonics, MEMS, and MOEMS. Such devices can receive the high-speed benefit of VSB over the conventional Gaussian-beam exposure, but not the full utility of CP capability due to wide variety of layout patterns in such applications. In addition, the stepwise edge shapes by VSB on oblique or curved edges cause rough edge conditions, which possibly degrade the device characteristics.

In our former work8, we proposed a general EBL methodology utilizing a combination of VSB and CP methods. In the process of layout data conversion with CP character instantiation, several parameters were introduced to control the shot count and the line-edge quality. We demonstrated our methodology using ADVANTEST F7000S-VD02 and HSQ resist., and made direct observations of the resist using a scanning electron microscope (SEM) for verification.

In this work, we utilized an atomic force microscope (AFM) for more precise evaluation of the resist quality to determine the influence of the control parameters. Resist shapes were captured as 3D data by careful, low-noise AFM measurement after depositing thin amorphous Osmium layer by plasma chemical vapor deposition to improve electric conductivity of the observation targets. Edge profiles of the resist were extracted numerically, and then, Fourier analysis of the edge profiles was carried out. We applied this analysis methodology to the small but regularly-presented undulations that was expected to be a result from the fringe CP shots in our CP-base EBL methodology. The Fourier analysis results of the edge profiles showed peaks at the wavelengths corresponding to the CP intervals and their fractions. It is noticeable that samples with very small undulations obviously showed such peaks while the SEM image of the same sample was not clear enough to decide the origin of the edge roughness; the CP instances or the random noise. Such capability of precise edge-roughness analysis is useful to our EBL methodology to optimize the control parameters in the layout data conversion to maintain both the line-edge quality and the exposure throughput.

10148-34, Session PSWed

Design space analysis of novel interconnect constructs for 22nm FDXTM technology

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In this paper, we describe an integrated design space analysis approach consisting of full factorial layout generation, lithography simulations with added proximity effects, and rigorous statistical analysis through monte-carlo simulations which is used in the Gate-Tie Down contact shape [1]. This agile Design Rule development process provides a quick turnaround time to down-select the potential layout configurations that can offer a competitive, robust and reliable design and manufacturing. Further layout and placement optimization is carried out to evaluate intra-cell, inter-cell and cell boundary situations, which are critical for a place and routed block. These constructs developed using the integrated approach is used to give 20-30% higher performance at the same Iddq leakage for 8T libraries in 22FDX Technology.

Process variability has not kept pace with CMOS technology scaling into the nanoscale regime, which in turn compromises integrated Circuit (IC) yields. Fully depleted Silicon-on-Insulator (FDSOI) has been proposed as a promising alternative to bulk-CMOS. Ultra low voltage operation, industry-leading performance and circuit density are key offerings of GLOBALFOUNDRIES' 22FDXTM technology. Aggressive Power, Performance and Area (PPA) and cost in 22FDXTM technology is achieved using the design rules that push the limits of process variability while guaranteeing manufacturability. To enable these cost effective and competitive designs, special Middle-of-Line (MOL) interconnect structures are offered, hereafter referred to as MOL Special Constructs. A critical development effort is to enable the Design Rules for these MOL Special Constructs. One such critical construct is identified as a Gate Tie-Down Construct to implement a continuous active area as patented by Rashed et. al. [1]. This construct and its variants are critical to gain back the loss in performance from single-diffusion break or Double Diffusion Break isolation structures in a strained channel 22FDXTM technology without compromising the power and area. The development of this construct using an agile, systematic, statistical and analytic technique is the key to ensure robust enablement which can be tested and validated through silicon in future.

Most approaches previously used have focused at full chip lithography simulations methods for design rule optimization [2], cumbersome layout generation techniques [3], fast layout generation but with limited accuracy [4] or the focus was to get area impact of Design Rules [5]. The integrated methodology (Figure 1) discussed in the paper, involves first identifying the interdependence of Design and process Fail modes and their process variation components. The Middle of line and Back-End of Line interconnect structures in advanced technology nodes have an increased interdependence of these fail modes (Figure 2). These key parameters which define the metrics of manufacturability of the interconnect structures are utilized to generate a full factorial Design of Experiments (DOE) with a quick turn-around time using automated Test Pattern Generation (TPG). Next, lithography simulations are executed and the critical patterns are down-selected based on the resolution and process-window criteria's. Additionally, rigorous analytic techniques are used for quantifying the impact of proximity shapes across three dimensions of space. This helps in the down-select of the pattern counts and establishing the impact of different

input parameters on the pattern fidelity. The process variation capability of a technology also plays a significant factor in the manufacture of these constructs. Through rigorous monte-carlo technique each of these down select patters are evaluated to quantify the impact of process variations on the yield or the performance of these interconnect constructs, eventually culminating in a group or a single optimized structure.

Following the down-select of these optimized structures, further layout and placement optimization is carried out to evaluate intra-cell, inter-cell and cell boundary situations, which are critical for a place and routed block. Finally, the cells are characterized to show the impact of these optimized interconnect structures on the Power, Performance and Area of the dense 8T standard cell library.

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10148-35, Session PSWed

IR-drop analysis for validating power grids and standard cell architectures in sub-10nm node designs

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Since chip performance and power are highly dependent on the operating voltage, the robust power distribution network (PDN) is of utmost importance in designs to provide with the reliable voltage without voltage (IR)-drop. However, rapid increase of parasitic resistance and capacitance (RC) in interconnects makes IR-drop much worse with technology scaling. This paper shows various IR-drop analyses in designs. The major objectives are to validate standard cell architectures, where different sizes of power/ground (PG) and metal tracks are validated, and to validate PDN architecture, where types of power hook-up approaches are evaluated with IR-drop calculation. To estimate IR-drops in 10nm and below technologies, we first prepare physically routed designs given standard cell libraries, where we use open RISC RTL, synthesize the CPU, and apply placement & routing with process-design kits (PDK). Then, static and dynamic IR-drop flows are set up with commercial tools. Using the IR-drop flow, we compare standard cell architectures, and analyze impacts on performance, power, and area (PPA) with the previous technology-node designs. Furthermore, we propose the best PDN structure against static IR-drop and optimize types of standard cell library against dynamic IR-drop.

10148-36, Session PSWed

A random approach of pattern library creation for full chip litho-simulation

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As technology advances, the need for running litho-checking to early detect hotspots before tapeout has become essential. This process has become more important on the level of designing standard cells and small block to the level of large IPs and full chip designs. Litho simulation provides high accuracy of detecting the printability issues for problematic patterns but it has the disadvantage of slow performance on large designs and blocks. Foundries have found a good compromise solution for doing litho-simulation on full chips by filtering out potential candidate hotspot patterns by running pattern matching (PM) and then performing simulation on the matched locations. The challenge was always how to create a PM library of candidate patterns that shows high coverage for litho-problems and in the same time shows fast runtime performance.

This paper presents a new strategy for generating candidate real design patterns through a random generation approach using Layout Schema Generator (LSG) utility. The output patterns from LSG are simulated and then classified by a scoring mechanism that can categorizes patterns according to severity of hotspots, probability of their presence in the design and the likelihood of causing a hotspot. The scoring output helps in filtering out the yield problematic patterns that should be removed from any standard cell design and in also defining the potential problematic patterns that need to be simulated within a bigger context to decide whether they represent a hotspot or not.

This flow is demonstrated on SMIC 14nm technology creating a candidate hotspot pattern library that can be used in full chip simulation with very high coverage and robust performance.

10148-37, Session PSWed

Die-to-database pattern monitor: a pattern centric approach for maximizing the potential of review SEM images and building a database of printed patterns

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Review SEM tools have been used for decades to take high resolution images of targeted locations on the wafer. The images are examined either manually or by software to detect the presence of a defect and classify the defect into one of several defect types. However, several chronic problems have plagued this seemingly simple task. For one, a large percentage of the images (often 50% or more) are discarded for being “SEM Non-Visual” or SNV, which means that the examiner – either a person or software – was unable to find any defect in those images. The remaining images are useful for yield learning, but once a defect is located within an image and classified, the image itself is typically discarded. This leads to significant underutilization of the rich information content of high resolution images. It takes precious fab time to collect the images (between 2000 and 3000 an hour on the latest tools) and sizeable capital investment in the tools themselves. When half of the output of these tools is discarded and the other half is reduced to a simple class code, it becomes poignantly clear that the Return on Investment is adversely impacted.

In this paper we discuss a solution for maximizing the potential of Review SEM images, even those that are dismissed as SEM Non-Visual (SNV). The solution entails Image to Design integration to exploit the rich information

content of each and every high resolution image. We begin by aligning each image to the design (GDS/OASIS) through contour extraction, performing a secondary defect detection by comparing the contour with the design (using single or multiple design layers) to identify defects that might otherwise have gone unnoticed, locating all critical and consequential features in the pattern (such as minimum space or minimum width geometries) using a flexible rule-based search engine (a form of automatic metrology site selection), measuring the contour at each of the critical and consequential locations, and storing both the contours and the design reference patterns in a comprehensive pattern tracking database. In this manner, the rich information content of Review SEM images is meticulously analyzed and preserved. Each image is no longer reduced to a class code; instead, each image is decomposed into as many sub-patterns as the number of critical and consequential features that are present in the field of view. And all of these sub-features are measured, stored, and tracked, giving rise to a database that tracks both intended patterns and actual printed patterns.

Additionally, we discuss an extension of this concept that begins by decomposing the physical layout of the chip (using the GDS / OASIS file) into a full set of critical and consequential features. Critical and consequential features are also extracted from Review SEM images collected over time. However, the features extracted from Review SEM images may be a relatively small subset of the critical and consequential features extracted through full chip layout decomposition. We therefore apply machine learning techniques to predictively rank the strength or weakness of the full set of critical and consequential features by letting the machine learn continuously from real world Review SEM images that are generated on an ongoing basis.

10148-38, Session PSWed

Gate tie-down construct in the 22FDX™ technology: a silicon-based method for layout optimization

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In order to allow competitive and compact designs in the 22nm FD-SOI technology 22FDX™, MOL/BEOL constructs have been specifically enabled in a low-cost single-pattern diffusion, gate and contacts process solution. The Gate Tie-Down (or “continuous RX”) [1] construct provides a robust electrical isolation between two abutted cells without need for diffusion break which would increase local layout effects (channel relaxation) and cause loss of area. The electrical isolation is obtained by biasing an isolation gate (IGT) and the adjacent diffusion through a specific contact (CO) (Fig.1).

To guarantee its full manufacturability and quality, the Gate Tie-Down construct must be validated against 5 key-failure modes:

1. open fail of the isolation gate to contact connection, driven by the physical overlapping area.

2. contact-to-diffusion short fail, driven by the spacing between CO and the neighboring diffusion.

3. contact-to-well short. In Silicon-on-Insulator technologies, the misalignment of the contact (insufficient enclosure of CO by diffusion) can result in a punch-through to the underlying substrate.

4. metal-to-contact connection.

5. contact-to-neighboring gate short.

The present work is focused on the more critical failure modes 1 to 3. Failure modes 4 and 5 were tested independently and show large design margins.

A full-factorial Design of Experiment is used for the construct validation. It is designed as a full-factorial set of the following geometrical parameters (Fig.1):

1. the position of the contact (CO_x).

2. a local increase of the isolation gate width on each side (IGT_siz- and IGT_siz-+).

3. the contact enclosure by diffusion (CO_enc_DIFF) to stress the contact-to-well short failure mechanism.

4. the nominal isolation gate width (IGT_w) to include the nominal channel leakage.

Dedicated test structures were designed and the contact resistance and leakage currents were measured. The contact-to-well short failure was not evidenced.

The CO-IGT resistance is predominantly influenced by the contact position CO_x while increasing the nominal (IGT_w) and the local gate width (IGT_siz-) has a secondary beneficial effect.

The main layout impact on the CO-DIFF leakage is the nominal gate width itself. This tends to show that the Gate tie-down construct does not create any additional short-typed fail within the investigated layout range. The leakage plotted versus CO_x seems disturbed by the contact open starting at negative CO_x values, weakening the tie-down.

Finally, the CO enclosure by Diffusion does not provide any significant response, showing a robust process margin against the contact-to-well short.

An optimal layout is found for a small positive contact offset beyond the IGT centerline with an increased local gate width. As a validation, the yield was calculated over a larger pool of 250 similar dies with approximately 100k contact links each (Fig.2). A robust trade-off is confirmed between a maximized contact-gate area and a safe contact-to-diffusion distance.

After presentation of the principal failure modes, the Design of Experiments applied to the critical Gate Tie-Down construct allowed to isolate the determine the gate-to-contact open and the contact-to-diffusion short as the two most sensitive failures and to determine an optimized layout. This layout shows a very robust margin when tested over a much larger number of occurrences.

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10148-39, Session PSWed

The new OPC method for obtaining the stability of MBAF OPC

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Current patterning technology for manufacturing memory devices is being developed towards enabling high density and high resolution capability. However, as applying high resolution technology results in decreased process margin, OPC has to compensate for such effect. Since the process margin is decreased greatly for contact layers, technologies such as RBAF (Rule-Based Assist Feature), MBAF (Model-Based Assist Feature), and ILT (Inverse Lithography Technology) are considered to maximize the process margin. Although ILT is the best solution in terms of process margin, it has several disadvantages such as long OPC run-time, mask complexity, and unstable mask fidelity. MBAF method has the same issues but to a lesser degree, which is why it is often used for contact layers.

When setting up the rules for RBAF, not all patterns are considered. Thus, applying RBAF for contact layers may result in decreased process margin for certain patterns since the same rule is applied globally. MBAF, on the other hand, can maximize the process margin for various patterns as it generates AF (Assist Feature) to locations that maximizes the margin for the patterns considered. However, MBAF method has a critical disadvantage

that even a slight change of a target influences the locations of the AF. This leads to generating different OPCed CD of the main features, even the ones that should not be affected by the changed target. Once the OPCed CD is changed, it is impossible to obtain the same mask CD even when the mask is manufactured with the same method. If this case occurs during mass production, the entire layer needs to be confirmed after each revision which leads to unnecessary time loss.

In this paper, we suggest a new OPC method to prevent this issue. With this flow, OPCed shapes of unchanged patterns remain the same while only the changed targets are OPCed and replaced into the corresponding location. This method can reduce the overall OPCTAT as well as the time spent in verifying the entire layout after each revision. Details of these afore mentioned results will be described in the paper. After further research, this flow can also be applied to ILT.

10148-40, Session PSWed

User-friendly design approach for analog layout design

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The rapid development of Internet of Things (IoT) technologies for home, retail, automotive, manufacturing and wearables applications, causes companies to face unique challenges and to accelerate their design cycle to meet the market demands.1, 2 In parallel, the semiconductor industry continuously introduces more sophisticated fabrication processes to manufacture multiple devices' variants in a single SoC design with lower power consumption and higher performances. With the unprecedented challenges faced by the circuit designers and the increasing functional requirement for the system-on-chips (SoC), the analog design has become the main bottleneck in the design process.

Traditionally, the analog circuits designers and layout engineers adopt custom circuit design techniques because the circuits are particularly sensitives to the changes in the environment conditions, manufacturing processes and variations. As the engineers are advancing into advanced process technology, such design techniques and practices do not guarantee that all the circuit are fully functional with its first silicon measurement.3 Engineers can no longer depend on their experience with proven concepts and components to design the product with the new technology.

In this paper, we implement an analog device matching check (ADMC) verification suite based on the Calibre Programmable Electrical Rule Check Logic Driven Layout (PERC-LDL) industry tool, which automatically recognize all matched devices from the layout and applies analog-focused layout constraint check to highlight any potential physical and electrical device mismatch. Compared to other works, our approach only requires the custom layout, which greatly simplifies the data preparation work, providing minimum disruption to existing custom layout flow. Therefore, our solution will address layout concerns faced by analog designers and providing them with more confident with their layout's quality.

This methodology only requires the physical layout, greatly simplifies the data preparation work and minimizes the disruption to the existing custom layout flow. As shown in Fig. 1, the verification flow is seamlessly integrated into the layout environment and is broken down into five phases.

1. Data preparation
2. Layout netlist extraction
3. Layout topology extraction
4. Layout constraint checks
5. Layout debugging

10148-41, Session PSWed

Layout decomposition and analysis using pattern matching

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As technology advances, the need for pattern-based layout analysis has become more essential, it provides critical information for manufacturability evaluation, compare the layouts between products, define new critical patterns, alert any potential process issue in advance and even more improve the OPC recipe coverage. The challenge is how to decompose a layout efficiently and set up a pattern database with meaningful patterns that can best satisfy the requirement of different applications.

This paper presents a reference flow based on Calibre DRC, DESIGNrev and Pattern Matching on SMIC 14nm technology. Depending on different applications, a layout can be decomposed on the cell or feature basis. Customers can also customize the decomposition flow by using the tools flexibly. One of the advantages using Calibre Platform is that Calibre DRC and Pattern Matching can be integrated seamlessly, that is one single deck can call both regular DRC commands and pattern matching commands. The results from this flow include a unique pattern database and sample layouts that can be used as test patterns for tape-out. By running pattern matching, a statistics summary can report the number of pattern occurrences and the chip locations that cannot be covered by the existing pattern library database for a new design. Patterns from those uncovered locations will be further investigated and then can be accumulated into the pattern database. The pattern database is a great asset that can be used across teams for different applications.

10148-42, Session PSWed

A fast process development by applying design technology co-optimization

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Beyond 40 nm technology node, the pattern weak points and hotspot types increase dramatically. The typical patterns for lithography verification suffers huge turn-around-time (TAT) to handle the design complexity. Therefore, in order to speed up process development and increase pattern variety, accurate design guideline and realistic design combinations are required. This paper presented a flow for creating a cell-based layout, a lite realistic design, to early identify problematic patterns which will negatively affect the yield.

A new random layout generating method, Design Technology Co-Optimization Pattern Generator (DTCO-PG), is reported in this paper to create cell-based design. DTCO-PG also includes how to characterize the randomness and fuzziness, so that it is able to build up the machine learning scheme which model could be trained by previous results, and then it generates patterns never seen in a lite design. This methodology not only increases pattern diversity but also finds out potential hotspot preliminarily.

This paper also demonstrates an integrated flow from DTCO pattern generation to layout modification. Optical Proximity Correction, OPC and

lithographic simulation is then applied to DTCO-PG design database to detect hotspots and then hotspots or weak points can be automatically fixed through the procedure or handled manually. This flow benefits the process evolution to have a faster development cycle time, more complexity pattern design, higher probability to find out potential hotspots in early stage, and a more holistic yield ramping operation.

10148-43, Session PSWed

A novel approach of ensuring layout regularity correct by construction in advanced technologies

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Long existing philosophy of DFM which includes doing small corrections, optimizations or taking margins based on available area for a layout in its completion stage is no longer sufficient in advanced technology nodes. Layout regularity has become a mandatory prerequisite to create robust designs less sensitive to variations in manufacturing process in order to improve yield and minimizing electrical variability. In this paper we describe a method for designing regular full custom layouts based on Design and Process co-optimization. The method includes various design rule checks that can be used on-the-fly during leaf-cell layout development so that layouts are correct by construction. In the paper we present various cases of silicon issues to show that sensitivity of layout patterns to manufacturing and no consideration to regularity lead to manufacturing defects in 45nm technology and such defects have increased to big variety in much advanced technology node such as 28nm. These silicon issues lead to costly affair of process re-tuning and design re-spins but every re-tuning mostly results into other unpredicted issues and the cycle between Process and Design goes on. Unlike other conventional DFM approaches this method reduces uncontrolled layout patterns to large extent which lack predictability and result in manufacturing failure. Layout regularity rules serve as guidance to designers not to choose process unfriendly practices while making layouts. We extract a figure of merit called Layout Regularity Index (LRI) from the layouts based on the jogs, alignments and pitches used in the design for any given critical layer. Regularity Index of a layout is the direct indicator of manufacturing yield and is used to compare the relative health of different layout blocks in terms of process friendliness. Quality acceptance of the layout is based on the passing threshold of the index. The method has been deployed for 28nm and 40nm technology nodes for Memory IP and is being extended to other IPs (IO, standard-cell). In the paper we describe the gain of this approach through LRI comparison of memory compilers, one done in standard layout approach and the other done in Regular approach. This method ensures micro level regularity but restrict layout designer from the flexibility to draw any shape, so this restriction has to be well justified in terms of gain. We have quantified the gain of layout regularity with the deployed method on printability and electrical characteristics by process-variation (PV) band simulation analysis. Most accurate contour simulations are performed using production Cad2Mask/OPC and models. PV-bands are then generated from the process window corner contours and the max width of each PV-band (1/polygon) is reported. On comparing layouts drawn in standard approach and those layouts drawn with the regular approach we have achieved up-to 5nm reduction in PV band. In advance technology nodes reduction of 5nm PV-Band brings huge gain in yield. Apart from printability of individual layer, in PV-band analysis we observe reduction in gate length (= poly and active) variability which should reduce directly electrical variability.

10148-44, Session PSWed

A flexible and efficient way to set-up QA system based on pattern database management

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There is an increasing demand to build up a pattern database platform to manage patterns from various teams. This platform can be used across teams for different purposes, for instance, DFM team adds the problematic hotspot patterns from simulation to the database so that designers can fast scan the layout before the tape-out and YE (Yield Enhancement) team adds the patterns to the database from failure scan to record every failure pattern they have ever found. There are some fundamental requirements for the database setup and management, such as automated pattern capture and database query, manipulation and modification capability.

This paper presents a flow used for SMIC 28nm DRC QA regression system, but this can be easily extended to other applications or flows. DRC rule decks are updated from time to time, to ensure the update accurately hits the target and meanwhile avoid any new issue to come, a QA regression testing is mandatory. The core element of the whole system is the pattern database. Considering the run time and pattern coverage, each pattern stored in the pattern database must be customized properly with a suitable pattern size and pattern layers according to the specific DRC rule. Patterns must be assigned different tags and can be selected by these tags according to the query criterial. This whole flow is based on Calibre Platform. Calibre Pattern Matching automates the pattern capture process and classifies the patterns. Calibre pattern matching contains a Tcl API, pattern library and the pattern objects within them can be traversed and manipulated. The system also contains utilities to compare results and summarize the QA report.

10148-45, Session PSWed

Hotspots fixing flow in NTD process by using DTCO methodology at 10nm metal 1 layer

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Multiple patterning technologies (MPT), namely, patterns splitting into different masks, have been widely used as litho solutions in critical layers in 10nm and beyond. Negative tone develop (NTD) process provides better image contrast, and therefore, being used together with the MPT. From layout perspective, the design technology co-optimization (DTCO) functions effectively to optimize design rules, avoid hotspots and enlarge the litho process windows (PWs).

A new hotspot fixing flow is presented to optimize design rules and find resolution enhancement technology (RET) solutions simultaneously, which is originated from design technology co-optimization (DTCO) and highly effective in the early stage of development. The novel hotspots fixing flow is composed of following phases.

Phase1 In consideration of no-stitching requirements, two layout files, corresponding to separate colors of a double-pattern layer, are first generated based on design rules by Layout Schema Generator (LSG). These random patterns in splits can stand for the full chip of techniques waiting

to be developed. Then the post fix function automatically repairs the DRC errors, which brings a more DRC clean layout for subsequent design rules optimizations and RET solutions path-finding.

Phase2 To begin with, the potential lithography hotspots should be marked based on the value of risky spaces and structures by DRC feature for future RET optimization. And then, source, mask and design rule co-optimization is executed on critical clips covering above potential hotspots and essential patterns. It must be particularly pointed out that the early design rule always provides AEI CD instead of ADI CD. Therefore, results of the co-optimization will not only offer an optimized global bias for obtaining reasonable ADI target, but also output the optimal source and optical model. If the process parameter modification can't be up to the standard of PW, appropriate design rule optimizations may help to achieve.

Phase3 It is necessary to implement mask optimization (MO) for the full layout with forgoing modified design rule and check the initially qualified RET solutions. On one hand, when the overlapped process window of MO can't meet the specification of DOF control requirements, the first thing to try is to fine tune the global parameters for conventional MO, such as dissection value. Moreover, the local optimization with manipulating the cost function is also the effective approach for eliminating PW-limiting hotspots. On the other hand, defects of early design rules often lead invalidations of RET. Hence the design rules should be modified according to the analysis of previous results.

Phase 4 After completing the steps above, the optimized design rule and corresponding RET solutions will help real products print more robustly.

The proposed methodology proposed a novel hotspots fixing flow under the concept of DTCO. The random patterns based on early design rules serve as the test patterns for providing optimized design rule and optimal RET solutions. Our demo simulations applied to 10nm node M1 layer indicates that the proposed the hotspots fixing flow can ensure a friendly design rule and avoid later design rework.

10148-46, Session PSWed

Stitching-aware in-design DPT auto fixing for sub-20nm logic devices

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As the technology continues to shrink below 20nm, Double Patterning Technology (DPT) becomes one of the mandatory solutions for routing metal layers. From the view point of Place and Route (P&R), the major concerns are how to prevent DPT odd-cycles automatically without sacrificing chip area. Even though the leading-edge P&R tools have advanced algorithms to prevent DPT odd-cycles, it is very hard to prevent the localized DPT odd-cycles, especially in Engineering Change Order (ECO) routing. In the last several years, we developed In-design DPT Auto Fixing method in order to reduce localized DPT odd-cycles significantly during ECO and achieve remarkable design turn-around times (TATs). But subsequently, as the design complexity continued increasing and chip size decreasing, we needed a new In-design DPT Auto Fixing approach to improve the auto. fixing rate.

In this paper, we present the Stitching-Aware In-design DPT Auto Fixing method for better fixing rates and smaller chip design. The previous In-design DPT Auto Fixing method detected all DPT odd-cycles and tried to remove odd-cycles by increasing the adjacent space. As the metal congestions increase in the newer technology nodes, the older Auto Fixing method has limitations to increase the adjacent space between routing metals. Consequently, the auto fixing rate of older method gets worse with the introduction of the smaller design rules. With DPT stitching enablement at In-design DRC checking procedure, the new Stitching-Aware DPT Auto Fixing method detects the most critical odd-cycles that cannot be corrected by stitching and need to have the adjacent space increased. The accuracy of the new flow ensures better usage of space in the congested areas, and helps design smaller chips.

By applying the Stitching-Aware DPT Auto Fixing method to sub-20nm logic devices, we can confirm that the auto fixing rate is improved by ~2X compared with auto fixing without stitching. Additionally, by developing the better heuristic algorithm and flow for DPT stitching, we can get DPT compliant layout with the acceptable design TATs.

10148-47, Session PSWed

An efficient way of layout processing based on pattern matching for defects inspection application

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As technology advances, escalating layout design complexity and chip size make defect inspection becomes more challenging than ever before. The YE (Yield Enhancement) engineers are seeking for an efficient strategy to ensure accuracy without suffering running time. A smart way is to set different resolutions for different pattern structures, for examples, logic pattern areas have a higher scan resolution while the dummy areas have a lower resolution, SRAM area may have another different resolution. This can significantly reduce the scan processing time meanwhile the accuracy does not suffer. Due to the limitation of the inspection equipment, the layout must be processed in order to output the Care Area marker in line with the requirement of the equipment, for instance, the marker shapes must be rectangle and the number of the rectangle shapes should be as small as possible. The challenge is how to select the different Care Areas by pattern structures, merge the areas efficiently and then partition them into pieces of rectangle shapes.

This paper presents a solution based on Calibre DRC and Pattern Matching. Calibre Pattern Matching's automated visual capture capability enables designers to define these geometries as layout patterns and store them in libraries which can be re-used in multiple design layouts. Pattern Matching simplifies the description of very complex relationships between pattern shapes efficiently and accurately. Pattern matching's true power is on display when it is integrated with normal DRC deck. In this application of defects inspection, we first use Calibre Pattern Matching's automated pattern capture capability to capture Care Area shapes centered on care areas layers with a tune able pattern halo. Then in the pattern matching step, when the patterns are matched, a bounding box marker will be output, this is equivalent to merge those care areas layers effectively with rectangle shapes. The pattern matching output merged marker can be further processed by the traditional DRC commands to partition them into the rectangle shape representatives.

10148-48, Session PSWed

Process weakness assessment by profiling all incoming design components

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Foundries normally receive a large number of designs from different customers every day. It is desired to automatically profile each incoming design to quantify certain metrics like 1) the number of polygons per GDS layers 2) what kind of electrical components this design contains 3) what the dimensions of each electrical component are 4) how frequently any size of components have been used and their physical locations.

This paper will present a novel method of how to generate a complete list of components for any particular design. The component checking flow need to be complete within hours so it will have very little impact on the tap-out time. A pre-layer checking method is run to group commonly used layers for different electrical components and then employ different layout profiling

flows. The foundry does this design chip analysis in order to find potentially weak devices due to their size or special size requirements for particular electrical components. The foundry can then take pre-emptive action to avoid yield loss or make an unnecessary mask for new incoming products before fab processing starts.

10148-49, Session PSWed

Using pattern matching to increase performance in hotspot fixing flows

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As feature sizes and pitches continue to decrease, more complex correction algorithms are needed to solve increasingly difficult geometric configurations. Usage of these more complex algorithms results in unacceptably long time-to-mask when applied to an entire design. In many cases, the more complex algorithms are only required in a small percentage of areas of the entire design, and these areas are not always known prior to tapeout. Hotspot fixing (HSF) flows are increasingly used to fix these hotspot areas to minimize errors and decrease time-to-mask. These flows involve "re-correcting" a design, using the previous correction output as the input to the HSF flow. This input file contains a hierarchy that was optimized for the original correction. Hotspot areas are frequently smaller than the original correction areas and frequently repeat in unique cell outputs of the original correction, so the optimal hierarchy for a HSF fix flow may be very different from the original correction. A new hierarchy, optimized for HSF, is difficult to form from the corrected output. This paper describes the usage of pattern-matching to regain hierarchical compression for identical hotspot areas that are not repeating cells in the original correction. Using this pattern-matching HSF flow, turnaround time for the hotspot fixing can be more than 50X faster than re-using the original correction's hierarchy for complex HSF methods. These significant gains can be achieved in spite of the additional complexity it can add to the flow. In the case where simpler/faster HSF correction methods are used, significant turnaround time gains can still be made by using this pattern matching technique.

10148-50, Session PSWed

Litho hotspots fixing using model-based algorithm

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As technologies advances designs are getting more sophisticated, and it is more critical to fix printability issues. Running lithography checks before tapeout is now mandatory for designers and this creates a need to find more advanced and easy techniques to fix hotspots found after litho simulation without creating a new DRC violation or generating a new hotspot.

This paper presents a methodology for fixing hotspots on layouts, using the same engine used for detecting hotspots. The fix is done by applying minimum movement of edges causing the hotspot, after considering DRC constraints. The fix is internally simulated by the Litho-simulation engine to verify that the hotspot is gone and that no new hotspot is generated because of this move.

The fix checking is extended by adding DRC checks in the LFD rule file to guarantee that any hint that violates DRC checks are removed from the output hint file. This extra checking takes off from the designer the burden of rerunning both DRC and LFD to make sure that the hint successfully fixed the hotspot.

This methodology is demonstrated on industrial designs, where the fixing rate of single and dual layer hotspots is reported.

10148-51, Session PSWed

Using design differentiating methods to find suspect design patterns which cause failure

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The systematic yield detractors are normally expected to be identified by ATPG test result diagnostics. Different test patterns have been designed to test different functions. Test diagnostics can identify failed functions so that product engineers, based on testing results, can narrow down which block in the design performs this function. However, it is hard to narrow down to a more specific region in a product.

This paper will present a working flow for using design diffing techniques to extract layout structures and perform a geometry analysis flow combined with testing results to find possible suspects that may cause particular function failures.

10148-52, Session PSWed

Electrical failure debug using interlayer profiling method

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It is very well known that as technology nodes moved to smaller sizes, the number of design rules increases and design structure becomes more regular but the process manufacture step has increased as well. Normal inspection tools can only monitor hard failure on a single layer. For electrical failure happened due to inter layers misalignments can only detect through testing.

This paper will present a working flow for using interlayer profiling techniques to turn multiple layer physical info into grouped linked parameter values. Using data analysis flow combined with electrical model to find critical region on a layout for yield learning.

10148-53, Session PSWed

A fast and efficient method for device level layout analysis

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There is an increasing demand for device level layout analysis, especially as technology advances. The analysis is to study standard cells by extracting and classifying critical dimension parameters. There are couples of parameters to extract, like channel width, length, gate to active distance, and active to adjacent active distance, etc. for 14nm technology, there are some other parameters that are cared about. On the one hand, these parameters are very important for studying standard cell structures and spice model development with the goal of improving standard cell manufacturing yield and optimizing circuit performance; on the other hand, a full chip device statistics analysis can provide useful information to diagnose the yield issue. Device analysis is essential for standard cell

customization and enhancements and manufacturability failure diagnosis.

Traditional parasitic parameters extraction tool like Calibre xRC is powerful but it is not sufficient for this device level layout analysis application as engineers would like to review, classify and filter out the data more easily. This paper presents a fast and efficient method based on Calibre equation-based DRC (eqDRC). Equation-based DRC extends the traditional DRC technology to provide a flexible programmable modeling engine which allows the end user to define grouped multi-dimensional feature measurements using flexible mathematical expressions. This paper demonstrates how such an engine and its programming language can be used to implement critical device parameter extraction. The device parameters are extracted and stored in a DFM database which can be processed by Calibre YieldServer. YieldServer is data processing software that lets engineers query, manipulate, modify, and create data in a DFM database. These parameters, known as properties in eqDRC language, can be annotated back to the layout for easy review. Calibre DesignRev can create an HTML formatted report of the results that are displayed in Calibre RVE which make it easy to share results between groups.

10148-54, Session PSWed

Pattern database applications from design to manufacturing

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Pattern-based approaches are becoming more common and popular as the industry moves to advanced technology nodes. At the beginning of a new technology node, a library of process weak point patterns for physical & electrical verification are starting to build up to prevent known hotspots from re-occurring on a new design. And then the pattern set are expanded to create test keys for process development in order to verify the manufacturing capability and pre-check new tap-out designs for any potential yield detractors. With the database growing, the adoption of pattern-based approaches has expand from design flows to technology development and then needed for mass-production purposes.

This paper will present the complete downstream working flows of a design pattern database. This pattern-based data analysis flow covers different applications cross different function teams from generating enhancement kits to improve design chip manufacturability, populate new testing design data based on previous-learning, generate analysis data to improve mass-production efficiency and manufacturing equipment in-line control to check machine status consistency across different fab sites.

10148-55, Session PSWed

Enhancing manufacturability of standard cells by using DTCO methodology

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Lithography professional community has come to an agreement that 193nm immersion will be the dominant technology till 7nm logic node (L7nm). Considering wafer topography and process variations, the practical resolution of 193nm immersion lithography is about 40nm half pitch. In order to support small scaling design rules, such as 14-16nm half-pitch in M1 of L7nm, double patterning, triple patterning, and even quadruple patterning have been applied into use. The original design layout with small pitches will be split into two, three, or even four masks. Meanwhile, every mask only contains patterns with half pitches much greater than 40nm and ensures to be processed by 193nm immersion lithography. Pattern split also needs to consider other relevant process situations, such as CDU, overlay, line-edge roughness. Under the concept of design technology co-optimization (DTCO), lithographers devote to the research of design flow and work with designers to guarantee manufacturability of an advanced novel layout. In one aspect, lithographers invent the patterning solution to support the design rules; in another aspect, lithographers offer feedbacks to designers for avoiding “difficult patterns”.

DTCO can be implemented in different ways, which depends on how the design flow is organized. In this paper, we demonstrate two practical ways of implementing DTCO in M1 layer. Standard cells are basic building blocks for CMOS circuits, and standard cell library (SCL) is the necessary part of PDK that is offered by foundry to design houses. SCL must have high manufacturability, i.e. large lithography process window. We present that SMO (source-mask co-optimization) can be used to assess lithography process window of SCL, and furthermore, SMO can find out potential lithography hotspots and suggest solutions. By doing this, patterns in SCL can be improved before mask tape-out. Another way of applying DTCO is more rudimentary, and it uses a pattern generator, for example LSG tool provided by Mentor Graphics, to generate various patterns based on a design rule. These patterns form a layout which can represent the full chip of technology to be developed. The layout runs through lithography simulation – SMO. The SMO results are then used to annotate the patterns with printability. We find the hotspots and provide feedbacks on design rule modifications.

10148-14, Session 5

Exploiting regularity: breakthroughs in sub-7nm place-and-route *(Invited Paper)*

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Restrictive design rules that enable the aggressive sub-resolution scaling needed for the 7nm technology node have forced critical wires to become highly regularized unidirectional gratings. Early work (The daunting complexity of scaling to 7NM without EUV: pushing DTCO to the extreme,SPIE 2015) demonstrated that un-optimized design flows can easily leave an entire node’s worth or area scaling on the table. Maintaining design efficiency and achieving adequate density in this highly restricted design environment became an important DTCO goal for 7nm and beyond. In gridded unidirectional layout environments it has become common practice to match the pitch of poly and the lowest level of metal running parallel to poly. Even though the minimum design rules allow metal pitches significantly smaller than the poly pitch, matching the pitches facilitates easy cell placement since cell abutment guarantees that both poly and metal features land ‘on grid’.

In this paper we will show that we achieved an area-efficient 6T cell layout in which the 1st-metal pitch is not constrained to match the poly pitch. Further we show that we demonstrated a placement solution that cleanly avoids conflicts with pre-placed power-staples while efficiently aligning the appropriate cell variants with both the poly and the metal design grids. Finally, we present a routing solution that takes full advantage of the additional wiring tracks facilitated by the tighter 1st-metal pitch to achieve extremely dense routing solutions in spite of very restrictive design rules.

This work demonstrates how ‘holistic co-optimization’ of design rules, cell architectures, and place-and-route capability can go beyond simply overcoming the negative impact of highly restrictive design rules by turning these restrictions into opportunities for synergistic co-optimization.

Reference:

Liebmann, Gutwin, Chu, ‘The daunting complexity of scaling to 7NM without EUV: pushing DTCO to the extreme,’ Proc. SPIE 9427, Design-Process-Technology Co-optimization for Manufacturability IX, 942702 (18 March 2015)

10148-15, Session 5

The effect of patterning options on embedded memory cells in logic technologies at N10 and N7

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Static Random Access Memory (SRAM) cells are used together with logic standard cells as the benchmark to develop the process flow for new logic technologies. In order to achieve successful integration of Spin-Transfer Torque Magnetic Random Access Memory (STT-MRAM) as area efficient higher level embedded cache, it also needs to be included as benchmark. The simple cell structure of STT-MRAM brings extra patterning challenges to achieve high density. The two memory types are compared in terms of minimum area and critical design rules in both the N10 and N7 node, with an extra focus on patterning options in N7. Both the use of SAQP mandrel and spacer engineering, as well as multi-level via's are explored. These patterning options result in large area gains for the STT-MRAM cell and moreover determine which cell variant is the smallest.

Memory cell architectures

For SRAM, three variants are investigated: the 111, 112 and 122 cells. These numbers describe the number of fins for the pull-up, pass gate and pull-down transistors. For STT-MRAM, there are also three variants of the standard dual bit line 1T 1MTJ cell investigated: the two finger cell (2 poly pitch (PP) wide), the dummy poly cell (1.5 PP wide) and the DRAM-style cell (1 PP wide).

Critical rules

The most critical layers in STT-MRAM are the contact metals and the lowest interconnect metals. As an example, figure 1 shows the circuit and layout with critical design rules for the two finger STT-MRAM cell in N10. These layers are of increased interest since their patterning techniques change from triple Litho Etch (LE3) in N10 to Self-Aligned Double or Quadruple Patterning (SADP or SAQP) in N7 due to pitch scaling (cfr Table 1). For N7, we will also explore the following options for both STT MRAM and SRAM:

• opt1: SAQP mandrel width and pitch tuning, including spacer merge (see figure 3)

• opt2: multi-level via's (see figure 2)

Results

For N7, the minimum size of short vertical metal strips limits the scaling of especially the STT-MRAM cells due to SAQP grid snapping. By either allowing flexibility in SAQP to adapt to the size of these strips or by introducing multi-level via's to avoid them all together, the cell size can be reduce by up to 33 %. The different options also result in different variants being the smallest: the two finger cell in N10, the DRAM style cell in N7 standard and opt1 or the dummy poly cell in N7 opt2. For the SRAM, the 111 cell is always smallest. The 122 cell can reach an area gain of 6 % by using either option (see also Table 2).

Conclusions

In technologies beyond N10, it is imperative to take into account all embedded memories as the benchmark for designing the process flow. STT-MRAM in particular, will be impacted significantly by the patterning options which will favor different cell variants. Since STT-MRAM targets bigger, denser memories, the minimum cell area will have a significant impact on total die size.

10148-16, Session 5

Design intent optimization at the beyond 7nm node: The intersection of DTCO and EUVL stochastic mitigation techniques

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The initial readiness of EUV patterning was demonstrated in 2016 with IBM Alliance's 7nm device technology. The focus has now shifted to driving the 'effective' k1 factor and enabling the second generation of EUV patterning. Thus, Design Technology Co-optimization (DTCO) has become a critical part of technology enablement as scaling has become more challenging and the industry pushes the limits of EUV lithography. The working partnership between the design teams and the process development teams typically involves an iterative approach to evaluate the manufacturability of proposed designs, subsequent modifications to those designs and finally a design manual for the technology. While this approach has served the industry well for many generations, the challenges at the Beyond 7nm node require a more efficient approach. In this work, we describe the use of "Design Intent" lithographic layout optimization where we remove the iterative component of DTCO and replace it with an optimization that achieves both a "patterning friendly" design and minimizes the well-known EUV stochastic effects. Solved together, this "design intent" approach can more quickly achieve superior lithographic results while still meeting the original device's functional specifications.

Specifically, in this work we will demonstrate "design intent" optimization for critical BEOL layers using design tolerance bands to guide the source mask co-optimization. The design tolerance bands can be either supplied as part of the original design or derived from some basic rules. Additionally, the EUV stochastic behavior is mitigated by enhancing the image log slope (ILS) for specific key features as part of the overall optimization. We will show the benefit of the "design intent approach" on both bidirectional and unidirectional 28nm min pitch standard logic layouts and compare the more typical iterative SMO approach. Thus demonstrating the benefit of allowing the design to float within the specified range. Lastly, we discuss how the evolution of this approach could lead to layout optimization based entirely on some minimal set of functional requirements and process constraints.

10148-17, Session 5

Identification and reliability sensitivity analysis of a correlated ground rule system (design arc)

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As semiconductor technology continues to scale in order to accommodate for smaller, low-power logic and memory chips, processes will become more complex in order to achieve the desired pitch and critical dimension requirements. At the same time layouts will become more complex so that designers may take full advantage of these new processes. This creates a demand for tools which are capable of efficiently modeling the probabilistic interactions between relevant layers and identifying key tolerances that will most affect yield and performance. These tools will allow process engineers and ground rule designers to make more informed decisions regarding design rule trade-offs as quickly and accurately as possible.

As the marginal benefit of scaling with respect to performance, power consumption, and yield continues to deteriorate, the traditional method of naïve design scaling is becoming less effective. For example, FINFET gate width has been scaling at a relatively slower pace due to degraded device characteristics. However, performance and area gains may still be achieved by decreasing PC pitch. This imbalance in geometric scaling factors forces reconsideration of entire design arcs which are constrained between gate or fin pitches from one technology to the next.

In order to accelerate the identification and modeling of relevant design arcs, a methodology is proposed to automatically identify competing design rules using a layout-based Monte Carlo simulation tool and correlation-based data analysis techniques. A Markov-Chain-based algorithm is then used to analyze the identified fail-mechanisms for their sensitivities to certain process-induced variabilities.

This method is demonstrated to be useful for both design rule definition and process technology development. From the perspective of design rule definition, this tool may be used to tune specific distances and sizes in order to optimize a design arc given a certain set of process assumptions. In the context of process technology development, the results of this sensitivity analysis were used in conjunction with high-level assumptions regarding the benefits of certain processes over others and a methodology for objectively choosing the best process(s) for a certain geometry is demonstrated. The geometric modeling tool used to conduct this analysis is shown to be scalable into the third dimension and is not limited to two-dimensional layout-based geometries. This capability will prove to be an important extension as the process technologies being proposed to further scale designs are becoming more and more sensitive to three-dimensional process variabilities. Furthermore, while this tool is not capable of actual lithographic simulations, it is shown to be capable of importing print simulations for multiple layers and subsequently performing Monte Carlo design rule calculations using the surrounding shape-dependent tolerances that advanced computational lithographic models simulate.

10148-18, Session 5

Large marginal 2D self-aligned via patterning for sub-5nm technology

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Via patterning becomes more challenging with aggressive scaling of feature size. While recent technology uses DUV immersion lithography and self-aligned via process, EUV lithography (EUVL) with 2D self-aligned via (SAV) is expected for future technology such as 5nm node. In conventional 2D SAV, material A runs alternately on each Mx and Mx+1 layer, while material C fills in between. Via design is re-targeted and inflated, so that it can be exposed under lithography and etch process variations (e.g. dose, defocus, mask error, and overlay). Note that only material A and dielectric are selectively etched while material C remains. A standard 2D SAV however has its own limitations in sub-5nm technology. For instance, 3nm technology with 24nm metal pitch takes only 6nm margin from a boundary of electrical open or short.

We propose a new integration flow of 2D SAV which provides three times larger margin compared to conventional approach. This flow utilizes three different materials (A, B, and C) on cap-layer of Mx and on dielectric of Mx+1; material A and B alternately run within metal trench of Mx+1. Metal intersections, where vias can form, are of four types according to stacked materials (AA, AB, BA, and BB). Each type is associated with a unique etch recipe; for instance, etch recipe AA allows a hole to touch metal on Mx only at AA location, using etch selectivity of material A, B, and C. In this context, adjacent intersections are always free from electrical short, so we can obtain much larger error margin for process variations. We need four masks to cover all vias in this approach, which is a limitation; in case of 24nm pitch, four DUV masks are required which is affordable, but smaller dimension requires four EUV masks.

We introduce two methods to reduce mask count: 1) forbidden via rule and 2) merged etch recipe. Forbidden via rule restricts via locations, for instance AB and BA locations are not allowed. Two masks now cover all vias; one mask is to make a hole at AA locations and the other for BB locations, respectively. This rule makes layout design less flexible, and its impact on layout area should be investigated. In the second method, four unique etch recipes are merged to two, and two masks are saved. We assume that etch in sequence AAB can cover etch recipe AA and AB, so that vias on AA locations and AB locations are simultaneously etched. If original via design is formed, vias are decomposed to two masks. One is for etch recipe AAB and the other is for etch recipe BBA. In both approaches, re-targeted patterns might form line shape rather than a square which allows better critical dimension uniformity.

The new integration flow is verified with SEMulator3 with practical amount of process variations. We then demonstrate both methods with scaled actual layout (LDPC) which assumes 3nm technology with 24nm metal pitch to see a defect probability.

10148-19, Session 5

Routability enhancement through unidirectional standard cells with floating metal-2

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Bidirectional cell, shown in Figure 1(a), refers to a standard cell, in which metal-1 is used for both horizontal and vertical directions. In unidirectional cell, shown in Figure 1(b), metal-1 is used only for horizontal and metal-2 is used for vertical connection; this cell has been introduced to take advantage of more regular metal patterns, which are easier to print, and so to overcome the lithography limitations in sub-32nm technology.1

In unidirectional cell, metal-2 has been usually laid out following the cell placement pitch as shown in Figure 2(a)123 . Since these metal-2 segments are unmovable, metal-2 routing (for cell to cell connection) has to follow the same cell placement pitch, which is usually larger than metal pitch (see Figure 2(b)). This causes significant reduction in metal-2 routability; it has been reported that the number of metal-2 routing tracks is reduced by 25-36%12 .

We propose a unidirectional cell with floating metal-2. Placement is performed while placement pitch is set to metal pitch. Metal-2 segment within each cell is then snapped to nearest metal pitch and is fixed as shown in Figure 2(b). This allows external metal-2 routing with metal pitch, which now uses a whole routing tracks. Our preliminary experiments indicate that the small shift of metal-2 segment negligibly affects electrical property of a cell (which has been characterized and stored in a cell library) including cell delay, capacitance, and power consumption, and hence traditional cell-based synthesis methodology can still be safely applied. Metal-1 connection within each cell should be appropriately extended so that metal-2 can be moved without any design rule violations.

Table 1 shows layout design of three example circuits using two methods: conventional unidirectional cells with fixed metal-2 following placement pitch, and the proposed unidirectional cells with floating metal-2 following metal pitch. Layout area is reduced (fourth column) because routing can be completed with smaller use of white space; this also yields smaller wirelength shown in the last column.

10148-20, Session 6

Wafer hotspot identification through advanced photomask characterization techniques: part 2

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Historically, 1D metrics such as Mean to Target (MTT) and CD Uniformity (CDU) have been adequate for mask end users to evaluate and predict the mask impact on the wafer process. However, the wafer lithographer's process margin is shrinking at advanced nodes to a point that classical mask CD metrics are no longer adequate to gauge the mask contribution to wafer process error. For example, wafer CDU error at advanced nodes is impacted by mask factors such as 3-dimensional (3D) effects and mask pattern fidelity on sub-resolution assist features (SRAFs) used in Optical Proximity Correction (OPC) models of ever-increasing complexity. To overcome the limitation of 1D metrics, there are numerous on-going industry efforts to better define wafer-predictive metrics through both standard mask metrology and aerial CD methods. Even with these improvements, the industry continues to struggle to define useful correlative metrics that link the mask to final device performance. In part 1 of this work, we utilized advanced mask pattern characterization techniques to extract potential hot spots on the mask and link them, theoretically, to issues with final wafer performance. In this paper, part 2, we complete the work by verifying these techniques at wafer level. The test vehicle (TV) that was used for hot spot detection on the mask in part 1 will be used to expose wafers. The results will be used to verify the mask-level predictions. Finally, wafer performance with predicted and verified mask/wafer condition will be shown as the result of advanced mask characterization. The goal is to maximize mask end user yield through mask-wafer technology harmonization. This harmonization will provide the necessary feedback to determine optimum design, mask specifications, and mask-making conditions for optimal wafer process margin.

10148-21, Session 6

A pattern-based design analysis method by using inline inspection data more efficiently

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The IC chip manufacturing process is an integrated working flow where after each manufacturing step, a yield inspection team will apply great effort and machine resources to inspect and sort through various check points to detect silicon failures. However, despite the great effort, they cannot efficiently cover a whole chip and cross check all the different layers and products at same time.

This paper will present a smart and efficient working flow that can map inspection data back onto a design. Based on those marked locations the foundry can extract the failure pattern signature to highlight rest of the potential weak regions across different layers and products. Furthermore, based on highlighted locations a distribution analysis has implemented to select good inspection check points to extend checking coverage. A full-chip post-processing flow is also implemented to process design layout so all the failure patterns are collected from inspection can direct check on this processed layout.

10148-22, Session 7

Quantifying electrical impacts on redundant wires insertion in 7nm unidirectional designs

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In nano-meter scale Integrated Circuits, via fails due to random defects is a well-known yield detractor, and via redundancy insertion is a common method to help enhance semiconductors yield. For the case of Self Aligned Double Patterning (SADP), which might require unidirectional design layers as in the case of some advanced technology nodes, the conventional methods of inserting redundant vias don't work any longer. This is because adding redundant vias conventionally requires adding metal shapes in the non-preferred direction, which will violate the SADP design constraints in that case. Therefore, such metal layers fabricated using unidirectional SADP require an alternative method for providing the needed redundancy.

This paper proposes a post-layout Design for Manufacturability (DFM) redundancy insertion method tailored for the design requirements introduced by unidirectional metal layers. The proposed method adds redundant wires in the preferred direction - after searching for nearby vacant routing tracks - in order to provide redundant paths for electrical signals. This method opportunistically adds robustness against failures due to silicon defects without impacting area or incurring new design rule violations. Implementation details of this redundancy insertion method will be explained in this paper.

One known challenge with similar DFM layout fixing methods is the possible introduction of undesired electrical impact, causing other unintentional failures in design functionality. In this paper, a study is presented to quantify the electrical impacts of such redundancy insertion scheme and to examine if that electrical impact can be tolerated. The paper will show results to evaluate DFM insertion rates and corresponding electrical impact for a given design utilization and maximum inserted wire length. Parasitic extraction and static timing analysis results will be presented. A typical digital design implemented using GLOBALFOUNDRIES 7nm technology is used for demonstration.

The provided results can help evaluate such extensive DFM insertion method from an electrical standpoint. Furthermore, the results could provide guidance on how to implement the proposed method of adding electrical redundancy such that intolerable electrical impacts could be avoided.

10148-23, Session 7

Selection of airgap layers for circuit timing optimization

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Airgap refers to air being used together with some material (i.e. material has intentional void) as inter metal dielectric (IMD). It is formed following below steps. After the formation of standard Cu interconnect, IMD between metal lines is removed. Two consecutive depositions are applied: conformal dielectric deposition using atomic layer deposition (ALD) for sidewall passivation of metal lines (this is to prevent Cu being oxidized by air), and non-conformal dielectric deposition using chemical vapor deposition (CVD) to pinch off the top portion of dielectric layer. Airgap brings about reduced IMD permittivity from 2.5 (porous SiOC:H) to below 2.0 (airgap with SiOC:H) and corresponding reduction in coupling capacitance. It has been reported that total wire capacitance including coupling component is reduced by 17% to 28%.

The number of layers that employ airgap, called airgap layers, is practically limited because airgap insertion is an expensive process involving more than 10 additional process steps. Let two airgap layers be permitted. The choice of airgap layers affects circuit timing, specifically our experiment shows the improvement of total negative slack (TNS) for various choices of two example circuits. There is a wide variation of TNS improvement in one circuit, e.g. 29% variation in b19. More importantly, the best choice is different for different circuit, i.e. M2+M3 is the best choice for b19 but M3+M4 is the best for gfx. Systematic method is thus required to choose the best airgap layers, which is the focus of this paper.

We propose an efficient method of selecting airgap layers for each circuit. We first extract information of nets in critical paths, such as driving cell, load capacitance, and input slew. Delay reduction in critical paths (i.e. TNS reduction) from airgap insertion is then calculated for each net using timing

library in which the extracted information is used. Assuming that the effect of capacitance reduction on delay is linear in small capacitance change, we obtain TNS reduction for each metal layer by using metal length ratios. For given airgap layers, we sum up TNS reductions of the layers and select airgap layers which correspond to maximum improvement. This procedure is performed without additional timing analysis, and delay reduction from airgap is calculated once. Finally, we assign wire segments, which belong to other than airgap layers, in critical paths to selected airgap layers, which allows further improvement in TNS.

The proposed method is assessed using 28-nm commercial library. We demonstrate the effectiveness of our method for various circuits in terms of TNS improvement, compared to circuit implementation with predetermined airgap layer.

10148-24, Session 7

Systematic analysis of the timing and power impact of pure lines and cuts routing for multiple patterning

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Patterning based on pure lines and cuts has been extremely effective for gate patterning since the 45-nm node and gridded gate layout has reduced both local and across chip linewidth variation. It is attractive for BEOL due to its amenability to self-aligned double patterning (SADP) and ability (indeed necessity) to integrate the fill step directly. Indeed, the fill is an artifact of floating metals left isolated by cuts to produce the metal routes. Patterning of blocking metal "cuts" rather than a block mask also simplifies the required lithography, akin to via patterning. In addition to the simplified processing, the resulting very regular metal grid significantly reduces metal thickness variation. However, we show here that the design impact is significant. While traditionally, dummy metals have been inserted into the design with careful attention to limiting the performance impact to (ideally) negligible levels, with integrated routing and fill the dummy metal spacing is minimal, and capacitance through the series capacitive paths increases the net delay and power dissipation.

Prior work showed minimal coupling capacitance increase on small benchmarks from post-fill to integrated fill. In this work, we analyze the impact of the integrated route and fill approach on multiple fully implemented auto-place and routed (APR) designs via a predictive 7-nm PDK. The designs are initially implemented assuming SADP BEOL with a conventional 2-D block mask (LELE) and then with fill added to simulate use of a lines and cuts BEOL. Our comparison is from no fill to integrated fill, assuming conventional fill would not impact timing. The impact of integrated fill on capacitance and overall timing is evaluated using Calibre PEX and PrimeTime. We show these results are in line with simple "back of the envelope" estimates and simple models.

On a microprocessor cache ECC generation and correct pipeline stage with 81% cell area utilization, the capacitance increase on a net segment (from gate output to next gate input) ranges from zero to 189%, with a 27% median. Nets with large capacitance tend to have lower increase. Total BEOL capacitance increases 26% and thus, active power dissipation is adversely impacted. Analyzing the same ECC block using RVT cells only, the initial supported clock rate at the typical process corner and nominal voltage is 2.5 GHz. The post fill timing impact is significant, with a worst-case critical path degradation of 3.2% at the typical process corner, with a 4.3% median register to register path degradation, clearly showing that APR tools must be aware of the integrated fill BEOL for proper design optimization. Notably, since the fill primarily increases intra-layer capacitance, line to line cross-coupling and thus noise, is generally reduced with the integrated fill—a large proportion (over 1/5) of the nets have their cross-coupling eliminated by intervening metal, while a small fraction see increases. Moreover, this also suggests that process changes to reduce intra-layer capacitance, e.g., air-gap intra-layer dielectrics are very desirable in a lines/cuts BEOL scheme, which a single spacing may ease.

10148-25, Session 7

Cutting-edge CMP modeling for front-end-of-line (FEOL) and full stack hotspot detection for advanced technologies

Ushasree Katakamsetty, Colin C. W. Hui, Yongfu Li, Jlansheng J. Chee, GLOBALFOUNDRIES Singapore (Singapore)

As the process technology scales down, the number of Chemical Mechanical Polishing (CMP) processes and steps used in chip manufacturing is increasing exponentially. Excessive metal or oxide thickness or topography variations can lead to shrinkage of process windows, causing potential yield problems such as dishing, erosion, resist lifting or printability issues.

Present DFM CMP modeling and applications mainly focus on the hotspot detection and fixing methodology for the Back-End-Of-Line (BEOL) layers1. Today, the present methodology is no longer sufficient to eliminate all the CMP related manufacturing defects. There is a strong demand for STI, poly and contact silicon calibrated CMP models to predict and fix the related CMP hotspots.

Shallow Trench Isolation (STI) and Poly CMP planarity is very critical in advanced technologies with Diffusion layer FIN structures and Replacement Metal Gate Process flow 2. Gate uniformity after CMP step will improve the device performance, reduces CMP defects and increases the yield. Contact (Tungsten) CMP polishing is another importance step that defines contact planarity, which will influence metal layer CMP planarization 3.

This paper discusses on the design dependent CMP variations for STI, Poly and Contact CMP steps and showcases the importance of FEOL CMP modeling. We present the methodology for Silicon calibrated STI CMP, Poly and Contact CMP models and the applications of FEOL CMP models for CMP dishing and erosion hotspot analysis. We also present FEOL plus BEOL multi stack CMP simulations applications and provide design guidelines to fix CMP hotspots.

10148-26, Session 7

Stitch overlap via coloring technique enables maskless via

Deniz E. Civay, Elise Laffosse, GLOBALFOUNDRIES Inc. (United States)

Lithographic patterning limits can be a cost-barrier that delays advancement to new nodes. This paper introduces a cost-saving design method that enables a maskless via. Multi-patterning or coloring of a design is a technique that is used at advanced nodes to aid in patterning. Coloring allows designers to designate different patterns on one level to be printed with different masks. Stitch overlap via (SOV) is a coloring technique introduced herein. SOV utilizes via-aware coloring and a unique process flow to print a maskless via. Identification of qualifying design structures is achieved through a custom program. The program inputs the design level of the multipatterned layer and the via levels above and below to determine the coloring decomposition. Vias are a particularly challenging layer to print due to the dimensions required for these pillars. SOV is a methodology for identifying qualifying multi-patterned layouts and replacing them with a new design that enables a maskless via layer.

10148-27, Session 8

Early stage hotspot analysis through standard cell base random pattern generation

Joong-Won Jeon, Jaewan Song, Jeong-Lim Kim, Seongyul Park, Seung-Hune Yang, Sooryong Lee, SAMSUNG

Electronics Co., Ltd. (Korea, Republic of); Kareem Madkour, Mentor Graphics Egypt (Egypt); Wael ElManhawy, Mentor Graphics Corp. (United States); Seungjo Lee, Mentor Graphics (Korea) LLC. (Korea, Republic of); Joe Kwan, Mentor Graphics Corp. (United States)

Due to limited availability of DRC clean patterns while developing the process and RET, OPC recipes are not fully verified considering pattern coverage. Various kinds of pattern can be used for detecting lithography sensitive patterns and random pattern generation is required to secure robust OPC recipe. However, random patterns without considering real product layout may not cover all patterning hotspots in production levels and also may not be effective for OPC optimization, thus it is important to generate random patterns representing all real product patterns.

This paper presents a strategy for generating random patterns based on design architecture information and preventing hotspot in early process development stage through a tool called Layout Schema Generator (LSG).

The standard cells generated by LSG are applied to an analysis methodology to assess their hotspot severity and those patterns are categorized by assigning a severity score according to their optical image parameters - NILS, MEEF, %PV band. Finally potential hotspots can be determined by their ranking.

This flow is demonstrated on advanced logic technology optimizing OPC recipe to avoid problematic patterns at early development stage.

10148-28, Session 8

Design space sampling using hierarchical clustering of patterns on a full chip

Andrey Lutich, GLOBALFOUNDRIES Dresden Module Two, GmbH & Co. KG (Germany)

This research considers the problem of sampling the design space of a given layout and extracting a set of characteristic design patterns uniformly distributed within the design space occupied by the layout. There are many potential applications and use cases where the design space sampling plays a key role. Often, it is used as a powerful tool to identify and classify lithography weak spots. However in this work, we approach this problem from a completely different prospective. Namely, from the manufacturing process setup, fine-tuning and change management point of view. In this context, adequate design space sampling and comprehensive understanding of the possible design configurations is essential for development and maintenance of the manufacturing process in general and OPC components and algorithms in particular. Typical scenario in a semiconductor manufacturing facility is when a representative set of design locations (on existing product or test site) needs to be delivered to the process/integration/modelling/OPC teams for various purposes. The most usual use cases include:

- verification and monitoring of the changes in the manufacturing process (resist changes, stack adjustment, etch process fine-tuning etc)
- model (resist/etch/...) build and verification
- optimization and verification of the illumination source performance
- SRAF and OPC recipe optimization
- design outliers/anomalies detection: finding design spots that are very different from others

The method that we developed to extract coordinates of the representative design patterns on a given layout consists of three essential steps:

- extraction of patterns and construction of feature vectors
- run hierarchical clustering on extracted set of feature vectors
- select features (and their coordinates) representing the clusters

The process flow and the infographics in Figure 1 sketch the steps listed above. First, the input design layout is scanned through and converted into a set of feature vectors that define individual patterns X = (X1, X2, ... , Xm) . For example, these could be distances, angles, areas of individual pattern sub-components, overlay, enclosure or any other metrics.

For example, for hole-like layers extracted patterns are centered on the holes and the following format of feature vectors could be used:

X = (A0, {A1, D1}, {A2, D2}, ... , {An, Dn}),

where A0 – area of the via/contact itself, pairs {Ax, Dx} are the area and distance of/to the neighboring vias, sorted in ascending order.

After a set of feature vectors has been extracted from an input layout, the hierarchical clustering is executed on the set of these vectors. Direct application of the hierarchical clustering algorithm to billions of features extracted from large designs is not feasible due to memory constraints. To overcome this limitation we have developed a customized version of it, which enables full-chip hierarchical clustering execution.

The method presented here has been successfully applied during 22FDX process development to contact and via design layers and helped identify and fix potential process weaknesses. In the presentation, we will cover in detail feature construction for hole-like layers, customized hierarchical clustering method as well as final pattern selection criteria.

10148-29, Session 8

A fuzzy pattern matching method based on graph kernel for lithography hotspot detection

Izumi Nitta, Yuzi Kanazawa, Tsutomu Ishida, Fujitsu Labs., Ltd. (Japan); Koji Banno, Socionext Inc. (Japan)

In advanced technology nodes, increasing sub-wavelength lithography gap causes unexpected shape distortions of the printed layout patterns called lithography hotspot. Although layout pattern is verified by design rule checking and optical proximity correction in physical verification phase, hotspot may still exist. Lithography hotspot detection has become one of the most important techniques in design for manufacturability.

Lithography hotspot detection techniques are classified into following categories: (1) lithography simulation, (2) exact pattern matching, and (3) machine learning based pattern matching. Lithography simulation can detect hotspots accurately but its running time is long. Exact pattern matching is fast but not good at detecting unknown hotspot patterns. To achieve the balance between runtime and accuracy, machine learning based techniques have been proposed. In machine learning approach, a classification model is constructed by training known patterns, and then, using the model, hotspots are detected from a testing layout. Traditional machine learning approaches with artificial neural network or support vector machine have tradeoffs between accuracy and false alarm. To improve accuracy with low false alarm, feature selection is significant. Therefore, many characterization methods of layout patterns have been proposed but it is still difficult to define optimal feature set. Deep neural network is expected to solve the feature selection problem because it optimizes feature set automatically during model construction. However, deep neural network method currently has some issues on runtime, machine-resources, and parameter tunings.

To apply the machine learning based method to the physical verification, the following two points are significant; (1) the hotspot detection method is required to minimize undetected hotspots to avoid yield degradation, and (2) designers have to confirm whether each detected hotspot is true or not because the machine learning based method provides only candidate hotspots. In such confirmation phase, designers may wish to know the similarity between a candidate hotspot pattern and the known hotspot pattern from training data set as a confidence level of the candidate hotspot.

In this paper, we propose a novel lithography hotspot detection method to minimize undetected hotspots and to provide similarity between two patterns. Our main contributions are as follows: (1) We utilize Delaunay triangulation which characterizes neighborhood connections of figures to extract appropriate features of hotspot patterns where polygons locate irregularly and closely one another. (2) We propose the graph kernel based machine learning technique to detect hotspot pattern from a graph of

Delaunay triangulation of a layout pattern. Graph kernel expresses inner structure of graph and is good at detecting subgraph which is related to hotspot pattern. (3) Using graph kernel, we also calculate similarity between two patterns and create a ranking of similar known patterns with a testing pattern which helps designers judge whether a detected hotspot is true or not.

Experiments results on ICCAD 2012 Contest benchmarks show that our method achieves high accuracy while false alarm rate is almost the same as those of previous methods. We also show some examples of the ranking of similar training pattern with detected hotspot patterns.

10148-30, Session 8

Design and pitch scaling for affordable node transition and EUV insertion scenario

Ryoung-Han Kim, Julien Ryckaert, Praveen Raghavan, Syed Muhammad Yasser Sherazi, Peter Debacker, Darko Trivkovic, Werner Gillijns, Ling Ee Tan, Youssef Drissi, Victor M. Blanco Carballo, Joost P. Bekaert, Ming Mao, Stephane Larivière, Gregory R. McIntyre, IMEC (Belgium)

IMEC progress on foundry N5-equivalent technology node develop is reported in broad perspective with a focus on patterning on top of design technology co-optimization (DTCO). We show how 33% wafer cost increase without a design scaling becomes a challenge in technology node transition, and propose a paradigm shift from pitch-only scaling to design-assisted pitch scaling to provide affordable patterning scheme while meeting cost and area scaling target. It is shown that the standard cell height from 9-track to 5-track by using scaling boosters such as CPP:M1 gear ratio, self-aligned gate contact, M1 open architecture as well as new SRAM cell design can be effectively achieve area scaling target when combined with pitch scaling. In parallel, EUV insertion scenario which encapsulates single patterning metal, metal block with iArF SAQP, and Via is discussed in combination with IMEC roadmap and technology develop status in patterning/integration and computational lithography.

10148-31, Session 8

Transforming information from silicon testing and design characterization into numerical data sets for yield learning

Yang Shen, Thomas Yang, Semiconductor Manufacturing International Corp. (China); Yifan Zhang, Cadence Design Systems, Inc. (China)

Silicon testing results are regularly collected for a particular lot of wafers to study yield loss from test result diagnostics. Product engineers will analyze the diagnostic results and perform a number of physical failure analyses to detect systematic defects which cause yield loss for these sets of wafers in order to feedback the information to process engineers for process improvements. Most of time, the systematic defects that are detected are only major issues or one of the causes for the overall yield loss.

This paper will present a working flow for using design analysis techniques combined with diagnostic methods to systematically transform silicon testing information into physical layout information. A new set of the testing results are received from a new lot of wafers for the same product. We can then correlate all the diagnostic results from different periods of time to check which blocks or nets have been highlighted and stop occurring on the failure reports in order to monitor process changes which impact the yield. The design characteristic analysis flow is also implemented to find the critical path on a design that has failed electrical test or frequently used cells that been highlighted multiple times.

Conference 10149: Advanced Etch Technology for Nanopatterning VI

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10149-1, Session 1

Where do we go now? The opportunities for semiconductor technology innovation and growth *(Keynote Presentation)*

George A. Gomba, GLOBALFOUNDRIES Inc. (United States)

No Abstract Available

10149-2, Session 1

Patterning challenges for new computer architectures and devices *(Keynote Presentation)*

Heike Riel, IBM Thomas J. Watson Research Ctr. (United States)

No Abstract Available

10149-3, Session 1

The N3XT technology for brain-inspired computing *(Keynote Presentation)*

H. S. P. Wong, Stanford Univ. (United States)

21st century information technology (IT) must process, understand, classify, and organize vast amount of data in real-time. 21st century applications will be dominated by memory-centric computing operating on Tbytes of active data with little data locality. At the same time, massively redundant sensor arrays sampling the world around us will give humans the perception of additional "senses" blurring the boundary between biological, physical, and cyber worlds. Abundant-data processing, which comprises real-time big-data analytics and the processing of perceptual data in wearable devices, clearly demands computation efficiencies well beyond what can be achieved through business as usual.

Advances in brain-inspired computing are making rapid progress to meet the demands of abundant-data processing using a variety of techniques, including spiking neural networks, hyper-dimensional computing using sparse vectors, deep neural nets, deep belief nets, restricted Boltzmann machines, and their variants. It is therefore crucial to create a scalable and flexible brain-inspired technology platform that can support all the essential elements, and can be adapted for a wide variety of neural computational model.

The key elements of a scalable, fast, and energy-efficient computation platform that may provide another 1,000x in computing performance (energy-execution time product) for future computing workloads are [1]: massive on-chip memory co-located with highly energy-efficient computation, enabled by monolithic 3D integration using ultra-dense and fine-grained massive connectivity. There will be multiple layers of analog and digital memories interleaved with computing logic, sensors, and application-specific devices. We call this technology platform N3XT-Nanoengineered Computing Systems Technology. N3XT will support computing architectures that embrace sparsity, stochasticity, and device variability.

In this talk, I will give an overview of nanoscale memory and logic technologies for implementing N3XT. In particular, I give an overview of the use of nanoscale analog non-volatile memory devices for implementing brain-inspired computing [2]. Phase change memory (PCM) and resistive switching memory (RRAM) are used as examples to illustrate the need to co-design, co-optimize the device technology, circuit design, system architecture, and learning algorithms.

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10149-4, Session 2

Impact of materials engineering on EPE *(Invited Paper)*

Regina Freed, Uday Mitra, Ying Zhang, Applied Materials, Inc. (United States)

Transistor scaling has transitioned from wavelength scaling to multi-patterning techniques, due to the resolution limits of immersion of immersion lithography. Deposition and etch have enabled scaling in the by means of SADP and SAQP. Spacer based patterning enables extremely small linewidths, sufficient for several future generations of transistors. However, aligning layers in Z-direction, as well as aligning cut and via patterning layers, is becoming a road-block due to global and local feature variation and fidelity. This presentation will highlight the impact of deposition and etch on this feature alignment (EPE) and illustrate potential paths toward lowering EPE using material engineering.

10149-5, Session 2

Overcoming patterning challenges related to EUV defined lithography *(Invited Paper)*

Andrew W. Metz, Hongyun Cottle, TEL Technology Ctr., America, LLC (United States); Masanobu Honda, Shinya Morikita, Tokyo Electron Miyagi Ltd. (Japan); Kaushik A. Kumar, Peter Biolsi, TEL Technology Ctr., America, LLC (United States)

Research and development activities related to Extreme Ultra Violet [EUV] defined patterning continue to grow for < 40 nm pitch applications. The confluence of high cost and extreme process control challenges of Self-Aligned Quad Patterning [SAQP] with continued momentum for EUV ecosystem readiness could provide cost advantages in addition to improved intra-level overlay performance relative to multiple patterning approaches. However, Line Edge Roughness [LER] and Line Width Roughness [LWR] performance of EUV defined resist images are still far from meeting technology needs or ITRS spec performance. Furthermore, extreme resist height scaling to mitigate flop over exacerbates the plasma etch trade-offs related to traditional approaches of PR smoothing, descum implementation and maintaining 2D aspect ratios of short lines or elliptical contacts concurrent with ultra-high photo resist [PR] selectivity. In this paper we

will discuss sources of LER/LWR, impact of material choice, integration, and innovative plasma process techniques and describe how TEL™ Vigus™ CCP Etchers can enhance PR selectivity, reduce LER/LWR, and maintain 2D aspect ratio of incoming patterns. Beyond traditional process approaches this paper will show the utility of: [1] DC Superposition in enhancing EUV resist hardening and selectivity, increasing resistance to stress induced PR line wiggle caused by CFx passivation, and mitigating organic planarizer wiggle; [2] Quasi Atomic Layer Etch [Q-ALE] for ARC open eliminating the tradeoffs between selectivity, CD, and shrink ratio control; and [3] ALD+Etch FUSION technology for feature independent CD shrink and LER reduction. Applicability of these concepts back transferred to 193i based lithography is also confirmed.

10149-6, Session 2

Nanoscale damascene processes for patterning and devices fabrication *(Invited Paper)*

Serge Ecoffey, Univ. de Sherbrooke (Canada)

No Abstract Available

10149-7, Session 2

Self-aligned block technology: a step toward further scaling

Frederic Lazzarino, IMEC (Belgium); Nihar Mohanty, Lior Huli, Vinh Luong, TEL Technology Ctr., America, LLC (United States); Marc Demand, Tokyo Electron Europe Ltd. (Belgium); Victor Vega-Gonzalez, IMEC (Belgium); Carlos Fonseca, Kaushik A. Kumar, Kathleen Nafus, TEL Technology Ctr., America, LLC (United States); Julien Ryckaert, Ryoung-Han Kim, Philippe Leray, Chris Wilson, Jürgen Bömmels, IMEC (Belgium); Anton Devilliers, Jeffrey T. Smith, Julie Bannister, Steven A. Scheer, TEL Technology Ctr., America, LLC (United States); Zsolt Tokei, Daniele Piumi, Kathy Barla, IMEC (Belgium)

Year after year, the semiconductor industry overcomes a tremendous amount of technical challenges to satisfy Moore's law. Through innovative device architectures, smart design, new integration and patterning concepts, better tools and new materials, the industry has successfully reached the 7-nm technology node. Both design and patterning options are identified and the High Volume Manufacturing (HVM) readiness is expected end of 2018. Meanwhile, the industry is preparing for the 5-nm technology node targeting a metal 2 pitch in the region of 32-nm for a contacted poly pitch close to 42-nm. At such tight pitches and considering only a full 193i flow, the standard Spacer Assisted Double Patterning (SADP) gives way to the Spacer Assisted Quadruple Patterning (SAQP) where a triple Litho-Etch (LE) is required to pattern both block and via layers. The multiple LE approach enables the realization of a dense blocking scheme but has some disadvantages mainly related to the mask multiplication. It significantly impacts the cost, increases process complexity and has serious repercussions on the Edge Placement Error (EPE) budget. Hence, Extreme Ultra Violet (EUV) lithography remains naturally the preferred patterning option. However, considering that the EUV source is not yet ready for HVM, other solutions to reduce process variabilities must be considered. Besides the improvement of unidirectional design to reduce the active area, fully exploiting self-alignment seems to be a viable path to regain performances and enable further scaling.

In this work, we present and compare two integration approaches to enable self-alignment of the block suitable for the 5-nm technology node. In the first part, the concept and the motivation will be discussed considering the effects on both design and mask count as well as the impact on process complexity and EPE budget. We will go through the integration schemes under consideration, we will compare them and discuss the requirements to enable self-alignment in both cases (filling and surface leveling material capability, layer stability over the different processing, etch selectivity and anisotropy, overall defectivity). In a second part, we will go through the details of both materials and processes selection to allow optimal selective etches and we will demonstrate the proof of concept using a 16-nm half-pitch BEOL vehicle. Finally, the EPE performance and process capability of both integration schemes will be evaluated by means of CD-SEM on-product measurements

10149-9, Session 3

Impact of VUV photons on performance of patterning processes *(Invited Paper)*

Olivier Joubert, Lab. des Technologies de La Microélectronique (France)

No Abstract Available

10149-10, Session 3

Low-frequency roughness mitigation on N7/N5 fin patterning *(Invited Paper)*

Efrain Altamirano-Sánchez, IMEC (Belgium)

No Abstract Available

10149-11, Session 3

Closed-loop control of low-pressure plasma processes *(Invited Paper)*

Miles Turner, National Ctr. for Plasma Science & Technology (Ireland)

No Abstract Available

10149-12, Session 3

3D CDSEM characterization of advanced sidewall patterning process

Shimon Levi, Applied Materials, Ltd. (Israel); Ying Zhang, Applied Materials, Inc. (United States)

Sidewall image transfer has become a key enabler of future design shrink. It is consisted of several process steps that multiply the number of lithography backbone patterns in a self-aligned form, shrinking pattern and pitch sizes.

The quality of the image transfer process depends on the characteristics of the sidewall pattern morphology. Rectangular Sidewalls with a flat top and vertical edges will result with symmetrical and uniform etched image. On the other hand, Facet top, bent sidewalls, sloped edges or foot, may distort the etched image and device electrical characteristics.

In this paper we present a description of the 3DSEM metrology technique used and simulation results. We demonstrate three dimensional characterization of Sidewalls pattern fabricated with different etch recipes:

o Top Facet measurements vs cross section images

o Spacer edge slop and oxide recess characterization

10149-13, Session 4

Silicon photonics and challenges for fabrication *(Invited Paper)*

Natalie Feilchenfeld, GLOBALFOUNDRIES Inc. (United States)

No Abstract Available

10149-14, Session 4

Ultra-high aspect ratio nanopores in silicon by DRIE as photonic nanostructures

Diana A. Grishina, Cornelis A. M. Harteveld, Willem L. Vos, Univ. Twente (Netherlands)

Recent developments in nanofabrication techniques are key factors that enable the growth of nanotechnology and its applications in devices. Silicon processing as a main material for modern CMOS industry attracts particular attention. Growing attention for three-dimensional devices requires creative approaches in their fabrication. One of the challenges related to the increasing dimensionality of the devices is the fabrication of structures in silicon with a high aspect ratio.

One of the most used tools for high aspect ratio (HAR) fabrication in silicon is a deep reactive ion etching (DRIE). A plasma etching equipment for high aspect ratio etching is typically featured with capacitive coupled plasma source (CCP) and inductively coupled plasma source (ICP) for separate control of ion energy and ion density respectively. The process used for the fabrication of deep structures in silicon is a two-step process and is called Bosch process [1]. In this process the etching step and the protective deposition step are continuously alternated. Careful manipulation of both etching and deposition steps as well as gas flows in the etching chamber is required to achieve deep structures. The Bosch process is known to be aspect ratio dependent thus the maximum achievable depth of the etched structure depends on its diameter. Most of the reported HAR structures etched by DRIE are trenches with dimensions in nanometer scale in two directions and large extent in third direction [2]. But difficulties arise when the etched feature is limited in all three directions such as in case of cylindrical pores. Cylindrical pores are important building blocks both for photonics and CMOS industry.

Here we present nanopores with the highest aspect ratios in silicon, etched by means of DRIE[3]. The etched structures have diameter of 510 nm and depth of 21.5 microns resulting in a high value of aspect ratio of 42.

The advances in the etching of deep pores in silicon brings exciting opportunities for both two-dimensional and three-dimensional silicon fabrication in the areas of photonic crystals, sensing, solar cells, high-frequency electronics and many others [3,4].

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10149-15, Session 4

Reducing LER in Si and SiN through RIE optimization for photonic waveguide applications

Nathan Marchack, Marwan H. Khater, Jason S. Orcutt, IBM Thomas J. Watson Research Ctr. (United States); Josephine Chang, IBM Thomas J. Watson Research Ctr. (United States) and Northrop Grumman Corp. (United States); Steven J. Holmes, Tymon Barwicz, Swetha Kamlapurkar, William M. J. Green, Sebastian U. Engelmann, IBM Thomas J. Watson Research Ctr. (United States)

The role of integrated circuit manufacture in growing technology focus topics such as Big Data/Analytics/Internet Of Things is not limited to improved processing power for vast quantities of data. Developing high-efficiency, low cost sensor technologies to gather information from the surroundings, such as sensing chemical concentrations in the environment, is crucial for facilitating reliable source data collection. Silicon waveguide technology has demonstrated much promise to supplant existing interconnect structures for future technology applications, and has potential uses in such sensor technology. However, it is imperative to demonstrate reduced LER in these waveguides to reduce signal transmission loss and improve device efficiency. We have demonstrated characterization of LER through each step of the fabrication process, and showed how the mask open step plays a key role in LER reduction (enabling ~25% reduction for isolated lines and 55% reduction for array features @ 400nm pitch – final LER of 3.4 and 2.5 respectively) and present the effect on transmission loss of increasing LER. We compare the devices fabricated through subtractive patterning to those generated through oxidation of Si, and also discuss a possible combination of these schemes. We also show extension of low-LER patterning to another material system of interest, SiN, using an advanced RIE chemistry.

10149-16, Session 4

Plasma-induced damage during InP patterning for photonic applications

Guillaume Gay, Erwine Pargon, Camille Petit-Etienne, Sébastien Labau, Lab. des Technologies de La Microélectronique, Ctr. National de la Recherche Scientifique (France) and Univ. Grenoble Alpes (France) and CEA-LETI (France); Eugénie Martinez, CEA-LETI (France); Jean-Pierre Landesman, Institut de Physique de Rennes, Univ. de Rennes 1 (France); Juan Jimenéz, Univ. de Valladolid (Spain); Mélisa Brihoum, Sébastien Barnola, CEA-LETI (France)

The cointegration of III-V active photonic components with standard silicon-based CMOS devices paves the way for the fabrication of innovative photonic integrated circuits. To complete this integration, the development of plasma etching processes dedicated to the In-based laser patterning is necessary. The major challenges are the realization of vertical sidewalls with a high quality surface (roughness and respect of stoichiometry), and high selectivity towards the SOI substrate. This work is dedicated to the characterization of damage induced by the plasma patterning on the InP pattern sidewalls, and to evaluate restoration process.

We have studied the plasma etching of InP with Cl2/CH4/Ar chemistry at high temperature (200°C) in an ICP reactor from applied materials. Then, chemical and morphological characterizations were done on the patterned InP ribbons. Open area surface composition is obtained by XPS, while sidewalls composition are probed with SEM-EDX and NanoAuger spectroscopies. Finally, impacts of plasma parameters on ribbons sidewall roughness are measured tilted-AFM, a home-made setup where the sample is tilted to allow the tip to scan the sidewalls. We also propose to investigate restoring processes to mitigate the etch-induced sidewalls damage by combining oxidation and wet removal steps.

We have shown that the presence of silicon oxide is an advantage since it allows for the formation of SiOC passivation layers on pattern sidewalls and leads to excellent anisotropy. However, the presence of silicon also brings drawbacks because it deposits on the InP open area and acts as micromasks responsible for the formation of a grassy surface. Changing Cl2 and CH4 gas

flows, we have found a compromise and demonstrated that a small process window exists where both anisotropy (88.6°) and smooth open area (RMS = 0.3nm) can cohabit. This process also brings high InP etch rate (900 nm/min) and good selectivity toward SiO2 (26). XPS has shown that etched InP open area surface is In-depleted (In/P=0.6). EDX and NanoAuger on the sidewalls have revealed formation of a thick (80 nm) SiOC-like passivation layer with indium incorporated. Several dry and wet treatments were studied to (i) remove properly the passivation layers and leave a clean sidewall InP layer and (ii) restore the InP open-area surface stoichiometry (In/P=1). Concerning the passivation layers, it was shown that an oxygen plasma is necessary to remove the carbon and leave a silicon-rich layer. A subsequent HF bath is then done to etch this residual passivation layer. With regard to open area stoichiometry, we demonstrated that a preliminary oxidation step followed by an HF or an HCl wet treatment selectively removes In and P oxides and leads to a balanced stoichiometry. However, silicon residues are still present and supplementary investigations are needed to solve this issue. Tilted-AFM measurements have demonstrated that LER is reduced by the etching process and that initial lithography mask rugosity (LER=24 nm) is transferred to InP (LER=16 nm). Lastly, we will show preliminary results of SEM-Cathodoluminescence measurements realized on patterned ribbons. Especially, we will correlate defects generated on ribbons sidewalls by the plasma process to light emission spectrum and efficiency.

10149-17, Session 5

Plasma-assisted thermal atomic layer etching of Al_2O_3

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Atomic layer etching (ALE) is a sequential etch process comprised of self-limited reaction steps. One of the drivers for the development of ALE is the need for high selectivity and absence of surface damage after etching /1/. This is critical for patterning of advanced devices such as FinFETs and nanowire transistors today. Increasingly, patterning of electrically passive structures such as mandrels and spacers for multi-patterning requires a similar level of selectivity and damage-free performance to meet advanced critical dimension (CD) control requirements.

Directional ALE with biased plasma removal steps have been explored in great detail and found industrial application /2/. A promising emerging class of ALE to achieve ultimate selectivity is thermal ALE via ligand exchange reactions /3/. While being very selective, thermal reactions can be very sensitive to surface imperfections such as residues. The use of hydrogen or argon plasma step has been shown to remove residues from the surface and yielded an increase of the removal rate in ALE of AlN with HF and Sn(acac)2 /4/. In this paper we explore plasma-assisted thermal ALE to etch Al2O3. The surface is fluorinated with a non-biased fluorine-containing plasma in a first step. The removal is accomplished in a thermal step with Sn(acac)2. When executing this sequence, material removal stops and film growth is observed after only a few cycles. XPS analysis revealed that the newly formed layer is metallic Sn. We propose that Sn is formed when Sn(acac)2 residues fragment upon exposure to the fluorination plasma. Insertion of a hydrogen plasma step removes the Sn layer and continuous material removal of 0.5 Å per cycle is obtained.

The results indicate that the use of targeted plasma steps can enhance thermal ALE, improve repeatability and robustness to surface residues and as a result increase the potential field of use of thermal ALE.

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10149-18, Session 5

Self-aligned quadruple patterning using spacer on spacer integration optimization for N5

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To meet scaling requirements, the semiconductor industry has extended 193nm immersion lithography beyond its minimum pitch limitation using multiple patterning schemes such as self-aligned double patterning, self-aligned quadruple patterning and litho-etch / litho etch iterations. Those techniques have been declined in numerous options in the last few years. Spacer on spacer pitch splitting integration has been proven to show multiple advantages compared to conventional pitch splitting approach. Reducing the number of pattern transfer steps associated with sacrificial layers resulted in significant decrease of cost and an overall simplification of the double pitch split technique.

While demonstrating attractive aspects, SAQP spacer on spacer flow brings challenges of its own. Namely, material set selections and etch chemistry development for adequate selectivities, mandrel shape and spacer shape engineering to improve edge placement error (EPE). In this paper we follow up and extend upon our previous learning and proceed into more details on the robustness of the integration in regards to final pattern transfer and full wafer critical dimension uniformity. Furthermore, since the number of intermediate steps is reduced, one will expect improved uniformity and pitch walking control. This assertion will be verified through a thorough pitch walking analysis.

10149-19, Session 5

Directed self-assembly patterning strategies for phase change memory applications

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Phase change material (PCM)-based memory cells have shown promise as an enabler for low power, high density memory. There is a current need to develop and improve patterning strategies to attain smaller device dimensions, however phase change chalcogenide alloys, such as Ge2Sb2Te5, are prone to processing damage such as from plasma etch, wet clean, encapsulation and annealing. In this paper, two methods of patterning of PCM device structures have been achieved using directed self-assembly (DSA): the formation of a high aspect ratio pore designed for atomic layer deposition of etch damage-free PCM, and pillar formation by image reversal and plasma etch transfer into a PCM film. We demonstrate significant CD reduction (sub-20nm) of a lithographically defined hole by dry etch shrink and DSA and subsequent pattern transfer into a high aspect ratio pore or pillar structure with appropriate hard mask selection and design of the plasma etching process.

10149-20, Session 6

Nanoimprint, DSA, and multi-beam lithography: patterning technologies with new integration challenges *(Invited Paper)*

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In the lithography landscape, extreme-UV (EUV) lithography technology recovered some credibility recently with the release of higher power sources. However, its large adoption remains uncertain, because its infrastructure still requires significant development with pending question about the real associated cost of ownership. Meanwhile, 193nm immersion lithography, with multiple-patterning strategies, supports the industry preference for advanced-node developments, despite the tremendous effort required for process controls. In this landscape, lithography alternatives maintain promise for continued R&D because they may present competitive compromises for the industry. Massively parallel electron-beam and nano-imprint lithography techniques remain highly attractive, as they can provide noteworthy cost-of-ownership benefits. In addition, directed self-assembly (DSA) lithography shows promising resolution capabilities and appears to be an option to reduce multi-patterning strategies, and therefore the associated mask-set budgets. Even if large amount of efforts are dedicated to overcome the lithography side issues of these new patterning solutions, they introduce also new challenges and opportunities for the integration schemes.

Through three collaborative R&D programs, IDEAL for Directed Self-Assembly Lithography, IMAGINE for Massively Parallel Electron Beam Lithography and INSPIRE for NanoImprint Lithography, CEA-Leti is currently assessing and boosting the development of these alternative technologies through strategic partnerships and innovative mix of them.

Directed Self-Assembly (DSA) of Block Copolymers (BCP) is a promising patterning solutions due to its simplicity, low cost of processing and capability to generate high density patterns. Demonstrations of DSA patterning, based on graphoepitaxy processes, for advanced devices in Front and Back-End lines have already been reported [1]. However, some challenges (DSA-friendly design, low defectivity and accurate placement error) need to be addressed for a complete adoption of DSA in manufacturing. We propose to discuss the advanced integration flows using DSA of block copolymer both for PS-PMMA materials but also for high chi next generation materials, like “DSA planarization” approach [2] (Figure 1).

The emerging massively parallel Electron Beam Direct Write (EBDW) is an attractive high resolution-high throughput technology, targeted to address 90 nm to 14 nm technology nodes. CEA-LETI is currently evaluating the pre-production FLX-1200 Mapper platform [3-4], through tool performance assessment, electron beam qualification with embedded metrology and inline metrology. We will provide in this paper an overview of the integration scheme (lithography and etching, Figure 2) required for a 28nm production flow.

Nanoimprint techniques stick out from other more conventional lithography processes (photolithography, electronic lithography, EUV lithography) because of the fundamental mechanism of creating the structures. In classical approaches, they are created through a chemical contrast. In the case of NanoImprint, the contrast is topographic and the flow of the resist through the stamp’s cavities shapes the pattern leading in some case to a non-uniform resist layer thickness underneath the printed features [5]. These characteristics involve to consider specific integration approaches or new transfer processes not always compatible with actual paradigms for 3D printed shapes or high resolution complex patterns (Figure 3).

10149-21, Session 6

Overview of several applications of chemical downstream etching (CDE) for IC manufacturing. advantages and drawbacks versus WET processes *(Invited Paper)*

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Today the IC manufacturing faces lots of problematics linked to the continuous down scaling of printed structures. Some of those issues are related to wet processing, which are often used in the IC manufacturing flow. Indeed the large panel of chemistries, the continuous improvement of the equipment and the needs in term of wafer cleanliness, isotropic etching and surface preparation before epitaxy, makes the wet processing a major actor in IC fabs. As a results it represents more than 30% of the process steps in standard MOS technology.

Nevertheless wet processing has its own limitations.

First, as long as the structures of interest are downsized, they are more and more sensitive to small particles and metallic contamination carried by chemicals.

In addition, MOS technology and its derivatives (DRAM, Flash memories, Imaging sensors, etc...) requires structures with increasing high aspect ratio (HAR). In HAR structures, surface tension forces can lead to collapse of the structure during the wafer drying, and recent works on Si pillars returned that collapse occurred for AR>20. In more critical conditions, wettability of the materials is so low that chemistry is even not able to reach the bottom of the cavities.

Then wet processing using spin on processes can lead to wafer charging and corrosion.

Finally, processes themselves have their own limitation in term of etch rate speed, or selectivity from one material to an other one.

In that context recent progress of CDE methods makes it attractive for all the reasons mentioned above. Indeed particle and metallic contamination are well controlled in such reactors. No mechanical stress is expected in gaseous phases. No more than charging or PID (plasma induced damaged). And CDE can retrieve large etch rate: >300 Å/min for Si3N4 vs. 60Å/min for WET H3P04 at 165°C

We report works that have been done on the use of CDE as a replacement of a wet process for some materials like S3iN4 and silicon. This for critical steps where wet process found its limitation.

First application to be studied is the Nitride Pull Back (NPB). This is a very common step used to enlarge trenches, facilitating its filling by conventional CVD methods. Two reactors were evaluated (denoted as A and B). For both, large etching rate and good uniformity were found. In addition, we obtained satisfying selectivities to SiO2 for both processes. The interest of a protective oxide liner on Silicon will be discussed.

Then we focused on a BEOL sacrificial liner removal for imaging sensors. This liner again made of Si3N4, could not be removed with traditional methods. Indeed RIE caused charging, and wet processing (H3PO4) was unable to remove this material without infiltration towards aluminum pads. Two chambers were evaluated (denoted as A and C). For both, despite surface pitting of PECVD USG (SiO2), we managed to remove nitride layers and get functional devices.

Last, we evaluated the removal of amorphous Si and Si3N4 in HAR trenches. An opportunity to remove Silicon selectively to SiO2, and to remove Si3N4 in small structures. More details will be available in the paper.

10149-22, Session 6

Study of selective chemical downstream plasma etching of silicon nitride and silicon oxide for advanced patterning applications

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Silicon nitride (Si3N4), poly-Si and silicon dioxide (SiO2) are widely used in the elaboration of integrated components in the semiconductor industry. Recent technological developments require to etch those silicon compounds selectively to the others. For example Si3N4 can be easily removed in hot phosphoric acid with excellent selectivity to Si and SiO2. However wet processes present drawbacks including surfaces' wettability, metallic contamination and pattern collapse in dense array of nanostructures ... Plasma etching is also commonly used in the industry, but mainly for anisotropic etching, owing to the directional and energetic ion bombardment of the surface. However, in typical sources (ICP, CCP) the etching selectivity is far to reach the requirements for some processes. For this reasons we have been looking for alternatives such as chemical downstream etching (CDE). The advantages of CDE technology are: no plasma induce damages, isotropic etching and very high selectivities. Several applications are targeted such as the transfer of wet isotropic step by dry etching's steps, selective etching of complex patterns for imagers products.

Etching processes of Si3N4, SiO2 and Poly-Si have been investigated in downstream remote plasma containing perfluorocarbons or nitrogen trifluoride (NF3). NF3 is preferentially used due to wear of the chamber as well as to decrease the global warming effect.

Previous work in the litterature have shown that the etch rate of Si3N4, SiO2 and Poly-Si increase with the flow of NF3 due to the increased availability of F atoms. The presence of O2 in the gas mixture increases the selectivity between SiN and Si/SiO2 but only for specific O2/NF3 ratios. Based on the literature the mechanism responsible for the etching is the following: NO* radicals' react with the SiN surface forming Si-N=N-O. N2 then desorbs, leaving behind O, which bind to Si thus leading to the oxidation of the surface .

The experiments were led on a 300mm commercial (? tool) CDE equipment.

Several DOE (design of experiments) were realized in the aim to screen the silicon nitride and silicon oxide etch rate depending on the gas varieties and their concentrations. After extracting the results given by the DOE we were able confirm the dominant influence of NF3 and O2 . The best selectivity obtained between Si3N4 and SiO2 was 10 for an etch rate of Si3N4 of 30nm/min.

Secondly we analyzed the influence of temperatures (LID, Chuck, wall, cathode) on the etch rate, selectivity and surface's composition, by means of XPS, AFM, ellipsometry. We observed a correlation between the temperature, the etch rate and the surface composition.

_The chuck temperature is the main factor influencing the observed modifications compared to other adjustable parameters for instance.

_ The SiN etch rate increases when the temperature is increased, while at the same time the atomic percentage ratio (Si-N) / (Si-O) rose rapidly. This implies that the SiN surface is strongly oxidized by the etching process at low temperature.. When the temperature is decreased, the oxidation of the surface becomes more efficent and the SiN etch rate decreases. This is strongly suggesting that there is a competition between F and O chemisorption at the SiN surface, and that the formation of Si-O bonds slows down the material etch rate .

Finally, we looked closer to the "passivation" phenomena i.e. the oxidation of SiN by investigating the effect of the gases ratio (NF3/O2) and their impact on the etch rates and the selectivity.

For a low flow of NF3 (50 sccm), shows that the Si3N4 etch rate increase by more than 100 A/min when the O2 flow is increased from 0 to 10 sccm (i.e. for ratio of (O2/NF3) below 0.3) . As the ratio (O2/NF3) exceed 0.3 the Si3N4 etch rate then decrease . In agreement with expectations from the litterature, the initial increase of the etch rate is attributed to an increase of the F atom density in the presence of O2. At higher flow the etch rate eventually decreases due to a competition between etching by F and oxidation by O.

The first results obtained thus concur with the literature, and we will further investigate the different parameters, NF3/O2 ratios and theirs associated flows, Temperature, Pressure, and power source, in order to obtain a higher selectivity.

10149-23, Session 6

Dry-plasma-free chemical etch technique for variability reduction in multi-patterning

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Scaling beyond the 7nm technology node demands significant control over the variability down to a few angstroms, in order to achieve reasonable yield. For example, to meet the current scaling targets it is highly desirable to achieve sub 30nm pitch line/space features at back-end of the line (BEOL) or front end of line (FEOL); uniform and precise contact/hole patterning at middle of line (MOL). One of the quintessential requirements for such precise and possibly self-aligned patterning strategies is superior etch selectivity between the target films while other masks/films are exposed. The need to achieve high etch selectivity becomes more evident for unit process development at MOL and BEOL, as a result of low density films choices (compared to FEOL film choices) due to lower temperature budget. Low etch selectivity with conventional plasma and wet chemical etch techniques, causes significant gouging (un-intended etching of etch stop layer, as shown in Fig 1), high line edge roughness (LER)/line width roughness (LWR), non-uniformity, etc. In certain circumstances this may lead to added downstream process stochastics. Furthermore, conventional plasma etches may also have the added disadvantage of plasma VUV damage and corner rounding (Fig. 1). Finally, the above mentioned factors can potentially compromise edge placement error (EPE) and/or yield.

Therefore a process flow enabled with extremely high selective etches inherent to film properties and/or etch chemistries is a significant advantage. To improve this etch selectivity for certain etch steps during a process flow, we have to implement alternate highly selective, plasma free techniques in conjunction with conventional plasma etches (Fig 2.). In this article, we will present our plasma free, chemical gas phase etch technique using chemistries that have high selectivity towards a spectrum of films owing to the reaction mechanism (as shown Fig 1). Gas phase etches also help eliminate plasma damage to the features during the etch process. Herein we will also demonstrate a test case on how a combination or plasma assisted and plasma free etch techniques has the potential to improve process performance of a 193nm immersion based self aligned quandruple patterning (SAQP) for BEOL compliant films (an example shown in Fig 2). In addition, we will also present on the application of gas etches for (1) profile improvement, (2) selective mandrel pull (3) critical dimension trim of mandrels, with an analysis of advantages over conventional techniques in terms of LER & EPE.

10149-8, Session PSTue

Spin-on metal oxide materials for N7 and beyond patterning applications

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In this work EMD spin on metal oxide layers are presented as alternative hard mask layer for two interesting applications in the context of scaling towards N7 CMOS logic technologies. Current limitation for traditional materials (SiOx, SiN, and aSi etc.) is the reduced process window in terms of selectivity for sub-10 nm technologies. Also cost saving arguments play an important role for replacing traditional CVD Si containing films by metal containing spin on films.

A first application (Fig. 1a) is situated in the SAQP fin patterning module, where two fin cuts have to be executed in a “cut last” approach. The requirements for this patterning step are very challenging in terms of overlay, dry etch profile, etch selectivity and alignment (not discussed in this paper). Since “cut last” happens on a planar substrate, EMD spin on ZrOx can be used as a spin on hard mask below a spin on glass layer, which has several benefits over conventional materials. EMD spin on ZrOx allows processing on the litho track, it allows to increase etch selectivity and we expect to improve alignment and overlay performances compared to conventional Si containing hard mask layers.

A second application (Fig. 1b) can be found in the high temperature ion implantation (450°C) step for extensions (LDD). In order to reduce residual crystalline Si fin damage, increasing the ion implantation process temperature is a way to reduce fin defectivity after activation anneal [1]. Though this approach requires adapted masking materials: e.g. high temperature resistant spin on carbon and spin on glass or metal oxide (TiOx or WOx). The challenge is to selectively strip the masking materials over the FEOL substrates (STI oxide, gate hard mask, Si Fins) at that stage. Replacing the spin on glass hard mask by an EMD spin on metal oxide material, which can be removed in wet chemistry, opens the process window towards the FEOL substrates. It is a cheap solution and allows to target critical CD dimensions in SRAM features.

10149-24, Session PSTue

Improvement of a block co-polymer (PS-b-PDMS) template etch profile using amorphous carbon layer

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Block copolymer (BCP) are consisted of at least two types of monomer which have covalent bonding. The widely investigated BCP is polystyrene-block-polydimethylsiloxane (PS-b-PDMS), which is used as an alternative patterning method for various deep nanoscale devices, such as optical devices and transistors, replacing conventional photolithography. As an alternate or supplementary next-generation lithographic technology to extreme ultra violet lithography (EUVL), BCP lithography utilizing the DSA of BCP has been actively studied. However, the nano-scale BCP mask material is easily damaged by the plasma and has a very low etch selectivity over bottom semiconductor materials, because it is composed of polymeric materials. To achieve high etching selectivity, numerous studies have described the complexation of one block with a heavy element containing BCP or complexation heavy metal into one block of BCPs. In this study, the dry development process enables the maintain high aspect ratio (HAR) of the fine DSA pattern using inserted under-layer such as amorphous carbon layer (ACL). A highly selective etching transferred the PS mask pattern into the silicon/ACL substrate to form HAR silicon trenches using plasma treatment. Be caused by maintain HAR, decrease the increasing LER (line edge roughness) and overcome thickness CD (critical dimension) problem by inserted ACL etching process.

10149-31, Session PSTue

Development of high-dose implanted thick resist stripping processes

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P-N junction formation, whatever the application targeted, implies several implantation steps using a photoresist (PR) mask. During this process, the photoresist is exposed to energetic ion beam leading to surface modifications. The modified layer formed is called the “crust layer” and is very hard to remove by conventional dry strip processes. The photoresist stripping after High Dose Implantation (HDI) is thus becoming a critical step with the increase of both implantation dose (> 1E15 atoms/cm?) and energy (up to 100keV).

The stripping process requirements are even more difficult to fulfill. The PR has to be efficiently removed without any residues on the surface and the impact on both underlying materials and dopants has also to be minimized, in particular the substrate consumption and oxidation as well as the dopants loss and redistribution on the implanted areas.

This paper is dedicated to the development of high dose implanted resist stripping process for photonic applications. It focuses on the stripping efficiency of a 1.4μm-thick 248nm photoresist implanted with phosphorus at 80keV. A solution to remove this photoresist is to use CF4 in the plasma chemistry, which allows to consume the crust layer quickly. However, the use of CF4 is to be avoided because of the high substrate consumption and pitting defectivity on Si substrate. In this work, several CF4-free stripping plasma chemistries (H2-based or O2-based) are evaluated with two values of implantation dose (1 and 5E15 atoms/cm?).

The first tests have been done with N2H2 also called forming gas which is often the best solution in terms of residues and substrate consumption for CMOS technologies. The results show that for all the H2-based plasmas evaluated (N2H2 and He/H2), resist bubbles are formed during the process and explode in the chamber. This phenomenon is called “popping” and leads to defectivity on the wafer surface but also on the stripping chamber walls. The popping phenomenon also occurred with O2-based plasmas but only for resist implanted with very high dose of 5E15 atoms/cm?. Besides, some other residues are left after stripping that can not be removed by a SPM-SC1 wet cleaning.

To understand these results, several techniques (such as ToF-SIMS and nanoindentation) have been used to evaluate the physical and chemical modifications induced by the implantation step in the photoresist. The comparison of implanted photoresist with the two dose values studied allows to propose an explanation of popping phenomenon.

The influence of substrate type (oxide, silicon or nitride) on popping and on residues observed after dry stripping process has also been studied. Substrates do not seem to have an influence on popping but differences have been observed on residues remaining after dry strip process. Indeed, only few residues are observed for nitride compared to oxide or silicon. Additional study is on going to understand the mechanisms and explain the differences observed depending on the substrate type and the chemistry used.

10149-32, Session PSTue

Roughness and uniformity improvements on self-aligned quadruple patterning technique for 10nm node and beyond by wafer stress engineering

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Dimension shrinkage has been the major driving force in development of integrated circuit processing in decades. Due to the delay of extreme ultraviolet (EUV) lithography, Self-Aligned Quadruple Patterning (SAQP) technique is widely adapted for sub-10nm node in order to achieve the desire pitch. This technique provides theoretical possibility of multi-pitch halving from 193nm immersion lithography by using various pattern transferring steps. The major concept of this approach is on spacer defined self-aligned patterning with single lithography print. The pattern mask is defined by the spacer on top of it with half of its original pitch. By repeating of this process steps, double, quadruple, or octuple are possible to be achieved theoretically. At sub-10nm node, roughness and uniformity controls become extremely critical since they may contribute major portion of process variations in such small dimension features. From the characteristics of SAQP with complex processing steps and spacer patterning, the improvements of roughness and uniformity are ineffective and complicated by comparing with traditional direct print method.

In this presentation, we will demonstrate a novel method to improve line roughness and uniformity performances on 30nm pitch SAQP flow. We discover that the line roughness and uniformity performances are strong related to stress management. By applying additional stress to the wafer, we can manipulate the amount and the direction of wafer curvature. This distinct curvature change will impact the physical performance during the pattern transferring steps. We will discuss in details the step-by-step physical performances for each pattern transferring steps in terms of CD/CDU/LWR/LER. At final, we summarize the process in order to reach the full wafer performance targets of LWR/LER/uniformity under 1.3nm/1.3nm/0.6nm on 30nm pitch line and space pattern.

10149-33, Session PSTue

A method to accelerate creation of plasma etch recipes using physics and Bayesian statistics

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Trench profiles for plasma etching are extremely challenging to predict using conventional modeling techniques for a number of reasons. Currently, plasma recipes can have up to ten different gas chemistries meaning hundreds of reactions can take place in a single process in parallel. Adding to the complexity, plasma reactors have many distinct length scales including one for the reaction chamber, wafer, die, and feature. Gradients in species concentrations across each of these length scales and coupling of the species transport processes makes it difficult and computationally expensive to predict molecular fluxes. In addition, most plasmas currently in use exhibit non-Maxwellian behavior making it challenging to determine the velocity distributions of the incoming plasma species to the wafer's surface. Finally, there is a significant lack of knowledge in plasma parameters. Kinetic and material properties like reaction rates and sputtering yields are often unknown and difficult to measure. All of these problems have become exacerbated as technology nodes get smaller and new materials and device structures are explored.

Despite a wide variety of innovative feature and reactor scale models that have been introduced in literature, plasma recipe development today is primarily empirical due to the aforementioned obstacles. In an oftentimes trial and error manner, qualitative relationships based on user experience are used to "tune" etch parameters for existing recipes. Disadvantageously, this approach does not provide for extrapolation to new processes and is costly and time consuming. Accordingly, there is an immediate need for innovation in the plasma etch recipe development process. Here we introduce a software tool called RODEo, which employs Bayesian statistics, flexible plasma models, and experimental data to rapidly develop and optimize recipes for plasma etching.

Using RODEo, we are able to calibrate our models significantly faster than classical design of experiments (DoE) and predict optimal process windows. In this presentation, we first demonstrate this method for predictions of etch rates in CCP and ICP-RIE plasma reactors. The accuracy of these predictions is then compared to synthetic and experimental data. We next use the method to determine the anisotropic etch rates through a single material, high aspect ratio trench using level set modeling. Lastly, we apply the method to the etch recipe development of a high aspect ratio trench through a multi-layer stack. Our results show that we can produce a threefold decrease in the cost and time required to develop an etch recipe. With RODEo we address the inherent difficulties in model calibration for a nonlinear process with a large number of unknown parameters and provide a more informed methodology for plasma etch recipe development.

10149-34, Session PSTue

The line roughness improvement with plasma coating and cure treatment for 193nm lithography and beyond

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As CMOS technology reaches 14nm node and beyond, one of key challenges of the extension of 193nm immersion lithography is how to control the line edge and width roughness (LER/LWR). For Self-aligned Multiple Patterning (SaMP), as the process proceeds, LER becomes larger while LWR becomes smaller [1]. It means plasma etch process becomes more and more dominant for LER reduction. In this work, we mainly focus on the core etch solution including an extra plasma coating process introduced before the barc-open step, and an extra plasma cure process applied right after barc open step. Firstly, we leveraged the optimal design experiment (ODE) to investigate the impact of plasma coating step on LER and identified the optimal condition. ODE is an appropriate method for the screening experiments of non-linear parameters in dynamic process models, especially for high-cost-intensive industry [2]. Finally, we obtained the proper plasma coating treatment condition which has been proven to achieve ~30% LER improvement compared with standard process. Furthermore, the plasma cure scheme has been also optimized with ODE method to cover the LWR degradation induced by plasma coating treatment. The synergic effect of coating and cure scheme on the final step of SaMP has been evaluated with a wiggling LER measurement, which is a latest method of wiggling factor quantification.

Acknowledgments

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10149-35, Session PSTue

The application of advanced pulsed plasma in Fin etch loading improvement

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With the background of general integrated circuit (IC) feature size shrinking designers get high performance transistors, Self-Alignment-Double-Patterning (SADP) FinFET etch was widely used in 14/16 nm technologies node and beyond. Rigorous process loading control (CD, profile, depth) in reactive ion etch (RIE) becomes more critical and challenging to ensure precise patterning and to avoid performance degradation among different features.[1] However, it's quite hard to tackle such notorious loading for its inherent high Te induced ionization in traditional continuous wave (CW) plasmas. Thus, significant improvements in controlling plasma properties in a dry etching reactor are essential to satisfy such stringent requirement.

Pulsed plasmas have demonstrated several advantages compared to CW plasmas. By varying the pulse frequency and the duty cycle, pulsed plasma provide additional "control knobs" in controlling critical plasma parameters, such as ion and electron densities, electron temperature, flux and energy of the ions and radicals incident on surface. These critical factors affecting overall on-wafer performance during plasma etching processes at both within wafer and within die levels. Etching and deposition, vertical and lateral etch rate, profile control, feature sidewall passivation and plasma damage.[2] In view of characters pulsed plasma noted above, it appears to be a promising approach to improve RIE-lag loading SADP fin etch.

In this paper, we systematically investigated the influence of both bias pulsed plasma and synchronous pulsed plasma to fin CD, profile (sidewall angle) and depth loading performance between dense and semi-isolated lines. It was found that proper duty cycle and frequency of pulsed power could drastically impact the loading performance. Based on the above learning, we finally delivered the overall solution by introducing synchronous pulsed plasma etch in mandrel and shallow trench isolation (STI) to address the rigorous loading control between dense and isolated patterns.

10149-37, Session PSTue

Facile fabrication of Si-based nanostructures

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In this work, we present an attractive and innovative fabrication technique of Si-based nanostructures over a large area by a novel material, amorphous silicon (?-Si). Previously, it is well known that this material has attracted considerable interest of thousands and thousands of scientists and engineers, who, over the years, have widely used it in a variety of applications from in a broad variety of applications especially in energy storage devices from photovoltaics to thin film transistors (TFTs) in flat-panel displays. However, to the best of our knowledge, although ?-Si material has obtained a wide application in semiconductor industry, it has not been investigated yet as a novel mask for fabricating various Si-based nanostructures until now.

Here, several typical Si-based nanostructures, such as nanoline, nanofin and transistor gate patterning, have been fabricated successfully using the simple ?-Si material as a mask layer. The etched ?-Si mask nanopatterns are precisely transferred into the underlying dielectrics substrate material with a high fidelity using an appropriate pattern transfer process.

Moreover, it is observed that the ?-Si is very helpful for significantly reducing the pattern edge roughness and achieving highly uniform and smooth sidewalls. By controlling the process conditions, it is also possible to achieve a desired vertical or tapered etched profile with a controlled size. Our results demonstrate that the SiO2 nanostructures as small as sub-20 nm may be achievable. The obtained SiO2 nanopatterns can be further used as a nanotemplate to produce simple or more complex silicon nanostructures. The novel top-down technique offers a greater flexibility towards the fabrication of cost-effective nanoelectronic and optoelectronic devices in a simple and efficient way.

10149-25, Session 7

Co-optimization of lithographic and patterning processes for improved EPE performance *(Invited Paper)*

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Complementary lithography is expected to be used for advanced logic patterns for N7. This means that the tight pitches for 1D Metal layers are expected to be created using spacer based multiple patterning ArFi exposures, and the more complex cuts and blocks are created using EUV exposures. At the same time, control requirements of CDU, pattern shift and pitch-walk are approaching sub-nanometer levels to meet edge placement error (EPE) requirements. Local variability, such as LER, Local CDU, and LPE, are dominant factors in the total Edge Placement error budget. From the scanner side, improving the imaging contrast when printing the core pattern has been shown to improve the local variability. From the etching side, it was shown that the fusion of atomic level etching and deposition can also improve these local variations [1] [2]. Co-optimization of lithography and etch processing is expected to further improve the performance over individual optimizations alone.

To meet the scaling requirements and keep process complexity to a minimum, EUV is increasingly seen as the platform for delivering the exposures for both the grating and the cut/block patterns beyond N7. In this work, we evaluated the overlay and pattern fidelity of an EUV block/cut on an SAQP grating. Overlay errors remain a key contributor to the EPE budget. High-order modeling and corrections during the exposure can reduce overlay error after development. During the etching process, additional degrees of freedom are available to improve the pattern placement error in single layer processes [3].

Process control of advanced pitch nanoscale-multi-patterning techniques as described above is exceedingly complicated in a high volume manufacturing environment. Incorporating potential ALE/ALD optimizations into both design and HVM controls for the lithography process is expected to bring a combined benefit over individual optimizations. In this work we will show the EPE performance improvement for a 32nm pitch SAQP + SE EUV Block patterning layer with co-optimized lithography and etch processes. Comparison of EPE performance of multiple etch process options will also be shown.

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10149-26, Session 7

Self-aligned blocking integration demonstration for critical sub-40nm pitch Mx level patterning

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Multipatterning has enabled continued scaling of chip technology at the 28nm node and beyond. Self-aligned double patterning (SADP) and self-aligned quadruple patterning (SAQP) as well as Litho-Etch/Litho-Etch

(LELE) iterations are widely used in the semiconductor industry to enable patterning at sub 193 immersion lithography resolutions for layers such as FIN, Gate and critical Metal lines. Multipatterning requires the use of multiple masks which is costly and increases process complexity as well as edge placement error variation driven mostly by overlay. To mitigate the strict overlay requirements for advanced technology nodes (N10 and below), a self-aligned blocking integration is desirable. This integration trades off the overlay requirement for a selectivity requirement and enables the cut mask overlay tolerance to be relaxed from half pitch to three times half pitch. Self-alignment has become the latest trend to enable scaling and self-aligned integrations are being pursued and investigated for various critical layers such as contact, via, metal patterning.

In this paper we propose and demonstrate a low cost flexible self-aligned blocking strategy for critical metal layer patterning for N10 and beyond from mask assembly to low –K etch . The integration is based on a 40nm pitch SADP flow with 2 cut masks compatible with either cut or block integration and employs films widely used in the BEOL such as SiO2, Si3N4, SOG and SOC. As a consequence this approach is compatible with traditional etch, deposition and cleans tools that are optimized for dielectric etches resulting in significant cost savings. We will review the critical steps and selectivities required to enable this integration along with bench-marking of each integration option (cut vs. block).

10149-27, Session 8

New challenging wafer architecture patterning *(Invited Paper)*

Laura Castoldi, STMicroelectronics (Italy)

No Abstract Available

10149-29, Session 8

Plasma processing of III-V materials for energy efficient electronics applications *(Invited Paper)*

Iain Thayne, Univ. of Glasgow (United Kingdom)

This presentation is a review of some recent activity at the James Watt Nanofabrication Centre in the University of Glasgow in the area of plasma processing for energy efficient compound semiconductor-based transistors. Atomic layer etching for controllable recess etching in GaN power transitors and antimonide-based nanowire sidewall cleaning. Recent results of a cyclic atomic layer etching process utilising a Cl2/Ar chemistry for GaN power transistor applications will be presented. Extension of this work using an HBr/Ar chemistry for InGaAs and InGaSb etched vertical nanowires will also be described. For reduced thermal budget source-drain formation in GaN power devices (< 600C), a SiCl4-based recess etch process incorporating a silane “flash” will be reported. In the area of surface passivation, the use of post-etch H2 plasma cleansfor improving the CV response of InGaAs and InGaSb vertically etched nanowires will be presented and finally some studies on the impact of the stress of SiN passivation coatings on surface leakage currents in GaN power devices will be mentioned.

10149-30, Session 8

Fabrication of SF6 gas sensor by inductively coupled plasma etching and ASML stepper

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The absorption of SF6 gas is of narrow band and peaks at 10.6μm. This narrow band absorption posts a stringent requirement on the corresponding sensors as they need to collect enough signals from this limited spectral range to maintain a high sensitivity. Resonator-Quantum Well Infrared Photo detectors (R-QWIPs) are the next generation of QWIP detectors that use resonances to increase the quantum efficiency (QE) for more efficient signal collection. Since the resonant approach is applicable to narrowband as well as broadband, it is particularly suitable for this application. We designed and fabricated a R-QWIP for SF6 gas detection and the initial test results showed promising results. To achieve the expected performance, the detector geometry must be produced in precise specification. In particular, the height of the diffractive elements (DE) and the thickness of the active resonator must be uniformly and accurately realized to within 0.05 um accuracy and the substrates of the detectors have to be removed totally to prevent the escape of unabsorbed light in the detectors. To achieve these specifications, two optimized inductively coupled plasma (ICP) etching processes are developed. Due to submicron detector feature sizes and overlay tolerance, we use an ASML stepper instead of a contact mask aligner to pattern wafers. Using these etching techniques and the tool, we have fabricated FPAs with 30 μm pixel pitches and 320x256 format. The detail of the fabrication and their characteristics will be presented.

10149-36, Session 8

Guiding gate-etch process development using 3D surface reaction modeling for 7nm and beyond *(Invited Paper)*

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Increasingly, advanced process nodes such as 7nm (N7) are fundamentally 3D and require stringent control of critical dimensions over high aspect ratio features. Process integration in these nodes requires a deep understanding of complex physical mechanisms that contribute to critical dimension control from lithography through final etch.

Polysilicon gate etch processes are critical steps in several device architectures for advanced nodes employing self-aligned patterning approaches to gate definition. These processes are required to meet several key metrics: (a) vertical etch profiles over high aspect ratios; (b) clean gate sidewalls free of etch process residue; (c) minimal damage to liner oxide films protecting key architectural elements such as fins; and (e) residue free corners at gate interfaces with critical device elements.

In this study, we report on a multi-step finFET polysilicon gate etch process modeling using a Particle Monte Carlo (PMC) based surface reaction approach [1]. When necessary, species and energy flux inputs to the PMC model are derived from simulations of the etch chamber. The polysilicon gate etch process modeled consists of several steps including a hard mask breakthrough step (BT), main feature etch steps (ME), and over-etch steps (OE) that control gate profiles at the gate fin interface. An additional constraint on this etch flow is that fin spacer oxides are left intact after final profile tuning steps. A natural optimization required from these processes is to maximize vertical gate profiles while minimizing damage to fin spacer films [2].

Chemistries required for each step are translated into a set of surface reactions that capture incident radical and ion fluxes on exposed surfaces. These reactions will result in a time dependent exposed-surface evolution. Different etching and deposition mechanisms such as ion assisted etch and passivation/inhibition through radicals, are modeled. Process recipes for each step are coupled with STEM image data collected during process development to construct feature scale models. In addition, STEM data provide a point of comparison to the simulation results after each step as well as boundary conditions for subsequent steps in the overall flow.

The entire sequence of process models developed are then used to study

the impact of process condition variation (e.g. change in operating pressure) on gate structure topography. In particular, results of variations in key process steps can be used to assess their impact on profile verticality, residue build-up on sidewall surfaces, and the deposition of residual or damage to fins. In addition, the OE step induced damage of the fins or of the oxide layer protecting fins is studied as a dependence of the ion angular distribution of the etching ion flux (controlled by the operating pressure), giving insight into the sensitivity of fin damage to process parameter changes.

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