

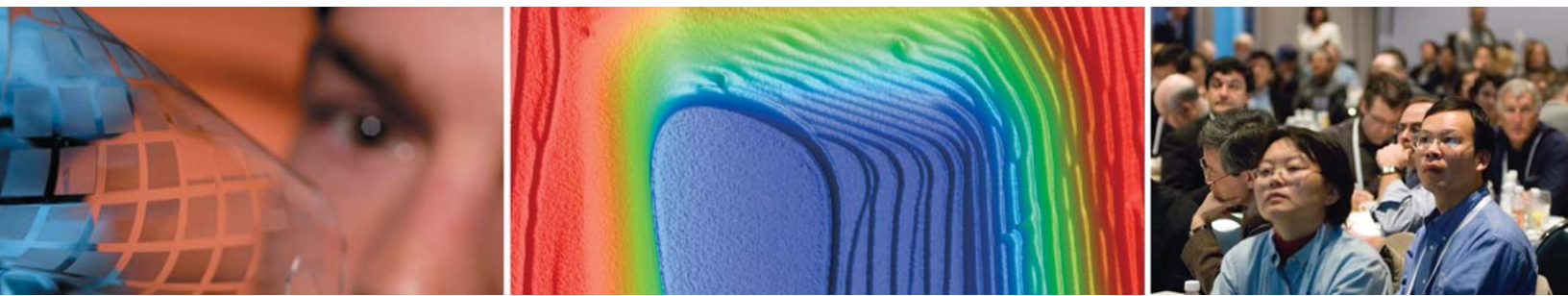
Technical Program

SPIE Advanced Lithography

Conferences + Courses: 24–29 February 2008

Exhibition: 26–27 February 2008

San Jose Convention Center and San Jose Marriott
San Jose, California USA



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Conferences + Courses: 24–29 February 2008

Exhibition: 26–27 February 2008

San Jose Convention Center and San Jose Marriott
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Welcome



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Left cover image: Georgia Tech Photo, Gary Meek. Graduate student Andrew Cannon shows a plastic sheet containing micro-mechanical features.

Center cover image: Courtesy of National Institute of Standards and Technology. Silicon staircase. Steps of silicon serve as a natural ruler for measuring vertical dimensions. This silicon "target" has step heights ranging from tens to hundreds of nanometers leading down to a flat, single atomic layer measuring only 0.3 nanometers. The microscope used to make this image sits on an isolated concrete slab equipped with air springs to cancel out even minute vibrations that could ruin the nanoscale measurements.

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Technical Conferences:

Emerging Lithographic Technologies XII. . 18-26

Conference Chair: Frank M. Schellenberg,
Mentor Graphics Corp.

Metrology, Inspection, and Process Control for Microlithography XXII. 27-32

Conference Chair: John A. Allgair,
SEMATECH, Inc. and Advanced Micro Devices, Inc.

Advances in Resist Materials and Processing Technology XXV. 33-38

Conference Chair: Clifford L. Henderson,
Georgia Institute of Technology

Optical Microlithography XXI 39-46

Conference Chair: Harry J. Levinson,
Advanced Micro Devices, Inc.

Design for Manufacturability through Design-Process Integration II 47-49

Conference Chair: Vivek K. Singh, Intel Corp.

Authors, Chairs and Committee Members 50-65

Proceedings of SPIE 67

Proceedings Order Form 68

Welcome

The SPIE Advanced Lithography Symposium is an annual international forum bringing practitioners of micro- and nanolithography together in a stimulating, informative, and interactive environment. The Symposium is fully committed to support your interests whether you work in semiconductor production lines, pilot lines, or research laboratories. It succeeds because the programs are tailored to professionals like you: those using technologies for today's production or developing it for production in the near future.

Moreover, the numerous short courses offered at Advanced Lithography 2008 are taught by individuals who are active in the field and recognized for their theoretical knowledge and practical experience.

We're excited to offer this opportunity to learn about the latest state-of-the-art applications and techniques, as well as emerging issues with the new challenges of alternative technologies. This wide range of topics becomes all the more important as optical lithography, historically the dominant patterning technology, faces new and tough challenges in providing the patterning solutions for leading-edge semiconductor manufacturing.

Welcome to San Jose for our 33rd year!



Roxann L. Engelstad,
Univ. of Wisconsin - Madison
2008 Symposium Chair



Christopher J. Progler,
Photonics Inc.
2008 Symposium Co-Chair

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Booth 628

Micro Lithography Inc., Booth 504

Micronic Laser Systems AB

Mitsui Chemicals America, Inc.,
Booth 2007

Special Events and Conference Daily Schedule

Monday	Tuesday	Wednesday	Thursday	Friday
Special Events				
<p><i>Plenary Presentation:</i> Ramifications of Lithography Choices on Memory Integration, D. Mark Durcan, 8:30 to 9:10 am, p. 6</p> <p><i>Plenary Presentation: Holistic Lithography Optimization: Wafer Lithography, Computational Lithography and Layout</i>, Martin A. van den Brink, 9:10 to 9:50 am, p. 6</p> <p><i>Plenary Presentation: Lithography and Design in Partnership: A New Roadmap</i>, Andrew B. Kahng, 9:50 to 10:30 am, p. 7</p> <p><i>Conference 6922: 2007 Best Paper Announcement</i>, 11:00 to 11:15 am, p. 8</p> <p><i>Conference 6923: 2007 C. Grant Willson Best Paper Award</i>, 11:00 to 11:10 am, p. 8</p> <p>Fellows Luncheon, 12:00 to 1:00 pm, p. 8</p> <p><i>BACUS Panel Discussion: Photomask Financial Fears: Fact, Fiction, or Fabrication</i>, Moderators: Mark Mason, Wilhem Maurer, 7:30 to 9:00 pm, p. 8</p> <p>Poster Reception, (Conferences 6922, 6923), 6:00 to 8:00 pm, p. 8</p>	<p>SPIE Women in Optics Lunch, Noon to 1:00 pm, p. 8</p> <p><i>Conferences 6921 and 6924 Panel Discussion: Future Projection Lithography: Optical or EUV?</i>, Moderators: Bruno LaFontaine, Nigel R. Farrar, 6:30 to 8:00 pm, p. 8</p>	<p>Student Lunch with the Experts – A Networking Event, 12:30 to 1:30 pm, p. 9</p> <p><i>Nanotechnology in Microlithography Panel Discussion: Massively Parallel Tools for Nanotechnology: Applications in Lithography and Metrology</i>, Moderators: Richard M. Silver, Christopher L. Soles, 6:30 to 8:00 pm, p. 9</p> <p><i>Conference 6922 Panel Discussion: Enabling Accurate Optical Proximity Correction</i>, Moderators: Christopher J. Raymond, Vladimir A. Ukraintsev, 8:00 to 9:30 pm, p. 9</p>	<p>Poster Reception, (Conferences 6921, 6924, 6925), 6:00 to 8:00 pm, p. 8</p> <p>Panel Discussion on Reference Metrology, Moderators: Ronald Dixon and George Orji, 7:00 to 9:00 pm, p. 9</p> <p><i>Conference 6925 Panel Discussion: DFM Idol</i>, Moderators: Mark E. Mason, Juan Antonio Carballo, 6:30 to 8:00 pm, p. 10</p>	<p><i>Conference 6520: Best Student Paper Award</i>, 10:30 to 10:40 am, p. 10</p>
	<p>Exhibition, p. 14 Tuesday, 26 February • 10:00 am to 5:00 pm Wednesday, 27 February • 10:00 am to 4:00 pm</p>			
Technical Conferences				
	Conf. 6921 Emerging Lithographic Technologies XII (Schellenberg) p. 18-26			
	Conf. 6922 Metrology, Inspection, and Process Control for Microlithography XXII (Allgair) p. 27-32			
	Conf. 6923 Advances in Resist Materials and Processing Technology XXV (Henderson) p. 33-38			
	Conf. 6924 Optical Microlithography XXI (Levinson) p. 39-46			
			Conf. 6925 Design for Manufacturability through Design-Process Integration II (Singh) p. 47-49	
<p style="text-align: center;">New Courses at Advanced Lithography 2008</p> <p style="text-align: center;">Don't miss these cutting-edge additions to this year's Professional Development program.</p> <ul style="list-style-type: none"> • SC855 Introduction to Design for Manufacturability (Liebmann, Wong) • SC856 Computational Lithography (Mansfield, Wong) • SC885 Principles and Practical Implementation of Double Patterning (Dusa) • SC886 Line Edge Roughness (Gallatin) • SC887 Modeling of Exposure Tools (Lai) • SC888 EUV Lithography (Bakshi, Soufli, Ahn, Naulleau) • SC889 Layout-Aware Circuit Analysis (Singh, Heng, Bansal) • SC890 Electron-Beam Lithography - Current Use and Recent Advances (Pfeiffer, McCord) <p style="text-align: center;">Register at the SPIE Cashier!</p>				

Plenary Presentations

Welcome and Announcements

Convention Center Hall 3

Monday 25 February 8:00 to 8:30 am

Symposium Chair: **Roxann L. Engelstad**, Univ. of Wisconsin/
Madison

- **Introduction of new SPIE Fellows**
- **Frits Zernike and the Advances in Optical Microlithography—5th Frits Zernike Award for Microlithography**

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Plenary Presentations

Convention Center Hall 3

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Ramifications of Lithography Choices on Memory Integration

Monday 25 February 8:30 to 9:10 am



D. Mark Durcan, President and Chief Operating Officer Micron Technology

A central challenge for every memory manufacturer is ensuring the availability of lithography capability. This is a key determinant in the cadence of device node shrinks, and as a result, many other process decisions revolve around the lithography capabilities that exist, or the alternative capability options that can be generated. Besides setting the memory roadmap aggressiveness and timeline, lithography choices also have many downstream implications for integrated technology

development, and ultimately affect how robust the manufacturing process will be. This presentation will focus on how lithography options interact with memory device integration, and why future innovation is critical to the business of memory device manufacturing.

Mark Durcan joined Micron Technology in 1984 as a diffusion engineer. Prior to being appointed Micron's president and chief operating officer June 26, 2007, he held a variety of increasingly responsible positions including process integration engineer, process integration manager, process development manager, chief technical officer, vice president of research and development and chief operating officer.

In addition to being responsible for Micron's worldwide manufacturing, Mark currently serves on the boards of the IM Flash Technologies, LLC; MP Mask, LLC; and the EUV LLC. He was recently appointed chairman of the Micron Technology Foundation, Inc., which was founded in October 1999, when Micron strengthened its commitment to education.

A member of Rice University's alumni, Mark earned a Masters in Chemical Engineering degree and a Bachelors of Science degree. He was presented the Sid Richardson College Athenian Award of Excellence and served as the college vice president.

Holistic Lithography Optimization: Wafer Lithography, Computational Lithography and Layout

Monday 25 February 9:10 to 9:50 am



Martin A. van den Brink, Executive Vice President Marketing & Technology, Member of the Board of Management for ASML (Netherlands)

Even as the semiconductor industry continued to advance to the beat of Moore's law, people have been calling the end of chip shrink. Device features have become 18 times smaller since 1987 as i-Line step-and-repeat technology evolved to today's ultra-high-NA argon fluoride (ArF) immersion step-and-scan systems, and the question looms if we

are nearing the end of the road? Even if the chip industry can continue to improve technology, will the economics still work?

The primary driver of Moore's law has been scaling through advances in optical lithography with shorter wavelengths, higher lens numerical apertures (NAs) and more effective lithography processing (k1).

Numerical apertures have reached the limit possible with the refractive indices of current machines and materials. Higher-index fluids and optical materials are years from achieving the performance required for advanced lithography. Process k1 factors can be extended by using double-patterning processes, which significantly impact cost, due to the doubling of process steps, halving of throughput and requirement for two masks. EUV, with its significantly shorter wavelength of 13.5-nm, offers a good prospect for continued scaling, but it has challenges of its own.

Previous technology transitions also appeared insurmountable, but were overcome. The lithography industry can continue to support the 40-year old cost reduction trend line which has created the \$260 billion semiconductor industry, but needs a holistic view in a more complex manufacturing environment. In order to keep the lithography roadmap viable, lithography makers need to look outside the box and explore many different strategies at the same time to offer value to their customers.

Martin van den Brink joined ASML when the company was founded in early 1984. He has held several positions in engineering and had prime responsibility for developing the PAS 5500 platform in the early 90's, which today represents the largest installed base at ASML's customers.

Since 1995 van den Brink has been part of ASML's management team and headed the total research and development organization. In 1999 he joined the Management Board and in addition to technology took on responsibility for Marketing.

Van den Brink received a degree in Electrical Engineering and a degree in Physics in 1984 from the University of Twente in the Netherlands.

Lithography and Design in Partnership: A New Roadmap

Monday 25 February 9:50 to 10:30 am



Andrew B. Kahng, Professor of Computer Science and Electrical Engineering, Univ. of California/San Diego

To surmount red brick walls of manufacturing variability, leakage power, and cost of ownership, the semiconductor industry has had to tear down several of its internal walls. The 21st century has seen deployment of early 'design-aware manufacturing' and 'manufacturing-aware design' concepts that improve mutual awareness of lithography and design. But this is not enough.

Semiconductor product teams are looking to software and 3-D to work around an onslaught of patterning, device and circuit challenges that include strain, mask error, RET complexity, double-patterning, and layout restrictions. Lithography and design must embark on a new roadmap of partnership - indeed, a partnership of roadmaps - for IC products to fully extract the value available from core front-end process technology. This talk will describe key elements of such a roadmap.

Andrew B. Kahng is professor of computer science and of electrical engineering at UC San Diego. He has published over 300 papers in the areas of IC physical design, performance analysis, and large-scale optimization. Since 1997, his research in IC design for manufacturability has pioneered methods for automated phase-shift mask layout, variability-aware analyses and optimizations, CMP fill synthesis, and parametric yield-driven, cost-driven methodologies for chip implementation.

Professor Kahng was the founding General Chair of the International Symposium on Physical Design, and technical program co-chair of the 2004 and 2005 Design Automation Conferences. From 2000 through 2003, he chaired both the U.S. and international working groups for Design technology for the ITRS roadmap, and continues to serve as co-chair of the Design ITWG. He has been an executive committee member of the MARCO Gigascale Systems Research Center since its inception in 1998. In October 2004, Professor Kahng co-founded Blaze DFM, Inc. (a company that provides cost and yield optimization tools at the VLSI design-to-manufacturing interface) and served as CTO of the company until resuming his duties at UCSD in September 2006.



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Special Events

Conference 6922:

2007 Best Paper Announcement for Metrology, Inspection, and Process Control for Microlithography

Convention Center J2

Monday 25 February11:00 to 11:15 am

Conference 6923:

2007 C. Grant Willson Best Paper Award

Convention Center Hall 3

Monday 25 February11:00 to 11:10 am

Sponsored by  Electronic Materials

SPIE Fellows Luncheon

Monday 25 February12:00 to 1:00 pm

Convention Center Room N

All Fellows of SPIE are invited to join your colleagues for an SPIE hosted luncheon at Advanced Lithography. Please join us for this informal gathering and a chance to interact with other.

BACUS Panel Discussion

Photomask Financial Fears: Fact, Fiction, or Fabrication

Convention Center C1

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Monday 25 February7:30 to 9:00 pm


Moderators: **Mark Mason**, Texas Instruments Inc.; **Wilhelm Maurer**, Infineon Technologies AG (Germany); **Warren Montgomery**, CNSE


Ever since Sematech hailed the coming of the Million Dollar Mask Set, industry pundits and prognosticators alike have bemoaned the rising cost of photomasks. Not surprisingly, this fever over mask cost has had some real consequences (both intended and unintended). Chief among those consequences is renewed interest in alternative maskless technologies. Still, the questions remain: how accurate were the predictions and how big an issue is mask cost? At this year's Photomask Panel, our collection of reticle experts will examine the real story behind mask cost, the impact to wafer cost, an how those costs compare to other rising expenses in our industry. Does the rising cost of mask spell doom for the semiconductor industry, or are we simply seeing a natural evolution in cost that is commensurate with the capability that advanced masks enable. We will invite our experts to comment and encourage the audience to take them to task on this important issue.

Poster Receptions


Convention Center Hall 3

Monday 25 February6:00 to 8:00 pm
(Conferences 6922, 6923)

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Thursday 28 February6:00 to 8:00 pm
(Conferences 6921, 6924, 6925)

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Conference attendees are invited to the poster sessions and receptions. Authors of poster papers will be present and at their posters during these sessions to answer questions and provide in-depth discussion concerning their posters. Attendees and authors are required to wear their conference registration badges to the poster sessions. See poster setup instructions page 15.

SPIE Women in Optics

SPIE Women in Optics Lunch

Tuesday 26 FebruaryNoon to 1:00 pm



Roxann L. Engelstad, Univ. of Wisconsin - Madison

Join us for an opportunity to network with other professionals at this lunch hosted by SPIE. Register at the SPIE Cashier on-site by 3:00 pm Monday; location information provided upon sign-up.

Conferences 6921 and 6924 Panel Discussion

Future Projection Lithography: Optical or EUV?

Convention Center A2

Tuesday 26 February6:30 to 8:00 pm

Panel Moderators: **Bruno M. LaFontaine**, Advanced Micro Devices, Inc.; **Nigel R. Farrar**, Cymer, Inc.

Panelists: **Timothy A. Brunner**, IBM Thomas J. Watson Research Ctr.; **Willard E. Conley**, Freescale Semiconductor, Inc.; **Benjamin G. Eynon**, SEMATECH, Inc.; **Tatsuhiko Higashiki**, Toshiba Corp. (Japan); **Winfried M. Kaiser**, Carl Zeiss SMT AG (Germany); **Kurt G. Ronse**, IMEC (Belgium); **Anthony Yen**, Taiwan Semiconductor Manufacturing Co. Ltd. (Taiwan)

As Moore's law drives IC dimensions ever smaller, it has been assumed that, at some node, some non-optical patterning technology would take the lead for IC manufacturing. Currently, EUV lithography is the top contender for that position. Yet, EUV has been delayed from its previous targets of 45nm and 32nm, while new advances in immersion lithography and various RETs have extended the life of conventional 193nm lithography generations beyond what was originally forecast.

This panel addresses the current forecast of requirements from both the memory and MPU perspectives for the 22nm node and beyond, and asks: can optical lithography, with all its tricks, have high enough yield? Can EUV, with all its problems, be ready in time? Will an alternative technology emerge and surprise us all? Or, will we all call it quits and give Moore's Law a rest?

Student Lunch with the Experts – A Networking Event

Wednesday 27 February 12:30 to 1:30 pm
 All students are invited. Seating is limited. See your registration packet onsite for location.

Enjoy a casual meal and lively discussion with optics/lithography experts at this complimentary event. Hosted by SPIE Student Services this event features experts willing to share their accumulated wisdom on career paths in optics and photonics. Take advantage of this opportunity to network with some of the best and brightest in the field!

Nanotechnology in Microlithography Panel Discussion

Massively Parallel Tools for Nanotechnology: Applications in Lithography and Metrology

Marriott San Jose Ballroom Salon III



Wednesday 27 February 6:30 to 8:00 pm
Moderators: Richard M. Silver, Christopher L. Soles, National Institute of Standards and Technology

The scaling of functional devices on the nanometer scale holds enormous potential for a wide range of technologies. Initial applications in arrayed dip pen nanolithography, AFM data storage and STM or AFM lithography at the atomic scale have been demonstrated. These applications have much in common with arrayed AFM metrology tools or arrayed field emitters. As an example, scanning electron beams can be used to lithographically pattern features on the order of 10 nm in size. However, this writing is a serial process and patterning relatively large areas with such small features is both extremely time consuming and costly. As a result, there has been a push to extend many of our current fabrication, inspection, and active single probe technologies into massively parallel beam or probe tip arrays.

However, there are many practical limitations of these scaling operations given the current fabrication and inspection tools on the market today. This panel will address key possibilities of fabricating thousands of independently operational devices capable of nanometer scale surface modification, device fabrication or metrology at the molecular scale. The experts will also address the major challenges of system integration and on-chip control processing including approaches to reliability and redundancy. There are many challenges to integrating system control and metrology at the nanometer scale to sensors and process control on the macro scale.

The panel will be comprised of international experts from leading universities, companies actively engaged in these developments and national laboratories. There will be a series of presentations followed by an open discussion period with audience participation.

Conference 6922 Panel Discussion

Enabling Accurate Optical Proximity Correction

Convention Center C1

Wednesday 27 February 8:00 to 9:30 pm
Christopher J. Raymond, Nanometrics Inc.; **Vladimir A. Ukraintsev**, Veeco Instruments Inc.

With lithographically printed features now pushed well into the sub-wavelength regime, the role of complex simulations for optical proximity correction (OPC) has never been more important. Yet validation of OPC models relies on accurate and precise metrology of the structures in question. Furthermore, as design rules shrink and devices become more complex, more metrology will be needed. CDSEM is the predominant metrology for the measurement of OPC structures, but with concerns over accuracy and precision, will it be suitable for OPC applications in the future? Measurement contouring is already proving useful, but what additional CDSEM applications are needed? Are distortions in a CDSEMs field of view invariant to layout orientation? Are there ways to improve its accuracy? As more measurements are needed, is throughput a concern? What is the optimal area coverage of sampling for model calibrations? What are the implications of contouring on regular process monitoring metrology? How can contour measurement quality be assessed?

The panel will be comprised of representatives from manufacturers, metrology and software vendors, and government laboratories.

Panel Discussion:

Reference Metrology

Convention Center B1

Thursday 28 February 7:00 to 9:00 pm
Moderators: Ronald Dixson and George Orji, National Institute of Standards and Technology

Reference metrology has been identified as one of the major challenges facing the measurement capability analysis. The rapid introduction of new instruments and the increased complexity of such instruments, make it difficult to evaluate their capability without having a reference instrument with sensitivity over the same range. In areas such as films metrology, the number of measurands and instruments with fundamentally different detection mechanism increases the need for a reference. Applications such as optical proximity correction verification and the introduction of designed based metrology methods highlight the need for having a baseline reference for a range of applications.

The panel discussion will discuss the need for advanced reference instruments, best practices, and selection criteria for reference instruments in lithography and films metrology, and the extendibility of such systems to the 22-nm and 18-nm nodes. Participants include experts from the semiconductor industry and government labs.



Special Events

Conference 6924 Panel Discussion

DFM Idol

Convention Center C1

Thursday 28 February 6:30 to 8:00 pm

Panel Moderators: **Mark E. Mason**, Texas Instruments Inc.; **Juan Antonio Carballo**, Argon Venture Partners

Over the last five years, pundits, pessimists, prognosticators, and the press have hailed the coming of the DFM Age for IC design. During this time, start-up companies have come and gone, been acquired, or gone public. Large EDA players have restructured product lines. IDMs have deployed internal solutions. Given all of this churn, now seem like the right time to ask some hard questions. Please join us as a "DFM Idol" Panel of Sages answers difficult questions about the state and value of DFM. We will start with our Celebrity DFM Gameshow Challenge, where prepared and random audience questions will be fired at the Sages. A hard-fast drill will then ensue, where each panelist will get to discuss the state of DFM within a strict two-minute limit. Hot and controversial DFM opinions, and difficult questions are not only welcome from the audience but encouraged. Ratings might be given using a secret voting system! As you can see, all DFM knowledge will be exposed.



Conference 6924

Best Student Paper Award

Friday 29 February 10:30 to 10:40 am

Sponsored by: **CYMER**

The Cymer Scientific Leadership Award for Best Student Paper, a monetary award to help support students engaged in research activities in optical microlithography, will be awarded this year again at the Optical Lithography conference. Student authors and student coauthors are eligible only. A panel of experts will be invited by the chair of the conference to serve as judges. The paper (oral or poster) demonstrating scientific excellence in presentation, quality and importance to the lithography community will be selected as the winner of this award.

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Webcast Event Coverage

Advanced Lithography 2008
Conf. 6924: Optical Microlithography XXI
Tuesday's Sessions 1-4

Session 1: **Keynote Session**

Chairs: **Harry J. Levinson**, Advanced Micro Devices, Inc.
Mircea V. Dusa, ASML

Speakers:

- **If it moves, simulate it**, Andrew R. Neureuther, Univ. of California/Berkeley
- **Iterations of double-patterning technology with OPC, wafer processing, and design flows**, Kevin D. Lucas, Synopsys, Inc.
- **Toward 3-nm overlay: an integrated error budget for double patterning lithography**, William H. Arnold, ASML US, Inc.
- **The future of EUVL**, Winfried M. Kaiser, Carl Zeiss SMT AG (Germany) et al.

Session 2: **Double Masking I**

Session 3: **Double Masking II**

Session 4: **Low-k1 Lithography I**

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Hot Topics in

Advanced Lithography

- EUV Lithography
- Immersion Lithography
- Double Patterning



Overview by **Kurt Ronse**, IMEC

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Dr. Carl M. Cohen, (March 2008, Members Only)

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Micheal Alley,
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SPIE Foundation Courses

Foundation courses provide an introduction to and overview of the technical area they address. They are an ideal entry point for understanding core concepts and tools if you're new to a field, looking to brush up your knowledge in a specific area, or want to take a closer look at a specialization you're considering pursuing. Courses are taught by instructors with deep knowledge and years of in-the-field experience, and offer the unique opportunity to learn from some of the most accomplished optics professionals in their respective industries.

SPIE reserves the right to cancel a course due to insufficient advance registration.

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Continuing Education Units



SPIE is an authorized provider of Continuing Education Units (CEUs) through IACET – The International Association of Continuing Education and Training. SPIE awards CEUs to participants who successfully attend courses, and complete and return the evaluation form within 30 days of the course presentation. SPIE maintains a record of all CEUs earned for each participant for seven years.

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- ▶ Further your career through ongoing education
- ▶ Earn CEUs for your continuing education

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at the SPIE Cashier!**

Daily Course Schedule

Sunday	Monday	Tuesday	Wednesday	Thursday
Advances in Resist Materials and Processing Technology				
<p>SC101 Introduction to Microlithography: Theory, Materials, and Processing (Bowden, Thompson, Willson) 8:30 am to 5:30 pm, \$595 / \$695</p>				<p>SC103 Chemically Amplified Resists (Willson) 8:30 am to 5:30 pm, \$530 / \$630</p> <p>SC616 Practical Photoresist Processing (Dammel) 1:30 to 5:30 pm, \$315 / \$365</p>
Design for Manufacturability through Design-Process Integration				
<p>SC540 Applying Optical Proximity Correction and Design for Manufacturability to Product Designs (Capodieci, Lucas) 8:30 am to 5:30 pm, \$530 / \$630</p> <p>SC105 CD Metrology and Image Formation in the Scanning Electron Microscope (SEM) (Wells, Postek) 8:30 am to 5:30 pm, \$580 / \$680</p> <p>SC116 Lithographic Optimization: A Theoretical Approach (Mack) 8:30 am to 5:30 pm, \$570 / 670</p> <p>SC833 Lithography Integration for Semiconductor Back-End-Of-The-Line (BEOL) (Lin) 8:30 am to 12:30 pm, \$315 / \$365</p> <p>NEW SC885 Principles and Practical Implementation of Double Patterning (Dusa) 8:30 am to 12:30 pm, \$315 / \$365</p> <p>NEW SC887 Modeling of Exposure Tools (Lai) 1:30 to 5:30 pm, \$315 / \$365</p>		<p>NEW SC855 Introduction to Design for Manufacturability (Liebmann, Wong) 1:30 to 5:30 pm, \$315 / \$365</p> <p>NEW SC889 Layout-Aware Circuit Analysis (Singh, Heng, Bansal) 8:30 am to 12:30 pm, \$315 / \$365</p> <p>NEW SC856 Computational Lithography (Mansfield, Wong) 1:30 to 5:30 pm, \$315 / \$365</p>		
Emerging Lithographic Technologies				
<p>NEW SC890 Electron-Beam Lithography - Current Use and Recent Advances (Pfeiffer, McCord) 8:30 am to 5:30 pm, \$530 / \$630</p> <p>SC888 EUV Lithography (Bakshi, Soufli, Ahn, Naulleau) 8:30 am to 6:30 pm, \$740 / \$840</p> <p>SC101 Introduction to Microlithography: Theory, Materials, and Processing (Bowden, Thompson, Willson) 8:30 am to 5:30 pm, \$595 / \$695</p> <p>SC622 Nano-Scale Patterning with Imprint Lithography (Sreenivasan, Willson, Resnick) 6:00 to 10:00 pm, \$315 / \$365</p>				
Intellectual Property & Patents				
				<p>WS619 Intellectual Assets for Micro/Nano Electronics and Lithography (Cole) 1:30 to 5:30 pm, \$315 / \$365</p>

Daily Course Schedule

Sunday	Monday	Tuesday	Wednesday	Thursday
Metrology, Inspection, and Process Control for Microlithography				
SC105 CD Metrology and Image Formation in the Scanning Electron Microscope (SEM) (Wells, Postek) 8:30 am to 5:30 pm, \$530 / \$630				
SC101 Introduction to Microlithography: Theory, Materials, and Processing (Bowden, Thompson, Willson) 8:30 am to 5:30 pm, \$595 / \$695				
SC831 Introduction to Scatterometry Metrology: Theory and Application (Bao, Barry) 1:30 to 5:30 pm, \$315 / \$365				
NEW SC886 Line Edge Roughness (Gallatin) 1:30 to 5:30 pm, \$315 / \$365				
Optical Microlithography				
SC120 193-nm Photoresist Materials (Dammel) 8:30 am to 12:30 pm, \$315 / \$365				
SC540 Applying Optical Proximity Correction and Design for Manufacturability to Product Designs (Capodieci, Lucas) 8:30 am to 5:30 pm, \$530 / \$630				
SC707 Basics of Optical Imaging in Microlithography: A Hands-on Approach (Milster, Brooker, Socha) 8:30 am to 12:30 pm, \$315 / \$365				
SC105 CD Metrology and Image Formation in the Scanning Electron Microscope (SEM) (Wells, Postek) 8:30 am to 5:30 pm, \$530 / \$630				
SC101 Introduction to Microlithography: Theory, Materials, and Processing (Bowden, Thompson, Willson) 8:30 am to 5:30 pm, \$595 / \$695				
SC116 Lithographic Optimization: A Theoretical Approach (Mack) 8:30 am to 5:30 pm, \$570 / 670				
SC833 Lithography Integration for Semiconductor Back-End-Of-The-Line (BEOL) (Lin) 8:30 am to 12:30 pm, \$315 / \$365				
SC579 Photomask Fabrication and Technology Basics (Duff) 8:30 am to 5:30 pm, \$530 / \$630			NEW SC855 Introduction to Design for Manufacturability (Liebmann, Wong) 1:30 to 5:30 pm, \$315 / \$365	NEW SC889 Layout-Aware Circuit Analysis (Singh, Heng, Bansal) 8:30 am to 12:30 pm, \$315 / \$365
NEW SC885 Principles and Practical Implementation of Double Patterning (Dusa) 8:30 am to 12:30 pm, \$315 / \$365				SC118 Anti-Reflective Coatings: Theory and Practice (Dammel) 8:30 am to 12:30 pm, \$315 / \$365
SC723 The Limits of Optical Lithography (Pierrat) 8:30 am to 12:30 pm, \$315 / \$365				NEW SC856 Computational Lithography (Mansfield, Wong) 1:30 to 5:30 pm, \$315 / \$365
SC706 Imaging and Optics Fundamentals in Microlithography (Flagello) 1:30 to 5:30 pm, \$315 / \$365				
NEW SC886 Line Edge Roughness (Gallatin) 1:30 to 5:30 pm, \$315 / \$365				
NEW SC887 Modeling of Exposure Tools (Lai) 1:30 to 5:30 pm, \$315 / \$365				
SC724 Optical Lithography Extension: Design for Manufacturing and New Resolution Enhancement Techniques (Pierrat) 1:30 to 5:30 pm, \$315 / \$365				
SC779 Polarization for Lithographers (Kye, McIntyre) 1:30 to 5:30 pm, \$315 / \$365				
SC102 Optical Lithography Modeling (Neureuther, Smith) 6:00 to 10:00 pm, \$315 / \$365				
			Register for courses onsite at the SPIE Cashier!	

Don't miss the Exhibition!



Exhibition Hours

Tuesday: 10:00 am to 5:00 pm

Wednesday: 10:00 am to 4:00 pm

Semiconductor Metrology



Contact SPIE Sales
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SPIESales@SPIE.org

See these companies at the exhibition:

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Anchor Semiconductor, Inc.
Applied Materials
ASML
ATMI, Inc.
AZ Electronic Materials USA Corp.
Benchmark Technologies, Inc.
Brewer Science
Brion Technologies, Inc.
Cadence Design Systems, Inc.
Canon USA, Inc.
Carl Zeiss SMT
CMPC Surface Finishes
Corning Inc.
CUNO Inc.
CVI Melles Griot - Albuquerque
Cyantek Corp.
CyberOptics Semiconductor
Cymer, Inc.
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San Jose McEnergy Convention Center, 150 West San Carlos, San Jose, CA 95113 USA.

Registration Hours

San Jose Convention Center, Exhibit Hall 2

Sunday	7:00 am to 6:00 pm
Monday	7:00 am to 4:00 pm
Tuesday	7:30 am to 5:00 pm
Wednesday	7:30 am to 5:00 pm
Thursday	7:30 am to 5:00 pm
Friday	7:30 am to 11:00 am

Multiple facilities in downtown San Jose are used for conferences and courses, so please allow yourself enough time to register, pick up your materials and possibly walk to a nearby facility before your meeting or course begins.

Exhibition Hours

Tuesday, 26 February	10:00 am to 5:00 pm
Wednesday, 27 February	10:00 am to 4:00 pm

Course Materials Desk

Open during Registration hours

If you have registered to attend a course, stop by the Course Materials Desk after you pick up your badge, to obtain your course notes and course location. Pick up a copy of the latest Education Services catalog to see SPIE Courses at symposia, on video and CD-ROM, and to discover the opportunities of customized In-Company courses.

Coffee Breaks

Sponsored by



Complimentary coffee will be served twice each day of the conference at approximately 10:00 am and 3:00 pm. Please check the individual technical conference listings for exact times and locations.

Breakfast Breads

Sponsored by **CYMER**

Breakfast breads and coffee will be served from 7:30 am to 8:30 am Monday through Friday for Symposium attendees in the Convention Center, Concourse 2 Lobby.

Lunch Coupons

Tuesday lunch sponsored by **TOPPAN**
 Wednesday lunch sponsored by **tok**

Full conference registrants will receive a lunch coupon redeemable towards a luncheon purchased Tuesday and Wednesday at designated areas of the Exhibit Hall. Coupons will be accepted from 11:30am to 1:30 pm both days. Some restrictions apply; please refer to the coupons in your registration packet.

Refreshment Purchases

For attendee purchase of light refreshments, including continental breakfast, specialty carts will be set up in the foyer of the Convention Center Sunday through Thursday.

Cash Lunches and Exhibition Concessions at Exhibition Halls 1-2, A cash sandwich bar will be available in the foyer of the CC Sunday through Thursday.

Visit the Exhibition Concessions located in the back of the exhibition halls on Tuesday-Wednesday featuring Domestic and International Cuisine. They will serve hot and cold snacks, beverages, deli-type sandwiches, salads, hot entrees, and pastries and will be open during exhibition hours.

Desserts

Sponsored by **JSR Micro** **JSR** **AZ Electronic Materials**

Served in the Advanced Lithography exhibition halls.

Tuesday and Wednesday

Dessert snacks will be served from 3:00 to 3:30 pm. Complimentary tickets for the dessert snacks will be included in attendee registration packets.

Internet Pavilion

Sponsored by **JEOL**

SPIE will have a complimentary Internet Pavilion at the Convention Center on Sunday through Friday where attendees can use provided workstations or hook up their laptop to an Ethernet connection to access the Internet.

Complimentary Internet Wireless Access

Sponsored by **TEL** **TOKYO ELECTRON**

SPIE is pleased to provide complimentary wireless access to the Internet for all conference attendees bringing 802.11b wireless-enabled laptops or PDAs. Coverage located in Convention Center Ballroom Concourse (east end) near the SPIE Marketplace and Internet Pavilion.

Properly secure your computer before accessing the public wireless network. Failure to do so may allow unauthorized access to your laptop as well as potentially introduce viruses to your computer and/or presentation.

Poster Setup

Poster presenters may set up on Monday between 10:30 am and 4:30 pm and Thursday between 9 am and 4:30 pm on the day of their assigned presentation. Poster presenters who have not set up by the appropriate time on the day of their presentation will be considered a "no show" and their manuscript will not be published. Presenters must remove their posters immediately after the poster session. Posters not removed will be considered unwanted and will be discarded. SPIE assumes no responsibility for posters left up after the end of each poster session.

Poster numbers will be pre-posted on the poster boards thus authors need to find their applicable poster number and post their paper on the appropriate 1/2 board space. Presenters who have not placed their papers on their assigned board by 4:30 pm on Monday, or Thursday on the day of their presentation will be considered a "no show" and their manuscript will not be published.

Removal: Presenters must remove their posters immediately after their respective poster session. Posters not removed will be considered unwanted and will be discarded. SPIE assumes no responsibility for posters left up after the end of each poster session.

Attendees are requested to wear their conference registration badges.

General Information

Speakers Check-In Desk / Preview Station

San Jose Convention Center, Concourse (near Marriott Hotel)

Sunday 2:00 pm to 6:00 pm

Monday through Thursday, 7:30 am to 5:00 pm

Friday. 7:30 am to 12:00 pm

All conference rooms will have a computer workstation, LCD projector, screen, lapel microphone, and laser pointer. All Presenters are requested to come to the speaker check in desk to confirm display settings of their presentations from their memory devices or laptops with the audiovisual equipment being used at this symposium.

SPIE Copy Center

Sunday through Thursday during registration hours San Diego Copy will provide a copy service during the week for symposium attendees. The rates are 5 cents per copy. The Copy Center will be located near registration.

SPIE Message Center

The SPIE Message Center telephone number is 408-271-6200 Messages will be taken during registration hours Sunday through Thursday. Please check the message board at the message center near SPIE registration daily to receive your messages.

SPIE Marketplace & Membership Services

Open during Registration hours

The SPIE Marketplace is your source for the latest SPIE Press books, Proceedings, and Educational and Professional Development materials. Become a Member of SPIE, explore the Digital Library, and take home a souvenir.

Industry Resources Booth

The SPIE Industry Resources Booth provides the tools you need to move ideas and technology to the market. Visit the booth for information on events, marketing opportunities, education, and training that SPIE can provide you to make your venture a success.

Press & Media Center

The Press & Media Center provides press conference facilities, refreshments, and press releases from exhibitors. Credentialed media are invited to communicate news via the provided telephone and high-speed internet connections. Registration and exhibition fees are waived for working journalists and editors. Preregister by e-mailing name, organization, title, address, e-mail, and phone number to media@spie.org.

Child Care Services

Two child sitting services available in San Jose are.

1 Bay Area 2nd MOM Inc., Hotel Nanny Service, Toll Free Phone: 1-888-926-3666, or (650) 858-2469, ext. 109. Fax: (650) 493-6598, Email: oncall@2ndmom.com or parentcounselor@2ndmom.com, Website: www.2ndmom.com

2. Sitters Unlimited: Toll Free Phone: (408) 452-0225, E-mail: info@bayareasittersunlimited.com or www.bayareasittersunlimited.com

Note: SPIE does not imply an endorsement or recommendation of these services. They are provided on an "information-only" basis for your further analysis and decision. Other services may be available.

Restaurant Reservations and Information Desk

The San Jose Convention and Visitors Bureau operates a Restaurant Reservations and Information Desk on the street level of the Convention Center near the main entrance. The desk will be open Sunday through Thursday during core hours of the convention. For more information visit their website <http://www.sanjose.org>

Audio, Video, Digital Recording Policy

In the Meeting Rooms and Poster Sessions: For copyright reasons, recordings of any kind are strictly prohibited without prior written consent of the presenter in any conference session, short course or of posters presented. Each presenter being taped must file a signed written consent form. Individuals not complying with this policy will be asked to leave a given session and asked to surrender their film or recording media. Consent forms are available at the Speakers Check In Desk.

In the Exhibition Hall: For security and courtesy reasons, photographing or videotaping individual booths and displays in the exhibit hall is allowed ONLY with explicit permission from on-site company representatives. Individuals not complying with this policy will be asked to surrender their film and to leave the exhibition hall.

Laser Pointer Safety Information

SPIE supplies tested and safety approved laser pointers for all conference meeting rooms, and for short course rooms if instructors request one. For safety reasons, SPIE requests that presenters use our provided laser pointers available in each meeting room.

If using your own laser pointer, have it tested at your facility to make sure it has <5 mW power output. Laser pointers in Class II and IIIa (<5 mW) are eye safe if power output is correct - but don't automatically trust the labeling. Commercially available laser pointers, red or green (or any color), could be incorrectly labeled as to their wavelength and power output.

Presenters intending to use their own laser pointer for presentations are required to come to the Speakers Check-In Desk onsite and test their pointer on our power meter. If the pointer fails the safe power level you may not use the pointer at the conference. You will be required to sign a waiver releasing SPIE of any liability for use of potentially non-safe laser pointers.

Use of a personal laser pointer at an SPIE event represents user's acceptance of liability for use of a non-SPIE supplied laser pointer device. Misuse of any laser pointer could lead to eye damage. In California, it is a criminal misdemeanor to shine a laser pointer at individuals "who perceive they are at risk."

Underage Persons on Exhibition Floor

For safety and insurance reasons, no persons under the age of 16 will be allowed in the exhibition area during move-in and move-out. During open exhibition hours, only children over the age of 12 accompanied by an adult will be allowed in the exhibition area.

Unauthorized Solicitation

Any manufacturer or supplier who is not an exhibitor and is observed to be soliciting business in the aisles or in another company's booth will be asked to leave immediately. Unauthorized solicitation in the Exhibition Hall is prohibited.

Unsecured Items

Personal belongings such as briefcases, backpacks, coats, book bags, etc. should not be left unattended in meeting rooms or public areas. These items will be subject to removal by security upon discovery

Car Rental



Hertz Car Rental has been selected as the official car rental agency for this Symposium. To reserve a car, identify yourself as an Advanced Lithography Conference attendee using the Hertz Meeting Code CV# 029B0011. Call 1-800-654-2240.

Parking

For the city: <http://www.sjdowntownparking.com/>

At the Convention Center, 150 W. San Carlos St.
 Max \$16 per day. (\$1 for each 20 min to max \$16.)
 There are approximately 650 spaces for the public to use.
 Alternate Parking Downtown San Jose - River Park Tower Garage, located on the corner of San Carlos and Woz Way, 333 W. San Carlos St. \$1.25 per each 20 minutes, \$18 daily maximum. Rates and hours subject to change without notice. Approx. 1,000 spaces available each day of the event. Hrs of operation:
 Mon-Fri - 6:30 am to 12:00 midnight, Sat - 8:00 am to 12 midnight
 Sun - 8:00 am - may close at 10pm if event over

Parking at the Hotels

On space available basis
 (rates subject to change without notice)

Fairmont San Jose

Valet Only
 Overnight guests - \$26 with in/out privileges.
 Visitors - \$5 for 1st 30 min, \$1.50 for each additional 20 min, max per day is \$26. Parking garage is beneath the hotel

San Jose Marriott

Guests - \$25 per day with in/out privileges
 Non-guests - \$6.00 per hour with a maximum of \$25/day.
 ARCADIA restaurant parking \$6.00 per hour, max 4 hours

Hilton San Jose & Towers

Guests: Self - \$18 max. with in/out privileges. Valet \$23 max. with in/out privileges and \$10 with validation at the City Bar & Grille.
 Non Guests: Self - \$21 max., Valet \$26 max. and complimentary for up to 5 hours with validation from the City Bar & Grille.

Crowne Plaza

Guests self parking \$18 with in/out privileges (no valet). Covered parking garage parallel to hotel.
 Non-guest parking is \$20 daily max. (\$6. for 1st hour, then \$1 every 1/2 hour to \$20 max)

Sainte Claire

For Guests only Valet Parking Only, \$21 for overnight. In/out privileges for those guests who charge the parking to their rooms. Parking garage is not owned by hotel. Fees are subject to change.

Park & Ride

Since parking at the Convention Center can be quite congested at times, try the Park and Ride alternative transportation method, utilizing VTA's complimentary Park & Ride parking lots to commute to the Convention Center. To see a full listing of Park and Ride lots, visit www.vta.org and click on 'schedules, Maps & Fares' and then "Park and Ride." Free regular Park & Ride parking is limited to 72 hours.

Hotel Information

San Jose Marriott, Headquarters Hotel

301 South Market St., Tel: 408 280 1300; Fax: 408 278 4444.

Fairmont Hotel

170 South Market St., Tel: 408 998 1900; Fax: 408 287 1648.

Hilton San Jose and Towers

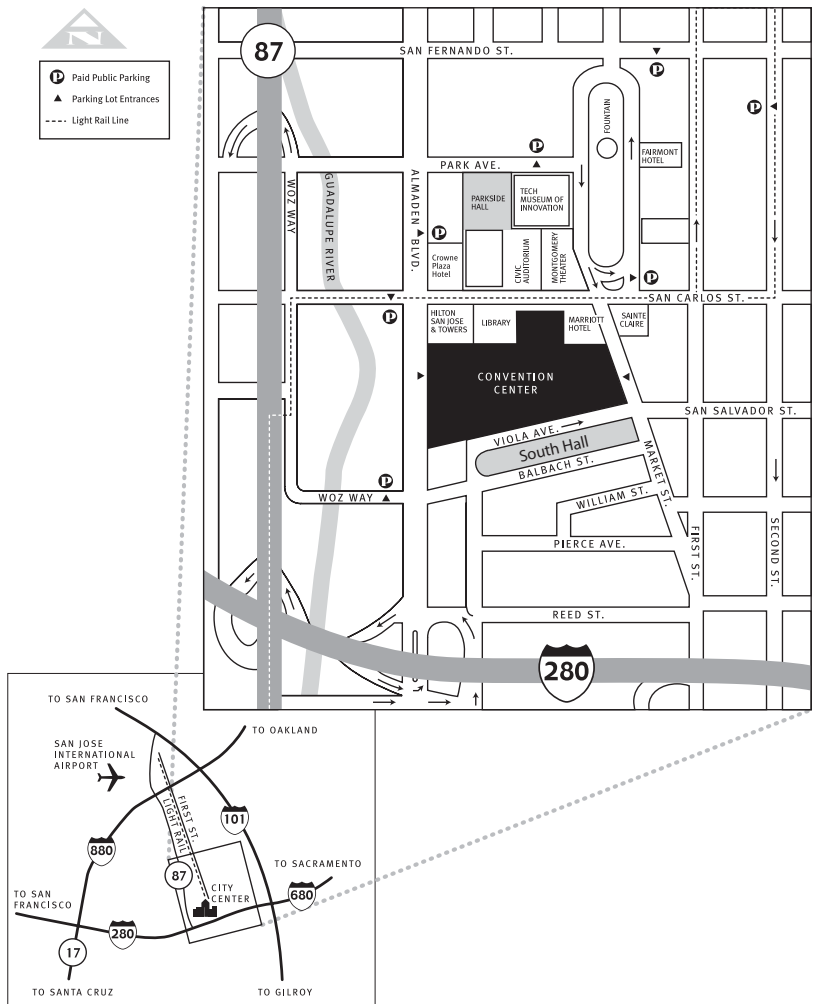
300 Almaden Blvd., Tel: 408 287 2100; Fax: 408 947 4489.

Crowne Plaza San Jose Hotel

282 Almaden Blvd., Tel: 408 998 0400; Fax: 408 289 9081.

The Sainte Claire

302 S. Market St., Tel: 408 885 1234; Fax: 408 977 0403.



Emerging Lithographic Technologies XII

Conference Chair: **Frank M. Schellenberg**, Mentor Graphics Corp.

Conference Co-Chair: **Bruno LaFontaine**, Advanced Micro Devices, Inc.

Program Committee: **David T. Attwood**, Univ. of California/Berkeley and Lawrence Berkeley National Lab.; **Vivek Bakshi**, SEMATECH, Inc.; **James W. Blatchford**, Texas Instruments Inc.; **Michael Goldstein**, Intel Corp.; **Timothy R. Groves**, SUNY/Univ. at Albany; **Daniel J. C. Herr**, Semiconductor Research Corp.; **Sung-Woo Lee**, SAMSUNG Electronics Co., Ltd. (South Korea); **Michael J. Lercel**, SEMATECH, Inc.; **James A. Liddle**, National Institute of Standards and Technology; **Hans Loeschner**, IMS Nanofabrication AG (Austria); **R. Scott Mackay**, Mackay & Associates; **Pawitter J.S. Mangat**, Motorola, Inc.; **Christie R. K. Marrian**, Spansion Inc.; **Anthony Novembre**, Lucent Technologies; **Shinji Okazaki**, Hitachi Ltd. (Japan); **Laurent Pain**, CEA-LETI (France); **Douglas J. Resnick**, Molecular Imprints, Inc.; **Kazuaki Suzuki**, Nikon Corp. (Japan); **William M. Tong**, Hewlett-Packard Co.; **Kevin T. Turner**, Univ. of Wisconsin/Madison

Tuesday 26 February

Room: Conv. Ctr. B1 Tues. 8:00 am to 8:20 pm

Introductory Remarks

Session Chairs: **Bruno M. LaFontaine**, Advanced Micro Devices, Inc.;
Frank M. Schellenberg, Mentor Graphics Corp.

SESSION 1

Conv. Ctr. B1 Tues. 8:20 to 9:20 am

Keynote Session

Session Chairs: **Frank M. Schellenberg**, Mentor Graphics Corp.;
Bruno M. LaFontaine, Advanced Micro Devices, Inc.

8:20 am: **Selete's EUV program: progress and challenges (Keynote Presentation)**, Ichiro Mori, Osamu Suga, Hiroyuki Tanaka, Iwao Nishiyama, Tsuneo Terasawa, Hiroyuki Shigemura, Takao Taguchi, Toshihiko Tanaka, Toshiro Itani, Semiconductor Leading Edge Technologies, Inc. (Japan) [6921-01]

8:50 am: **Breaking the limits: combination of electron-beam lithography and nanoimprint lithography for production of next-generation magnetic media and optical media (Keynote Presentation)**, Babak Heidari, OBDUCAT AB (Sweden). [6921-02]

SESSION 2

Conv. Ctr. B1 Tues. 9:20 am to 12:10 pm

Nanoimprint I

Session Chairs: **Douglas J. Resnick**, Molecular Imprints, Inc.;
Christie R. K. Marrian, Spansion Inc.

9:20 am: **Study of nanoimprint lithography for applications toward 22-nm node CMOS devices (Invited Paper)**, Ikuo Yoneda, Shinji Mikami, Takumi Ota, Masamitsu Ito, Tetsuro Nakasugi, Tatsuhiko Higashiki, Toshiba Corp. (Japan) [6921-03]

9:50 am: **Hybrid circuit of CMOS and crossbar nanowires by nanoimprint: semiconductor nanowire interconnects (SNIC)**, William M. Tong, Hewlett-Packard Labs.; Micheal Cumbie, James E. Ellenson, Tsuyoshi Yamashita, Neal W. Meyer, Dennis Lazaroff, Laura H. King, Hewlett-Packard Co.; Greg Snider, R. Stanley S. Williams, Hewlett-Packard Labs. [6921-08]

Coffee Break. 10:10 to 10:40 am

10:40 am: **Status of the UV nanoimprint stepper technology for silicon IC fabrication (Invited Paper)**, S. V. Sreenivasan, Philip Schumaker, Byung Jin Choi, Molecular Imprints, Inc. [6921-06]

11:10 am: **Full-field imprinting of sub-40-nm patterns**, Kyoung Taek Kim, SAMSUNG Electronics Co., Ltd. (South Korea). [6921-05]

11:30 am: **Nanoimprinted crossbar switches integration on silicon MOSFET**, Zhiyong Li, Julien Borghetti, Xuema Li, Douglas A. Ohlberg, Joseph Straznicki, Wei Wu, Zhaoning Yu, R. Stanley Williams, Hewlett-Packard Labs. [6921-04]

11:50 am: **Minimizing linewidth roughness for 22-nm node patterning with step-and-flash imprint lithography**, Gerard M. Schmid, Douglas J. Resnick, Niyaz Khusnatdinov, Dwayne LaBrake, Molecular Imprints, Inc. [6921-07]

Lunch/Exhibition Break 12:10 to 1:30 pm

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Sessions 3 and 4 run concurrently with sessions 5 and 6.

SESSION 3

Conv. Ctr. B1 Tues. 1:30 to 3:40 pm

Nanoimprint II

Session Chairs: **William M. Tong**, Hewlett-Packard Labs.; **Pawitter J.S. Mangat**, Motorola, Inc.

1:30 pm: **Metrology and materials for nanoimprint technologies: needs and prospects** (*Invited Paper*), Christopher L. Soles, National Institute of Standards and Technology [6921-09]

2:00 pm: **Chemical and mechanical properties of UV-cured nanoimprint resists**, Frances A. Houle, Ann Fornof, Dolores C. Miller, IBM Almaden Research Ctr.; Eva Simonyi, IBM Thomas J. Watson Research Ctr. [6921-10]

2:20 pm: **Dual-Damascene BEOL processing using multilevel step and flash-imprint lithography**, Brook Chao, Frank Palmieri, Wei-Lun Jen, D. H. McMichael, C. Grant Willson, The Univ. of Texas at Austin; Jordan Owens, Rich Berger, Ken Sotoodeh, Bruce Wilks, Joseph Pham, Ronald Carpio, Ed LaBelle, Jeff Wetzel, Advanced Technology Development Facility, Inc. [6921-11]

2:40 pm: **High-resolution nanoimprint templates for dual Damascene: fabrication and imprint results**, Mathias Irmscher, Joerg Butschke, Holger Sailer, Marcus Pritschow, Institut für Mikroelektronik Stuttgart (Germany); Jordan Owens, Advanced Technology Development Facility, Inc.; C. Grant Willson, The Univ. of Texas at Austin [6921-84]

3:00 pm: **Interfacial adhesion studies for step and flash imprint lithography**, Michael W. Lin, Daniel J. Hellebusch, The Univ. of Texas at Austin; Li Tao, The Univ. of Texas at Dallas; Gary Lu, Kenneth M. Liechti, Paul S. Ho, C. Grant Willson, The Univ. of Texas at Austin [6921-13]

3:20 pm: **Subwavelength optical diffraction and photo-acoustic metrologies for the characterization of nanoimprinted structures**, Timothy Kehoe, Tyndall National Institute (Ireland); Juerg Dual, ETH Zürich (Switzerland); Vincent Reboud, Nikolaos Kehagias, Tyndall National Institute (Ireland); Stefan Landis, Cecile Gourgon, Lab. d'Electronique de Technologie de l'Information (France); Jacqueline Vollmann, ETH Zürich (Switzerland); Clivia M. Sotomayor Torres, Tyndall National Institute (Ireland) and Català de Recerca i Estudis Avançats (Spain) [6921-12]

Coffee Break 3:40 to 4:10 pm

SESSION 5

Conv. Ctr. C1 Tues. 1:20 to 4:20 pm

EUV Systems

Session Chairs: **Shinji Okazaki**, Hitachi, Ltd. (Japan); **David T. Attwood**, Univ. of California/Berkeley

1:20 pm: **Field performance of the EUV alpha demo tools** (*Invited Paper*), Hans Meiling, Vadim Banine, ASML Netherlands B.V. (Netherlands); Kevin Cummings, ASML US, Inc.; Mieke Goethals, IMEC (Netherlands); Noreen Harned, ASML Wilton; Bas Hultermans, ASML Netherlands B.V. (Netherlands); Peter Kürz, Carl Zeiss SMT AG (Germany); Sjoerd Lok, ASML Netherlands B.V. (Netherlands); Martin Lowisch, Carl Zeiss SMT AG (Germany); Henk Meijer, Uwe Mickan, ASML Netherlands B.V. (Netherlands); Kurt Ronse, IMEC (Netherlands); James G. Ryan, Michael D. Tittnich, College of Nanoscale Science and Engineering; John Zimmerman, ASML Wilton [6921-21]

1:50 pm: **Nikon EUVL-development progress update**, Takaharu Miura, Katsuhiko Murakami, Kazuaki Suzuki, Yoshiaki Kohama, Kenji Morita, Kazunari Hada, Yukiharu Ohkubo, Nikon Corp. (Japan) [6921-22]

2:10 pm: **Canon's development status of EUVL technologies**, Shigeyuki Uzawa, Hiroyoshi Kubo, Yoshinori Miwa, Toshihiko Tuji, Takayuki Hasegawa, Hideki Morishima, Canon Inc. (Japan) [6921-23]

2:30 pm: **Imaging performance of the EUV alpha demo tool at IMEC**, Gian F. Lorusso, Anne-Marie Goethals, Rik M. Jonckheere, IMEC (Belgium); Alan Myers, Intel Corp.; Insung Kim, SAMSUNG Electronics Co., Ltd. (South Korea); Jan Hermans, Bart Baudemprez, IMEC (Belgium); Ardavan Niromaand, Micron Technology, Inc. (Belgium); Kurt G. Ronse, IMEC (Belgium) [6921-24]

2:50 pm: **Use of EUV lithography to produce demonstration devices**, Bruno M. LaFontaine, Yunfei Deng, Ryoung-Han Kim, Harry J. Levinson, Sarah McGowan, Uzodinma Okoroanyanwu, Cyrus Tabery, Thomas Wallow, Cyrus E. Tabery, Advanced Micro Devices, Inc.; Sander Bouten, Michael Crouse, Kevin Cummings, Judy Galloway, Sang-In Han, Bart Kessels, Brian Lee, Brian Niekrewicz, Bill Pierson, Robert Routh, ASML US, Inc.; Kurt Kimmel, Chiew-Seng Koay, IBM Corp.; Karen Petrillo, IBM Thomas J. Watson Research Ctr.; James Word, Mentor Graphics Corp.; Minoru Sugawara, Sony Electronics Inc.; Hiroyuki Mizuno, Toshiba America Electronics Components [6921-25]

Coffee Break 3:10 to 3:40 pm

3:40 pm: **Development status of projection optics and illumination optics for EUV1**, Katsuhiko Murakami, Testuya Oshino, Hiroyuki Kondo, Hiroshi Chiba, Hideki Komatsuda, Kazushi Nomura, Hiromitsu Iwata, Nikon Corp. (Japan) [6921-26]

4:00 pm: **Smoothing properties of single and multilayer coatings: a method to smoothen substrates**, Eric Louis, Toine van den Boogaard, Erwin Zoethout, Santi Alonso van der Westen, FOM-Instituut voor Plasmafysica Rijnhuizen (Netherlands); Stephan Muellender, Carl Zeiss SMT AG (Germany); Fred Bijkerk, FOM-Instituut voor Plasmafysica Rijnhuizen (Netherlands) [6921-27]



Sessions 3 and 4 run concurrently with sessions 5 and 6.

SESSION 4

Conv. Ctr. B1 Tues. 4:10 to 6:00 pm

EBDW I

Session Chairs: **Laurent Pain**, STMicroelectronics (France); **Hans Loeschner**, IMS Nanofabrication AG (Austria)

4:10 pm: **Challenges in electron-beam lithography for high-resolution template fabrication for patterned media** (*Invited Paper*), XiaoMin Yang, Shuaigang Xiao, Seagate Technology LLC [6921-15]

4:40 pm: **EBDW technology for EB shuttle at 65-nm node and beyond**, Takashi Maruyama, Yoshinori Kojima, Yasushi Takahashi, Masaki Takakuwa, e-Shuttle, Inc. (Japan) [6921-16]

5:00 pm: **E-beam direct-write alignment strategies for the next-generation node**, Helder Alves, Peter Hahmann, Vistec Electron Beam GmbH (Germany); Carl G. Frase, Physikalisch-Technische Bundesanstalt (Germany); Karl-Heinz Kliem, Vistec Electron Beam GmbH (Germany); Roy Zimmermann, Kang-Hoon Choi, Qimonda Dresden GmbH & Co. OHG (Germany); Dominic J. Gnieser, Harald Bosse, Physikalisch-Technische Bundesanstalt (Germany); Frank Thrum, Qimonda Dresden GmbH & Co. OHG (Germany) [6921-91]

5:20 pm: **Gate-edge roughness in electron-beam direct write and its influence to device characteristics**, Kang-Hoon Choi, Matthias Goldbach, Frank Thrum, Katja Keil, Christoph Hohle, Roy Zimmermann, Mark Tesaro, Thomas Marschner, Johannes Kretz, Qimonda Dresden GmbH & Co. OHG (Germany) [6921-18]

5:40 pm: **Proton beam writing: a platform technology for nano-integration**, Jeroen A. Van Kan, Fang Zhang, Andrew A. Bettiol, Frank Watt, National Univ. of Singapore (Singapore) [6921-54]

SESSION 6

Conv. Ctr. C1 Tues. 4:20 to 6:30 pm

EUV Source I

Session Chair: **Vivek Bakshi**, SEMATECH, Inc.

4:20 pm: **Laser-produced plasma source system development** (*Invited Paper*), David C. Brandt, Igor V. Fomenkov, Alex I. Ershov, Norbert R. Bowering, David W. Myers, William N. Partlo, Alexander N. Bykanov, Georgiy O. Vaschenko, Oleh V. Khodykin, Jerzy R. Hoffman, Ernesto L. Vargas, Christopher P. Chrobak, Juan A. Chavez, Rodney D. Simmons, Anson Hsu, Cymer, Inc. [6921-28]

4:50 pm: **CO₂ laser-produced Sn-plasma source for high-volume manufacturing EUV lithography**, Akira Endo, Yoshifumi Ueno, Georg Soumagne, Masaki Nakano, Hiroshi Komori, Hideo Hoshino, Takashi Sugauma, Takayuki Yabu, Takeshi Asayama, Krzysztof Nowak, Masato Moriya, Hiroshi Someya, Tamotsu Abe, Hakaru Mizoguchi, Akira Sumitani, Koichi Toyoda, Extreme Ultraviolet Lithography System Development Association (Japan) [6921-29]

5:10 pm: **Enabling source technology for current and future EUVL exposure tools**, Masaki Yoshioka, Denis Bolshukhin, Guido Hergenhan, Juergen Kleinschmidt, Vladimir Korobochko, Guido Schriever, Max Christian Schuermann, Uwe Stamm, Chinh Duc Tran, Christian Ziener, XTREME technologies GmbH (Germany) [6921-30]

5:30 pm: **Sn DPP source collector modules for HVM**, Marc Corthout, Jeroen Jonkers, Philips GmbH (Germany); Willi Neff, Fraunhofer Institute for Lasertechnology (Germany); Peter Zink, Philips GmbH (Germany) [6921-31]

5:50 pm: **EUV-source collector module development based on tin-doped droplet target technology and multiplexed industrial solid state lasers**, Kazutoshi Takenoshita, Simi A. George, Jose Cunado, Revani Kamptaprasad, Martin C. Richardson, College of Optics & Photonics/Univ. of Central Florida; Ben Fulford, Ian Henderson, Nick Hay, Samir S. Ellwi, Powerlase Ltd. (United Kingdom) [6921-32]

6:10 pm: **Overcoming the parametric trade-offs in laser plasma sources for extreme ultraviolet lithography**, Davide R. Bleiner, Bob Rollinger, Andrea Giovannini, Reza S. Abhari, Swiss Federal Institute of Technology (Switzerland) [6921-109]

Conv. Ctr. A2. Tues. 6:30 to 8:00 pm

Panel Discussion on Future Projection Lithography: Optical or EUV?

Panel Moderators: **Bruno M. LaFontaine**, Advanced Micro Devices, Inc.; **Nigel R. Farrar**, Cymer, Inc.

Panelists: **Timothy A. Brunner**, IBM, Thomas J. Watson Research Ctr.; **Willard E. Conley**, Freescale Semiconductor, Inc.; **Benjamin G. Eynon**, SEMATECH, Inc.; **Tatsuhiko Higashiki**, Toshiba Corp. (Japan); **Winfried M. Kaiser**, Carl Zeiss SMT AG (Germany); **Kurt G. Ronse**, IMEC (Belgium); **Anthony Yen**, Taiwan Semiconductor Manufacturing Co. Ltd. (Taiwan)

Joint Panel Discussion with Conferences 6921 and 6924.

As Moore's law drives IC dimensions ever smaller, it has been assumed that, at some node, some non-optical patterning technology would take the lead for IC manufacturing. Currently, EUV lithography is the top contender for that position. Yet, EUV has been delayed from its previous targets of 45nm and 32nm, while new advances in immersion lithography and various RETs have extended the life of conventional 193nm lithography generations beyond what was originally forecast.

This panel addresses the current forecast of requirements from both the memory and MPU perspectives for the 22nm node and beyond, and asks: can optical lithography, with all its tricks, have high enough yield? Can EUV, with all its problems, be ready in time? Will an alternative technology emerge and surprise us all? Or, will we all call it quits and give Moore's Law a rest?

Conference 6921 • Convention Center B1

Wednesday 27 February

SESSION 7

Conv. Ctr. B1 Wed. 8:00 to 10:10 am

EUV Source II

Session Chair: **Michael Goldstein**, Intel Corp.

8:00 am: **Advanced laser-produced EUV light source for HVM with conversion efficiency of 5-6% and B-field mitigation of ions** (*Invited Paper*), Katsunobu Nishihara, Atsushi Sunahara, Osaka Univ. (Japan); Akira Sasaki, Japan Atomic Energy Research Institute (Japan); Masanori Nunami, Masakatsu Murakami, Osaka Univ. (Japan); Hajime Tanuma, Tokyo Metropolitan Univ. (Japan); Kazumi Fujima, Univ. of Yamanashi (Japan); Hiroyuki Furukawa, Osaka Univ. (Japan); Fumihiko Koike, Kitasato Univ. (Japan); Takeshi Nishikawa, Okayama Univ. (Japan); Shinsuke Fujioaka, Hiroaki Nishimura, Yoshinori Shimada, Tatsuya Aota, Noriaki Miyanaga, Yasukazu Izawa, Kunioki Mima, Osaka Univ. (Japan) [6921-33]

8:30 am: **High-conversion efficiency tin-doped droplet fiber laser-driven plasma source development**, Simi A. George, Kazutoshi Takenoshita, Jose Cunado, Revani Kamptaprasad, Martin C. Richardson, College of Optics & Photonics/Univ. of Central Florida; Kai-Chung Hou, Almantas Galvanauskas, Univ. of Michigan [6921-34]

8:50 am: **Characteristics of a minimum-debris optimum conversion efficiency tin-based LPP source**, Bob Rollinger, Davide R. Bleiner, Ndaona Chokani, Reza S. Abhari, ETH Zürich (Switzerland) [6921-35]

9:10 am: **Enhanced reflectivity and stability of high-temperature LPP collector mirrors**, Torsten Feigl, Sergiy Yulin, Nicolas Benoit, Marco Perske, Mark Schuermann, Norbert Kaiser, Fraunhofer-Institut für Angewandte Optik und Feinmechanik (Germany); Norbert R. Böwering, Oleh V. Khodykin, Igor V. Fomenkov, David C. Brandt, Cymer, Inc. [6921-36]

9:30 am: **Thermal and optical characterization of collectors**, Adam N. Brunton, Media Lario Technologies (Italy); Giovanni Bianucci, Gian Luca Cassol, Jean-Marc Gery, Boris Grek, Fabio Zocchi, Media Lario S.r.l. (Italy); Arnaud Mauder, Klaus Bergmann, Fraunhofer-Institut für Lasertechnik (Germany); Hans Scheuermann, Peter Zink, Philips Extreme UV GmbH (Germany) [6921-37]

9:50 am: **Multidimensional simulation and optimization of hybrid laser and discharge plasma devices for EUV lithography**, Ahmed Hassanein, Argonne National Lab. and Argonne National Laboratory; Valeryi A. Sizyuk, Tatyana S. Sizyuk, Argonne National Lab. [6921-38]

Coffee Break. 10:10 to 10:40 am

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Conference 6921 • Convention Center B1/Concurrent Sessions C1

Session 8, 9 and 10 run concurrently with session 11, 12, and 13.

SESSION 8

Conv. Ctr. B1 Wed. 10:40 am to 12:20 pm

EUV Contamination

Session Chair: Michael J. Lercel, SEMATECH, Inc.

10:40 am: **Radiation-induced defect formation and reactivity of model TiO₂ capping layers with MMA: a comparison with Ru**, Theodore E. Madey, Boris V. Yakshinskiy, M. Nejib Hedhili, Rutgers Univ. [6921-39]

11:00 am: **Lifetime evaluation of EUVL masks based on carbon contamination: dependence on capping materials**, Sung Min Huh, Hoon Kim, Gisung Yoon, Jaehyuck Choi, Han-Shin Lee, Dong Gun Lee, Byungsup Ahn, Dongwan Kim, Seoung Sue Kim, Han Ku Cho, SAMSUNG Electronics Co., Ltd. (South Korea); Takeo Watanabe, Hiroo Kinoshita, Univ. of Hyogo (Japan) [6921-40]

11:20 am: **Carbon contamination of EUV mask: film characterization, impact on lithographic performance, and cleaning**, Yasushi Nishiyama, Toshihisa Anazawa, Hiroaki Oizumi, Iwao Nishiyama, Osamu Suga, Semiconductor Leading Edge Technologies, Inc. (Japan); Kazuki Abe, Satoru Kagata, Akira Izumi, Kyushu Institute of Technology (Japan) [6921-41]

11:40 am: **Studies of carbon growth on multilayer mirrors designed for EUV lithography**, Shannon Hill, Charles Tarrío, Ivan Ermanoski, Thomas B. Lucatorto, National Institute of Standards and Technology; Theodore Madey, Elena Loginova, Boris Yakshinskiy, Rutgers Univ. [6921-42]

12:00 pm: **Mo/Si multilayers with enhanced TiO₂- and RuO₂-capping layers**, Sergiy A. Yulin, Nicolas Benoit, Torsten Feigl, Norbert Kaiser, Fraunhofer-Institut für Angewandte Optik und Feinmechanik (Germany); Ming Fang, Manish Chandhok, Intel Corp. [6921-43]

Lunch/Exhibition Break 12:20 to 1:30 pm

SESSION 9

Conv. Ctr. B1 Wed. 1:30 to 3:00 pm

EUV Imaging

Session Chair: Sung-Woo Lee, SAMSUNG Electronics Co., Ltd. (South Korea)

1:30 pm: **Smoothing-based fast model for images of isolated buried EUV multilayer defects** (*Invited Paper*), Chris H. Clifford, Andrew R. Neureuther, Univ. of California/Berkeley [6921-44]

2:00 pm: **Aberration budget in extreme ultraviolet lithography**, Yumi Nakajima, Takashi Sato, Kazuya Sato, Ryoichi Inanami, Tetsuro Nakasugi, Tatsuhiko Higashiki, Toshiba Corp. (Japan) [6921-45]

2:20 pm: **EUV pattern shift and bias compensation strategies**, Thomas Schmoeller, Hans Koop, Thomas Klimpel, Synopsys GmbH (Germany); Insung Kim, Gian F. Lorusso, Rik Jonckheere, Mieke Goethals, Kurt Ronse, IMEC (Belgium) [6921-46]

2:40 pm: **Study of system performance in SFET**, Naosuke Nishimura, Gaku Takahashi, Toshihiko Tsuji, Hideki Morishima, Shigeyuki Uzawa, Canon Inc. (Japan) [6921-47]

3:00 pm: **Effects of aberration and flare on the lithographic performance of SFET**, Yuusuke Tanaka, Kazuo Tawarayama, Shunko Magoshi, Seiichiro Shirai, Hiroyuki Tanaka, Semiconductor Leading Edge Technologies, Inc. (Japan) [6921-132]

Coffee Break 3:20 to 3:50 pm

SESSION 11

Conv. Ctr. C1 Wed. 10:30 am to 12:20 pm

Nanoimprint III

Session Chair: William M. Tong, Hewlett-Packard Labs.

10:30 am: **A cost-effective nanoimprint lithography module** (*Invited Paper*), Wei Wu, William M. Tong, Hewlett-Packard Labs.; Jonathan Bartman, Yufeng Chen, Hewlett-Packard Co.; Robert G. Walmsley, Zhaoning Yu, Duncan Stewart, Inkyu Park, Carl E. Picciotto, Jun Gao, Shih Wang, R. Stanley Williams, Hewlett-Packard Labs. [6921-87]

11:00 am: **Etching of 42-nm and 32-nm half-pitch features patterned using step and Flash(r) imprint lithography**, Dwayne L. LaBrake, Cynthia B. Brooks, Niyaz Khusnatdinov, Molecular Imprints, Inc. [6921-14]

11:20 am: **High-resolution defect inspection of step and flash imprint lithography for the 32-nm node and beyond**, Ian McMackin, John G. Maltabes, Joseph Perez, Wesley Martin, Kosta S. Selinidis, Douglas J. Resnick, S. V. Sreenivassan, Molecular Imprints, Inc. [6921-86]

11:40 am: **Porosity characteristics of ultra-low dielectric insulator films directly patterned by nano-imprint lithography**, Hyun Wook Ro, Hae-Jeong Lee, National Institute of Standards and Technology; Ken-ichi Nihara, Hiroshi Jinai, Kyoto Institute of Technology (Japan); David W. Gidley, Univ. of Michigan; Do Y. Yoon, Seoul National Univ. (South Korea); Christopher L. Soles, National Institute of Standards and Technology [6921-85]

12:00 pm: **A method for fabricating below 22-nm feature patterns in quartz mold**, Atsunori Terasaki, Junichi Seki, Haruhito Ono, Canon Inc. (Japan) [6921-88]

Lunch/Exhibition Break 12:20 to 1:30 pm

SESSION 12

Conv. Ctr. C1 Wed. 1:30 to 3:00 pm

Parallel E-Beam Systems

Session Chair: Timothy R. Groves, SUNY/Univ. at Albany

1:30 pm: **Projection maskless lithography (PML2): proof-of-concept setup and first experimental results** (*Invited Paper*), Christof Klein, Elmar Platzgummer, Hans Loeschner, Gerhard Gross, IMS Nanofabrication AG (Austria); Pavel Dolezel, Martin Tmej, Vladimir Kolarik, DELONG INSTRUMENTS a.s. (Czech Republic); Wolfram Klingler, Florian Letzkus, Jörg Butschke, Mathias Irmscher, Institut für Mikroelektronik Stuttgart (Germany); Martin Witt, Wolfgang Pilz, Fraunhofer Institut für Siliziumtechnologie (Germany) [6921-93]

2:00 pm: **MAPPER: high-throughput maskless lithography**, Marco J. Wieland, Guido de Boer, Pieter Kruit, Gerard F. ten Berge, Anne M. C. Houkes, Remco J. A. Jager, Ton van de Peut, Jerry J. M. Peijster, Erwin Slot, Stijn W. H. K. Steenbrink, Tijs F. Teepen, Alexander van Veen, Bert J. Kampherbeek, Mapper Lithography B. V. (Netherlands) [6921-92]

2:20 pm: **Modeling of influence of beam edge acuity**, Norman W. Parker, Daniel Henry, Tirunelveli S. Ravi, Multibeam Systems Inc. [6921-17]

2:40 pm: **Patterning fidelity on low-energy multiple-electron-beam direct-write lithography**, Shih-Ming Chang, Wen-Chun Huang, Shy-Jay Lin, Jeng-Hong Chen, Tsai-Sheng Gau, Burn Lin, Taiwan Semiconductor Manufacturing Co. Ltd. (Taiwan); Erwin Slot, Marco J. Wieland, Bert J. Kampherbeek, Mapper Lithography B. V. (Netherlands) [6921-19]

Coffee Break 3:00 to 3:30 pm

Conference 6921 • Convention Center B1/ Concurrent Session 10, Marriott San Jose Ballroom Salon III

Session 8, 9 and 10 run concurrently with session 11, 12, and 13.

SESSION 10

SESSION 13

Marriott San Jose Ballroom Salon III Wed. 3:50 to 6:10 pm

Conv. Ctr. B1 Wed. 3:50 to 5:10 pm

Joint Session on EUV Resists

EBDW II

Session Chairs: **Bruno M. LaFontaine**, Advanced Micro Devices, Inc.;
Ernisse Steve Putna, Intel Corp.

Session Chairs: **Timothy R. Groves**, SUNY/Univ. at Albany; **James W. Blatchford**, Texas Instruments Inc.

Joint session with conference 6923: Advances in Resist Materials and Processing XXV.

3:50 pm: **Resolution, LER, and sensitivity limitations of photoresists**, Gregg M. Gallatin, Applied Math Solutions, LLC; Patrick Naulleau, Lawrence Berkeley National Lab.; Robert Brainard, Univ. at Albany; Dimitra Niakoula, Lawrence Berkeley National Lab.; Kim Dean, SEMATECH, Inc. [6921-55]

3:50 pm: **MAGIC: a European program to push the insertion of maskless lithography for IC manufacturing**, Laurent Pain, Beatrice Icard, STMicroelectronics (France); Serge Tedesco, Commissariat à l'Energie Atomique (France); Bert J. Kampherbeek, Mapper Lithography B. V. (Netherlands); Gerhard Gross, Christof Klein, Hans Loeschner, Elmar Platzgummer, IMS Nanofabrication AG (Austria); Ray E. Morgan, Sr., Synopsys, Inc.; Serdar Manakli, STMicroelectronics (France); Johannes Kretz, Christoph Holhe, Kang-Hoon Choi, Frank Thrum, Qimonda Dresden GmbH & Co. OHG (Germany); Elyakim Kassel, KLA-Tencor Corp. (Israel); Wolfgang Pilz, Fraunhofer Institut für Siliziumtechnologie (Germany); Katja Keil, Fraunhofer-Ctr. Nanoelektronische Technologien (Germany); Jorg Butschke, Mathias Irmischer, Florian Letzkus, Institut für Mikroelektronik Stuttgart (Germany); Peter Hudek, Fachhochschule Vorarlberg Univ. (Austria); Anagnostis Paraskevopoulos, Fraunhofer-Institut für Nachrichtentechnik Heinrich-Hertz-Institut (Germany) [6921-49]

4:10 pm: **Evaluation of EUV resist materials for use at the 32-nm half-pitch node**, Thomas I. Wallow, Advanced Micro Devices, Inc.; Robert Brainard, Greg Denbeaux, Univ. at Albany; Chiew-Seng Koay, IBM Corp.; Warren Montgomery, Univ. at Albany; Karen Petrillo, IBM Thomas J. Watson Research Ctr.; Yayi Wei, Qimonda North America Corp.; Obert Wood, Advanced Micro Devices, Inc. [6921-56]

4:30 pm: **Extreme ultraviolet resist outgassing measurements and their effect on nearby surfaces**, Gregory Denbeaux, Rashi Garg, Chimaobi Mbanaso, Justin Waterman, Alin Antohe, Leonid Yankulin, Yu-Jen Fan, Univ. at Albany; Kim Dean, Andrea Wüest, SEMATECH, Inc. [6921-57]

4:10 pm: **High-throughput maskless lithography: low-voltage versus high-voltage**, Bert J. Kampherbeek, Marco J. Wieland, Mapper Lithography B. V. (Netherlands); Jeng H. Chen, Shih M. Chang, Taiwan Semiconductor Manufacturing Co. Ltd. (Taiwan); Michael F. Pas, Texas Instruments Inc.; Johannes Kretz, Christoph K. Hohle, Qimonda Dresden GmbH & Co. OHG (Germany); David van Steenwinkel, NXP Semiconductors (Belgium); Serdar Manakli, Jean-Christophe Le-Denmat, Laurent Pain, STMicroelectronics (France) [6921-20]

4:50 pm: **Quantitative measurement of outgas products from EUV photoresists**, Charles Tarrío, Shannon Hill, Thomas Lucatorto, Jay Hendricks, Pat Abbott, Bruce Benner, National Institute of Standards and Technology. [6921-58]

4:30 pm: **Shot minimization for throughput improvement of character projection electron-beam direct writing**, Hai D. M. Pham, Tetsuya Iizuka, Makoto Ikeda, Kunihiko Asada, The Univ. of Tokyo (Japan) [6921-51]

5:10 pm: **Quantum yield, contrast curves, and optical density of EUV and 193i photoresists**, Robert L. Brainard, Elsayed Hassanein, Patrick P. Naulleau, Univ. at Albany; Gregg M. Gallatin, Applied Math Solutions, LLC; Richard J. Matyi, Univ. at Albany; James W. Thackeray, Kathleen Spear-Alfonso, Rohm and Haas Electronic Materials; Matthew Malloy, Anwar Khurshid, Emil C. Piscani, Andrew C. Rudack, Jeff D. Byers, Kim R. Dean, SEMATECH, Inc. [6921-59]

5:30 pm: **Rational design and synthesis of non-CA high-sensitivity polymeric EUV resists**, Andrew K. Whittaker, Kevin Jack, Heping Liu, The Univ. of Queensland (Australia); Idriss Blakely, Univ. of Queensland (Australia); David J. T. Hill, The Univ. of Queensland (Australia); Wang Yueh, Heidi B. Cao, Michael J. Leeson, Intel Corp. [6923-55]

4:50 pm: **Shaped beam technique using a novel 3rd order imaging approach**, Tadashi Kotsugi, Takashi Fuse, Hidetoshi Kinoshita, Tokyo Electron Ltd. (Japan); Norman W. Parker, Multibeam Systems Inc. [6921-53]

5:50 pm: **A resist materials study for resolution and LWR improvement in EUV lithography**, Sou Kamimura, Katsuhiko Yamashita, Naoyuki Nishikawa, Fuji Photo Film Co., Ltd. (Japan). [6923-56]

Thursday 28 February

SESSION 14

Conv. Ctr. B1 Thurs. 8:00 to 9:50 am

EUV Mask

Session Chair: **R. Scott Mackay**, Mackay and Associates

8:00 am: **Dependence of EUV mask-printing performance on blank architecture** (*Invited Paper*), Rik M. Jonckheere, Anne-Marie Goethals, Gian F. Lorusso, Ivan K. Pollentier, Kurt G. Ronse, IMEC (Belgium) [6921-62]

8:30 am: **Ion-beam deposition for defect-free EUVL mask blanks**, Patrick A. Kearney, C.C. Lin, SEMATECH, Inc.; Takashi Sugiyama, Asahi Glass Co., Ltd.; Chan-Uk Jeon, SEMATECH, Inc. and SAMSUNG Electronics Co., Ltd. (South Korea); Rajul V. Randive, Veeco Instruments Inc.; Ira Reiss, Paul Mirkarimi, Eberhard A. Spiller, Renga Rajan, Veeco Ion Beam Equipment Inc. [6921-63]

8:50 am: **Determining the critical size of EUV-mask substrate defects**, HakSeung Han, Wonil Cho, SEMATECH, Inc.; Kenneth A. Goldberg, Lawrence Berkeley National Lab.; Anton Barty, Lawrence Livermore National Lab.; Chanuk Jeon, Stefan Wurm, SEMATECH, Inc. [6921-65]

9:10 am: **Status of EUV-reticle handling solution in meeting 32 and 22-nm HP-EUV lithography**, Long He, Stefan Wurm, Phil Seidel, Kevin Orvek, SEMATECH, Inc. [6921-66]

9:30 am: **Sub-50-nm cleaning-induced damage in EUV mask blanks**, Abbas Rastegar, Sean K. Eichenlaub, Arun Johnkadaksham, Vivek Kapila, Pat Marmillion, SEMATECH, Inc. [6921-67]

Coffee Break. 9:50 to 10:30 am

SESSION 15

Conv. Ctr. B1 Thurs. 10:30 am to 12:10 pm

EUV Metrology

Session Chair: **Kazuaki Suzuki**, Nikon Corp. (Japan)

10:30 am: **EUV-source development at Energetiq**, Matthew Partlow, Stephen Horne, Matthew Besen, Donald Smith, Paul Blackborow, Deborah Gustafson, Energetiq Technology, Inc. [6921-68]

10:50 am: **Accuracy, precision, and stability of EUV mask reflectometry**, Rainer Lebert, Christian Wies, AIXUV GmbH (Germany); Masaki Mikami, Asahi Glass Co., Ltd. (Japan) [6921-69]

11:10 am: **EUV-mask inspection tool using high-NA DUV inspection tool**, Yongkyoo Choi, Yongdae Kim, Munsik Kim, Sunghyun Oh, Oscar Han, Hynix Semiconductor Inc. (South Korea) [6921-70]

11:30 am: **Accelerated contamination testing and imaging of EUV Masks**, Gregory Denbeaux, Yu-Jen Fan, Alin Antohe, Leonid Yankulin, Rashi Garg, Adam Wasserzug, Univ. at Albany; Obert Wood, Advanced Micro Devices, Inc.; Francis Goodwin, Qimonda North America Corp.; Chiew-Seng Koay, IBM Corp. [6921-71]

11:50 am: **Lifetime determination of EUV sources: reflectivity, neutral, and ion debris measurements**, David N. Ruzic, Shailendra N. Srivastava, Keith C. Thompson, John Sporre, Carlos H. Castano, Ramasamy Raju, Univ. of Illinois at Urbana-Champaign; Vivek Bakshi, SEMATECH, Inc. [6921-72]

Lunch Break. 12:10 to 1:20 pm

SESSION 16

Conv. Ctr. B1 Thurs. 1:20 to 3:30 pm

Directed Self Assembly

Session Chairs: **Kevin T. Turner**, Univ. of Wisconsin/Madison; **Daniel J. C. Herr**, Semiconductor Research Corp.

1:20 pm: **NIL mold manufacturing using self-organized diblock copolymer as patterning template** (*Invited Paper*), Naoko Kihara, Hiroyuki Hieda, Katsuyuki Naito, Toshiba Corp. (Japan) [6921-73]

1:50 pm: **Directed polymer self-assembly for patterning applications**, Joy Y. Cheng, Daniel P. Sanders, Ho-Cheol Kim, Charles Rettner, William D. Hinsberg, Linda K. Sundberg, Sally A. Swanson, Robert D. Allen, IBM Almaden Research Ctr. [6921-74]

2:10 pm: **Probing 3D morphological evolution in directed self assembly**, Ronald L. Jones, Brian Berry, Alamgir Karim, National Institute of Standards and Technology. [6921-75]

2:30 pm: **Rapid directed self-assembly of Lamellar microdomains from a block copolymer containing hybrid**, Ho-Cheol Kim, Joy Cheng, Oun-Ho Park, Ricardo Ruiz, IBM Almaden Research Ctr.; Charles Black, IBM Thomas J. Watson Research Ctr.; Jed Pitera, Myron Flickner, IBM Almaden Research Ctr. [6921-76]

2:50 pm: **Pattern fidelity of chemical template-directed thin block copolymer films**, Sangcheol Kim, National Institute of Standards and Technology and Univ. of Maryland/College Park; Ronald L. Jones, Alamgir Karim, National Institute of Standards and Technology; R. M. Briber, Univ. of Maryland/College Park; Ho-Cheol Kim, IBM Almaden Research Ctr. ... [6921-77]

3:10 pm: **Device-oriented directed self-assembly of Lamellar microdomains from a block copolymer containing hybrid**, Ho-Cheol Kim, Joy Cheng, Oun-Ho Park, Charles Rettner, IBM Almaden Research Ctr. [6921-78]

Coffee Break. 3:30 to 4:00 pm

SESSION 17

Conv. Ctr. B1 Thurs. 4:00 to 5:40 pm

New Patterning Technologies

Session Chairs: **Frank M. Schellenberg**, Mentor Graphics Corp.; **James Alexander Liddle**, National Institute of Standards and Technology

4:00 pm: **Nanopatterning with a single high-transmission nanometal aperture system**, Yong Woo Kim, Sinjeung Park, Eungman Lee, Jae W. Hahn, Yonsei Univ. (South Korea) [6921-79]

4:20 pm: **Etchless UV-NIL process for patterning photonic crystal structure onto OLED substrate**, Jun-Ho Jeong, Korea Institute of Machinery and Materials (South Korea); Sohee Jeon, Seoul National Univ. (South Korea); Jongyoun Shim, Korea Institute of Machinery and Materials (South Korea); Jae Ryoun Youn, Seoul National Univ. (South Korea); Ki-Don Kim, Dae-Geun Choi, Junhyuk Choi, Dong-Il Lee, Ali Ozhan Altun, Soon-Won Lee, Eung-Sug Lee, Korea Institute of Machinery and Materials (South Korea) [6921-80]

4:40 pm: **A photolithographic process for grossly nonplanar substrates**, Gavin L. Williams, Nicholas L. Seed, Andrew Maiden, Jose J. Toriz-Garcia, The Univ. of Sheffield (United Kingdom); Richard McWilliam, Alan Purvis, Richard Curry, Simon Johnson, Univ. of Durham (United Kingdom) [6921-81]

5:00 pm: **Submicron patterning on flexible substrates by optical reduction lithography**, Wim de Laat, ASML Netherlands B.V. (Netherlands); Maria Peter, Francois Furthner, Peter Giesen, TNO (Netherlands); Cheng-Qun Gui, ASML Netherlands B.V. (Netherlands); Erwin R. Meinders, Philips Research Labs. (Netherlands) [6921-82]

5:20 pm: **1-nm alignment and overlay control precision by using electronic parallel datum for all the lithography of semiconductor industry**, Xiang-Wen Xiong, Zhongheng High-Tech Inc. (China) [6921-83]

Conference 6921 • Convention Center B1

Posters-Thursdays

The following posters will be displayed all day Thursday. Authors will be present during the formal poster session Thursday evening between 6:00 and 8:00 pm for discussion. Authors may set-up their posters after 9:00 am on Thursday.

Conv. Ctr. Hall 3 Thurs. 6:00 to 8:00 pm

Nanoimprint

Residual-layer free nanoimprint lithography for direct patterning, Franklin C. Hong, National Cheng Kung Univ. (Taiwan); Bo-Yun Hsueh, United Microelectronics Corp. [6921-90]

Integration issues in step and repeat UV nanoimprint lithography, Christelle Charpin-Nicolle, J. Chiaroni, Lab. d'Electronique de Technologie de l'Information (France); Jean Massin, STMicroelectronics (France); Mathias Irmscher, Institut für Mikroelektronik Stuttgart (Germany); Boris Vratzov, NT&D (Germany); Huib Van Vossen, Univ. Twente (Netherlands); Pascal Gubbini, Molecular Imprints, Inc. (France) [6921-149]

EBDW

Simulation of robustness of a new e-beam column with the 3rd order imaging technique, Koji Takeya, Takashi Fuse, Hidetoshi Kinoshita, Tokyo Electron Ltd. (Japan); Norman W. Parker, Multibeam Systems Inc. [6921-94]

Applying photolithography friendly design to e-beam direct writing in 65-nm node and beyond, Hiroshi Hoshino, Yasuhide Machida, Kozo Ogino, Fujitsu Ltd. (Japan); Masaaki Miyajima, Fujitsu VLSI Ltd. (Japan); Takashi Maruyama, Yoshinori Kojima, Shinji Sugatani, e-Shuttle, Inc. (Japan) [6921-96]

DSA and New Patterning Technologies

Directed self-assembly using curved templates, Xiaohua Zhang, Silvia Lacerda, Brian Berry, Ronald Jones, Alamgir Karim, National Institute of Standards and Technology [6921-97]

Di-block copolymer directed self-assembly for CMOS device fabrication, Li-Wen Chang, Marissa Caldwell, H.-S. Philip Wong, Stanford Univ. [6921-98]

An ultra-small poly-Si Gate (Lg=30nm) FinFET fabricated with 193-nm photolithography and TEOS hard mask etching, Wen-Shiang Liao, United Microelectronics Corp. (Taiwan) [6921-99]

Diffraction feature of microlens array with a small aperture size, Seungryong Park, Jinho Park, Hakyu Choi, Young-Je Yun, Jeahae Kim, Keeho Kim, Dongbu Electronics Co., Ltd. (South Korea) [6921-100]

Modeling of photoresist profiles in plasmonic lithography, Eungman Lee, Jae W. Hahn, Yonsei Univ. (South Korea) [6921-101]

EUV System

Scattering of EUV optics: substrate, coating, and degradation effects, Sven Schröder, Nicolas Benoit, Torsten Feigl, Angela Duparré, Andreas Tünnermann, Fraunhofer-Institut für Angewandte Optik und Feinmechanik (Germany) [6921-102]

Progress in EUV-IL at University of Wisconsin, Yang-Chun Cheng, Artak Isoyan, Fan Jiang, John Wallace, Mikhail Efremov, Paul Nealey, Franco Cerrina, Univ. of Wisconsin/Madison [6921-103]

Study on the optimization of venting procedure using specially designed vent diffusers for semiconductor vacuum process tools, Mary Ann Ford, Christopher Vroman, Marshall Randolph, Entegris, Inc. [6921-104]

Study of laser-driven extreme ultraviolet (EUV) source with tin-droplets: elemental study and integrated experiments, Tatsuya Aota, Yuki Nakai, Shinsuke Fujioka, Osaka Univ. (Japan); Etsuo Fujiwara, Univ. of Hyogo (Japan); Masashi Shimomura, Hiroaki Nishimura, Nobukatsu Nishihara, Noriaki Miyayama, Yasukazu Izawa, Kunioki Mima, Osaka Univ. (Japan) [6921-105]

EUV wavefront measurement of six-mirror optics using EWMS, Katsumi Sugisaki, Masashi Okada, Katsura Otaki, Yucong Zhu, Jun Kawakami, Katsuhiko Murakami, Nikon Corp. (Japan); Chidane Ouchi, Masanobu Hasegawa, Seima Kato, Takayuki Hasegawa, Hideo Yokota, Tokuyuki Honda, Canon Inc. (Japan); Masahito Niibe, Univ. of Hyogo (Japan) [6921-106]

Evaluation result of Selete's exposure tool, Kazuo Tawarayama, Semiconductor Leading Edge Technologies, Inc. (Japan); Shunko Magoshi, Toshiba Corp. (Japan); Yuusuke Tanaka, Association of Super-Advanced Electronics Technologies (Japan); Seiichiro Shirai, Hiroyuki Tanaka, Semiconductor Leading Edge Technologies, Inc. (Japan) [6921-107]

EUV Source

Bubble tin targets for LPP EUV-light source with high-CE and high-repletion supply, Keiji Nagai, Liqin Ge, Takayoshi Norimatsu, Hiroaki Nishimura, Noriaki Miyayama, Katsunobu Nishihara, Yasukazu Izawa, Kunioki Mima, Osaka Univ. (Japan) [6921-110]

Medium-power EUV-sources for metrology, Rainer Lebert, Christian Wies, Bernhard Jäggle, AIXUV GmbH (Germany) [6921-111]

EUV and debris characteristics of a laser plasma, Shoichi Kubodera, Masanori Kaku, Sumihiro Suetake, Yusuke Senba, Masahito Katto, Univ. of Miyazaki (Japan) [6921-112]

Magnetic debris mitigation of a CO₂ laser-produced Sn plasma, Yoshifumi Ueno, Georg Soumagne, Masato Moriya, Takashi Suganuma, Takayuki Yabu, Tamotsu Abe, Hirosh Komori, Akira Endo, Akira Sumitani, Extreme Ultraviolet Lithography System Development Association (Japan) [6921-113]

Sn-droplet target development for laser-produced plasma EUV-light source, Masaki Nakano, Takayuki Yabu, Hiroshi Someya, Tamotsu Abe, Georg Soumagne, Akira Endo, Akira Sumitani, Extreme Ultraviolet Lithography System Development Association (Japan) [6921-114]

LPP EUV-light source employing high-power CO₂ laser, Hideo Hoshino, Takashi Suganuma, Tamotsu Abe, Takeshi Asayama, Krzysztof Nowak, Masato Moriya, Akira Endo, Akira Sumitani, Extreme Ultraviolet Lithography System Development Association (Japan) [6921-115]

Plasma Sn cleaning integrated in EUV source system, Hyungjoo Shin, Ramasamy Raju, David N. Ruzic, Univ. of Illinois at Urbana-Champaign [6921-116]

Modeling of EUV emission features and conversion efficiency from laser-generated tin plasmas for nanolithography, Sivanandan S. Harilal, Joseph J. MacFarlane, Igor E. Golovkin, Pamela R. Woodruff, Ping Wang, Prism Computational Sciences, Inc. [6921-117]

LPP EUV-source development for HVM, Igor V. Fomenkov, Alex I. Ershov, Norbert R. Bowering, David W. Myers, William N. Partlo, Alexander N. Bykanov, Georgiy O. Vaschenko, Oleg V. Khodykin, Jerzy R. Hoffman, Ernesto L. Vargas, Christopher P. Chrobak, David C. Brandt, Cymer, Inc. [6921-118]

Near-normal incidence collector development at SAGEM, Roland Geyl, Xavier F. Bozec, SAGEM SA (France) [6921-148]

EUV Contamination

Implementation of in-situ reflectivity measurement capability in an EUV ROX system at Albany to study optics contamination, Rashi Garg, Leonid Yankulin, Alin Antohe, Univ. at Albany; Andrea Wuest, SEMATECH, Inc.; Eric M. Gullikson, Lawrence Berkeley National Lab.; Steve E. Grantham, Charles Tarrío, National Institute of Standards and Technology; Sasa Bajt, Lawrence Livermore National Lab.; Gregory P. Denbeaux, Univ. at Albany [6921-119]

Ionic debris assessment of various EUVL systems, Carlos H. Castano, David N. Ruzic, Shailendra N. Srivastava, Keith C. Thompson, John Sporre, Univ. of Illinois at Urbana-Champaign; Vivek Bakshi, SEMATECH, Inc. [6921-120]

NEG(non-evaporable getter) pumps for organic compounds and water removal in EUVL tools, Andrea Conte, Paolo Manini, Stefano Raimondi, SAES Getters S.p.A. (Italy) [6921-121]

Cleaning of tin debris using hydrogen radicals and its electronic structure compared with hydrides of Ge and Si, Kazumi Fujima, Kenzo Hiraoka, Itsuki Banno, Univ. of Yamanashi (Japan); Yoshihiko Yuba, Katsunobu Nishihara, Osaka Univ. (Japan) [6921-122]

Performance and lifetime of EUV-source collectors measured with a full-size EUV-collector reflectometer, Ulf Hinze, Boris N. Chichkov, Laser Zentrum Hannover e.V. (Germany); Torsten Feigl, Uwe D. Zeitner, Christoph Damm, Fraunhofer-Institut für Angewandte Optik und Feinmechanik (Germany); Denis Bolshukhin, Jürgen Kleinschmidt, Guido Schriever, Max C. Schürmann, XTREME technologies GmbH (Germany) [6921-123]

Characteristics of additional carbon on the surface of carbon capping layer, Takahiro Nakayama, Canon Inc. (Japan); Hiromitsu Takase, Shigeru Terashima, Yutaka Watanabe, Extreme Ultraviolet Lithography System Development Association (Japan); Takashi Sudo, Canon Inc. (Japan); Yasuaki Fukuda, Takashi Aoki, Extreme Ultraviolet Lithography System Development Association (Japan); Shuichi Matsunari, Nikon Corp. (Japan); Katsuhiko Murakami, Extreme Ultraviolet Lithography System Development Association (Japan); Shintaro Kawata, Yukinobu Kakutani, Nikon Corp. (Japan); Masahito Niibe, Univ. of Hyogo (Japan) [6921-124]

Protection from surface oxidation of Ru-capping layers for EUVL projection-optics mirrors by introducing hydrocarbon gas, Keigo Koida, Masahito Niibe, Yukinobu Kakutani, Univ. of Hyogo (Japan); Shuichi Matsunari, Nikon Corp. (Japan); Takashi Aoki, Shigeru Terashima, Extreme Ultraviolet Lithography System Development Association (Japan); Takahiro Nakayama, Canon Inc. (Japan); Hiromitsu Takase, Yasuaki Fukuda, Extreme Ultraviolet Lithography System Development Association (Japan). [6921-125]

Lithium debris removal by sputtering and evaporation for EUV optics and applications, Martin J. Neumann, Matthew J. Cruce, David N. Ruzic, Univ. of Illinois at Urbana-Champaign. [6921-126]

Surface phenomena related to degradation of EUV mirrors: interaction of ethyl alcohol with ruthenium surfaces, Boris V. Yakshinskiy, Rutgers Univ.; Iwao Nishiyama, Semiconductor Leading Edge Technologies, Inc. (Japan); Andrea Wuest, SEMATECH, Inc.; Theodore E. Madey, Rutgers Univ. [6921-127]

Gas study phase of the reactivity of optical coating materials with hydrocarbons using a desktop size EUV laser, Feng Dong, Scott C. Heinbuch, Elliot R. Bernstein, Jorge J. Rocca, Colorado State Univ. . [6921-150]

EUV Imaging

Particle-contamination analysis for reticles in carrier inner pods, John R. Torczynski, Michael A. Gallis, Daniel J. Rader, Sandia National Labs. [6921-128]

Flare evaluation for 32-nm half-pitch using SFET, Hajime Aoyama, Semiconductor Leading Edge Technologies, Inc. (Japan); Yuusuke Tanaka, Association of Super-Advanced Electronics Technologies (Japan); Nobuyuki M. Iriki, Yukiyasu Arisawa, Toshihiko Tanaka, Semiconductor Leading Edge Technologies, Inc. (Japan) [6921-129]

EUV-simulation extension study for mask shadowing effect and its correction, Hoyoung Kang, ASML Korea Co., Ltd. (South Korea); Steven G. Hansen, ASML US, Inc.; Koen van Ingen Schenau, Jan B. van Schoot, ASML Netherlands B.V. (Netherlands) [6921-130]

Model-based pupil-fill optimization for the SEMATECH Berkeley EUV microfield exposure tool, Jonathan S. Nation, Arizona State Univ.; Patrick P. Naulleau, Lawrence Berkeley National Lab.. [6921-131]

EUV Resist

Vacuum-induced EUV photoresist outgassing, Justin Waterman, Gregory Denbeaux, Univ. at Albany; Kim Dean, SEMATECH, Inc. [6921-133]

Investigation of sensitivity of extreme-ultraviolet resists to out-of-band radiation, Chimaobi Mbanaso, Gregory Denbeaux, Univ. at Albany; Kim Dean, SEMATECH, Inc. [6921-134]

Proximity printing using extreme-ultraviolet radiation, Rashi Garg, Chimaobi Mbanaso, Univ. at Albany; Patrick Naulleau, Lawrence Berkeley National Lab.; Robert Brainard, Gregory P. Denbeaux, Univ. at Albany [6921-135]

Advanced extreme-ultraviolet resist testing using the SEMATECH Berkeley 0.3-NA microfield exposure tool, Patrick P. Naulleau, Lawrence Berkeley National Lab.; Christopher N. Anderson, Univ. of California/Berkeley; Kim R. Dean, SEMATECH, Inc.; Paul E. Denham, Kenneth A. Goldberg, Brian Hoef, Gideon Jones, Lawrence Berkeley National Lab.; Bruno M. LaFontaine, Advanced Micro Devices, Inc.; Dimitra Niakoula, Lawrence Berkeley National Lab.; Thomas I. Wallow, Advanced Micro Devices, Inc. [6921-136]

Benchmarking of commercial EUVL resists at SEMATECH, Andy Ma, Joo-On Park, Kim R. Dean, SEMATECH, Inc. [6921-137]

EUV Mask

Evaluation of TiO₂-SiO₂ ultra-low-expansion glass fabricated by the soot method using the line-focus-beam ultrasonic material characterization system, Jun-ichi Kushibiki, Mototaka Arakawa, Tohoku Univ. (Japan); Akira Fujinoki, Tetsuji Ueda, Shin-Etsu Quartz Products Co., Ltd. (Japan) . [6921-138]

The study of attenuated-PSM structure for extreme ultraviolet lithography with minimized mask shadowing effect, Chang Young Jeong, Byung Hun Kim, Tae Geun Kim, Sangsul Lee, Eun Jin Kim, Hye-Keun H. Oh, In-Sung Park, Jinho Ahn, Hanyang Univ. (South Korea) [6921-139]

Evaluation of EUV scatterometry for CD characterization of EUV masks using rigorous FEM-simulation, Frank Scholze, Christian Laubis, Gerhard Ulm, Physikalisch-Technische Bundesanstalt (Germany); Jan Pomplun, Sven Burger, Frank Schmidt, Zuse Institute Berlin (Germany); Uwe Dersch, Advanced Mask Technology Ctr. (Germany) [6921-140]

Experimental evaluation of out-of-plane distortion of electrically chucked EUV reticle, Kazuya Ota, Takao Taguchi, Mitsuaki Amemiya, Takashi Kamono, Naosuke Nishimura, Tadahiko Takikawa, Youichi Usui, Osamu Suga, Semiconductor Leading Edge Technologies, Inc. (Japan). [6921-141]

Particle-free mask handling techniques and a dual-pod carrier, Mitsuaki Amemiya, Kazuya Ota, Takao Taguchi, Youichi Usui D.D.S., Tadahiko Takikawa, Takashi Kamono, Naosuke Nishimura, Osamu Suga, Semiconductor Leading Edge Technologies, Inc. (Japan) [6921-142]

EUV-mask reflectivity measurements with micron-scale spatial resolution, Kenneth A. Goldberg, Lawrence Berkeley National Lab.; Anton Barty, Lawrence Livermore National Lab.; Senajith B. Rekawa, Charles D. Kemp, Lawrence Berkeley National Lab.; Erdem Ultanir, Intel Corp.; Patrick Kearney, SEMATECH, Inc.; Eric Gullikson, Lawrence Berkeley National Lab.; Hakseung Han M.D., SEMATECH, Inc. [6921-143]

Design of hybrid-type attenuated phase-shift mask with ITO absorber for EUV lithography, Hee Young Kang, Inha Univ. (South Korea); Chang Kwon Hwangbo, Inha Univ. (South Korea) and Optical Society of Korea (South Korea); Mi Kyoung Kim, Inha Univ. (South Korea) [6921-144]

EUV Metrology

At-wavelength reflectometry with a microfocus EUV tube, André Egbert, Stefan Becker, Phoenix EUV Systems & Services GmbH (Germany) . [6921-145]

Evaluating EUV-mask pattern imaging with two EUV microscopes, Kenneth A. Goldberg, Patrick P. Naulleau, Anton Barty, Lawrence Berkeley National Lab.; Hiroo Kionoshita, Kazuhiro Hamamoto, Univ. of Hyogo (Japan); Hak-Seung Han, SEMATECH, Inc. [6921-146]

Design requirements for a stand-alone EUV interferometer, Philippe Michallon, Commissariat à l'Énergie Atomique (France) [6921-147]

Courses of Related Interest

See Course Materials Desk for course descriptions.

SC888 **EUV Lithography** (Bakshi, Soufii, Ahn, Naulleau) Sunday 8:30 am to 6:30 pm

SC890 **Electron-Beam Lithography – Current Use and Recent Advances** (Pfeiffer, McCord) Sunday, 8:30 am to 5:30 pm

SC724 **Optical Lithography Extension: Design for Manufacturing and New Resolution Enhancement Techniques** (Pierrat) Sunday, 1:30 to 5:30 pm

SC831 **Introduction to Scatterometry Metrology: Theory and Application** (Barry, Bao) Sunday, 1:30 to 5:30 pm

SC116 **Lithographic Optimization: A Theoretical Approach** (Mack) Sunday, 8:30 am to 5:30 pm

SC622 **Nano-Scale Patterning with Imprint Lithography** (Sreenivasan, Willson, Resnick) Sunday, 6:00 to 10:00 pm

SC101 **Introduction to Microlithography: Theory, Materials, and Processing** (Willson, Thompson, Bowden) Sunday, 8:30 am to 5:30 pm

SC105 **CD Metrology and Image Formation in the Scanning Electron Microscope (SEM)** (Postek, Wells) Sunday, 8:30 am to 5:30 pm

WS619 **Intellectual Assets for Micro/Nano Electronics and Lithography** (Cole) Monday, 1:30 to 5:30 pm

Metrology, Inspection, and Process Control for Microlithography XXII

Conference Chair: **John A. Allgair**, SEMATECH, Inc. and Advanced Micro Devices, Inc.

Conference Co-Chair: **Christopher J. Raymond**, Nanometrics Inc.

Program Committee: **Ofer Adan**, Applied Materials (Israel); **Michael J. Anderson**, Rohm and Haas Electronic Materials; **Charles N. Archie**, IBM Corp.; **Jason P. Cain**, Advanced Micro Devices, Inc.; **Alain G. Deleporte**, STMicroelectronics (France); **Daniel J. C. Herr**, Semiconductor Research Corp.; **David C. Joy**, The Univ. of Tennessee; **Chih-Ming Ke**, Taiwan Semiconductor Manufacturing Co., Ltd. (Taiwan); **Byoung-Ho Lee**, SAMSUNG Electronics Co., Ltd. (South Korea); **Martha I. Sanchez**, IBM Almaden Research Ctr.; **Richard M. Silver**, National Institute of Standards and Technology; **Bhanwar Singh**, Advanced Micro Devices, Inc.; **Alexander Starikov**, Intel Corp.; **Neal T. Sullivan**, Arrandance, Inc.; **Brian M. Trafas**, KLA-Tencor Corp.; **Vladimir A. Ukraintsev**, Veeco Instruments Inc.

Monday 25 February

Conv. Ctr. J2 Mon. 11:00 to 11:15 am

Opening Remarks
Metrology, Inspections, and Process Control
2007 Best Paper Award Announcement

SESSION 1

Conv. Ctr. J2 Mon. 11:15 am to 12:15 pm

Invited Session

Session Chairs: **John A. Allgair**, SEMATECH, Inc. and Advanced Micro Devices, Inc.; **Christopher J. Raymond**, Nanometrics Inc.

11:15 am: **Diffraction order control in overlay metrology: a review of the roadmap options** (*Invited Paper*), Mike E. Adel, Daniel Kandel, Vladimir Levinski, Joel L. Seligson, KLA-Tencor Corp. (Israel) [6922-01]

11:45 am: **Overlay metrology at the crossroads** (*Invited Paper*), Nigel P. Smith, Nanometrics Taiwan (Taiwan); Lewis A. Binns, Nanometrics Inc. (United Kingdom); Bert F. Plambeck, Kevin E. Heidrich, Nanometrics Inc. [6922-02]

Lunch Break 12:15 to 1:30 pm

SESSION 2

Conv. Ctr. J2 Mon. 1:30 to 3:30 pm

Solutions for Today

Session Chairs: **Brian M. Trafas**, KLA-Tencor Corp.; **Alexander Starikov**, Intel Corp.

1:30 pm: **Production aspects of 45-nm immersion lithography defect monitoring using laser DUV inspection methodology**, Eran Valfer, Applied Materials (Israel); Remo Kirsch, AMD Saxony LLC & Co. KG (Germany); Mirko Beyer, Applied Materials GmbH (Germany); Renana Perlovitch, Applied Materials (Israel); Erez Ravid, Applied Materials; Ofer Rotlevi, Applied Materials (Israel); Susan Weiher-Tellford, Applied Materials GmbH (Germany); Ute Vogler, AMD Saxony LLC & Co. KG (Germany); Uzodinma Okoroanyanwu, AMD Saxony LLC & Co. KG; Wolfram Grundke, AMD Saxony LLC & Co. KG (Germany); Peter Vanoppen, Richard Moerman, ASML Netherlands B.V. (Netherlands) . [6922-03]

1:50 pm: **Impact of track-path dedication on 32-nm double-patterning CD uniformity**, Len Tedeschi, SOKUDO USA, LLC; David Laidler, IMEC. . [6922-04]

2:10 pm: **Versatile DUV scatterometer of the PTB and FEM-based analysis for mask metrology**, Bernd Bodermann, Matthias Wurm, Alexander Diener, Hermann A. Gross, Regine Model, Physikalisch-Technische Bundesanstalt (Germany); Andreas Rathsfeld, Weierstrass-Institute für Angewandte Analysis und Stochastik (Germany) [6922-05]

2:30 pm: **Toward accurate feature shape metrology**, Ndubuisi G. Orji, National Institute of Standards and Technology [6922-06]

2:50 pm: **Extracting dose and focus from critical dimension data: optimizing the inverse solution**, Kevin R. Lensing, Broc Stirton, Siddharth Chauhan, Advanced Micro Devices, Inc. [6922-07]

3:10 pm: **Challenges of implementing contour modeling in 32-nm technology**, Daniel S. Fischer, Geng Han, James Oberschmidt, IBM Microelectronics Div.; Yong Wah Cheng, Chartered Semiconductor Manufacturing Ltd.; Jae-Yeol Maeng, SAMSUNG Electronics Co., Ltd.; Charles Archie, Wei Lu, IBM Microelectronics Div. [6922-08]

Coffee Break 3:30 to 4:00 pm

SESSION 3

Conv. Ctr. J2 Mon. 4:00 to 5:20 pm

Methods for Tomorrow

Session Chairs: **Christopher J. Raymond**, Nanometrics Inc.; **Daniel J. C. Herr**, Semiconductor Research Corp.

4:00 pm: **The potentials of helium ion microscopy for semiconductor process metrology**, Michael T. Postek, Andrés E. Vladár, National Institute of Standards and Technology [6922-09]

4:20 pm: **Evaluating diffraction-based overlay metrology for double-patterning technologies**, Chandra Saru Saravanan, Prasad Dasari, Nanometrics Inc.; Oleg Kritsun, Alden Acheta, Catherine Volkman, Bruno LaFontaine, Advanced Micro Devices, Inc.; Mircea Dusa, ASML [6922-10]

4:40 pm: **Plasma cleaning of nanoparticles from EUV mask materials by electrostatics**, Ramasamy Raju, Wayne M. Lytle, Hyung Joo Shin, Colin Das, Martin J. Neumann, David N. Ruzic, Univ. of Illinois at Urbana-Champaign [6922-12]

5:00 pm: **Optical through-focus technique that differentiates small changes in line width, line height, and sidewall angle for CD, overlay, and defect metrology applications**, Ravikiran Attota, Richard Silver, Bryan M. Barnes, Michael Stocker, National Institute of Standards and Technology [6922-13]

Conv. Ctr. Hall 3 Mon. 6:00 to 8:00 pm

Posters-Monday

The following posters will be displayed all day Monday. Authors will be present during the formal poster session Monday evening between 6:00 and 8:00 pm for discussion. Authors may set-up their posters after 10:30 am on Monday.

Exploring the limitations of x-ray reflectivity as a critical-dimension pattern-shape metrology, Hae-Jeong Lee, Sangcheol Kim, Christopher L. Soles, Eric K. Lin, Wen-Li Wu, National Institute of Standards and Technology [6922-11]

Printing assessment of parameter specific phase-shift-mask patterns for scatterometry monitoring, Jing Xue, Costas Spanos, Andrew Neureuther, Univ. of California/Berkeley [6922-63]

Objective image focus and stigmatism monitor for CD-SEM, Huichai Zhang, Matthew M. McQuillan, Christopher J. Gould, William R. Roberts, Qimonda Richmond LLC [6922-68]

Ellipsometric inspection of the inner surface of pellicle-covered masks, Chulgi Song, Hanyang Univ. (South Korea); Sangyouk Lee, Hanyang Univ.; Jusang Rhim, Hyoungjoo Lee, Jaisun Kyoung, Hanyang Univ. (South Korea); Soo-Bok Chin, Tae Hyuk Ahn, SAMSUNG Electronics Co., Ltd. (South Korea); Hyekeun Oh, Ilsin An, Hanyang Univ. (South Korea) [6922-78]

Conference 6922 • Convention Center J2

- Optics characterization with compact EUV spectrophotometer**, Holger Blaschke, Istvan Balasa, Lothar Koch, Kai Starke, Detlev Ristau, Laser Zentrum Hannover e.V. (Germany); Christian Wies, Rainer Lebert, AIXUV GmbH (Germany); Armin Bayer, Frank Barkusky, Klaus Mann, Laser-Lab. Göttingen e.V. (Germany) [6922-79]
- Verification of optics for the die-to-wafer-like-image mask inspection**, Akira Takada, Topcon Corp. (Japan); Masato Shibuya, Tokyo Polytechnic Univ. (Japan) [6922-80]
- Phase metrology on 45-nm node phase-shift mask structures**, Kyung M. Lee, Malahat A. Tavassoli, Intel Corp.; Sascha Perlit, Ute Buttgeriet, Carl Zeiss SMS GmbH (Germany) [6922-81]
- A new high-resolution photomask inspection system for contamination detection**, Bo Mu, KLA-Tencor Corp. [6922-82]
- Verification for distributions of critical dimension in OPC models utilizing design-based metrology tool**, Jeong-Geun Park, SAMSUNG Electronics Co., Ltd. (South Korea) [6922-83]
- Advanced method to monitor design-process marginality for 65-nm node and beyond**, Chris C. Young, KLA-Tencor Corp. [6922-84]
- CD-SAXS measurements using lab-based and synchrotron-based instruments**, Cheng-Qing Wang, Wen-Li Wu, National Institute of Standards and Technology [6922-85]
- A novel methodology for model-based OPC verification**, Tengyen Huang, Nanya Technology Corp. (Taiwan) [6922-86]
- Pattern deform due to the narrow CD caused by BARC thinning**, Ilho Song, Jeahee Kim, Keeho Kim, Juhyun Kim, Dongbu Electronics Co., Ltd. (South Korea) [6922-87]
- Effect of set point on CD measurement in CD-AFM: plausibility study**, Byong-Chon Park, Jinho Choi, Sang Jung Ahn, Korea Research Institute of Standards and Science (South Korea); Min-Jung Shin, Dongchul Ihm, Byoung-Ho Lee, SAMSUNG Electronics Co., Ltd. (South Korea) [6922-88]
- Design, manufacturing, and optimization of customized high-quality high-NA DUV lenses**, Oliver R. Falkenstörfer, Helmut Bernitzki, Ullrich Krüger, Hans Lauth, Stefan Müller-Pfeiffer, Lutz Reichmann, JENOPTIK Laser, Optik, Systeme GmbH (Germany) [6922-90]
- Recent developments of advanced CD AFM probes for sub-45-nm technology nodes**, Hao-Chih Liu, Jason R. Osborne, Gregory A. Dahlen, Veeco Metrology Inc.; Johann Greschner, Thomas Bayer, Samuel Kalt, Georg Fritz, Team Nanotec GmbH (Germany) [6922-91]
- Electron-beam-patterning simulation and metrology of complex layouts on Si/Mo multilayer substrates**, George P. Patsis, Dimitrios Drygiannakis, Nikolaos Tsirikas, Ioannis Raptis, Institute of Microelectronics (Greece) [6922-92]
- Improvement in model-based metrology algorithm for practical use in the CD-SEM**, Maki Tanaka, Chie Shishido, Wataru Nagatomo, Hitachi, Ltd. (Japan); Kenji Watanabe, Hitachi High-Technologies Corp. (Japan) [6922-93]
- Calibration of CD-SEM: moving from relative to absolute measurements**, Sergey Babin, Sergey Borisov, Andrey Ivanchikov, Igor Ruzavin, Abeam Technologies [6922-94]
- Automated metrology for SEM calibration and CD-line measurements using image analysis and SEM modeling methods**, Vitali Khvatkov, Smart Imaging Technologies; Sergey Babin, Abeam Technologies. [6922-96]
- Further study on the verification of CD-SEM based monitoring for hyper-NA lithography**, Toru Ishimoto, Hitachi High-Technologies Corp. (Belgium) and IMEC (Belgium) and Hitachi Ltd. (Japan) [6922-97]
- MuGFET observation and CD measurement by using CD SEM**, Tatsuya Maeda, Hitachi High-Technologies Corp. (Japan); Maki Tanaka, Hitachi, Ltd. (Japan) [6922-98]
- High-order correction and sampling strategy for 45-nm immersion lithography overlay control**, Chin-Chou K. Huang, KLA-Tencor Corp.; Bo-Yun Hsueh, George K.Huang, Chun-Chi Yu, Jerry K.Hsu, United Microelectronics Corp. (Taiwan); Chien-Jen Huang, David C. Tien, KLA-Tencor Corp. [6922-99]
- Improve overlay control and scanner utilization through high-order corrections**, Hung-Ming Lin, Benjamin Lin, Chan-Tsun J. Wu, William Liu, Powerchip Semiconductor Corp. (Taiwan); Chin-Chou K. Huang, James R. Manka, Desmond Goh, Healthy C. T.Huang, David C. Tien, KLA-Tencor Corp. [6922-100]
- Overlay control using scatterometry based metrology (SCOL™) in production environment**, Berta A. Dinu, KLA-Tencor Corp. (Israel); Stefan Fuchs, Uwe Kramer, Michael Kubis, Qimonda Dresden GmbH & Co. OHG (Germany); Anat Marchelli, KLA-Tencor Corp. (Israel); Christian Sparka, KLA-Tencor Corp. (Germany); Amir Widmann, KLA-Tencor Corp. [6922-101]
- Alignment system and process optimization for improvement of double-patterning overlay**, Won-Kwang Ma, Jung-Hyun Kang, Chang-Moon Lim, Hyeong-Soo Kim, Seung-Chan Moon, Hynix Semiconductor Inc. (South Korea); Seung-Chul Oh, ASML Korea Co., Ltd (South Korea) [6922-103]
- Sampling for advanced overlay process control**, Hyun Tae Kang, HongSeok Kim, MoonSang Lee, Jangho Shin, SAMSUNG Electronics Co., Ltd. (South Korea); John C. Robinson, KLA-Tencor Corp.; DongSub Choi, KLA-Tencor Corp. (South Korea); Pavel Izikson, KLA-Tencor Corp. (Israel) [6922-105]
- A system to optimize mix-and-match overlay in lithography**, Shinji Wakamoto, Yuuki Ishii, Nikon Corp. (Japan); Shinroku Maejima, Renesas Technology Corp. (Japan); Atsuhiko Kato, KLA-Tencor Japan Ltd. (Japan); John C. Robinson, Dong-Sub Choi, KLA-Tencor Corp. [6922-107]
- Diffraction-based overlay metrology for α -carbon applications**, Chandra S. Saravanan, Asher Tan, Prasad Dasari, Gary Goelzer, Nigel Smith, Nanometrics Inc.; Seouk-Hoon Woo, Jang Ho Shin, Hyun-Jae Kang, Ho-Chul Kim, SAMSUNG Electronics Co., Ltd. [6922-108]
- Film stacking architecture for immersion lithography process**, Tomohiro Goto, Masakazu Sanada, Tadashi Miyagi, Kazuhito Shigemori, Masashi Kanaoka, Shuichi Yasuda, Osamu Tamada, Masaya Asai, SOKUDO Co., Ltd. (Japan) [6922-109]
- Controlling 45-nm Cu CMP processes using a high-resolution profiler**, Jeff Reichert, KLA-Tencor Corp. [6922-111]
- Effects produced by CDU improvement of resist pattern with PEB temperature control for wiring resistance variation reduction**, Masahide Tadokoro, Shinichi Shinozuka, Kunie Ogata, Tokyo Electron Kyushu Ltd. (Japan); Tamotsu Morimoto, Tokyo Electron Ltd. (Japan) [6922-112]
- Rationalizing the mechanism of HMDS degradation in air and effective control of the reaction by-products**, Gerald Weineck, Kevin Seguin, Andrew J. Dallas, Donaldson Co., Inc. [6922-113]
- Stress measurement system for process control**, Kumiko Akashika, Masahiro Horie, Dainippon Screen Manufacturing Co., Ltd. (Japan) [6922-114]
- MEEF-driven defect disposition for contamination inspection: optimization of the inspection algorithm**, Tracy Huang, Aditya Dayal, KLA-Tencor Corp. [6922-115]
- 2-nm re-orientation accuracy parallel electronic datum system**, Xiang-Wen Xiong, Zhongheng High-Tech Inc. (China) [6922-116]
- CDU improvement technology of etching pattern with photolithography**, Masahide Tadokoro, Shinichi Shinozuka, Megumi Jyousaka, Kunie Ogata, Tokyo Electron Kyushu Ltd. (Japan); Tamotsu Morimoto, Tokyo Electron Ltd. (Japan); Yoshitaka Konishi, Tokyo Electron Software Technologies Ltd. (Japan) [6922-117]
- Film thickness measurement tool with the stress measurement function**, Masahiro Horie, Kumiko Akashika, Shuji Shiota, Shinji Yamaguchi, Kakumichi Yamano, Dainippon Screen Manufacturing Co., Ltd. (Japan) [6922-118]
- A study for hard-polymer removal in ultra-thick dielectric patterning process**, Yun Kijun, Dongbu HiTek (South Korea) [6922-119]
- In-situ real-time temperature control of baking systems in lithography**, Yuheng Wang, National Univ. of Singapore (Singapore); Hui Tong Chua, The Univ. of Western Australia (Australia); Arthur E. B.Tay, National Univ. of Singapore (Singapore) [6922-120]
- Virtual metrology with multivariate statistical process monitoring**, Dekong Zeng, Univ. of California/Berkeley [6922-121]
- Wide-applications of design-based metrology with tool integration**, Hyun-Jo Yang, Jung-Chan Kim, Taehyeong Lee, Areum Jung, Dong-Gyu Yim, Jin-Woong Kim, Hynix Semiconductor Inc. (South Korea) [6922-123]
- Detecting wafer-edge defects in production process flow prevents yield loss**, Lynn Endsley, Rudolph Technologies, Inc.; Jeffrey W. Ritchison, Texas Instruments Inc.; Alan P. Carlson, Rudolph Technologies, Inc. [6922-124]
- Wafer-edge polishing process for defect reduction during immersion lithography**, Motoya Okazaki, Applied Materials, Inc.; Raymond Maas, ASML Netherlands B.V. (Netherlands); Sen-Hou Ko, Yufei Chen, Paul Miller, Mani Thothadri, Manjari Dutta, Chong-Ping Chang, Abraham Anapolsky, Chris Lazik, Yuri Uritsky, Martin Seamons, Deenesh Padhi, Wendy Yeh, Applied Materials, Inc.; Stephan Sinkwitz, ASML Netherlands B.V. (Netherlands); Chris Ngai, Applied Materials, Inc. [6922-125]

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High-throughput wafer defect monitor for integrated metrology applications in photolithography, Nagaraja Rao, Patrick D. Kinney, Anand Gupta, Real Time Metrology, Inc. [6922-126]

Part-per-trillion AMC detection, Steven Rowley, Particle Measuring Systems, Inc. [6922-127]

Using UV-reflectometry for fast trench-depth measurement, Masahiro Horie, Shuji Shiota, Shinji Yamaguchi, Kakumichi Yamano, Masayoshi Kobayashi, Dainippon Screen Manufacturing Co., Ltd. (Japan) [6922-128]

Study of after develop inspection of photoresist wafers using electron beam III, Teruyuki Hayashi, Misako Saito, Kaoru Fujihara, Masahiro Shiga, Tokyo Electron Ltd. (Japan); Jack Y. Jau, Hermes Microvision, Inc. [6922-129]

Nanoscale structure qualification of patterned media in hard-disk drive manufacturing, Yoshiteru Katsumura, Takenori Hirose, Yasuhiro Yoshitake, Hitachi, Ltd. (Japan); Zvonimir Bandic, Thomas R. Albrecht, Hitachi Global Storage Technologies [6922-130]

Improving dry-etch control for contact plugs in advanced DRAM manufacturing, Tianming Bao, Veeco Instruments Inc.; Yuval Bar, Micron Technology, Inc.; David H. Fong, Veeco Instruments Inc.; Mukund Godbole, Micron Technology, Inc. [6922-131]

In-line focus-dose monitoring for hyper-NA imaging, Marco Polli, KLA-Tencor Corp. (Italy); Sara Loi, Alejandro Fasciszewski Zeballos, Umberto Iessi, STMicroelectronics (Italy); John C. Robinson, KLA-Tencor Corp.; Antonio Mani, KLA-Tencor Italy SRL (Italy) [6922-132]

Gas phase study of the reactivity of optical coating materials with hydrocarbons using a desk-top size EUV laser (Presentation Only), Feng Dong, Scott C. Heinbuch, Elliot R. Bernstein, Jorge J. Rocca, Colorado State Univ. [6922-133]

Pitch metrology by optical diffraction and atomic force microscopy, Donald A. Chernoff, Advanced Surface Microscopy, Inc.; Egbert Buhr, Physikalisch-Technische Bundesanstalt (Germany); David L. Burkhead, Advanced Surface Microscopy, Inc.; Alexander Diener, Physikalisch-Technische Bundesanstalt (Germany) [6922-134]

Development of back-end-of-the-line applications using optical digital profilometry, Ying Luo, Timbre Technologies, Inc.; Jun-Ji Huang, United Microelectronics Corp. (Taiwan) [6922-135]

Scatterometry based overlay metrology, Takahiro Matsumoto, Hideki Ina, Koichi Sentoku, Satoru Oishi, Canon Inc. (Japan) [6922-136]

Spectroscopic ellipsometer for ultra-thin film, Kumiko Akashika, Masahiro Horie, Dainippon Screen Manufacturing Co., Ltd. (Japan) [6922-137]

Characterization of sub-50-nm line array structures with angle-resolved multiple wavelength scatterometry, Michael J. Kotlyanskii, Fei Shen, Gary Jiang, Rudolph Technologies, Inc.; Benjamin D. Bunday, International SEMATECH Manufacturing Initiative [6922-139]

Sensitivity and performance estimates for the multiple-wavelength, multiple-incidence angle ellipsometry for OCD applications, Michael J. Kotlyanskii, Gary Jiang, Rudolph Technologies, Inc. [6922-140]

Modeling the effect of finite size gratings on scatterometry measurements, Elizabeth Kenyon, Michael W. Cresswell, Thomas A. Germer, National Institute of Standards and Technology [6922-142]

Characterization of the poly gate ACI structure with laser-based angle resolved multiple-wavelength scatterometry, Gary Jiang, Michael J. Kotlyanskii, Fei Shen, Rudolph Technologies, Inc. [6922-143]

Low-k n&k variation impact on CD accuracy of scatterometry, Masahiro Yamamoto, Akihiro Sonoda, Tokyo Electron Ltd. (Japan); Vi Vuong, Dmitry Likhachev, Yan Chen, Gang He, Timbre Technologies, Inc. [6922-145]

Implementation of spectroscopic critical dimension (SCD) for leveling inline monitor of ASML 193-nm scanner, Wen-Kuang Lin, Mike Yeh, United Microelectronics Corp. (Taiwan) [6922-146]

Three-dimensional semiconductor-grooves measurement simulations (scatterometry) using nonstandard and ADI FDTD for calculation time shortening, Hirokimi Shirasaki, Tamagawa Univ. (Japan) [6922-147]

Novel approach for immersion lithography defectivity control to increase productivity, Ilan Englard, Applied Materials BV (Netherlands); Peter Vanoppen, Ingrid Minnaert-Janssen, Raf Stegen, Ted der Kinderen, Erik van Berederode, Frank Duray, ASML Netherlands B.V. (Netherlands); Jeroen Linders, Philips Research Labs. (Netherlands); Denis V. Ovchinnikov, ASML Netherlands B.V. (Netherlands); Richard Piech, Applied Materials France SARL (France); Claudio Masia, Applied Materials BV (Netherlands); Noam Hillel, Applied Materials (Israel); Erez Ravid, Applied Materials, Inc.; Ofer Rotlevi, Amir Wilde, Applied Materials (Israel); Robert Schreutelkamp, Applied Materials BV (Netherlands) [6922-148]

Traceable calibration of AFM step height, James Robert, Bill Banke, Jr., Carlos Strocchia-Rivera, IBM Corp.; Ronald Dixson, National Institute of Standards and Technology [6922-149]

CD-evaluation methods in photomask defect dispositioning using AIMS tools, Arndt C. Dürr, Advanced Mask Technology Ctr. (Germany) . . . [6922-150]

22-nm node contact hole formation in extreme ultra-violet lithography, Eun-Jin Kim, Hanyang Univ. (South Korea); Kwan-Hyung Kim, Hyeong-Ryeol Park, Jun-Yeob Yeo, Jai-Soon Kim, Seoul National Univ. (South Korea); Hye-Keun Oh, Hanyang Univ. (South Korea) [6922-151]

Advanced lithography parameters extraction by using scatterometry system (Part II), Stephen Zhou, Chartered Semiconductor Manufacturing Ltd. (Singapore) [6922-152]

Fabricating nanoscale reference material for precise morphology measurement, Hiroshi Itoh, National Institute of Advanced Industrial Science and Technology (Japan) [6922-153]

The importance of accuracy in SEM metrology, Arkady V. Nikitin, Dmitry Y. Yeremin, Matthew Sandy, E. Timothy Goldburtt, Nanometrology LLC [6922-154]

TeraFab solutions enable flexibility in optimizing photomask quality control process in wafer fab, Jeff C. Lin, Raj Badoni, Mu Bo, Tracy Huang, KLA-Tencor Corp. [6922-155]

Tuesday 26 February

SESSION 4

Conv. Ctr. J2 Tues. 8:00 to 10:20 am

Standards and Reference Metrology

Session Chairs: **Vladimir A. Ukraintsev**, Veeco Instruments Inc.;
David C. Joy, The Univ. of Tennessee

8:00 am: **Paving the way for multiple applications for the CD-AFM technique in the semiconductor industry**, Johann Foucher, Mickael Martin, Erwine Pargon, Lab. d'Electronique de Technologie de l'Information (France) . [6922-14]

8:20 am: **Controlled deposition of NIST-traceable nanoparticles as additional size standards for photomask applications**, Jing Wang, David Y.Pui, Chaolong Qi, Sejin Yook, Univ. of Minnesota; Heinz Fissan, Univ. Duisburg-Essen (Germany); Erdem A. Ultanir, Ted Liang, Intel Corp. [6922-15]

8:40 am: **Accurate and traceable dimensional metrology with a reference CD-SEM**, András E. Vladár, Michael T. Postek, Petr Cizmar, John S. Villarrubia, National Institute of Standards and Technology [6922-16]

9:00 am: **Subnanometer pitch calibration and data quality evaluation methodology**, Chih-Ming Ke, Willie Wang, Jacky Huang, Tsai-Sheng Gau, Burn Lin, Taiwan Semiconductor Manufacturing Co. Ltd. (Taiwan) [6922-17]

9:20 am: **A novel AFM method for sidewall measurement of high-aspect ratio patterns**, Masahiro Watanabe, Shuichi Baba, Hitachi, Ltd. (Japan); Takafumi Morimoto, Satoshi Sekino, Hitachi Kenki FineTech Co., Ltd. (Japan) [6922-18]

9:40 am: **TEM validation of CD-AFM image reconstruction: part II**, Gregory A. Dahlen, Thorleaf Research, Inc.; Hao-Chih Liu, Marc Osborn, Jason R. Osborne, Veeco Metrology Inc.; Bryan Tracy, Amalia del Rosario, Spansion Inc. [6922-19]

10:00 am: **Dimension controlled CNT probe of AFM metrology system for 45-nm node and beyond**, Satoshi Sekino, Takafumi Morimoto, Toru Kurenuma, Hitachi Kenki FineTech Co., Ltd. (Japan); Motoyuki Hirooka, Hitachi, Ltd. (Japan); Hiroki Tanaka, Hitachi Kyowa Engineering Co., Ltd. (Japan) . . [6922-20]

Coffee Break 10:20 to 10:50 am

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SESSION 5

Conv. Ctr. J2 **Tues. 10:50 am to 12:30 pm**

Overlay I

Session Chairs: **Brian M. Trafas**, KLA-Tencor Corp.; **Daniel J.C. Herr**, Semiconductor Research Corp.

10:50 am: **Overlay metrology tool calibration using blossom**, Lewis A. Binns, Nigel P. Smith, Nanometrics Inc. (United Kingdom); Prasad Dasari, Nanometrics Inc. [6922-21]

11:10 am: **Using in-chip overlay metrology**, Stefanie Gil Girol, Bernd Schulz, AMD Saxony LLC & Co. KG (Germany); Nigel Smith, Lewis Binns, Nanometrics Inc. (United Kingdom) [6922-22]

11:30 am: **Diffraction-based overlay metrology: accuracy and performance on front-end stack**, Philippe J. Leray, Shaunee Y. Cheng, IMEC (Belgium); Daniel Kandel, Michael E. Adel, Berta A. Dinu, Boris Golovanevsky, Pavel Izikson, KLA-Tencor Corp. (Israel); SeungHoon Yoon, Dohwa Lee, KLA-Tencor Corp. (South Korea); Vladimir B. Levinski, Irina Vakshstein, KLA-Tencor Corp. (Israel); Mauro Vasconi, STMicroelectronics (Italy); Bartlomiej W. Salski, QWED (Poland) [6922-23]

11:50 am: **Optimization of high-order control including overlay, alignment, and sampling**, Dongsu Choi, KLA-Tencor Corp. (South Korea); Chulseung Lee, Changjin Bang, Daehee Cho, Hynix Semiconductor Inc. (South Korea); Pavel Izikson, KLA-Tencor Corp. (Israel); SeungHoon Yoon, Dohwa Lee, KLA-Tencor Corp. (South Korea) [6922-106]

12:10 pm: **Overlay measurement based on dual-overlaid grating image**, Deh-Ming Shyu, Yi-Sha Ku, Industrial Technology Research Institute (Taiwan) [6922-24]

Lunch/Exhibition Break 12:30 to 1:30 pm

SESSION 6

Conv. Ctr. J2 **Tues. 1:30 to 3:30 pm**

Scatterometry I

Session Chairs: **Christopher J. Raymond**, Nanometrics Inc.; **Richard M. Silver**, National Institute of Standards and Technology

1:30 pm: **Assessing scatterometry for measuring advanced spacer structures with embedded SiGe**, Matthew Sendelbach, Shahin Zangoie, IBM Microelectronics Div.; Alok Vaid, Advanced Micro Devices, Inc.; Pedro Herrera, Walter Mieher, KLA-Tencor Corp. [6922-25]

1:50 pm: **Characterization of 32-nm node BEOL grating structures using scatterometry**, Shahin Zangoie, Matthew Sendelbach, Charles N. Archie, Matthew Angyal, Alok Vaid, IBM Microelectronics Div.; Pedro P. Herrera, KLA-Tencor Corp. [6922-26]

2:10 pm: **Advanced profile control and the impact of sidewall angle at gate etch for critical nodes**, HyungJoo Lee, Alok Ranjan, Merritt L. Funk, Radha Sundararajan, Dan Prager, Asao Yamashita, Tokyo Electron America, Inc. [6922-27]

2:30 pm: **Scatterometry as technology enabler for embedded SiGe process**, Alok Vaid, Advanced Micro Devices, Inc.; Shahin Zangoie, Matthew Sendelbach, IBM Microelectronics Div.; Rohit Pal, Kevin Lensing, Advanced Micro Devices, Inc.; Carsten Hartig, AMD Saxony Manufacturing GmbH (Germany) [6922-28]

2:50 pm: **Measurement of high-k and metal film thickness on FinFET sidewalls using scatterometry**, Jimmy M. Price, SEMATECH, Inc.; Benjamin Bunday, International SEMATECH Manufacturing Initiative; Casey Smith, Muhammad M. Hussain, Rusty Harris, SEMATECH, Inc.; Michelle Zhang, Thaddeus G. Dziura, KLA-Tencor Corp. [6922-29]

3:10 pm: **Industrial characterization of scatterometry for advanced APC of 65-nm CMOS logic gate patterning**, Karen Dabertrand, Mathieu Touchet, STMicroelectronics (France); Stephanie Kremer, KLA-Tencor Corp. (France); Catherine Chaton, CEA-LETI (France); Maxime Gatefait, Enrique Aparicio, STMicroelectronics (France); Marco Polli, KLA-Tencor Corp. (France); Jean-Claude Royer, Lab. d'Electronique de Technologie de l'Information (France) [6922-30]

Coffee Break 3:30 to 4:00 pm

SESSION 7

Conv. Ctr. J2 **Tues. 4:00 to 6:00 pm**

Process Control

Session Chairs: **Jason P. Cain**, Advanced Micro Devices, Inc.; **Alexander Starikov**, Intel Corp.

4:00 pm: **Impact of sampling on uncertainty: semiconductor dimensional metrology applications**, Benjamin D. Bunday, International SEMATECH Manufacturing Initiative; Charles N. Archie, IBM Microelectronics Div.; G. William Banke, Jr., IBM Corp.; Ingrid B. Peterson, Applied Materials, Inc.; Bart Rijpers, ASML Netherlands B.V. (Netherlands); Andr as E. Vlad ar, National Institute of Standards and Technology; Vladimir A. Ukraintsev, Texas Instruments Inc.; Thomas Hingst, Qimonda Dresden GmbH & Co. OHG; Masafumi Asano, Toshiba Corp. [6922-31]

4:20 pm: **CD uniformity control via real-time control of photoresist properties**, Weng-Khuen Ho, Ming Chen, Jun Fu, Arthur E. B. Tay, National Univ. of Singapore (Singapore) [6922-32]

4:40 pm: **Process control for 45-nm CMOS logic gate patterning**, Bertrand Le-Gratiet, Enrique Aparicio, STMicroelectronics (France); Laurene Babaud, Freescale Semiconductor, Inc. (France); Karen Dabertrand, Mathieu Touchet, STMicroelectronics (France); Stephanie Kremer, KLA-Tencor Corp. (France); Catherine Chaton, Franck Foussadier, Frank Sundermann, Jean-Damien Chapon, Maxime Gatefait, Blandine Minghetti, Pascal Gouraud, Jean Massin, STMicroelectronics (France) [6922-33]

5:00 pm: **Improvement of gate CD uniformity for 55-nm node logic devices**, Takashi Murakami, Taisaku Nakata, Kensuke Taniguchi, Takayuki Uchiyama, NEC Electronics Corp. (Japan); Megumi Jyousaka, Masahide Tadokoro, Tokyo Electron Kyushu Ltd. (Japan); Yoshitaka Konishi, Tokyo Electron Software Technologies Ltd. (Japan) [6922-34]

5:20 pm: **Metrology characterization for self-aligned double patterning**, Ami Berger, Sergey Latinsky, Applied Materials (Israel) [6922-35]

5:40 pm: **Focus and dose control to actual process wafer**, Hideki Ina, Koichi Sentoku, Canon Inc. (Japan) [6922-36]

Wednesday 27 February

SESSION 8

Conv. Ctr. J2 Wed. 8:00 to 10:00 am

Inspection and Defect

Session Chairs: **Byoung-Ho Lee**, SAMSUNG Electronics Co., Ltd. (South Korea); **Martha I. Sanchez**, IBM Almaden Research Ctr.

8:00 am: **Defect criticality index (DCI): a new methodology to significantly improve DOI sampling rate in 45-nm production environment**, Yoshiyuki Sato, Toshiba Semiconductor Co. (Japan); Masami Aoki, KLA-Tencor Japan Ltd. (Japan) [6922-37]

8:20 am: **Lot acceptance sampling inspection plan for non-normal CD distribution**, Takahiro Ikeda, Masafumi Asano, Toshiba Corp. (Japan) [6922-38]

8:40 am: **Improvements on the simulation of microscopic images for the defect detection of nanostructures**, Stephan Rafler, Karsten Frenner, Univ. Stuttgart (Germany) [6922-39]

9:00 am: **Defect inspection using a high-resolution pattern image obtained from multiple low-resolution images of the same pattern on an observed noisy SEM image**, Masahiko Takashima, Yoshihiro Midoh, Koji Nakamae, Osaka Univ. (Japan) [6922-40]

9:20 am: **Contamination specification for dimensional metrology SEMs**, András E. Vladár, K. P. Purushotham, Michael Postek, National Institute of Standards and Technology [6922-41]

9:40 am: **In-line inspection resistance mapping using quantitative measurement of voltage contrast in SEM images**, Miyako Matsui, Yoshihiro Anan, Takahiro Odaka, Hitachi, Ltd. (Japan); Hiroshi Nagaishi, Koichi Sakurai, Renesas Technology Corp. (Japan) [6922-42]

Coffee Break 10:00 to 10:30 am

SESSION 9

Conv. Ctr. J2 Wed. 10:30 to 11:50 am

CDSEM I

Session Chairs: **David C. Joy**, The Univ. of Tennessee; **Ofer Adan**, Applied Materials (Israel)

10:30 am: **Optimization of SEM condition with Monte Carlo SEM simulation**, Yumiko Miyano, Akira Hamaguchi, Hideaki Abe, Yuuichiro Yamazaki, Toshiba Corp. (Japan) [6922-43]

10:50 am: **Characterization of CD-SEM metrology for iArF photoresist materials**, Benjamin D. Bunday, John Allgair, International SEMATECH Manufacturing Initiative; Bryan J. Rice, Jeff Byers, SEMATECH, Inc.; Ram Peltinov, Ofer Adan, Yohanan Avitan, Maayan Bar-Zvi, Applied Materials (Israel); John Swyers, Applied Materials, Inc. [6922-44]

11:10 am: **Advanced CD-SEM metrology to improve total process control performance for hyper-NA lithography**, Mayuka Osaki, Hitachi, Ltd. (Japan) and Hitachi High-Technologies Corp. (Japan) and IMEC (Belgium); Maki Tanaka, Chie Shishido, Hitachi, Ltd. (Japan); Toru Ishimoto, Hitachi High-Technologies Corp. (Belgium) and IMEC (Belgium); Kohei Sekiguchi, Hitachi High-Technologies Europe GmbH (Germany) and IMEC (Belgium); Norio Hasegawa, Kenji Watanabe, Hitachi High-Technologies Corp. (Japan); Shaunee Y. Cheng, David Laidler, Monique Ercken, IMEC (Belgium) [6922-45]

11:30 am: **CD-SEM contour-based process monitoring in DRAM production environment**, Uwe Kramer, Stefan Fuchs, Franck Jauzion-Graverolle, Robert Wildfeuer, Qimonda Dresden GmbH & Co. OHG (Germany); Gilad Ben-Nahumb, Ovadya Menadeva, Applied Materials (Israel); Stefano Ventola, Applied Materials GmbH (Germany) [6922-47]

Lunch/Exhibition Break 11:50 to 1:30 pm

SESSION 10

Conv. Ctr. J2 Wed. 1:30 to 2:50 pm

Overlay II

Session Chairs: **John A. Allgair**, International SEMATECH Manufacturing Initiative; **Chih-Ming Ke**, Taiwan Semiconductor Manufacturing Co. Ltd. (Taiwan)

1:30 pm: **Accurate in-resolution level overlay metrology for multipatterning lithography techniques**, Ilan England, Applied Materials BV (Netherlands); Richard Piech, Applied Materials France SARL (France); Claudio Masia, Applied Materials BV (Netherlands); Noam Hillel, Liraz Gershtein, Ram Peltinov, Ofer Adan, Applied Materials (Israel) [6922-48]

1:50 pm: **Sources of overlay error in double-patterning integration schemes**, David Laidler, Philippe Leray, Shaunee Cheng, IMEC (Belgium) [6922-49]

2:10 pm: **Correlating overlay metrology precision to interlayer dielectric film properties**, Kris R. Paserba, Seagate Technology LLC [6922-52]

2:30 pm: **Overlay improvement by zone alignment strategy**, Chun-Yen Huang, Ai-Yi Lee, Chiang-Lin Shih, Nanya Technology Corp. (Taiwan); Richer Yang, Inotera Memories Inc. (Taiwan) [6922-53]

Coffee Break 2:50 to 3:30 pm

SESSION 11

Conv. Ctr. J2 Wed. 3:30 to 5:10 pm

CD for Development and OPC

Session Chairs: **Ofer Adan**, Applied Materials (Israel); **Christopher J. Raymond**, Nanometrics Inc.

3:30 pm: **Challenges of OPC model calibration from SEM contours**, Yuri Granik, Ir Kusnadi, Mentor Graphics Corp. [6922-54]

3:50 pm: **Empirical data validation for model building**, Aram Kazarian, Synopsys, Inc. [6922-55]

4:10 pm: **Automated creation of production metrology recipes based on design information**, Jason P. Cain, Mark Threefoot, Kishan Shah, Advanced Micro Devices, Inc.; Bernd Schulz, Stefanie Gil Girol, Jon-Tobias Hoeft, AMD Saxony LLC & Co. KG (Germany) [6922-56]

4:30 pm: **Impact of assistance feature to pattern profile for isolated feature in sub-65-nm node**, Myungsoo Kim, Jeahhee Kim, Keeho Kim, Eunsoo Jeong, Dongchan Lee, Dongbu Electronics Co., Ltd. (South Korea) [6922-57]

4:50 pm: **Accurate device simulations through CD-SEM-based edge-contour extraction**, Ovadya Menadeva, Applied Materials (Israel); Eitan N. Shauly, Rami Drori, Tower Semiconductor Ltd. (Israel); Ram Peltinov, Avishai Bartov, Sergey Latinski, Applied Materials (Israel) [6922-95]

Conv. Ctr. C1 Wed. 8:00 to 9:30 pm

Enabling Accurate Optical Proximity Correction Panel Discussion

Panel Moderators: **Christopher J. Raymond**, Nanometrics Inc.; **Vladimir A. Ukraintsev**, Veeco Instruments Inc.

With lithographically printed features now pushed well into the sub-wavelength regime, the role of complex simulations for optical proximity correction (OPC) has never been more important. Yet validation of OPC models relies on accurate and precise metrology of the structures in question. Furthermore, as design rules shrink and devices become more complex, more metrology will be needed. CDSEM is the predominant metrology for the measurement of OPC structures, but with concerns over accuracy and precision, will it be suitable for OPC applications in the future? Measurement contouring is already proving useful, but what additional CDSEM applications are needed? Are distortions in a CDSEMs field of view invariant to layout orientation? Are there ways to improve its accuracy? As more measurements are needed, is throughput a concern? What is the optimal area coverage of sampling for model calibrations? What are the implications of contouring on regular process monitoring metrology? How can contour measurement quality be assessed?

The panel will be comprised of representatives from manufacturers, metrology and software vendors, and government laboratories.

Thursday 28 February

SESSION 12

Conv. Ctr. J2 Thurs. 8:20 to 10:00 am

Scatterometry II

Session Chairs: **Christopher J. Raymond**, Nanometrics Inc.;
Alexander Starikov, Intel Corp.

8:20 am: **Angle-resolved optical metrology**, Richard M. Silver, National Institute of Standards and Technology; Bryan M. Barnes, KT Consulting, Inc.; Ravikiran Attota, Michael Stocker, Egon Marx, National Institute of Standards and Technology [6922-59]

8:40 am: **Opportunities and challenges for optical CD metrology in double-patterning process control**, Daniel C. Wack, John Hench, Leonid Poslavsky, John Fielden, Heath Pois, KLA-Tencor Corp. [6922-60]

9:00 am: **A review of forward solve algorithms for optical critical dimension metrology**, Hanyou Chu, Peilin Jiang, Timbre Technologies, Inc.; John Hench, Andrei B. Veldman, KLA-Tencor Corp. [6922-61]

9:20 am: **Comparison of spectroscopic Mueller polarimetry, standard scatterometry, and real space-imaging techniques (SEM and 3D-AFM) for dimensional characterization of periodic structures**, Antonello De Martino, Martin Foldyna, Tatiana A. Novikova, Ecole Polytechnique (France); Denis Cattelan, HORIBA Jobin Yvon Ltd. (France); Pierre Barritault, Jérôme Hazart, Christophe Licitra, Johan Foucher, Francis Bogeat, Lab. d'Electronique de Technologie de l'Information (France) [6922-62]

9:40 am: **Complex etched 3D pattern over 2D pattern metrology using new scatterometry techniques**, Young S. Lee, KLA-Tencor Corp.; Manfred Moert, Peter Reinig, Thomas Hingst, Qimonda Dresden GmbH & Co. OHG (Germany) [6922-64]

Coffee Break 10:00 to 10:30 am

SESSION 13

Conv. Ctr. J2 Thurs. 10:30 am to 12:10 pm

CDSEM II

Session Chairs: **Martha I. Sanchez**, IBM Almaden Research Ctr.;
John A. Allgair, SEMATECH, Inc. and Advanced Micro Devices, Inc.

10:30 am: **Physical matching of CD-SEM: noise analysis and verification in FAB environment**, Uwe Kramer, Alessandra Navarra, Goeran Fleischer, Jan Kaiser, Frank Voss, Qimonda Dresden GmbH & Co. OHG (Germany); G. Zuckerman, R. Kris, Igal Ben-Dayana, Elad Sommer, Applied Materials (Israel); Dirk Schoene, Stefano Ventola, Applied Materials GmbH (Germany) . . [6922-65]

10:50 am: **AWV: high-throughput cross-array cross-wafer variation mapping**, Byoung-Ho Lee, Dongchul Ihm, Tae-Yong Lee, SAMSUNG Electronics Co., Ltd. (South Korea); Jeong-Ho Yeo, Gadi Greenberg, Doron Meshulach, Erez Ravid, Shimon Levi, Kobi Kan, Applied Materials (Israel) [6922-66]

11:10 am: **CD-bias reduction in CD-SEM linewidth measurements for advanced lithography process**, Maki Tanaka, Chie Shishido, Hitachi, Ltd. (Japan); Miki Isawa, Hitachi High-Technologies Corp. (Japan); Jeroen Meessen, Ingrid Minnaert-Janssen, Peter Vanoppen, ASML Netherlands B.V. (Netherlands); Kenji Watanabe, Hitachi High-Technologies Corp. (Japan) [6922-67]

11:30 am: **Automatic CD-SEM offline recipe creation for process monitoring in a logic fab environment in high-volume production**, Stefanie Gil Girol, Stefan Roling, AMD Saxony LLC & Co. KG (Germany); Ovadya Menadeva, Dan Levitzky, Adi Costa, Daniel Fischer, Applied Materials (Israel) [6922-69]

11:50 am: **Automated CD-SEM metrology for efficient TD and HVM**, Alexander Starikov, Satya P. Mulapudi, Intel Corp. [6922-70]

Lunch/Exhibition Break 12:10 to 1:50 pm

SESSION 14

Conv. Ctr. J2 Thurs. 1:50 to 3:10 pm

Novel Methods and Applications

Session Chairs: **Richard M. Silver**, National Institute of Standards and Technology; **Bhanwar Singh**, Advanced Micro Devices, Inc.

1:50 pm: **Modeling for metrology with a helium beam**, Ranjan Ramachandra, David C. Joy, The Univ. of Tennessee [6922-71]

2:10 pm: **Novel CD inspection technology leveraging a form birefringence in a Fourier space**, Akitoshi Kawai, Daisaku Mochida, Nikon Corp. (Japan); Kiminori Yoshino, Yuuichiro Yamazaki, Toshiba Corp. (Japan) [6922-72]

2:30 pm: **Experimental observation of reticle electrostatic damage that occurs below the threshold for ESD**, Gavin C. Rider, Microtome Precision, Inc.; Thottam S. Kalkur, Univ. of Colorado/Colorado Springs [6922-73]

2:50 pm: **Line-width roughness and cross-sectional characterization of sub-50-nm structures using CD-SAXS, SEM, and OCD**, Wen-Li Wu, National Institute of Standards and Technology [6922-74]

Coffee Break 3:10 to 3:40 pm

SESSION 15

Conv. Ctr. J2 Thurs. 3:40 to 5:00 pm

Line-Edge Roughness

Session Chairs: **Martha I. Sanchez**, IBM Almaden Research Ctr.; **Ofer Adan**, Applied Materials (Israel)


3:40 pm: **A novel method for pushing the limits of line-edge roughness detection by scatterometry**, Yoel Cohen, Nova Measuring Instruments Ltd. (Israel); Yoed Tsur, Technion-Israel Institute of Technology (Israel) . . . [6922-75]

4:00 pm: **Influence of image processing on line-edge roughness in CD-SEM measurement**, Atsuko Yamaguchi, Jiro Yamamoto, Hitachi, Ltd. (Japan); Hiroki Kawada, Takashi Iizumi, Hitachi High-Technologies Corp. (Japan) . . . [6922-76]

4:20 pm: **Practical and bias-free LWR measurement by CDSEM**, Shiang Bau Wang, Yuan-Hun Chiu, Hun-Yuan Tao, Y.J. Mii, Taiwan Semiconductor Manufacturing Co. Ltd. (Taiwan) [6922-77]

4:40 pm: **Fractal dimension of line-width roughness and its effects on transistor performance**, V. Constantoudis, E. Gogolides, Institute of Microelectronics (Greece) [6922-156]

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Courses of Related Interest

See Course Materials Desk for course descriptions.

SC886 **Line Edge Roughness** (Gallatin) Sunday, 1:30 to 5:30 pm

SC831 **Introduction to Scatterometry Metrology: Theory and Application** (Barry, Bao) Sunday, 1:30 to 5:30 pm

SC105 **CD Metrology and Image Formation in the Scanning Electron Microscope (SEM)** (Postek, Wells) Sunday, 8:30 am to 5:30 pm

SC101 **Introduction to Microlithography: Theory, Materials, and Processing** (Willson, Thompson, Bowden) Sunday, 8:30 am to 5:30 pm

SC579 **Photomask Fabrication and Technology Basics** (Duff) Sunday, 8:30 am to 5:30 pm

WS619 **Intellectual Assets for Micro/Nano Electronics and Lithography** (Cole) Monday, 1:30 to 5:30 pm

Conference 6923 • Convention Center Hall 3-Monday/ Marriott San Jose Ballroom Salon III-Tuesday and Wednesday

Monday-Wednesday 25-27 February 2008 • Proceedings of SPIE Vol. 6923

Advances in Resist Materials and Processing Technology XXV

Conference Chair: **Clifford L. Henderson**, Georgia Institute of Technology

Conference Co-Chair: **Robert D. Allen**, IBM Almaden Research Ctr.

Program Committee: **George G. Barclay**, Rohm and Haas Electronic Materials; **Sean D. Burns**, IBM Thomas J. Watson Research Ctr.; **Ralph R. Dammel**, AZ Electronic Materials USA Corp.; **Douglas J. Guerrero**, Brewer Science, Inc.; **Christoph K. Hohle**, Qimonda Dresden GmbH & Co. OHG (Germany); **Qinghuang Lin**, IBM Thomas J. Watson Research Ctr.; **Nobuyuki N. Matsuzawa**, Sony Atsugi Technology Ctr. (Japan); **Dah-Chung Owe-Yang**, Shin-Etsu MicroSi, Inc.; **Adam R. Pawloski**, Affymetrix, Inc.; **Vivek M. Prabhu**, National Institute of Standards and Technology; **Ernisse Steve Putna**, Intel Corp.; **Mark H. Somervell**, Tokyo Electron America, Inc.; **Gregory M. Wallraff**, IBM Almaden Research Ctr.

Monday 25 February

SESSION 3

Conv. Ctr. Hall 3 Mon. 11:00 to 11:10 am

Opening Remarks

Session Chair: **Clifford L. Henderson**, Georgia Institute of Technology

2007 C. Grant Willson Best Paper Presentation

ROHMIHAAS 
Electronic Materials

SESSION 1

Conv. Ctr. Hall 3 Mon. 11:10 am to 12:30 pm

Keynote Session

Session Chair: **Robert D. Allen**, IBM Almaden Research Ctr.

11:10 am: **Rise of chemical amplification resists from laboratory curiosity to paradigm enabling Moore's Law (Keynote Presentation)**, Hiroshi Ito, IBM Almaden Research Ctr. [6923-01]

11:50 am: **DNA Origami: folding DNA to create arbitrary shapes and patterns (Keynote Presentation) (Presentation Only)**, Paul W. K. Rothemund, California Institute of Technology. [6923-02]

Lunch Break 12:30 to 1:50 pm

SESSION 2

Conv. Ctr. Hall 3 Mon. 1:50 to 3:30 pm

Materials and Processes for Immersion Lithography I

Session Chairs: **Ralph R. Dammel**, AZ Electronic Materials USA Corp.; **Gregory M. Wallraff**, IBM Almaden Research Ctr.

1:50 pm: **The limitations of high-index resists for 193-nm hyper-NA lithography**, Gregory R. McIntyre, IBM Corp.; Daniel P. Sanders, Ratnam Sooriyakumaran, Hoa D. Truong, Robert D. Allen, IBM Almaden Research Ctr. [6923-03]

2:10 pm: **High-index resist for 193-nm immersion lithography**, Kazuya Matsumoto, The Univ. of Texas at Austin and Tokyo Institute of Technology (Japan); Elizabeth A. Costner, Isao Nishimura, The Univ. of Texas at Austin; Mitsuru Ueda, Tokyo Institute of Technology (Japan); C. Grant Willson, The Univ. of Texas at Austin. [6923-04]

2:30 pm: **Development of an operational high-refractive index resist for 193-nm immersion lithography**, Paul Zimmerman, Jeffrey D. Byers, Bryan J. Rice, SEMATECH, Inc. [6923-05]

2:50 pm: **Non-topcoat resist design for immersion process at 32-nm node**, George G. Barclay, Rohm and Haas Electronic Materials; Cheng-Han Wu, Wan-Ju Tseng, Chien Nan Pan, Chia Hung Lin, Chun-Chi Yu, Bo Jou Lu, United Microelectronics Corp. (Taiwan); Deyan Wang, Vaishali R. Vohra, Cheng Bai Xu, Stefan J. Caporale, Rohm and Haas Electronic Materials. [6923-06]

3:10 pm: **Understanding the relationship for advancing and receding angles versus defects in top-coatless immersion photoresists**, Willard E. Conley, Freescale Semiconductor, Inc.; Mark Slezak, JSR Micro, Inc.; Richard Johnson, IBM Corp. [6923-07]

Coffee Break 3:30 to 4:00 pm

Conv. Ctr. Hall 3 Mon. 4:00 to 6:00 pm

Materials and Processes for Immersion Lithography II

Session Chairs: **George G. Barclay**, Rohm and Haas Electronic Materials; **Qinghuang Lin**, IBM Thomas J. Watson Research Ctr.

4:00 pm: **Self-segregating materials for immersion lithography**, Daniel P. Sanders, Linda K. Sundberg, Ratnam Sooriyakumaran, Phillip J. Brock, Hiroshi Ito, Hoa D. Truong, Joy Y. Cheng, Robert D. Allen, IBM Almaden Research Ctr. [6923-08]

4:20 pm: **Development and evaluation of a 193-nm immersion generation-three fluid**, Paul A. Zimmerman, Jeffrey D. Byers, Bryan J. Rice, SEMATECH, Inc.; Robert Rodriguez, Dongyan Wang, Emmannuel P. Giannelis, Christopher K. Ober, Cornell Univ.; Naphtali O'Connor, Nicholas J. Turro, Columbia Univ. [6923-09]

4:40 pm: **New high-index fluids for immersion lithography**, Elizabeth A. Costner, Kazuya Matsumoto, J. Christopher Taylor, Brian Long, The Univ. of Texas at Austin; William A. Wojtczak, SACHEM, Inc.; C. Grant Willson, The Univ. of Texas at Austin. [6923-10]

5:00 pm: **A new class of low-bake resists for 193-nm immersion lithography**, Ratnam Sooriyakumaran, Richard A. DiPietro, Hoa D. Truong, Phillip J. Brock, Robert D. Allen, IBM Almaden Research Ctr.; Irene Popova, Wu-Song Huang, Kuang-Jung R. Chen, Pushkara R. Varanasi, IBM Microelectronics Div. [6923-11]

5:20 pm: **Process development for high-speed scanning ArF immersion lithography**, Nobuji Matsumura, Norihiko Sugie, Kentaro Goto, Yoshikazu Yamaguchi, JSR Corp. (Japan); Hirokazu Tanizaki, Katsushi Nakano, Tomoharu Fujiwara, Nikon Corp. (Japan); Shinya Wakamizu, Hirofumi Takeguchi, Hiroshi Arima, Hideharu Kyoda, Kosuke Yoshihara, Junichi Kitano, Tokyo Electron Kyushu Ltd. (Japan) [6923-12]

5:40 pm: **Immersion resist process for 32-nm node logic devices**, Tatsuhiko Ema, Koutaro Sho, Hiroki Yonemitsu, Shinichi Ito, Shoji Mimotogi, Hideaki Harakawa, Akiko Nomachi, Toshiba Corp. (Japan) [6923-13]

Conference 6923 • Convention Center Hall 3

Conv. Ctr. Hall 3 Mon. 6:00 to 8:00 pm

Posters-Monday

The following posters will be displayed all day Monday. Authors will be present during the formal poster session Monday evening between 6:00 and 8:00 pm for discussion. Authors may set-up their posters after 10:30 am on Monday.

Molecular Resists

Water-developable negative-tone single-molecule resists: high-sensitivity nonchemically amplified resists, Richard A. Lawson, Georgia Institute of Technology; Wang Yueh, Intel Corp.; Laren M. Tolbert, Clifford L. Henderson, Georgia Institute of Technology. [6923-57]

Adamantane-based molecular glass resist for 193-nm lithography and beyond, Shinji Tanaka, Nobuaki Matsumoto, Hidetoshi Ohno, Idemitsu Kosan Co., Ltd. (Japan); Naoyoshi Hatakeyama, Idemitsu Chemicals; Katsuki Ito, Kazuya Fukushima, Idemitsu Kosan Co., Ltd. (Japan). [6923-58]

Positive-tone molecular glass photoresist based on acidolysis of acetal compounds, Liyuan Wang, Xiaoxiao Zhai, Beijing Normal Univ. (China) [6923-59]

Molecular glass resists for NGL lithography, Anuja De Silva, Nelson M. Felix, Jin-Kyn Lee, Christopher K. Ober, Cornell Univ. [6923-60]

The effect of EUV molecular glass architecture on the bulk dispersion of photo-acid generators, David L. VanderHart, Kristopher A. Lavery, National Institute of Standards and Technology; Kwang-Woo Choi, Intel Corp.; Vivek M. Prabhu, Eric K. Lin, National Institute of Standards and Technology; Anuja De Silva, Nelson M. Felix, Christopher K. Ober, Cornell Univ. [6923-61]

Molecular resists for EUV and EB lithography, Ichiki Takemoto, Nobuo Ando, Sumitomo Chemical Co., Ltd. (Japan) [6923-62]

Materials and Processes for Immersion Lithography

Options for high-index fluids for third-generation 193i lithography, Seth Kruger, Srividya Revuru, Shao-Zhong Zhang, Dimitri Vaughn, Eric Block, Univ. at Albany; Paul Zimmerman, SEMATECH, Inc.; Robert L. Brainard, Univ. at Albany. [6923-63]

High-index resists of anionic photo-acid generator (PAG) bound polymers for 193-nm immersion lithography, Kenneth E. Gonsalves, Mingxing Wang, The Univ. of North Carolina at Charlotte [6923-64]

Development of top-coatless immersion resist, Guanyang Lin, Srinivasan Chakrapani, Clement Anyadiegwu, Takanori Kudo, Ralph Dammel, Munirathna Padmanaban, AZ Electronic Materials USA Corp. [6923-65]

Wafer bevel cleaning technology for immersion lithography, Osamu Tamada, Masakazu Sanada D.D.S., Shuichi Yasuda, Masaya Asai, SOKUDO Co., Ltd. (Japan) [6923-66]

Application technology of stacked film with highly controlled edge structure, Tomohiro Iseki, Tokyo Electron Kyushu Ltd. [6923-67]

The relationship between material properties and patterning performance in sub-50-nm immersion lithography, Jae-Hyun Kim, Youngho Kim, Taesung Kim, SAMSUNG Electronics Co., Ltd. (South Korea). [6923-68]

The study of defect control and patterning performance for top coating free resist process, Myoung Soo Kim, Hynix Semiconductor Inc. (South Korea) [6923-69]

Highly hydrophobic materials for ArF immersion lithography, Yoko Takebe, Naoko Shirota, Takashi Sasaki, Koichi Murata, Osamu Yokokoji, Asahi Glass Co., Ltd. (Japan) [6923-71]

Improvements of adhesion and hydrophobicity of wafer bevel in water immersion lithography, Mamoru Terai, Teruhiko Kumada, Mitsubishi Electric Corp. (Japan); Takeo Ishibashi, Takuya Hagiwara, Tetsuro Hanawa, Renesas Technology Corp. (Japan); Yoko Takebe, Osamu Yokokoji, Asahi Glass Co., Ltd. (Japan); Tomoharu Fujiwara, Hiroshi Akiyama, Nikon Corp. (Japan) ... [6923-72]

Process manufacturability evaluation for next-generation immersion technology node, Kathleen R. Nafus, Masashi Enomoto, Takeshi Shimoaoki, Takahisa Otsuka, Hitoshi Kosugi, Tsuyoshi Shibata, Megumi Jyousaka, Tokyo Electron Kyushu Ltd. (Japan); Joerg Mallmann, Mireia Blanco-Montecon, Eelco van Setten, Jo M. Finders, ASML Netherlands B.V. (Netherlands) ... [6923-73]

High-index resists for immersion lithography using metal oxide nanoparticles, Andrew K. Whittaker, Idriss Blakey, Heping Liu, Lan Chen, Bronwin Dargaville, The Univ. of Queensland (Australia); Paul Zimmerman, SEMATECH, Inc. [6923-75]

Formation mechanism of 193-nm immersion defects and defect reduction strategies, Yayi Wei, Stefan R. Brandl, Frank Goodwin, Qimonda North America Corp. [6923-76]

Synthesis of novel α -fluoroacrylates and related polymers for immersion lithography, Yamashita Tsuneo, Ishikawa Takuji, Morita Masamichi, Kanemura Takashi, Aoyama Hirokazu, Daikin Industries, Ltd. (Japan) [6923-77]

Fundamental characterization of resist and topcoat properties for immersion lithography, Kaveri Jain, Micron Technology, Inc. [6923-78]

Materials and Processes for Double Patterning/Double Exposure

A lithographic and process assessment of photoresist stabilization for double-patterning using 172-nm photoresist curing, Nikolaos Bekiaris, Hiram Cervera, Junyan Dai, SOKUDO Co., Ltd.; Ryoung-Han Kim, Alden Acheta, Thomas Wallow, Jong-Wook Kye, Harry J. Levinson, Advanced Micro Devices, Inc.; Thomas Nowak, James Yu, Applied Materials, Inc. [6923-79]

Insoluble treatment by ion plantation in resist stacking process, Hiroko Nakamura, Takeshi Shibata, Katsumi Rikimaru, Sanae Ito, Satoshi Tanaka, Soichi Inoue, Toshiba Corp. (Japan) [6923-80]

Double-patterning study with inverse lithography, Sang-Kon Kim, Hanyang Univ. (South Korea) [6923-81]

193-nm negative-tone resist for double imaging, Jun Iwashita, Kazuhito Sasaki, Sho Abe, Tomoyuki Ando, Takeshi Iwai, Tokyo Ohka Kogyo Co., Ltd. (Japan) [6923-82]

Resist Fundamentals

Photons, electrons, and acid yields in EUV photoresists, Robert L. Brainard, Elsayed Hassanein, Brad L. Thiel, Univ. at Albany; Franco Cerina, Univ. of Wisconsin/Madison; Richard Moore II, Richard J. Matyi, Univ. at Albany; Matt Malloy, Anwar Khurshid, Andrew C. Rudack, SEMATECH, Inc.; Patrick P. Naulleau, Univ. at Albany; Kim R. Dean, SEMATECH, Inc. [6923-84]

Thickness impact on deprotection kinetic of 193-nm resist thin films, Jean-Hervé Tortai, Lab. d'Electronique de Technologie de l'Information (France). [6923-85]

Process-induced bias: a study of resist design and process implications, Steven A. Scheer, Michael A. Carcasi, Tokyo Electron America, Inc.; Tsuyoshi Shibata, Takahisa Otsuka, Tokyo Electron Kyushu Ltd. (Japan) [6923-86]

ArF photoresist formulation influence on elliptic contact shape when using a dipole illumination, Danilo De Simone, Enrico Tenaglia, Gina Cotti, STMicroelectronics (Italy); Toru Kimura, Jan Ronsmans, JSR Micro Materials Innovation (Belgium). [6923-87]

Dynamics of poly(4-hydroxystyrene) radical cation, Kazumasa Okamoto, Takahiro Kozawa, Seiichi Tagawa, Osaka Univ. (Japan) [6923-89]

Dependence of acid generation efficiency on molecular structure and concentration of acid generator in chemically amplified EUV resist, Ryo Hirose, Takahiro Kozawa, Seiichi Tagawa, Osaka Univ. (Japan); Toshiyuki Kai, Tsutomu Shimokawa, JSR Corp. (Japan) [6923-90]

Characterization of the latent image to developed image by chemical force microscopy in model-EUV photoresists, Kwang-Woo Choi, Intel Corp.; John T. Woodward, Kristopher A. Lavery, Vivek M. Prabhu, Eric K. Lin, Wen-Li Wu, National Institute of Standards and Technology; Michael J. Leeson, Intel Corp. [6923-91]

Study on deprotection reaction analysis system, Atsushi Sekiguchi, Litho Tech Japan Co., Ltd. (Japan) [6923-92]

A comparison of photoresist resolution metrics, Piyush Pathak, IBM Corp.; Thomas I. Wallow, Bruno M. LaFontaine, Yunfei Deng, Ryoung-Han Kim, Jong-Wook Kye, Harry J. Levinson, Advanced Micro Devices, Inc.; Patrick P. Naulleau, Lawrence Berkeley National Lab.; Chris N. Anderson, Univ. of California/Berkeley. [6923-94]

RAFT technology for the production of advanced photoresist polymers, Michael T. Sheehan, Hiroshi Okazaki, James R. Sounik, William B. Farnham, DuPont Electronic Polymers. [6923-96]

Effect of PAG and matrix structure on PAG acid generation behavior under UV and high-energy radiation exposure, Cheng-Tsung Lee, Georgia Institute of Technology; Mingxing Wang, Kenneth E. Gonsalves, The Univ. of North Carolina at Charlotte; Wang Yueh, Intel Corp.; Clifford L. Henderson, Georgia Institute of Technology. [6923-97]

ARCs and Multilayer Material and Processes

Plasma etch properties of organic BARCs. Runhui Huang, Michael J. Weigand, Shannon Brown, Brian A. Smith, Brewer Science, Inc. [6923-98]

The design and evaluation of high-barrier performance organic BARC material. Tomohisa Ishida, Rikimaru Sakamoto, Yoshiomi Hiroi, Daisuke Maruyama, Takuya Oohashi, Takafumi Endo, Shigeo Kimura, Yasushi Sakaida, Makoto Nakajima, Bang-Ching Ho, Hisayuki Watanabe, Nissan Chemical Industries, Ltd. (Japan). [6923-99]

Development of high-performance trilayer materials. Dah-Chung Owe-Yang, Shin-Etsu MicroSi, Inc.; Toshihara Yano, Takafumi Ueda, Tsutomu Ogihara, Shocho Shirai, Motoaki Iwabuchi, Shin-Etsu Chemical Co., Ltd. (Japan)[6923-100]

High-etch-rate low-bias bow outgassing BARC via-filling materials for 193-nm ArF lithographic process. Huirong Yao, Zhong Xiang, Salem K. Mullen, Jian Yin, Walter Liu, Jianhui Shan, Eleazar Gonzalez, Guanyang Lin, Mark Neisser, AZ Electronic Materials USA Corp. [6923-101]

Ultraviolet cross-link process using sacrificial materials for advanced planarization, resist poisoning, and sublimate defect reduction. Satoshi Takei, Yusuke Horiguchi, Tetsuya Shinjo, Yuichi Mano, Kazuhisa Ishii, Bang-Ching Ho, Yasuyuki Nakajima, Nissan Chemical Industries, Ltd. (Japan); Makoto Muramatsu, Mitsuaki Iwashita, Katsuhiko Tsuchiya, Tokyo Electron Ltd. (Japan) [6923-102]

Gap-fill type HSQ/ZEP520A bilayer resist process-(I): HSQ-coated ZEP520A CD shrinkage for 32-nm trench patterns. Wei-Su G. Chen, Industrial Technology Research Institute (Taiwan) [6923-103]

Challenges of non-PFOS top antireflective coating material. Shu-Hao Hsu, Qimonda Dresden GmbH & Co. OHG (Germany) and Nanya Technology Corp. (Taiwan); Inge Vermeir, Matthias Scholze, Matthias Voigt, Janine Gierth, Armelle Mittermeier, Iris Mäge, Lars Voelkel, Qimonda Dresden GmbH & Co. OHG (Germany). [6923-104]

KrF bilayer resist defects: cause, analysis, and reduction. Brian Osborn, Cherry Tang, Stacy Sakai, Go Nagatani, Gloria Quinto, Anna M. Minvielle, Spansion Inc. [6923-105]

Sub-45-nm resist process using stacked-mask process. Yuriko Seino, Katsutoshi Kobayashi, Koutaro Sho, Hirokazu Kato, Seiro Miyoshi, Yasunobu Oonishi, Keisuke Kikutani, Junko Abe, Hisataka Hayashi, Tokuhisa Ohiwa, Toshiba Corp. (Japan) [6923-106]

High-etch-rate bottom-antireflective coating and gap-fill materials using dextrin derivatives in via first dual-Damascene lithography process. Satoshi Takei, Tetsuya Shinjo, Yasushi Sakaida, Keisuke Hashimoto, Yasuyuki Nakajima, Nissan Chemical Industries, Ltd. (Japan). [6923-107]

Silicon-based antireflective spin-on hardmask materials for 45-nm pattern of immersion ArF lithography. Sang Kyun Kim, Hyeon Mo Cho, Sang Ran Koh, Mi-Young Kim, Hui Chan Yoon, Yong-Jin Chung, Jong-Seob Kim, Tu-Won Chang, CHEIL Industries, Inc. (South Korea). [6923-108]

Optimization of BARC process for hyper-NA immersion. Kilyoung Lee, Jung-Hyung Lee, Sung-Koo Lee, Dong-Heok Park, Cheolkyu Bok, Seung-Chan Moon, Hynix Semiconductor Inc. (South Korea) [6923-109]

Development of wet development BARCs for implant applications. Takahiro Hamada, Nissan Chemical Industries, Ltd. (Japan). [6923-110]

Development of new BARC for immersion process using hyper-NA. Hyo Jung Roh, Man Ho Han, Sang Jeoung Kim, Hyun Jin Kim, Jaehyun Kim, Dongjin Semichem Co. Ltd. (South Korea) [6923-111]

A lithographic and pattern transfer evaluation of dual-BARC systems for flash integration schemes. Jun-Chen Lai, Powerchip Semiconductor Corp. (Taiwan); Robert Auger, Michael T. Reilly, Nick Pugliano, Rohm and Haas Electronic Materials [6923-112]

Application of organic BARC for 193-nm immersion litho. Jian Yin, Zhong Xiang, Huirong Yao, Waiter Liu, Jianhui Shan, Richard A. Collett, Eleazar Gonzalez, Salem K. Mullen, Mark Neisser, AZ Electronic Materials USA Corp. [6923-113]

Novel spin-on organic hardmask with high plasma-etch resistance. Chang-Il Oh, Jin-Kuk Lee, Min-Soo Kim, Kyong-Ho Yoon, Hwan-Sung Cheon, Nataliya Tokareva, Jee-Yun Song, Jong-Seob Kim, Tu-Won Chang, CHEIL Industries, Inc. (South Korea). [6923-114]

Dye-filled developer-soluble BARCs for 193-nm immersion lithography. James D. Meador, Carol Beaman, Charlyn Stroud, Joyce A. Lowes, Ramil-Marcelo L. Mercado, Brewer Science, Inc. [6923-115]

Low out-gassing organic spin-on hardmask. Shinya Minegishi, Nakaatsu Yoshimura, Mitsuo Sato, Yosuke Konno, Keiji Konno, Junichi Takahashi, Shigeru Abe, Yoshikazu Yamaguchi, Tsutomu Shimokawa, JSR Corp. (Japan)[6923-116]

Gap-fill type HSQ/ZEP520A bilayer resist process-(II): HSQ island and spacer formation. Wei-Su G. Chen, Industrial Technology Research Institute (Taiwan) [6923-117]

Reflection control for immersion lithography at 45/32-nm nodes. Wan-Ju Tseng, Ruei-Hung Hsu, Shu Huei Hou, Tzu-Huai Tseng, Bill Lin, Chun-Chi Yu, United Microelectronics Corp. (Taiwan); Sue Ryeon Kim, Jeong Yun Yu, Gerald B. Wayton, Maurizio Ciambra, Nick Pugliano, Suzanne Coley, Rohm and Haas Electronic Materials [6923-118]

Second-generation radiation sensitive 193-nm developable bottom antireflective coatings (DBARC): recent results. Francis M. Houlihan, AZ Electronic Materials USA Corp. [6923-119]

Effects of bake temperature and surface modifications. Charles J. Neef, Rachel Giessert, Cheryl Nesbit, Brewer Science, Inc. [6923-120]

Simulation of Resist Processes

A calibrated photoresist model for pattern prediction. Yung L. Hung, Chun C. Liao, Tengyen Huang, Nanya Technology Corp. (Taiwan); Stewart A. Robertson, John J. Biafore, KLA-Tencor Corp.; Arthur Lin, KLA-Tencor Corp. (Taiwan) [6923-121]

Resist Materials and Processes

Fabrication of 32-nm contact/via hole by photolithographic-friendly method. Tetsu Kawasaki, Satoru Shimura, Fumiko Iwao, Masato Kushibiki, Kazuhide Hasebe, Tokyo Electron Ltd. (Japan); Michael A. Carcasi, Mark H. Somervell, Steven A. Scheer, Tokyo Electron America, Inc. [6923-122]

Evaluation of adamantane derivatives for chemically amplified resist: a comparison between ArF, EUV, and EB exposures. Kikuo Furukawa, Mitsubishi Gas Chemical Co., Inc. (Japan); Seiichi Tagawa, Shu Seki, Takahiro Kozawa, Osaka Univ. (Japan). [6923-123]

Leading-edge adamantyl polymers designed for 193-nm lithography. Kazuya Fukushima, Shinji Tanaka, Nobuaki Matsumoto, Hidetoshi Ohno, Naoya Kawano, Hideki Yamane, Idemitsu Kosan Co., Ltd. (Japan); Naoyoshi Hatakeyama, Idemitsu Chemicals; Katsuki Ito, Idemitsu Kosan Co., Ltd. (Japan) [6923-124]

Wet trimming process for critical dimension reduction. Brian A. Smith, Sam X. Sun, Brewer Science, Inc. [6923-125]

Investigation of the modifications induced in 193-nm photoresists by the HBr cure plasma treatment. Arnaud F. Bazin, STMicroelectronics (France); Erwine Pargon, Xavier Mellhaoui, Commissariat à l'Energie Atomique (France); Damien Perret, Rohm and Haas Electronic Materials (France); Bénédicte P. Mortini, STMicroelectronics (France); Olivier P. Joubert, Commissariat à l'Energie Atomique (France) [6923-126]

Molecular contamination control technologies for high-volume production in high-NA 193-nm lithography (Phase II). Toshiro Nakano, Takashi Tanahashi, Akihiro Imai, Kazuki Yamana, Tainen Shimotsu, NICHIAS Corp. (Japan) [6923-127]

Contact-hole reduction technique for 45-nm and beyond. Warren M. Montgomery, College of Nanoscale Science and Engineering; Steve Bennett, Lior Huli, John L. Weeks, Univ. at Albany [6923-128]

Resist reflow process for arbitrary 22-nm node pattern. Hye-Keun Oh, Joon-Min Park, Ilsin An, Hanyang Univ. (South Korea). [6923-129]

Processing and modeling optimization for grayscale lithography. Thomas E. Dillon, Janusz A. Murakowski, Dennis W. Prather, Univ. of Delaware. [6923-131]

Advanced resist process enabling implementation of CD controllability for 32-nm and beyond. Satoru Shimura, Fumiko Iwao, Tetsu Kawasaki, Hidetami Yaegashi, Yoshiaki Yamada, Tokyo Electron Ltd. (Japan). [6923-132]

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An innovative approach to describing 32-nm/22-nm node poly-silicon gates, Satoru Shimura, Fumiko Iwao, Tetsu Kawasaki, Hidetami Yaegashi, Tokyo Electron Ltd. (Japan) [6923-133]

Development of thick negative photoresists for electroplating applications, Chunwei Chen, Robert Plass, Edward Ng, Chien-Hsien Sam Lee, Stephen Meyer, Georg Pawlowski, AZ Electronic Materials USA Corp.; Rozalia Beica, Semitool, Inc. [6923-134]

Synthesis and evaluation of novel resist monomers and copolymers for ArF lithography: part II, Osamu Nakayama, Takashi Fukumoto, Miki Tachibana, Kuraray Co., Ltd. (Japan); Junko Sato, Consultant (Japan); Masahiko Kitayama, Tsuyoshi Kajiyashiki, Kuraray Co., Ltd. (Japan) [6923-135]

Line-width roughness performance of novel surface conditioner solutions for immersion lithography, Bo Jou Lu, United Microelectronics Corp. (Taiwan) [6923-136]

Effect of nanofiltration on photochemical integrity, Jian Wei, Haizheng Zhang, Entegris, Inc.; Ryan Buschjost, Brewer Science, Inc.; Aiwen Wu, Entegris, Inc. [6923-137]

Performance comparison of negative resists for copper rerouting and other electroplating applications, Medhat A. Toukhy, Chunwei Chen, Margareta Paunescu, Georg Pawlowski, AZ Electronic Materials USA Corp. . . . [6923-138]

Post develop stain defect reduction, Masahiko Harumoto, Akihiro Hisai, Minoru Sugiyama, Takuya Kuroda, SOKUDO Co., Ltd. (Japan) [6923-139]

Impact of surface treatment on resist reflow process, Young-Je Yun, Jin-Ho Park, Hakyu Choi, Seung Ryoung Park, Jeahee Kim, Keeho Kim, Dongbu Electronics Co., Ltd. (South Korea) [6923-141]

Achieving small dimensions with an environmentally friendly solvent: photoresist development using supercritical CO₂, Nelson M. Felix, Anuja De Silva, Christopher K. Ober, Cornell Univ. [6923-142]

Wafer shape measurement and compensation at the track PEB for improved CD uniformity, Junyan Dai, Lu Chen, Timothy B. Michaelson, Hiram Cevera, Brian C. Lue, Harald Herchen, Kim R. Vellore, Nikos Bekiaris, SOKUDO USA, LLC [6923-143]

Wafer warp caused by thick film resists acting as a permanent part of the device, Rainer Leuschner, Martin Franosch, Infineon Technologies AG (Germany); Timothy Dow, Infineon Technologies Austria AG (Austria) [6923-144]

Characterization of array CD uniformity with respect to pattern density in 193-nm dry photolithography, Vishal Sipani, David A. Kewley, Kaveri Jain, Erik R. Byers, Bruce Daybell, Anthony C. Krauth, Micron Technology, Inc. [6923-145]

Sensitivity enhanced CMOS imager with the minimized-UV radiation of patterning process, Sang Wook Ryu, Mangil Han, Kanghyun Lee, Keeho Kim, Dongbu HiTek (South Korea) [6923-146]

Non-ionic photo-acid generators for chemically amplified resists, Hitoshi Yamato, Toshikage Asakura, Yuichi Nishimae, Masaki Ohwa, Ciba Specialty Chemicals K.K. (Japan) [6923-147]

The synthesis of novel ester acetal polymers and their application for chemically amplified positive i-line photoresist, Liyuan Wang D.D.S., Beijing Normal Univ. (China) [6923-148]

Study for aluminum metal patterning process with oxide hardmask in 90-nm s-flash memory device fabrication, Sangil Hwang, Mangil Han, Kanghyun Lee, Keeho Kim, Dongbu HiTek (South Korea) [6923-149]

Defect reduction using new digital valve dispensing technology, Garrett Standley, Freescale Semiconductor, Inc.; Brian W. Kidd, Integrated Designs, L.P. [6923-150]

Study for high-voltage gate RIE process in LDI (LCD Driver IC) device fabrication, Min-Gon Lee, Dongbu HiTek (South Korea) [6923-152]

Study of shallow trench isolation dry etching process using oxide hard mask and KrF photoresist in 90-nm stand-alone flash device, Eun-sang Cho, Sangwook Ryu, Kanghyun Lee, Keeho Kim, Dongbu HiTek (South Korea) [6923-153]

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Evaluation of reflection control for line features of multiple pitch, Michael T. Reilly, Mike Wagner, Rohm and Haas Electronic Materials; Warren Montgomery, Albany NanoTech; Nick Pugliano, Rohm and Haas Electronic Materials [6923-155]

Improvement of 90-nm technology photo alignment through TiN hard-mask removing upon scribe-line alignment mark area, Wen-Shiang Liao, United Microelectronics Corp. (Taiwan) [6923-157]

Successful application of new rinse approach for defect reduction in sub-60-nm ArF lithography processes, C. Chiang, Qimonda Dresden GmbH & Co. OHG (Germany) and Nanya Technology Corp. (Taiwan); M. Voigt, Y. Chiu, Y. Wu, C. Lin, F. Kamm, Qimonda Dresden GmbH & Co. OHG (Germany) [6923-158]

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Spray photoresist dispense uniformity, Joe Z. Coulter, Avago Technologies Ltd.; Brian W. Kidd, Integrated Designs, L.P.; Jeff Hawks, EV Group Inc. [6923-160]

EUV Resists

EUV-resist outgassing analysis in Selete, Julius Joseph S. Santillan, Shinji Kobayashi, Toshiro Itani, Semiconductor Leading Edge Technologies, Inc. (Japan) [6923-161]

Synthesis and evaluation of new photo-acid generators for EUV lithography, Yool Kang, Haisub Na, Kyoungtak Kim, Hyun-Woo Kim, Seong Woon Choi, SAMSUNG Electronics Co., Ltd. (South Korea) [6923-162]

EUV-resist based on low-molecular weight PHS, Masamitsu Shirai, Akitaka Kuroshima, Haruyuki Okamura, Osaka Prefecture Univ. (Japan); Koji Kaneyama, Toshiro Itani, Semiconductor Leading Edge Technologies, Inc. (Japan) [6923-163]

Quantitative analysis of EUV-resist outgassing, Shinji Kobayashi, Julius Joseph S. Santillan, Toshiro Itani, Semiconductor Leading Edge Technologies, Inc. (Japan) [6923-164]

Development of novel positive-tone resists for EUVL, Takanori Owada, Idemitsu Kosan Co., Ltd. (Japan); Takeo Watanabe, Hiroo Kinoshita, Univ. of Hyogo (Japan); Hiroaki Oizumi, Iwao Nishiyama, Association of Super-Advanced Electronics Technologies (Japan) [6923-165]

Development of partially fluorinated EUV-resist polymers for LER and sensitivity improvement, Takashi Sasaki, Osamu Yokokoji, Asahi Glass Co., Ltd. (Japan); Takeo Watanabe, Hiroo Kinoshita, Univ. of Hyogo (Japan) [6923-166]

Tuesday 26 February

SESSION 4

Marriott San Jose Ballroom Salon III Tues. 8:30 to 9:50 am

Materials and Processes for Double Patterning/Double Exposure

Session Chairs: Robert D. Allen, IBM Almaden Research Ctr.; Christoph K. Hohle, Qimonda Dresden GmbH & Co. OHG (Germany)

8:30 am: **Development of materials and processes for double patterning toward 32- nm node 193- nm immersion lithography process**, Shinji Tarutani, Hideaki Tsubaki, Kenji Wada, Fuji Photo Film Co., Ltd. (Japan) [6923-14]

8:50 am: **Resist freezing process for double-exposure scheme**, Kuang-Jung R. Chen, Wu-Song Huang, Waikin Li, Pushkara R. Varanasi, IBM Microelectronics Div.; Daniel P. Sanders, Linda K. Sundberg, IBM Almaden Research Ctr. [6923-16]

9:10 am: **Sub-40-nm half-pitch double patterning with resist freezing process**, Masafumi Hori, Tomoki Nagai, Atsushi Nakamura, Takayoshi Abe, Gouji Wakamatsu, Tomohiro Kakizawa, Yuusuke Anno, Makoto Sugiura, Shiro Kusumoto, Yoshikazu Yamaguchi, Tsutomu Shimokawa, JSR Corp. (Japan) [6923-17]

9:30 am: **The simulated effects of etch and novel material CD biasing on frequency doubling nanolithography**, Stewart A. Robertson, John J. Biafore, Trey Graves, Mark D. Smith, KLA-Tencor Corp. [6923-18]

Coffee Break 9:50 to 10:30 am

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SESSION 5

Marriott San Jose Ballroom Salon III. Tues. 10:30 am to 12:30 pm

Molecular Resists

Session Chairs: **Clifford L. Henderson**, Georgia Institute of Technology; **Ralph R. Dammel**, AZ Electronic Materials USA Corp.

10:30 am: **Novel molecular resist based on an amorphous truxene derivative**, Shigeki Hattori, Satoshi Saito, Koji Asakawa, Takeshi Koshiba, Tetsuro Nakasugi, Toshiba Corp. (Japan) [6923-20]

10:50 am: **Single-molecule chemically amplified resists based on ionic and non-ionic PAGs**, Richard A. Lawson, Cheng-Tsung Lee, Georgia Institute of Technology; Wang Yueh, Intel Corp.; Laren M. Tolbert, Clifford L. Henderson, Georgia Institute of Technology. [6923-21]

11:10 am: **Surface roughness of molecular resist for EUV lithography**, Minoru Toriumi, Semiconductor Leading Edge Technologies, Inc. (Japan) and Lab. for Interdisciplinary Science and Technology (Japan); Toshiro Itani, Semiconductor Leading Edge Technologies, Inc. (Japan). [6923-22]

11:30 am: **Chemically amplified molecular resists for e-beam lithography**, Jedsada Manyam, Francis Gibbons, Sara Diegoli, Mayandithevar Manickam, Jon A. Preece, Richard E. Palmer, Alex P. G. Robinson, The Univ. of Birmingham (United Kingdom) [6923-23]

11:50 am: **Chemically amplified molecular resist based on fullerene derivative for nanolithography**, Hiroki Yamamoto, Takahiro Kozawa, Seiichi Tagawa, Osaka Univ. (Japan); Tomoyuki Ando, Katsumi Ohmori, Junichi Onodera, Tokyo Ohka Kogyo Co., Ltd. (Japan) [6923-24]

12:10 pm: **New architectures for high-resolution patterning**, Christopher K. Ober, Anuja De Silva, Yi Yi, Nelson M. Felix, Drew C. Forman, Cornell Univ. [6923-25]

Lunch/Exhibition Break 12:30 to 1:50 pm

SESSION 6

Marriott San Jose Ballroom Salon III. Tues. 1:50 to 3:30 pm

Simulation of Resist Processes

Session Chairs: **Adam R. Pawloski**, Affymetrix, Inc.; **Robert D. Allen**, IBM Almaden Research Ctr.

1:50 pm: **Base quencher effects in chemically amplified resist at sub-30-nm fabrication**, Takahiro Kozawa, Seiichi Tagawa, Osaka Univ. (Japan); Julius Joseph S. Santillan, Minoru Toriumi, Toshiro Itani, Semiconductor Leading Edge Technologies, Inc. (Japan) [6923-26]

2:10 pm: **Molecular scale simulation of molecular glass photoresists**, Richard A. Lawson, Georgia Institute of Technology; Wang Yueh, Intel Corp.; Laren M. Tolbert, Clifford L. Henderson, Georgia Institute of Technology. [6923-27]

2:30 pm: **A comprehensive resist model for the prediction of line-edge roughness material and process dependencies in optical lithography**, Thomas Schnattinger, Andreas Erdmann, Fraunhofer Institut Integrierte System und Bauelem (Germany). [6923-28]

2:50 pm: **Monte Carlo simulation on line-edge roughness after development in chemically amplified resist of post-optical lithography**, Akinori Saeki, Takahiro Kozawa, Seiichi Tagawa, Osaka Univ. (Japan); Heidi B. Cao, Hai Deng, Michael J. Leeson, Intel Corp. [6923-29]

3:10 pm: **Extraction and identification of resist modeling parameters for EUV lithography**, Carlos Fonseca, Steven A. Scheer, Tokyo Electron America, Inc.; Roel Gronheid, IMEC (Belgium) [6923-30]

Coffee Break. 3:30 to 4:00 pm

SESSION 7

Marriott San Jose Ballroom Salon III. Tues. 4:00 to 5:40 pm

ARCs and Multilayer Materials and Processes

Session Chairs: **Douglas J. Guerrero**, Brewer Science, Inc.; **Sean D. Burns**, IBM Thomas J. Watson Research Ctr.

4:00 pm: **Generating high-resolution substrate features using spin-on trilayer materials**, David J. Abdallah, AZ Electronic Materials USA Corp.; Shinji Miyazaki, AZ Electronic Materials K.K. (Japan); Allen G. Timko, M. Dalil Rahman, Douglas S. McKenzie, Woo-Kyu Kim, Lyudmila Pylyneva, Hengpeng Wu, Ruzhi Zhang, Ping-Hung Lu, Mark Neisser, Ralph R. Dammel, AZ Electronic Materials USA Corp. [6923-32]

4:20 pm: **Graded spin-on organic bottom antireflective coating for high-NA lithography**, Dario L. Goldfarb, Sean D. Burns, Libor Vyklicky, Dirk Pfeiffer, IBM Thomas J. Watson Research Ctr.; Daniel P. Sanders, IBM Almaden Research Ctr.; Karen E. Petrillo, Aleksandra Clancy, IBM Thomas J. Watson Research Ctr.; Robert N. Lang, IBM Microelectronics Div.; Robert D. Allen, IBM Almaden Research Ctr.; David R. Medeiros, IBM Thomas J. Watson Research Ctr.; Dah-Chung Owe-Yang, Shin-Etsu MicroSi, Inc.; Kazumi Noda, Seiichiro Tachibana, Shozo Shirai, Shin-Etsu Chemical Co., Ltd. (Japan) [6923-33]

4:40 pm: **A high-Si content middle layer for ArF trilayer patterning applications**, Joseph T. Kennedy, Song-Yuan Xie, Ron Katsanes, Kyle Flanigan, Edward W. Rutter, Jr., Sudip Mukhopadhyay, Honeywell Inc. [6923-34]

5:00 pm: **Antireflective coating for multipatterning lithography**, Douglas J. Guerrero, Ramil-Marcelo L. Mercado, Joyce A. Lowes, Brewer Science, Inc. [6923-35]

5:20 pm: **A modified bilayer resist approach for 45-nm flash lithography**, Brian Osborn, Gloria Quinto, Cristina Cheung, Fei Wang, Fred Cheung, Frank Tsai, Anna M. Minvielle, Spansion Inc. [6923-36]

Wednesday 27 February

SESSION 8

Marriott San Jose Ballroom Salon III. Wed. 8:00 to 10:00 am

EUV Resists

Session Chairs: **Ernisse Steve Putna**, Intel Corp.; **Dah-Chung Owe-Yang**, Shin-Etsu MicroSi, Inc.

8:00 am: **Robust high-throughput resolution metrics for photoresists: a full-process sensitivity study**, Christopher N. Anderson, Patrick P. Naulleau, Lawrence Berkeley National Lab. [6923-37]

8:20 am: **Resist development to improve flare issue of EUV lithography**, Makiko Irie, Takako Suzuki, Takeyuki Mimura, Takeshi Iwai, Tokyo Ohka Kogyo Co., Ltd. (Japan). [6923-38]

8:40 am: **Progress in EUV-resist development**, Akio Saitou, Ken Maruyama, Daisuke Shimizu, Toshiyuki Kai, Tsutomu Shimokawa, JSR Corp. (Japan); Koichi Fujiwara, JSR Micro, Inc. [6923-39]

9:00 am: **Synthesis and properties of new anionic photoacid generators (PAGs) bound polymer resists for EUV lithography**, Mingxing Wang, The Univ. of North Carolina at Charlotte [6923-40]

9:20 am: **EUV-resist development in Selete**, Daisuke Kawamura, Koji Kaneyama, Shinji Kobayashi, Julius Joseph S. Santillan, Toshiro Itani, Semiconductor Leading Edge Technologies, Inc. (Japan). [6923-41]

9:40 am: **Photoresist-induced contrast loss and its impact on EUV imaging extendibility**, Koen van Inghen Schenau, Jan B. P. van Schoot, ASML Netherlands B.V. (Netherlands); Steven G. Hansen, ASML US, Inc. [6923-42]

Coffee Break. 10:00 to 10:30 am

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SESSION 9

Marriott San Jose Ballroom Salon III. Wed. 10:30 am to 12:30 pm

Resist Fundamentals

Session Chairs: **Clifford L. Henderson**, Georgia Institute of Technology; **Vivek M. Prabhu**, National Institute of Standards and Technology

10:30 am: **Finite element modeling of water uptake and PAG leaching in immersion lithography resist materials**, Benjamin M. Rath sack, Steven A. Scheer, Tokyo Electron America, Inc.; Yuhei Kuwahara, Junichi Kitano, Tokyo Electron Kyushu Ltd. (Japan); Roel Gronheid, IMEC (Belgium) [6923-43]

10:50 am: **A new technique for studying photo-acid generator chemistry and physics in polymer films using on-wafer ellipsometry and acid-sensitive dyes**, Cheng-Tsung Lee, Georgia Institute of Technology; Wang Yueh, Jeanette M. Roberts, Intel Corp.; Clifford L. Henderson, Georgia Institute of Technology. [6923-44]

11:10 am: **A comparison of the reaction-diffusion kinetics between model-EUV polymer and molecular-glass photoresists**, Shuhui Kang, Kristopher Lavery, National Institute of Standards and Technology; Kwang-Woo Choi, National Institute of Standards and Technology and Intel Corp.; Vivek M. Prabhu, Wen-Li Wu, Eric Lin, National Institute of Standards and Technology; Anuja De Silva, Nelson Felix, Christopher Ober, Cornell Univ. [6923-45]

11:30 am: **Roles of lactones in 193-nm resists**, Hiroshi Ito, Hoa D. Truong, Phillip J. Brock, IBM Almaden Research Ctr. [6923-46]

11:50 am: **Polymer matrix effects on acid generation**, Theodore H. Fedynyshyn, Russell B. Goodman, MIT Lincoln Lab.; Jeanette M. Roberts, Intel Corp. [6923-47]

12:10 pm: **Acid-base equilibrium in chemically amplified resist**, Kenichiro Natsuda, Takahiro Kozawa, Kazumasa Okamoto, Seiichi Tagawa, Osaka Univ. (Japan) [6923-48]

Lunch/Exhibition Break 12:30 to 1:40 pm

SESSION 10

Marriott San Jose Ballroom Salon III. Wed. 1:40 to 3:20 pm

Resist Materials and Processes

Session Chairs: **Nobuyuki N. Matsuzawa**, Sony Atsugi Technology Ctr. (Japan); **Mark H. Somervell**, Tokyo Electron America, Inc.

1:40 pm: **Ionic photo-acid generators containing functionalized semifluorinated sulfonates for high-resolution lithography**, Yi Yi, Ramakrishnan Ayothi, Christopher K. Ober, Cornell Univ.; Yueh Wang, Heidi B. Cao, Intel Corp. [6923-49]

2:00 pm: **Nonchemically amplified resists for 193-nm lithography**, Isao Nishimura, William H. Heath, Kazuya Matsumoto, Wei-Lun Jen, Saul S. Lee, Colin Neikirk, The Univ. of Texas at Austin; Tsutomu Shimokawa, Koji Ito, JSR Corp. (Japan); Koichi Fujiwara, JSR Micro, Inc.; Grant C. Willson, The Univ. of Texas at Austin. [6923-50]

2:20 pm: **ArF resists for 45-nm node implant layers and beyond**, Amandine Pikon, Rohm and Haas Electronic Materials [6923-51]

2:40 pm: **LWR reduction in low-k1 ArF-immersion lithography**, Kentaro Matsunaga, Daisuke Kawamura, Eishi Shiobara, Toshiba Corp. (Japan); Yuichiro Inatomi, Tetsu Kawasaki, Mitsuoaki Iwashita, Tokyo Electron Ltd. (Japan); Shinichi Ito, Toshiba Corp. (Japan) [6923-52]

3:00 pm: **All-dry photoresist systems: physical vapor deposition of molecular glasses**, Hans-Werner Schmidt, Christian Neuber, Frauke Pfeiffer, Univ. Bayreuth (Germany); Christopher K. Ober, Nelson M. Felix, Cornell Univ. [6923-53]

Coffee Break. 3:20 to 3:50 pm

SESSION 11

Marriott San Jose Ballroom Salon III. Wed. 3:50 to 6:10 pm

Joint Session on EUV Resists

Session Chairs: **Ernis Steve Putna**, Intel Corp.; **Bruno M. LaFontaine**, Advanced Micro Devices, Inc.

Joint Session with Conference 6521: Emerging Lithographic Technologies XII

3:50 pm: **Resolution, LER, and sensitivity limitations of photoresists**, Gregg M. Gallatin, Applied Math Solutions, LLC; Patrick Naulleau, Lawrence Berkeley National Lab.; Robert Brainard, Univ. at Albany; Dimitra Niakoula, Lawrence Berkeley National Lab.; Kim Dean, SEMATECH, Inc. [6921-55]

4:10 pm: **Evaluation of EUV resist materials for use at the 32-nm half-pitch node**, Thomas I. Wallow, Advanced Micro Devices, Inc.; Robert Brainard, Greg Denbeaux, Univ. at Albany; Chiew-Seng Koay, IBM Corp.; Warren Montgomery, Univ. at Albany; Karen Petrillo, IBM Thomas J. Watson Research Ctr.; Yayi Wei, Qimonda North America Corp.; Obert Wood, Advanced Micro Devices, Inc. [6921-56]

4:30 pm: **Extreme ultraviolet resist outgassing measurements and their effect on nearby surfaces**, Gregory Denbeaux, Rashi Garg, Chimaobi Mbanaso, Justin Waterman, Alin Antohe, Leonid Yankulin, Yu-Jen Fan, Univ. at Albany; Kim Dean, Andrea Wüest, SEMATECH, Inc. [6921-57]

4:50 pm: **Quantitative measurement of outgas products from EUV photoresists**, Charles Tarrio, Shannon Hill, Thomas Lucatorto, Jay Hendricks, Pat Abbott, Bruce Benner, National Institute of Standards and Technology. [6921-58]

5:10 pm: **Quantum yield, contrast curves, and optical density of EUV and 193i photoresists**, Robert L. Brainard, Elsayed Hassanein, Patrick P. Naulleau, Univ. at Albany; Gregg M. Gallatin, Applied Math Solutions, LLC; Richard J. Matyi, Univ. at Albany; James W. Thackeray, Kathleen Spear-Alfonso, Rohm and Haas Electronic Materials; Matthew Malloy, Anwar Khurshid, Emil C. Piscani, Andrew C. Rudack, Jeff D. Byers, Kim R. Dean, SEMATECH, Inc. [6921-59]

5:30 pm: **Rational design and synthesis of non-CA high-sensitivity polymeric EUV resists**, Andrew K. Whittaker, Kevin Jack, Heping Liu, The Univ. of Queensland (Australia); Idriss Blakely, Univ. of Queensland (Australia); David J. T.Hill, The Univ. of Queensland (Australia); Wang Yueh, Heidi B. Cao, Michael J. Leeson, Intel Corp. [6923-55]

5:50 pm: **A resist materials study for resolution and LWR improvement in EUV lithography**, Sou Kamimura, Katsuhiro Yamashita, Naoyuki Nishikawa, Fuji Photo Film Co., Ltd. (Japan). [6923-56]

Courses of Related Interest

See Course Materials Desk for course descriptions.

SC885 **Principles and Practical Implementation of Double Patterning** (Dusa) Sunday, 8:30 am to 12:30 pm

SC103 **Chemically Amplified Resists** (Willson) Thursday, 8:30 am to 5:30 pm

SC616 **Practical Photoresist Processing** (Dammel) Thursday, 1:30 to 5:30 pm

SC831 **Introduction to Scatterometry Metrology: Theory and Application** (Barry, Bao) Sunday, 1:30 to 5:30 pm

SC886 **Line Edge Roughness** (Gallatin) Sunday, 1:30 to 5:30 pm

SC101 **Introduction to Microlithography: Theory, Materials, and Processing** (Willson, Thompson, Bowden) Sunday, 8:30 am to 5:30 pm

SC105 **CD Metrology and Image Formation in the Scanning Electron Microscope (SEM)** (Postek, Wells) Sunday, 8:30 am to 5:30 pm

SC579 **Photomask Fabrication and Technology Basics** (Duff) Sunday, 8:30 am to 5:30 pm

WS619 **Intellectual Assets for Micro/Nano Electronics and Lithography** (Cole) Monday, 1:30 to 5:30 pm

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Optical Microlithography XXI

Conference Chair: **Harry J. Levinson**, Advanced Micro Devices, Inc.

Conference Co-Chair: **Mircea V. Dusa**, ASML US, Inc.

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Tuesday 26 February

SESSION 3

Conv. Ctr. A2 Tues. 8:00 to 8:10 am

Introduction

Session Chair: **Harry J. Levinson**, Advanced Micro Devices, Inc

SESSION 1

Conv. Ctr. A2 Tues. 8:10 to 10:00 am

Keynote Session

Session Chairs: **Harry J. Levinson**, Advanced Micro Devices, Inc.; **Mircea V. Dusa**, ASML

8:10 am: **If it moves, simulate it (Keynote Presentation)**, Andrew R. Neureuther, Univ. of California/Berkeley [6924-01]

8:40 am: **Interactions of double-patterning technology with OPC, wafer processing, and design flows (Keynote Presentation)**, Kevin D. Lucas, Synopsys, Inc. [6924-02]

9:10 am: **Toward 3-nm overlay: an integrated error budget for double-patterning lithography (Keynote Presentation)**, William H. Arnold, ASML US, Inc. [6924-03]

9:40 am: **The future of EUVL**, Winfried M. Kaiser, Manfred Dahl, Carl Zeiss SMT AG (Germany); Udo Dinger, Carl Zeiss Laser Optics GmbH (Germany); Frank Eisert, Peter Kuerz, Martin Lowisch, Hans-Juergen Mann, Stefan Muellender, Carl Zeiss SMT AG (Germany); William H. Arnold, ASML US, Inc.; Jos Benschop, ASML Netherlands B.V. (Netherlands); Steven G. Hansen, ASML US, Inc.; Koen van Ingen-Schenau, ASML Netherlands B.V. (Netherlands) [6924-04]

Coffee Break. 10:00 to 10:30 am

SESSION 2

Conv. Ctr. A2 Tues. 10:30 to 11:50 am

Double Masking I

Session Chairs: **SukJoo Lee**, SAMSUNG Electronics Co., Ltd. (South Korea); **Willard E. Conley**, Freescale Semiconductor, Inc.

10:30 am: **A study of CD budget in spacer patterning process**, Hidefumi Mukai, Eishi Shiobara, Shinya Takahashi, Toshiba Semiconductor Co. (Japan); Kohji Hashimoto, Toshiba Corp. (Japan) [6924-05]

10:50 am: **Single-etch double-patterning process for sub-40-nm 1/2 pitch imaging**, Willard E. Conley, Freescale Semiconductor, Inc.; Mark Slezak, Jeff Smith, Koichi Fujiwara, JSR Micro, Inc.; Richard Johnson, IBM Corp.; Michael Crouse, Robert Routh, Robert Socha, Mircea Dusa, ASML US, Inc. . . [6924-06]

11:10 am: **Double patterning for 32-nm and below: an update**, Jo M. Finders, ASML Netherlands B.V. (Netherlands); Mircea Dusa, ASML US, Inc.; Bert Vleeming, ASML Netherlands B.V. (Netherlands); Mireille Maenhoudt, Shaanee Cheng, IMEC (Belgium); Robert Routh, ASML US, Inc. [6924-07]

11:30 am: **Split and design guidelines for double patterning**, Vincent Wiaux, Staf Verhaegen, Shaanee Cheng, Mireille Maenhoudt, IMEC (Belgium); Takashi Matsuda, IMEC (Japan); Sergei Postnikov, Infineon Technologies AG (Germany); Geert Vandenberghe, IMEC (Belgium) [6924-08]

Lunch/Exhibition Break 11:50 am to 1:20 pm

Conv. Ctr. A2 Tues. 1:20 to 2:40 pm

Double Masking II

Session Chairs: **Koichi Matsumoto**, Nikon Corp. (Japan); **Geert Vandenberghe**, IMEC (Belgium)

1:20 pm: **Double patterning combined with shrink techniques to extend ArF lithography for contact holes to 22-nm node and beyond**, Xiangqun J. Miao, Xumou Xu, Christopher Bencher, Hyungje Woo, Hao Chen, Applied Materials, Inc.; Lior Huli, Albany NanoTech; Liyan Miao, Jen Su, Chris Ngai, Applied Materials, Inc.; Warren M. Montgomery, Albany NanoTech [6924-09]

1:40 pm: **Negative and iterated spacer lithography processes for low variability and ultra-dense integration**, Andrew E. Carlson, Tsu-Jae King Liu, Univ. of California/Berkeley [6924-10]

2:00 pm: **Double patterning of contact array with carbon polymer**, Woo Yung Jung, Hynix Semiconductor Inc. (South Korea) [6924-11]

2:20 pm: **PDL™ oxide enabled pitch doubling**, Nader Shamma, Novellus Systems, Inc.; Wen-Ben Chou, Lam Research Corp.; Ilia Kalinovski, Don Schlosser, Tom Mountsier, Wai-fan Yau, Julian Hsieh, Collin Mui, Raihan Tarafdar, Bart van Schravendijk, Novellus Systems, Inc. [6924-12]

Coffee Break. 2:40 to 3:20 pm

SESSION 4

Conv. Ctr. A2 Tues. 3:20 to 4:40 pm

Low-k1 Lithography I

Session Chairs: **Tatsuhiko Higashiki**, Toshiba Corp. (Japan); **Kafai Lai**, IBM Microelectronics Div.

3:20 pm: **Pixelated phase mask as novel lithography RET**, Yan A. Borodovsky, Wen-Hao Cheng, Paul Davids, Richard E. Schenker, Vivek Singh, Intel Corp. [6924-13]

3:40 pm: **Mask optimization for arbitrary patterns with 2D-TCC resolution enhancement technique**, Yoshiyuki Sekine, Miyoko Kawashima, Kenji Yamazoe, Manabu Hakko, Masakatsu Ohta, Tokuyuki Honda, Canon Inc. (Japan) [6924-14]

4:00 pm: **Special treatments on subresolution assist features in photolithography process simulation**, Jian-Liang Li, Lawrence Melvin III, Synopsys, Inc. [6924-15]

4:20 pm: **Comparative study of binary intensity mask and attenuated phase-shift mask using hyper-NA immersion lithography for sub-45-nm era**, Tae-Seung Eom, Jun-Taek Park, Sarohan Park, Sunyoung Koo, Jin-Soo Kim, Byoung-Hoon Lee, Chang-Moon Lim, Hyeong-Soo Kim, Seung-Chan Moon, Hynix Semiconductor Inc. (South Korea) [6924-16]

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Conv. Ctr. A2 Tues. 6:30 to 8:00 pm

Future Projection Lithography: Optical or EUV? Panel Discussion

Panel Moderators: **Bruno M. LaFontaine**, Advanced Micro Devices, Inc.; **Nigel R. Farrar**, Cymer, Inc.

Panelists: **Timothy A. Brunner**, IBM Thomas J. Watson Research Ctr.; **Willard E. Conley**, Freescale Semiconductor, Inc.; **Benjamin G. Eynon**, SEMATECH, Inc.; **Tatsuhiko Higashiki**, Toshiba Corp. (Japan); **Winfried M. Kaiser**, Carl Zeiss SMT AG (Germany); **Kurt G. Ronse**, IMEC (Belgium); **Anthony Yen**, Taiwan Semiconductor Manufacturing Co. Ltd. (Taiwan)

Joint Panel Discussion with conference 6924 and 6921.

As Moore's law drives IC dimensions ever smaller, it has been assumed that, at some node, some non-optical patterning technology would take the lead for IC manufacturing. Currently, EUV lithography is the top contender for that position. Yet, EUV has been delayed from its previous targets of 45nm and 32nm, while new advances in immersion lithography and various RETs have extended the life of conventional 193nm lithography generations beyond what was originally forecast.

This panel addresses the current forecast of requirements from both the memory and MPU perspectives for the 22nm node and beyond, and asks: can optical lithography, with all its tricks, have high enough yield? Can EUV, with all its problems, be ready in time? Will an alternative technology emerge and surprise us all? Or, will we all call it quits and give Moore's Law a rest?

Wednesday 27 February

SESSION 5

Conv. Ctr. A2 Wed. 8:00 to 10:00 am

Low-k1 Lithography II

Session Chairs: **Wilhelm Maurer**, Infineon Technologies AG (Germany); **Ken Ozawa**, Sony Atsugi Technology Ctr. (Japan)

8:00 am: **Integration of phase pixel masks for full-chip random logic layers**, Richard E. Schenker, Srinivas B. Bollepalli, Bin Hu, Kenny Toh, Vivek Singh, Karmen Yung, Wen-Hao Cheng, Yan A. Borodovsky, Intel Corp. [6924-17]

8:20 am: **Applications of TM polarized illumination and its use in frequency doubled imaging**, Bruce W. Smith, Jianming Zhou, Peng Xie, Rochester Institute of Technology. [6924-18]

8:40 am: **Enabling technology scaling with in production lithography processes**, Tejas K. Jhaveri, Carnegie Mellon Univ. [6924-19]

9:00 am: **Hyper-NA imaging of 45-nm node random contact hole layouts using inverse lithography**, Eric Hendrickx D.D.S., IMEC (Belgium); Won Kim, Texas Instruments Inc.; Geert Vandenbergh, IMEC (Belgium); Alexander V. Tritchkov, Kyoto Sakajiri, Yuri Granik, Mentor Graphics Corp. [6924-20]

9:20 am: **Patterning strategy and performance of 1.3NA tool for 32-nm node lithography**, Shoji Mimotogi, Masaki Satake, Yosuke Kitamura, Katsuyoshi Kodera, Hiroharu Fujise, Koutaro Sho, Tatsuhiko Ema, Kazutaka Ishigo, Takuya Kono, Masafumi Asano, Kenji Yoshida, Hideki Kanai, Suigen Kyo, Hideaki Harakawa, Akiko Nomachi, Tatsuya Ishida, Katsura Miyashita, Soichi Inoue, Toshiba Corp. (Japan) [6924-21]

9:40 am: **Advanced resolution-enhancement technique for 32-nm node contact hole layer using source mask optimization**, Byung-Sung Kim, Sung-Ho Lee, Hong-Jae Shin, Nae-In Lee, SAMSUNG Electronics Co., Ltd. (South Korea); Jung-Chul Park, Brion Technologies, Inc.; Jung-Bae Kim, ASML Korea Co., Ltd. (South Korea). [6924-22]

Coffee Break. 10:00 to 10:30 am

SESSION 6

Conv. Ctr. A2 Wed. 10:30 to 11:50 am

Double Masking III

Session Chairs: **Sam Sivakumar**, Intel Corp.; **Pary Baluswamy**, Micron Technology, Inc.

10:30 am: **Post-decomposition assessment of double-patterning layouts**, Juliet A. Rubinstein, Andrew R. Neureuther, Univ. of California/Berkeley[6924-23]

10:50 am: **Alternative process schemes for double patterning that eliminate the intermediate etch step**, Mireille Maenhoudt, Roel Gronheid, Nickolay Stepanenko, Takashi Matsuda, Diziana Vangoidsenhoven, IMEC (Belgium). [6924-24]

11:10 am: **Double patterning down to k1=0.15 with bilayer resist**, Christoph Noelscher, Franck Jauzion-Graverolle, Marcel Heller, Matthias Markert, Bee Kim Hong, Qimonda Dresden GmbH & Co. OHG (Germany) [6924-25]

11:30 am: **Double-patterning requirements for optical lithography and prospects for optical extension without double patterning**, Andrew J. Hazelton, Shigeru Hirukawa, Nikon Corp. (Japan); Martin McCallum, Nikon Precision Europe GmbH (Germany); Soichi Owa, Nobutaka Magome, Jun Ishikawa, Nikon Corp. (Japan); Celine Lapeyre, Isabelle Guilmeau, Lab. d'Electronique de Technologie de l'Information (France). [6924-26]

Lunch/Exhibition Break 11:50 am to 1:20 pm

SESSION 7

Conv. Ctr. A2 Wed. 1:20 to 3:00 pm

Simulation I

Session Chairs: **Kafai Lai**, IBM Microelectronics Div.; **Nigel R. Farrar**, Cymer, Inc.

1:20 pm: **Making a trillion pixels dance**, Vivek Singh, Bin Hu, Kenny Toh, Srinivas Bollepalli, Stephan Wagner, Yan Borodovsky, Intel Corp. [6924-27]

1:40 pm: **Validation of inverse lithography technology (ILT) and its adaptive SRAF at advanced technology node**, Linyong Pang, Grace Dai, Luminescent Technologies, Inc. [6924-28]

2:00 pm: **General imaging of advanced 3D mask objects based on the fully vectorial extended Nijboer-Zernike (ENZ) theory**, Sven van Haver, Olaf T. A.Janssen, Joseph J. M.Braat, Technische Univ. Delft (Netherlands); Augustus J. E. M.Janssen, Philips Research Eindhoven (Netherlands); Paul H. Urbach, Philips Research Europe (Netherlands) and Technische Univ. Delft (Netherlands); Silvania F. Pereira, Technische Univ. Delft (Netherlands) [6924-29]

2:20 pm: **Radiometric consistency in source specifications for lithography**, Alan E. Rosenbluth, IBM Thomas J. Watson Research Ctr.; Jaione Tirapu-Azpiroz, Kafai Lai, IBM Microelectronics Div.; Michael Totzeck, Vladan Blahnik, Carl Zeiss SMT AG (Germany); Donis Flagello, ASML US, Inc.; Armand Koolen, ASML Netherlands B.V. (Netherlands) [6924-30]

2:40 pm: **The throughput and accuracy of a coupled-dipole model for 3D mask simulations**, Vlad Temchenko, Chinteong Lim, David Wallis, Infineon Technologies AG (Germany). [6924-31]

Coffee Break. 3:00 to 3:30 pm

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SESSION 8

Conv. Ctr. A2 **Wed. 3:30 to 5:10 pm**

Simulation II

Session Chairs: **Akiyoshi Suzuki**, Canon Inc. (Japan); **Yao-Ching Ku**, Taiwan Semiconductor Manufacturing Co., Ltd. (Taiwan)

3:30 pm: **Generalized inverse problem for partially coherent projection lithography**, Paul Davids, Srinivas B. Bollepalli, Intel Corp. [6924-32]

3:50 pm: **Massively parallel finite-difference time-domain simulations to address mask electromagnetic effects in hyper-NA immersion lithography**, Jaione Tirapu-Azpiroz, IBM Microelectronics Div.; Geoffrey W. Burr, IBM Almaden Research Ctr.; Alan E. Rosenbluth, IBM Thomas J. Watson Research Ctr.; Michael S. Hibbs, IBM Microelectronics Div. [6924-33]

4:10 pm: **Polarization characteristics of state-of-art lithography optics reconstructed from on-body measurement**, Toru Fujii, Jun Kogo, Yasushi Mizuno, Akinori Suda, Masayasu Sawada, Nikon Corp. (Japan) [6924-34]

4:30 pm: **Extended Nijboer-Zernike (ENZ)-based mask imaging: efficient coupling of electromagnetic field solvers and the ENZ imaging algorithm**, Olaf T. A.Janssen, Sven van Haver, Technische Univ. Delft (Netherlands); Augustus J. E. M.Janssen, Philips Research Eindhoven (Netherlands); Joseph J. M.Braat, Technische Univ. Delft (Netherlands); Paul H. P.Urbach, Philips Research Eindhoven (Netherlands) and Technische Univ. Delft (Netherlands); Sylvania F. Pereira, Technische Univ. Delft (Netherlands) [6924-35]

4:50 pm: **Evaluating the accuracy of a calibrated full-physical resist model**, Stewart A. Robertson, KLA-Tencor Corp.; Byung-Sung Kim, Woon-Hyuk Choi, Yoo-Hyon Kim, SAMSUNG Electronics Co., Ltd. (South Korea); John Biafore, Mark D. Smith, KLA-Tencor Corp. [6924-36]

Thursday 28 February

SESSION 9

Conv. Ctr. A2 **Thurs. 8:00 to 10:00 am**

High Index Immersion Lithography

Session Chairs: **Willard E. Conley**, Freescale Semiconductor, Inc.; **Sam Sivakumar**, Intel Corp.

8:00 am: **Novel high-refractive index materials design for the next-generation ArF immersion lithography**, Taiichi Furukawa, Takanori Kishida, Kyouyuu Yasuda, Tsutomu Shimokawa, JSR Corp. (Japan); Zhi Liu, Mark Slezak, JSR Micro, Inc.; Katsuhiko Hieda, JSR Corp. (Japan) [6924-37]

8:20 am: **Studies of high-index immersion lithography**, Yasuhiro Ohmura, Hiroyuki Nagasaka, Tomoyuki Matsuyama, Toshiharu Nakashima, Teruki Kobayashi, Motoi Ueda, Soichi Owa, Nikon Corp. (Japan) [6924-38]

8:40 am: **High-index lens material LuAG: development status and prospect**, Lutz Parthier, Gunther Wehrhan, Dietmar Keutel, Markus Ansorg, Tilo Aichele, Christoph Seitz, SCHOTT Lithotec AG (Germany) [6924-39]

9:00 am: **High-n immersion lithography**, Harry Sewell, ASML US, Inc.; Jan Mulken, ASML Netherlands B.V. (Netherlands); Paul Graeupner, Carl Zeiss SMT AG (Germany); Sjoerd Donders, ASML Netherlands B.V. (Netherlands); Diane McCafferty, Louis Markoya, Nandarisi Samarakone, ASML US, Inc. [6924-40]

9:20 am: **Combating lens photocontamination during high-index fluid exposure in immersion lithography**, Vladimir Liberman, Mordechai Rothschild, Steven T. Palmacci, MIT Lincoln Lab.; Paul Zimmerman, SEMATECH, Inc. [6924-41]

9:40 am: **High-index immersion fluids enabling cost-effective single-exposure lithography for 32-nm half pitches**, Roger H. French, Hoang V. Tran, Doug J. Adelman, Weiming Qiu, Jerald Feldman, Robert C. Wheland, DuPont Co.; Mureo Kaku, DuPont Co. (Japan); Nyriisa S. Rogado, DuPont Co.; Charles Y. Chen, DuPont Electronic Technologies [6924-42]

Coffee Break 10:00 to 10:30 am

SESSION 10

Conv. Ctr. A2 **Thurs. 10:30 to 11:50 am**

Process I

Session Chairs: **Nigel R. Farrar**, Cymer, Inc.; **Wilhelm Maurer**, Infineon Technologies AG (Germany)

10:30 am: **Immersion defectivity study with volume-production immersion lithography tool for 45-nm node and below**, Katsushi Nakano, Hiroshi Kato, Masato Yoshida, Yasuhiro Iriuchijima, Tomoharu Fujiwara, Kenichi Shiraiishi, Soichi Owa, Nikon Corp. (Japan) [6924-43]

10:50 am: **Focus, dynamics, and defectivity performance at wafer edge in immersion lithography**, Takao Tamura, Naka Onoda, Masafumi Fujita, Takayuki Uchiyama, NEC Electronics Corp. (Japan) [6924-44]

11:10 am: **The rapid introduction of immersion lithography for NAND flash: challenges and experience**, Hung-Ming Lin, Benjamin S. Lin, Chan-Tsun Wu, Wei-Ming Wu, Meng-Hsun Chan, Powerchip Semiconductor Corp. (Taiwan); Toshio Ohhashi, Katsushi Nakano, Yasuhiro Iriuchijima, Andrew J. Hazelton, Nikon Corp. (Japan) [6924-45]

11:30 am: **Immersion defect performance and particle control method for 45-nm mass production**, Takahito Chibana, Masamichi Kobayashi, Hitoshi Nakano, Mikio Arakawa, Yoichi Matsuoka, Youji Kawasaki, Canon Inc. (Japan); Masayuki Tanabe, Extreme Ultraviolet Lithography System Development Association (Japan); Hirohisa Oda, Canon Inc. (Japan) [6924-46]

Lunch Break 11:50 am to 1:20 pm

SESSION 11

Conv. Ctr. A2 **Thurs. 1:20 to 3:20 pm**

OPC and Mask Technology

Session Chairs: **Yao-Ching Ku**, Taiwan Semiconductor Manufacturing Co., Ltd. (Taiwan); **Bruce W. Smith**, Rochester Institute of Technology

1:20 pm: **Development of a computational lithography roadmap**, Jang-Fung Chen, ASML MaskTools Inc.; Hua-Yu Liu, Brion Technologies, Inc.; Thomas Laidig, ASML MaskTools Inc.; Yu Cao, Brion Technologies, Inc.; Christian Zuniga, ASML MaskTools Inc.; Robert Socha, ASML [6924-47]

1:40 pm: **Analysis of OPC optical model accuracy with detailed scanner signature information**, Kevin D. Lucas, Qiaolin Zhang, Hua Song, Satyendra Sethi, Synopsys, Inc.; Jacek Tyminski, Nikon Precision Inc. [6924-48]

2:00 pm: **Hybrid Hopkins-Abbe method for modeling oblique angle mask effects in OPC**, Konstantinos Adam, Michael Lam, Mentor Graphics Corp. [6924-49]

2:20 pm: **Robust PPC and DfM methodology for exposure tool variations**, Toshiya Kotani, Hiromitsu Mashita, Fumiharu Nakajima, Satoshi Tanaka, Kazuya Sato, Soichi Inoue, Toshiba Semiconductor Co. (Japan) [6924-50]

2:40 pm: **Fabrication of defect-free full-field pixelated phase mask**, Jeff Farnsworth, Wen-Hao Cheng, Intel Corp. [6924-51]

3:00 pm: **Advanced OPC and 2D verification for tip engineering using aggressive illuminations**, Xima Zhang, Spansion Inc. [6924-52]

Coffee Break 3:20 to 3:50 pm

SESSION 12

Conv. Ctr. A2 Thurs. 3:50 to 5:30 pm

Process II

Session Chairs: Roger H. French, DuPont Co.; Pary Baluswamy, Micron Technology, Inc.

3:50 pm: **Optimization procedure of exposure tools with polarization aberrations**, Tadashi Arai, Kenichiro Mori, Akihiro Yamada, Yoshinori Ohsaki, Yasuo Hasegawa, Toshiyuki Yoshihara, Canon Inc. (Japan) [6924-53]

4:10 pm: **Proposal for determining exposure latitude requirements**, Harry J. Levinson, Yuansheng Ma, Bruno LaFontaine, Advanced Micro Devices, Inc.; Rolf Seltmann, AMD Saxony LLC & Co. KG (Germany); Mircea Dusa, ASML US, Inc. [6924-54]

4:30 pm: **The influence of shot noise on the LER and CDU with DUV, EUV, and electron beam**, Zhih-Yu Pan, Chun-Kuang Chen, Tsai-Sheng Gau, Burn J. Lin, Taiwan Semiconductor Manufacturing Co. Ltd. (Taiwan) [6924-55]

4:50 pm: **Determining DOF and exposure latitude requirements needed to meet technology process assumptions**, Allen H. Gabor, IBM Microelectronics Div.; Bernhard Liegl, IBM Corp.; Colin Brodsky, IBM Microelectronics Div.; Gerhard Lembach, Advanced Micro Devices, Inc.; Scott Mansfield, IBM Microelectronics Div.; Shailendra Mishra, IBM Corp.; Timothy Brunner, IBM Thomas J. Watson Research Ctr.; Timothy Wiltshire, IBM Microelectronics Div.; Vinayan Menon, Wai-Kin Li, IBM Corp. [6924-56]

5:10 pm: **Application of scatterometry techniques for the measurements of sub-40-nm line patterns and 3D OPC structures**, Oleg Kritsun, Bruno M. LaFontaine, Advanced Micro Devices, Inc.; Chandra S. Saravanan, Nanometrics Inc. [6924-57]

Conv. Ctr. Hall 3 Thurs. 6:00 to 8:00 pm

Posters-Thursdays

The following posters will be displayed all day Thursday. Authors will be present during the formal poster session Thursday evening between 6:00 and 8:00 pm for discussion. Authors may set-up their posters after 9:00 am on Thursday.

Double Masking

A comprehensive comparison between double patterning and double patterning with spacer on sub-50-nm product implementation, Chi Feng Tseng, Chin Cheng Yang, Tien Chu Yang, Ta Hone Yang, Kuang-Chao Chen, Chih-Yuan Lu, Macronix International Co., Ltd. (Taiwan) [6924-69]

100-nm half-pitch double-exposure KrF lithography using binary masks, Sebastian Geisler, Joachim J. Bauer, Ulrich Haak, IHP Microelectronics (Germany); David Stolarek, Consultant (Germany); Katrin Schulz, IHP Microelectronics (Germany); Herman Wolf, Photonics MZD GmbH (Germany); Winfried W. Meier, Nikon Precision Europe GmbH (Germany); Manfred Trojahn, Rohm and Haas Electronic Materials (Germany); Egbert Matthus, IHP Microelectronics (Germany) [6924-70]

Double patterning using dual spin-on Si containing layers with multilayer hard mask process, Mamoru Terai, Teruhiko Kumada, Mitsubishi Electric Corp. (Japan); Takeo Ishibashi, Takuya Hagiwara, Masaaki Shinohara, Kazumasa Yonekura, Takahiro Maruyama, Tetsuro Hanawa, Renesas Technology Corp. (Japan) [6924-71]

45-nm and 32-nm half-pitch patterning with 193-nm dry lithography and double patterning, Huixiong Dai, Christopher Bencher, Yong-Mei Chen, Applied Materials, Inc. [6924-72]

Issues and challenges of double-patterning technology and its corresponding OPC, Yijie Pan, Zhejiang Univ. (China) [6924-73]

Study of poly extension splitting techniques to random logic LSI toward 32-nm node, Yuji Setta, Kazumasa Morishita, Katsuyoshi Kobayashi, Tatsuo Chijimatsu, Satoru Asai, Fujitsu Ltd. (Japan) [6924-74]

Double patterning in lithography for 65-nm node with oxidation process, Eunsoo Jeong, Dongbu Electronics Co., Ltd. (South Korea) [6924-75]

Precise CD control techniques for double patterning and sidewall transfer, Eiichi Nishimura, Masato Kushibiki, Koichi Yatsuda, Tokyo Electron Ltd. (Japan) [6924-76]

Fabrication of contact/via holes for 32-nm technology device using cost-effective RIE CD shrink process and double-patterning technique, Masato Kushibiki, Eiichi Nishimura, Koichi Yatsuda, Tokyo Electron Ltd. (Japan) [6924-77]

Monte Carlo simulation of critical dimension distribution after double patterning, Yuansheng Ma, Advanced Micro Devices, Inc.; Lovejeet Singh, Frank Tsai, Spansion Inc.; Harry Levinson, Advanced Micro Devices, Inc.; Anna Minvielle, Spansion Inc. [6924-78]

Double-patterning overlay and CD budget for 32-nm technology node, Umberto Iessi, STMicroelectronics (Italy) [6924-79]

Double-exposure double-etch for dense SRAM: a designer's dream, Chandrasekhar Sarma, Infineon Technologies North America; Allen H. Gabor, Scott D. Halle, IBM Microelectronics Div.; Klaus Herold, Paul Schroeder, Infineon Technologies North America; Len Y. Tsou, Helen Wang, IBM Microelectronics Div.; Haoren Zhuang, Infineon Technologies North America [6924-80]

An analysis of double-exposure lithography options, Saul Lee, The Univ. of Texas at Austin; Jeffrey Byers, SEMATECH, Inc.; Kane Jen, The Univ. of Texas at Austin; Paul Zimmerman, Bryan Rice, SEMATECH, Inc.; Nicholas J. Turro, Columbia Univ.; Grant Willson, The Univ. of Texas at Austin [6924-81]

Double printing through the use of ion implantation, Nandasiri Samarakone, ASML US, Inc.; Mary Zawadzki, Silicon Valley Toxics Coalition [6924-82]

30-nm half-pitch metal patterning using Motif(tm) CD shrink technique and double patterning, Janko Versluis, Jean-Francois de Marneffe, Danny Goossens, Maaik Op de Beeck, Tom Vandeweyer, Vincent Wiaux, Herbert Struyf, Mireille Maenhoudt, Mohand Brouri, Johan Vertommen, IMEC (Belgium); Helen Zhu, Reza Sadjadi, Lam Research Corp. [6924-83]

Enabling 30-nm double-patterning contact imaging using a novel hole shrink process, Yoshiaki Yamada, Tokyo Electron Kyushu Ltd. (Japan); Michael M. Crouse, ASML US, Inc.; Shannon Dunn, TEL Technology Ctr., America, LLC; Tetsu Kawasaki, Satoru Shimura, Eiichi Nishimura, Yoshitsugu Tanaka, Tokyo Electron Ltd. (Japan); Judy Galloway, Bill Pierson, Robert Routh, ASML US, Inc. [6924-84]

Process window characterization and photoresist characterization method in double-exposure photolithography, Qiang Wu, Jun Zhu, Shanghai Hua Hong NEC Electronics Co., Ltd. (China) [6924-85]

High Index Immersion Lithography

Prediction of imaging performance of immersion lithography using high-diffraction index fluid, Takashi Sato, Toshiba Corp. (Japan); Masamitsu Itoh, Akiko Mimotogi, Toshiba Semiconductor Co. (Japan); Shoji Mimotogi, Toshiba Corp. (Japan); Kazuya Sato, Satoshi Tanaka, Toshiba Semiconductor Co. (Japan) [6924-86]

Contrast management on a 193i interferometer to match scanners conditions, Alexandre Lagrange, Philippe Bandelier, Christelle Charpin, Olivier Lartigue, Lab. d'Electronique de Technologie de l'Information (France) [6924-88]

Immersion exposure system using high-index materials, Keita Sakai, Yuichi Iwasaki, Sunao Mori, Keiji Yamashita, Makoto Ogusu, Keiji Emoto, Tomofumi Nishikawara, Shinichi Hara, Yutaka Watanabe, Canon Inc. (Japan) [6924-89]

Continuing 193-nm optical lithography for 32-nm imaging and beyond, Emil C. Piscani, Dominic Ashworth, Jeff Byers, Chris Van Peski, SEMATECH, Inc.; Paul Zimmerman, SEMATECH, Inc. and Intel Corp. [6924-90]

Lithography Tools

Novel refractive optics enable multipole off-axis illumination, Tanja Bizjak, Thomas Mitra, Lutz Aschke, LIMO-Lissotschenko Mikroskopik GmbH (Germany) [6924-91]

45-nm logic device OPE matching between exposure tools through laser bandwidth tuning, Kazuyuki Yoshimochi, Takao Tamura, Seiji Nagahara, Takayuki Uchiyama, NEC Electronics Corp. (Japan); James Bonafede, Cymer Japan, Inc. [6924-92]

Fluoride single crystals for the next-generation lithography, Teruhiko Nawata, Youji Inui, Naoto Mochizuki, Isao Masada, Eiichi Nishijima, Hiroki Sato, Tokuyama Corp. (Japan); Tsuguo Fukuda, Tohoku Univ. (Japan) [6924-93]

Lithography tool with open-space architecture, Yuuki Ishii, Katsuaki Ishimaru, Nikon Corp. (Japan) [6924-95]

2-nm overlay control system of electronic parallel datum, Xiang-Wen Xiong, Zhongheng High-Tech Inc. (China) [6924-96]

An improved process for manufacturing diffractive optical elements (DOEs) for off-axis illumination systems, Jerry L. Leonard, James Carriere, Rich Jones, Marc Himel, Jared Stack, John Childers, Tessera North America; David Vellenga, Triangle National Lithography Ctr. [6924-97]

A novel photo-thermal setup for determination of absorbance losses and waferfront deformations in DUV optics, Klaus Mann, Uwe Leinhos, Torsten Miede, Bernd Schäfer, Laser-Lab. Göttingen e.V. (Germany) [6924-98]

Performance demonstration of significant availability improvement in lithography light sources using advanced gas management, Wayne J. Dunstan, Kevin O'Brien, Daniel Riggs, Aravind Ratnam, Herve Besaucele, Daniel Brown, Robert Jacques, Cymer, Inc. [6924-100]

Reliable high-power injection locked 6kHz 60W laser for ArF immersion lithography, Takahito Kumazaki, Ryoichi Nohdomi, Hiroaki Nakarai, Takashi Matsunaga, Kouji Kakizaki, Junichi Fujimoto, Hakaru Mizoguchi, Gigaphoton Inc. (Japan) [6924-198]

High-power and high-energy stability injection lock laser light source for double exposure or double patterning ArF immersion lithography, Masaya Yoshino, Hiroaki Nakarai, Takashi Matsunaga, Junichi Fujimoto, Ryoichi Nohdomi, Kouji Kakizaki, Taku Yamazaki, Hakaru Mizoguchi, Gigaphoton Inc. (Japan) [6924-199]

Uniaxial crystal last optical element for second- and third-generation immersion lithography, Gabriel Y. Sirat, Crystalith (Israel); Michael Goldstein, SEMATECH, Inc. and Intel Corp. [6924-201]

Low-k1 Lithography

Impact of optimization conditions on the result at optimizing illumination and mask, Koichiro Tsujita, Koji Mikami, Hiroyuki Ishii, Akiyoshi Suzuki, Canon Inc. (Japan) [6924-101]

Understanding and application of constructive, destructive SRAF, Fook L. Chin, Spansion Inc. [6924-102]

90-nm node contact-hole patterning through applying model-based OPC in KrF lithography, Young-Doo Jeon, Sang-Uk Lee, Jeahee Kim, Keeho Kim, Dongbu Electronics Co., Ltd. (South Korea) [6924-103]

Manufacturing implementation of 32-nm SRAM, Shoshen Lee, United Microelectronics Corp. (Taiwan). [6924-105]

Random 65-nm/45-nm contact hole printing using optimized illumination source and CD sizing by post processing, Jo M. Finders, Gert-Jan Janssen, ASML Netherlands B.V. (Netherlands); Tsuyoshi Shibata, Ryouichirou Naitou, Tokyo Electron Kyushu Ltd. (Japan) [6924-106]

Study of SRAF placement for contact at 45-nm and 32-nm node, Vincent Farys, STMicroelectronics (France) [6924-107]

Automated method of detecting SRAF and sidelobe printing with automated CD-SEM recipes, Mary E. Coles, Yong Choi, Texas Instruments Inc. [6924-109]

Novel lithography rule check for full-chip side-lobe detection, Tzong-Shane Wu, Elvis Yang, Ta Hone Yang, Kuang-Chao Chen, Chih-Yuan Lu, Macronix International Co., Ltd. (Taiwan) [6924-110]

Quasi-iso-focal hole pattern formation by Checker-Board PSM (CB-PSM), Shuji Nakao, Shinroku Maejima, Ayumi Minamide, Hirokazu Saitoh, Tetsuro hanawa, Kazuyuki Suko, Renesas Technology Corp. (Japan) [6924-111]

Optimum biasing for 45-nm node chromeless and attenuated phase-shift mask, Hye Keun Oh, Young-Min Kang, Seung-Wook Park, Hanyang Univ. (South Korea) [6924-112]

Improvement of the common DOF across field for hole structure process layers, Shu H. Hou, Aroma Tseng, Janus Pan, Edgar Huang, Bill Lin, Chun-Chi Yu, United Microelectronics Corp. (Taiwan); Eason Lin, ASML Taiwan Ltd. (Taiwan) [6924-113]

Customized illumination shapes for 193-nm immersion lithography, Moh-Lung Ling, National Univ. of Singapore (Singapore); Gek-Soon Chua, Chartered Semiconductor Manufacturing Ltd. (Singapore); Cho-Jui Tay, Chenggen Quan, National Univ. of Singapore (Singapore); Qunying Lin, Chartered Semiconductor Manufacturing Ltd. (Singapore) [6924-114]

Binary and attenuated PSM mask evaluation for sub-50-nm device development perspective, James Moon, Byoung-Sub Nam, Joo-Hong Jeong, Dong-Ho Kong, Byung-Ho Nam, Dong-Gyu Yim, Hynix Semiconductor Inc. (South Korea) [6924-115]

Highly reliable detection and correction of pinched areas for high-transmission phase-shift mask, Julius C. Chen, Nanya Technology Corp. (Taiwan) [6924-116]

Evaluation of inverse lithography technology for 55-nm node memory device, Byung-Ug Cho, Hye-jin Shin, Jae-seung Choi, Cheol-Kyun Kim, Hyun-Jo Yang, Dong-Gyu Yim, Hynix Semiconductor Inc. (South Korea) [6924-117]

Extension of low-k1 lithography processes with KrF for 90-nm technology node, Sung-Ho Jun, Eunsoo Jeong, Young-Je Yun, Kwangseon Choi, Jeahee Kim, Keeho Kim, Dongbu Electronics Co., Ltd. (South Korea) [6924-118]

60-nm half-pitch contact layer printing: exploring the limits at 1.35NA lithography, Joost P. M. Bekaert, Eric Hendrickx, Geert Vandenbergh, IMEC (Belgium) [6924-119]

Combined mask and illumination scheme optimization for robust contact patterning on 45-nm technology node flash memory devices, Alessandro Vaglio-Pret, STMicroelectronics (Italy) and Univ. di Milano (Italy); Gianfranco Capetti, Pietro Cantu, Danilo De Simone, Alessandro Vaccaro, Laura Soma, STMicroelectronics (Italy) [6924-120]

32-nm logic patterning options with immersion lithography, Kafai Lai, Larry Zhuang, IBM Microelectronics Div.; Cyrus E. Tabery, Advanced Micro Devices, Inc.; Henning Haffner, Infineon Technologies AG; Jason E. Meiring, Derron Dunn, Scott M. Mansfield, Zachary Baum, IBM Microelectronics Div.; Yi Zou, Carl P. Babcock, Vito Dai, Advanced Micro Devices, Inc.; Dario Gil, IBM Thomas J. Watson Research Ctr.; Scott D. Halle, IBM Microelectronics Div.; Sean D. Burns, IBM Thomas J. Watson Research Ctr.; B. Morgenfeld, IBM Microelectronics Div.; Martin Burkhardt, IBM Corp.; Margaret C. Lawson, IBM Microelectronics Div.; Matthew Colburn, IBM Thomas J. Watson Research Ctr.; Wendy Yan, Len Y. Tsou, IBM Microelectronics Div.; Haoren Zhuang, Infineon Technologies North America; E. Geiss, Advanced Micro Devices, Inc.; Scott D. Allen, IBM Microelectronics Div.; David R. Medeiros, IBM Thomas J. Watson Research Ctr. [6924-200]

OPC and Mask Technology

Consideration of VT5 etch-based OPC modeling implementation in mass production environment, Chin-Teong Lim, Vlad Temchenko, Infineon Technologies AG (Germany) [6924-121]

Optimized OPC approach for process window improvement, Ching-Heng Wang, Qingwei Liu, Semiconductor Manufacturing International Corp. (China); Liguozhang, Mentor Graphics Corp. (China) [6924-122]

Impact of photomask quadrature edge effects through focus, Marshal A. Miller, Andrew Neureuther, Daniel Ceperley, Koji Kikuchi, Univ. of California/Berkeley [6924-123]

The comparison of OPC performance and run time for dense versus sparse solutions, Amr Y. Abdo, Jason Meiring, Ryan Burns, Ramya Viswanathan, Geng Han, James Oberschmidt, Scott Mansfield, Ian Stobert, IBM Microelectronics Div.; Donald Samuels, IBM Corp.; Zengqin Zhao, IBM Microelectronics Div.; Chidam Kallingal, Yi Zou, Advanced Micro Devices, Inc.; Oseo Park, Klaus Herold, Infineon Technologies North America [6924-124]

Advanced mask process modeling, correction, and verification for 45-nm and 32-nm nodes, Gokhan Percin, Emile Sahouria, Yuri Granik, Yuanfang Hu, Steffen Schulze, Pradiptya Ghosh, Mentor Graphics Corp. [6924-125]

An efficient and robust mask model for lithography simulation, Zhenhai Zhu, Cadence Design Systems, Inc.; Frank Schmidt, Zuse Institute Berlin (Germany) [6924-126]

Reticle CD error calibrated OPC model generation, Youngmi Kim, Sang-Uk Lee, Jong-Doo Kim, Eui-Sang Park, Jeahee Kim, Keeho Kim, Dongbu Electronics Co., Ltd. (South Korea) [6924-127]

Modeling of focus blur in the context of optical proximity correction, Qiaolin Zhang, Hua Song, Kevin Lucas, James Shiely, Synopsys, Inc. [6924-129]

Full-chip compensation for local flare effects using OPC/DRC method, Jae Young Choi, Jong-Doo Kim, Jeahee Kim, Keeho Kim, Dongbu Electronics Co., Ltd. (South Korea) [6924-130]

Development of layout split algorithms and printability evaluation for double-patterning technology, Tsann-Bim Chiou, ASML Taiwan Ltd. (Taiwan); Robert Socha, ASML; Hong Chen, Luoqi Chen, Stephen Hsu, Brion Technologies, Inc.; Peter Nikolsky, Anton van Oosten, ASML Netherlands B.V. (Netherlands); Alek Chen, ASML Taiwan Ltd. (Taiwan) [6924-131]

Optical proximity correction with regression, Allan X. Gu, Peiran Gao, Avideh Zakhor, Univ. of California/Berkeley [6924-133]

OPC optimization and practical application of double-dipole lithography for 45-nm node with dry exposure, Se-Jin Park, Dongbu Electronics Co., Ltd. (China); Jae-Kyung Seo, Cheng-He Li, Daisy Liu, Petros An, Semiconductor Manufacturing International Corp. (China); Xiao-hui Kang, Mentor Graphics Corp. (China); Eric Guo, Semiconductor Manufacturing International Corp. (China) [6924-135]

Novel method for optimizing lithography exposure conditions using full-chip post-OPC simulation, John L. Sturtevant, Travis Brist, Le Hong, Alexandr Drozdov, Mentor Graphics Corp. [6924-136]

Optical proximity correction for elongated contact-hole printing, Young-Chang Kim, Sangwook Kim, Sungsoo Suh, Yong-Jin Cheon, SukJoo Lee, Junghyeon Lee, Chang-Jin Kang, Joo-Tae Moon, SAMSUNG Electronics Co., Ltd. (South Korea); Sooryong Lee, Synopsys Korea Inc. (South Korea)[6924-138]

Study of the mask topography effect on the OPC modeling accuracy of hole patterns, Seongbo Shim, YoungChang Kim, SukJoo Lee, Junghyeon Lee, Changjin Kang, SAMSUNG Electronics Co., Ltd. (South Korea) [6924-139]

Evaluation of OPC test patterns using parameter sensitivity, Brian Ward, IMEC (Netherlands); Kevin Lucas, Synopsys, Inc. [6924-140]

Pellicle effect on OPC modeling, Boren Luo, Taiwan Semiconductor Manufacturing Co. Ltd. (Taiwan) [6924-142]

OPC model calibration considerations for data variance, Mohamed S. Bahnas, Mohamed Al-Imam, Mentor Graphics Corp. (Egypt); George E. Bailey, Mentor Graphics Corp. [6924-144]

Pattern centric OPC flow: a special RET flow with dramatic turn-around time, Ching-Heng Wang, Benny Wang, Qingwei Liu, Semiconductor Manufacturing International Corp. (China); Changsheng Ying, Guojie Chen, Gary Zhang, Joanne J. Wu, Bo Su, Anchor Semiconductor, Inc. (China) . . [6924-146]

Extreme mask corrections: technology and benefits, Yuri Granik, Nick Cobb, Mentor Graphics Corp. [6924-147]

Variable load kernels for OPC modeling, Shih-Lung Tsai, Fred Lo, Elvis Yang, Ta Hone Yang, Kuang-Chao Chen, Chih-Yuan Lu, Macronix International Co., Ltd. (Taiwan) [6924-148]

Impact of medium and long-range effects on polygate patterning, Manuel Tagliavini, Elisabetta Annoni, Pietro Cantu, Gianfranco Capetti, Chiara Catarisano, Roberto Colombo, Giovanni Magri, Marcello Ravasio, Laura Soma, Federica Zanderigo, STMicroelectronics (Italy) [6924-149]

Design of automatic controllers for model-based OPC with optimal resist threshold determination for improving correction convergence, Yi-Sheng Su, Philip C. W.Ng, Kuen-Yu Tsai, Yung-Yaw Chen, National Taiwan Univ. (Taiwan) [6924-150]

Optical proximity correction performance in the full-chip level by using the 3D mask modeling, No-Young Chung D.V.M., SAMSUNG Electronics Co., Ltd. (South Korea) [6924-151]

Analysis of predictability for contact hole model of 45-nm node using mask corner-rounding factor, Soung-Su Woo, Dae-Kwon Kang, Sung-Ho Lee, Seong-Il Kim, Sun-Yong Lee, SAMSUNG Electronics Co., Ltd. (South Korea) [6924-152]

OPC modeling setup with considering flare effect, Jong-Doo Kim, Euisang Park, Jeahee Kim, Keeho Kim, Dongbu Electronics Co., Ltd. (South Korea) [6924-153]

Enhancement of full-chip CD variation by using design- based metrology for critical layer of sub-60-nm memory, Dae-Jin Park, Sung-woo Ko, Jae-Seung Choi, Cheol-Kyun Kim, Dong-Gyu Yim, Hynix Semiconductor Inc. (South Korea) [6924-154]

Intelligent process window OPC for 32-nm node full-chip device, Woon-Hyuk Choi, No-Young Chung, Byung-Sung Kim, Hong-Jae Shin, Nae-In Lee, SAMSUNG Electronics Co., Ltd. (South Korea) [6924-155]

Fitness and runtime correlation of compact model complexity, Monica L. Kempbell, Rochester Institute of Technology; Yuri Granik, Nick B. Cobb, Mentor Graphics Corp. [6924-158]

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AltPSM contact hole application at DRAM 4x-nm nodes with dry 193-nm lithography, Christoph Noelscher, Thomas Henkel, Franck Jauzion-Graverolle, Mario Hennig, Qimonda Dresden GmbH & Co. OHG (Germany); Ralph Schlieff, Qimonda North America Corp.; Molela Moukara, Roderick Koehle, Qimonda AG (Germany); Ralf Neubauer, Advanced Mask Technology Ctr. (Germany) [6924-159]

An approach for nanometer trench and hole formation, Zhongyan Wang, Ming Sun, Xilin Peng, Thomas Boonstra, Seagate Technology. [6924-160]

Multipatterning overlay control, Christopher P. Ausschnitt, IBM Microelectronics Div. [6924-161]

Resist bias in Iso-focal structure, Jian-Liang Li, Aram Kazarian, Lawrence Melvin III, Synopsys, Inc. [6924-162]

Reflectivity control in hyper-NA immersion lithography, Zhimin Zhu, Brewer Science, Inc. [6924-163]

Resolution enhancement techniques, Hyesung Lee, Sang-Uk Lee, Jeahee Kim, Keeho Kim, Dongbu Electronics Co., Ltd. (South Korea); Keun-Young Kim, International Technology Alliances, Inc. [6924-164]

32nm overlay improvement capability, Brad J. Eichelberger, Kevin Huang, Kelly O'Brien, KLA-Tencor Corp. [6924-166]

Optimization of focus profile in small lens systems, Hakyu Choi, Seungryong Park, Jin-Ho Park, Young-Je Yun, Kwangseon Choi, Jea-Hee Kim, Keeho Kim, Dongbu Electronics Co., Ltd. (South Korea) [6924-168]

22-nm half-pitch patterning by CVD spacer self-aligned double patterning, Chris Bencher, Yongmei Chen, Huixiong Dai, Applied Materials, Inc.; Warren Montgomery, Univ. at Albany. [6924-169]

Reflectivity induced variation in implant layer lithography, Todd C. Bailey, IBM Microelectronics Div.; Greg McIntyre, IBM Corp.; Bidan Zhang, Ryan Deschner, Sohan S. Mehta, Won Song, IBM Microelectronics Div.; Hyung-Rae Lee, SAMSUNG Electronics Co., Ltd.; Yu Hue, IBM Microelectronics Div.; Mary J. Brodsky, IBM Corp. [6924-171]

Investigation of mechanism of pattern deformation on TiN substrate and O2 plasma effect without BARC, Juhyoung Moon, Young-Je Yun, Kwangseon Choi, Jeahee Kim, Keeho Kim, Dongbu Electronics Co., Ltd. (South Korea) [6924-172]

Rigorous modeling and analysis of impact produced by microstructures in mask-on-wafer pattern fidelity, Irina Pundaleva, Roman Chalykh, Myoung-Soo Lee, Hee-Bom Kim, Byung-Gook Kim, Han-Ku Cho, SAMSUNG Electronics Co., Ltd. (South Korea) [6924-173]

The flash memory battle: how low can we go?, Eelco van Setten, Kees Grim, Jo Finders, ASML Netherlands B.V. (Netherlands); Mircea Dusa, ASML US, Inc.; Robert Birkner, Rigo Richter, Thomas Scheruebl, Carl Zeiss SMS GmbH (Germany) [6924-174]

Measuring layer specific depth-of-focus requirements, Bernhard R. Liegl, IBM Corp.; Allen Gabor, IBM Microelectronics Div.; Michael Lofaro, John M. Cotte, Mahadevaiayer Krishnan, IBM Thomas J. Watson Research Ctr.[6924-175]

Effects of laser bandwidth on tool-to-tool CD matching, Bo-Yun Hsueh, United Microelectronics Corp. (Taiwan) [6924-176]

A comparison of experimental and production imaging systems for high-NA 193-nm immersion lithography, Emil C. Piscani, Daniel Cochran, SEMATECH, Inc.; Will Conley, Freescale Semiconductor, Inc.; Mark J. Maslow, Shane R. Palmer, John S. Petersen, Petersen Advanced Lithography, Inc. [6924-178]

Improving lithography intra-wafer CD for implant layers using STI thickness feed forward, Jean Massin, Jean-Damien Chapon, Maxime Gatefait, Bertrand Le-Gratiet, Blandine Minghetti, STMicroelectronics (France) [6924-179]

More on practical solutions for reticle haze control: purged reticle stockers, Oleg Kishkovich, Bill Goodwin, Entegris, Inc. [6924-180]

Monitoring defects at wafer's edge for improved immersion lithography performance, Chris F. Robinson, Jeff Bright, IBM Corp.; Dan Corliss, IBM Microelectronics Div.; Mike Guse, IBM Corp.; George Mack, IBM Microelectronics Div. [6924-181]

Modeling the work piece charging during e-beam lithography, Benjamin L. Alles, Bernd Simeon, Technische Univ. München (Germany); Eric Cotte, Timo Wandel, Advanced Mask Technology Ctr. (Germany) [6924-182]

SEM contour-based mask modeling, James E. Vasek, Freescale Semiconductor, Inc.; Ir Kusnadi, Edita Tejnli, Mentor Graphics Corp.; Ovadya Menadeva, Ram Peltinov, Applied Materials (Israel) [6924-183]

Integration of high-speed surface-channel charge coupled devices into an SOI CMOS process using strong phase-shift lithography, Jeffrey M. Knecht, Vladimir Bolkhovsky, Jay Sage, Brian Tyrrell, Bruce Wheeler, Charles Wynn, MIT Lincoln Lab. [6924-184]

22-nm 1:1 line and space patterning by resist reflow process, Hye-Keun Oh, Joon-Min Park, HeeJun Jeong, Ilsin An, Hanyang Univ. (South Korea) [6924-185]

Optimum dose variation caused by post-exposure bake-temperature difference inside photoresist over different sublayers and thicknesses, Hye-Keun Oh, Young-Min Kang, Ilsin An, Do Wan Kim, Hanyang Univ. (South Korea) [6924-186]

Haze defects by pellicle adhesive, Young-Min Kang, Seung Wook Park, Hye Keun Oh, Hanyang Univ. (South Korea) [6924-187]

The analysis of optical lithography at quarter wavelength two-dimensional structure, Chan-Ha Park, Tae-Seung Eom, Hye-Jin Shin, Ki-Ho Yang, Jin-Young Choi, Hyun-Jo Yang, Hyeong-Soo Kim, Dong-Gyu Yim, Jin-Woong Kim, Hynix Semiconductor Inc. (South Korea) [6924-188]

Image contrast contributions to immersion lithography defect formation and process yield, Benjamin M. Rathsack, Joshua Hooge, Steven Scheer, Tokyo Electron America, Inc.; Kathleen Nafus, Shinichi Hatakeyama, Hontake Kouichi, Junichi Kitano, Tokyo Electron Kyushu Ltd. (Japan); Dieter Van Den Heuval, Eric Hendrickx, Philippe Leray, Philippe Foubert, IMEC [6924-189]

Demonstration of production readiness of an immersion lithography cell, Paolo Piacentini, STMicroelectronics (Italy) [6924-190]

Simulation

High-speed microlithography aerial image simulation without four-dimensional single-value decomposition, Charlie C. Chen, National Taiwan Univ. (Taiwan) [6924-191]

TE and TM Eigenmodes applied to thick mask modeling, Gary A. Allen, Paul S. Davids, Intel Corp. [6924-192]

A new domain decomposition method for rigorous electromagnetic field simulations, Lin W. Zschiedrich, Sven Burger, Achim Schädle, Frank Schmidt, Zuse Institute Berlin (Germany) [6924-193]

Influence of pellicle on hyper-NA imaging, Kazuya Sato, Toshiba Semiconductor Co. (Japan); Satoshi Nagai, Shinichiro Nakagawa, Takashi Sato, Toshiba Corp. (Japan); Masamitsu Itoh, Toshiba Semiconductor Co. (Japan) [6924-195]

Rigorous electromagnetic-field simulation of two-beam interference exposures for the exploration of double-patterning and double-exposure scenarios, Andreas Erdmann, Peter Evanschitzky, Tim Fühner, Thomas Schnattinger, Fraunhofer Institut Integrierte System und Bauelem (Germany); Cheng-Bai Xu, Chuck Szamanda, Rohm and Haas Electronic Materials. [6924-196]

A simulation study on the impact of lithographic process variations on CMOS device performance, Tim Fühner, Fraunhofer Institut Integrierte System und Bauelem (Germany); Ina Kodrasi, Jacobs Univ. Bremen (Germany); Christian Kampen, Thomas Schnattinger, Alexander Burenkov, Andreas Erdmann, Fraunhofer Institut Integrierte System und Bauelem (Germany) [6924-197]

Friday 29 February

SESSION 13

Conv. Ctr. A2 Fri. 8:00 to 10:00 am

Lithography Tools I

Session Chairs: **Bruce W. Smith**, Rochester Institute of Technology; **Tatsuhiko Higashiki**, Toshiba Corp. (Japan)

8:00 am: **Recent performance results of Nikon immersion lithography tools**, Andrew J. Hazelton, Kenichi Shiraishi, Shinji Wakamoto, Yuuki Ishii, Masahiko Okumura, Nobutaka Magome, Hiroyuki Suzuki, Nikon Corp. (Japan) . . [6924-58]

8:20 am: **Performance of the FPA-7000AS7: 1.35-NA immersion exposure system for 45-nm mass production**, Keiji Yoshimura, Hitoshi Nakano, Hideo Hata, Nobuyoshi Deguchi, Masamichi Kobayashi, Takeaki Ebihara, Yoshio Kawanobe, Tsuneo Kanda, Canon Inc. (Japan) [6924-59]

8:40 am: **Latest developments on immersion exposure systems**, Jan Mulkens, Jos de Klerk, Jan W. Cromwijk, Martijn Leenders, Christian Wagner, ASML Netherlands B.V. (Netherlands) [6924-60]

9:00 am: **Tool-to-tool optical proximity effect matching**, Lieve Van Look, Joost Bekaert, Peter De Bisschop, Jeroen Van de Kerckhove, Geert Vandenberghe, IMEC (Belgium); Edwin Knols, Jasper Menger, Guido Schiffelers, Rob Willekers, ASML Netherlands B.V. (Netherlands) [6924-61]

9:20 am: **XLR 600i: recirculating ring ArF light source for double-patterning immersion lithography**, Theodore Cacouris, Vladimir Fleurov, Slava Rokitski, Robert Bergstedt, Hong Ye, Kevin O'Brien, Robert Jacques, Fedor Trintchouk, Efrain Figueroa, Daniel Brown, William Partlo, Cymer, Inc. [6924-62]

9:40 am: **An intelligent imaging system for ArF scanner**, Tomoyuki Matsuyama, Yasuhiro Ohmura, Toshiharu Nakashima, Hironori Ikezawa, Taro Ogata, Yusaku Uehara, Hisashi Nishinaga, Nikon Corp. (Japan) [6924-63]

Coffee Break. 10:00 to 10:30 am

Best Student Paper Award Announcement

Conv. Ctr. A2 Fri. 10:30 to 10:40 am



SESSION 14

Conv. Ctr. A2 Fri. 10:40 am to 12:20 pm

Lithography Tools II

Session Chairs: **Ken Ozawa**, Sony Atsugi Technology Ctr. (Japan); **Roger H. French**, DuPont Co.

10:40 am: **In-situ polarimetry of illumination for 193-nm lithography**, Hiroshi Nomura, Yohko Furutono, Toshiba Semiconductor Co. (Japan) [6924-64]

11:00 am: **Understanding illumination effects for control of optical proximity effects**, Donis G. Flagello, ASML US, Inc.; Bernd Geh, Carl Zeiss SMT AG (Germany); Roland Stas, Edwin Knols, ASML Netherlands B.V. (Netherlands); Oliver Natt, Joerg Zimmermann, Carl Zeiss SMT AG (Germany) [6924-65]

11:20 am: **Thermal aberration control in projection lens**, Toshiharu Nakashima, Yasuhiro Ohmura, Yusaku Uehara, Hisashi Nishinaga, Taro Ogata, Tomoyuki Matsuyama, Nikon Corp. (Japan) [6924-66]

11:40 am: **Imaging performance optimization for hyper-NA scanner systems in high-volume production**, Mark A. van de Kerckhof, Andre Engelen, Eelco van Setten, ASML Netherlands B.V. (Netherlands); Emil Schmitt-Weaver, ASML US, Inc.; Vincent Plachecki, Hua-Yu Liu, Brion Technologies, Inc.; Wilbert Rooijackers, Klaus Simon, ASML Netherlands B.V. (Netherlands) [6924-67]

12:00 pm: **Monitoring polarization at 193-nm high-numerical aperture with phase shift masks: experimental results and industrial outlook**, Gregory R. McIntyre, IBM Corp.; Richard Tu, Benchmark Technologies. [6924-68]

Courses of Related Interest

See Course Materials Desk for course descriptions.

SC101 Introduction to Microlithography: Theory, Materials, and Processing (Willson, Thompson, Bowden) Sunday, 8:30 am to 5:30 pm
SC102 Optical Lithography Modeling (Neureuther, Smith) Sunday, 6:00 to 10:00 pm
SC105 CD Metrology and Image Formation in the Scanning Electron Microscope (SEM) (Postek, Wells) Sunday, 8:30 am to 5:30 pm
SC116 Lithographic Optimization: A Theoretical Approach (Mack) Sunday, 8:30 am to 5:30 pm
SC118 Anti-Reflective Coatings: Theory and Practice (Dammel) Thursday, 8:30 am to 12:30 pm
SC120 193-nm Photoresist Materials (Dammel) Sunday, 8:30 am to 12:30 pm
SC579 Photomask Fabrication and Technology Basics (Duff) Sunday, 8:30 am to 5:30 pm
SC616 Practical Photoresist Processing (Dammel) Thursday, 1:30 to 5:30 pm
SC831 Introduction to Scatterometry Metrology: Theory and Application (Barry, Bao) Sunday, 1:30 to 5:30 pm
SC886 Line Edge Roughness (Gallatin) Sunday, 1:30 to 5:30 pm
SC540 Applying Optical Proximity Correction and Design for Manufacturability to Product Designs (Capodiec, Lucas) Sunday, 8:30 am to 5:30 pm
SC579 Photomask Fabrication and Technology Basics (Duff) Sunday, 8:30 am to 5:30 pm
SC706 Imaging and Optics Fundamentals in Microlithography (Flagello) Sunday, 1:30 to 5:30 pm
SC707 Basics of Optical Imaging in Microlithography: A Hands-on Approach (Milster, Brooker, Socha) Sunday, 8:30 am to 12:30 pm
SC723 The Limits of Optical Lithography (Pierrat) Sunday, 8:30 am to 12:30 pm
SC724 Optical Lithography Extension: Design for Manufacturing and New Resolution Enhancement Techniques (Pierrat) Sunday, 1:30 to 5:30 pm
SC779 Polarization for Lithographers (Kye, McIntyre) Sunday, 1:30 to 5:30 pm
SC833 Lithography Integration for Semiconductor Back-End-Of-The-Line (BEOL) (Lin) Sunday, 8:30 am to 12:30 pm
SC855 Introduction to Design for Manufacturability (Liebmann, Wong) Tuesday, 1:30 to 5:30 pm
SC856 Computational Lithography (Mansfield, Wong) Wednesday, 1:30 to 5:30 pm
SC885 Principles and Practical Implementation of Double Patterning (Dusa) Sunday, 8:30 am to 12:30 pm
SC887 Modeling of Exposure Tools (Lai) Sunday, 1:30 to 5:30 pm
SC889 Layout-Aware Circuit Analysis (Singh, Heng, Bansal) Wednesday, 8:30 am to 12:30 pm
WS619 Intellectual Assets for Micro/Nano Electronics and Lithography (Cole) Monday, 1:30 to 5:30 pm

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Design for Manufacturability through Design-Process Integration II

Conference Chair: **Vivek K. Singh**, Intel Corp.

Conference Co-Chair: **Michael L. Rieger**, Synopsys, Inc.

Program Committee: **Juan Antonio Carballo**, Argon Venture Partners; **Hiroichi Kawahira**, Sony Corp. (Japan); **Lars W. Liebmann**, IBM Microelectronics Div.; **Mark E. Mason**, Texas Instruments Inc.; **John L. Sturtevant**, Mentor Graphics Corp.; **Dennis M.C. Sylvester**, Univ. of Michigan; **Jörg Thiele**, Qimonda AG (Germany); **Alfred K. K. Wong**, Magma Design Automation

Thursday 28 February

SESSION 3

Conv. Ctr. C1 Thurs. 8:00 to 10:00 am

Keynote Session

Session Chair: **Vivek Singh**, Intel Corp.

- 8:00 am: **DfM: The Teenage Years (Keynote)**, Lars W. Liebmann, IBM Microelectronics Div. [6925-01]
8:40 am: **Evolution and role of design rules to enable 45-nm dry patterning (Keynote)**, Clair Webb, Intel Corp. [6925-02]
9:20 am: **Foundry Talk (Keynote)**, Fu-Chieh Hsu, Taiwan Semiconductor Manufacturing Co. Ltd. (Taiwan) [6925-03]
Coffee Break. 10:00 to 10:30 am

SESSION 2

Conv. Ctr. C1 Thurs. 10:30 am to 12:30 pm

Layout Verification, Hotspots, Variations

Session Chairs: **Michael L. Rieger**, Synopsys, Inc.; **John L. Sturtevant**, Mentor Graphics Corp.

- 10:30 am: **Automatic hotspot classification using pattern-based clustering**, Ning Ma, Justin Ghan, Sandipan Mishra, Costas J. Spanos, Kameshwar Poola, Univ. of California/Berkeley [6925-04]
10:50 am: **Effective learning and feedback to designers through design and wafer inspection integration**, Hermes Liu, United Microelectronics Corp.; Allen Park, KLA-Tencor Corp. [6925-05]
11:10 am: **Rigorous CMP and electroplating simulations for DFM applications**, Yuri Granik, Norbert Strecker, Mentor Graphics Corp. ... [6925-06]
11:30 am: **Global and local factors of on-chip variation of gate length**, Morimi Osawa, Koji Hosono, Satoru Asai, Fujitsu Ltd. (Japan) [6925-07]
11:50 am: **Layout verification in the era of process uncertainty: target process variability bands versus actual process variability bands**, J. Andres Torres, Mentor Graphics Corp. [6925-08]
12:10 pm: **Context analysis and validation of lithography induced systematic variations in 65-nm designs**, Arjun Rajagopal, Anand Rajaram, Raguram Damodaran, Frank Cano, Clive Bittlestone, R. Mark Terry, Mark Mason, Texas Instruments Inc.; Yajun Ran, Haizhou Chen, Robert Richie, Bala Kasthuri, Jac Condella, Nishath Verghese, Philippe Hurat, Cadence Design Systems, Inc.; Srinivas Swaminathan, The Univ. of Texas at Dallas [6925-09]
Lunch Break. 12:30 to 2:00 pm

Conv. Ctr. C1 Thurs. 2:00 to 3:20 pm

Design Rules for Manufacturability

Session Chairs: **Mark E. Mason**, Texas Instruments Inc.; **Hiroichi Kawahira**, Sony Corp. (Japan)

- 2:00 pm: **Low-k1 logic design using gridded design rules**, Michael C. Smayling, Tela Innovations, Inc.; Hua-Yu Liu, Lynn Cai, Brion Technologies, Inc. [6925-68]
2:20 pm: **DFM lessons learned from altPSM design**, Lars W. Liebmann, IBM Global Engineering Solutions; Zachary Baum, Ioana C. Graur, IBM Microelectronics Div.; Donald J. Samuels, IBM Corp. [6925-11]
2:40 pm: **An integrated design strategy for critical layers of a 45nm low-cost LOGIC process for low-power applications using an NA 0.93 KrF dry lithography system**, Ewoud Vreugdenhil, ASML Netherlands B.V. (Netherlands); Harold van Bente, NXP Semiconductors (Netherlands) [6925-12]
3:00 pm: **Inverse lithography as a DFM tool: accelerating design rule development with model-based assist feature placement, fast optical proximity correction and lithographic hotspot detection**, Steven L. Prins, Lewis W. Flanagan, James W. Blatchford, Simon Chang, Scott W. Jessen, Mark E. Mason, Sean C. O'Brien, Texas Instruments Inc.; Guangming Xiao, Timothy Lin, Thuc H. Dam, Bob E. Gleason, Luminescent Technologies, Inc. ... [6925-13]
Coffee Break. 3:20 to 3:50 pm

SESSION 4

Conv. Ctr. C1 Thurs. 3:50 to 5:30 am

Layout Optimization

Session Chairs: **Alfred K. K. Wong**, Magma Design Automation; **Jörg Thiele**, Qimonda AG (Germany)

- 3:50 am: **Layout optimization based on a generalized process variability model**, Qian Ying Tang, Paul Friedberg, Univ. of California/Berkeley; George H. Cheng, Enwave Optronics, Inc.; Costas Spanos, Univ. of California/Berkeley [6925-14]
4:10 am: **Manufacturing for design: a novel interconnect optimization method**, Liang Deng, Univ. of Illinois at Urbana-Champaign; Kai-Yuan Chao, Intel Corp.; Martin D. F. Wong, Univ. of Illinois at Urbana-Champaign . [6925-15]
4:30 am: **Layout optimization for 65-nm standard-cell production library: simultaneous improvement of random and systematic yield loss including lithography**, Maurice Lousberg, Rene J. M. Wientjes, Laurent Le Cam, Ronald de Bruijn, NXP Semiconductors (Netherlands); Simon Klaver, Michiel Oostindie, Frank A. Driessen, Takumi Technology B.V. (Netherlands) [6925-16]
4:50 am: **Shaping gate channels for improved devices**, Saumil Shah, Puneet Gupta, Blaze DFM Inc.; Youngmin Kim, Dennis Sylvester, Univ. of Michigan; Andrew B. Kahng, Univ. of California/San Diego. [6925-17]
5:10 am: **A routing clean-up methodology for improvement of defect and lithography related yield**, Hanno Melzner, Infineon Technologies AG (Germany); Olivier Rizzo, Jacques Herry, Infineon Technologies France S.A.S. (France); Kai Peter, Reinhard Maerz, Infineon Technologies AG (Germany) [6925-18]

Conv. Ctr. C1 Thurs. 6:30 to 8:00 pm

Panel Discussion on DFM Idol

Panel Moderators: **Mark E. Mason**, Texas Instruments Inc.; **Juan Antonio Carballo**, Argon Venture Partners

Over the last five years, pundits, pessimists, prognosticators, and the press have hailed the coming of the DFM Age for IC design. During this time, start-up companies have come and gone, been acquired, or gone public. Large EDA players have restructured product lines. IDMs have deployed internal solutions. Given all of this churn, now seem like the right time to ask some hard questions. Please join us as a "DFM Idol" Panel of Sages answers difficult questions about the state and value of DFM. We will start with our Celebrity DFM Gameshow Challenge, where prepared and random audience questions will be fired at the Sages. A hard-fast drill will then ensue, where each panelist will get to discuss the state of DFM within a strict two-minute limit. Hot and controversial DFM opinions, and difficult questions are not only welcome from the audience but encouraged. Ratings might be given using a secret voting system! As you can see, all DFM knowledge will be exposed.

Conv. Ctr. Hall 3 Thurs. 6:00 to 8:00 pm

Posters-Thursdays

The following posters will be displayed all day Thursday. Authors will be present during the formal poster session Thursday evening between 6:00 and 8:00 pm for discussion. Authors may set-up their posters after 9:00 am on Thursday.

Exposure tool specific post-OPC verification, John L. Sturtevant, Travis E. Brist, Le Hong, Mentor Graphics Corp. [6925-10]

CDU and overlay improvement for the 65-nm NOR technology nodes, Jerome Depre, ASML Netherlands B.V. (Netherlands); Kok-Fai Lim, Nanyang Technological Univ. (Singapore); Jerry R. Ruff, STMicroelectronics (Singapore) [6925-28]

A procedure to back-annotate process-induced layout dimension changes into the post layout simulation netlist, Yan Wang, Jonathan Ho, Xin Wu, Jane Soward, Xilinx, Inc.; Ping Zhang, Joanne J. Wu, Anchor Semiconductor, Inc. [6925-29]

Predicting conversion time of circuit design file by artificial neural networks, Sung-Hoon Jang, SAMSUNG Electronics Co., Ltd. (South Korea) and Sungkyunkwan Univ. (South Korea); Jee-Hyong Lee, Sungkyunkwan Univ. (South Korea); Won-Tai Ki, Ji-Hyeon Choi, Sang-Gyun Woo, Han-Ku Cho, SAMSUNG Electronics Co., Ltd. (South Korea) [6925-30]

System to improve RET/OPC production by dynamic design coverage using sign-off litho simulator, Jean-Marie Brunet, Mark Simmons, Mentor Graphics Corp.; Y. K. Kim, Mentor Graphics Corp. (South Korea); Seung Weon Paek, SAMSUNG Electronics Co., Ltd. (South Korea) [6925-31]

An extraction of repeating patterns from OPCed layout data, Yoshihiro Fujimoto, Masahiro Shoji, Nippon Control System Corp. (Japan); Kokoro Kato, Tadao Inoue, SII NanoTechnology Inc. (Japan); Masaki Yamabe, Association of Super-Advanced Electronics Technologies (Japan) [6925-32]

Accurate model base verification scheme to eliminate hotspots and manage warmspots, Shigeki Nojima, Suigen Kyoh, Shimon Maeda, Soichi Inoue, Toshiba Corp. (Japan) [6925-33]

ACLV- and process-window-aware extraction of transistor parameters using litho-friendly design (Lfd) methodologies, Reinhard März, Kai Peter, Eduard Ratai, Alexander Nielsen, Anton Huber, Infineon Technologies AG (Germany) [6925-34]

Device performance-based OPC for optimal circuit performance and mask cost reduction, Siew Hong Teh, Chun Huat Heng, Arthur E. B. Tay, National Univ. of Singapore (Singapore) [6925-35]

Concurrent development methodology from design rule to OPC in 45-nm node logic device, Kenji Konomi, Shigeki Nojima, Shimon Maeda, Takeshi Fujimaki, Hirofumi Igarashi, Ryuji Ogawa, Shoji Mimotogi, Toshiba Corp. (Japan) [6925-36]

Improvement on OPC completeness through pre-OPC hot spot detection and fix, Yeonah Shim, Sang-Uk Lee, Jeahee Kim, Keeho Kim, Dongbu Electronics Co., Ltd. (South Korea); Keun-Young Kim, International Technology Alliances, Inc. [6925-37]

DFM application on dual tone sub-50-nm device, Byoung Sub Nam, James Moon, Joo-Hong Jung, Dong-Ho Kong, Seh-young Oh, Cheol-Kyun Kim, Byung-Ho M. Nam, Dong Gyu Yim, Hynix Semiconductor Inc. (South Korea) [6925-38]

Library validation for yield enhancement by hybrid method including improved geometric and parametric characterization simultaneously, Seung Weon Paek, SAMSUNG Electronics Co., Ltd. (South Korea) . . . [6925-39]

SEM contour-based model OPC calibrated with optical sensitive patterns, Jee-Eun Jung, SAMSUNG Electronics Co., Ltd. (South Korea). [6925-40]

Hotspot management with die-to-database wafer inspection system, Kohji Hashimoto, Satoshi Usui, Kenji Yoshida, Ichirota Nagahama, Osamu Nagano, Yuuichiro Yamazaki, Soichi Inoue, Toshiba Corp. (Japan) [6925-41]

32-nm OPC design rule evaluation through virtual patterning, Scott W. Jessen, James W. Blatchford, Steve L. Prins, Simon Chang, Yiming Gu, Texas Instruments Inc.; Christopher A. Sallee, Mark D. Smith, Dale Legband, KLA-Tencor Corp. [6925-42]

A new robust process window qualification (PWQ) technique to perform systematic defect characterization to enlarge the lithographic process window is described, using a die-to-database verification tool (NGR2100), Tadashi Kitamura, NanoGeometry Research Inc. (Japan); Michael Hoffman, NanoGeometry Research Inc. [6925-43]

Continuous process window modeling for process variation aware optical proximity correction, Qiaolin Zhang, Yunqiang Zhang, Qiliang Yan, Kevin Lucas, Synopsys, Inc. [6925-44]

Using dual-pitch gratings for optical system characterization through scatterometry, Yu Ben, Jing Xue, Costas J. Spanos, Univ. of California/Berkeley [6925-45]

Rules-based process window OPC, Sean C. O'Brien, Robert A. Soper, Shane Best, Mark E. Mason, Texas Instruments Inc. [6925-46]

RET selection for critical layouts using highly accurate computational lithography, Sanjay H. Kapasi, Trey Graves, Mark D. Smith, KLA-Tencor Corp. [6925-47]

APF pitch-halving for 22-nm logic cells using gridded design rules, Michael C. Smayling, Tela Innovations, Inc.; Christopher Bencher, Michael P. Duane, Applied Materials, Inc. [6925-48]

Site portability and extrapolative accuracy of a predictive resist model, James E. Vasek, Chi-Min Yuan, Freescale Semiconductor, Inc.; John J. Biafore, Stewart A. Robertson, KLA-Tencor Corp. [6925-49]

A comprehensive model of process variability for statistical timing optimization, Kun Qian, Costas J. Spanos, Univ. of California/Berkeley [6925-50]

Application of layout DOE in RET flow, Yunqiang Zhang, Paul van Adrichem, Synopsys, Inc.; Ji Li, Synopsys, Inc. (China); Amy Yang, Kevin Lucas, Synopsys, Inc. [6925-51]

Impact of line-edge roughness on double-gate FinFET performance variability, Kedar Patel, SanDisk Corp.; Tsu-Jae King Liu, Costas Spanos, Univ. of California/Berkeley [6925-52]

Validation and application of a mask model for inverse lithography, Thuc H. Dam, Bob E. Gleason, Dongxue Chen, Danping Peng, Xin Zhou, Luminescent Technologies, Inc. [6925-53]

Combination of rule and pattern-based lithography unfriendly pattern detection in OPC flow, Sang-Uk Lee, Yeonah Shim, Jeahee Kim, Keeho Kim, Dongbu Electronics Co., Ltd. (South Korea); Bo Su, Walter Chan, Ping Zhang, Joanne Wu, Keun-Young Kim, Anchor Semiconductor, Inc. [6925-54]

Friday 29 February

SESSION 5

Marriott San Jose Ballroom Salon III Fri. 8:20 to 10:00 am

DFM Strategies in Design

Session Chairs: **Juan Antonio Carballo**, Argon Venture Partners; **Lars W. Liebmann**, IBM Microelectronics Div.

8:20 am: **A systematic variation aware circuit simulation engine**, Shayak Banerjee, The Univ. of Texas at Austin; Praveen Elakkumanan, James A. Culp, Duruseti Chidambarrao, IBM Microelectronics Div.; Michael Orshansky, The Univ. of Texas at Austin; Saibal Mukhopadhyay, IBM Microelectronics Div. [6925-19]

8:40 am: **VARAN: variability analysis for memory cell robustness**, Gideon Reisfeld, Intel Corp. (Israel); Adi Lazar, Intel Corp. [6925-20]

9:00 am: **Implementation of silicon-validated variability analysis and optimization for standard cell libraries**, Raphael Bingert, Alain Aurand, Eric Balossier, Thierry Devoivre, Jean-Claude Marin, STMicroelectronics (France); Yorick Trouiller, Lab. d'Electronique de Technologie de l'Information (France); Florent Vautrin, STMicroelectronics (France); Michel Cote, Philippe Hurat, Cadence Design Systems, Inc.; Richard Rouse, Nishath Verghese, Clear Shape Technologies, Inc. [6925-21]

9:20 am: **Modeling timing across the lithographic process window**, Eric Chin, Andrew Neureuther, Univ. of California/Berkeley [6925-22]

9:40 am: **Microprocessor chip timing analysis using extraction of simulated silicon-calibrated contours**, Toshiaki Yanagihara, Takeshi Hamamoto, Atsushi Okamura, Naohiro Kobayashi, Koya Sato, Toshiyuki Matsunaga, Tatsuya Maekawa, NEC Electronics Corp. (Japan); Philippe Hurat, Cadence Design Systems, Inc.; Nishath Verghese, Clear Shape Technologies, Inc.; Jac Condella, Cadence Design Systems, Inc. [6925-23]

Coffee Break 10:00 to 10:30 am

SESSION 6

Marriott San Jose Ballroom Salon III Fri. 10:30 to 11:50 am

DFM and Yield

Session Chair: **Michael L. Rieger**, Synopsys, Inc.

10:30 am: **Hyper-sensitive parameter-identifying ring oscillators for lithography process monitoring**, Lynn T. Wang, Wojtek J. Poppe, Liang-Teck Pang, Andrew Neureuther, Elad Alon, Borivoje Nikolic, Univ. of California/Berkeley [6925-24]

10:50 am: **Systematic yield estimation method with lithography simulation**, Suigen Kyoh, Soichi Inoue, Toshiba Corp. (Japan) [6925-25]

11:10 am: **Litho options and their impact on the electrical yield of a 32-nm node 6T SRAM cell**, Staf Verhaegen, Pol Marchal, Axel Nackaerts, IMEC (Belgium); Mircea V. Dusa, ASML; Geert Vandenbergh, IMEC (Belgium) [6925-26]

11:30 am: **Predicting yield using model-based OPC verification: calibrated with electrical test data**, James A. Bruce, IBM Corp.; Tso-Hui Ting, IBM Microelectronics Div. [6925-27]

Cell-based OPC with standard-cell fill insertion for deep-submicron technology node, Liang Deng, Univ. of Illinois at Urbana-Champaign; Kai-Yuan Chao, Intel Corp.; Hua Xiang, IBM Thomas J. Watson Research Ctr.; Martin D. F.Wong, Univ. of Illinois at Urbana-Champaign. [6925-56]

Process variation in metal-oxide-metal (MOM) capacitors, Lynn T. Wang, Andrew Neureuther, Univ. of California/Berkeley. [6925-57]

Manufacturability metrics for failure analysis with layout characteristic check and lithographic simulation, Beom-Seok Seo, Sang-Hee Bae, Woon-Hyuk Choi, No-Young Jung, Sung-Ho Lee, SAMSUNG Electronics Co., Ltd. (South Korea) [6925-58]

Decomposition difficulty analysis for double patterning and the impact, Yuuichi Inazuki, Nobuhito Toyama, Takanori Sutou, Takaharu Nagai, Yasutaka Morikawa, Hiroshi Mohri, Naoya Hayashi, Dai Nippon Printing Co., Ltd. (Japan); Martin Drapeau, Synopsys, Inc. (Canada); Kevin Lucas, Synopsys, Inc. [6925-59]

A method of obtaining optical lithography friendly layout, Sungsoo Suh, Sukjoo Lee, Wooseok Shim, Sangwook Kim, Young-Chang Kim, Yong-Jin Chun, Junghyeon Lee, Changjin Kang, SAMSUNG Electronics Co., Ltd. (South Korea) [6925-61]

Checking design conformance and optimizing manufacturability using automated double-patterning decomposition, Christopher M. Cork, Synopsys, Inc. (France); Levi D. Barnes, Ben Painter, Gerry Luk-Pat, Kevin Lucas, Synopsys, Inc.; Vincent Wiaux, Staf Verhaegen, Mireille Maenhoudt, IMEC (Belgium). [6925-62]

Layout patterning check for DFM, Chia-Cheng Chang, Taiwan Semiconductor Manufacturing Co. Ltd. (Taiwan) [6925-63]

Design-based binning for litho qualification and process window qualification, Laurent Karsenti, Mark Geshel, Amiad Conley, Avishai Bartov, Applied Materials (Israel); Andreas Fischer, Uwe Seifert, Arno Wehner, Qimonda Dresden GmbH & Co. OHG (Germany) [6925-64]

DFM software for photomask production and qualification of its accuracy and functionality, Frank A. Driessen, Jurjen Westra, Takumi Technology B.V. (Netherlands); Etsuya Morita, Takumi Technology Corp.; Eiji Yamanaka, Fumiaki Shigemitsu, Toshiba Semiconductor Co. (Japan) [6925-65]

Validating an improved method for lithography model calibration, Chris A. Mack, Lithoguru.com [6925-66]

Implementing a framework to generate a unified OPC from different EDA vendors for 45-nm node and beyond, Chia Wei Huang, Pei Ru Tsai, Calvin Wu, Chuen Huei Yang, United Microelectronics Corp. (Taiwan); Shady A. Abdelwahed, Nader Hindawy, Mohamed AL-Iman, Rami Fathy, Mentor Graphics Corp. (Egypt); Regina Shen, Jochen Schacht, Mentor Graphics Corp. (Taiwan) [6925-67]

Electrically driven optical proximity correction, Shayak Banerjee, The Univ. of Texas at Austin; Praveen Elakkumanan, Lars W. Liebmann, James A. Culp, IBM Microelectronics Div.; Michael Orshansky, The Univ. of Texas at Austin [6925-69]

Courses of Related Interest
<i>See Course Materials Desk for course descriptions.</i>
SC855 Introduction to Design for Manufacturability (Liebmann, Wong) Tuesday, 1:30 to 5:30 pm
SC856 Computational Lithography (Mansfield, Wong) Wednesday, 1:30 to 5:30 pm
SC889 Layout-Aware Circuit Analysis (Singh, Heng, Bansal) Wednesday, 8:30 am to 12:30 pm
SC885 Principles and Practical Implementation of Double Patterning (Dusa) Sunday, 8:30 am to 12:30 pm
SC887 Modeling of Exposure Tools (Lai) Sunday, 1:30 to 5:30 pm
SC833 Lithography Integration for Semiconductor Back-End-Of-The-Line (BEOL) (Lin) Sunday, 8:30 am to 12:30 pm
SC540 Applying Optical Proximity Correction and Design for Manufacturability to Product Designs (Capodiec, Lucas) Sunday, 8:30 am to 5:30 pm
SC116 Lithographic Optimization: A Theoretical Approach (Mack) Sunday, 8:30 am to 5:30 pm
SC105 CD Metrology and Image Formation in the Scanning Electron Microscope (SEM) (Postek, Wells) Sunday, 8:30 am to 5:30 pm
WS619 Intellectual Assets for Micro/Nano Electronics and Lithography (Cole) Monday, 1:30 to 5:30 pm

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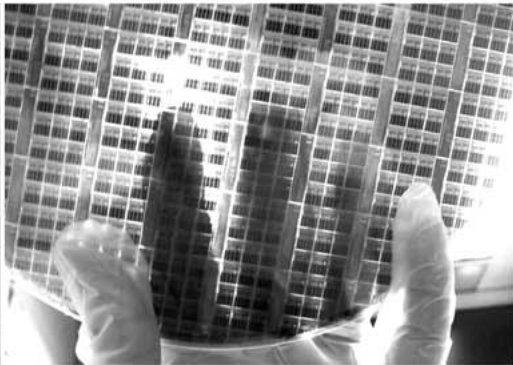
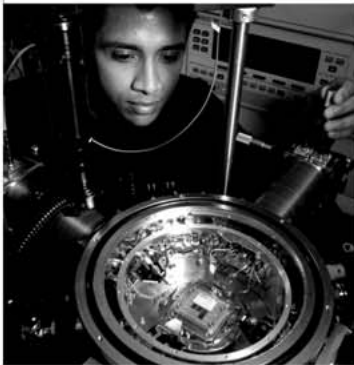
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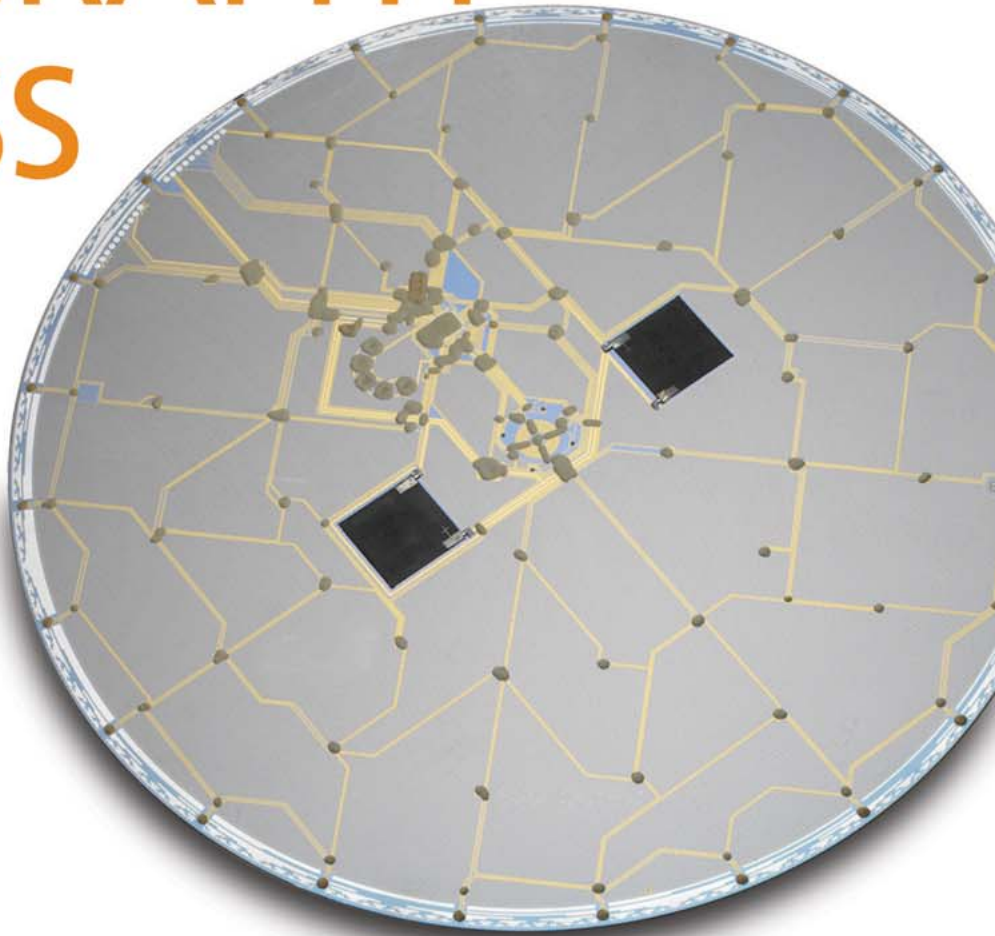
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