# 54AC/74AC708 • 54ACT/74ACT708

## 64 x 9 First-In, First-Out Memory

### Description

The 'AC/'ACT708 is an expandable first-in, first-out memory organized as 64 words by 9 bits. An 85 MHz shift-in and 60 MHz shift-out data rate make it ideal for high-speed applications. It uses a dual port RAM architecture with pointer logic to achieve the high speed with almost negligible fall-through time.

Separate Shift-In (SI) and Shift-Out (SO) clocks control the use of synchronous or asynchronous write or read. Other controls include a Master Reset ($\overline{MR}$) and Output Enable ($\overline{OE}$) for initializing the internal registers and allowing the data outputs to be 3-stated. Input Ready (IR) and Output Ready (OR) signal when the FIFO is ready for I/O operations. The status flags HF and FULL indicate when the FIFO is full, empty or half full.

The FIFO can be expanded to increase the depth by cascading or to provide different word lengths by tying off unused data inputs.

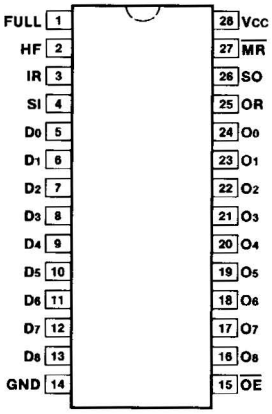
- **64-Words by 9-Bit Dual Port RAM Organization.**
- **85 MHz Shift-In, 60 MHz Shift-Out Data Rate with Flags, Typical 'ACT708**
- **Expandable in Word Depth and Width Dimensions**
- **'ACT708 has TTL-Compatible Inputs**
- **Asychronous or Synchronous Operation**
- **Asynchronous Master Reset**
- **Outputs Source/Sink 8 mA**
- **3-State Outputs**
- **Full ESD Protection**
- **Output and Input Pins Directly in Line for Easy Board Layout**
- **TRW 1030 Work-Alike Operation Available**

### Applications

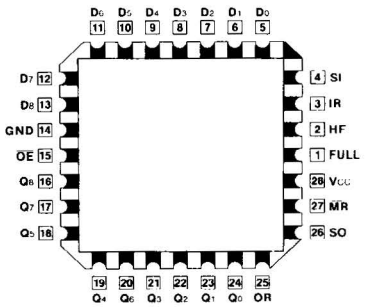
- **High-Speed Disk or Tape Controllers**
- **A/D Output Buffers**
- **High-Speed Graphics Pixel Buffer**
- **Video Time Base Correction**
- **Digital Filtering**

**Ordering Code:** See Section 6

### Connection Diagrams

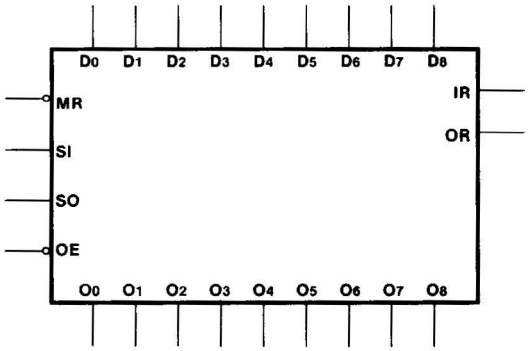



**Pin Assignment for DIP and Flatpak**




**Pin Assignment for LCC and PCC**

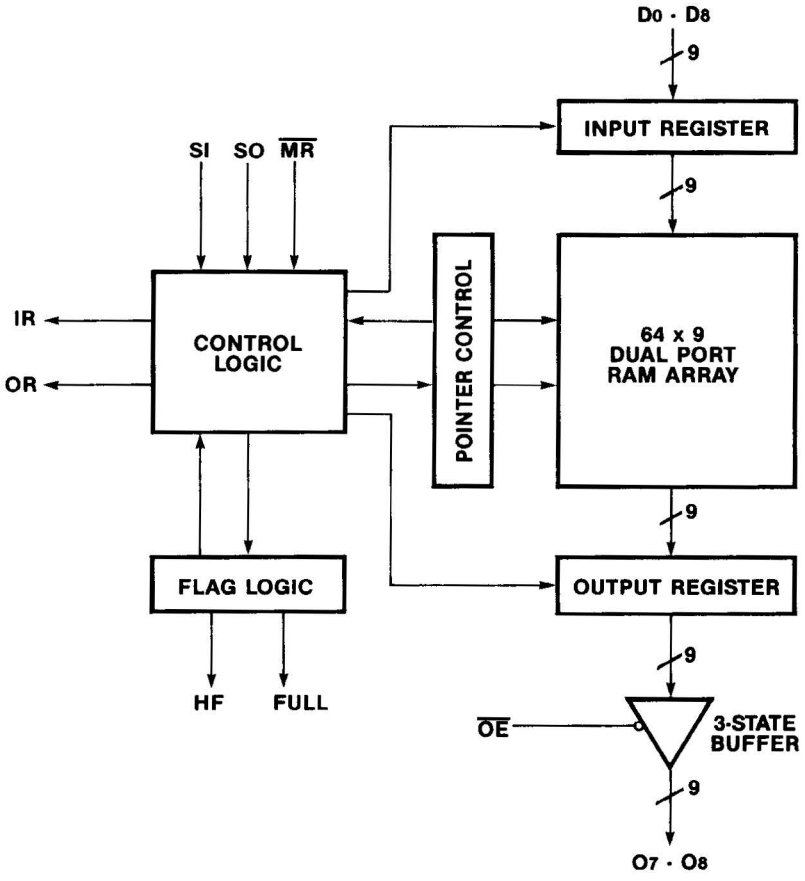
## Logic Symbol




## Pin Names

| | |
|---|---|
| $D_0$ - $D_8$ | Data Inputs |
| $\overline{MR}$ | Master Reset |
| $\overline{OE}$ | Output Enable Input |
| SI | Shift-In |
| SO | Shift-Out |
| IR | Input Ready |
| $\overline{OR}$ | Output Ready |
| HF | Half Full Flag |
| FULL | Full Flag |
| $O_0$ - $O_8$ | Data Outputs |

## Block Diagram

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## Functional Description

### Inputs

Data Inputs ($D_0$ - $D_8$)
Data inputs for 9-bit wide data are TTL-compatible ('ACT708). Word width can be reduced by tying unused inputs to ground and leaving the corresponding outputs open.

Reset ($\overline{MR}$)
Reset is accomplished by pulsing the $\overline{MR}$ input LOW. During normal operation $\overline{MR}$ is HIGH. A reset is required after power up to guarantee correct operation. On reset, the data outputs go LOW, IR goes HIGH, OR goes LOW, HF and FULL go LOW. During reset, both internal read and write pointers are set to the first location in the array.

Shift-In (SI)
Data is written into the FIFO by pulsing SI HIGH. When Shift-In goes HIGH, the data is loaded into an internal data latch. Data setup and hold times need to be adhered to with respect to the falling edge of SI. The write cycle is complete after the falling edge of SI. The shift-in is independent of any ongoing shift-out operation. After the first word has been written into the FIFO, the falling edge of SI makes HF go HIGH, indicating a non-empty FIFO. The first data word appears at the output after the falling edge of SI. After half the memory is filled, the next rising edge of SI makes FULL go HIGH indicating a half-full FIFO. When the FIFO is full, any further shift-ins are disabled.

When the FIFO is empty and $\overline{OE}$ is LOW, the falling edge of the first SI will cause the first data word just shifted-in to appear at the output, even though SO may be LOW.

Shift-Out (SO)
Data is read from the FIFO by the Shift-Out signal provided the FIFO is not empty. SO going HIGH causes OR to go LOW indicating that output stage is busy. On the falling edge of SO, new data reaches the output after propagation delay $t_D$. If the last data has been shifted-out of the memory, OR continues to remain LOW, and the last word shifted-out remains on the output pins.

Output Enable ($\overline{OE}$)
$\overline{OE}$ LOW enables the 3-state output buffers. When $\overline{OE}$ is HIGH, the outputs are in a 3-state mode.

### Outputs

Data Outputs ($O_0$ - $O_8$)
Data outputs are enabled when $\overline{OE}$ is LOW and in the 3-state condition when $\overline{OE}$ is HIGH.

Input Ready (IR)
IR HIGH indicates data can be shifted-in. When SI goes HIGH, IR goes LOW, indicating input stage is busy. IR stays LOW when the FIFO is full and goes HIGH after the falling edge of the first shift-out.

Output Ready (OR)
OR HIGH indicates data can be shifted-out from the FIFO. When SO goes HIGH, OR goes LOW, indicating output stage is busy. OR is LOW when the FIFO is reset or empty and goes HIGH after the falling edge of the first shift-in.

Half-Full (HF)
This status flag along with the FULL status flag indicates the degree of fullness of the FIFO. On reset, HF is LOW; it rises on the falling edge of the first SI. The rising edge of the SI pulse that fills up the FIFO makes HF go LOW. Going from the empty to the full state with SO LOW, the falling edge of the first SI causes HF to go HIGH, the rising edge of the 33rd SI causes FULL to go HIGH, and the rising edge of the 64th SI causes HF to go LOW.

When the FIFO is full, HF is LOW and the falling edge of the first shift-out causes HF to go HIGH indicating a "non-full" FIFO.

Full Flag (FULL)
This status flag along with the HF status flag indicates the degree of fullness of the FIFO. On reset, FULL is LOW. When half the memory is filled, on the rising edge of the next SI, the FULL flag goes HIGH. It remains set until the difference between the write pointer and the read pointer is less than or equal to one-half of the total memory of the device. The FULL flag then goes LOW on the rising edge of the next SO.

### Status Flags Truth Table

| HF | FULL | Status Flag Conditions |
|---|---|---|
| 0 | 0 | Empty |
| 0 | 1 | Full |
| 1 | 0 | $<32$ Locations Filled |
| 1 | 1 | $\geq 32$ Locations Filled |

### Reset Truth Table

| Inputs | | | Outputs | | | | |
|---|---|---|---|---|---|---|---|
| $\overline{MR}$ | SI | SO | IR | OR | HF | FULL | O0 - O8 |
| 1 | X | X | X | X | X | X | X |
| 0 | X | X | 1 | 0 | 0 | 0 | 0 |

### Modes of Operation

**Mode 1: Shift In Sequence for FIFO Empty to Full**

**Sequence of Operation**

1. Input Ready is initially HIGH; HF and FULL flags are LOW. The FIFO is empty and prepared for valid data. OR is LOW indicating that the FIFO is not yet ready to output data.

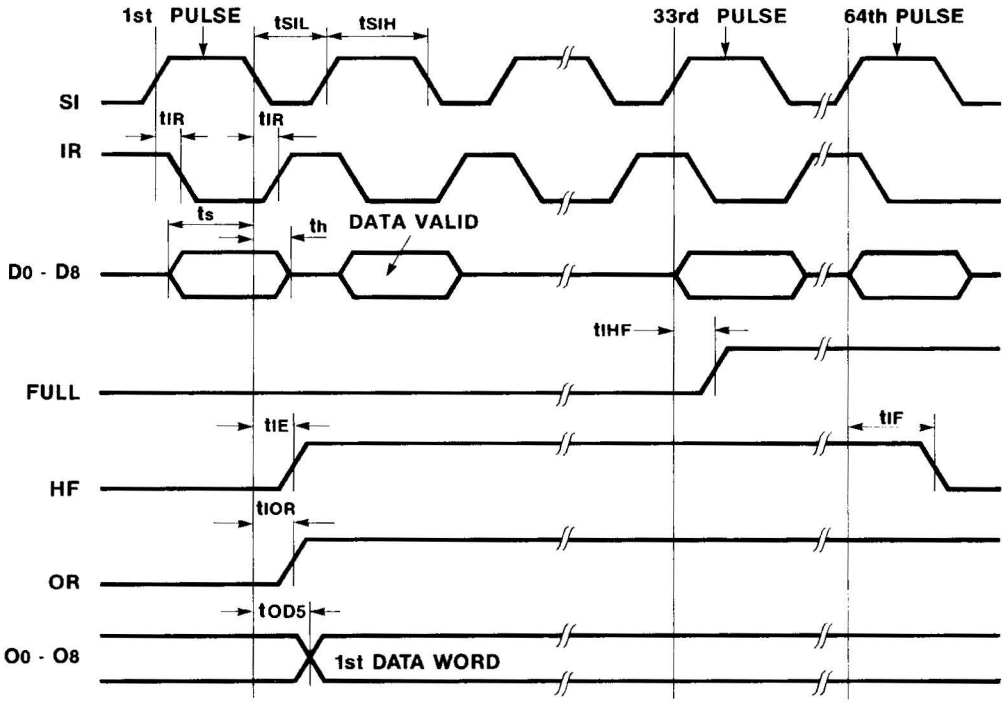
2. Shift-In is set HIGH, and data is loaded into the FIFO. Data has to be settled $t_S$ before the falling edge of SI and held $t_H$ after.

3. Input Ready (IR) goes LOW propagation delay $t_{IR}$ after SI goes HIGH: input stage is busy.

4. Shift-In is set LOW; IR goes HIGH indicating the FIFO is ready for additional data. Data just shifted-in arrives at output propagation delay $t_{OD5}$ after SI falls. OR goes HIGH propagation delay $t_{IOR}$ after SI goes LOW, indicating the FIFO has valid data on its outputs. HF goes HIGH propagation delay $t_{IE}$ after SI falls, indicating the FIFO is no longer empty.

5. The process is repeated through the 64th data word. On the rising edge of the 33rd SI, FULL flag goes HIGH propagation delay $t_{IHF}$ after SI, indicating a half-full FIFO. HF goes LOW propagation delay $t_{IF}$ after the rising edge of the 64th pulse indicating that the FIFO is full. Any further shift-ins are disabled.

**Figure 1: Modes of Operation**
**Mode 1**




Note: SO and $\overline{OE}$ are LOW; $\overline{MR}$ is HIGH.

**Mode 2: Master Reset**

**Sequence of Operation**

1. Input and Output Ready, HF and FULL can be in any state before the reset sequence with Master Reset ($\overline{MR}$) HIGH.

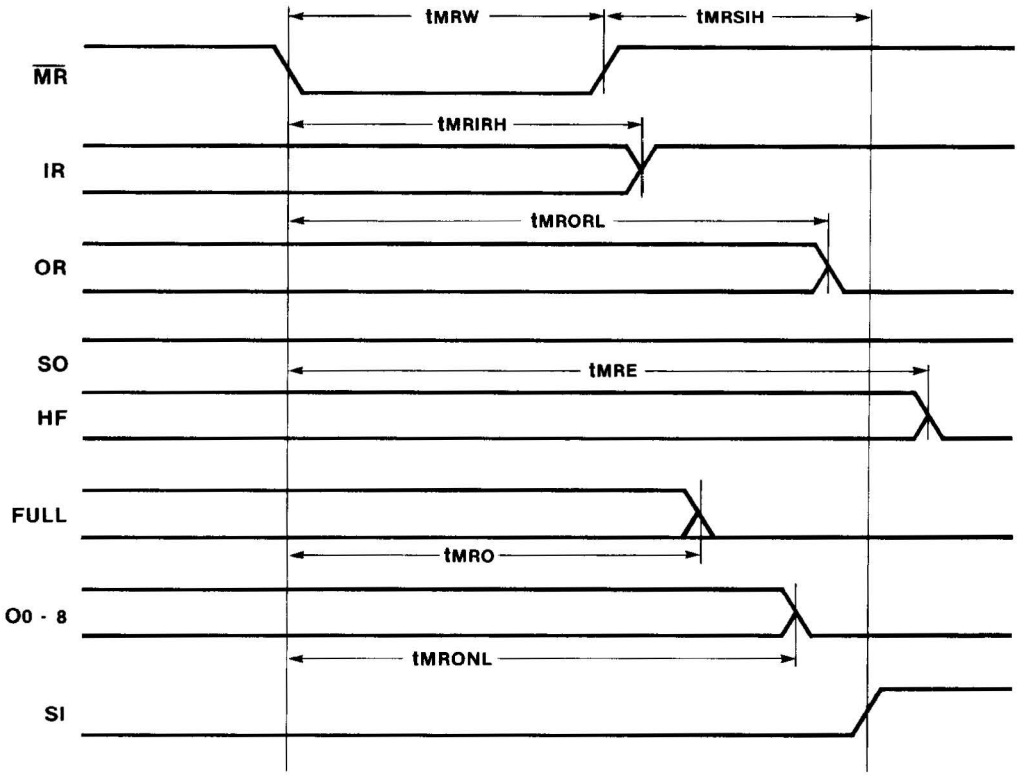
2. Master Reset goes LOW and clears the FIFO, setting up all essential internal states. Master Reset must be LOW pulse width $t_{MRW}$ before rising again.

3. Master Reset rises.

4. IR rises (if not HIGH already) to indicate ready to write state recovery time $t_{MRIRH}$ after the falling edge of $\overline{MR}$. Both HF and FULL will go LOW indicating an empty FIFO, occurring recovery times $t_{MRE}$ and $t_{MRO}$ respectively after the falling edge of $\overline{MR}$. OR falls recovery time $t_{MRORL}$ after $\overline{MR}$ falls. Data at outputs goes LOW recover time $t_{MRONL}$ after $\overline{MR}$ goes LOW.

5. Shift-In goes HIGH a minimum of recovery time $t_{MRSIH}$ after $\overline{MR}$ goes HIGH.

**Figure 2: Modes of Operation**
**Mode 2**

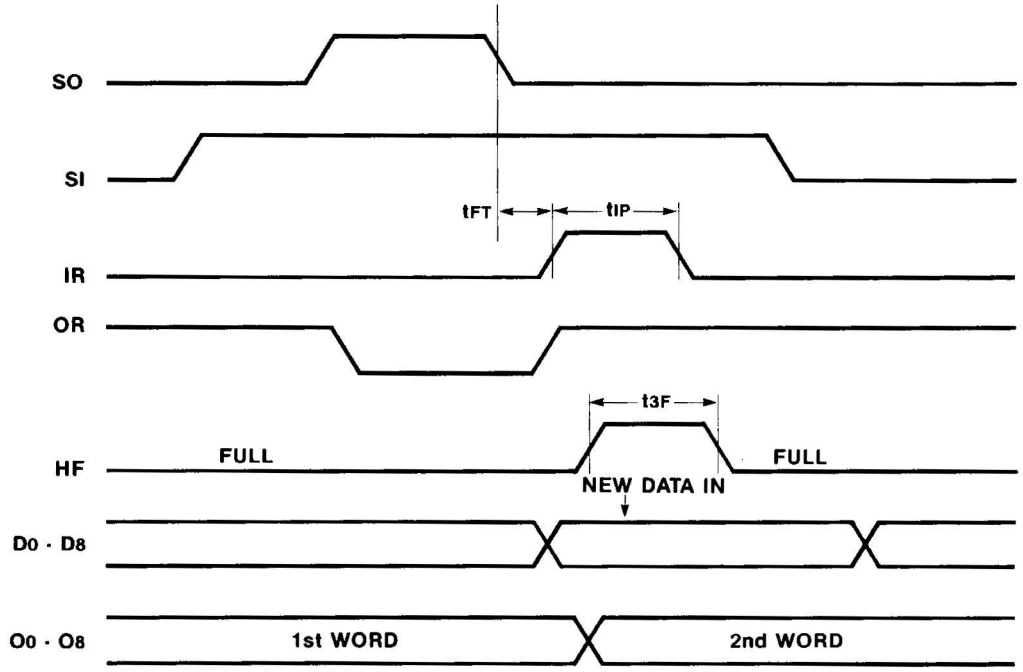


**Mode 3: With FIFO Full, Shift-In is Held HIGH in Anticipation of an Empty Location**

**Sequence of Operation**

1. The FIFO is initially full and Shift-In goes HIGH. OR is initially HIGH. Shift-Out is LOW. IR is LOW.
2. Shift-Out is pulsed HIGH, Shift-Out pulse propagates and the first data word is latched on the rising edge of SO. OR falls on this edge. On the falling edge of SO, the second data word appears after propagation delay $t_D$. New data is written into the FIFO after SO goes LOW.
3. Input Ready goes HIGH fall-through time $t_{FT}$ after the falling edge of SO. Also, HF goes HIGH $t_{OF}$ after SO falls, indicating that the FIFO is no longer full.
4. IR returns LOW pulse width $t_{IP}$ after rising and shifting fresh data in. Also, HF returns LOW pulse width $t_{3F}$ after rising, indicating the FIFO is once more full.
5. Shift-In is brought LOW to complete the shift-in process and maintain normal operation.

**Figure 3: Modes of Operation**
**Mode 3**



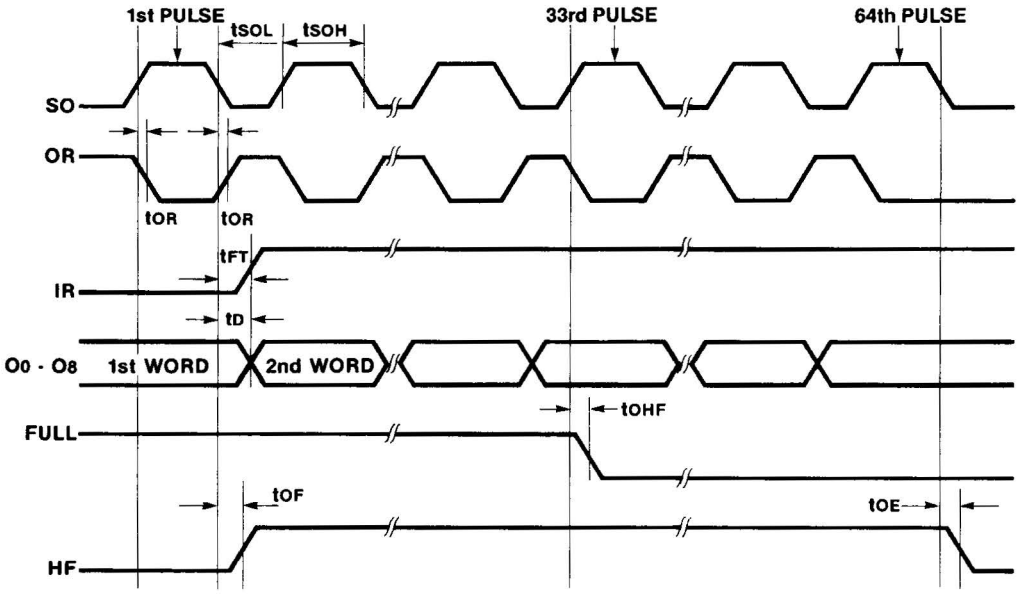

Note: $\overline{MR}$ and FULL are HIGH; $\overline{OE}$ is LOW.

**Mode 4: Shift-Out Sequence, FIFO Full to Empty**

**Sequence of Operation**

1. FIFO is initially full and OR is HIGH, indicating valid data is at the output. IR is LOW.
2. SO goes HIGH, resulting in OR going LOW propagation delay $t_{OR}$ after SO rises. OR LOW indicates output stage is busy.
3. SO goes LOW, new data reaches output propagation delay $t_D$ after SO falls; OR goes HIGH propagation delay $t_{OR}$ after SO falls and HF rises propagation delay $t_{OF}$ after SO falls. IR rises fall-through time $t_{FT}$ after SO falls.
4. Repeat process through the 64th SO pulse. FULL flag goes LOW propagation delay $t_{OHF}$ after the rising edge of 33rd SO, indicating that the FIFO is less than half full. On the falling edge of the 64th SO, HF goes LOW propagation delay $t_{OE}$ after SO, indicating the FIFO is empty. The SO pulse may rise and fall again with an attempt to unload an empty FIFO. This results in no change in the data on the outputs as the 64th word stays latched.

**Figure 4: Modes of Operation**
**Mode 4**



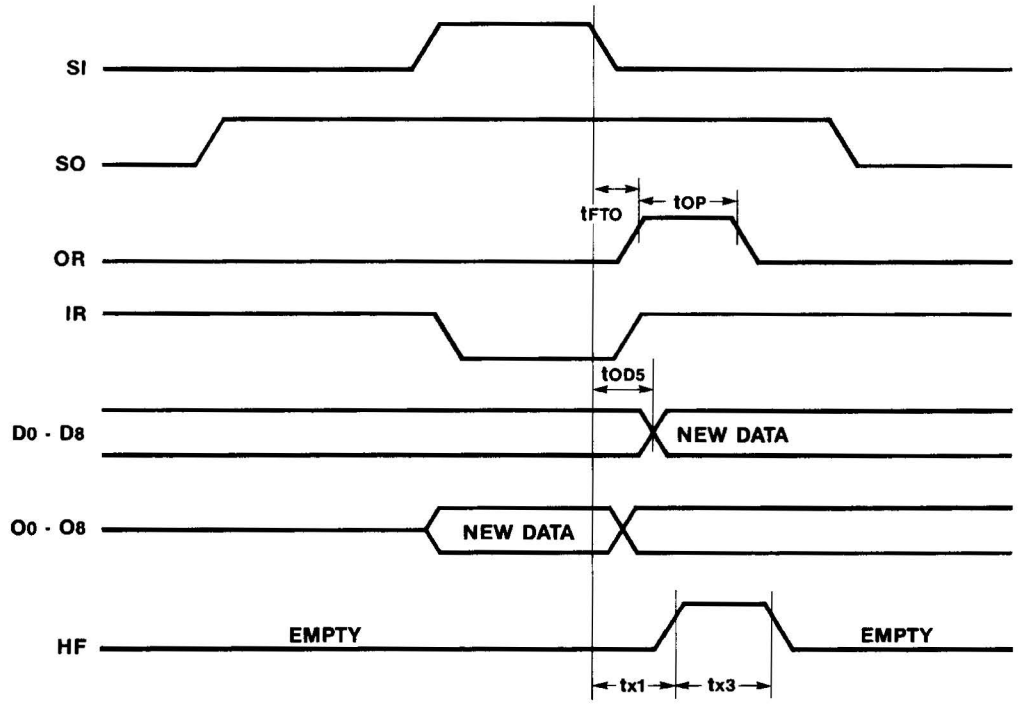

Note: SI and $\overline{OE}$ are LOW; $\overline{MR}$ is HIGH; $D_0$ - $D_8$ are immaterial.

**Mode 5: With FIFO Empty, Shift-Out is Held HIGH in Anticipation of Data**

**Sequence of Operation**

1. FIFO is initially empty; Shift-Out goes HIGH.
2. Shift-In pulse loads data into the FIFO and IR falls. HF rises propagation delay $t_{X1}$ after the falling edge of SI.
3. OR rises fall-through time $t_{FTO}$ after the falling edge of Shift-In, indicating that new data is ready to be output.
4. Data arrives at output propagation delay $t_{OD5}$ after the falling edge of Shift-In.
5. OR goes LOW pulse width $t_{OP}$ after rising and HF goes LOW pulse width $t_{X3}$ after rising, indicating that the FIFO is empty once more.
6. Shift-Out goes LOW, necessary to complete the Shift-Out process.

**Figure 5: Modes of Operation**
**Mode 5**




Note: FULL is LOW; $\overline{MR}$ is HIGH; $\overline{OE}$ is LOW; $t_{DOF} = t_{FTO} - t_{OD5}$. Data output transition—valid data arrives at output stage $t_{DOF}$ after OR is HIGH.

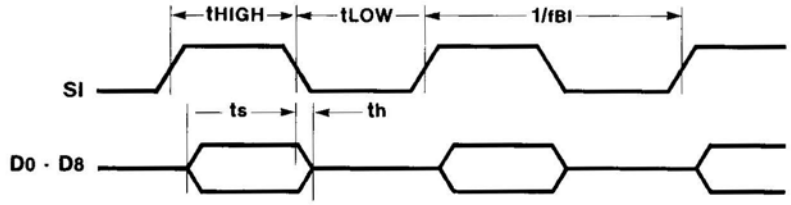
**Mode 6: Shift-In Operation in High-Speed Burst Mode**

**Sequence of Operation**

1. Shift-In goes HIGH, loading data into the FIFO. IR is ignored.
2. Shift-in goes LOW pulse width $t_{HIGH}$ time later, loading is complete.
3. Shift-In rises again for the second load pulse width $t_{LOW}$ after the falling edge.

The burst-in rate is determined by SI HIGH and LOW. Data is shifted-in, ignoring the IR flag. Any SI after the FIFO is filled up will be ignored.

**Figure 6: Modes of Operation**
**Mode 6**




Note: $\overline{MR}$ is HIGH; $t_{HIGH} > t_{SIH}$; $t_{LOW} > t_{SIL}$; $t_{HIGH} + t_{LOW} \geq 1/f_{BI}$.

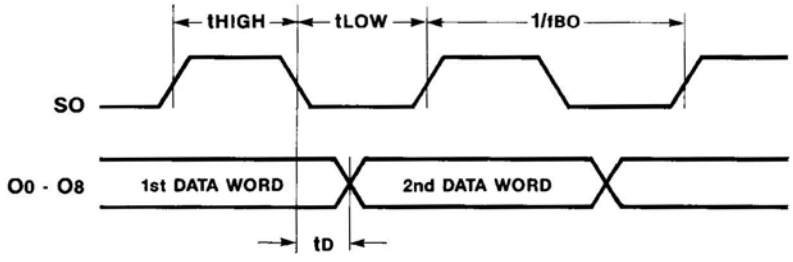
**Mode 7: Shift-Out Operation in High Speed Burst Mode**

**Sequence of Operation**

1. Shift-Out is LOW; valid data is available on output with OR ignored.
2. Shift-Out rises; data out is latched.
3. Shift-Out falls; new data is loaded onto output.

The Burst-out rate is determined by minimum SO HIGH and LOW. The OR flag is ignored.

**Figure 7: Modes of Operation**
**Mode 7**




Note: $\overline{OE}$ is LOW; $\overline{MR}$ is HIGH; $t_{HIGH} > t_{SOH}$; $t_{LOW} > t_{SOL}$; $t_{HIGH} + t_{LOW} \geq 1/f_{BO}$.

**FIFO Expansion**

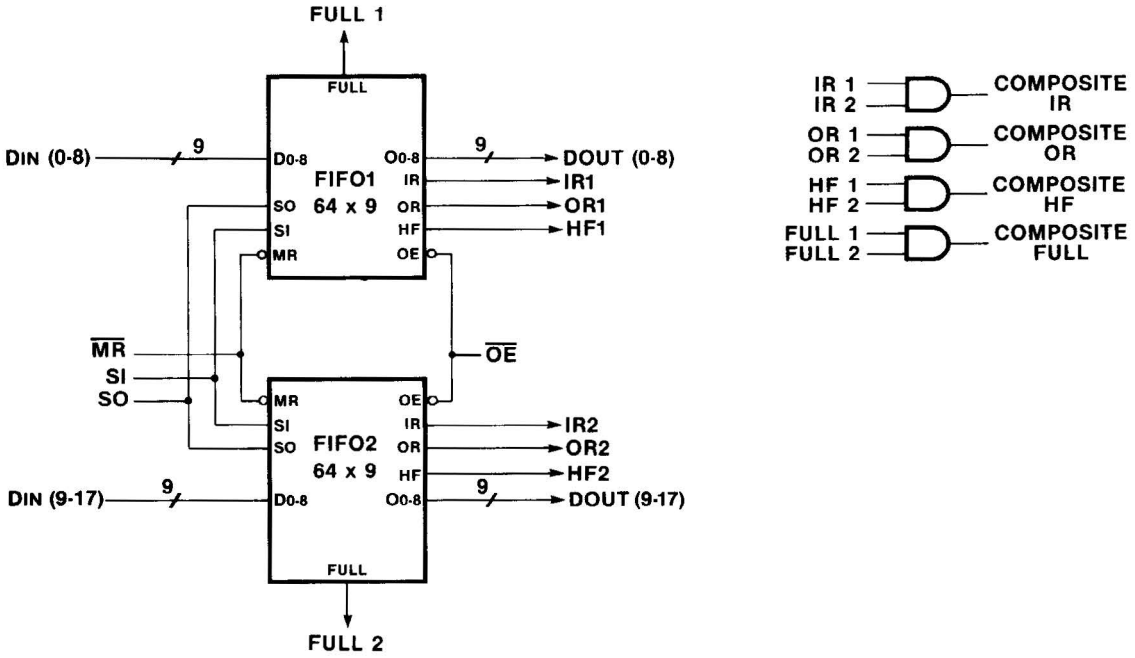
**Word Width Expansion**
Word width can be increased by connecting the corresponding input control signals of multiple devices. Flags can be monitored on any one device (Figure 8), or composite flag signals can be achieved by ANDing the corresponding flags.

**Depth Expansion**
Depth Expansion can be achieved by connecting as shown in Figure 9. No external circuitry is required for handshaking, which is achieved by the internal FIFO signals IR and OR.

When n FIFOs are cascaded to attain a 64n-word FIFO, the SI signal is connected to the first FIFO and the SO signal to the nth FIFO. The IR and OR signals are monitored from the first and last FIFOs respectively. The IR signal from each FIFO is connected to its preceding SO signal: IR(n)→SO(n-1); IR(n-1)→SO(n-2) . . . IR(2)→SO(1). The OR signal from each FIFO is connected to its succeeding SI signal: i.e., OR(1)→SI(2); OR(2)→SI(3) . . . OR(n-1)→SI(n). Handshaking signals are shown in Figure 10.

FIFO1 operates in Mode 5 during Shift-In until FIFO2 is filled. FIFO2 operates in Mode 3 during Shift-Out until FIFO1 is empty. Data from FIFO1 is written into FIFO2 after a word is read from FIFO2. To achieve this, the $\overline{OE}$ pin is grounded for FIFO1. In general, for n FIFOs, all $\overline{OE}$ pins except the nth FIFO's $\overline{OE}$ pin are enabled. 3-state control of the outputs can be achieved by controlling the nth FIFO's $\overline{OE}$ pin.

**Figure 8: Word Width Expansion — 64 x 18 FIFO**




Note: Monitor flags from any one FIFO, or AND the corresponding flags to obtain a composite signal.

**Figure 9: Depth Expansion Mode — 128 x 9 FIFO**

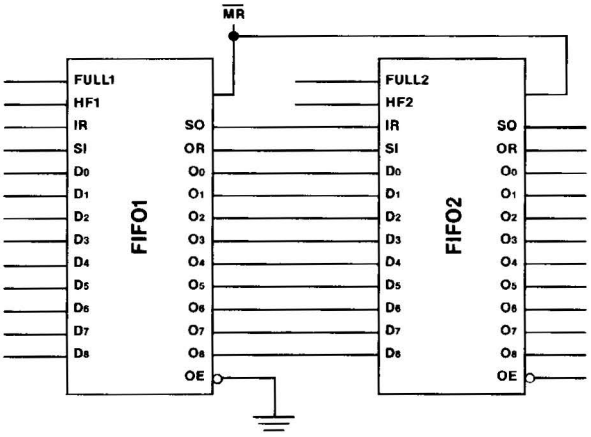
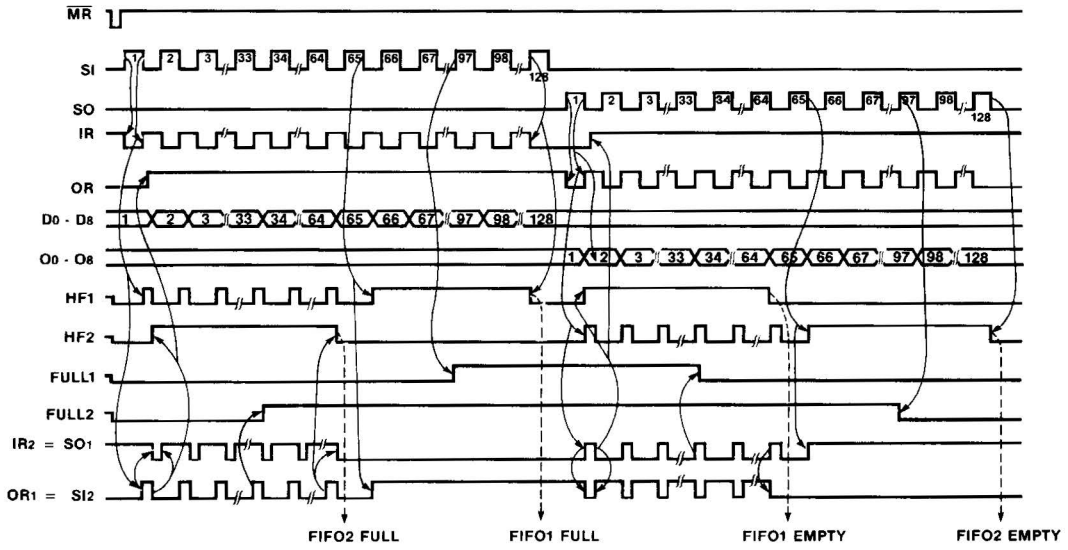



**Figure 10: Handshaking for Depth Expansion Mode—128 x 9 FIFO**




Note: The numbers for SI and SO indicate the pulse numbers. The numbers for data in and data out indicate data words: 1 is first data word, 2 is second data word, etc.

**DC Characteristics over Operating Temperature Range** (unless otherwise specified)

| Symbol | Parameter | 74AC/ACT 25°C | 54AC/ACT | 74AC/ACT | Units | Conditions |
|---|---|---|---|---|---|---|
| | | Typ | Guaranteed Limit | | | |
| $I_{IN}$ | Maximum Input Current | | 0.1 | 10.0 | 1.0 | $\mu$A | $V_{CC}$ = Max<br>$V_{IN}$ = $V_{CC}$ |
| $I_{OZ}$ | Maximum 3-State Current | | 0.5 | 10.0 | 5.0 | $\mu$A | High Z, $V_{CC}$ = Max<br>$V_{OUT}$ = 0 to $V_{CC}$ |
| $I_{CCQ}$ | Supply Current, Quiescent | 50.0 | 2.0 | 10.0 | 10.0 | mA | $V_{CC}$ = Max, $V_{IN}$ = 0 V |
| $I_{CCD}$ | Supply Current, 20 MHz Loaded | 325 | | 150 | 150 | mA | $V_{CC}$ = Max, f = 20 MHz<br>Test Load: See Note 1 |
| $V_{OH}$ | Minimum HIGH Level Output | 4.49 | 4.4 | 4.4 | 4.4 | V | $V_{IN}$ = $V_{IL}$ or $V_{IH}$<br>$I_{OUT}$ = 20 $\mu$A,<br>$V_{CC}$ = 4.5 V |
| | | 5.49 | 5.4 | 5.4 | 5.4 | V | $V_{IN}$ = $V_{IL}$ or $V_{IH}$<br>$I_{OUT}$ = 20 $\mu$A,<br>$V_{CC}$ = 5.5 V |
| | | | 3.86 | 3.70 | 3.76 | V | $I_{OH}$ = −8 mA,<br>$V_{CC}$ = 4.5 V |
| | | | 4.86 | 4.70 | 4.76 | V | $I_{OH}$ = −8 mA,<br>$V_{CC}$ = 5.5 V |
| $V_{OL}$ | Maximum HIGH Level Output | 0.001 | 0.1 | 0.1 | 0.1 | V | $V_{IN}$ = $V_{IL}$ or $V_{IH}$<br>$I_{OUT}$ = 20 $\mu$A,<br>$V_{CC}$ = 4.5 V |
| | | 0.001 | 0.1 | 0.1 | 0.1 | V | $V_{IN}$ = $V_{IL}$ or $V_{IH}$<br>$I_{OUT}$ = 20 $\mu$A,<br>$V_{CC}$ = 5.5 V |
| | | | 0.32 | 0.4 | 0.37 | V | $I_{OL}$ = 8 mA, $V_{CC}$ = 4.5 V |
| | | | 0.32 | 0.4 | 0.37 | V | $I_{OL}$ = 8 mA, $V_{CC}$ = 5.5 V |
| $I_{OLD}$ | Minimum Dynamic Output Current | | | 32 | 32 | mA | $V_{CC}$ = 5.5 V<br>$V_{OLD}$ = 2.2 V |
| $I_{OHD}$ | Minimum Dynamic Output Current | | | −32 | −32 | mA | $V_{CC}$ = 5.5 V<br>$V_{OHD}$ = 3.3 V |

Note 1: Test Load 50 pF, 500 ohm to Ground

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## AC Characteristics

| Symbol | Parameter | Vcc* (V) | 74AC $T_A = +25°C$, $C_L = 50$ pF | | | 54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF | | 74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF | | Units | Fig. No. |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Max | Min | Max | | |
| $t_{PLH}$, $t_{PHL}$ | Propagation Delay, $t_{IR}$ SI to IR | 3.3<br>5.0 | | 8.5<br>5.5 | | | | | | ns | 1 |
| $t_{PLH}$ | Propagation Delay, $t_{IHF}$ SI to >HF | 3.3<br>5.0 | | 13.0<br>9.5 | | | | | | ns | 1 |
| $t_{PHL}$ | Propagation Delay, $t_{IF}$ SI to Full Condition | 3.3<br>5.0 | | 13.0<br>9.5 | | | | | | ns | 1 |
| $t_{PLH}$ | Propagation Delay, $t_{IE}$ SI to Not Empty | 3.3<br>5.0 | | 12.5<br>9.0 | | | | | | ns | 1 |
| $t_{PLH}$ | Propagation Delay, $t_{IOR}$ SI to OR | 3.3<br>5.0 | | 13.0<br>9.5 | | | | | | ns | 1 |
| $t_{PLH}$ | Recovery Time, $t_{MRIRH}$ $\overline{MR}$ to IR | 3.3<br>5.0 | | 9.5<br>7.0 | | | | | | ns | 2 |
| $t_{PHL}$ | Recovery Time, $t_{MRORL}$ $\overline{MR}$ to OR | 3.3<br>5.0 | | 20.0<br>15.0 | | | | | | ns | 2 |
| $t_{PHL}$ | Recovery Time, $t_{MRO}$ $\overline{MR}$ to Full Flag | 3.3<br>5.0 | | 9.5<br>7.0 | | | | | | ns | 2 |
| $t_{PHL}$ | Recovery Time, $t_{MRE}$ $\overline{MR}$ to HF Flag | 3.3<br>5.0 | | 20.0<br>15.0 | | | | | | ns | 2 |
| $t_{PHL}$ | Recovery Time, $t_{MRONL}$ $\overline{MR}$ to $O_n$, LOW | 3.3<br>5.0 | | 11.0<br>8.0 | | | | | | ns | 2 |
| $t_w$ | IR Pulse Width, $t_{IP}$ | 3.3<br>5.0 | | 38.0<br>28.0 | | | | | | ns | 3 |
| $t_w$ | HF Pulse Width, $t_{3F}$ | 3.3<br>5.0 | | 40.0<br>30.0 | | | | | | ns | 3 |
| $t_{PHL}$, $t_{PLH}$ | Propagation Delay, $t_D$ SO to Data Out | 3.3<br>5.0 | | 23.0<br>17.0 | | | | | | ns | 4 |
| $t_{PHL}$ | Propagation Delay, $t_{OHF}$ SO to <HF | 3.3<br>5.0 | | 11.0<br>8.0 | | | | | | ns | 4 |
| $t_{PLH}$ | Propagation Delay, $t_{OF}$ SO to Not Full | 3.3<br>5.0 | | 15.0<br>11.0 | | | | | | ns | 4 |
| $t_{PLH}$, $t_{PHL}$ | Propagation Delay, $t_{OR}$ SO to OR | 3.3<br>5.0 | | 9.5<br>7.0 | | | | | | ns | 4 |

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

**AC Characteristics, cont'd**

| Symbol | Parameter | Vcc* (V) | 74AC $T_A = +25°C$ $C_L = 50$ pF | | | 54AC $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF | | 74AC $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF | | Units | Fig. No. |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Max | Min | Max | | |
| $t_{PLH}$ | Propagation Delay, $t_{OE}$<br>SO to Empty | 3.3<br>5.0 | | 12.5<br>9.0 | | | | | | ns | 4 |
| $t_{PHL}$, $t_{PLH}$ | Propagation Delay, $t_{OD5}$<br>SI to New Data Out | 3.3<br>5.0 | | 22.0<br>16.0 | | | | | | ns | 1, 5 |
| $t_{PLH}$ | Propagation Delay, $t_{X1}$<br>SI to HF | 3.3<br>5.0 | | 13.0<br>9.5 | | | | | | ns | 5 |
| $t_{PLH}$ | Propagation Delay, $t_{DOF}$<br>OR HIGH to Data Out | 3.3<br>5.0 | | <br>-11.5 | | | | | | ns | 5 |
| $t_{PLH}$ | Fall-Through Time, $t_{FTO}$<br>SI to OR | 3.3<br>5.0 | | 16.0<br>11.5 | | | | | | ns | 5 |
| $t_w$ | OR Pulse Width, $t_{OP}$ | 3.3<br>5.0 | | 23.0<br>17.0 | | | | | | ns | 5 |
| $t_w$ | HF Pulse Width, $t_{X3}$ | 3.3<br>5.0 | | 26.0<br>19.0 | | | | | | ns | 5 |
| $t_{PLH}$ | Fall-Through Time, $t_{FT}$<br>SO to IR | 3.3<br>5.0 | | 18.5<br>13.5 | | | | | | ns | 3 |
| $t_{PZL}$ | Output Enable<br>$\overline{OE}$ to $O_n$ | 3.3<br>5.0 | | 7.5<br>5.5 | | | | | | ns | 3-8 |
| $t_{PLZ}$ | Output Disable<br>$\overline{OE}$ to $O_n$ | 3.3<br>5.0 | | 6.0<br>4.5 | | | | | | ns | 3-8 |
| $t_{PZH}$ | Output Enable<br>$\overline{OE}$ to $O_n$ | 3.3<br>5.0 | | 9.0<br>6.5 | | | | | | ns | 3-7 |
| $t_{PHZ}$ | Output Disable<br>$\overline{OE}$ to $O_n$ | 3.3<br>5.0 | | 9.0<br>6.5 | | | | | | ns | 3-7 |
| $f_{SI}$ | Maximum SI<br>Clock Frequency | 3.3<br>5.0 | | 60<br>85 | | | | | | MHz | 1 |
| $f_{SO}$ | Maximum SO<br>Clock Frequency | 3.3<br>5.0 | | 50<br>60 | | | | | | MHz | 4 |
| $f_{BO}$ | Maximum<br>Clock Frequency<br>SO Burst Mode | 3.3<br>5.0 | | 55<br>65 | | | | | | MHz | 7 |
| $f_{BI}$ | Maximum<br>Burst-In Clock | 3.3<br>5.0 | | 60<br>85 | | | | | | MHz | 6 |

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.



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## AC Operating Requirements

| Symbol | Parameter | Vcc* (V) | 74AC $T_A = +25°C$ $C_L = 50$ pF | | 54AC $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF | 74AC $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF | Units | Fig. No. |
|---|---|---|---|---|---|---|---|---|
| | | | Typ | Guaranteed Minimum | | | | |
| $t_w$ | SI Pulse Width, $t_{SIH}$ HIGH | 3.3<br>5.0 | 4.0<br>1.5 | | | | ns | 1, 6 |
| $t_w$ | SI Pulse Width, $t_{SIL}$ LOW | 3.3<br>5.0 | 4.0<br>1.5 | | | | ns | 1, 6 |
| $t_s$ | Setup Time, HIGH or LOW, $D_n$ to SI | 3.3<br>5.0 | 2.0<br>1.0 | | | | ns | 1 |
| $t_h$ | Hold Time, HIGH or LOW, $D_n$ to SI | 3.3<br>5.0 | 3.0<br>1.5 | | | | ns | 1 |
| $t_w$ | $\overline{MR}$ Pulse Width, $t_{MRW}$ | 3.3<br>5.0 | 17.0<br>13.0 | | | | ns | 2 |
| $t_{rec}$ | Recovery Time, $t_{MRSIH}$ $\overline{MR}$ to SI | 3.3<br>5.0 | 7.0<br>4.0 | | | | ns | 2 |
| $t_w$ | SO Pulse Width, $t_{SOH}$ HIGH | 3.3<br>5.0 | 4.5<br>2.0 | | | | ns | 4, 7 |
| $t_w$ | SO Pulse Width, $t_{SOL}$ LOW | 3.3<br>5.0 | 12.5<br>9.0 | | | | ns | 4, 7 |

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

## AC Characteristics

| Symbol | Parameter | Vcc* (V) | 74ACT $T_A = +25°C$, $C_L = 50$ pF | | | 54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF | | 74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF | | Units | Fig. No. |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Max | Min | Max | | |
| $t_{PLH}$, $t_{PHL}$ | Propagation Delay, $t_{IR}$ SI to IR | 5.0 | 1.0 | 6.5 | 11.0 | 1.0 | 14.0 | 1.0 | 12.0 | ns | 1 |
| $t_{PLH}$ | Propagation Delay, $t_{IHF}$ SI to >HF | 5.0 | 1.0 | 10.5 | 17.0 | 1.0 | 21.5 | 1.0 | 19.5 | ns | 1 |
| $t_{PHL}$ | Propagation Delay, $t_{IF}$ SI to Full Condition | 5.0 | 1.0 | 10.5 | 16.5 | 1.0 | 21.5 | 1.0 | 19.5 | ns | 1 |
| $t_{PLH}$ | Propagation Delay, $t_{IE}$ SI to Not Empty | 5.0 | 1.0 | 10.0 | 15.5 | 1.0 | 19.5 | 1.0 | 17.5 | ns | 1 |
| $t_{PLH}$ | Propagation Delay, $t_{IOR}$ SI to OR | 5.0 | 1.0 | 10.5 | 16.5 | 1.0 | 21.5 | 1.0 | 19.0 | ns | 1 |
| $t_{PLH}$ | Recovery Time, $t_{MRIRH}$ $\overline{MR}$ to IR | 5.0 | 13.5 | 8.5 | | 17.5 | | 15.5 | | ns | 2 |
| $t_{PHL}$ | Recovery Time, $t_{MRORL}$ $\overline{MR}$ to OR | 5.0 | 25.5 | 16.5 | | 32.5 | | 29.0 | | ns | 2 |
| $t_{PHL}$ | Recovery Time, $t_{MRO}$ $\overline{MR}$ to Full Flag | 5.0 | 14.0 | 9.0 | | 17.5 | | 16.0 | | ns | 2 |
| $t_{PHL}$ | Recovery Time, $t_{MRE}$ $\overline{MR}$ to HF Flag | 5.0 | 27.5 | 17.5 | | 34.0 | | 30.5 | | ns | 2 |
| $t_{PHL}$ | Recovery Time, $t_{MRONL}$ $\overline{MR}$ to $O_n$, LOW | 5.0 | 15.0 | 9.0 | | 18.5 | | 17.0 | | ns | 2 |
| $t_w$ | IR Pulse Width, $t_{IP}$ | 5.0 | 43.0 | 28.0 | | 58.5 | | 51.5 | | ns | 3 |
| $t_w$ | HF Pulse Width, $t_{3F}$ | 5.0 | 46.5 | 30.0 | | 64.5 | | 56.0 | | ns | 3 |
| $t_{PHL}$, $t_{PLH}$ | Propagation Delay, $t_D$ SO to Data Out | 5.0 | 1.0 | 18.5 | 29.5 | 1.0 | 38.0 | 1.0 | 34.5 | ns | 4 |
| $t_{PHL}$ | Propagation Delay, $t_{OHF}$ SO to <HF | 5.0 | 1.0 | 8.5 | 13.5 | 1.0 | 17.5 | 1.0 | 15.5 | ns | 4 |
| $t_{PLH}$ | Propagation Delay, $t_{OF}$ SO to Not Full | 5.0 | 1.0 | 12.5 | 19.5 | 1.0 | 24.0 | 1.0 | 22.0 | ns | 4 |
| $t_{PLH}$, $t_{PHL}$ | Propagation Delay, $t_{OR}$ SO to OR | 5.0 | 1.0 | 7.0 | 11.5 | 1.0 | 14.5 | 1.0 | 13.5 | ns | 4 |
| $t_{PLH}$ | Propagation Delay, $t_{OE}$ SO to Empty | 5.0 | 1.0 | 9.5 | 15.5 | 1.0 | 19.5 | 1.0 | 17.5 | ns | 4 |

*Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

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**AC Characteristics, cont'd**

| Symbol | Parameter | Vcc* (V) | 74ACT $T_A = +25°C$ $C_L = 50$ pF | | | 54ACT $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF | | 74ACT $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF | | Units | Fig. No. |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Max | Min | Max | | |
| $t_{PHL}$, $t_{PLH}$ | Propagation Delay, $t_{OD5}$ SI to New Data Out | 5.0 | 1.0 | 19.0 | 30.5 | 1.0 | 38.5 | 1.0 | 35.5 | ns | 1, 5 |
| $t_{PLH}$ | Propagation Delay, $t_{X1}$ SI to HF | 5.0 | 1.0 | 10.0 | 16.0 | 1.0 | 19.5 | 1.0 | 18.0 | ns | 5 |
| $t_{PLH}$ | Propagation Delay, $t_{DOF}$ OR HIGH to Data Out | 5.0 | 1.0 | -11.5 | -8.5 | 1.0 | -12.5 | 1.0 | -11.5 | ns | 5 |
| $t_{PLH}$ | Fall-Through Time, $t_{FTO}$ SI to OR | 5.0 | 1.0 | 13.5 | 21.0 | 1.0 | 26.0 | 1.0 | 24.0 | ns | 5 |
| $t_w$ | OR Pulse Width, $t_{OP}$ | 5.0 | 26.0 | 17.0 | | 35.0 | | 30.5 | | ns | 5 |
| $t_w$ | HF Pulse Width, $t_{X3}$ | 5.0 | 30.5 | 20.5 | | 41.5 | | 36.5 | | ns | 5 |
| $t_{PLH}$ | Fall-Through Time, $t_{FT}$ SO to IR | 5.0 | 1.0 | 15.0 | 23.5 | 1.0 | 34.0 | 1.0 | 30.5 | ns | 3 |
| $t_{PZL}$ | Output Enable $\overline{OE}$ to On | 5.0 | 1.0 | 6.5 | 11.0 | 1.0 | 13.5 | 1.0 | 12.0 | ns | 3-8 |
| $t_{PLZ}$ | Output Disable $\overline{OE}$ to On | 5.0 | 1.0 | 5.0 | 8.5 | 1.0 | 10.0 | 1.0 | 9.5 | ns | 3-8 |
| $t_{PZH}$ | Output Enable $\overline{OE}$ to On | 5.0 | 1.0 | 7.0 | 12.0 | 1.0 | 14.5 | 1.0 | 13.0 | ns | 3-7 |
| $t_{PHZ}$ | Output Disable $\overline{OE}$ to On | 5.0 | 1.0 | 7.0 | 12.0 | 1.0 | 13.5 | 1.0 | 13.0 | ns | 3-7 |
| $f_{SI}$ | Maximum SI Clock Frequency | 5.0 | 55 | 85 | | 40 | | 45 | | MHz | 1 |
| $f_{SO}$ | Maximum SO Clock Frequency | 5.0 | 42 | 60 | | 30 | | 35 | | MHz | 4 |
| $f_{BO}$ | Maximum Clock Frequency SO Burst Mode | 5.0 | 42 | 65 | | 30 | | 35 | | MHz | 7 |
| $f_{BI}$ | Maximum Burst-In Clock | 5.0 | 55 | 85 | | 40 | | 45 | | MHz | 6 |

*Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

## AC Operating Requirements

| Symbol | Parameter | Vcc* (V) | 74ACT | | 54ACT | 74ACT | Units | Fig. No. |
|---|---|---|---|---|---|---|---|---|
| | | | $T_A = +25°C$ $C_L = 50$ pF | | $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF | $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF | | |
| | | | Typ | Guaranteed Minimum | | | | |
| $t_w$ | SI Pulse Width, $t_{SIH}$ HIGH | 5.0 | 1.5 | 3.0 | 3.5 | 3.5 | ns | 1, 6 |
| $t_w$ | SI Pulse Width, $t_{SIL}$ LOW | 5.0 | 1.5 | 3.0 | 3.0 | 3.0 | ns | 1, 6 |
| $t_s$ | Setup Time, HIGH or LOW, $D_n$ to SI | 5.0 | 1.0 | 3.5 | 4.0 | 4.0 | ns | 1 |
| $t_h$ | Hold Time, HIGH or LOW, $D_n$ to SI | 5.0 | 1.5 | 3.5 | 4.5 | 4.0 | ns | 1 |
| $t_w$ | $\overline{MR}$ Pulse Width, $t_{MRW}$ | 5.0 | 13.0 | 20.0 | 26.0 | 24.5 | ns | 2 |
| $t_{rec}$ | Recovery Time, $t_{MRSIH}$ $\overline{MR}$ to SI | 5.0 | 4.5 | 7.5 | 9.0 | 8.5 | ns | 2 |
| $t_w$ | SO Pulse Width, $t_{SOH}$ HIGH | 5.0 | 2.0 | 3.5 | 5.0 | 4.5 | ns | 4, 7 |
| $t_w$ | SO Pulse Width, $t_{SOL}$ LOW | 5.0 | 9.0 | 14.0 | 19.0 | 17.0 | ns | 4, 7 |

*Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

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## Capacitance

| Symbol | Parameter | 54/74AC | Units | Conditions |
|---|---|---|---|---|
| | | Typ | | |
| $C_{IN}$ | Input Capacitance | 4.5 | pF | $V_{CC} = 5.5$ V |