A Low-Power, Low-Voltage WBAN-Compatible Sub-Sampling PSK Receiver in 65 nm CMOS

Jiao Cheng, *Member, IEEE*, Nan Qi, *Member, IEEE*, Patrick Yin Chiang, *Member, IEEE*, and Arun Natarajan, *Member, IEEE*

***Abstract*—A PSK receiver (RX) is proposed that employs a digital-intensive architecture based on sub-sampling, Q-enhancement, and digital IF to enable low-power (1.3 mW) and low-voltage (0.6 V) operation. Implemented in 65 nm CMOS, this work is compatible with the IEEE 802.15.6 (WBAN) narrowband physical layer specification and achieves -91 dBm and -96 dBm sensitivity at 10^{-3} BER for $\pi/4$-DQPSK and $\pi/2$-DBPSK modulation respectively. The proposed highly digital architecture and supply voltage scaling lead to a 3x improvement in RX energy efficiency and minimize silicon area consumption ($\sim$ 0.35 mm^2 in 65 nm CMOS) while achieving state-of-the-art sensitivity. While this implementation focuses on WBAN demodulation, the proposed architecture and circuit techniques are generally applicable to RX targeting ultra-low power consumption for sensor networks.**

***Index Terms*—$\pi/2$-DBPSK, $\pi/4$-DQPSK, CMOS, digital IF, digital RF, low power, low voltage, narrowband, PSK, Q-enhancement, receiver (RX), sub-sampling, WBAN.**

I. Introduction

THE IEEE 802.15.6 Wireless Body Area Network (WBAN) standard focuses on low power, short range wireless links for biomedical applications [1]. Notably, the WBAN standard aims to achieve reliable wireless data links around and/or inside a human body to enable a variety of healthcare services. The targeted application space implies that most WBAN radios will be battery-powered and long operating lifetime requirements motivate minimization of radio power consumption. Furthermore, button cell lithium batteries rated at 3.0 Volts typically have low peak current delivery capacity (e.g., 20 mA for CR2032). This makes it desirable to reduce peak RX power consumption, thereby increasing the peak current and power budget for other system components such as bio-sensors and potentially enabling increased local processing for system-on-chip (SoC) solutions. In addition to the peak and average power consumption, the active die area of the implementation must also be minimized to enable low-cost ICs for disposal/ubiquitous WBAN sensor deployment.

Manuscript received May 28, 2014; revised August 16, 2014; accepted September 25, 2014. Date of publication October 27, 2014; date of current version November 20, 2014. This paper was approved by Guest Editor Sven Mattisson.

The authors are with the Department of Electrical Engineering and Computer Science, Oregon State University, Corvallis, OR 97331 USA (e-mail: chengji@onid.oregonstate.edu).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/JSSC.2014.2362840

The potential of low-power wireless sensors for biomedical and internet-of-things applications has led to extensive circuit-level and system-level efforts to lower wireless RX power consumption [2]–[16]. Super-regenerative architectures have been extensively used to achieve ultra-low power consumption in RX, leveraging low hardware complexity [2]–[6]. While power consumption of $\sim 350\ \mu$W has been reported for 2 Mb/s 2.4 GHz RX in CMOS [5], super-regenerative RX are only applicable to relatively simple modulation schemes, such as OOK and BFSK. However, the WBAN standards mandate more advanced differential phase-shift-keying (DPSK) for higher spectrum efficiency. Furthermore, super-regenerative RX does not provide sufficient adjacent channel rejection (ACR) for close channel spacing (e.g., 1 MHz in WBAN).

Sliding-IF heterodyne architecture can also lower power consumption, particularly in local oscillation (LO) generation circuits by avoiding I/Q LO generation at RF [7]–[11]. However, only moderate reductions can be achieved since LO frequency for the first mixer must still be close to RF for low intermediate frequency (IF) operation.

Current reuse approaches that stack analog building blocks (e.g., LNA, mixers and filters) on top of each other to minimize biasing current have also been explored for low-power radios [12]–[14]. However, this increases the required supply voltage (usually higher than 1.2 V), which either increases digital baseband power consumption or introduces extra power management circuits if the digital circuits are operated from a different lower-voltage supply.

The power consumption can be significantly reduced by adopting an extremely low supply voltage (e.g., 0.3 V in [15], [16]). Since the lower supply voltage leads to insufficient headroom, inter-stage signal transfer is often achieved through transformer coupling, resulting in a large active die area. Additionally, a low-voltage analog-intensive approach does not scale the peak current which remains high (~ 5 mA in [15], [16]).

In this paper, we propose a WBAN-compatible digital-intensive RX architecture that leverages sub-sampling, Q-enhancement and digital IF to simultaneously achieve low power, low voltage, low peak current, and small active die area [17]. System design considerations for the proposed sub-sampling architecture are introduced in Section II. The RX topology and detailed circuit design of key building blocks are discussed in Section III. Measurement results of the sub-sampling RX prototype are shown in Section IV, validating the proposed architecture. Finally, conclusions are drawn in Section V based on analysis and experiments.

II. Proposed Sub-Sampling RX

As described in Section I, RF and analog architecture and circuit techniques can substantially reduce RX power consumption. However such techniques are limited by the power consumption of the LO-generation circuits and the analog IF. For example, in [10], a sliding-IF RX topology and push-pull mixers lead to state-of-the-art $\sim 3.8\,\mathrm{mW}$ power consumption. Notably, the circuits related to frequency translation, including LO generation and high frequency mixing, consume over 50% of the total power budget. Furthermore, the analog IF stage also consumes a significant share ($\sim 25\%$) of the total power. Achieving further reductions in power consumption for sub-1 mW RX operation requires a holistic approach that includes architectures and circuits to minimize analog and high-frequency building blocks. In this work, we investigate sub-sampling in the RF frontend to reduce power in the frequency translation circuits, and focus on a digital IF scheme that takes advantage of advanced CMOS nodes and uses standard digital place-and-route synthesis methodology to replace analog IF signal processing.

A. Low Noise Figure (NF) Operation for Sub-Sampling RX

As shown in Fig. 1(a), when a signal is sampled at the frequency f_S, the spectrum around harmonics of f_S (Nf_S , where N is an integer) are translated to low IF, along with the desired signal. As long as f_S is larger than twice the sampled signal bandwidth f_{BW}, aliasing can be avoided. For narrow band RX, the signal bandwidth f_{BW} is much smaller than the carrier frequency $f_{RF}(f_{BW} \ll f_{RF})$ and hence f_S satisfying non-overlapping criterion ($f_S > 2f_{BW}$) can be much lower than f_{RF}. However, selecting $f_S \ll f_{RF}$ leads to frequency translation from the noise bands at image frequency ($f_{IMi}, i = 1, 2, 3, \ldots$) with respect to each harmonic of f_S. This well-known noise folding phenomena in sub-sampling can seriously degrade the overall noise figure [18]. For this reason, sub-sampling is seldom employed at RF to perform the first downconversion and is more commonly used for IF mixing which only provides moderate reduction in power consumption [14], [19], [20].

This degradation due to noise folding can be reduced by placing a highly selective filter at RF that reduces the noise from harmonics of f_S, as shown in Fig. 1(b). The system NF can be calculated as a function of RF filter quality factor, Q, and sub-sampling frequency f_S as shown in Fig. 2(a). Assuming that the gain stage, $G(\omega)$, preceding the sample and hold (S/H) introduces 2nd order filtering with a quality factor Q, the cascaded system noise factor can be calculated as

$$\begin{aligned} F_{\text{cascaded}} &= \frac{\frac{S_{\text{in}}}{N_{\text{in}}}}{\frac{S_{\text{out}}}{N_{\text{out}}}} = \frac{1}{G(\omega_0)} \\ &\quad \cdot \frac{N_{\text{in}} \sum_{k=0}^{\infty} G\left(\omega_0 \pm k \cdot \frac{f_S}{2}\right) + \frac{N_{G(\omega_0)}}{G(\omega_0)} \sum_{k=0}^{\infty} G\left(\omega_0 \pm k \cdot \frac{f_S}{2}\right)}{N_{\text{in}}} \\ &= \frac{N_{\text{in}} G(\omega_0) + N_{G(\omega_0)}}{N_{\text{in}} G(\omega_0)} \cdot \sum_{k=0}^{\infty} \frac{G\left(\omega_0 \pm k \cdot \frac{f_S}{2}\right)}{G(\omega_0)} \\ &= F_{G(\omega_0)} \sum_{k=0}^{\infty} \frac{G\left(\omega_0 \pm k \cdot \frac{f_S}{2}\right)}{G(\omega_0)} \end{aligned} \tag{1}$$

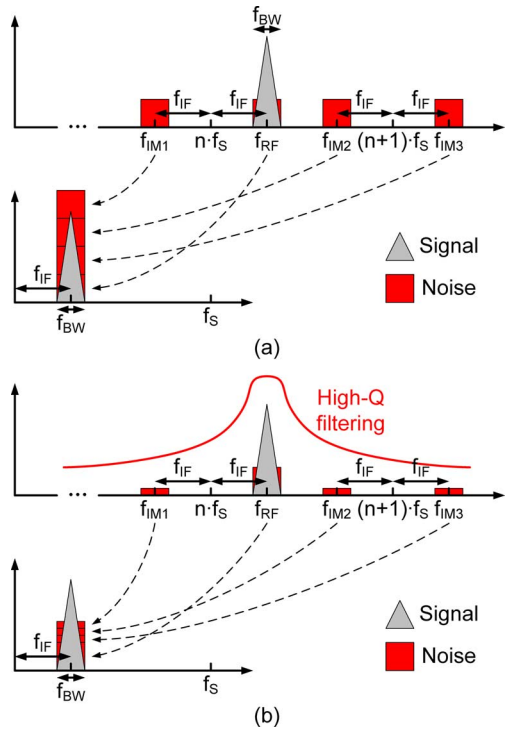


Fig. 1. Noise folding in sub-sampling (a) without and (b) with preceding high-Q filtering.

where $N_{G(\omega_0)}$ denotes the noise spectrum density contributed by $G(\omega)$ at frequency ω_0, and $F_{G(\omega_0)}$ denotes the noise factor of $G(\omega)$ at frequency ω_0. The expression for noise factor in (1) assumes a) spectrum of input noise and the spectrum of the noise contributed by the gain stage before filtering are flat across the frequency of interest; b) the S/H gain is 0 dB; and c) that the IF equals $f_S/4$ (discussed further in Section II.C). As we can see in (1), the cascaded system noise factor consists of the sum of the scaled noise factor of $G(\omega)$ at ω_0, where the scaling factor is the normalized gain at all image frequencies. The relationship among NF, f_S and Q, based on (1), is shown graphically in Fig. 2(b). This figure indicates that low NF operation at 2.4 GHz RF can be achieved using sub-sampling RX for sampling frequency f_S higher than 150 MHz if filter Q is larger than 100. While such high-Q filters can be achieved using external or co-integrated components such as BAW or FBAR resonators [19], [21], this work focuses on fully integrated RX in a commercial CMOS technology with no external high-Q filters. Since the Q of on-chip RF inductors in CMOS technologies is < 20 even with thick metal layers in the backend, active Q-enhancement in the LNA is utilized in this work to achieve the desired narrowband filtering at RF.

Q-enhancement technique intrinsically degrades the front-end linearity, therefore limiting the RX large signal performance. However, for typical short-range low-power communication, the transmitter (TX) output power is relatively low (< 0 dBm) and therefore adjacent channel interferers can be tolerated while achieving targeted BER with linearity degradation caused by Q-enhancement. For example, the WBAN standard [1] specifies an adjacent channel power of 9 dB with received signal amplitude 3 dB higher than reference sensitivity

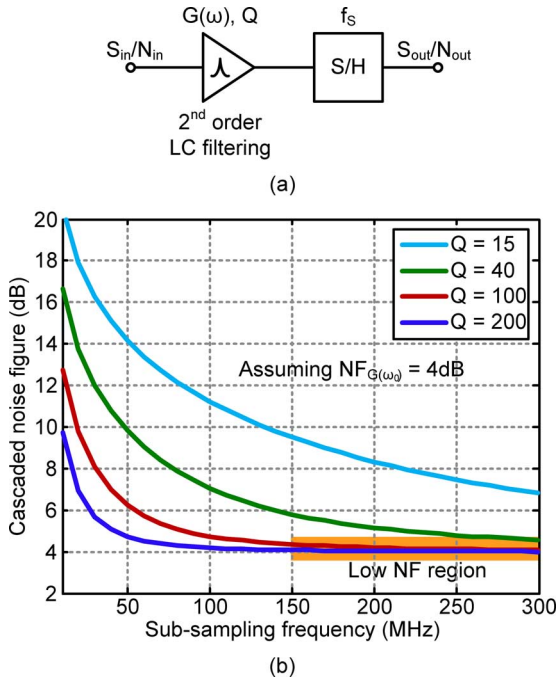


Fig. 2. (a) Block diagram of the cascaded filtering and sub-sampling stages. (b) Cascaded noise figure versus sub-sampling frequency for different filter Q with 2.4 GHz carrier.

and as shown in Section IV, the proposed RX achieves targeted 10^{-3} BER for such adjacent channel power.

B. RF Front-End Frequency Tunability

The Q-enhanced RF front-end should have sufficient frequency tunability to closely align center frequency with the RF carrier, to avoid reduction or variation in gain. As shown in Fig. 3, if the LSB of RF front-end frequency tuning is f_L, the signal carrier frequency f_C will be $f_L/2$ off with respect to the front-end center frequency f_0 in the worst case. The worst-case gain reduction due to an offset between RF carrier and center frequency can be calculated as

$$\Delta G_Q = G_{Q,1} - G_{Q,2} = G_Q\left(f_O\right) - G_Q\left(f_O - \frac{f_L}{2}\right) \quad (2)$$

where

$$G_Q\left(f\right) = \frac{1}{\sqrt{Q^2\left(\frac{f}{f_O} - \frac{f_O}{f}\right)^2 + 1}}$$

denotes the normalized gain profile of the 2nd-order LC filter and f_L is the LSB of RF front-end frequency tuning. The gain variation across the channel bandwidth can also be calculated as

$$\begin{aligned}&\Delta G_{CH}\\ &= G_{Q,3} - G_{Q,4}\\ &= G_Q\left(f_O - \frac{f_L}{2} + \frac{f_{CH}}{2}\right) - G_Q\left(f_O - \frac{f_L}{2} - \frac{f_{CH}}{2}\right)\end{aligned} \quad (3)$$

where f_{CH} is the channel bandwidth. Fig. 4(a) and (b) graphically represent (2) and (3), respectively, demonstrating that 1 MHz resolution in frequency tuning is sufficient to ensure

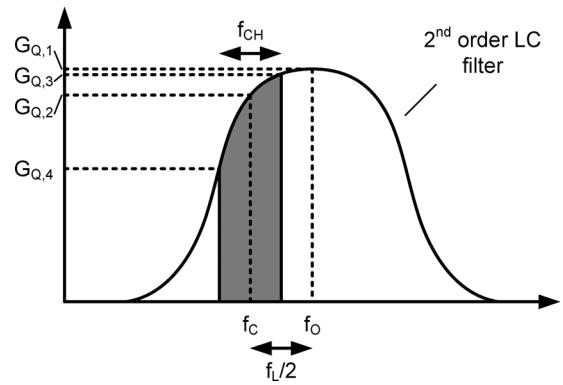


Fig. 3. Gain reduction and variation in high-Q RF front-end.

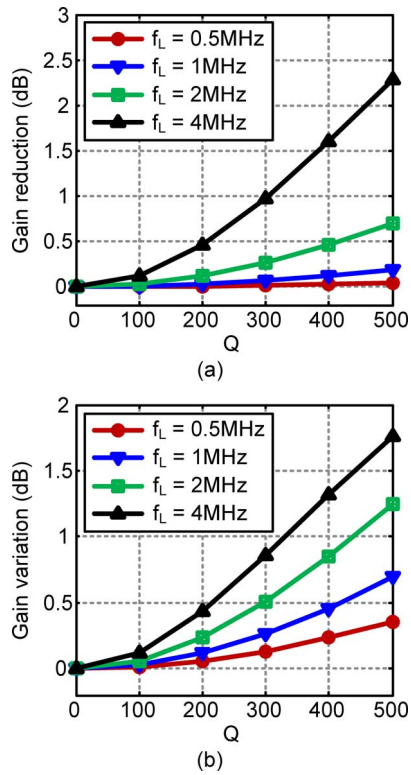


Fig. 4. (a) Gain reduction and (b) gain variation versus Q for different frequency tuning LSB.

less than 0.5 dB reduction and variation in gain for filter Q in the range of 50 to 400 that are of interest in this work.

C. Frequency Plan

Fig. 5 shows the frequency plan of the proposed sub-sampling RX. The received signal is filtered and amplified at RF by the high-Q front-end, and then translated to IF by the sub-sampling mixer. Subsequent quadrature down-conversion is achieved in the digital domain. Selecting an IF frequency that is $f_S/4$, where f_S is the sampling frequency, results in a sampled quadrature wave at IF where

$$\begin{aligned}\cos 2\pi f_{IF} \cdot \frac{N}{f_S} &= \cos 2\pi \frac{f_S}{4} \cdot \frac{N}{f_S}\\ &= \cos\frac{\pi}{2} \cdot N = \{1, 0, -1, 0, \ldots\},\end{aligned}$$

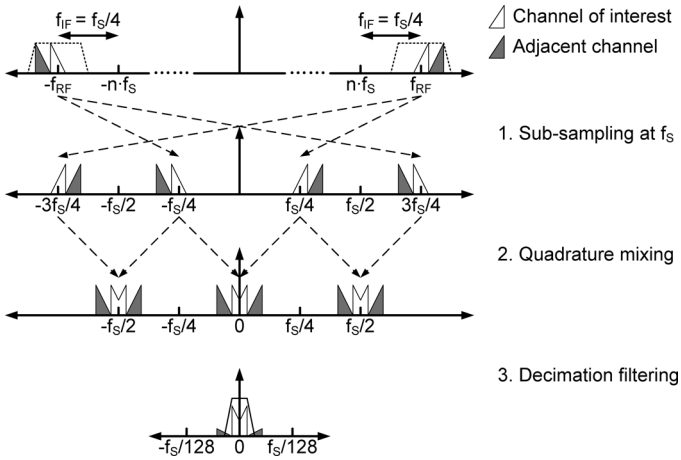


Fig. 5. Frequency plan of the proposed sub-sampling RX.

$$\begin{aligned} N &= \{0,1,2,3,\ldots\} \\ \sin 2\pi f_{IF} \cdot \frac{N}{f_S} &= \sin 2\pi \frac{f_S}{4} \cdot \frac{N}{f_S} \\ &= \sin \frac{\pi}{2} \cdot N = \{0,1,0,-1,\ldots\}, \\ N &= \{0,1,2,3,\ldots\}. \end{aligned} \tag{4}$$

According to (4), the digital quadrature mixing operation at IF assigns odd (even) quantized samples to I (Q) channel. While this mixing scheme implies an equivalent sampling scheme of $f_S/2$, it facilitates the design of the interface between the high-Q LNA and the S/H circuit (discussed in detail in Section III.A). Decimation filtering of the digital quadrature mixer output attenuates adjacent channel interference. The effective sampling rate of the decimation filter output is 4.92 MHz, oversampling the baseband signal by a factor of 8, facilitating baseband signal processing.

D. ADC Resolution

The WBAN standard requires 9 dB ACR for $\pi/4$-DQPSK modulation (1 MHz channel spacing) [1]. Fig. 6 shows the relative signal and noise power level for ACR measurements according to the WBAN standard. In Fig. 6, P_S denotes signal power, P_A denotes adjacent channel power, P_Q denotes the ADC quantization noise level, P_N denotes the noise contributed by the input source and the whole RX chain except for the ADC quantization noise, and P_T is the overall noise floor (sum of P_Q and P_N). SNR_{DEM} is the SNR required by the baseband demodulator to achieve 10^{-3} bit error rate (BER). The WBAN standard specifies P_S to be 3 dB higher than the sensitivity when ACR is measured. Therefore, at 10^{-3} BER for this signal power, overall noise floor P_T is 3 dB higher than P_N. This implies $P_Q = P_N$, and hence

$$SQNR_{\mathrm{ADC}} = ACR + SNR_{\mathrm{DEM}} + 3. \tag{5}$$

System simulations were performed to evaluate SNR_{DEM}, resulting in ~ 17 dB target, implying that $SQNR_{\mathrm{ADC}} = 29$ dB. Therefore, 4.5 bit ADC resolution is targeted for this implementation.

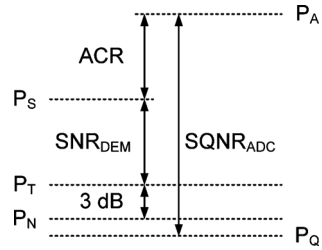


Fig. 6. Relative signal and noise power level for ACR calculation.

Early digitization in the RX chain reduces the analog components and leverages the standard digital synthesis and place-and-route methodology, resulting in lower power consumption, smaller die area and fewer design iterations, but requires sophisticated design to avoid extra power penalty due to the increased sampling frequency. In this work, the quantizer can be conveniently inserted after the S/H stage to leverage the 150 MHz sampling frequency required for low NF operation. Since the S/H oversamples the baseband signal by a factor of 128, an over-sampled, low-resolution ADC scheme is adopted since only 1 bit quantization is necessary at 150 MHz to achieve 4.5 bit equivalent ADC resolution, resulting in negligible power overhead and simplified ADC design.

III. Circuit Design

A. RX Topology

The proposed RX architecture is depicted in Fig. 7. The RX RF signal is first amplified and filtered by the Q-enhancement LNA, then sampled by the S/H stage. The sampled signal is provided to a dynamic comparator that performs 1 bit A-to-D conversion. The quantized signal is then fed into the digital IF and baseband circuit for further processing. The local oscillation frequency is chosen to be 309.7 MHz satisfying the noise folding suppression described in Fig. 2(b) and (1). It must be noted that the sampling rate ensures that the baseband is oversampled by a factor of 128. The only purely analog component in the RX chain in Fig. 7 is the Q-enhancement LNA, while the remaining circuits operate dynamically and do not consume static power. Furthermore, the digital-intensive architecture allows the whole IF and baseband to be implemented using standard digital synthesis and place-and-route methodology, simplifying design and layout. As described in Section II.C, the choice of $f_{IF} = f_S/4$, simplifies the IF digital mixing with alternate samples. Therefore, two identical samplers are implemented at the LNA output and turned on alternatively which separates I and Q samples. An important benefit of this approach is that it ensures that the Q-enhancement LNA always see a constant load impedance, which is important to keep the resonance frequency of a high-Q tank constant. The system noise contribution break down is shown in Table I.

B. Q-Enhancement LNA

The LNA employs differential inductively degenerated common source architecture as shown in Fig. 8. Capacitors C_1 through C_4 are added to form a positive feedback with the cascaded transistors M_3 and M_4, resulting in a negative

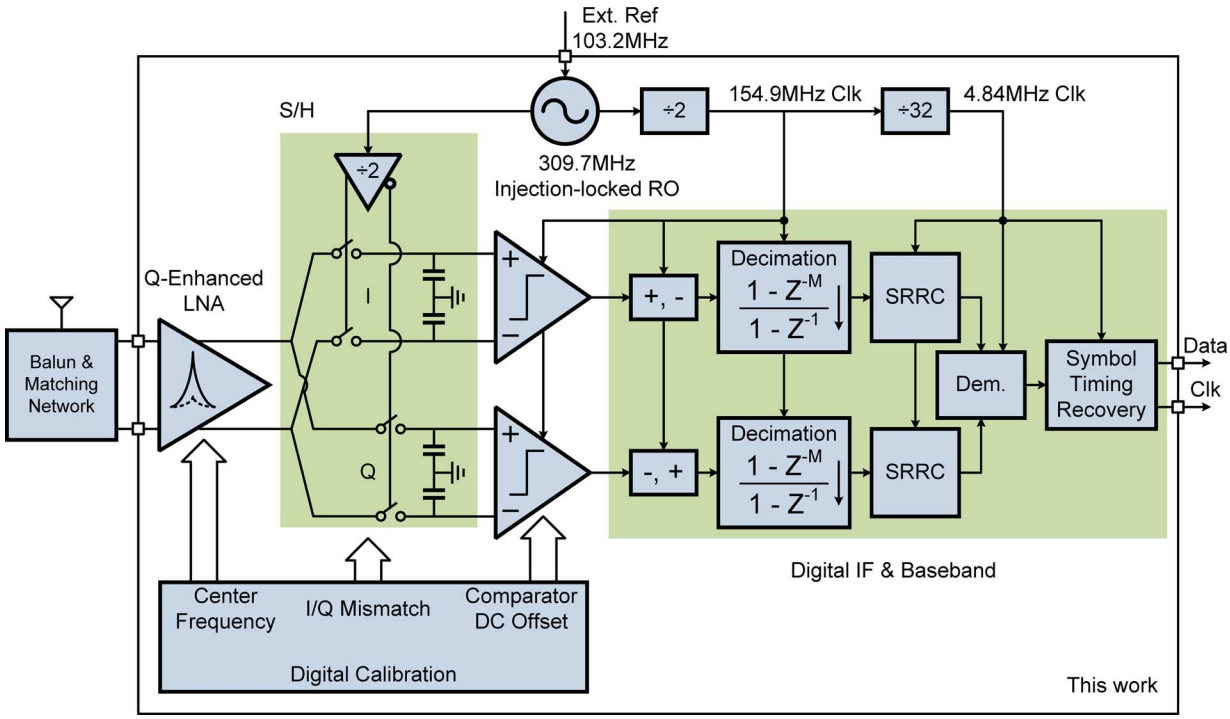


Fig. 7. System block diagram of the proposed sub-sampling RX .

TABLE I
SYSTEM NOISE CONTRIBUTION BREAK DOWN

Components	Noise figure or integrated output noise
Q-enhancement LNA	4 dB
S/H	32 μV_{rms}
1-b Comparator	44 μV_{rms}

resistance appearing in parallel with the tank, which cancels part of the intrinsic tank resistance and enhances effective tank I. As mentioned in Section II.B, high-Q operation must be accompanied by fine frequency resolution to ensure that all channels can be received. In this work, coarse tuning is achieved using 7 bit binary-to-thermometer coded capacitor bank ensuring monotonicity and linearity [22]. Another 3 bit binary-to-thermometer coded bank provides fine frequency control. The circuit of a single unit switch capacitor in the coarse tuning bank is shown in Fig. 8. M_8 through M_{11} are added to set the DC voltage of the drain/source of M7, resulting in minimum turn-on resistance and maximum turn-off resistance for M_7. A voltage DAC with 44 bit thermometer tuning code controls the bias current of the Q-enhancement LNA, enabling a current tuning range from 0.66 mA to 3 mA with a worst-case tuning step of 90 uA to enhance Q up to 400 (discussed further in following paragraphs). Capacitors C_{in}, inductors L_{in} in matching network and the single-to-differential balun are implemented off-die.

Variations across process, voltage and temperature (PVT) impact the resonance frequency and the equivalent Q of the LNA output tank. Therefore a frequency and Q-enhancement calibration scheme (shown in Fig. 9) is necessary for practical operation to facilitate high-Q operation. In this calibration scheme, transistors M_5 and M_6 are turned on initially to short the LNA input and shield interference from external signals during calibration. Following this, the LNA bias current is set to its maximum value, increasing positive feedback leading to oscillation. The oscillation frequency is sensed by comparing it to the reference frequency using frequency dividers and counters, and the resonant tank is tuned to the targeted center frequency by adjusting the coarse and fine tuning code of the capacitor banks. After center-frequency calibration is complete, the bias current is decreased until the amplifier stops oscillating, which is also detected using the counter. This is the so-called critical current for an oscillator. Finally, the operating bias current is set as a fraction of the critical current according to the (9).

Based on the small signal model of the positive feedback loop consisting of M_3, C_1 and C_2 shown in Fig. 10(a), the negative admittance shown in Fig. 10(c) offered by the Q-enhancement circuit is obtained as

$$G_N = -\frac{g_{m3}C_1C_2}{2(C_1+C_2)^2} = -k(I_{\text{bias}})^n,$$
$$k = \frac{C_1C_2}{2(C_1+C_2)^2}\cdot\sqrt{2\mu C_{ox}\left(\frac{W}{L}\right)_3} \quad (6)$$

where n varies from 0.6 to 0.4 when the transistor operates from moderate inversion to strong inversion in this technology. When the bias current reaches the critical current value, the tank's intrinsic loss G_T should equal the absolute value of the negative admittance in (6) as

$$G_T = \frac{1}{Q_T\omega L} = k(I_{\text{crit}})^n \quad (7)$$

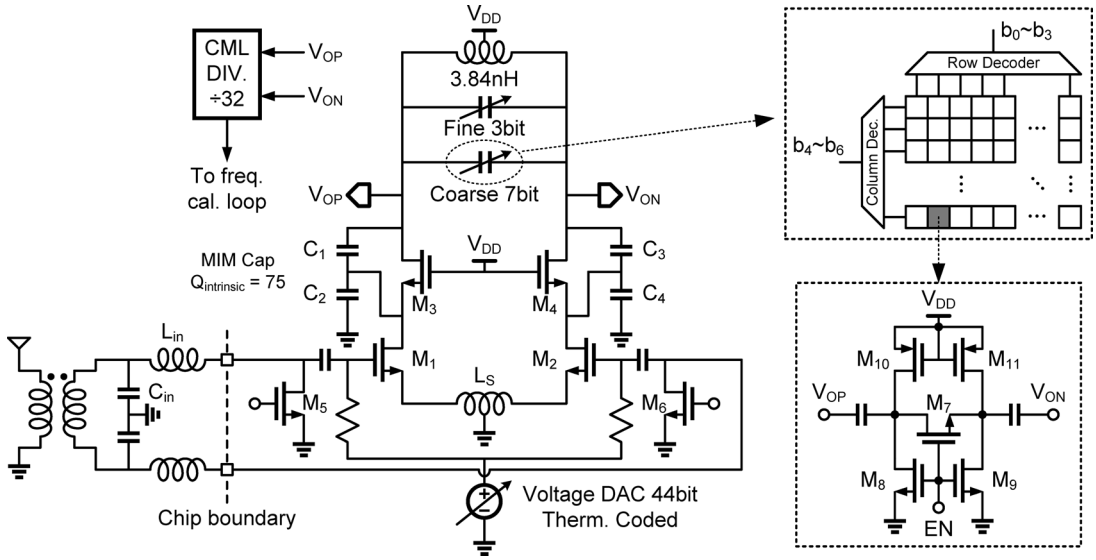


Fig. 8. Schematic of the Q-enhancement LNA.

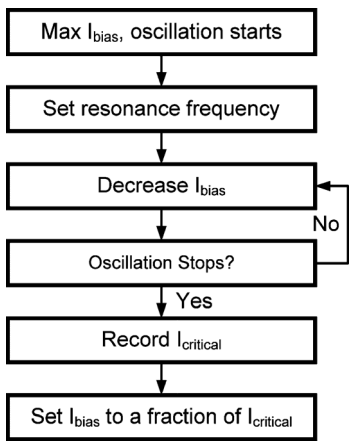


Fig. 9. LNA output resonance and equivalent Q calibration steps.

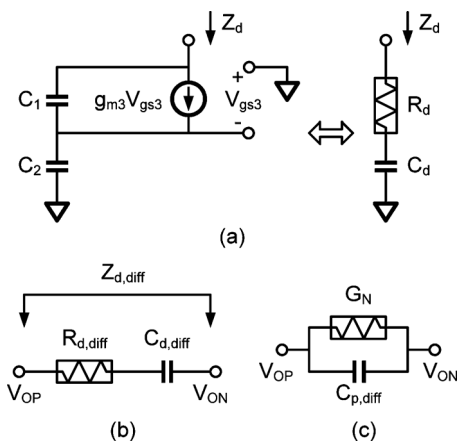


Fig. 10. (a) Small-signal circuit of the single-end positive feedback loop; differential impedance of the positive feedback loop in (b) series and (c) parallel.

where Q_T indicates the intrinsic tank quality factor. Thus, with the bias current set to be a fraction of the critical current as $I_{\rm bias} = mI_{\rm critical}$, the equivalent Q of the LNA output tank can be derived as

$$Q_{eq} = \frac{1}{(G_T + G_N)\,\omega L} = \frac{1}{\omega L} \cdot \frac{1}{k(I_{\rm crit})^n - k(mI_{\rm crit})^n} = \frac{Q_T}{1 - m^n} \tag{8}$$

which can be rearranged as

$$m = \frac{I_{\rm bias}}{I_{\rm critical}} = \left(1 - \frac{Q_T}{Q_{eq}}\right)^{1/n}. \tag{9}$$

Based on (9), for a simulated Q_T of 15, a bias current which is 93% of the critical current yields an equivalent Q of 400. The worst-case bias current tuning step of 90 uA mentioned in this part earlier is about 4% of simulated critical current, ensuring that Q of 400 can be achieved by appropriate $I_{\rm bias}$ settings.

In (9), Q_T decreases when the temperature increases due to higher ohm loss. However, the transistor biasing current is also higher for the same Q_{eq} with higher temperature. This leads to a smaller n in (9) since the transistor channel inversion is stronger. As a result, the factor m for a certain Q_{eq} remains fairly constant for a wide temperature range. This is validated by simulation results in Fig. 11. Therefore, although the critical current varies with the temperature, this calibration procedure works for a wide temperature range even with a fixed m factor.

The difference in LNA output resonance frequency with switch M_5 off and on must be considered to ensure calibration with M_5 on is valid during actual operation with M_5 off. The admittance looking into the drain of M_1 can be derived using the small-signal circuit shown in Fig. 12 ($C_{\rm par}$ denotes the lumped parasitic capacitance due to M_5 and the pad) as

$$Y_1 = sC_{gd}\left(1 + \frac{g_m}{s^2 g_m L_s C_{gd} + s\left(g_m L_s Y_s + C_{gs}\right) + Y_s}\right) \tag{10}$$

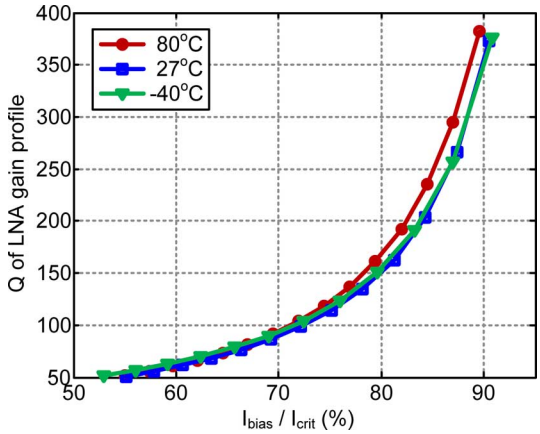


Fig. 11. Simulated Q of LNA gain profile versus $\mathrm{I_{bias}/I_{crit}}$ with temperature variation.

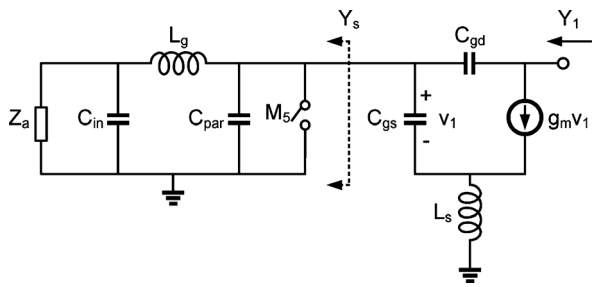


Fig. 12. Small-signal circuit of the input matching network and transistor.

where Y_s is the admittance looking to the left side of $\mathrm{M_5}$ (assuming $\omega^2 L_s C_{gd} \ll 1$, $\omega^2 L_s C_{gs} \ll 1$, and ignoring the channel-length modulation and body effect). When switch $\mathrm{M_5}$ on and off, we have

$$Y_{s,\mathrm{off}} = \frac{1 + sC_{\mathrm{in}} Z_a}{s^2 L_g C_{\mathrm{in}} Z_a + sL_g + Z_a} + sC_{\mathrm{par}}, \quad Y_{s,\mathrm{on}} = \infty. \tag{11}$$

Thus, the difference in Y_1 with switch $\mathrm{M_5}$ on and off is

$$\begin{aligned} \Delta Y_1 &= sC_{gd} \cdot k_n, \\ k_n &= \frac{g_m}{s^2 g_m L_s C_{gd} + s\left(g_m L_s Y_{s,\mathrm{off}} + C_{gs}\right) + Y_{s,\mathrm{off}}}. \end{aligned} \tag{12}$$

Since the magnitude of the k_n is smaller than 5 for typical g_m, L_s, C_{gd}, C_{gs} and $Y_{s,\mathrm{off}}$, and C_{gd} is much smaller than C_2 in Fig. 8, the LNA output resonance frequency variation due to the change of Y_1 can be ignored, ensuring that accurate calibration can be performed with $\mathrm{M_5}$ on.

C. S/H Stage

The holding capacitors at the S/H stage should be large enough to suppress the kT/C noise for low NF, but small enough to accommodate resonance tuning capacitor banks and positive feedback capacitors that are a significant fraction of the total capacitance at the LNA output. For 290 K room temperature, 1 MHz system bandwidth, 40 dB voltage gain and 4dB NF of LNA, 0 dB S/H gain, the amplitude of the noise contributed by the input source and the LNA can be estimated as

$$\begin{aligned} N_{\mathrm{in,LNA}} &= -174\ \mathrm{dBm} + 10\log 10^6\ \mathrm{dB} + 40\ \mathrm{dB} + 4\ \mathrm{dB} \\ &= -70\ \mathrm{dBm} = (100\ \mu\mathrm{V})^2. \end{aligned} \tag{13}$$

The kT/C noise contribution from the S/H switch is

$$N_{kT/C} = \frac{kT}{C_{hold}} \times 2 \times \frac{1}{128} = 0.1 N_{\mathrm{in,LNA}}|_{C=60\ \mathrm{fF}} \tag{14}$$

where the factor 2 indicates that there are two differential holding capacitors and the factor 1/128 is due to digital IF and baseband filtering. Equation (14) indicates the S/H kT/C noise is negligible for a 60 fF holding capacitor.

D. 1-Bit Quantizer

The architecture achieves early low-resolution quantization using a dynamic comparator that performs 1 bit quantization shown in Fig. 13. Since the comparator inputs are driven by the preceding holding capacitors, a two-stage architecture is implemented to isolate the holding capacitors and the regenerative Armstrong latch. As the signal is at IF ($f_{RF} - Nf_S = 77.4$ MHz) when it is quantized, comparator DC offset does not impair signal spectrum after I/Q mixing and low pass filtering in digital domain as long as the offset does not saturate the comparator. However, the offset must be reduced to ensure that RX can detect the targeted -90 dBm signal at RX input. Given the LNA gain of $\sim$ 40 dB, the -90 dBm signal at RF input implies $\sim$ 1 mV signal amplitude at comparator input. In this work, comparator DC offset calibration is implemented with a 1 mV LSB, which yields a 0.5 mV worst-case DC offset residue. A 1000-run Monte Carlo simulation shows a standard deviation of the comparator DC offset of 4.4 mV, therefore a 40 bit thermometer coded current DAC is implemented to cover up to 9-σ of the DC offset variation. With the comparator inputs connected to fixed DC voltages, the following 16 bit accumulator adds up the comparator output through 2^{16} comparisons to calculate the probability of '1's. Since the comparator input-referred noise voltage amplitude satisfies Gaussian distribution for a large number of samples, this probability will reflect the equivalent differential input voltage (i.e., the sum of the input voltage and the input-referred DC offset), and therefore quantify the DC offset residue.

E. Local Oscillator and Clock Generation

Ring oscillators are superior to LC oscillators with respect to die area and power consumption when the oscillation frequency is relatively low. In this work, a 4-stage, cross-coupled, current starved differential ring oscillator is implemented to provide 309.7 MHz local oscillation, as shown in Fig. 14. All delay cells in the oscillator share one top and one tail current source, which can be programmed by the 4 bit current DAC to control the free running frequency. Injection locking is achieved by the NMOS transistor $\mathrm{M_1}$ syncing the delay cell transition with the reference frequency when its gate voltage is high. To make use

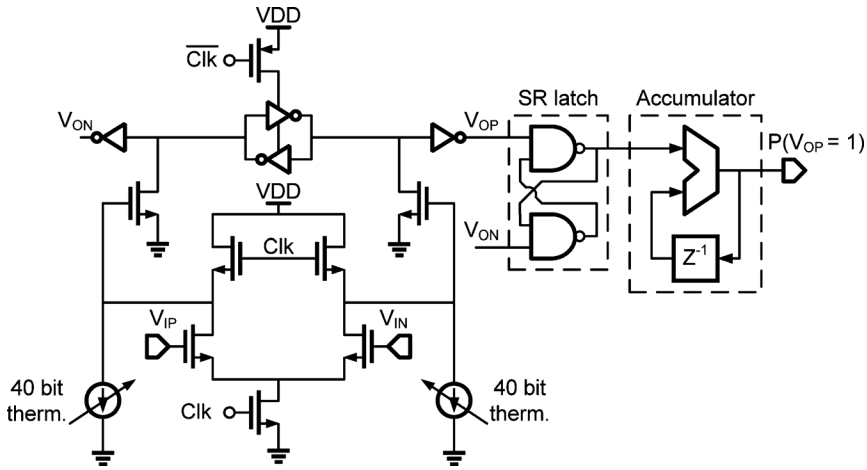


Fig. 13. Schematic of the dynamic comparator performing 1 bit A-to-D conversion.

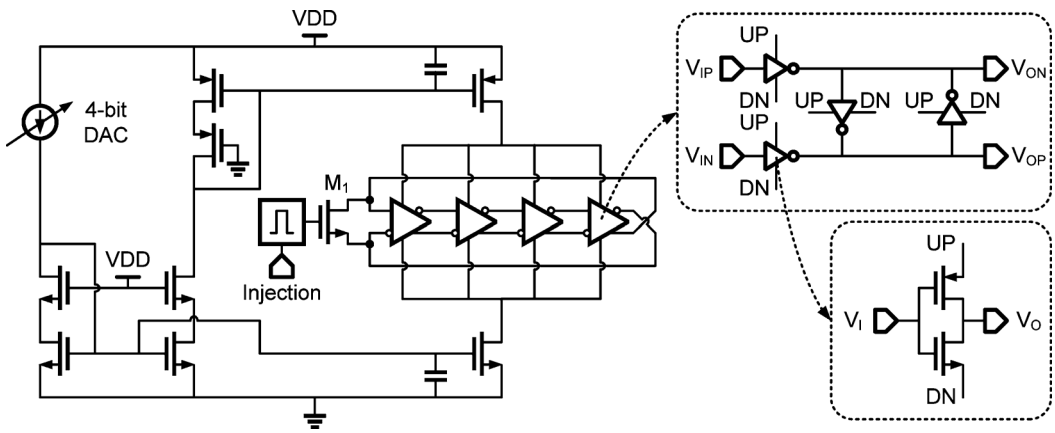


Fig. 14. Schematic of the ring oscillator.

of the 3rd sub-harmonic injection locking with the off-die reference of 103.2 MHz, a pulse generator is inserted to prevent the injection signal from quenching the ring oscillator.

Unlike traditional I/Q RX that have 90° phase shift in I/Q oscillations, I/Q separation in this sub-sampling RX is performed by two clocks with 180° phase difference, generated by a cross-coupled divider, as shown in Fig. 15. SHI and SHQ denote the sampling clock for I channel and Q channel S/H stage, respectively. Phase asymmetry between I/Q sampling clock is trimmed through the tunable delay line inserted in each clock path. QI and QQ denote the clock driving the 1 bit quantizers in I channel and Q channel, respectively. The quantizers are fully reset in the sample phase of the corresponding samplers, minimizing the parasitic capacitance contributed to LNA output.

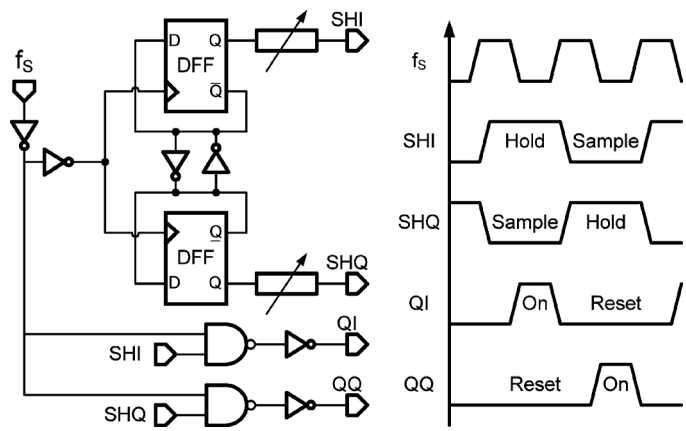


Fig. 15. Schematic and timing diagram of the clock generation circuit.

F. Digital IF and Baseband

Two key building blocks in the digital IF and baseband are highlighted here. Fig. 16(a) shows the block diagram of the modified cascaded integrator-comb filter which performs decimation filtering. The sampling frequency of the quantized samples, 154.9 MHz, leads to a decimation rate of 128 for 500 kHz signal bandwidth in baseband. However, the down-sampling rate in the decimation filter is set to 32 in order to ensure adequate data-transition timing resolution for the symbol timing recovery circuit. This results in a baseband clock frequency of 4.84 MHz, which is 8-times oversampling for 600 kHz symbol rate. The delay in the differentiator is changed to 4 clock cycles in order to keep the decimation rate constant at 128.

The 600 kHz symbol clock is generated from the 4.84 MHz baseband clock to avoid an extra frequency reference. A fractional-N divider is utilized in the symbol timing recovery circuit, as shown in Fig. 16(b), since the baseband clock is not in-

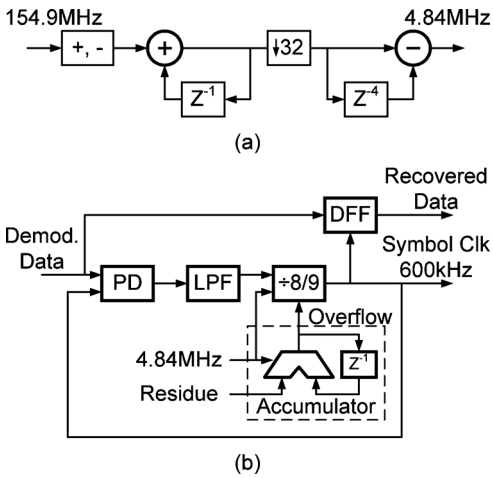


Fig. 16. Block diagram of (a) the modified CIC filter and (b) the symbol timing recovery circuit.

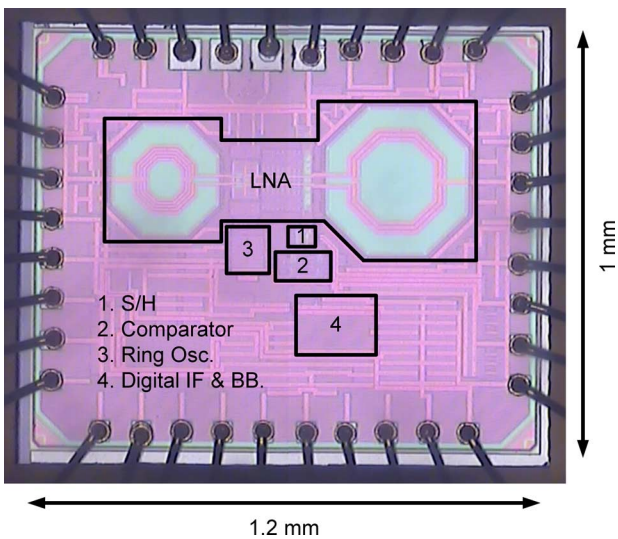


Fig. 17. Die photo.

teger times of the symbol clock. The programmable fractional divider also ensures constant baseband clock for different RF channel frequencies.

IV. Measurement Results

The proposed WBAN-compatible sub-sampling RX is implemented in 65 nm CMOS technology with a 3.4 μm thick metal layer for inductors. The digital-intensive architecture results in elimination of most analog circuits following the LNA. Therefore, the RX occupies only 0.35 mm^2 active area (0.3 mm^2 in the LNA) as shown in the die photograph in Fig. 17.

A. Q-Enhancement LNA

With the hybrid coarse/fine tuning strategy, the LNA output resonance frequency tuning LSB at 2.4 GHz is measured to be smaller than 0.9 MHz, yielding a worst case center frequency offset of 0.45 MHz, as shown in Fig. 18. The small size in relation to the carrier frequency of 2.4 GHz means that this high-Q front-end can be operated with effective Q enhancement up to

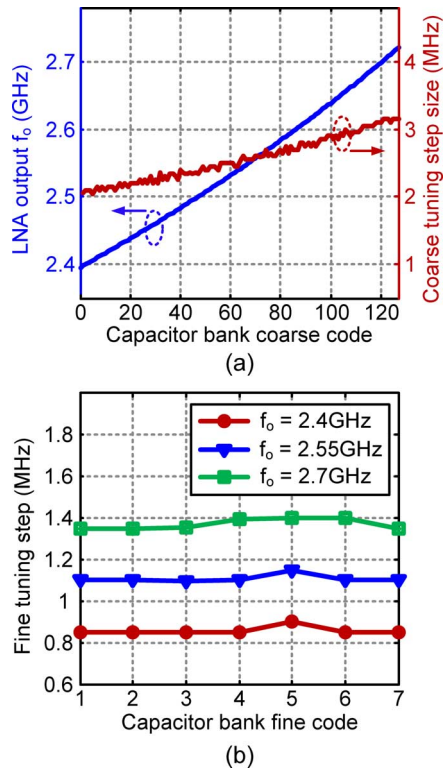


Fig. 18. Measurement of LNA output resonance tuning with (a) coarse code and (b) fine code.

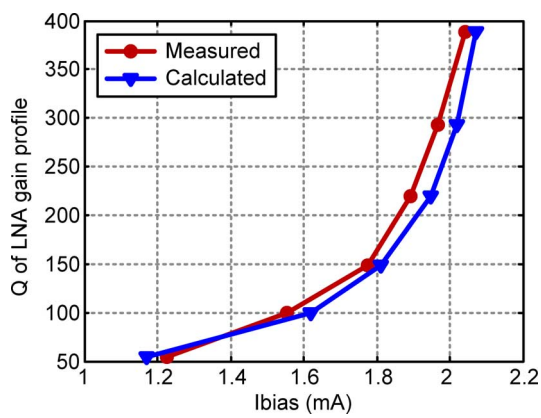


Fig. 19. Comparison between measurement and calculation of enhanced Q and LNA bias current.

400 with only 0.1 dB gain reduction and 0.5 dB gain fluctuation for 1 MHz channels at 2.4 GHz.

Fig. 19 validates the relationship between LNA bias current and effective tank Q as described in (9). The highest measured filter Q is close to 400 and the 44 bit digital bias current tuning translates to a Q step size of about 70 in Q-enhancement operation.

In WBAN application, antenna impedance can vary due to surrounding objects, resulting in a variation in source impedance for the LNA. To examine the impact of such changes, the input S11 is measured when the LNA is tuned to different center frequencies. As shown in Fig. 20, the input match does not change when the resonance frequency is tuned across the entire tuning range (validating the approximation in

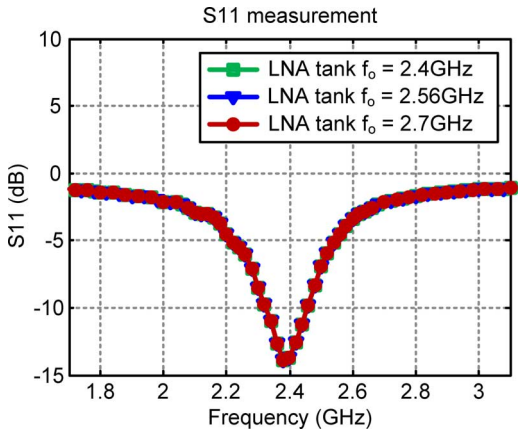


Fig. 20. Measurement of LNA input matching with different LNA output resonance.

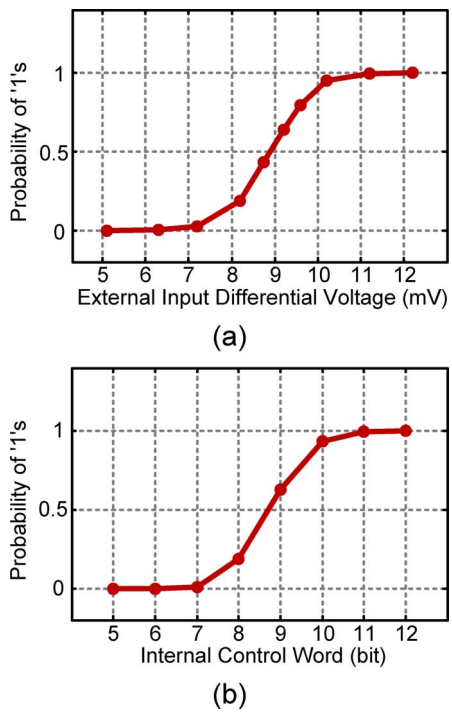


Fig. 21. Measured quantizer output accumulative Gaussian distribution curve versus (a) external input and (b) internal control word.

(12)), allowing input matching and LNA resonance calibration to be performed independently.

B. 1-Bit Quantizer

External DC voltage source are involved in measuring the performance and on-chip calibration accuracy for the 1 bit quantizer. By sweeping the differential DC input voltage of the 1 bit quantizer, a cumulative probability distribution is drawn based on the accumulator output. Fig. 21(a) shows an example of such measurement, in which the quantizer DC offset is calculated to be 8.9 mV and the input referred noise sigma is 0.88 mV. The actual on-die offset calibration does not involve those external DC voltage source. Only the internal digital control word of the current DAC shown in Fig. 13 needs to be set to bring the possibility of '1's close to 0.5. A similar cumulative curve can also

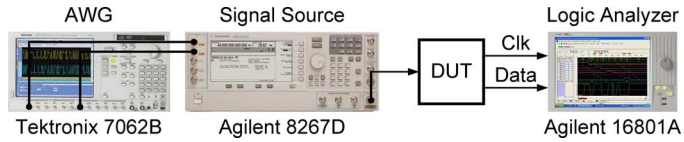


Fig. 22. BER measurement set up.

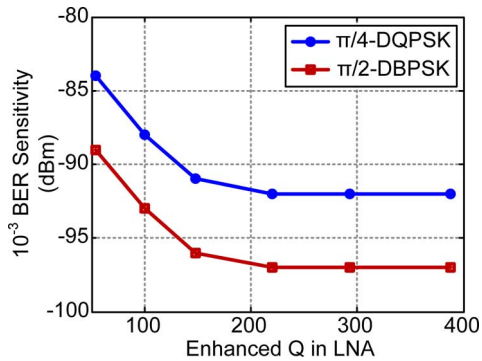


Fig. 23. Measurement of the RX sensitivity versus enhanced Q in LNA.

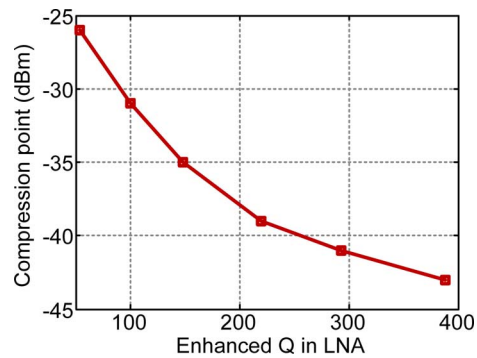


Fig. 24. Measurement of the RX compression point versus enhanced Q in the LNA.

be measured by sweeping the internal control word. The measurement example in Fig. 21(b) shows a calibration step size of 1.02 mV, yielding a worst case offset residue of 0.51 mV.

C. Sensitivity

Fig. 22 shows the set up for bit error rate (BER) measurement. An I/Q baseband waveform based on a 32767 bit PRBS is generated using MATLAB and a Tektronix 7062B arbitrary waveform generator (AWG). The AWG provides the baseband I/Q signal to an Agilent 8267D signal source that generates the I/Q modulated RF input signal for the device under test. An Agilent 16801A logic analyzer samples the demodulated data at the output and calculates BER. The RX sensitivity is measured based on 10^{-3} BER for different enhanced-Q values in the LNA. As shown in Fig. 23, sensitivities of both $\pi/4$-DQPSK and $\pi/2$-DBPSK are finally converged to -92 dBm and -97 dBm, respectively, as predicted in Section II.A.

D. Linearity

The large signal performance of the proposed sub-sampling RX is measured by increasing the input signal amplitude to the

TABLE II
COMPARISON WITH RECENTLY PUBLISHED LOW POWER RX

	JSSC 13 [8] [9]	ISSCC 13 [10]	JSSC 13 [24]	JSSC 13 [15] [16]	This work [1]	
RX architecture	Sliding IF	Sliding IF	Low IF	Low IF	Sub-sampling	
Modulation	π/2-DBPSK / π/4-DQPSK	π/4-DQPSK	BFSK	BFSK	π/2-DBPSK / π/4-DQPSK	
Data rate	121 kbps / 971 kbps	971 kbps	1 Mbps	200 kbps	486 kbps / 971 kbps	
Frequency band	2.4 GHz	2.4 GHz	2.4 GHz	2.46 GHz	2.4 GHz	2.7 GHz
Noise figure	6 dB	6 dB	6 dB	6.1 dB	6 dB	5 dB
Sensitivity	-104 dBm / -96.5 dBm (10% PER)	-96 dBm (10% PER)	-84 dBm (0.1% BER)	-91.5 dBm (0.1% BER)	-96 / -91 dBm (0.1% BER)	-97 / -92 dBm (0.1% BER)
Compr. (10^{-3} BER)	-	-	-	-	>10 / -35 dBm	>10 / -38 dBm
ACR	-	-	40 dB	-	14 / 10 dB	14 / 10 dB
Image rejection	-	35 dB	-	-	33 dB	33 dB
RX FE bandwidth	-	-	~300 MHz	~600 MHz	140 MHz	140 MHz
Active / die area	**- / 5.9 mm² (130nm)**	**2 / 3.7 mm² (90nm)**	**- / 6.25 mm² (130nm)**	**- / 2.5 mm² (65nm)**	**0.35 / 1.2 mm² (65nm)**	
Supply	**1 V**	**1.2 V**	**1 V**	**0.3 V**	**0.6 V**	
Power dissipation	**4.8 mW [3]**	**3.8 mW [2]**	**3.45 mW**	**1.6 mW [2,3]**	**1301 µW**	**1054 µW**
RX energy effi.	**4.9 nJ/b**	**3.9 nJ/b**	**3.45 nJ/b**	**8 nJ/b**	**1.34 nJ/b**	**1.09 nJ/b**
RX FOM [4]	**221 dB**	**222 dB**	**217 dB**	**216 dB**	**227 dB**	**228 dB**

1. Measured with a typical Q of 148
2. Power dissipation excluding digital baseband
3. Power dissipation excluding ADC / off chip drivers
4. RX FOM = - 10*log(kTBF) - 10*log(P_{DC}/Data rate), based on [10]

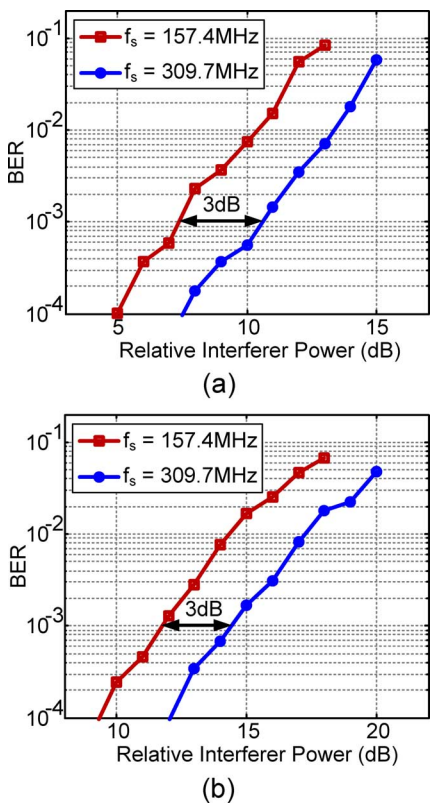


Fig. 25. Measurement of adjacent channel rejection for (a) $\pi/4$-DQPSK and (b) $\pi/2$-DBPSK.

point where the BER drops to 10^{-3}, which is named as "compression point" in Fig. 24. While the enhanced-Q in LNA increases from 54 to 388, the compression point decreases from -26 dBm to -43 dBm due to the LNA voltage gain increase. This feature can be used to accommodate the potential variation of the received signal dynamic range.

Another Agilent 8267D signal source is added to emulate the adjacent channel signal in ACR measurement. As shown in Fig. 25, with the sampling frequency of 309.7 MHz, the ACR of DQPSK and DBPSK are measured to be 10 dB and 14 dB, respectively. When the sampling frequency is decreased to 157.4 MHz, an expected 3 dB degradation in ACR is observed, since the 2 times lower oversampling rate leads to 3 dB lower linearity in oversampled A–D conversion.

E. 2.7 GHz Operation

In measurement, the highest intrinsic Q of the passive inductor and switched capacitors was found to be at 2.7 GHz. Because the bank capacitors are all switched off and the intrinsic loss is smaller, lower LNA bias current at 2.7 GHz is needed as compared to 2.4 GHz to obtain the same Q. We characterized the RX performance with a carrier frequency of 2.7 GHz as well and as can be seen the 2.7 GHz operation achieves similar performance as 2.4 GHz with even lower power consumption of 1.05 mW, as shown in Table II. Therefore, we estimate that increasing the inductor size to increase intrinsic Q at 2.4 GHz will lead to sub-mW RX power consumption.

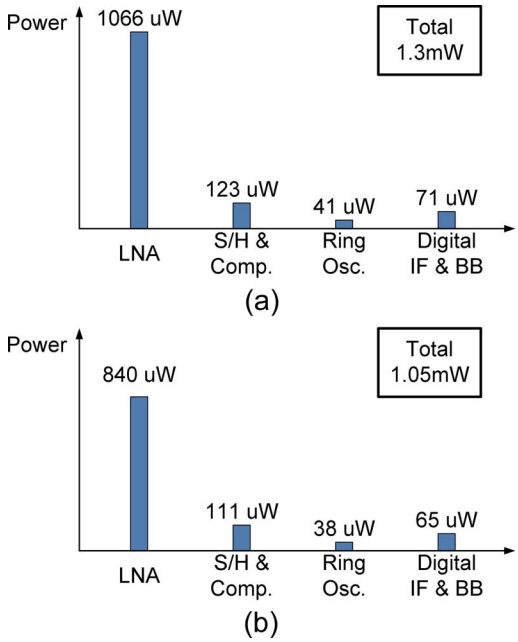


Fig. 26. Power breakdown of the RX prototype operated at (a) 2.4 GHz and (b) 2.7 GHz.

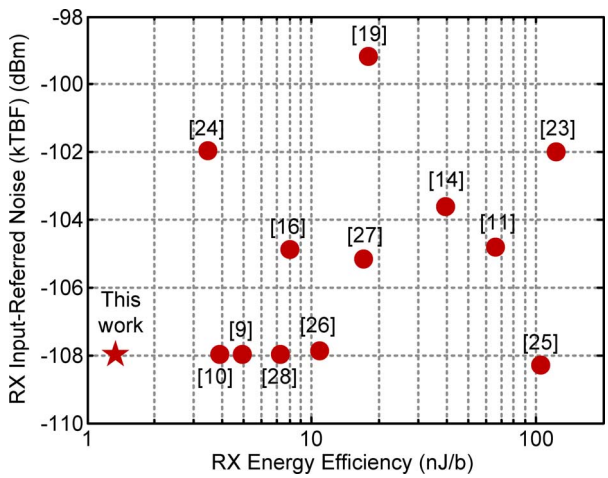


Fig. 27. FOM comparison of 2.4 GHz low power RX.

F. Comparison With Prior Art

Fig. 26 shows the power breakdown of the RX prototype operated at 2.4 GHz and 2.7 GHz, respectively. Table II compares the sub-sampling RX prototype with other recently published low power 2.4 GHz RX. With noise figure and sensitivity comparable to the state of art, this work achieves 3 times lower power consumption [8]–[10] and 3 times lower energy per bit than the RX with lower spectrum efficiency modulation (BFSK) [16], [24]. Fig. 27 shows the RX figure of merit (FOM) (defined in Table II) of the proposed sub-sampling RX and prior 2.4 GHz low power RX, demonstrating that the proposed architecture and implementation advances state-of-the-art in low-power wireless radios.

V. Conclusion

A mostly digital 2.4–2.7 GHz RX architecture that uses a sub-sampling technique with Q-enhancement LNA and digital IF/baseband signal processing to enable low-power and low-voltage operation is proposed. By decreasing the local oscillation frequency and eliminating most analog circuits from the design, this sub-sampling RX prototype achieves -91 dBm and -96 dBm sensitivities for $\pi/4$-DQPSK and $\pi/2$-DBPSK modulation, respectively, with only 1.3 mW power consumption and occupies only 0.35 mm^2 active area. The proposed techniques demonstrate the feasibility of sub-mW 2.4 GHz WBAN RX in advanced CMOS technologies. These techniques are applicable to other low-power wireless standards and the digital-intensive techniques can be further extended to achieve lower power, smaller area and improved sensitivity with scaling to more advanced CMOS technologies.

References

[1] IEEE Standard for Local and Metropolitan Area Networks—Part 15.6: Wireless Body Area Networks, IEEE 802 LAN/MAN Standards Committee, Feb. 29, 2012 [Online]. Available: www.ieee.org

[2] A. Vouilloz, M. Declercq, and C. Dehollain, "A low-power CMOS super-regenerative receiver at 1 GHz," *IEEE J. Solid-State Circuits*, vol. 36, no. 3, pp. 440–451, Mar. 2001.

[3] F. X. Moncunill-Geniz *et al.*, "An 11-Mb/s 2.1-mW synchronous superregenerative receiver at 2.4 GHz," *IEEE Trans. Microw. Theory Tech.*, vol. 55, no. 6, pp. 1355–1362, Jun. 2007.

[4] J. Bohorquez, A. Chandrakasan, and J. Dawson, "A 350 μW CMOS MSK transmitter and 400 μW OOK super-regenerative receiver for medical implant communications," *IEEE J. Solid-State Circuits*, vol. 44, no. 4, pp. 1248–1259, Apr. 2009.

[5] J. Ayers, K. Mayaram, and T. Fiez, "An ultralow-power receiver for wireless sensor networks," *IEEE J. Solid-State Circuits*, vol. 45, no. 9, pp. 1759–1769, Sep. 2010.

[6] C. Ma *et al.*, "A near-threshold, 0.16 nJ/b OOK-transmitter with 0.18 nJ/b noise-cancelling super-regenerative receiver for the medical implant communications service," *IEEE Trans. Biomed. Circuit Syst.*, vol. 7, no. 6, pp. 841–850, Dec. 2013.

[7] N. Stanic *et al.*, "A 2.4-GHz ISM-band sliding-IF receiver with a 0.5-V supply," *IEEE J. Solid-State Circuits*, vol. 43, no. 5, pp. 1138–1145, May 2008.

[8] A. Wong *et al.*, "A 1 V 5 mA multimode IEEE 802.15.6/bluetooth low-energy WBAN transceiver for biotelemetry applications," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 2012, pp. 300–301.

[9] A. C. W. Wong *et al.*, "A 1 V 5 mA multimode IEEE 802.15.6/Bluetooth low-energy WBAN transceiver for biotelemetry applications," *IEEE J. Solid-State Circuits*, vol. 48, no. 1, pp. 186–198, Jan. 2013.

[10] Y.-H. Liu *et al.*, "A 1.9 nJ/b 2.4 GHz multistandard (Bluetooth low energy/Zigbee/IEEE802.15.6) transceiver for personal/body-area networks," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 2013, pp. 446–447.

[11] L. Zhang *et al.*, "A reconfigurable sliding-IF transceiver for 400 MHz/2.4 GHz IEEE 802.15.6/ZigBee WBAN hubs with only 21% tuning range VCO," *IEEE J. Solid-State Circuits*, vol. 48, no. 11, pp. 2705–2716, Nov. 2013.

[12] A. Liscidini *et al.*, "Single-stage low-power quadrature RF receiver front-end: The LMV cell," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2832–2841, Dec. 2006.

[13] M. Tedeschi, A. Liscidini, and R. Castello, "Low-power quadrature receivers for ZigBee (IEEE 802.15.4) applications," *IEEE J. Solid-State Circuits*, vol. 45, no. 9, pp. 1710–1719, Sep. 2010.

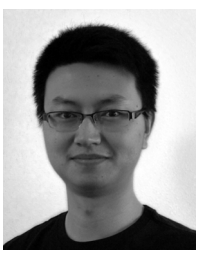
[14] A. Heragu, D. Ruffieux, and C. Enz, "A 2.4-GHz MEMS-based PLL-free multi-channel receiver with channel filtering at RF," *IEEE J. Solid-State Circuits*, vol. 48, no. 7, pp. 1689–1700, Jul. 2013.

[15] F. Zhang *et al.*, "A 1.6 mW 300 mV-supply 2.4 GHz receiver with -94 dBm sensitivity for energy-harvesting applications," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 2013, pp. 456–457.

[16] F. Zhang, Y. Miyahara, and B. Otis, "Design of a 300-mV 2.4-GHz receiver using transformer-coupled techniques," *IEEE J. Solid-State Circuits*, vol. 48, no. 12, pp. 3190–3205, Dec. 2013.

[17] J. Cheng, N. Qi, P. Chiang, and A. Natarajan, "A 1.3 mW 0.6 V WBAN-compatible sub-sampling PSK receiver in 65 nm CMOS," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 2014, pp. 168–169.

[18] R. Vaughan, N. Scott, and D. White, "The theory of bandpass sampling," *IEEE Trans. Signal Process.*, vol. 39, no. 9, pp. 1973–1984, Sep. 1991.
[19] A. Heragu, D. Ruffieux, and C. Enz, "A low power BAW resonator based 2.4-GHz receiver with bandwidth tunable channel selection filter at RF," *IEEE J. Solid-State Circuits*, vol. 48, no. 6, pp. 1343–1356, Jun. 2013.
[20] R. Mason, J. Fortier, and C. DeVries, "Complete SOC transceiver in 0.18 μm CMOS using Q-enhanced filtering, sub-sampling and injection locking," *IEEE J. Solid-State Circuits*, vol. 47, no. 8, pp. 1800–1809, Aug. 2012.
[21] A. Paidimarri *et al.*, "A 2.4 GHz multi-channel FBAR-based transmitter with an integrated pulse-shaping power amplifier," *IEEE J. Solid-State Circuits*, vol. 48, no. 4, pp. 1042–1054, Apr. 2013.
[22] Y. Cui *et al.*, "Process variation compensation of a 2.4 GHz LNA in 0.18 μm CMOS using digitally switchable capacitance," in *Proc. IEEE Int. Symp. Circuit and Systems*, May 2007, pp. 2562–2565.
[23] H. Darabi *et al.*, "A 2.4-GHz CMOS transceiver for bluetooth," *IEEE J. Solid-State Circuits*, vol. 36, no. 12, pp. 2016–2024, Dec. 2001.
[24] R. Ni, K. Mayaram, and T. Fiez, "A 2.4 GHz hybrid polyphase filter based BFSK receiver with high frequency offset tolerance for wireless sensor networks," *IEEE J. Solid-State Circuits*, vol. 48, no. 5, pp. 1250–1263, May 2013.
[25] W. Kluge *et al.*, "A fully integrated 2.4-GHz IEEE 802.15.4-compliant transceiver for ZigBee™ applications," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2767–2775, Dec. 2006.
[26] T. Song *et al.*, "A low-power 2.4-GHz current-reused receiver front-end and frequency source for wireless sensor network," *IEEE J. Solid-State Circuits*, vol. 42, no. 5, pp. 1012–1022, May 2007.
[27] S. Verma *et al.*, "A 17-mW 0.66-mm^2 direct-conversion receiver for 1-Mb/s cable replacement," *IEEE J. Solid-State Circuits*, vol. 40, no. 12, pp. 2547–2554, Dec. 2005.
[28] B. W. Cook *et al.*, "Low-power 2.4-GHz transceiver with passive RX front-end and 400-mV supply," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2757–2766, Dec. 2006.



Jiao Cheng (S'10–M'14) received the B.E. degree in microelectronics from Tsinghua University, Beijing, China, in 2009, and the Ph.D. degree in electrical engineering from Oregon State University, Corvallis, OR, USA, in 2014.

In 2012, he was a summer intern at Broadcom Corporation, Irvine, CA. He is currently with Maxim Integrated, Hillsboro, OR.

Dr. Cheng received the Best Poster Paper Award at CICC 2012 and the ADI Outstanding Student Designer Award in 2014.

Nan Qi (M'14) received the M.S. and Ph.D. degrees from the Institute of Microelectronics, Tsinghua University, Beijing, China, in 2008 and 2013, respectively. He is now working as a post-doctorate scholar in the Department of EECS, Oregon State University, Corvallis, OR, USA.

From 2010 to 2013, he led the GNSS group in Tsinghua University in building RF receivers. Since 2013, he has been focusing on high-speed silicon photonics. His interests include the design of analog/RF circuits and systems, as well as high-speed optical transceivers.

Patrick Yin Chiang (M'04) received the B.S. degree in electrical engineering and computer sciences from the University of California, Berkeley, CA, USA, in 1998, and the M.S. and Ph.D. degrees in electrical engineering from Stanford University, Stanford, CA, USA, in 2001 and 2007.

He is an Associate Professor at Oregon State University, Corvallis, OR, USA, and a visiting Professor at Fudan University in Shanghai, China. His research group has published more than 100 conference/journal papers in the area of energy-efficient circuits and systems, including near-threshold wireline transceivers, silicon photonics and 25G optical transceivers, reliable near-threshold computing, and energy-constrained biomedical sensors.

Dr. Chiang is the recipient of a 2010 Department of Energy Early CAREER award and a 2012 NSF CAREER award for energy-efficient interconnects and robust near-threshold computing.

Arun Natarajan (M'07) received the B.Tech. degree from the Indian Institute of Technology, Madras, India, in 2001, and the M.S. and Ph.D. degrees from the California Institute of Technology, Pasadena, CA, USA, in 2003 and 2007, respectively, all in electrical engineering.

From 2007 to 2012, he was a Research Staff Member with IBM T. J. Watson Research Center, Yorktown Heights, NY, USA, and worked on millimeter-wave (mm-wave) phased arrays for multi-Gb/s data links and airborne radar and on self-healing circuits for increased yield in submicron process technologies. In 2012, he joined Oregon State University, Corvallis, OR, USA, as an Assistant Professor with the School of Electrical Engineering and Computer Science. His current research is focused on low-power RF, mm-wave and sub-mm-wave integrated circuits and systems for high-speed wireless communication and imaging.

Dr. Natarajan was the recipient of the National Talent Search Scholarship from the Government of India (1995–2000), the Caltech Atwood Fellowship in 2001, the Analog Devices Outstanding Student IC Designer Award in 2004, and the IBM Research Fellowship in 2005, and serves on the Technical Program Committee of the IEEE Radio-Frequency Integrated Circuits Conference, IEEE Compound Semiconductor IC Symposium, and the 2013 IEEE International Microwave Symposium.