

# Understanding AC Coupling Capacitors at Multi-Gbps Data Rates



---

a  MICROCHIP company

## Contents

---

1	Revision History .....	1
1.1	Revision 1.0 .....	1
2	Introduction .....	2
2.1	What is Important? .....	2
2.2	Non-ideal Capacitor Parasitics .....	2
2.3	Behavior of Real Capacitors in a High-Speed System .....	4
3	HSPICE Simulations .....	6
4	Summary .....	9

# 1 Revision History

---

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

## 1.1 Revision 1.0

Revision 1.0 was the first release of this document. It was published in September 2011.

## 2 Introduction

AC coupling capacitors are frequently used in multi-gigabit data links. Many current data standards require AC coupling (for example PCIe Gen 3, 10 Gb Ethernet, and so on). In addition, there exist incompatible common mode voltages between drivers and receivers, for which AC coupling is the simplest means to solve this problem.

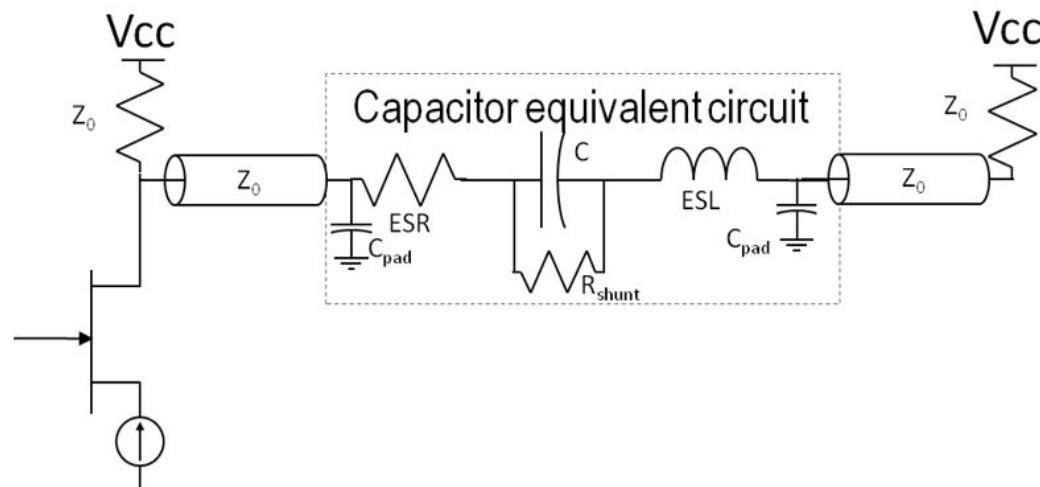
Designers may look in vain for capacitors with self-resonant frequencies above the Nyquist frequency of the system data standard. Only very small value capacitors (less than 10 pF) have resonant frequencies above 1 GHz. On the other hand, to preserve low frequency data content, required coupling capacitance is in the range of 0.1 mF to 4.7 mF, with self-resonances in the 100s of MHz. In some cases, the approach is to use the “best” capacitors available (for example, low ESR), intended for power supply decoupling, and hope that it is good enough.

In this application note, we emphasize the function of an AC coupling capacitor is to block DC and not to approach the performance of an ideal capacitor. Furthermore, we have used standard low-cost capacitors for AC coupling on our evaluation boards at data rates up to 12.5 Gbps with good results.

### 2.1 What is Important?

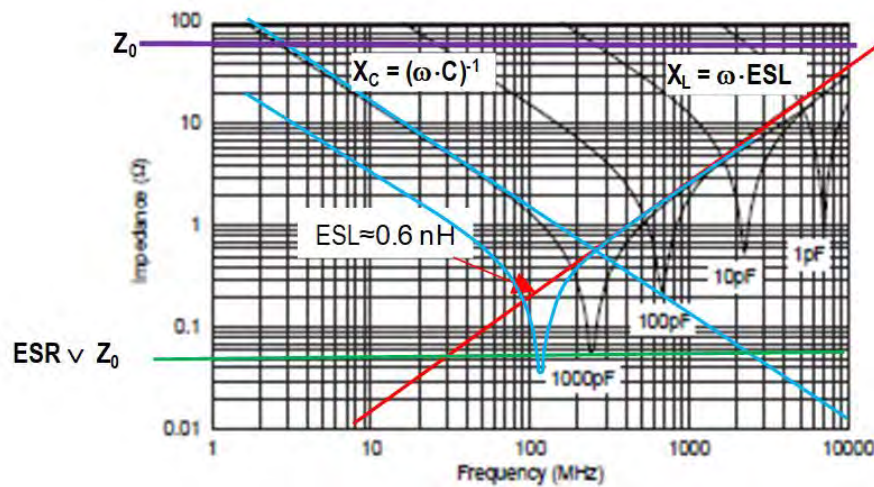
Figure 1 shows a simplified data path equivalent circuit. This consists of a CML source driver, terminated through resistance  $Z_0$  to  $V_{CC}$ , a transmission line with impedance  $Z_0$ , equivalent circuit for a coupling capacitor, and termination of the transmission line through a resistor  $Z_0$  to  $V_{CC}$ . In most cases, the value of  $R_{shunt}$  is large enough to be unimportant to the following analysis.

Figure 1 • Transmission Line with AC Coupling Capacitor: Equivalent Circuit



### 2.2 Non-ideal Capacitor Parasitics

For power supply decoupling, all parasitics are important. Capacitors are chosen to minimize power distribution impedance over the frequency ranges of interest. Figure 2 shows typical impedance magnitude vs. frequency curves for a particular capacitor family. The different curves are for different capacitance values, the package size being held constant. By staggering a variety of capacitor values, it is possible to reduce the power distribution impedance over a wide range of frequencies. In this case, the capacitor ESR (equivalent series resistance) is critical. ESL (equivalent series inductance) is also important but, as we shall see, it is largely dependent upon package size and construction, not upon capacitance value.

**Figure 2 • Typical Frequency-Dependent Impedance vs. Capacitor Value**


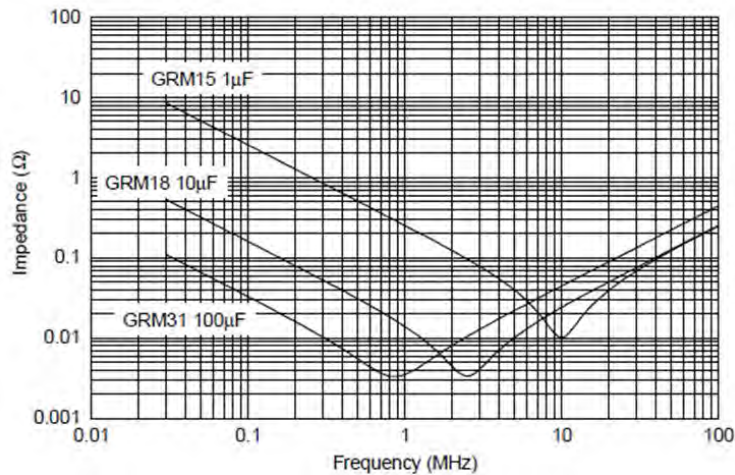
Example: Murata 0402, 5%

- High Dielectric Constant Type X6S
- 6.3V: GRM155C80Jxxx
- 1 mF, 100 pF, 10 pF, 1 pF, (4.7 mF, in blue, extrapolated)
- Self resonant frequency is inversely proportional to capacitance
- Above resonance:
  - For a fixed package size, the asymptotic high frequency impedance (inductive) is nearly identical, independent of capacitance value
- $ESL \approx 0.6 \text{ nH}$ , based on high-frequency asymptotic behavior
- $ESR \approx 0.25 \text{ W}$  (0.06 W) for 100 pF (1000 pF) capacitor curves, respectively, based on Z at resonance

For AC coupling applications, ESR is small compared to  $Z_0$ ,  $R_{shunt}$  is large, thus both can largely be ignored. Parasitic shunt capacitance,  $C_{pad}$ , can be a problem if not properly dealt with through PCB layout edits. For example, the capacitance of a 0.63 mm<sup>2</sup> pad<sup>1</sup> over 5 mil of FR4 dielectric is about 0.18 pF. This can be minimized and, therefore, ignored, with proper ground anti-pads beneath the capacitor and solder pad footprint.

For multi-Gbps data rates, series impedance is dominated by series inductive reactance,  $X_L$ . Series inductance is a geometric property determined by the capacitor's package type, package size, and by excess loop inductance of the entire signal path. Figure 3 illustrates this with three capacitors each with different values and package sizes. Note that the 0805 package has greater ESL than the 0603 and 0402 packages. **Note:**

1. One capacitor manufacturer, for example, recommends a pad size of 28 x 35 mil (0.63 mm<sup>2</sup>) for an 0402 ceramic SMT capacitor. 0402 capacitors are often used for AC coupling applications as a good compromise between performance and occupied area.

**Figure 3 • Effect of Capacitor Package Size on Impedance**


#### Effect of Package Size

- Comparing impedance vs. frequency for :
  - 0402 (1 mF), 0603 (10 mF), and 0805 (100 mF)
  - Above resonance
    - 0402 and 0603 have same high-frequency asymptotic behavior (ESL)
    - 0805 package has  $\sim 1/2$  the ESL of the 0402 package

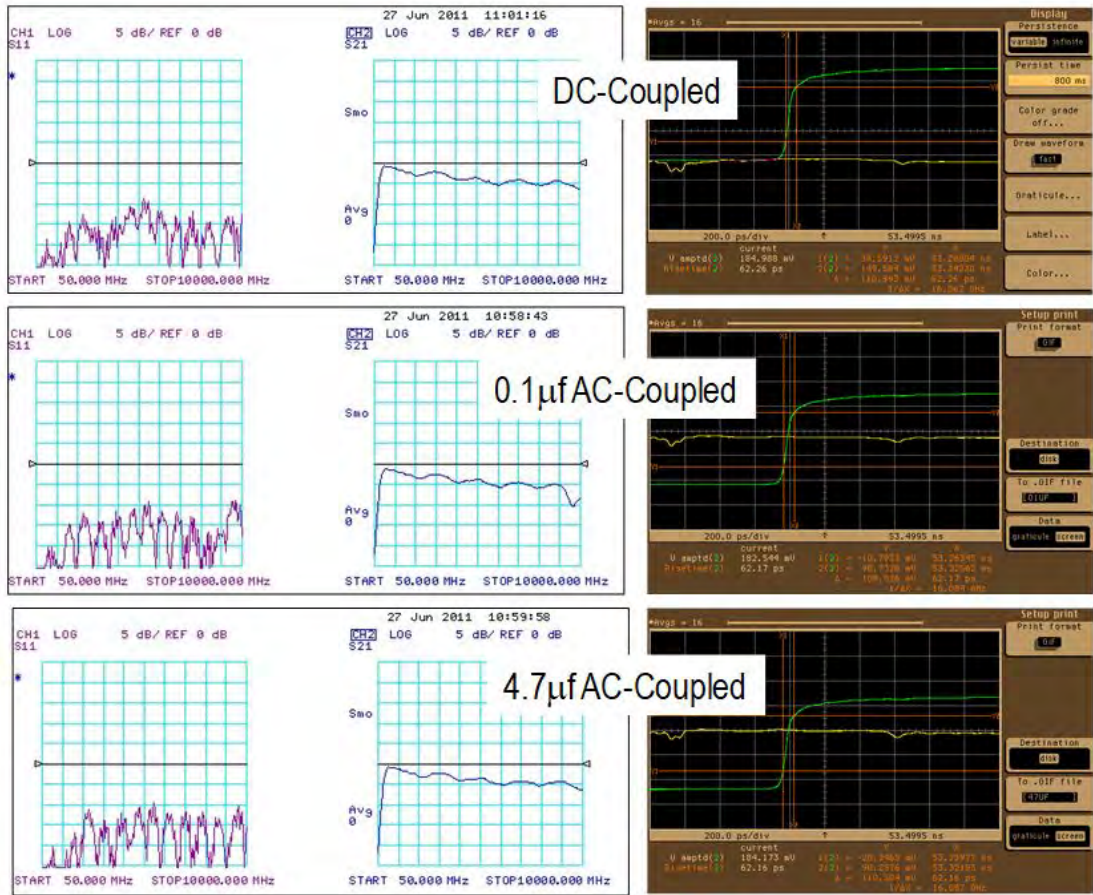
## 2.3 Behavior of Real Capacitors in a High-Speed System

To demonstrate that the capacitor value has a negligible effect on high-speed signals in the 10 Gbps range, a simple fixture (Figure 4) was used. This consisted of two SMA connectors linked by a 4-inch 50 W microstrip trace with a single 0402 capacitor in the path. The capacitor footprint has ground relief to compensate for parasitic capacitance. VNA, TDR, and TDT measurements were made with three components in the capacitor location, a 0 W resistor, 0.1 mF capacitor, and a 4.7 mF capacitor.

**Figure 4 • Microstrip Text Fixture**


Signal quality results are shown in Figure 5. There are no significant visible differences for the VNA measurements between 50 MHz and 10 GHz or for the TDR/TDT traces.

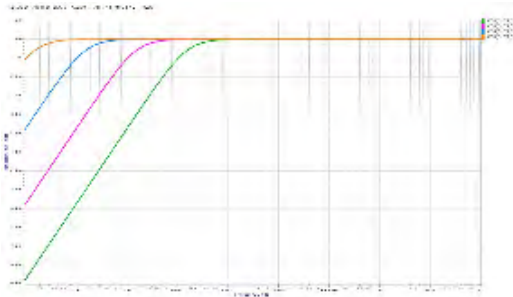
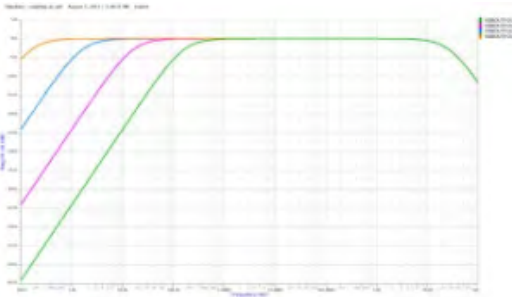
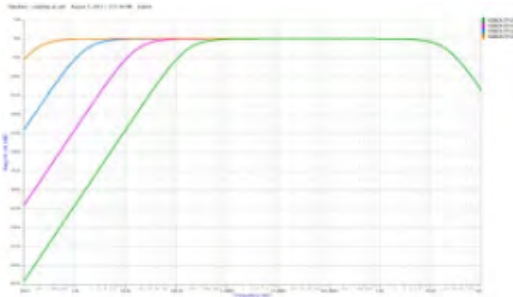
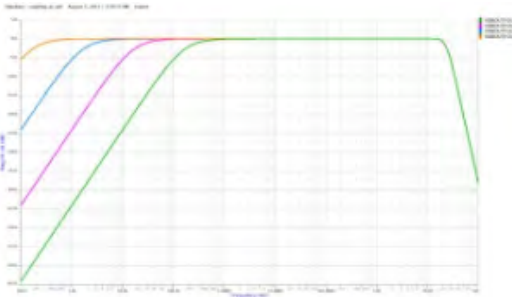
Figure 5 • Effect of AC Coupling Capacitance Value on Signal Quality



### 3 HSPICE Simulations

In this section, HSPICE is used to illustrate the relative signal integrity effects of the different parameters in the non-ideal capacitor model described in Figure 1. A series of HSPICE simulations were run, beginning with an ideal AC coupling capacitor and sequentially adding typical values for the different parasitics in the non-ideal model. Figure 6 shows S21 simulations with ESL = 0 and ESL = 0.6nH, a value extrapolated from the plot in Figure 2. In this, and subsequent simulations, solder pad capacitances (Cpad) of 0 pF and 0.15 pF were assumed. 7 adds ESR values, and a *s4p* file from a real customer data path replaces the second ideal transmission line.

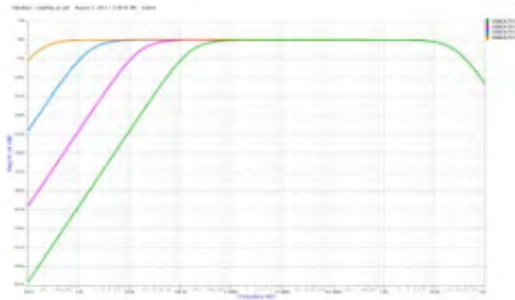
**Table 1 • S21 Plots for an Ideal Transmission Line with Capacitor in the Center, without ESR**

<p>This column adds ESR values to the capacitor model estimated from the resonance minima in Figure 2.</p>	<p>This column models the same as the left but replaces the second differential transmission line with a Touchstone <i>s4p</i> model from a customer.</p>
	
<p>No ESL, No ESR, No Cpad, ideal T-lines</p>	<p>ESL=6nH, No ESR, No Cpad, ideal T-lines</p>
	
<p>No ESL, No ESR, Cpad=150F, ideal T-lines</p>	<p>ESL=6nH, No ESR, Cpad=150F, ideal T-lines</p>

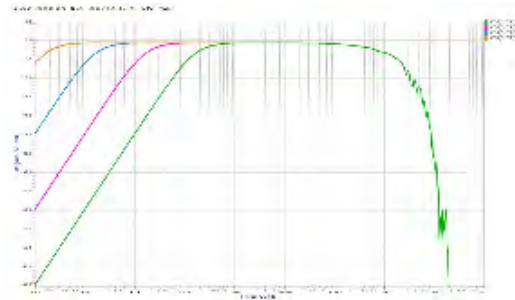
**Table 2 • S21 Plots for an Ideal Transmission Line with Capacitor in the Center, with ESR**

<p>This column adds ESR values to the capacitor model estimated from the resonance minima in Figure 2.</p>	<p>This column models the same as the left but replaces the second differential transmission line with a Touchstone <i>s4p</i> model from a customer.</p>
--	---

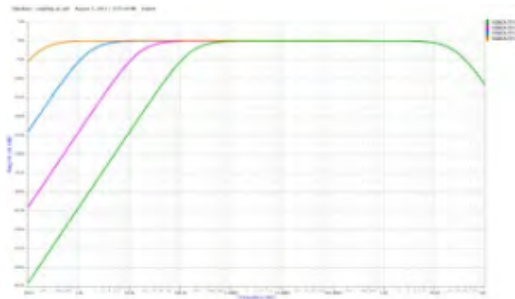




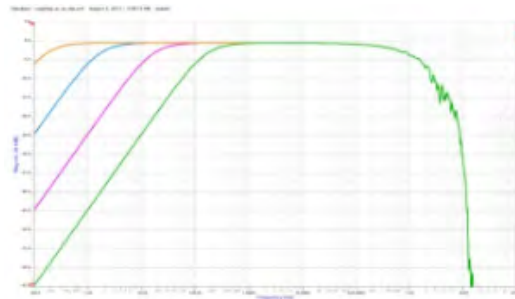
Multiple ESR, ESL = 0.6nH, No Cpad, ideal T-lines



Multiple ESR, ESL = 0.6nH, No Cpad, S4P



Multiple ESR, ESL = 0.6nH, Cpad=150F, ideal T-lines

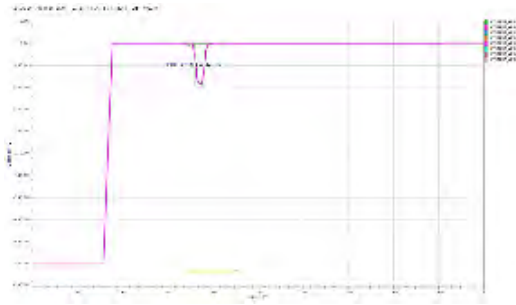


Multiple ESR, ESL = 0.6nH, Cpad=150F, S4P

Figure 8 shows a series of simulated TDR (Time Domain Reflectometry) and TDT (Time Domain Transmission) plots showing the time-domain response of an AC-coupled differential transmission line with different levels of capacitor model parasitics. Figures 8a and 8b show the response of an ideal transmission line with an ideal AC coupling capacitor. In these and all other plots, green curves are without pad parasitics and magenta curves are with simulated pad shunt capacitances, Cpad. For figures 8a and 8b, Cpad = 0.15 pF, approximate value for uncompensated 0402 solder pads over 5 mil FR4. Figures 8c and 8d add 0.6nH of ESL, as described above, to the model with Cpad = 0.15 pF. The effect is small, almost cancelling the parasitic pad capacitance and causing a small amount of peaking. Adding 0.25 W of ESR has a barely-visible effect and is not shown. Finally, Figures 8e through 8f show a similar progression of added parasitics but with the second ideal transmission line replaced with a Touchstone S4P file. Only the capacitor pad parasitic capacitance has any significant effect on the waveforms.

**Table 3 • Simulated TDR and TDT Waveforms**

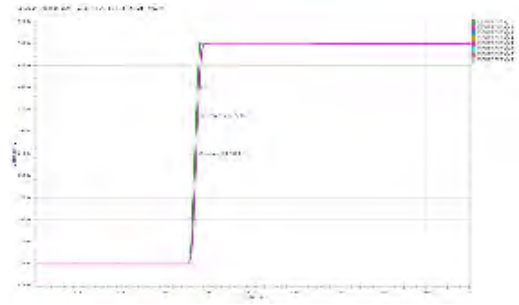
The green traces are with no pad capacitance. The magenta waveforms are with different pad capacitance values of 0.15 pF, as noted. The left column plots are simulated TDR waveforms while the right plots are simulated TDT waveforms.



**8a.** TDR ? No ESL, No ESR,

Cpad = 0 and 0.15 pF, ideal T-lines.

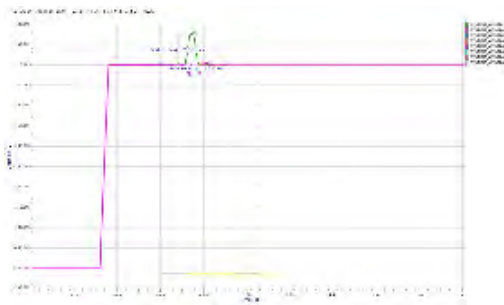
Typical pad capacitance shows small reflection compared with no pad capacitance.



**8b.** TDT ? No ESL, No ESR,

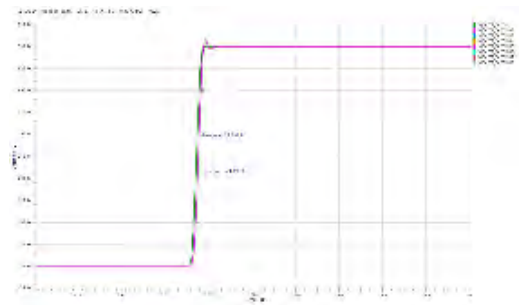
Cpad = 0 and 0.15 pF, ideal T-lines.

Typical pad capacitance shows negligible risetime increase.



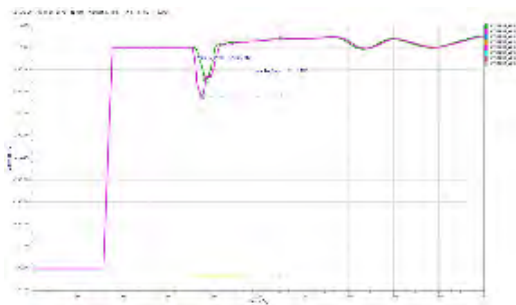
**8c.** TDR ? ESL = 0.6nH, No ESR,

Cpad = 0 and 0.15 pF, ideal T-lines



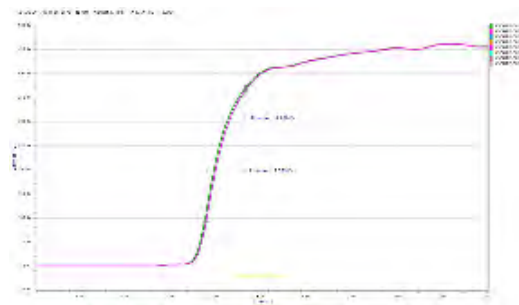
**8d.** TDT ? ESL = 0.6nH, No ESR,

Cpad = 0 and 0.15 pF, ideal T-lines



**8e.** TDR ? No ESL, No ESR,

Cpad = 0 and 0.15 pF, S4P T-line model



**8f.** TDT ? No ESL, No ESR,

Cpad = 0 and 0.15 pF, S4P T-line model

## 4 Summary

---

Ceramic surface mount capacitors are frequently used for AC coupling in multi-Gbps applications where they are required by a standard or needed to connect two devices with incompatible I/O common mode voltages. The tendency is to use the highest quality coupling capacitors available. In this application note, we have shown that the parasitics of non-ideal capacitors are virtually irrelevant to AC coupling requirements, which is in stark contrast to power supply de-coupling needs. Therefore, for most AC coupling uses, even in the 10 Gbps range, low-cost ceramic 0402 capacitors are entirely satisfactory.

**Microsemi Headquarters**

One Enterprise, Aliso Viejo,  
CA 92656 USA

Within the USA: +1 (800) 713-4113

Outside the USA: +1 (949) 380-6100

Sales: +1 (949) 380-6136

Fax: +1 (949) 215-4996

Email: [sales.support@microsemi.com](mailto:sales.support@microsemi.com)

[www.microsemi.com](http://www.microsemi.com)

© 2011 Microsemi. All rights reserved. Microsemi and the Microsemi logo are trademarks of Microsemi Corporation. All other trademarks and service marks are the property of their respective owners.

Microsemi makes no warranty, representation, or guarantee regarding the information contained herein or the suitability of its products and services for any particular purpose, nor does Microsemi assume any liability whatsoever arising out of the application or use of any product or circuit. The products sold hereunder and any other products sold by Microsemi have been subject to limited testing and should not be used in conjunction with mission-critical equipment or applications. Any performance specifications are believed to be reliable but are not verified, and Buyer must conduct and complete all performance and other testing of the products, alone and together with, or installed in, any end-products. Buyer shall not rely on any data and performance specifications or parameters provided by Microsemi. It is the Buyer's responsibility to independently determine suitability of any products and to test and verify the same. The information provided by Microsemi hereunder is provided "as is, where is" and with all faults, and the entire risk associated with such information is entirely with the Buyer. Microsemi does not grant, explicitly or implicitly, to any party any patent rights, licenses, or any other IP rights, whether with regard to such information itself or anything described by such information. Information provided in this document is proprietary to Microsemi, and Microsemi reserves the right to make any changes to the information in this document or to any products and services at any time without notice.

Microsemi, a wholly owned subsidiary of Microchip Technology Inc. (Nasdaq: MCHP), offers a comprehensive portfolio of semiconductor and system solutions for aerospace & defense, communications, data center and industrial markets. Products include high-performance and radiation-hardened analog mixed-signal integrated circuits, FPGAs, SoCs and ASICs; power management products; timing and synchronization devices and precise time solutions; setting the world's standard for time; voice processing devices; RF solutions; discrete components; enterprise storage and communication solutions; security technologies and scalable anti-tamper products; Ethernet solutions; Power-over-Ethernet ICs and midspans; as well as custom design capabilities and services. Microsemi is headquartered in Aliso Viejo, California, and has approximately 4,800 employees globally. Learn more at [www.microsemi.com](http://www.microsemi.com).

VPPD-02901