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FinFET-based Full Adder using SDTSPC Logic with High Performance

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***Abstract*—This paper presents an optimized design of SDTSPC logic (stacked diode transistor based TSPC) using FinFET transistors for 1-bit full adder. The analysis was performed for average power consumption, leakage power, propagation delay and power delay product (PDP) for different supply voltages, loads and temperatures. Comparing the proposed FinFET-based full adder design with MOSFET-based SDTSPC full adder, we achieved a 95.75% improvement in leakage power consumption. The proposed scheme is also compared with several previous designs and based on different simulations, the proposed FinFET-based full adder exhibits excellent performance. The proposed high-efficiency full adder cell operates at low voltages (0.4 V) even with large capacitors.**

***Keywords*—SDTSPC (stacked diode transistor based TSPC) logic, FinFET transistor, power delay product (PDP), TSPC logic**

I. Introduction

Transistors are essential components in electronic equipment such as radios, calculators, personal computers, notebooks, tablets and other electronic equipment. The demand for these electronic equipment is increasing day-to-day. Therefore, it is important for manufacturers to produce high quality electronic equipment and various functions. Scaling down the MOSFET process in CMOS technology has become increasingly important in order to meet customer demands. Reducing the channel length, gate oxide thickness, and supply voltage over the past three decades has increased transistor performance in terms of speed and power consumption [1]. Fabrication costs have also decreased sharply. Reducing the size of transistors by scaling of technology has led to increased number of devices and the density of integrated circuits [2-4] and an increase in capacitive coupling due to the high clock frequency [5]. In addition, by scaling the supply voltage, the threshold voltage is also lowered to maintain circuit performance, which increases the leakage current of the device.

If the channel length drops below 20 nm, transistors will lose performance. This means that conventional silicon MOSFETs will no longer be able to maintain Moore's Law. However, improved performance of electronic devices is very desirable in today's semiconductor industry. Therefore, engineers and scientists are trying to find a solution to overcome this challenge. Multi-Gate MOSFETs (i.e. FinFET) [6, 7], Quantum-Dot Cellular Automata (QCA) [8], Single Electron Transistor (SET) [9] and Carbon Nanotube Field-Effect Transistor (CNTFET) [10] are possible surrogates for conventional silicon-based MOSFET technology.

Addition is very important in computational operations and has been widely used in many VLSI designs, in most general-purpose systems operations, and in specific processors. Improving the performance of the full adder improves the overall performance of the system. Full adder design methods can be generally classified as static and dynamic logic. Static logic is robust and easy to design. Dynamic logic has attractive features despite its high switching activity. They are usually faster than their static counterparts. They need fewer transistors, which results in less area. In addition, voltage levels generally have full swing, and have no static power loss due to the elimination of short-circuit currents, which flow in static circuits when creating a direct path from the power line to the ground [11, 12]. However, in dynamic circuits, clock distribution connections lead to increased power consumption [13]. Also, dynamic logic is more sensitive to noise. However, this noise can be reduced by several methods. Most plans are offered with one or more compromises. Conventional standard CMOS designs cannot deliver high-speed digital design, so dynamic logic circuits are used to achieve fast digital designs.

Since the full adder cell is the core and the building block of most computing circuits, it has always been important to design high-performance full adder cells and complex computing circuits with low PDP [6, 10]. This paper presents a high-speed, low-power, low-PDP FinFET-based full adder for low voltages. The performance of the proposed design will be evaluated in different situations and compared to other conventional and up-to-date full adder cells in different styles. This article is organized as follows. In the Section II, we will have an overview of the FinFET transistor. In Section III, we present the proposed FinFET-based full adder circuit. The results of the simulation and performance analysis of several circuits along with the proposed circuit are discussed in Section IV. The conclusions will be summarized in Section V.

II. Overview of the FinFET Transistor

FinFET is categorized as a multi-gate device whose performance is often similar to traditional MOSFET. Typically, it has a source, a drain and a gate to control the current. The channel is made between the source and the drain of FinFET, which is a 3D strip at the top of the silicon substrate (so called Fin). In order to form several gate

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electrodes on each side, which may reduce the effects of leakage and increase the excitation current, the gate is covered around the channel (as Fig. 1). FinFET devices are manufactured in many different ways. In shorted-gate FinFETs (SG-FinFETs), two gates are connected to each other, resulting in a three-terminal device. This can be used as a direct alternative to traditional bulk-CMOS devices. In independent-gate FinFETs (IG-FinFETs), the upper part of the gate is etched and it provides two independent gates. Since, two independent gates can be controlled individually, IG-FinFETs provide more design options (see Fig. 1). Front gate (FG) and back gate (BG) of IG-FinFET can be connected in different configurations. IG-FinFET can be considered as two parallel transistors, and two gates can be stimulated independently as shown in Fig. 2. One of the gates, commonly called the back gate, affects the vertical field of the other transistor in the channel region. Thus, it changes the threshold voltage of device. It also affects the diffusion current in the sub-threshold regime, thereby controlling the leakage current. In addition, two parallel transistors in the IG-FinFET can be interconnected to improve driveability or to form a single transistor with independent gates. In Fig. 1, the effective channel length and width are equal to L_{FIN} and h_{FIN}, respectively. The device parameters used in this article are listed in Tab. I.

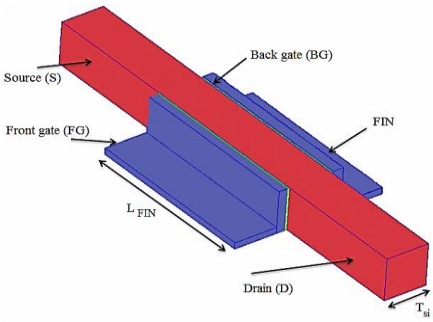
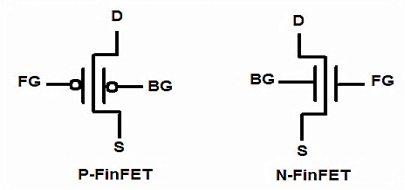


Fig. 1. IG-FinFET structure [6]



(a) (b)

Fig. 2. IG-FinFET symbols; (a) p-type, (b) n-type [6]

TABLE I. Device parameters of FinFET [1]

Parameter	Value
Length of the channel (L)	32nm
Thickness of front/back gate oxide (t_{oxfg}/t_{oxbg})	1.6nm
Thickness of the fin (t_{Si})	8nm
Height of the fin (h_{fin})	32nm
Work function (N/P) (φ_N/φ_P)	4.5eV/4.9eV
Power supply (V_{dd})	0.9
Channel doping (N_{BODY})	2×10^{20} cm^{-3}
Source/ Drain doping	2×10^{20} cm^{-3}

III. Proposed Design

Having a full adder with low power, high speed and energy efficient is very important. Compared to conventional MOSFET technology, the new FinFET technology can be implemented in 1-bit full adders, to continue scale reduction in silicon, and to enhance device performance and energy efficiency of full adders.

In [14], the designing problem of energy efficient and low noise dynamic TSPC logic for digital CMOS circuits is addressed. The proposed scheme in [14] is named as SDTSPC logic (stacked diode transistor based TSPC). To reduce power consumption, the effect of stacking on the power supply path to the ground has been used and to reduce noise, a self-biased NMOS transistor has been used in series with the evaluation transistor. In self-biased transistors, the gate and the drain are connected together as a single node. The good thing about the self-biased transistors is that they do not require any external control circuitry and the control signal is generated inside the circuit itself. Since gate and drain are interconnected, the saturation conditions $V_{ds} > V_{gs}-V_{th}$ are always maintained [15]. Where V_{ds} is the drain-source voltage, V_{gs} the gate-source voltage and V_{th} is the threshold voltage of the MOS transistor.

In [14], the method of step charging and discharging of the node capacitance using self-biased transistors is used. This reduces the ground and supply bouncing noise. Advantages of the SDTSPC design in [14] over other available designs include low power consumption, switching noise reduction, high speed over other dynamic circuit design styles, no charge sharing problem in dynamic node during pre-charge mode, reducing the ground and supply bouncing noise, robust against process corner changes. The proposed circuit in [14] effectively reduces total power consumption and idle power consumption. The key idea behind this method is to reduce power consumption by efficiently stacking the transistors from the supply voltage path to the ground [16, 17]. Also, a diode connected transistor is connected in series with the evaluation transistor to further improve noise and power consumption [18].

For this purpose, we implement SDTSPC full adder using FinFET transistors. We replace all MOSFET transistors in the structure of this full adder with IG-FinFET transistors. Fig. 3 shows a schematic of the proposed full adder based on the FinFET transistor. Compared to [14], the number of transistors in the proposed full adder cell is reduced, because that two parallel MOSFET transistors are replaced by a two-gate FinFET transistor [7].

The proposed circuit consists of two P-FinFET pre-charge transistors (M_{pc1} and M_{pc2}), one N-FinFET evaluation transistor (M_E), and four leakage control transistors (consists of two N-FinFET (M_{n1} and M_{n2}) and two P-FinFET (M_{p1} and M_{P2})). An N-FinFET transistor called M_D is placed as a diode connected transistor in series with to the evaluation network (M_E). In this structure, leakage control transistors and diode connected transistors creates the stacking effect and thereby reduces power consumption.

The advantage of transistor M_D is the bouncing noise reduction during the evaluation phase. As during the transition from the pre-charge to evaluation state the transistor M_E is switched on first, then M_D is switched on when the voltage at node N_3 is around the threshold voltage of M_D, thereby reducing the sudden current impact and noise [14]. Another advantage is that no additional control circuitry is needed to control the performance of the leakage control transistors. In addition, the reduction in power consumption is achieved by connecting the source terminal of latch N-FinFET to the node N_E.

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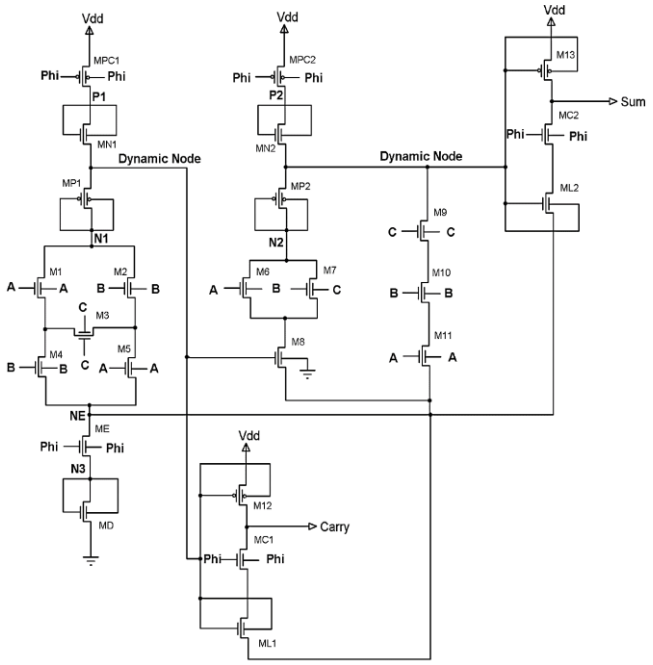

Fig. 3. Proposed FinFET-based full adder

During the pre-charge mode, the pre-charge transistors (M_{PC1} and M_{PC2}) are switched on, so the voltage at nodes P_1 and P_2 are increased, M_{n1} and M_{n2} (leakage control transistors) are switched on and the output node is pre-charged. During this phase, M_{p1} and M_{p2} (leakage control transistors) are switched off. Since the evaluation transistor is switched off, the voltage at nodes N_1 and N_2 increases as a result of the increased stack of transistors.

During evaluation mode, pre-charged transistor is off. As a result, leakage control transistors are also turned off. Therefore, an stack of transistors is generated from the power supply to ground path. Depending on the input values, voltage levels at nodes N_1 and N_2 are lowered or remained high. If it drops, M_{p1} and M_{p2} will get turned on and provide the evaluation path for the charge stored in the dynamic node. Therefore, during the evaluation phase, if the inputs are such that there is no discharge path to ground, then the leakage control transistors increase the stacking effect since they are switched off and thus reduce the power consumption of the device.

IV. Simulation Results and Analysis

The proposed design has been widely evaluated in various situations and compared with other classical and modern full adders. All designs are simulated using the Synopsys HSPICE 2008 simulator with 32nm CMOS technology for CMOS circuits, and 32nm FinFET technology [19] for FinFET circuits.

Simulations were performed at room temperature and at different voltages, frequencies, and load capacitances. The complete input pattern was applied to circuits with all possible transition states from one input combination to another to measure their propagation delay. The delay measurement of each circuit is performed from the time the input signal reaches $V_{dd}/2$ until the output signal reaches the same voltage level. All states of transmission from one input to another are investigated and delay is measured for each transmission and the maximum value is reported as the propagation delay of each circuit. Average power consumption over a long period of time is also considered as the average power parameter. In order to make a compromise between the power consumption and the delay of the circuits, the performance of these circuits can be evaluated by calculating the power delay product (PDP), which is the product of average power consumption and maximum delay. Consequently, PDP can be an important parameter for evaluating and comparing the performance of these circuits.

Simulations in [14] were performed using 180 nm PDK BSIM3V3 process models in cadence with power supply voltage of 1.8 V, clock frequency of 500 MHz and load capacitance of 1 fF at sum and carry outputs. In the first experiment, we simulated this circuit at 25 °C with 32nm CMOS technology with power supply voltage of 1V, clock frequency of 500 MHz and load capacitance of 1 fF at sum and carry outputs. We also simulated the proposed FinFET-based circuit with 32 nm FinFET technology with the above conditions.

Fig. 4(a) and Fig. 4(b) show the input and output waveforms of the SDTSPC full adder with 32 nm CMOS technology, and the proposed SDTSPC full adder based on 32 nm FinFET technology in the first experiment. In both forms, the first waveform is clock signal (Phi), the second and third waveforms are data inputs (A and B), the fourth waveform is carry input (C), the fifth and sixth waveforms are sum and carry output, respectively.

Tab. II presents the simulation results with the above conditions and the best results are bolded. These results show that the SDTSPC full adder at low voltage and 32nm CMOS technology perform poorly in terms of delay, power consumption, leakage power and PDP. While the proposed FinFET-based SDTSPC full adder perform well. In further experiments we will show the better performance of the proposed full adder.

TABLE II. Simulation results of the first experiment

Full Adder Design	**Tech.**	**V_{dd} (V)**	**Delay (ps)**	**Leakage Power (nW)**	**Power (µW)**	**PDP (aJ)**
FinFET SDTSPC (Proposed)	32nm FinFET	1	**49.44**	**0.43**	0.640	31.6
CMOS SDTSPC [19]	32nm CMOS	1	113.77	752.78	0.788	89.7
CMOS SDTSPC [19]	180nm CMOS	1.8	53.1	10.12	0.402	**21.3**

In the second experiment, the proposed full adder was simulated at the supply voltages of 0.8, 0.65 and 0.5 V, the clock frequency of 500 MHz, and the inputs with frequency of 100 MHz and with load capacitance (C_{load}) of 2.1 fF. The exact results of these simulations are listed in Tab. 3 and compared with other conventional structures such as Hybrid, CMOS-Bridge, TGA and Design3. The best results are displayed at each voltage with bolded numbers. According to the experimental results, the proposed FinFET-based full adder has the lowest leakage power compared to other

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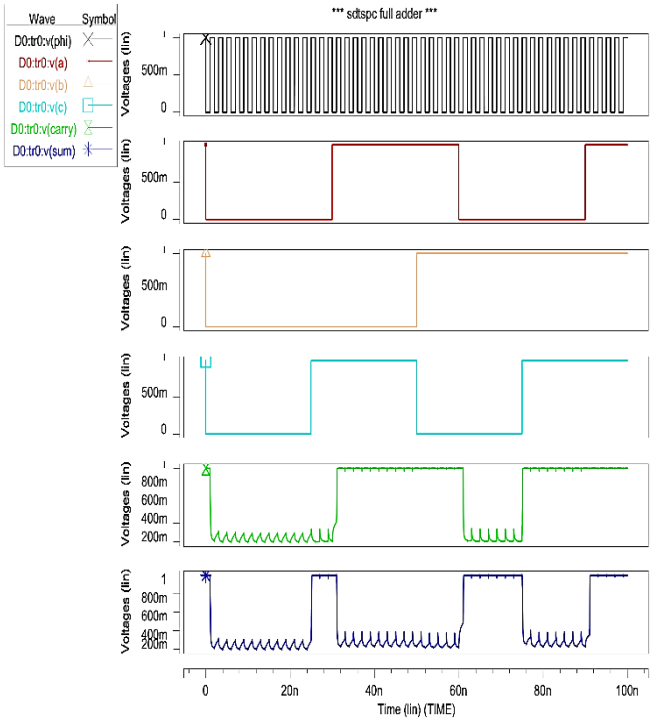
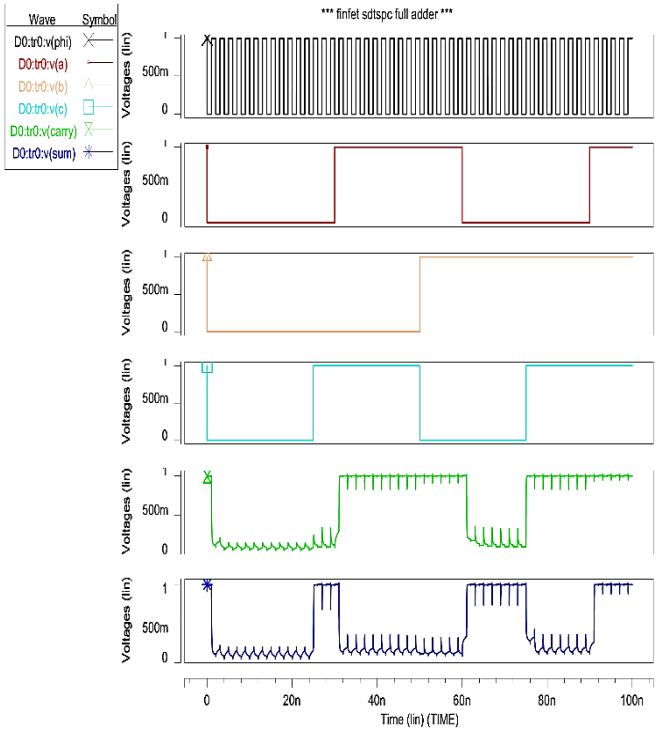
structures at the voltages of 0.8, 0.65 and 0.5 V. In terms of propagation delay and PDP, it also performs better than other structures.



(a)



(b)

Fig. 4. Transient mode characteristic; (a) SDTSPC full adder with 32 nm CMOS technology, (b) proposed FinFET-based SDTSPC full adder

TABLE III. Simulation results of the proposed full adder and comparison with other structures (frequency=100 MHz, Cload=2.1 fF)

V_{DD} (v)	0.5	0.65	0.8
Delay ($\times 10^{-12}$ s)			
Hybrid [20]	1064	339.41	192.85
CMOS-Bridge [21]	1269.9	01.44	229.43
TGA [22]	2036.9	57.09	283.39
Design3 [23]	2283.8	62.05	364.19
FinFET SDTSPC (Proposed)	**196.57**	**111.46**	**85.40**
Average power ($\times 10^{-6}$ w)			
Hybrid [20]	0.0603	0.1023	0.1588
CMOS-Bridge [21]	**0.0573**	**0.0981**	**0.1492**
TGA [22]	0.0659	0.1054	0.1617
Design3 [23]	0.0592	0.1048	0.1617
FinFET SDTSPC (Proposed)	0.1506	0.287	0.474
Leakage power ($\times 10^{-9}$ w)			
Hybrid [20]	386.37	689.64	1500.9
CMOS-Bridge [21]	6.4181	2.0780	4.2522
TGA [22]	8.2755	5.0872	9.2551
Design3 [23]	17.450	5.3407	7.1369
FinFET SDTSPC (Proposed)	**0.201**	**0.27**	**0.35**
PDP ($\times 10^{-17}$ j)			
Hybrid [20]	6.4235	3.4722	**3.0630**
CMOS-Bridge [21]	7.2793	3.9401	3.4236
TGA [22]	13.424	5.8770	4.5832
Design3 [23]	13.530	6.9398	5.8890
FinFET SDTSPC (Proposed)	**2.96**	**3.20**	4.05

To evaluate the immunity of the proposed full adder to the ambient temperature variation, the proposed circuit have been simulated at a wide range of temperatures from 0 °C to 100 °C at the supply voltage of 0.65 V, the clock frequency of 500 MHz, the input signals of 100 MHz and the load capacitance of 2.1 fF have been simulated and compared to other full adders. The results of this experiment are plotted in Fig. 5. From the experimental results, it can be deduced that the proposed full adder has acceptable performance at a wide range of temperatures and its PDP is lower compared to other designs.

The driveability of the proposed full adder with load capacitance changes was also investigated. The worst case of delay occurs when the supply voltage is low and high load capacitances are used. To investigate this feature, we simulated the proposed circuit at a clock frequency of 500 MHz, an input signal frequency of 100 MHz, and a supply voltage of 0.65 V using a large number of load capacitances in the range of 1.4 fF to 4.9 fF and compared it with other previous designs. The results of this experiment are shown in Fig. 6. The results of this diagram can be useful for better analyzing the driveability of the proposed design. From the simulation results it can be deduced that the proposed full adder cell works with high-efficiency at low voltages even with large capacitors.

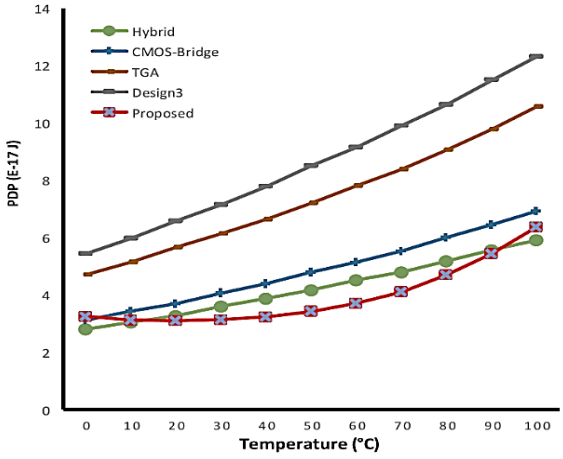


Fig. 5. PDP of circuits versus temperature changes

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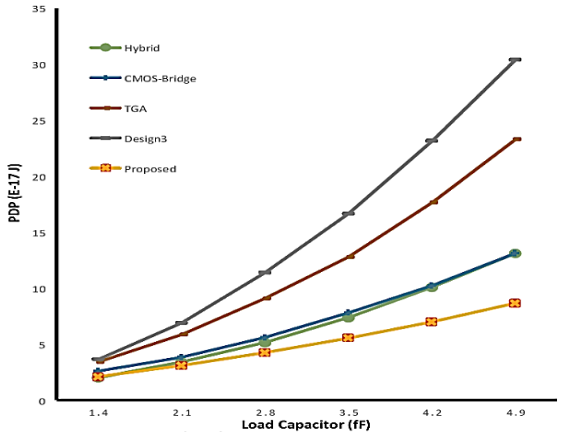
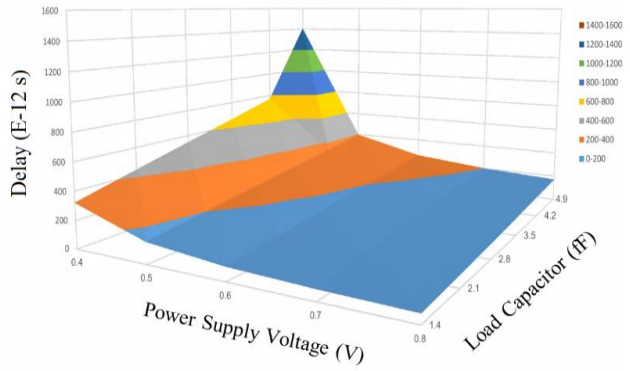


Fig. 6. PDP of circuits in terms of load capacitance changes

To investigate the driveability of the proposed full adder in detail, we simulated the proposed circuit at clock frequency of 500 MHz, input signal frequency of 100 MHz, and supply voltages in the range of 0.8 V to 0.4 V using a large number of load capacitances in the range of 1.4 fF to 4.9 fF. The results of this experiment are plotted in three-dimensional graphs, shown in Figures 7(a), 7(b) and 7(c), respectively, for propagation delay, power consumption, and PDP. The results of these charts can be useful for better analyzing the driveability of the proposed scheme. From the simulation results it can be deduced that the proposed full adder cell works with high-efficiency at low voltages even with large capacitors. The proposed full adder at supply voltage of 0.4 V can still work well. According to the simulation results, at supply voltage of 0.4 V and load capacitance of 1.4 fF to 4.9 fF, the propagation delay changes in the range of 0.32 ns to 1.4 ns, the average power consumption changes in the range of 73.2 nW to 105.12 nW, and PDP changes in the range of 23.6 aJ to 147.21 aJ. The value of leakage power at this operating voltage is 0.14 nW. These values indicate the excellent performance of the FinFET-based design at very low voltage and high load capacitance.



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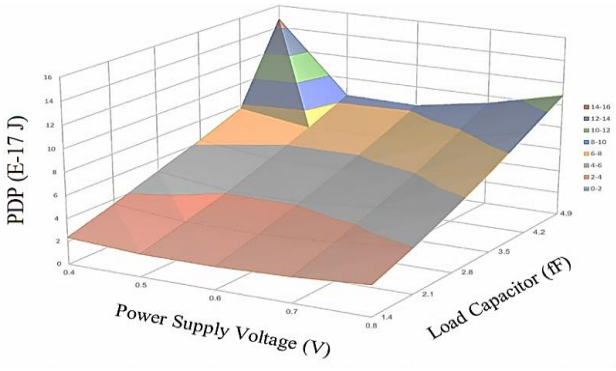

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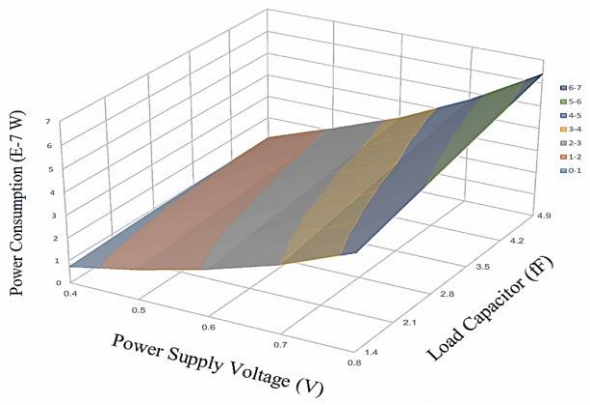

(c)

Fig. 7. Variations of power supply voltage and load capacitance of the proposed full adder and its impact on (a) propagation delay, (b) average power consumption, and (c) PDP

V. Conclusion

In this paper, a high-speed low-PDP FinFET-based full adder for low voltage applications was proposed. The proposed full adder at supply voltage of 0.4 V can still work well. According to the simulation results, at the supply voltage of 0.4 V and load capacitance of 1.4 fF to 4.9 fF, the propagation delay changes in the range of 0.32 ns to 1.4 ns, the average power consumption changes in the range of 73.2 nW to 105.125 nW, and PDP changes in the range of 23.6 aJ to 147.21 aJ. The value of leakage power at this operating voltage is 0.14 nW. These values indicate the excellent performance of the FinFET-based design at very low voltage and high capacitance.

References

[1] D.A. Neamen, B. Pevzner, Semiconductor physics and devices: basic principles, vol. 3, McGraw-Hill New York, 2003.

[2] G. Sery, S. Borkar, V. De, "Life is CMOS: Why chase life after? ," In Proceedings of the IEEE/ACM international design automation conference, 2002, pp. 78–83.

[3] V. De, S. Borkar, "Technology and design challenges for low power and high performance," In Proceedings of the IEEE/ACM international symposium on low power electronics and design, 2002, pp. 163–168.

[4] Y. Taur, "CMOS design near the limit of scaling. IBM Journal of Research and Development," 46 (2/3), 2002, pp. 213–221.

[5] F. M. Hernandez, M. L. Aranda, V. Champac, "Noise tolerant improvement in dynamic CMOS logic circuit," IEEE Proceedings Circuits Devices Systems, 153(6), 2006, pp. 565–573.

[6] A. Baghi Rahin, V. Baghi Rahin, "Ultra-Low-Voltage and High-Speed 1-Bit Full Adder Cell Using FinFET Transistors for Mobile

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EISSN: 2305-0543, PISSN: 2411-6173

Applications", International Journal of Mechatronics, Electrical and Computer Technology (IJMEC), 8(28), 2018, pp. 3847-3858.

[7] A. Baghi Rahin, V. Baghi Rahin, "Ultra low voltage and low power 4-2 compressor using FinFET transistors", Journal of Intelligent Procedures in Electrical Technology (JIPET), 9(33), 2018, pp. 25-36.

[8] K. Navi, S. Sayedsalehi, R. Farazkish, M. Rahimi Azghadi, "Five-Input Majority Gate, a New Device for Quantum-Dot Cellular Automata," Journal of Computational and Theoretical Nanoscience, 7(8), 2010, pp.1546-1553.

[9] A.K. Abu El-Seoud, M. El-Banna, M.A. Hakim, "On modelling and characterization of single electron transistor", International Journal of Electronics, 94(6), 2007, pp. 573-585.

[10] A. Baghi Rahin, V. Baghi Rahin, "A New 2-input CNTFET-Based XOR Cell With Ultra-Low Leakage Power For Low-Voltage and Low-Power Full Adders," Journal of Intelligent Procedures in Electrical Technology (JIPET), 10(37), 2019, pp. 13-22.

[11] A. Marshall, S. Natarajan, SOI Design: Analog, Memory and Digital Techniques, Springer, 2002.

[12] D. Soudris, C. Piguet, C. Goutis, Designing CMOS Circuits for Low Power, Kluwer Academic Publishers, 2002.

[13] F.H.A. Asgari, M. Sachdev, "A low-power reduced swing global clocking methodology," IEEE Transactions on Very Large Scale Integration (VLSI) Systems,vol.12, no.5, 2004, pp. 538–545.

[14] P. Verma, A.K. Sharma, A. Noor, V.S. Pandey, "SDTSPC-technique for low power noise aware 1-bit full adder," Analog Integr Circ Sig Process, 92(2), 2017, pp. 303-314.

[15] B. Razavi, Design of analog CMOS integrated circuits, Mc-Graw hill, 2002.

[16] R.X., Gu, M.I., Elmasry, "Power dissipation analysis and optimization for deep submicron CMOS digital circuits," IEEE Journal Solid-State Circuits, 31, 1996, pp. 707–713.

[17] S. Katrue, D. Kudithipudi, "GALEOR: Leakage reduction for CMOS circuits," 15th IEEE International Conference on Electronics, Circuits and Systems, St. Julien's, 2008, pp. 574-577.

[18] D. Flandre, O. Bulteel, G. Gosset, B. Rue, D. Bol, "Ultra-low-power analog and digital circuits and micro systems using disruptive ultra-low-leakage design techniques," 2012 8th International Caribbean Conference on Devices, Circuits and Systems (ICCDCS), Playa del Carmen, 2012, pp. 1-2.

[19] http://ptm.asu.edu/

[20] C.H. Chang, J. Gu, M. Zhang, "A review of 0.18-μm full adder performances for tree structured arithmetic circuits," IEEE Trans. Very Large Scale Integr. (VLSI) Syst.13(6), 2005, pp. 686–695.

[21] O. Kavehei, M. Rahimi Azghadi, K. Navi, A.P. Mirbaha, "Design of robust and high-performance 1-Bit CMOS full adder for nanometer design," IEEE Computer Society Annual Symposium on VLSI (ISVLSI), Montpellier, France, 2008, pp. 10–15.

[22] N. West, K. Eshragian, Principles of CMOS VLSI Design: A systems Perspective, Addison-wesley, 1993.

[23] M. Ghadiry, M. Nadi, A. KhariA'Ain, "Discrepant low PDP 8-Bit adder," Circ. Syst. Signal Process. 32(1), 2013, pp. 1–14.

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