AMP DISPLAY INC.

A Brighter Solution

SPECIFICATIONS

TFT MODULE

CUSTOMER:	
CUSTOMER PART NO.	
AMP DISPLAY PART NO.	
APPROVED BY:	
DATE:	

☐ APPROVED FOR SPECIFICATIONS

☐ APPROVED FOR SPECIFICATION AND PROTOTYPES

AMP DISPLAY INC

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RECORD OF REVISION

Revision Date	Page	Contents	Editor
2008/02/15	-	New Release	Emil
2008/05/27	18	Addition protocol of SPI I/F.	Emil
2008/06/23	-	Release the official part No. to AM-240320METNQW-00H.	Emil
2008/07/07	10	Correction the Gate and Source scan direction.	Emil

1 Features

This single-display module is suitable for cell phone application. The Main-LCD adopts one backlight with High brightness 4-lamps white LED.

(1) Construction: 2.8" a-Si color TFT-LCD, White LED Backlight, and FPCB.

(2) Main LCD: 2.1 Amorphous-TFT 2.8 inch display, transmissive, Normally white type, 12 o'clock.
2.2 240(RGB)×320 dots Matrix,1/320 Duty.
2.3 Main LCD Driver IC: ILI9320.
2.4 Real 262K colors display (18bit Interface mode).

(3) Low cross talk by frame rate modulation.
(4) Direct data display with display RAM.
(5) Partial display function: You can save power by limiting the display space.
(6) MPU interface: 8/9/16/18-bit 80-Series, parallel interface and SPI interface.
(7) Digital RGB interface: 18bit and 6bit Digital RGB interface.
(8) Abundant command functions:
Area scroll function
Display direction switching function
Power saving function
Electric volume control function: you are able to program the temperature compensation function.

2 Mechanical specifications

Dimensions and weight

Item		Specifications	Unit
External shape dimensions		*1 50.2 (W) x 69.2 (H) .	mm
Main LCD	Pixel size	0.18 (W) x 0.18 (H)	mm
	Active area	43.2 (W) x 57.6 (H)	mm
	Number of Pixels	240(H)x320(V) pixels	mm
Weight		TBD	g

*1. This specification is about External shape on shipment from AMPIRE.

3 Absolute max. ratings and environment

3-1 Absolute max. ratings

Ta=25°C GND=0V

Item	Symbol	Min.	Max.	Unit	Remarks
Power voltage	VCC – GND	-0.3	+4.6	V	
Power voltage	VCI – GND	-0.3	+4.6	V	
Power voltage	LED A – LED K	-0.5	+4.0	V	
Input voltage	VIN	-0.5	VDD	V	

3-2 Environment

Item	Specifications	Remarks
Storage temperature	Max. +70℃ Min. -20℃	Note 1: Non-condensing
Operating temperature	Max. +60 ℃ Min. -10 ℃	Note 1: Non-condensing

Note 1：Ta≦+40℃・・・・Max.85%RH

Ta＞+40℃・・・・The max. humidity should not exceed the humidity with 40℃ 85%RH.

4 Electrical specifications

4-1 Electrical characteristics of LCM

(V_{DD}=3.0V, Ta=25 °C)

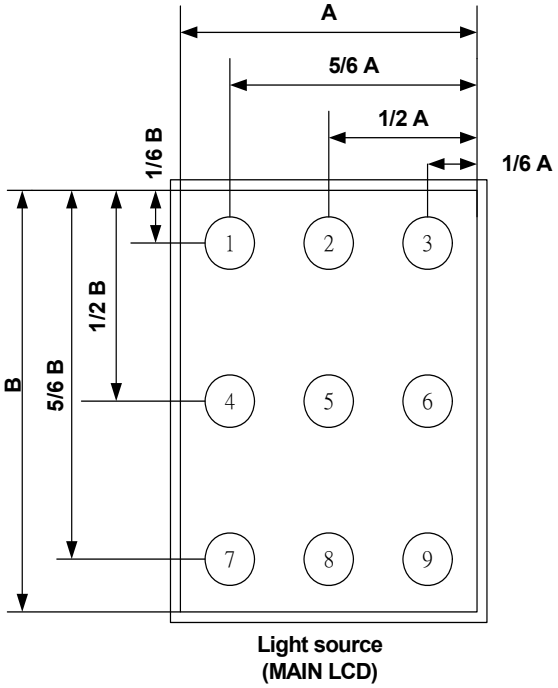
Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
IC power voltage	V_{cc}		2.6	2.8	3.3	V
IC power voltage	V_{ci}		2.6	2.8	3.3	
High-level input voltage	V_{IHC}		0.8V_{DD}		V_{DD}	V
Low-level input voltage	V_{ILC}		0		0.2V_{DD}	V
Consumption current of VDD	I_{DD}	LED OFF	-	8	-	mA
Consumption current of LED	I_{LED_ON}	V_{LED_ON}=3.6V	-	80	-	mA

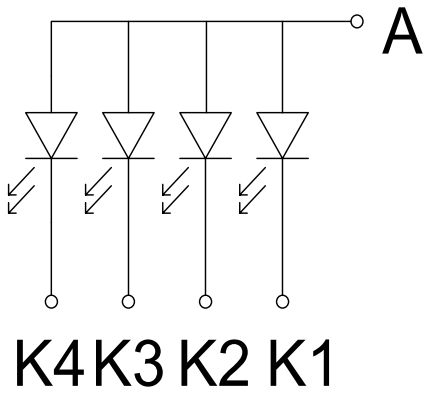
※ 1. 1/320 duty.

4-2 LED back light specification

Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Forward voltage	V_f	I_f =80mA	2.9	3.3	3.6	V
Reverse voltage	V_r		-	-	12	V
Forward current	I_f	4-chip Parallel	75	80	85	mA
Power Consumption	P_{BL}	I_f =80mA	-	288	-	mW
Uniformity (with L/G)	-	I_f=80mA	80%*1	-	-	
Bare LED Luminous intensity	V_f I_f	3.6V 80mA	3000	-	-	cd/m^2
Luminous color	White					
Chip connection	4 chip parallel connection					

Bare LED measure position:





*1 Uniformity (LT): $\frac{Min(P1 \sim P9)}{Max(P1 \sim P9)} \times 100 \geq 80\%$

5 Optical characteristics

Main LCD

5.1 Optical characteristics

(1/320 Duty in case except as specified elsewhere Ta = 25°C)

LED backlight transmissive module:

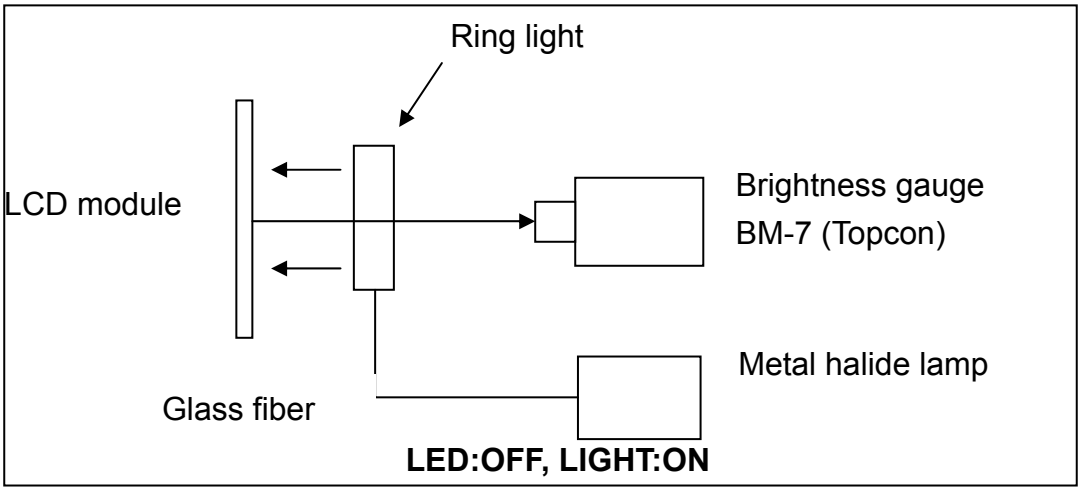
Item	Symbol	Temp.	Min.	Std.	Max.	Unit	Conditions
Response time	Tr	25°C	--	15	25	ms	θ=0°,φ=0° (Note 2)
	Tf	25°C	--	20	30		
Contrast ratio	CR	25°C	200	300	-	-	θ=0°, φ=0° LED:ON, LIGHT:OFF (Note 4)
Transmittance	T	25°C	5.7	6.0	-	%	
NTSC	%	25°C	50	55			
Visual angle range front and rear	θ	25°C	(θf) 60 (θb) 60			De-gree	φ= 0°, CR≧10 LED:ON LIGHT:OFF (Note 3)
Visual angle range left and right	θ	25°C	(θl) 70 (θr) 70			De-gree	φ=90°, CR≧10 LED:ON LIGHT:OFF (Note 3)
Visual angle direction priority			12:00				(Note 5)
Brightness			225	250	--	Cd/m2	V_{LED}=3.6V, 80mA Full White pattern

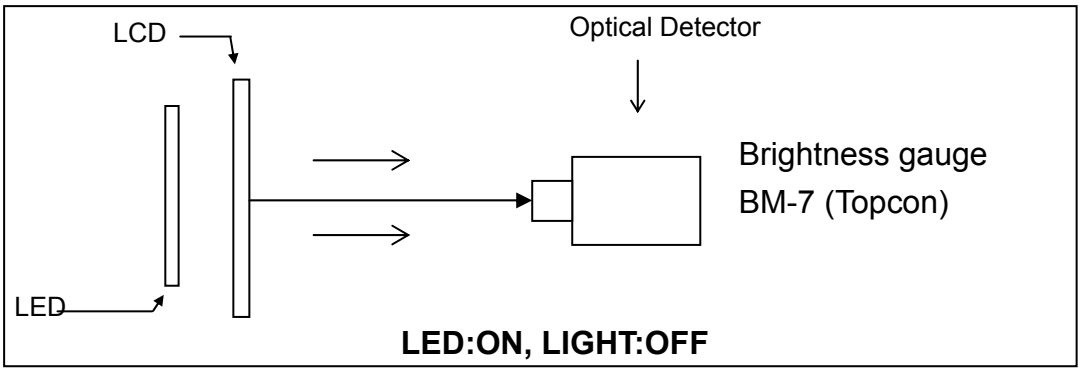
5.2 CIE (x, y) chromaticity (1/320 Duty Ta = 25°C)

Item	Symbol	Transmissive			Conditions
		Min.	Typ.	Max.	
Red	X	(0.590)	(0.620)	(0.650)	θ=0°,φ=0°
	Y	(0.310)	(0.340)	(0.370)	
Green	X	(0.303)	(0.333)	(0.363)	θ=0°,φ=0°
	Y	(0.564)	(0.594)	(0.624)	
Blue	X	(0.132)	(0.152)	(0.182)	θ=0°,φ=0°
	Y	(0.196)	(0.116)	(0.146)	
White	X	(0.275)	(0.305)	(0.335)	θ=0°,φ=0°
	Y	(0.294)	(0.324)	(0.354)	

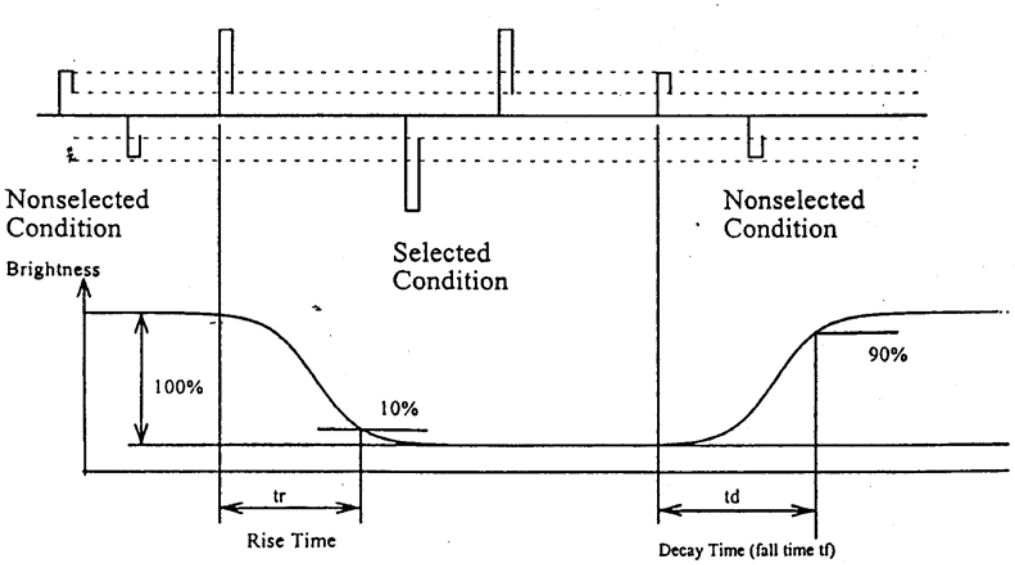
( ) is a default

NOTE 1: Optical characteristic measurement system

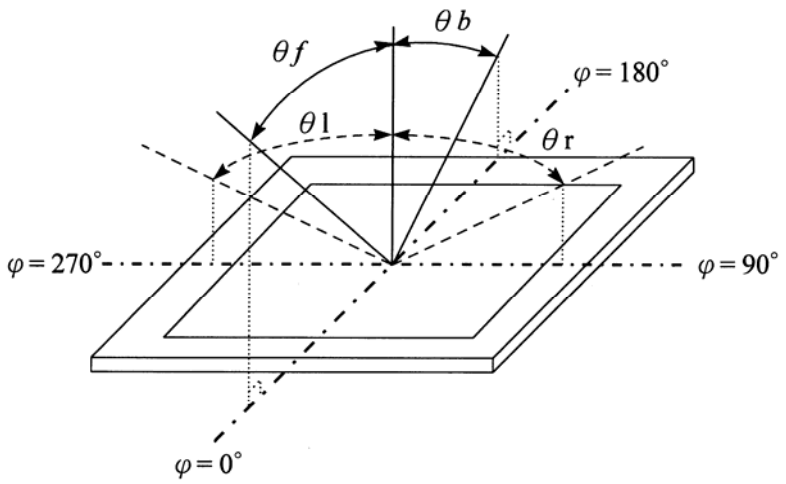




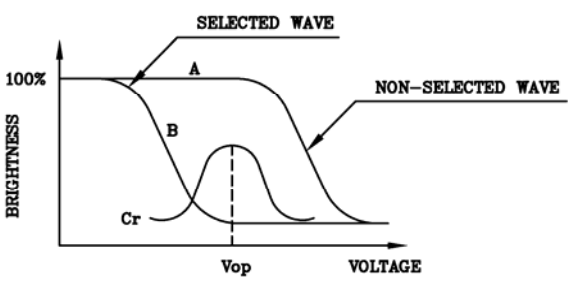
NOTE 2: Response tome definition



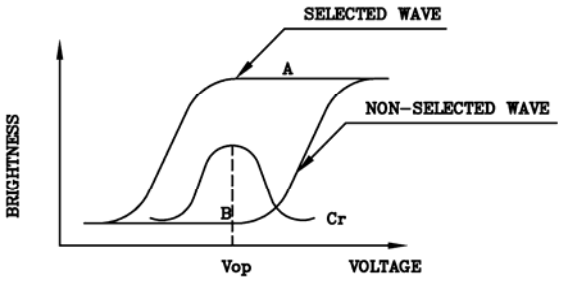
NOTE 3: φ、θ definition



NOTE 4: Contrast definition



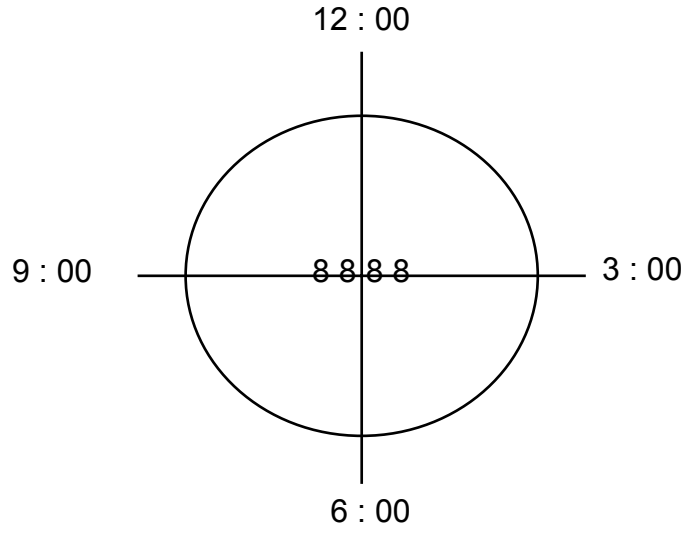
(positive type)



(negative type)

Contrast Ratio : Cr=A/B

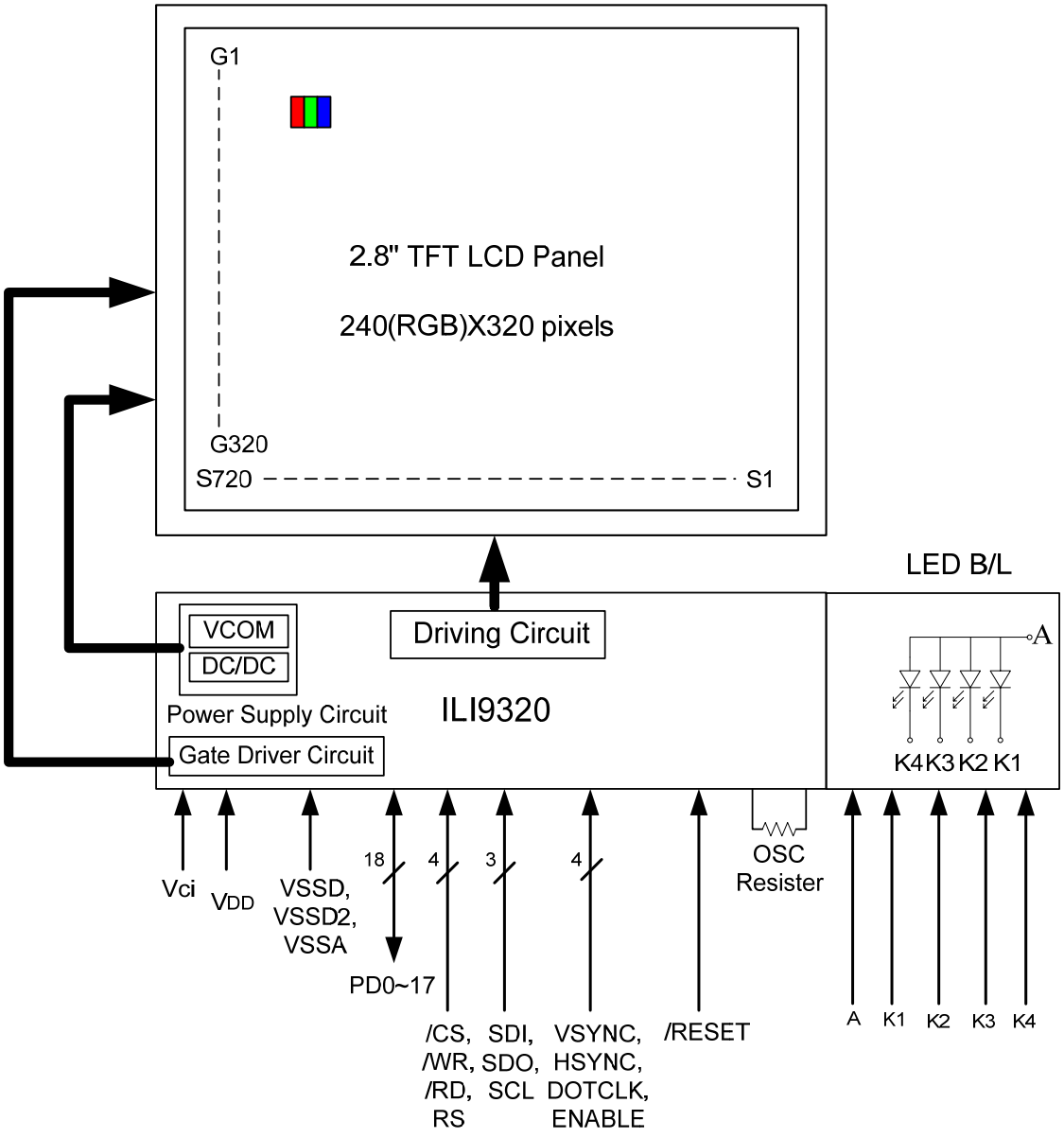
NOTE 5: Visual angle direction priority



6 Block Diagram

Block diagram (Main LCD)

Display format: A-Si TFT transmissive, Normally white type, 12 o'clock.
Display composition: 240 × RGB × 320 dots
LCD Driver: ILI9320
Back light: White LED × 4 (I_{LED}=80mA)



7 Interface specifications

<table>
<tr><th>Pin No.</th><th>Terminal</th><th>Functions</th></tr>
<tr><td>1</td><td rowspan="4">NC</td><td rowspan="4">No Connection.</td></tr>
<tr><td>2</td></tr>
<tr><td>3</td></tr>
<tr><td>4</td></tr>
<tr><td>5</td><td>GND</td><td>GND-terminal.</td></tr>
<tr><td>6</td><td>/CS</td><td>Chip select signal.
Fix to GND level when not in use.</td></tr>
<tr><td>7</td><td>RS</td><td>A register select signal.
Low: select an index or status register.
High: select a control register.
Fix to GND level when not in use.</td></tr>
<tr><td>8</td><td>WR/SCL</td><td>A write strobe signal and enables an operation to write data when the signal is low.
Fix to VCC level when not in use.
SPI Mode:
Synchronizing clock signal in SPI mode.</td></tr>
<tr><td>9</td><td>RD</td><td>A read strobe signal and enables an operation to read out data when the signal is low.
Fix to VCC level when not in use.</td></tr>
<tr><td>10</td><td>SDI</td><td>Serial bus interface data input pin.
Fix to GND level when not in use.</td></tr>
<tr><td>11</td><td>SDO</td><td>Serial bus interface data output pin.
Let SDO as open when not in use.</td></tr>
<tr><td>12</td><td>DB0/PD0</td><td rowspan="18"><table>
<tr><th>Mode</th><th>DB Pin in use</th></tr>
<tr><td>MCU 18-bit</td><td>DB [17:0]</td></tr>
<tr><td>MCU 16-bit</td><td>DB [17:10],
DB[8:1]</td></tr>
<tr><td>MCU 9-bit</td><td>DB [17:9]</td></tr>
<tr><td>MCU 8-bit</td><td>DB [17:10]</td></tr>
<tr><td>Serial Mode/Digital RGB Interface Mode</td><td>SDI, SDO/ PD [17:0]
R[5:0]=PD[5:0]
G[5:0]=PD[11:6]
B[5:0]=PD[17:12]</td></tr>
</table></td></tr>
<tr><td>13</td><td>DB1/PD1</td></tr>
<tr><td>14</td><td>DB2/PD2</td></tr>
<tr><td>15</td><td>DB3/PD3</td></tr>
<tr><td>16</td><td>DB4/PD4</td></tr>
<tr><td>17</td><td>DB5/PD5</td></tr>
<tr><td>18</td><td>DB6/PD6</td></tr>
<tr><td>19</td><td>DB7/PD7</td></tr>
<tr><td>20</td><td>DB8/PD8</td></tr>
<tr><td>21</td><td>DB9/PD9</td></tr>
<tr><td>22</td><td>DB10/PD10</td></tr>
<tr><td>23</td><td>DB11/PD11</td></tr>
<tr><td>24</td><td>DB12/PD12</td></tr>
<tr><td>25</td><td>DB13/PD13</td></tr>
<tr><td>26</td><td>DB14/PD14</td></tr>
<tr><td>27</td><td>DB15/PD15</td></tr>
<tr><td>28</td><td>DB16/PD16</td></tr>
<tr><td>29</td><td>DB17/PD17</td></tr>
</table>

30	/RESET	A Reset pin.
31	ENABLE	A data ENABLE signal in RGB I/F mode. ***Fix to GND level when not in use.***
32	DOTCLK	Dot clock signal in RGB I/F mode. ***Fix to GND level when not in use.***
33	HSYNC	Frame synchronizing signal in RGB I/F mode. ***Fix to GND level when not in use.***
34	VSYNC	Frame synchronizing signal in RGB I/F mode. ***Fix to GND level when not in use.***
35	VCC	A supply voltage to the internal logic: VCC = 2.4~3.3V.
36	VCC	
37	VCI	A supply voltage to the analog circuit. Connect to an external power supply of 2.5 ~ 3.3V.
38	GND	GND-terminal.
39	LED_A	LED Anode.
40	LED_K1	LED Cathode.
41	LED_K2	
42	LED_K3	
43	LED_K4	
44	GND	GND-terminal

Selection the System Interface mode

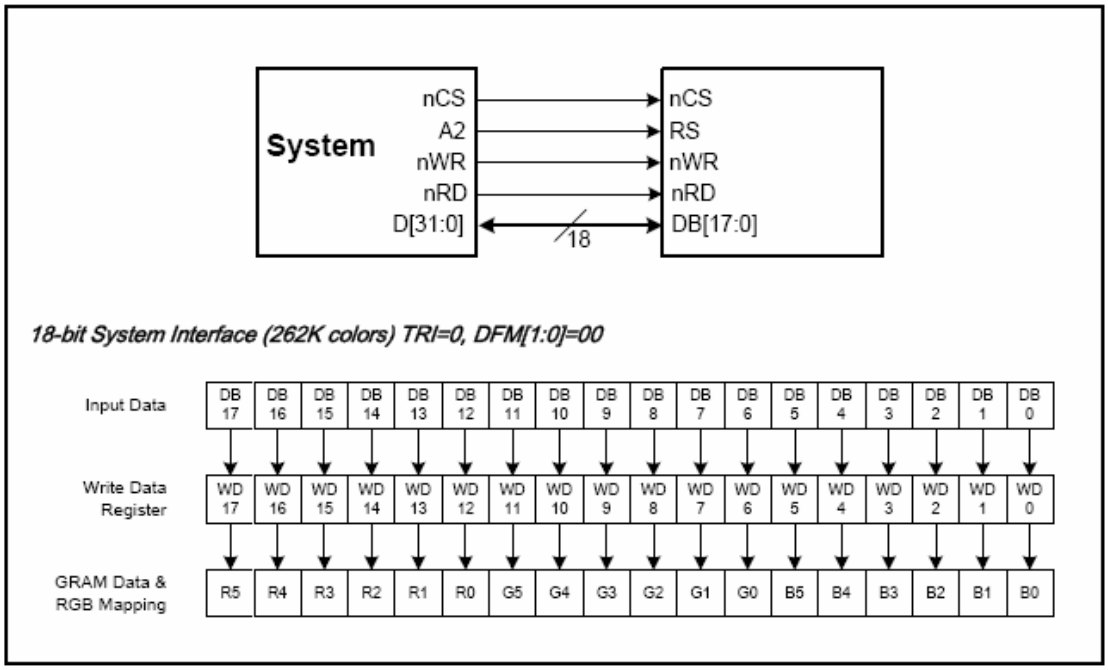
Mode	IM3 (JP3	IM2 (JP2	IM1 (JP1	IM0 (JP0
MCU-18Bit	H	L	H	L
MCU-16 Bit	L	L	H	L
MCU-9 Bit	H	L	H	H
MCU-8 Bit	L	L	H	H
*Serial Mode/Digital RGB Interface Mode	**L**	**H**	**L**	**L**

***Jumper Default: JP1= "L" JP2= "L" JP3= "H" JP4= "L"**

8 System interface and RGB interface

8.1 80-system 18-bit interface

The i80/18-bit system interface is selected by setting the IM[3:0] as "1010" levels.

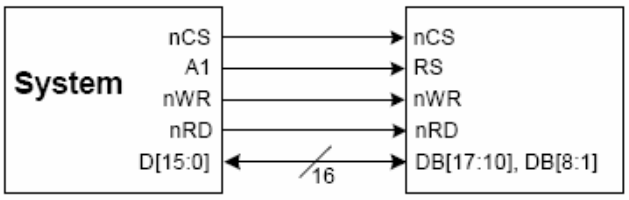


18-bit System Interface (262K colors) TRI=0, DFM[1:0]=00

Input Data	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 9	DB 8	DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 1	DB 0
Write Data Register	WD 17	WD 16	WD 15	WD 14	WD 13	WD 12	WD 11	WD 10	WD 9	WD 8	WD 7	WD 6	WD 5	WD 4	WD 3	WD 2	WD 1	WD 0
GRAM Data & RGB Mapping	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0

8.2 80-system 16-bit interface

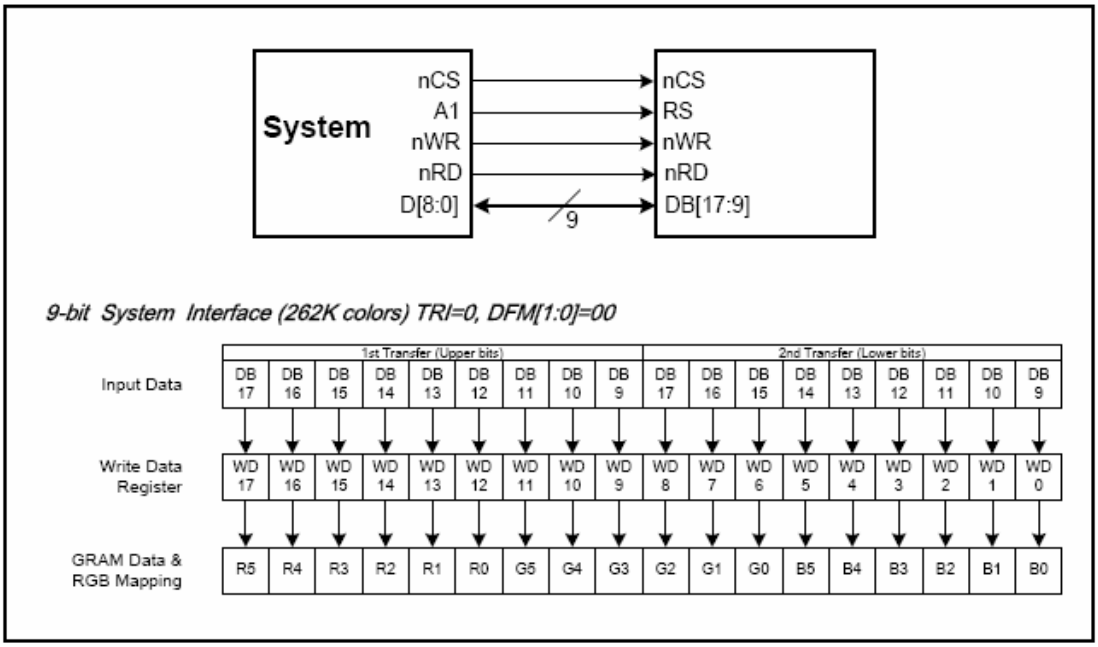
The i80/16-bit system interface is selected by setting the IM[3:0] as "0010" levels. The 262K or 65K color can be display through the 16-bit MPU interface. When the 262K color is displayed, two transfers (1st transfer: 2 bits, 2nd transfer: 16 bits or 1st transfer: 16 bits, 2nd transfer: 2 bits) are necessary for the 16-bit CPU interface.



TRI	DFM	16-bit MPU System Interface Data Format
0	*	system 16-bit interface (1 transfers/pixel) 65,536 colors
1	0	80-system 16-bit interface (2 transfers/pixel) 262,144 colors
1	1	80-system 16-bit interface (2 transfers/pixel) 262,144 colors

8.3 80-system 9-bit interface

The i80/9-bit system interface is selected by setting the IM[3:0] as "1011" and the DB17~DB9 pins are used to transfer the data. When writing the 16-bit register, the data is divided into upper byte (8 bits and LSB is not used) lower byte and the upper byte is transferred first. The display data is also divided in upper byte (9 bits) and lower byte, and the upper byte is transferred first. The unused DB[8:0] pins must be tied to either Vcc or AGND.



9-bit System Interface (262K colors) TRI=0, DFM[1:0]=00

	1st Transfer (Upper bits)									2nd Transfer (Lower bits)								
Input Data	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 9	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 9
Write Data Register	WD 17	WD 16	WD 15	WD 14	WD 13	WD 12	WD 11	WD 10	WD 9	WD 8	WD 7	WD 6	WD 5	WD 4	WD 3	WD 2	WD 1	WD 0
GRAM Data & RGB Mapping	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0

8.4 80-system 8-bit interface

The i80/8-bit system interface is selected by setting the IM[3:0] as "0011" and the DB17~DB10 pins are used to transfer the data. When writing the 16-bit register, the data is divided into upper byte (8 bits and LSB is not used) lower byte and the upper byte is transferred first. The display data is also divided in upper byte (8 bits) and lower byte, and the upper byte is transferred first. The written data is expanded into 18 bits internally (see the figure below) and then written into GRAM. The unused DB[9:0] pins must be tied to either Vcc or AGND.

TRI	DFM	8-bit MPU System Interface Data Format
0	*	system 8-bit interface (2 transfers/pixel) 65,536 colors
1	0	80-system 8-bit interface (3 transfers/pixel) 262,144 colors
1	1	80-system 8-bit interface (3 transfers/pixel) 262,144 colors

Data transfer synchronization in 8/9-bit bus interface mode

ILI9320 supports a data transfer synchronization function to reset upper and lower counters which count the transfers numbers of upper and lower byte in 8/9-bit interface mode. If a mismatch arises in the numbers of transfers between the upper and lower byte counters due to noise and so on, the "00"h register is written 4 times consecutively to reset the upper and lower counters so that data transfer will restart with a transfer of upper byte. This synchronization function can effectively prevent display error if the upper/lower counters are periodically reset.

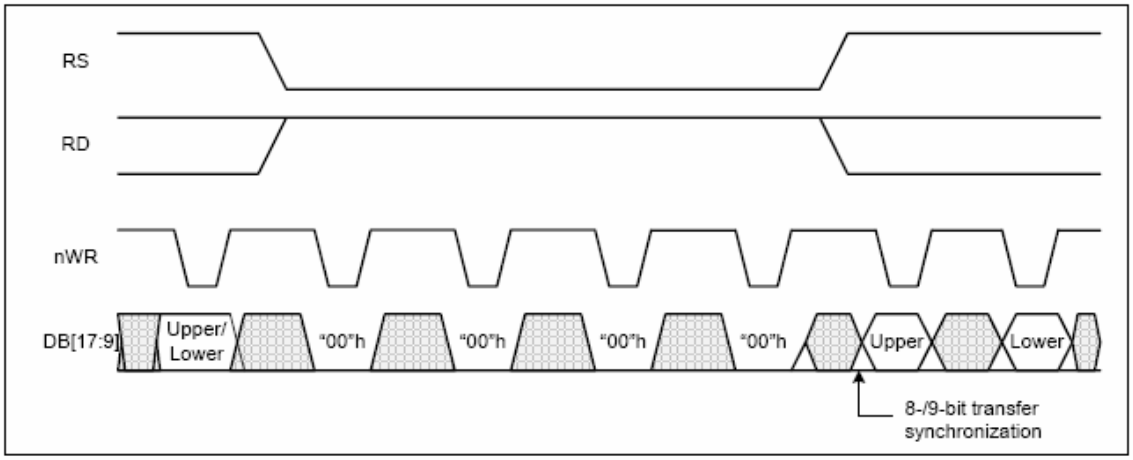


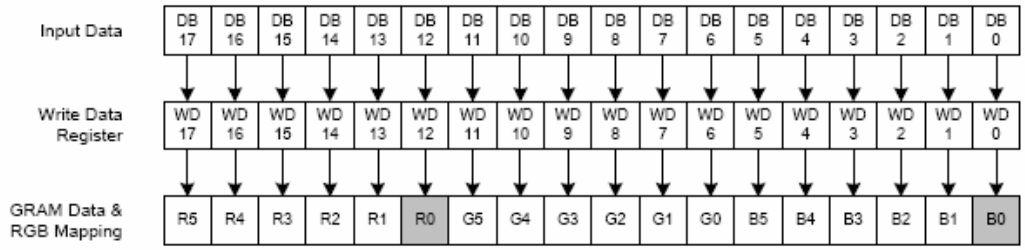
Figure6 Data Transfer Synchronization in 8/9-bit System Interface

8.5 RGB interface

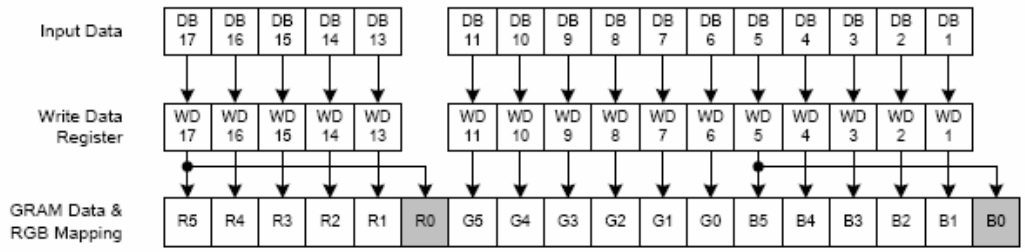
The RGB Interface mode is available for ILI9320 and the interface is selected by setting the RIM[1:0] bits as following table.

RIM1	RIM0	RGB Interface	DB pins
0	0	18-bit RGB Interface	DB[17:0]
0	1	16-bit RGB Interface	DB[17:13], DB[11:1]
1	0	6-bit RGB Interface	DB[17:12]
1	1	Setting prohibited	

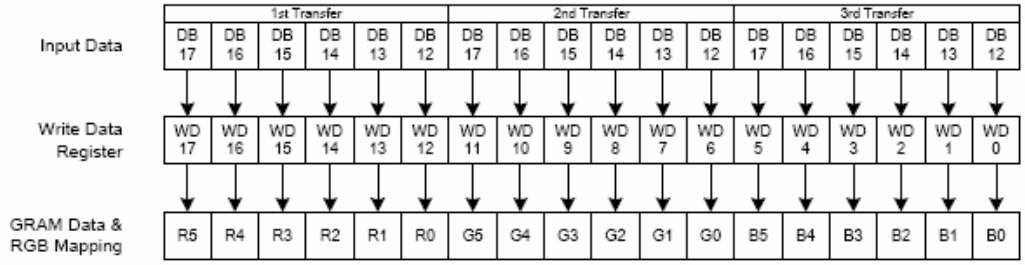
18-bit RGB Interface (262K colors)



16-bit RGB Interface (65K colors)



6-bit RGB Interface (262K colors)



8.6 Serial Peripheral Interface (SPI)

The Serial Peripheral Interface (SPI) is selected by setting the IM[3:0] pins (in FPC side) as “010x” level. The chip select pin (nCS), the serial transfer clock pin (SCL), the serial data input pin (SDI) and the serial data output pin (SDO)are used in SPI mode. The ID pin sets the least significant bit of the identification code. The DB[17:0] pins, which are not used, must be tied to DGND.

The SPI interface operation enables from the falling edge of nCS and ends of data transfer on the rising edgeof nCS. The start byte is transferred to start the SPI interface and the read/write operation and RS information are also included in the start byte. When the start byte is matched, the subsequent data is received by ILI9320.

The seventh bit of start byte is RS bit. When RS = “0”, either index write operation or status read operation is executed. When RS = “1”, either register write operation or RAM read/write operation is executed. The eighth bit of the start byte is used to select either read or write operation (R/W bit). Data is written when the R/W bit is “0” and read back when the R/W bit is “1”.

After receiving the start byte, ILI9320 starts to transfer or receive the data in unit of byte and the data transfer starts from the MSB bit. All the registers of the ILI9320 are 16-bit format and receive the first and the second byte data as the upper and the lower eight bits of the 16-bit register respectively. In SPI mode, 5 bytes dummy read is necessary and the valid data starts from 6th byte of read back data.

Start Byte Format

Transferred bits	S	1	2	3	4	5	6	7	8
Start byte format	Transfer start	Device ID code						RS	R/W
		0	1	1	1	0	ID	1/0	1/0

Note: ID bit is selected by setting the IM0/ID pin.

RS and R/W Bit Function

RS	R/W	Function
0	0	Set an index register
0	1	Read a status
1	0	Write a register or GRAM data
1	1	Read a register or GRAM data

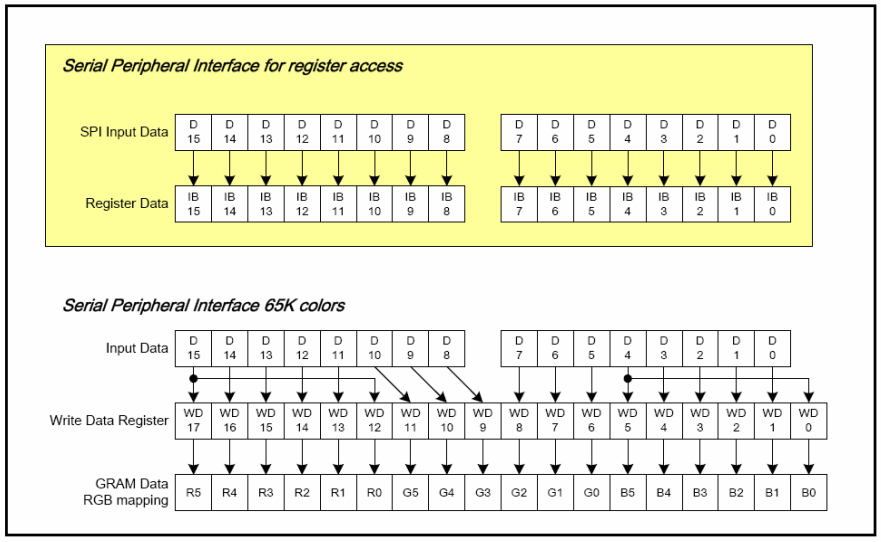


Figure 7 Data Format of SPI Interface

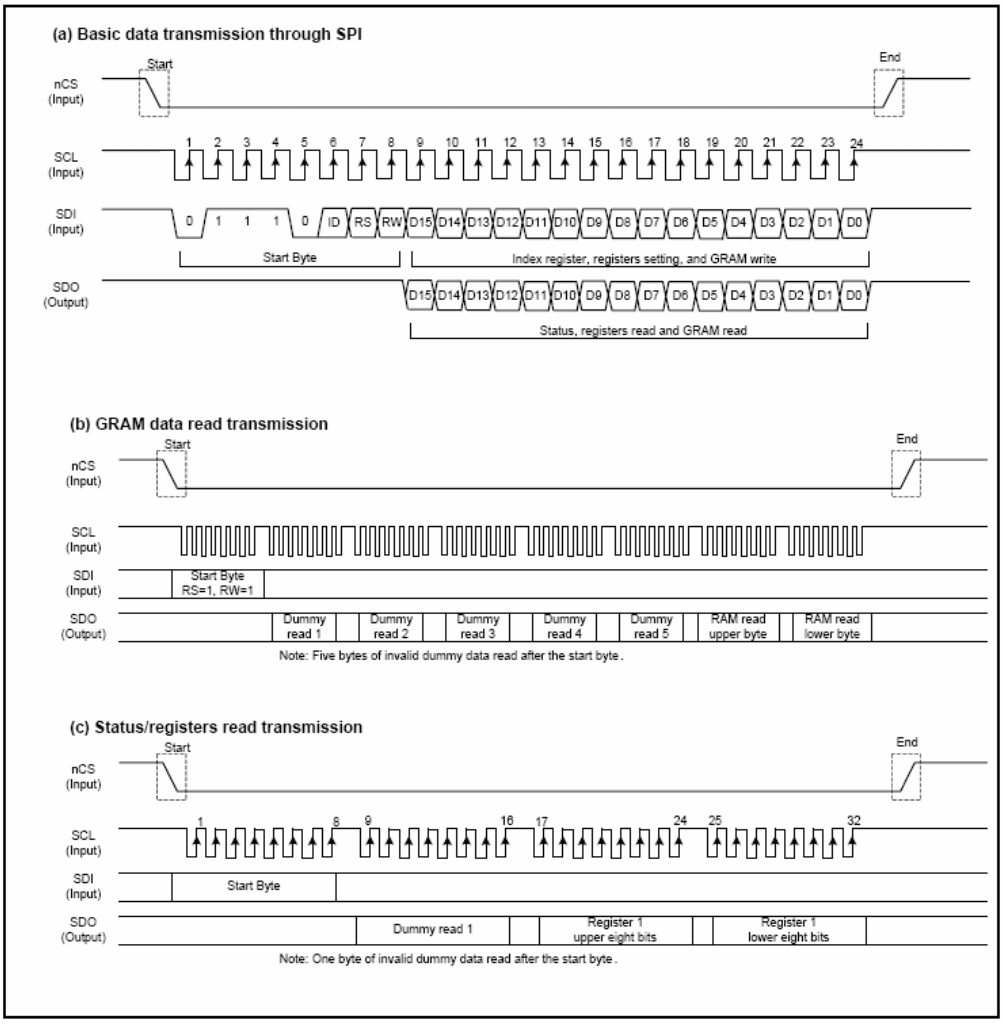
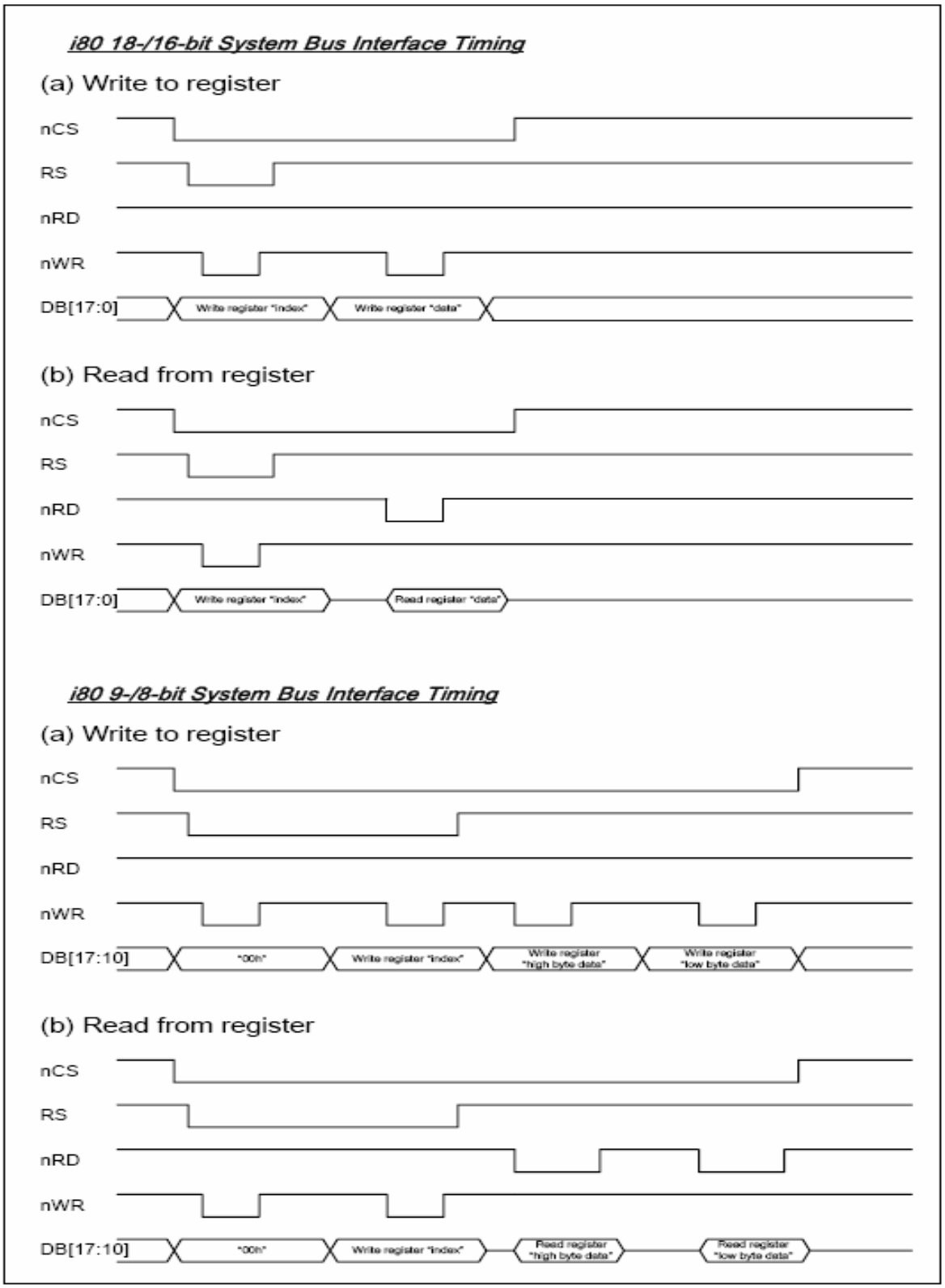


Figure8 Data transmission through serial peripheral interface (SPI)

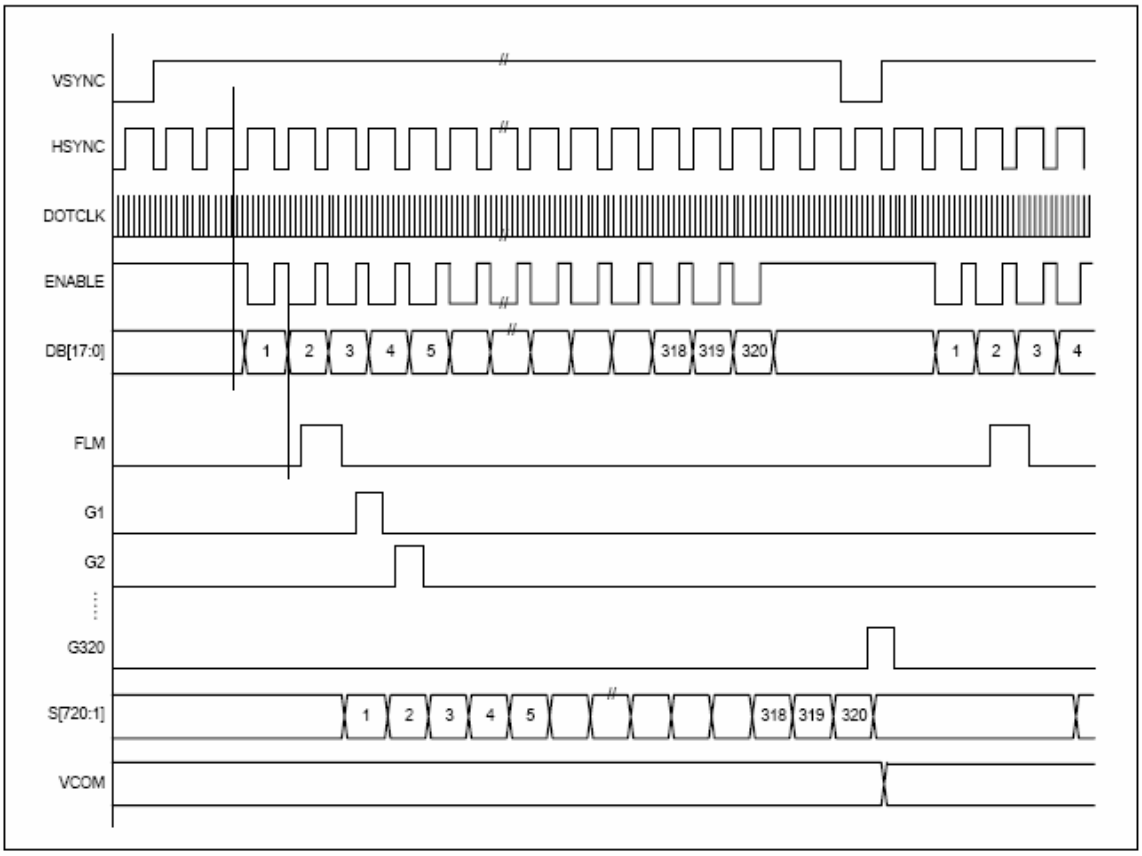
8.7 Timing of System Interface and RGB Interface

a. System Interface



b. RGB Interface

The following are diagrams of interfacing timing with LCD panel control signals in internal operation and RGB interface modes.



9 INSTRUCTION DESCRIPTIONS

9.1 Instruction List

Main LCD Driver IC: ILI9320

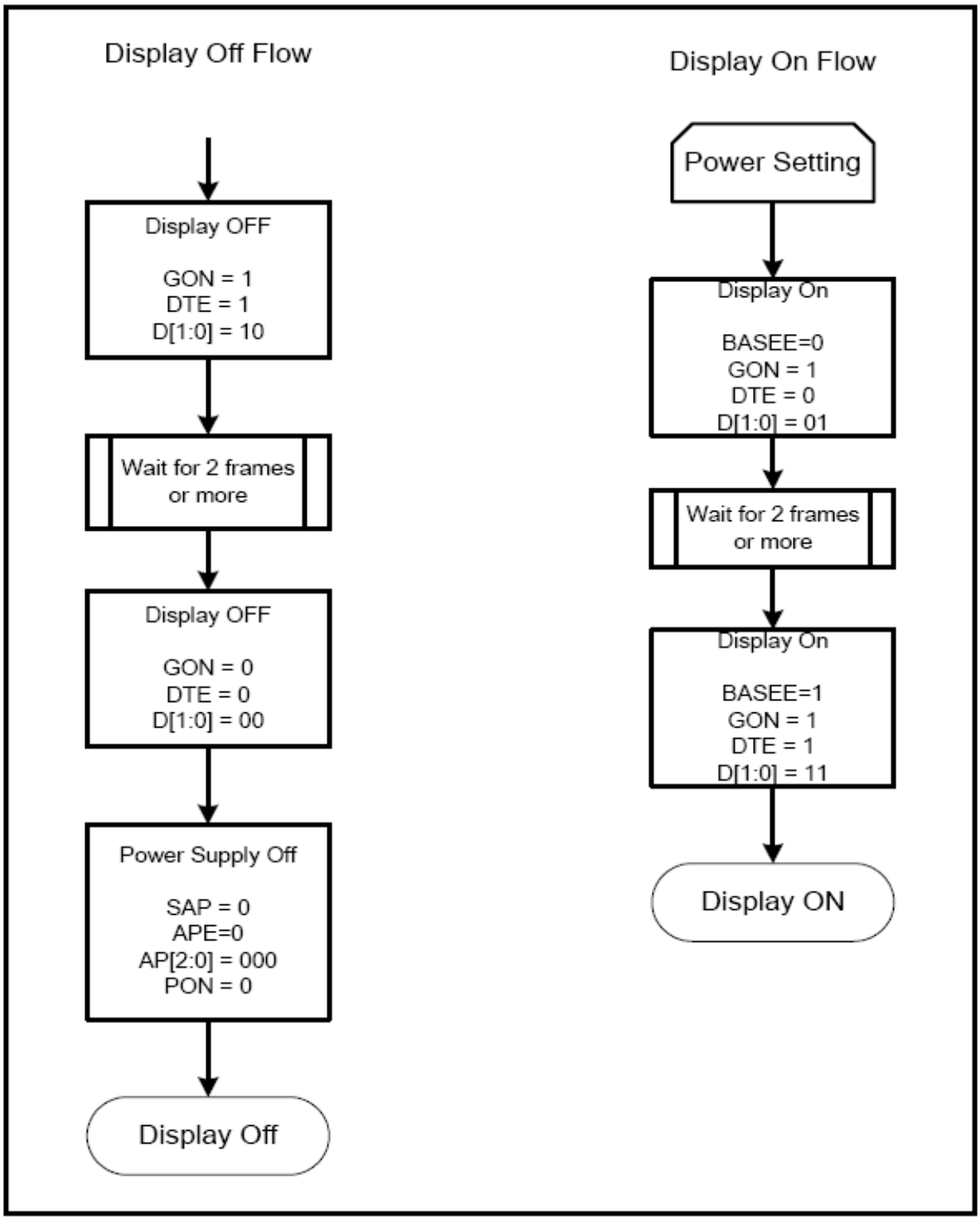
No.	Registers Name	R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
IR	Index Register	W	0	-	-	-	-	-	-	-	-	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
SR	Status Read	R	0	L7	L6	L5	L4	L3	L2	L1	L0	0	0	0	0	0	0	0	0
00h	Driver Code Read	R	1	1	0	0	1	0	0	1	0	0	0	1	0	0	0	1	0
00h	Start Oscillation	W	1	-	-	-	-	-		-	-		-	-	-	-	-	-	OSC
01h	Driver Output Control 1	W	1	0	0	0	0	0	SM	0	SS	0	0	0	0	0	0	0	0
02h	LCD Driving Control	W	1	0	0	0	0	0	1	B/C	EOR	0	0	0	0	0	0	0	0
03h	Entry Mode	W	1	TRI	DFM	0	BGR	0	0	HWM	0	ORG	0	I/D1	I/D0	AM	0	0	0
04h	Resize Control	W	1	0	0	0	0	0	0	RCV 1	RCV 0	0	0	RCH 1	RCH 0	0	0	RSZ1	RSZ0
07h	Display Control 1	W	1	0	0	PTD E1	PTD E0	0	0	0	BAS EE	0	0	GON	DTE	CL	0	D1	D0
08h	Display Control 2	W	1	0	0	0	0	FP3	FP2	FP1	FP0	0	0	0	0	BP3	BP2	BP1	BP0
09h	Display Control 3	W	1	0	0	0	0	0	PTS2	PTS1	PTS0	0	0	PTG1	PTG0	ISC3	ISC2	ISC1	ISC0
0Ah	Display Control 4	W	1	0	0	0	0	0	0	0	0	0	0	0	0	FMA RKO E	FMI2	FMI1	FMI0
0Ch	RGB Display Interface Control 1	W	1	ENC 2	ENC 1	ENC 0	0	0	0	0	RM	0	0	DM1	DM0	0	0	RIM1	RIM0
0Dh	Frame Maker Position	W	1	0	0	0	0	0	0	0	FMP 8	FMP 7	FMP 6	FMP 5	FMP 4	FMP 3	FMP 2	FMP 1	FMP 0
0Fh	RGB Display Interface Control 2	W	1	0	0	0	0	0	0	0	0	0	0	0	VSPL	HSP L	0	DPL	EPL
10h	Power Control 1	W	1	0	0	0	SAP	BT3	BT2	BT1	BT0	APE	AP2	AP1	AP0	0	DST B	SLP	0
11h	Power Control 2	W	1	0	0	0	0	0	DC12	DC11	DC10	0	DC02	DC01	DC00	0	VC2	VC1	VC0
12h	Power Control 3	W	1	0	0	0	0	0	0	0	VCM R	0	0	0	PON	VRH 3	VRH 2	VRH 1	VRH 0
13h	Power Control 4	W	1	0	0	0	VDV4	VDV3	VDV2	VDV1	VDV0	0	0	0	0	0	0	0	0
20h	Horizontal GRAM Address Set	W	1	0	0	0	0	0	0	0	0	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
21h	Vertical GRAM Address Set	W	1	0	0	0	0	0	0	0	AD16	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8
22h	Write Data to GRAM	W	1	RAM write data (WD17-0) / read data (RD17-0) bits are transferred via different data bus lines according to the selected interfaces.															
29h	Power Control 7	W	1	0	0	0	0	0	0	0	0	0	0	0	VCM 4	VCM 3	VCM 2	VCM 1	VCM 0
2Bh	Frame Rate and Color Control	W	1	0	0	0	0	0	0	0	0	EXT_ R	0	FR_S EL1	FR_S EL0	0	0	0	0
30h	Gamma Control 1	W	1	0	0	0	0	0	KP1[2]	KP1[1]	KP1[0]	0	0	0	0	0	KP0[2]	KP0[1]	KP0[0]
31h	Gamma Control 2	W	1	0	0	0	0	0	KP3[2]	KP3[1]	KP3[0]	0	0	0	0	0	KP2[2]	KP2[1]	KP2[0]
32h	Gamma Control 3	W	1	0	0	0	0	0	KP5[2]	KP5[1]	KP5[0]	0	0	0	0	0	KP4[2]	KP4[1]	KP4[0]
35h	Gamma Control 4	W	1	0	0	0	0	0	RP1[2]	RP1[1]	RP1[0]	0	0	0	0	0	RP0[2]	RP0[1]	RP0[0]

36h	Gamma Control 5	W	1	0	0	0	VRP1 [4]	VRP1 [3]	VRP1 [2]	VRP1 [1]	VRP1 [0]	0	0	0	VRP0 [4]	VRP0 [3]	VRP0 [2]	VRP0 [1]	VRP0 [0]
37h	Gamma Control 6	W	1	0	0	0	0	0	KN1[2]	KN1[1]	KN1[0]	0	0	0	0	0	KN0[2]	KN0[1]	KN0[0]

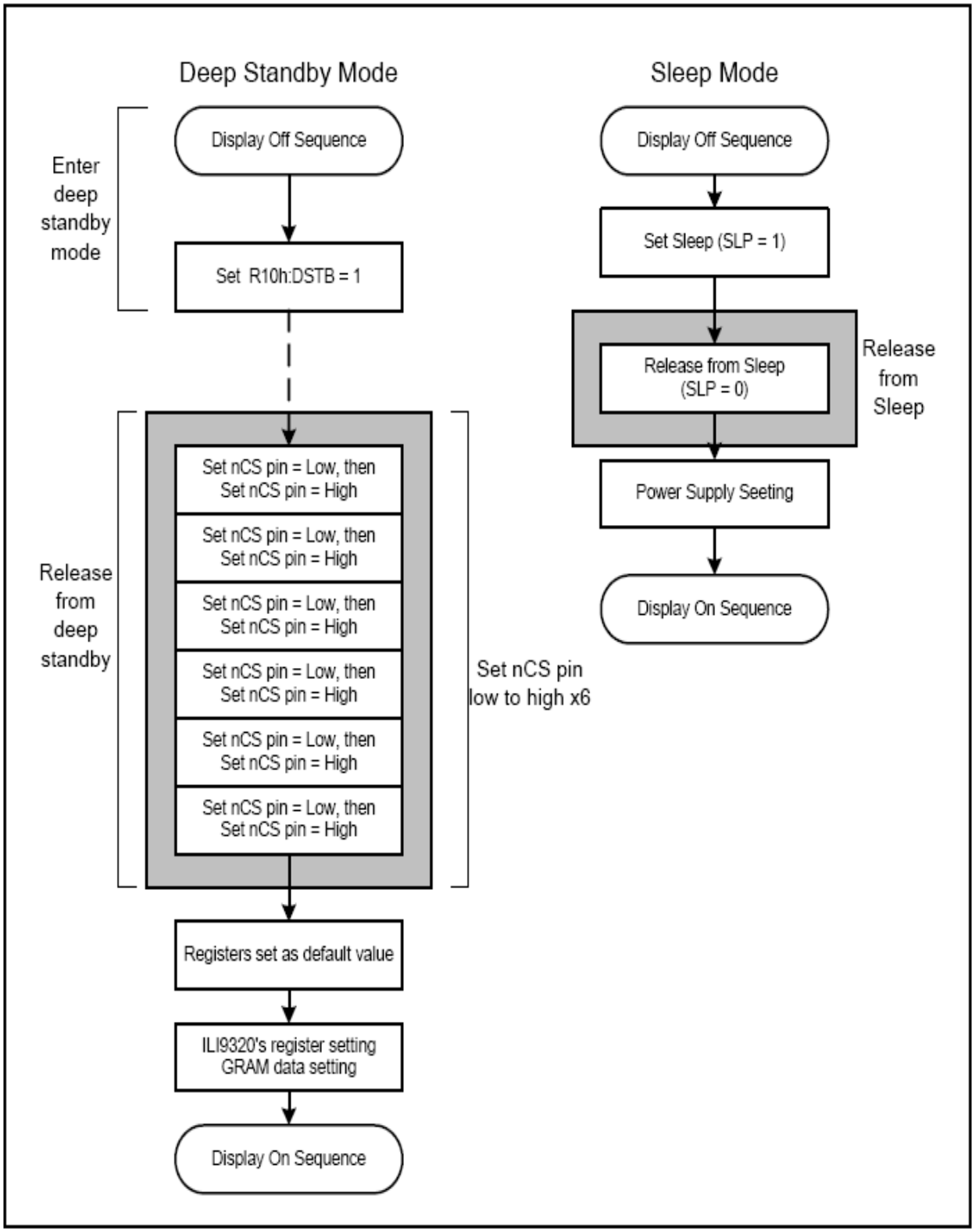
No.	Registers	R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
38h	Gamma Control 7	W	1	0	0	0	0	0	KN3[2]	KN3[1]	KN3[0]	0	0	0	0	0	KN2[2]	KN2[1]	KN2[0]
39h	Gamma Control 8	W	1	0	0	0	0	0	KN5[2]	KN5[1]	KN5[0]	0	0	0	0	0	KN4[2]	KN4[1]	KN4[0]
3Ch	Gamma Control 9	W	1	0	0	0	0	0	RN1[2]	RN1[1]	RN1[0]	0	0	0	0	0	RN0[2]	RN0[1]	RN0[0]
3Dh	Gamma Control 10	W	1	0	0	0	VRN 1[4]	VRN 1[3]	VRN 1[2]	VRN 1[1]	VRN 1[0]	0	0	0	VRN 0[4]	VRN 0[3]	VRN 0[2]	VRN 0[1]	VRN 0[0]
50h	Horizontal Address Start Position	W	1	0	0	0	0	0	0	0	0	HSA7	HSA6	HSA5	HSA4	HSA3	HSA2	HSA1	HSA0
51h	Horizontal Address End Position	W	1	0	0	0	0	0	0	0	0	HEA7	HEA6	HEA5	HEA4	HEA3	HEA2	HEA1	HEA0
52h	Vertical Address Start Position	W	1	0	0	0	0	0	0	0	VSA8	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0
53h	Vertical Address End Position	W	1	0	0	0	0	0	0	0	VEA8	VEA7	VEA6	VEA5	VEA4	VEA3	VEA2	VEA1	VEA0
60h	Driver Output Control 2	W	1	GS	0	NL5	NL4	NL3	NL2	NL1	NL0	0	0	SCN 5	SCN 4	SCN 3	SCN 2	SCN 1	SCN 0
61h	Base Image Display Control	W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	NDL	VLE	REV
6Ah	Vertical Scroll Control	W	1	0	0	0	0	0	0	0	VL8	VL7	VL6	VL5	VL4	VL3	VL2	VL1	VL0
80h	Partial Image 1 Display Position	W	1	0	0	0	0	0	0	0	PTD P08	PTD P07	PTD P06	PTD P05	PTD P04	PTD P03	PTD P02	PTD P01	PTD P00
81h	Partial Image 1 Area (Start Line)	W	1	0	0	0	0	0	0	0	PTSA 08	PTSA 07	PTSA 06	PTSA 05	PTSA 04	PTSA 03	PTSA 02	PTSA 01	PTSA 00
82h	Partial Image 1 Area (End Line)	W	1	0	0	0	0	0	0	0	PTEA 08	PTEA 07	PTEA 06	PTEA 05	PTEA 04	PTEA 03	PTEA 02	PTEA 01	PTEA 00
83h	Partial Image 2 Display Position	W	1	0	0	0	0	0	0	0	PTD P18	PTD P17	PTD P16	PTD P15	PTD P14	PTD P13	PTD P12	PTD P11	PTD P10
84h	Partial Image 2 Area (Start Line)	W	1	0	0	0	0	0	0	0	PTSA 18	PTSA 17	PTSA 16	PTSA 15	PTSA 14	PTSA 13	PTSA 12	PTSA 11	PTSA 10
85h	Partial Image 2 Area (End Line)	W	1	0	0	0	0	0	0	0	PTEA 18	PTEA 17	PTEA 16	PTEA 15	PTEA 14	PTEA 13	PTEA 12	PTEA 11	PTEA 10
90h	Panel Interface Control 1	W	1	0	0	0	0	0	0	DIVI1	DIVI0 0	0	0	0	0	RTNI 3	RTNI 2	RTNI 1	RTNI 0
92h	Panel Interface Control 2	W	1	0	0	0	0	0	NOW I2	NOW I1	NOW I0	0	0	0	0	0	0	0	0
93h	Panel Interface Control 3	W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	MCPI 2	MCPI 1	MCPI 0
95h	Panel Interface Control 4	W	1	0	0	0	0	0	0	DIVE 1	DIVE 0	0	0	RTN E5	RTN E4	RTN E3	RTN E2	RTN E1	RTN E0
97h	Panel Interface Control 5	W	1	0	0	0	0	NOW E3	NOW E2	NOW E1	NOW E0	0	0	0	0	0	0	0	0
98h	Panel Interface Control 6	W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	MCP E2	MCP E1	

10 Application

10.1 Display ON / OFF

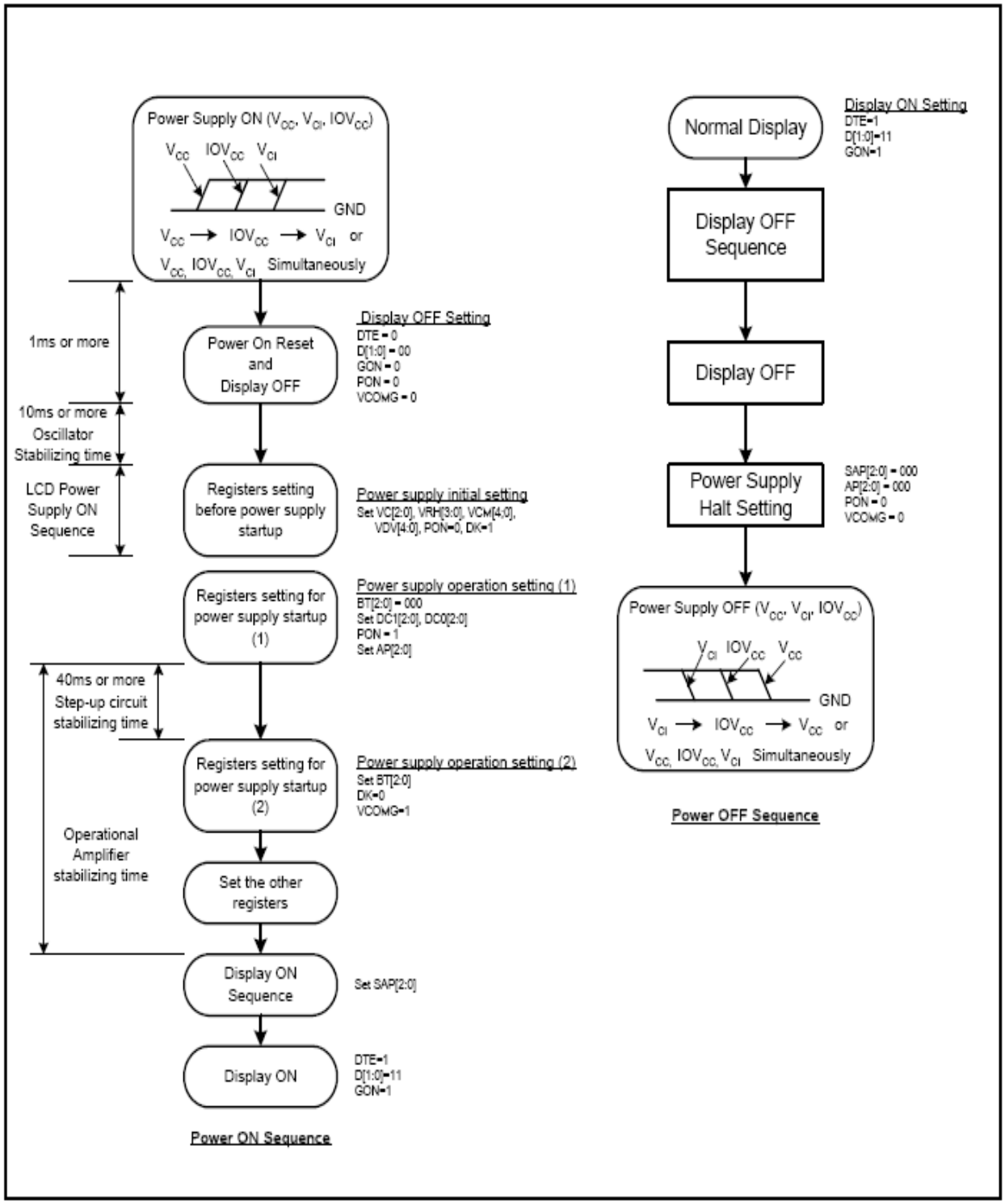


10.2 Deep Standby and Sleep Mode



10.3 Power Supply Configuration

When supplying and cutting off power, follow the sequence below. The setting time for oscillators, step-up circuits and operational amplifiers depends on external resistance and capacitance.



11 Timing Characteristics

11.1 Clock Characteristics

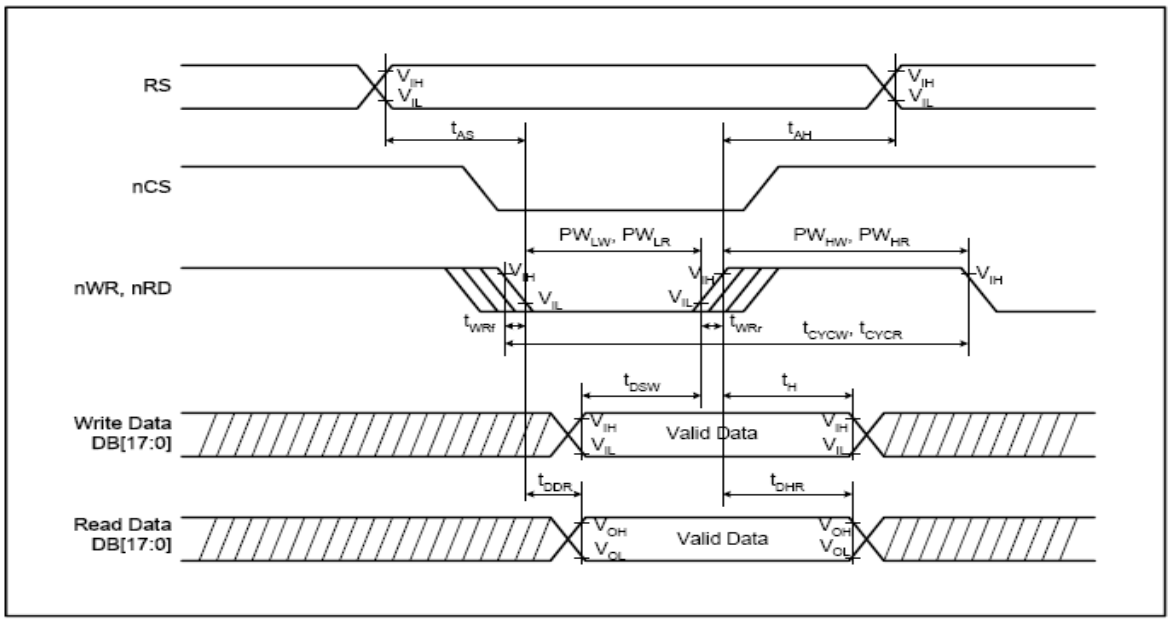
VCC = 2.40 ~ 3.30V, IOVCC = 1.65 ~ 3.30V

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
External Clock Frequency	fcp	VCC = 2.4 ~ 3.3V	450	550	650	KHz
External Clock Duty	f_{Duty}	VCC = 2.4 ~ 3.3V	45	50	55	
External Clock Rising Time	Trcp	VCC = 2.4 ~ 3.3V	-	-	0.2	µs
External Clock Falling Time	Tfcp	VCC = 2.4 ~ 3.3V	-	-	0.2	µs
RC oscillation clock	f_{osc}	Rf = 100KΩ, VCC = 2.8V	450	550	650	KHz

11.2 AC Characteristics (i80 – system Interface Timing Characteristics)

Normal Write Mode (IOVCC = 1.65~3.3V, VCC=2.4~3.3V)

Item		Symbol	Unit	Min.	Typ.	Max.	Test Condition
Bus cycle time	Write	t_{CYCW}	ns	100	-	-	-
	Read	t_{CYCR}	ns	300	-	-	-
Write low-level pulse width		PW_{LW}	ns	50	-	500	-
Write high-level pulse width		PW_{HW}	ns	50	-	-	-
Read low-level pulse width		PW_{LR}	ns	150	-	-	-
Read high-level pulse width		PW_{HR}	ns	150	-	-	
Write / Read rise / fall time		t_{WRr}/t_{WRf}	ns	-	-	25	
Setup time	Write (RS to nCS, E/nWR)	t_{AS}	ns	10	-	-	
	Read (RS to nCS, RW/nRD)			5	-	-	
Address hold time		t_{AH}	ns	5	-	-	
Write data set up time		t_{DSW}	ns	10	-	-	
Write data hold time		t_H	ns	15	-	-	
Read data delay time		t_{DDR}	ns	-	-	100	
Read data hold time		t_{DHR}	ns	5	-	-	



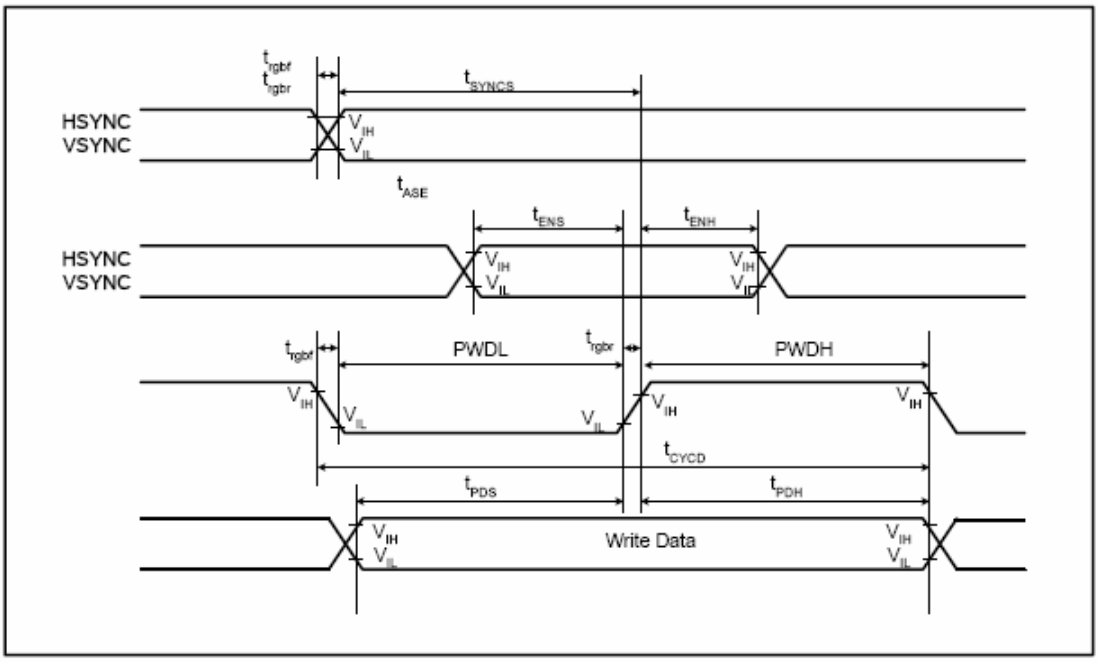
11.3 AC Characteristics (RGB Interface Timing Characteristics)

18/16-bit Bus RGB Interface Mode (IOVCC = 1.65 ~ 3.3V, VCC=2.4~3.3V)

Item	Symbol	Unit	Min.	Typ.	Max.	Test Condition
VSYNC/HSYNC setup time	t_{SYNCS}	ns	0	-	-	-
ENABLE setup time	t_{ENS}	ns	10	-	-	-
ENABLE hold time	t_{ENH}	ns	10	-	-	-
PD Data setup time	t_{PDS}	ns	10	-	-	-
PD Data hold time	t_{PDH}	ns	40	-	-	-
DOTCLK high-level pulse width	PWDH	ns	40	-	-	-
DOTCLK low-level pulse width	PWDL	ns	40	-	-	-
DOTCLK cycle time	t_{CYCD}	ns	100	-	-	-
DOTCLK, VSYNC, HSYNC, rise/fall time	t_{rghr}, t_{rghf}	ns	-	-	25	-

6-bit Bus RGB Interface Mode (IOVCC = 1.65 ~ 3.3V, VCC=2.4~3.3V)

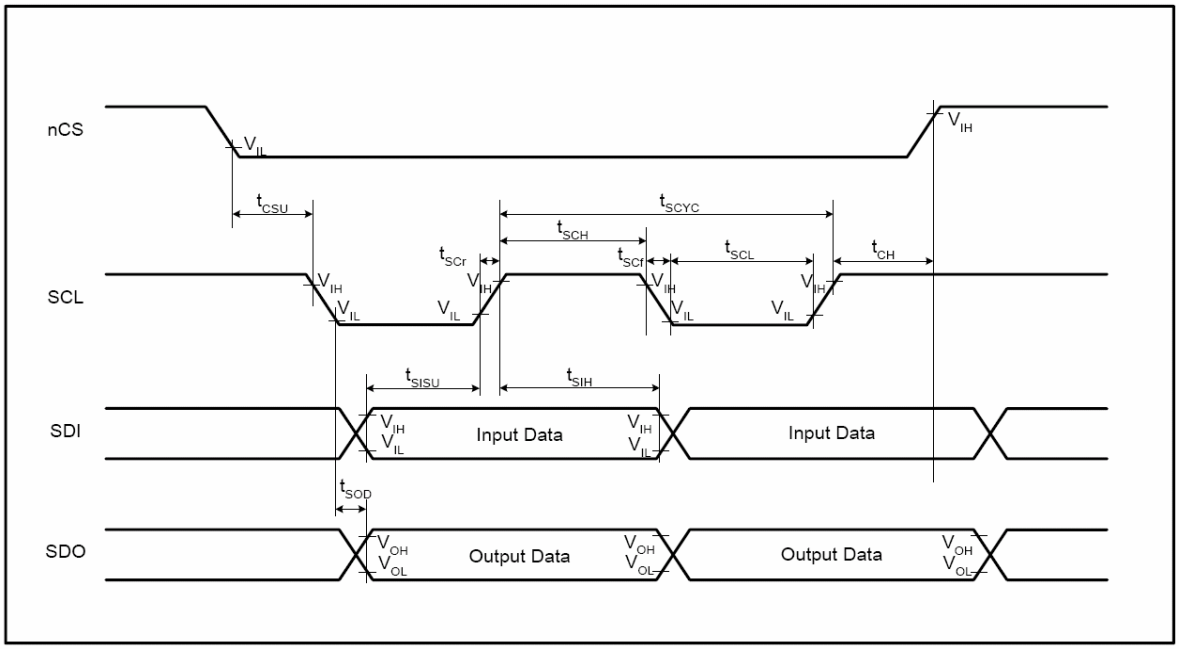
Item	Symbol	Unit	Min.	Typ.	Max.	Test Condition
VSYNC/HSYNC setup time	t_{SYNCS}	ns	0	-	-	-
ENABLE setup time	t_{ENS}	ns	10	-	-	-
ENABLE hold time	t_{ENH}	ns	10	-	-	-
PD Data setup time	t_{PDS}	ns	10	-	-	-
PD Data hold time	t_{PDH}	ns	30	-	-	-
DOTCLK high-level pulse width	PWDH	ns	30	-	-	-
DOTCLK low-level pulse width	PWDL	ns	30	-	-	-
DOTCLK cycle time	t_{CYCD}	ns	80	-	-	-
DOTCLK, VSYNC, HSYNC, rise/fall time	t_{rghr}, t_{rghf}	ns	-	-	25	-



11.4 AC Characteristics (SPI Interface Timing Characteristics)

(IOVCC= 1.653.3V and VCC=2.4~3.3V)

Item		Symbol	Unit	Min.	Typ.	Max.	Test Condition
Serial clock cycle time	Write (received)	t_{SCYC}	ns	100	-	-	
	Read (transmitted)	t_{SCYC}	ns	200	-	-	
Serial clock high – level pulse width	Write (received)	t_{SCH}	ns	40	-	-	
	Read (transmitted)	t_{SCH}	ns	100	-	-	
Serial clock low – level pulse width	Write (received)	t_{SCL}	ns	40	-	-	
	Read (transmitted)	t_{SCL}	ns	100	-	-	
Serial clock rise / fall time		t_{SCr}, t_{SCf}	ns	-	-	5	
Chip select set up time		t_{CSU}	ns	10	-	-	
Chip select hold time		t_{CH}	ns	50	-	-	
Serial input data set up time		t_{SISU}	ns	20	-	-	
Serial input data hold time		t_{SIH}	ns	20	-	-	
Serial output data set up time		t_{SOD}	ns	-	-	100	
Serial output data hold time		t_{SOH}	ns	5	-	-	



12 QUALITY AND RELIABILITY

12.1 TEST CONDITIONS

Tests should be conducted under the following conditions:

Ambient temperature: 25 ± 5°C

Humidity : 60 ± 25% RH.

12.2 SAMPLING PLAN

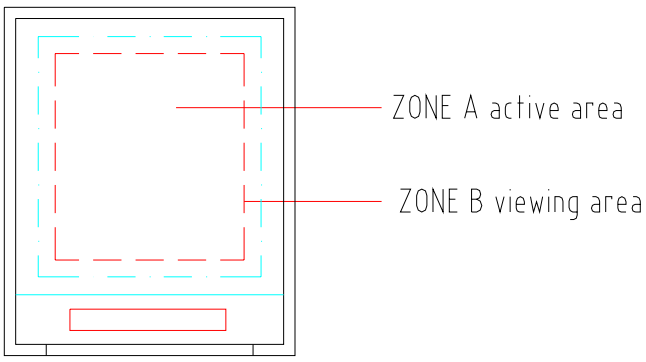
Sampling method shall be in accordance with MIL-STD-105E , level II, normal single sampling plan .

12.3 ACCEPTABLE QUALITY LEVEL

A major defect is defined as one that could cause failure to or materially reduce the usability of the unit for its intended purpose. A minor defect is one that does not materially reduce the usability of the unit for its intended purpose or is an infringement from established standards and has no significant bearing on its effective use or operation.

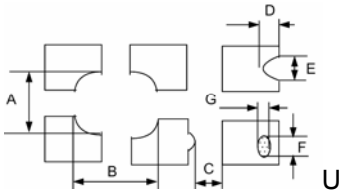
12.4 APPEARANCE

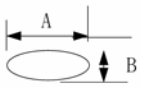
An appearance test should be conducted by human sight at approximately 30 cm distance from the LCD module under flourescent light. The inspection area of LCD panel shall be within the range of following limits.



12.5 INSPECTION QUALITY CRITERIA

<table>
<tr><th>No.</th><th>Item</th><th>Criterion for defects</th><th>Defect type</th></tr>
<tr><td>1</td><td>Non display</td><td>No non display is allowed</td><td>Major</td></tr>
<tr><td>2</td><td>Irregular operation</td><td>No irregular operation is allowed</td><td>Major</td></tr>
<tr><td>3</td><td>Short</td><td>No short are allowed</td><td>Major</td></tr>
<tr><td>4</td><td>Open</td><td>Any segments or common patterns that don’t activate are rejectable.</td><td>Major</td></tr>
<tr><td>5</td><td>Black/White spot (I)</td><td><table><tr><th>Size D (mm)</th><th>Acceptable number</th></tr><tr><td>D ≤ 0.15</td><td>Ignore</td></tr><tr><td>0.15 < D ≤ 0.20</td><td>3</td></tr><tr><td>0.20 < D ≤ 0.30</td><td>2</td></tr><tr><td>0.30 < D</td><td>0</td></tr></table></td><td>Minor</td></tr>
<tr><td>6</td><td>Black/White line (I)</td><td><table><tr><th>Length(mm)</th><th>Width (mm)</th><th>Acceptable number</th></tr><tr><td>10 < L</td><td>0.03 < W ≤ 0.04</td><td>5</td></tr><tr><td>5.0 < L ≤10</td><td>0.04 < W ≤ 0.06</td><td>3</td></tr><tr><td>1.0 < L ≤ 5.0</td><td>0.06 < W ≤ 0.07</td><td>2</td></tr><tr><td>L ≤ 1.0</td><td>0.07 < W ≤ 0.09</td><td>1</td></tr></table></td><td>Minor</td></tr>
<tr><td>7</td><td>Black/White sport (II)</td><td><table><tr><th>Size D (mm)</th><th>Acceptable number</th></tr><tr><td>D ≤ 0.30</td><td>Ignore</td></tr><tr><td>0.30 < D ≤ 0.50</td><td>5</td></tr><tr><td>0.50 < D ≤ 1.20</td><td>3</td></tr><tr><td>1.20 < D</td><td>0</td></tr></table></td><td>Minor</td></tr>
<tr><td>8</td><td>Black/White line (II)</td><td><table><tr><th>Length (mm)</th><th>Width (mm)</th><th>Acceptable number</th></tr><tr><td>20 < L</td><td>0.05 < W ≤ 0.07</td><td>5</td></tr><tr><td>10 < L ≤ 20</td><td>0.07 < W ≤ 0.09</td><td>3</td></tr><tr><td>5.0 < L ≤ 10</td><td>0.09 < W ≤ 0.10</td><td>2</td></tr><tr><td>L ≤ 5.0</td><td>0.10 < W ≤ 0.15</td><td>1</td></tr></table></td><td>Minor</td></tr>
<tr><td>9</td><td>Back Light</td><td>1. No Lighting is rejectable
2. Flickering and abnormal lighting are rejectable</td><td>Major</td></tr>
</table>

<table>
<tr><td>10</td><td>Display pattern</td><td> 

Unit:mm
<table>
<tr><td>$\frac{A+B}{2} \le 0.30$</td><td>0 < C</td><td>$\frac{D+E}{2} \le 0.25$</td><td>$\frac{F+G}{2} \le 0.25$</td></tr>
</table>
Note: 1. Acceptable up to 3 damages
2. NG if there're to two or more pinholes per dot</td><td>Minor</td></tr>
<tr><td>11</td><td>Blemish & Foreign matters
Size:
$D = \frac{A+B}{2}$</td><td>
<table>
<tr><th>Size D (mm)</th><th>Acceptable number</th></tr>
<tr><td>D ≤ 0.15</td><td>Ignore</td></tr>
<tr><td>0.15 < D ≤ 0.20</td><td>3</td></tr>
<tr><td>0.20 < D ≤ 0.30</td><td>2</td></tr>
<tr><td>0.30 < D</td><td>0</td></tr>
</table>
</td><td>Minor</td></tr>
<tr><td>12</td><td>Scratch on Polarizer
 
</td><td>
<table>
<tr><th>Width (mm)</th><th>Length (mm)</th><th>Acceptable number</th></tr>
<tr><td>W≤0.03</td><td>Ignore</td><td>Ignore</td></tr>
<tr><td rowspan="2">0.03<W≤0.05</td><td>L ≤ 2.0</td><td>Ignore</td></tr>
<tr><td>L > 2.0</td><td>1</td></tr>
<tr><td rowspan="2">0.05<W≤0.08</td><td>L > 1.0</td><td>1</td></tr>
<tr><td>L ≤ 1.0</td><td>Ignore</td></tr>
<tr><td>0.08<W</td><td>Note (1)</td><td>Note(1)</td></tr>
</table>
Note(1) Regard as a blemish</td><td>Minor</td></tr>
<tr><td>13</td><td>Bubble in polarizer</td><td>
<table>
<tr><th>Size D (mm)</th><th>Acceptable number</th></tr>
<tr><td>D ≤ 0.20</td><td>Ignore</td></tr>
<tr><td>0.20 < D ≤ 0.50</td><td>3</td></tr>
<tr><td>0.50 < D ≤ 0.80</td><td>2</td></tr>
<tr><td>0.80 < D</td><td>0</td></tr>
</table>
</td><td>Minor</td></tr>
<tr><td>14</td><td>Stains on LCD panel surface</td><td>Stains that cannot be removed even when wiped lightly with a soft cloth or similar cleaning too are rejectable.</td><td>Minor</td></tr>
<tr><td>15</td><td>Rust in Bezel</td><td>Rust which is visible in the bezel is rejectable.</td><td>Minor</td></tr>
<tr><td>16</td><td>Defect of land surface contact (poor soldering)</td><td>Evident crevices which is visible are rejectable.</td><td>Minor</td></tr>
<tr><td>17</td><td>Parts mounting</td><td>1. Failure to mount parts
2. Parts not in the specifications are mounted
3. Polarity, for example, is reversed</td><td>Major
Major
Major</td></tr>
</table>

18	Parts alignment	1. LSI, IC lead width is more than 50% beyond pad outline. 2. Chip component is off center and more than 50% of the leads is off the pad outline.	Minor Minor
19	Conductive foreign matter (Solder ball, Solder chips)	1. 0.45< φ ,N≧1 2. 0.30< φ ≤0.45 ,N≧1 φ :Average diameter of solder ball (unit: mm) 3. 0.50<L ,N≧1 L: Average length of solder chip (unit: mm)	Major Minor Minor
20	Faulty PCB correction	1. Due to PCB copper foil pattern burnout, the pattern is connected, using a jumper wire for repair; 2 or more places are corrected per PCB. 2. Short circuited part is cut, and no resist coating has been performed.	Minor Minor

12.6 **RELIABILITY**

Test Item	Test Conditions	Note
High Temperature Operation	70±3°C , t=96 hrs	
Low Temperature Operation	-20±3°C , t=96 hrs	
High Temperature Storage	80±3°C , t=96 hrs	1,2
Low Temperature Storage	-30±3°C , t=96 hrs	1,2
Humidity Test	40°C , Humidity 90%, 96 hrs	1,2
Thermal Shock Test	-30°C ~ 25°C ~ 70°C 30 min. 5 min. 30 min. (1 cycle) Total 5 cycle	1,2
Vibration Test (Packing)	Sweep frequency：10~55~10 Hz/1min Amplitude : 0.75mm Test direction : X.Y.Z/3 axis Duration : 30min/each axis	2
Static Electricity	150pF 330 ohm ±8kV, 10times air discharge	

Note 1 : Condensation of water is not permitted on the module.

Note 2 : The module should be inspected after 1 hour storage in normal conditions

(15-35°C , 45-65%RH).

Definitions of life end point :

- Current drain should be smaller than the specific value.
- Function of the module should be maintained.
- Appearance and display quality should not have degraded noticeably.
- Contrast ratio should be greater than 50% of the initial value.

11 USE PRECAUTIONS

11.1 Handling precautions

1) The polarizing plate may break easily so be careful when handling it. Do not touch, press or rub it with a hard-material tool like tweezers.
2) Do not touch the polarizing plate surface with bare hands so as not to make it dirty. If the surface or other related part of the polarizing plate is dirty, soak a soft cotton cloth or chamois leather in benzine and wipe off with it. Do not use chemical liquids such as acetone, toluene and isopropyl alcohol. Failure to do so may bring chemical reaction phenomena and deteriorations.
3) Remove any spit or water immediately. If it is left for hours, the suffered part may deform or decolorize.
4) If the LCD element breaks and any LC stuff leaks, do not suck or lick it. Also if LC stuff is stuck on your skin or clothing, wash thoroughly with soap and water immediately.

11.2 Installing precautions

1) The PCB has many ICs that may be damaged easily by static electricity. To prevent breaking by static electricity from the human body and clothing, earth the human body properly using the high resistance and discharge static electricity during the operation. In this case, however, the resistance value should be approx. 1MΩ and the resistance should be placed near the human body rather than the ground surface. When the indoor space is dry, static electricity may occur easily so be careful. We recommend the indoor space should be kept with humidity of 60% or more. When a soldering iron or other similar tool is used for assembly, be sure to earth it.
2) When installing the module and ICs, do not bend or twist them. Failure to do so may crack LC element and cause circuit failure.
3) To protect LC element, especially polarizing plate, use a transparent protective plate (e.g., acrylic plate, glass etc) for the product case.
4) Do not use an adhesive like a both-side adhesive tape to make LCD surface (polarizing plate) and product case stick together. Failure to do so may cause the polarizing plate to peel off.

11.3 Storage precautions

1) Avoid a high temperature and humidity area. Keep the temperature between 0°C and 35°C and also the humidity under 60%.
2) Choose the dark spaces where the product is not exposed to direct sunlight or fluorescent light.
3) Store the products as they are put in the boxes provided from us or in the same conditions as we recommend.

11.4 Operating precautions

1) Do not boost the applied drive voltage abnormally. Failure to do so may break ICs. When applying power voltage, check the electrical features beforehand and be careful. Always turn off the power to the LC module controller before removing or inserting the LC module input connector. If the input connector is removed or inserted while the power is turned on, the LC module internal circuit may break.
2) The display response may be late if the operating temperature is under the normal standard, and the display may be out of order if it is above the normal standard. But this is not a failure; this will be restored if it is within the normal standard.
3) The LCD contrast varies depending on the visual angle, ambient temperature, power voltage etc. Obtain the optimum contrast by adjusting the LC dive voltage.
4) When carrying out the test, do not take the module out of the low-temperature space suddenly. Failure to do so will cause the module condensing, leading to malfunctions.
5) Make certain that each signal noise level is within the standard (L level: 0.2Vdd or less and H level: 0.8Vdd or more) even if the module has functioned properly. If it is beyond the standard, the module may often malfunction. In addition, always connect the module when making noise level measurements.
6) The CMOS ICs are incorporated in the module and the pull-up and pull-down function is not adopted for the input so avoid putting the input signal open while the power is ON.
7) The characteristic of the semiconductor element changes when it is exposed to

light emissions, therefore ICs on the LCD may malfunction if they receive light emissions. To prevent these malfunctions, design and assemble ICs so that they are shielded from light emissions.

8) Crosstalk occurs because of characteristics of the LCD. In general, crosstalk occurs when the regularized display is maintained. Also, crosstalk is affected by the LC drive voltage. Design the contents of the display, considering crosstalk.

11.5 Other

1) Do not disassemble or take the LC module into pieces. The LC modules once disassembled or taken into pieces are not the guarantee articles.
2) The residual image may exist if the same display pattern is shown for hours. This residual image, however, disappears when another display pattern is shown or the drive is interrupted and left for a while. But this is not a problem on reliability.
3) AMIPRE will provide one year warrantee for all products and three months warrantee for all repairing products.

12. MECHANIC DRAWING