ASP-DAC
Asia and South Pacific
Design Automation Conference 2000

January 25 - 28, 2000
Pacifico Yokohama,
Yokohama, Japan

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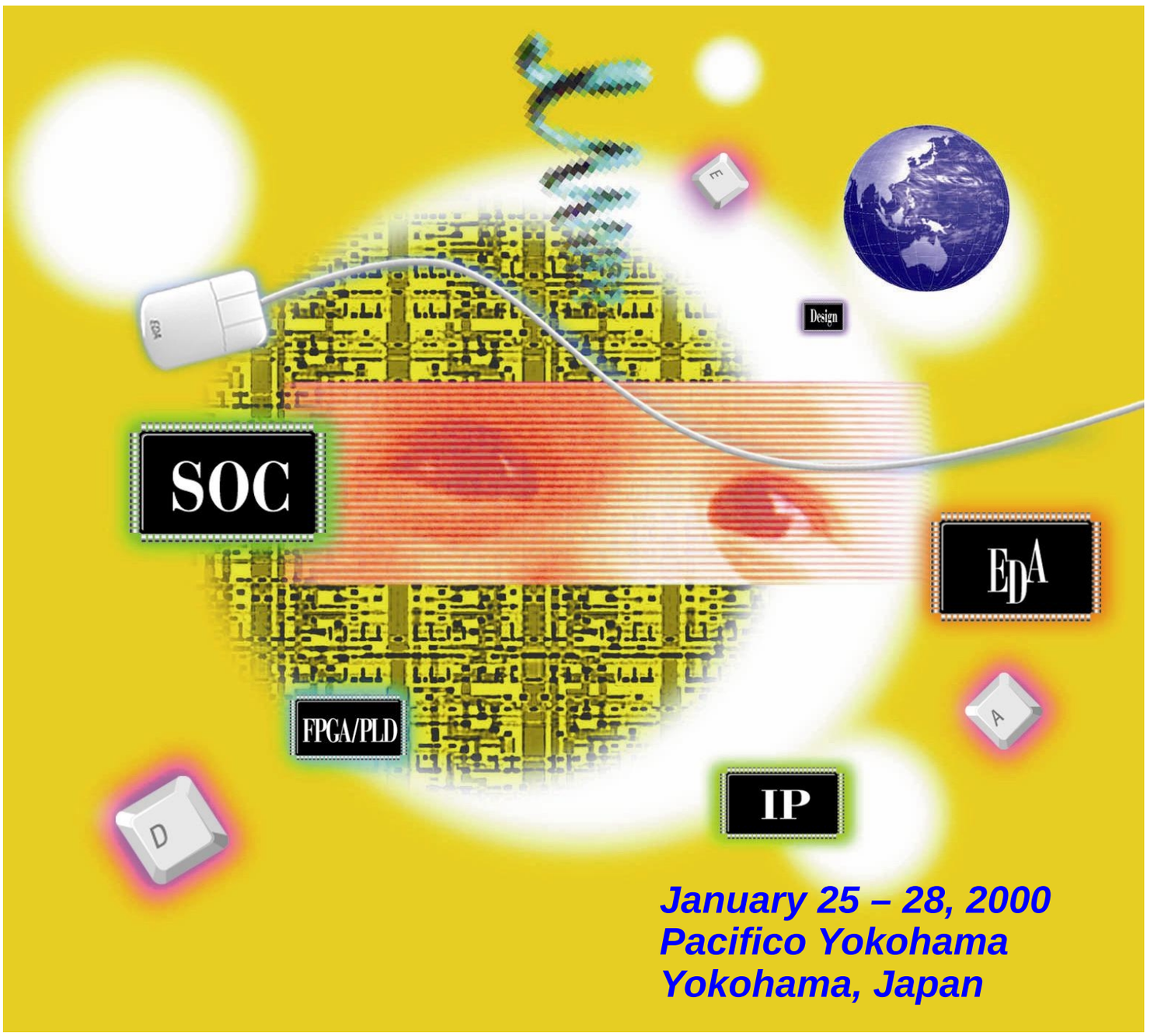
ASP-DAC 2000

Asia and South Pacific Design Automation Conference 2000

with

EDA TechnoFair 2000



January 25 – 28, 2000
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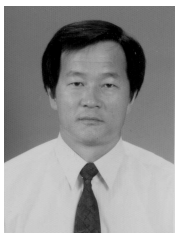

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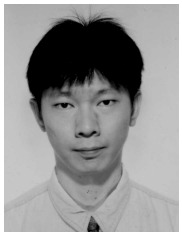

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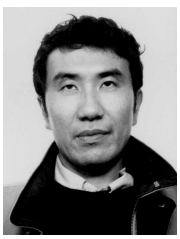

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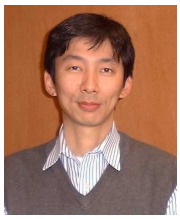

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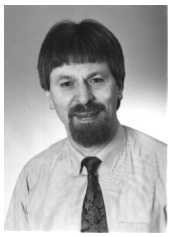

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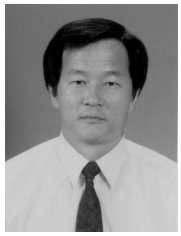

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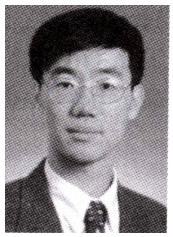

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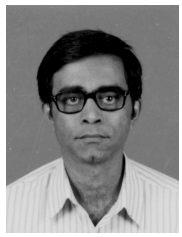

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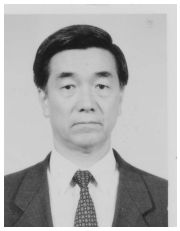

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ASP-DAC 2000 General Chair's Message

Welcome to ASP-DAC 2000

On behalf of the Organizing Committee, I would like to welcome you to the Asia and South Pacific Design Automation Conference 2000 (ASP-DAC 2000). This year's ASP-DAC will be held again in the Pacifico Yokohama, Japan, jointly with EDA TechnoFair 2000, premier Japanese EDA exhibition. The goal of the ASP-DAC is to provide an international forum for researchers and engineers in academia and industry, in the area of electronic system/VLSI design, and DA/CAD. ASP-DAC is a sister conference of DAC in the USA and DATE in Europe.

Three keynote speakers will talk about future directions of VLSI design technologies from different points of view. Dr. Shojiro Asai, Corporate Officer & President of Hitachi R & D Group will talk about the impact of communications convergence on VLSI. Prof. C. L. Liu, President of National Tsing Hua University, Taiwan, will talk about education, design and fabrication technologies. And, finally, Mr. Willam Herrick, Director of Compaq Alpha Development Group, USA, will talk about challenges in multi-GHz processor designs.

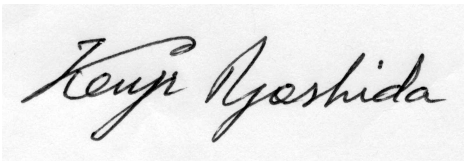
An excellent technical program has been organized by the committee co-chaired by Prof. H. Kunieda and Prof. C.M. Kyung, and with voluntary work of numerous experts from worldwide. This year we have an increased number of paper submissions in a wide spectrum of technical areas, and also from variety of geographical regions. 90 papers selected have been organized into five trucks; LSI Design, System DA, Logic and Test, Physical DA, and Circuit and Device CAD. Each of them also includes special sessions, panels, embedded tutorials or invited talks by distinguished speakers. Among panels, a panel by EDA vendor executive is planned just after the opening session on Wednesday. They will talk on their strategies to solve the next generation design challenges.

A unique feature of ASP-DAC is the University LSI Design Contest, which focuses a real chip design in academia. 18 designs have been selected for poster presentation, from which 3 or 4 award winners will be selected at the conference.

On Tuesday, full day tutorials are scheduled to give complete introductions of five state-of-the-art design/CAD topics; (1) Embedded Microprocessor Design, (2) Power Reduction Techniques, (3) Test Techniques, (4) Front-End Optimization and Verification, and (5) Ultra Deep Submicron Design and Analysis.

Our community is now facing tremendous challenges caused by accelerated scaling down and ever increasing complexity of System-on-a-Chip. I believe the ASP-DAC 2000 will be a precious opportunity for you to find many hints for your solution by meeting, talking and exchanging ideas with many leading edge researchers, or friends of yours, in the same, or different, technical areas.

I hope you will have a valuable and enjoyable experience at Yokohama, Japan, in next January.



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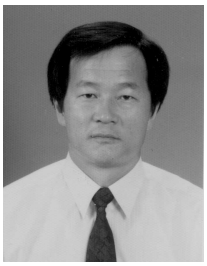
Hiroaki Kunieda



Chong-Min Kyung

On behalf of the Technical Program Committee of ASP-DAC 2000, I would like to welcome all of you to ASP-DAC in the memorial year of 2000. Following the past successful conferences in Tokyo (1995, 1997, 1998) and in Hong Kong (1999), the Committee has invited contributions for 2000 conference in the area of Design Automation of various design stages and LSI design methodologies.

This year, our committee specifically introduced LSI Development into the area of interest for the ASP-DAC 2000 Technical Program. The number of gates on a chip is rapidly approaching 10 million gates. System-On-A-Chip is now in our hands. As the roles of CAD tools in these highly complex system designs become more and more important, CAD tool designers have to pay particularly close attention to the latest system design examples and methodologies. In this context, we believe that our ASP-DAC needs to increase presentations of LSI developments, to provide a place where system designers and CAD designers can exchange ideas and establish an intensive and mutual understandings of the important problems we are currently facing.

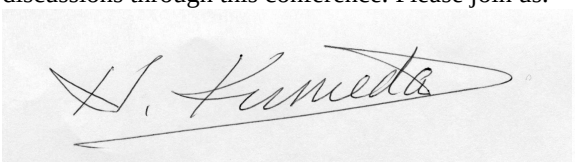
Also, reflecting the current trend of System-On-A-Chip, there is a great increase in paper submissions related to system-level design automation which includes software/hardware codesign, a variety of system-level optimization issues, system description languages, etc. Physical layout CAD continues to provide challenging new topics and maintains to be one of the major contributors to this conference. Especially, continuous efforts on conquering various layout problems in deep submicron process have been undertaken by many researchers.

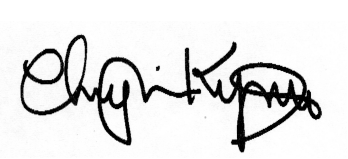
For this conference, 144 technical papers were submitted from 14 countries. The technical program committee have reviewed all the submitted papers and accepted 80 regular papers and 10 short papers for presentation at the conference. We have organized the session tracks based on the field categories, each of which runs in the same room. They are 1) LSI Design Track, 2) System DA track, 3) Logic DA track including testing, 4) Physical DA track, 5) Device CAD track including Analog DA. They are designed so that the participants can easily follow the session tracks related to their own fields.

There are also 8 special sessions and panel sessions included in our technical program, inviting a number of distinguished researchers from around the world. These sessions address a wide variety of important issues such as CAD for embedded systems, System-In-Packaging (SIP), timing closure between logic and physical designs, issues on industry-academia cooperation, and system level design languages. Also, there are a number of embedded tutorials and invited talks within the regular sessions. We would like to express our appreciations for the efforts of organizers, chairs, panelists and invited speakers, which add special values to our program.

Best paper awards are presented to the authors whose papers are of exceptionally high quality among all the presented papers. 7 best paper award candidates were first nominated by the Technical Program Committee, where they were further subjected to intensive evaluation by the Committee.

As co-chair of ASP-DAC 2000 Technical Program Committee, I am really grateful for all of the members of our committee, organizers of special sessions and panel sessions, chairs and speakers of special sessions and regular sessions for their continuing efforts. Among them, I really appreciate TPC secretaries, Dr. Kazuhito Ito, Dr. Kei Suzuki and Dr. Tsuyoshi Isshiki for their dedications. Without them, ASP-DAC 2000 could not be held. At last, I would like to emphasis that the real success depends on how much all of you, the participants of ASP-DAC 2000, show your attention and join the conference activity. In other words, I hope you can enjoy 3 days hot discussions through this conference. Please join us.





Hiroaki Kunieda and Chong-Min Kyung
Co-Chairs, ASP-DAC 2000 Program Committee

ASP-DAC 2000 Best Paper Award Candidates

E7.1 "A 12b 50 MHz 3.3V CMOS Acquisition Time Minimized A/D Converter", Young-Deuk Jeon, Byeong-Lyeol Jeon, Hyoung-Kyu Choi, Seung-Hoon Lee (Sogang Univ., Korea) [LSI Development]

A6.1 "Optimization of VDD and VTH for Low-Power and High Speed Applications",
Koichi Nose, Takayasu Sakurai (Univ. of Tokyo, Japan) [Designs]

B2.1 "A New Method for Constructing IP Level Power Model Based on Power Sensitivity",
Heng-Liang Huang, Jiing-Yuan Lin, Wen-Zen Shen, Jing-Yang Jou (Nat'l Chaio-Tung Univ., Taiwan) [Design Methods & Environments]

C5.1 "Performance-Optimal Clustering with Retiming for Sequential Circuits",
Tzu-Chieh Tien, Youn-Long Lin (Tsing Hua Univ., Taiwan) [Logic Synthesis]

D3.1 "Delay-Optimal Wiring Plan for the Microprocessor of High Performance Computing Machine",
Jun Kikuchi, Tetsuo Sasaki, Tohru Hashimoto, Kazuhisa Miyamoto (Hitachi, Japan) [Physical DA]

D6.1 "A Cell Synthesis Method for Salicide Process",
Kazuhisa Okada, Takayuki Yamanouchi, Taksahi Kambe (Sharp, Japan) [Physical DA]

E4.2 "Circuit Performance Oriented Device Optimization using BSIM3 Pre-Silicon Model Parameters",
Mikako Miyama, Shiro Kamohara, (Hitachi, Japan) [T-CAD]

University LSI Design Contest Committee

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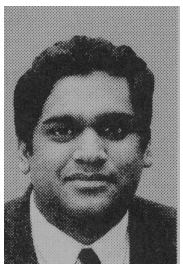
Thad Gabara
Bell Labs

Brock Barton
Texas Instruments

University LSI Design Contest Co-Chairs' Message

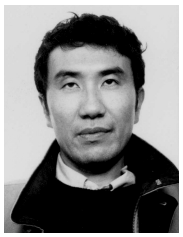
Ryota Kasai



Annatha Chandrakasan

The University LSI Design Contest was born a unique program of ASP-DAC Conference. The purpose of the Contest is to encourage education and research on LSI design and its implementation into chips at universities, and other educational organizations, by providing the opportunities to present and discuss their latest designs at the conference.

Application areas and types of circuits include (1) Analog and Mixed-Signal Circuits, (2) Digital Signal Processing, (3) Microprocessors, and (4) Custom Application Specific Circuits. Methods, or technology used for implementation include (a) Full Custom and Cell-Based LSIs, (b) Gate Arrays, and (c) Field Programmable Devices, including FPGA/PLDs. Actually implemented on real chips is required of all the designs.



Hideharu Anamo

This year, eighteen selected designs from four countries will be disclosed in Session A1, with a short aural presentations followed by Q & A, using posters. Three out of the eighteen are with analog and mixed signal, six are with microprocessors, and nine are with custom application specific circuits. Demonstrations on the achievements will also be made for some designs. Opportunities for demonstrations at EDA TechnoFair2000 will be provided for the above designs.

Submitted designs were reviewed by the members of the University Design Contest Committee, based on the following criteria: Reliability of design and implementation, Quality of implementation, Performance of the design, Novelty, and Additional factors. In the selection process, emphasis was placed more on reliability, quality, and performance, rather than on novelty of designs. AS a result, the eighteen designs were selected. And also, a certain number of awards will be given to outstanding designs, selected from those presented at the conference.

It is our great pleasure if the design contest will contribute to the promotion of research and education in LSI design field at academic organizations. It is also our hope that many people not only in academia but in industry will attend the contest and enjoy stimulating discussion.

Ryota Kasai Anantha Padmanabha

Ryota Kasai and Anantha Chandrakasan
Co-Chairs, University LSI Design Contest Committee

天野 英晴

Hideharu Amano
Vice Chair, University LSI Design Contest Committee

ASP-DAC 2000 University LSI Design Contest Summary

Submission

Nineteen designs were submitted from four countries, Japan, Korea, China and Taiwan. Design area and methodologies are as follows. This year, most of design used full custom or cell based design methodology.

Country	Number of Submission	Application Area			Design Methodology		
		A	M	C	F/C	G/A	F/P
Japan	9	4	4	1	9	0	0
China	5	0	1	4	4	0	1
Korea	3	0	1	2	3	0	0
Taiwan	2	0	0	2	2	0	0

Area
A: Analog or A/D Mixed, M: Microprocessor or DSP, C: Custom or Application Specific
Methodology
G/A: Gate Array, F/P: FPGA/PLD
F/C: Full Custom/ Cell Based, G/A: Gate Array, F/P: FPGA/PLD

Paper Selection

Submitted designs were subjected to the reviewing by committee members who were classified into three groups corresponding areas: Analog or A/D Mixed, Microprocessor or DSP, and Custom or Application Specific. Each committee member was requested to fill in the review sheet, including the following criteria, rank and comments. (1) Reliability of design and implementation, (2) Quality of Implementation, (3) Performance of the Design, (4) Novelty of Application, Algorithm, Architecture, and Circuit configuration, (5) Additional Points, such as new design methodology and testability. Unlike usual reviews of technical papers, our evaluation of submitted placed more importance on how the LSI circuits were designed and implemented than anything else. Design selection was carried out the committee meeting held on September 21. Discussion on the selection rejection of each design was carried out, based on the recommendation points and comments. As a result, 18 designs are selected and are presented in these proceedings. One design was rejected, since it is too specific to interest the conference. A candidate for the Outstanding Design Award, and two candidates for Special Feature Awards were selected.

ASP-DAC 2000 University LSI Design Contest Awards

Outstanding Design Award

A VLSI Implementation of the Blowfish Encryption/Decryption Algorithm
Michael C.-J.Lin and Youn-Long Lin
(Department of Computer Science, National Tsing Hua University)

Outstanding Design Award presented for the implementation of a high performance cryptographic processor utilizing novel critical path reduction techniques at the logic and architecture levels.

Special Feature Award (Microprocessors/DSP)

An Application Specific JAVA Processor with Reconfigurabilities
Shinji Kimura, Hiyoyuki Kida, Kazuyoshi Takagi, Tatsumori Abematsu and
Katsumasa Watanabe
(Graduate School of Information Science, Nara Institute of Science and Technology)

Special Feature Award presented for incorporating reconfigurability into an embedded Java processor to enable instruction set customizations and facilitate access to external computational resources.

Special Feature Award (Analog / A/D Mixed)

A Smart Imager for the Vision Processing Front-END
Noriaki Takeda, Mitsuru Homma, Makoto Nagata, Takashi Morie and Atsushi Iwata
(Advanced Scientific of Matter, Hiroshima University)

Special Feature Award presented for utilizing novel PWM-based signal processing techniques for front-end processing in a CMOS imager for intelligent vision applications.

Keynote Address I

“The Impact of Communications Convergence on Silicon Integrated Circuits”

Shojiro Asai, Ph.D.

Corporate Officer and President,
Research & Development Group, Hitachi,Ltd., Japan

Telephone, wireless, datacom, and broadcasting are quickly converging around the internet, creating an integrated environment for work, education, entertainment, and shopping. You will have access to any service whether you are at home or on the road. In order to ensure the quality of services it is necessary to provide ubiquitous support, high bandwidth, security, and ease of use. A new family of integrated circuits that brings about this brave new world and the design methodology it requires will be described.

Keynote Address II

“Research, Design, and Fabrication - Brain Power, Tool Power, and Electric Power”

Prof. C. L. Liu, Sc.D.

President,
National Tsing Hua University, Hsin-chu, Taiwan

Research and education, design tools, and fabrication technology are key and inter-related ingredients in to-day’s vast and rapidly growing micro-electronic economics. We shall examine some of the current issues and future challenges we are facing.

Keynote Address III

“Design Challenges in Multi-GHz Microprocessors”

William Herrick

Director, Alpha Microprocessor Development,
Compaq Computer Corporation, USA

Advances in semiconductor technology will soon enable multi-GHz microprocessors and present designers with opportunities and challenges. Transistors and interconnect will exhibit new behaviors which must be modeled. Logical and circuit complexity will explode making data management critical. Power distribution and clocking methods must be re-thought. A new generation of synthesizers must be developed and new electrical and timing verification tools must be created.

ASP-DAC 2000 EDA Vendor Executive Panel

Can We Rely on EDA Vendors for the Next Generation Design Technologies?

Organizer: **Kenji Yoshida –** *Toshiba Corp., Japan*

Moderator: **Ron Collett –** *Collett International, Inc., USA*

Panelsists: **Aart de Geus –** *Synopsys, Inc., USA*
Shane Robison – *Cadence Design Systems, Inc. USA*
Wally Rhinse – *Mentor Graphics Corp., USA*
Jinya Katsube – *Zuken Inc., Japan*
Penny Herscher – *Simplex, Inc., USA*
Guido Arnout – *CoWare, Inc., USA*

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Session B1
IP Reuse and Protection Methods

Co-Chairs : *Graham R. Hellestrand – VaST Systems Technology Corp., USA*
Minoru Yamamoto – Fujitsu Ltd., Japan

Session C1
Decision Diagrams and Verification Methods

Co-Chairs : *Yirng-An Chen – National Chiao Tung Univ., Taiwan*
Kiyoharu Hamaguchi – Osaka Univ., Japan

Session D1
Routing in Deep-Submicron

Co-Chairs : *Jason Cong – Univ. of California, Los Angeles, USA*
Takumi Okamoto – NEC Corp., Japan

Session A2 (Special Session)
CAD for Embedded Systems

Chair : *Miodrag Potkonjak – Univ. of California, Los Angeles, USA*

Session B2
System-Level Power Optimization & Estimation

Co-Chairs : *Akira Matsuzawa – Matsushita Electrical Industrial, Co. Ltd., Japan*
Masato Edahiro – NEC Corp., Japan

Session C2
Design Environment for FPGA

Co-Chairs : *Shinji Kimura – Nara Inst. of Science and Technology, Japan*
Kazutoshi Wakabayashi – NEC Corp., Japan

Session D2
Placement Consistent with Routing

Co-Chairs : *Yu-Liang Wu – Chinese University of Hong Kong, China*
Hiroshi Murata – Microark, Japan

Session E2 (Special Session)
System-In-Package (SIP)

Chair : *Wayne W.-M. Dai – Univ. of California, Santa Cruz, USA*

Session A3
Low Power Design : Implementation

Co-Chairs : *Shoji Kawahito – Toyohashi Univ. of Technology, Japan*
Jan M. Rabaey – Univ. of California, Berkeley, USA

Session B3
Embedded Software

Co-Chairs : *Peter Marwedel – Univ. of Dortmund, Germany*
Hiroaki Takada – Toyohashi University of Technology, Japan

Session C3
Implementation of Boolean Functions

Co-Chairs : *Yusuke Matsunaga – Fujitsu Laboratories, Ltd., Japan*
Hiroyuki Ochi – Hiroshima City Univ., Japan

Session D3
Physical Design Planning

Co-Chairs : *Wayne W.-M. Dai – Univ. of California, Santa Cruz, USA*
Shuji Tsukiyama – Chuo Univ., Japan

Session E3
Methodologies for Reliable Design

Co-Chairs : *Mitiko Miura-Mattausch – Hiroshima Univ., Japan*
Andrzej J. Strojwas – Carnegie Mellon Univ., USA

Session A4
Synthesis for System-On-A-Chip

Co-Chairs : *Rolf Ernst – Technical Univ. Braunschweig, Germany*
Ahmed A. Jerraya – TIMA Laboratory, France

Session B4
Reconfigurable Computation

Co-Chairs : *Toshiaki Miyazaki – NTT Network Innovation Laboratories, Japan*
Tetsuo Hironaka – Hiroshima City Univ., Japan

Session C4
Synthesis for Low Power

Co-Chairs : *Akira Nagoya – NTT Communication Science Laboratories, Japan*
Manish Pandey – Cadence Design Systems, Inc., USA

Session D4 (Panel Discussion)
Timing Closure : The Solution and Its Problems

Organizer: *Ralph H.J.M. Otten – Delft University of Technology, The Netherlands*
Moderator: *Ralph H.J.M. Otten – Delft University of Technology, The Netherlands*
Panelists: *Raul Camposano (Synopsys, Inc., USA), Oliver Coudert (Monterey Design Systems, Inc., USA), Patrick Groeneveld (Magma Design Automation, USA), Leon Stok (Thomas J. Watson Research Center, IBM, USA)* 359

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Co-Chairs : *Naoyuki Shigyo – Toshiba Corp., Japan*
C.-J. Richard Shi – Univ. of Washington, USA

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Co-Chairs : *Keshab K. Parhi – Univ. of Minnesota, USA*
Koji Kotani – Tohoku Univ., Japan

Session B5
System Design and Debugging

Co-Chairs : *Rajesh Gupta – Univ. of California, Irvine, USA*
Takashi Kambe – Sharp Corp., Japan

Session C5
Optimization Issues in Logic Synthesis

Co-Chairs : *Tsutomu Sasao – Kyushu Inst. of Technology, Japan*
Shin'ichi Minato – NTT Network Innovation Laboratories, Japan

Session D5
Novel Techniques in Advanced Partitioning

Co-Chairs : *Shin'ichi Wakabayashi – Hiroshima Univ., Japan*
Tetsushi Koide – Univ. of Tokyo, Japan

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Efficient Estimation for Interconnection

Co-Chairs : *Hiroshi Matsumoto – NEC Corp., Japan*
Xianlong Hong – Tsinghua Univ., China

Session A6
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Co-Chairs : *Chong-Min Kyung – Korea Advanced Inst. of Science and Technology, Korea*
Takashi Morie – Hiroshima Univ., Japan

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DSP and Memory Architecture

Co-Chairs : *Ichiro Kuroda – NEC Corp., Japan*
Keshab K. Parhi – Univ. of Minnesota, USA

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Validation and Test

Co-Chairs : *Cheng-Wen Wu – Univ. of California, Santa Barbara, USA*
Tomoo Inoue – Hiroshima City Univ., Japan

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Co-Chairs : *Jun-Dong Cho – Sungkyunkwan Univ., Korea*
Yoichi Shiraishi – Gunma Univ., Japan

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Co-Chairs : *Mineo Kaneko – Japan Advanced Inst. of Science and Technology, Japan*
Peter M. Lee – Hitachi Ltd., Japan

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Co-Chairs : *Kazuo Yano – Hitachi, Ltd., Japan*
Takao Onoye – Kyoto Univ., Japan

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Chair : *Masaharu Imai – Osaka Univ., Japan*

Session C7
Delay Testing and Design-For-Testability

Co-Chairs : *Yukiya Miura – Tokyo Metropolitan Univ., Japan*
Hiroshi Date – Inst. of Systems & Information Technologies Kyushu, Japan

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Industry-Academia Cooperation

Session E7
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Co-Chairs : *Hidetoshi Onodera – Kyoto Univ., Japan*

Nobuo Fujii – Tokyo Inst. of Technology, Japan

Session A8
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Co-Chairs : *Takayasu Sakurai – Univ. of Tokyo, Japan*

Makoto Ikeda – Univ. of Tokyo, Japan

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