Contents: Power and Delay

CMOS Static and Dynamic Power Consumption:
J Rabaey et al ”Digital Integrated Circutis”

Integration of III/V HEMTs on Si :
S Datta et al IEEE Electron Dev. Lett. 28, 2007 p 685 ” Ultrahigh-Speed 0.5 V Supply ...”

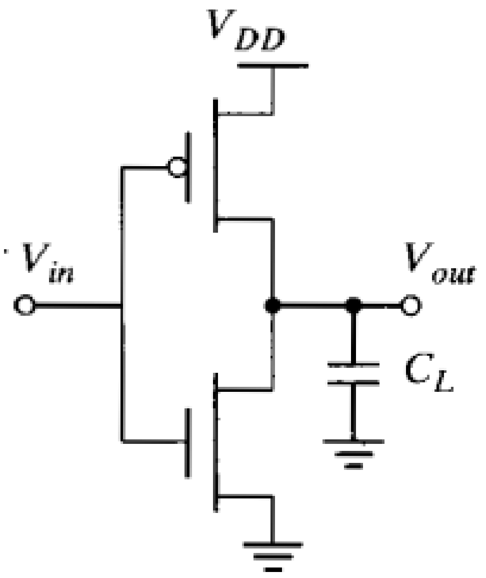
HEMTS for Beyond-CMOS:
D-H Kim et al IEEE Trans. Electron Dev. 54, 2007 p 2606 ” Logic Suitability of 50 nm ...”

CMOS Dynamic and Static Power Consumption

Advantages with CMOS:

Full logic swing
High noise margin
Superior robustness
Low steady state power consumption

Robust low-power digital technology



V_{out}=V_{in} for next stage
C_L both parasitics and gate capacitance

Dynamic Power Consumption

Advantages with CMOS:

Full logic swing
High noise margin
Superior robustness
Absence of steady state power consumption

Calculate the charging energy during one switching event!

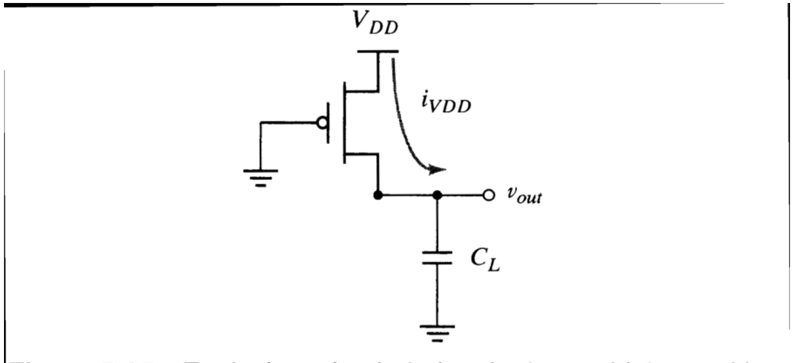


Figure 5-25 Equivalent circuit during the low-to-high transition.

Calculate the charging energy:

$$E_{VDD} = \int_0^{\infty} i_{VDD}(t) V_{DD}\, dt = V_{DD} \int_0^{\infty} C_L \frac{dv_{out}}{dt} dt = C_L V_{DD} \int_0^{VDD} dv_{out} = C_L V_{DD}^2$$

Calculate the stored energy:

$$E_C = \int_0^{\infty} i_{VDD}(t) v_{out}\, dt = \int_0^{\infty} C_L \frac{dv_{out}}{dt} v_{out}\, dt = C_L \int_0^{VDD} v_{out}\, dv_{out} = \frac{C_L V_{DD}^2}{2}$$

Dynamic Power Consumption

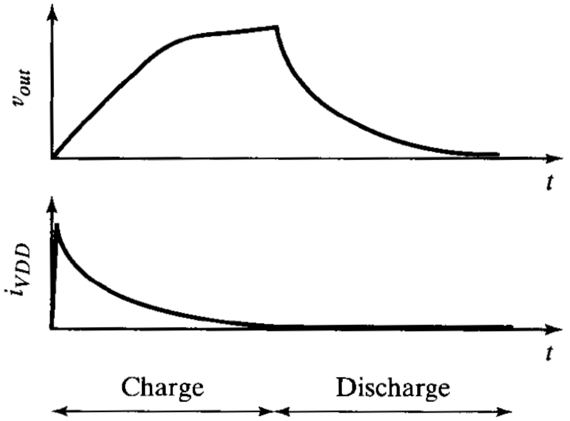


Figure 5-26 Output voltages and supply current during (dis)charge of C_L.

During charging (low-to-high transition) half energy is stored on capacitor, half energy is dissipated in the transistor

During discharging (high-to-low transition) half energy is stored on capacitor, the stored energy (half energy) is dissipated in the transistor

$$P_{dyn} = C_L V_{DD}^2 f_{0->1}$$

Example: 50 nm CMOS
f=2 GHz C_L=3 fF/gate
V_{DD}=1.0 V
P_{dyn}=6 μW

Note: Not all transistors active!
(effectively reduces frequency)
Voltage scaling reduces P_{dyn}
Scaling reduces gate capacitance, but increases parasitic capacitance!

Direct-Path Current Power Consumption

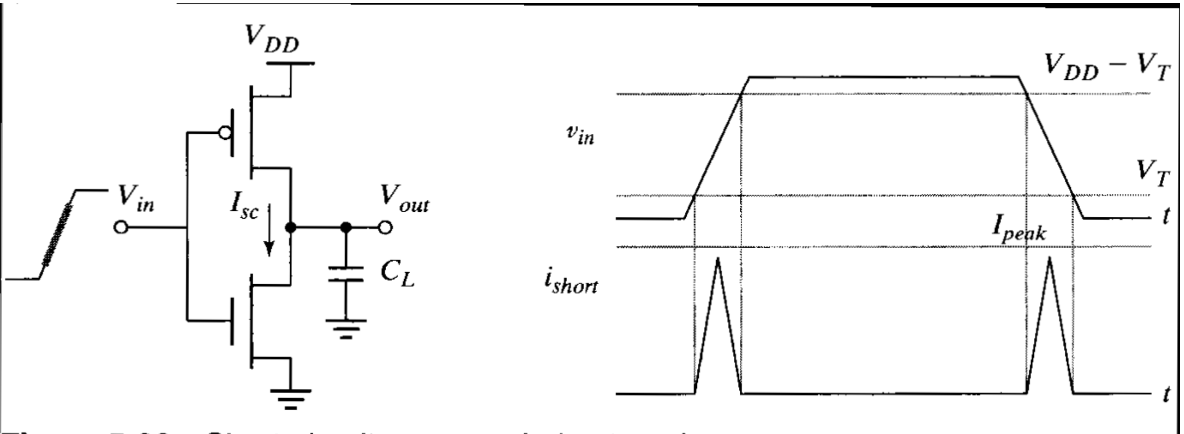


Figure 5-30 Short-circuit currents during transients.

During the finite time switching, a direct current is flowing in the transistor pair

Assume triangular current peaks

$$E_{dp} = V_{DD}\frac{I_{peak}t_{sc}}{2} + V_{DD}\frac{I_{peak}t_{sc}}{2} = t_{sc}V_{DD}I_{peak}$$

$$P_{dp} = t_{sc}V_{DD}I_{peak}f = C_{sc}V_{DD}^{2}f$$

This is typically a minor part of the power consumption

Static Power Consumption: Drain Leakage

Leakage current typically 10-100 pA/μm^2. Drain area 50 nm^2 and 1 billion gates with V_{DD}=1.0 V gives 0.5 μW.

$$P_{stat} = I_{stat}V_{DD}$$

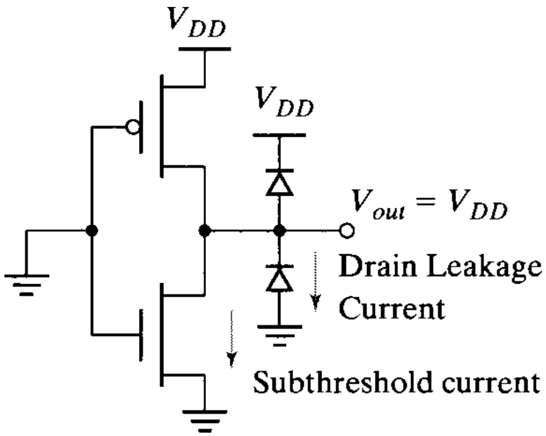


Figure 5-34 Sources of leakage currents in CMOS inverter (for V_{in} = 0 V).

Solution:
Use NWs to reduce channel leakage
Use SOI technology to reduce contact leakage

Static Power Consumption: Subthreshold Leakage

As the drive voltage is reduced, the threshold voltage should also be scaled (recall V_t~$V_{DD}/3$!). This implies that the subthreshold current is substantially increased.

Consider a 50 nm NMOS transistor with SS of 60 mV/dec. and V_t=0.4 V. At V_{GS}=0 V it consumes about 10^{-12} A. Reducing the threshold to 0.2 V increased the current a factor 300! In a 1 billion transistor operating at 1 V, we get a power consumption of 10^9x300x10^{-12}x1.0=300 mW!

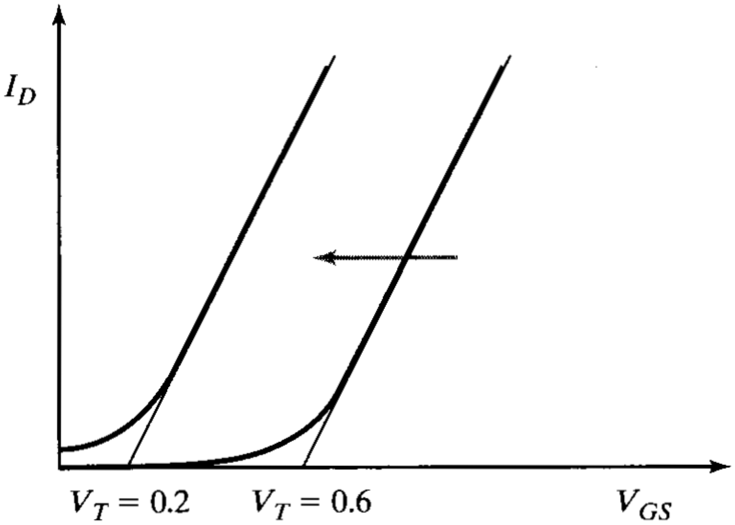
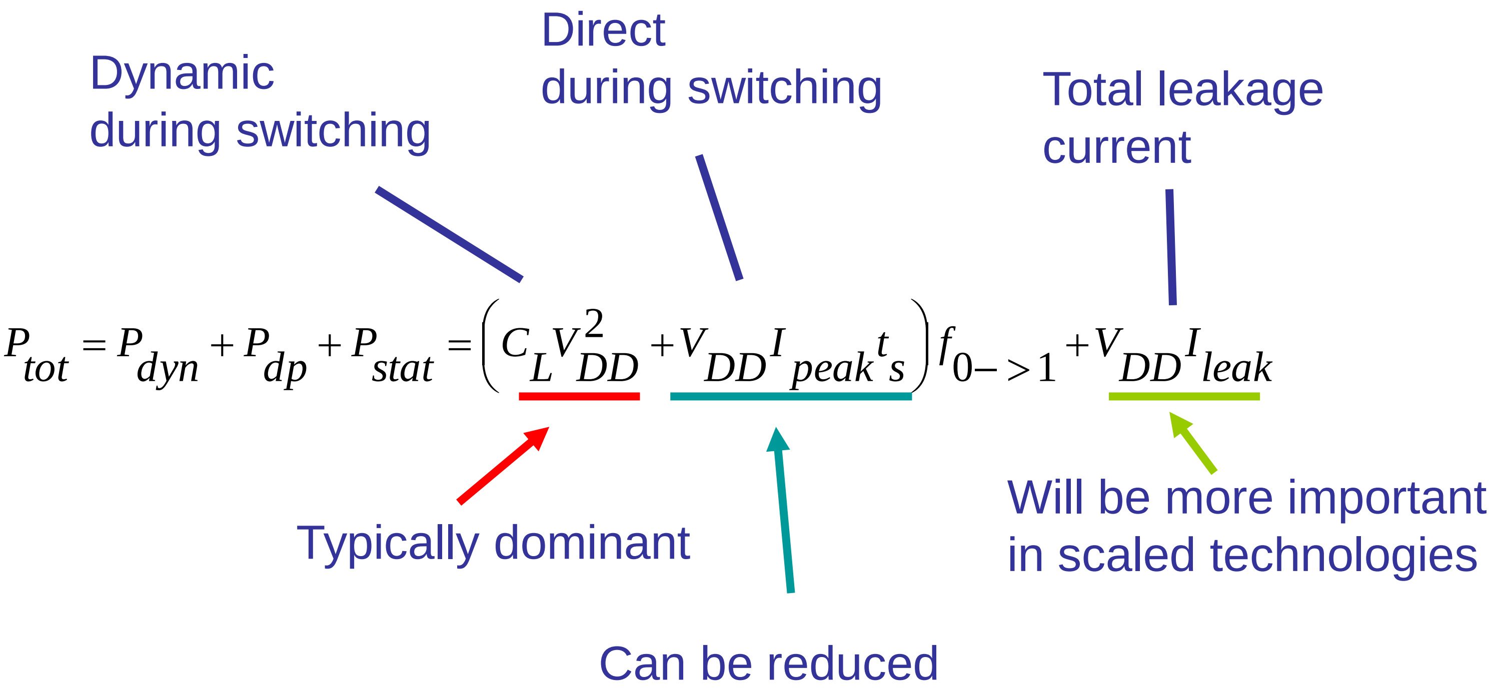


Figure 5-35 Decreasing the threshold increases the subthreshold current at $V_{GS} = 0$.

Threshold voltage key parameter to balance on- and off-state

Fundamental transistor problem!

Put It All Together!



Dynamic during switching

Direct during switching

Total leakage current

$$P_{tot} = P_{dyn} + P_{dp} + P_{stat} = \left(\underline{C_L V_{DD}^2} + \underline{V_{DD} I_{peak} t_s} \right) f_{0->1} + \underline{V_{DD} I_{leak}}$$

Typically dominant

Will be more important in scaled technologies

Can be reduced

The Power-Delay Product

Introduce the power-delay product
as a quality measure of a logic gate:

$$PDP = P_{av} t_p$$

If the gate is switched at full speed, the PDP corresponds
To the average energy consumed per switching event
(0->1 or 1->0 transition)

$$PDP = C_L V_{DD}^2 f_{\max} t_p = \frac{C_L V_{DD}^2}{2}$$

Better, The Energy-Delay Product

Introduce the energy-delay product, which
balances the performance and energy consumption!

$$EDP = PDP \times t_p = P_{av} t_p^2 = \frac{C_L V_{DD}^2}{2} t_p$$

t_p is the propagation delay (gate delay) and $f_{max}=1/(2t_p)$

Voltage Dependence on EDP!!!

$$EDP = PDP \times t_p = P_{av} t_p^2 = \frac{C_L V_{DD}^2}{2} t_p$$

$$t_p \approx \frac{\alpha C_L V_{DD}}{\left(V_{DD} - V_T\right)^2}$$

$$EDP = \frac{\alpha C_L^2 V_{DD}^3}{2(V_{DD} - V_T)^2}$$

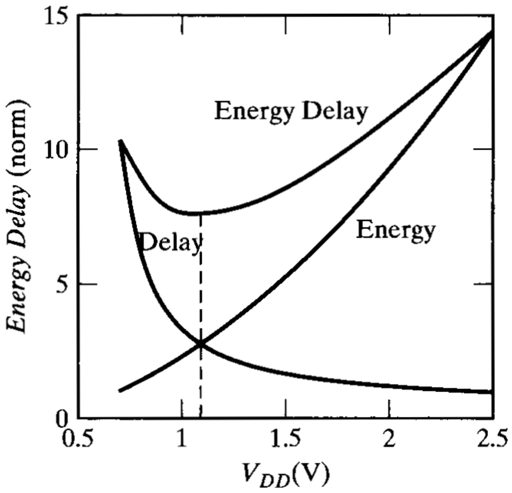


Figure 5-36 Normalized delay, energy, and energy-delay plots for CMOS inverter in 0.25-μm CMOS technology.

Increase V_d:

Speed improves
(higher current)
Energy increases
(more charge)
Optimum!

Extra (model validation):

$$t_p = \frac{t_{pHL} + t_{pLH}}{2} = \ln 2 \times C_L \left(\frac{R_{eqn} + R_{eqp}}{2}\right)$$

$$t_{pHL} = \ln 2 \times \frac{3}{4} \frac{C_L V_{DD}}{(W/L)_n \left(\mu_n \varepsilon_{ox}/t_{ox}\right)\left(V_{DD} - V_{Tp}\right)^2}$$

RC-time constant during switching

Use transistor equations to derive the effective transistor resistance

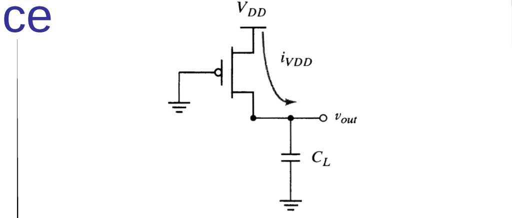
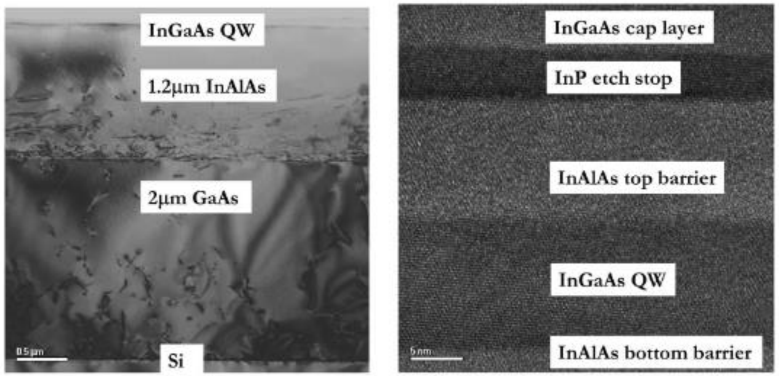


Figure 5-25 Equivalent circuit during the low-to-high transition.

Ultrahigh-Speed 0.5 V Supply Voltage $In_{0.7}Ga_{0.3}As$ Quantum-Well Transistors on Silicon Substrate

Suman Datta, *Senior Member, IEEE*, G. Dewey, J. M. Fastenau, *Member, IEEE*, M. K. Hudait, D. Loubychev, W. K. Liu, *Senior Member, IEEE*, M. Radosavljevic, W. Rachmady, and R. Chau, *Fellow, IEEE*



(a) (b)

Fig. 1. Cross-sectional TEM images of $In_{0.7}Ga_{0.3}As$ QW structures on Si using metamorphic buffer architecture: (a) Entire layer structure. (b magnification of $In_{0.7}Ga_{0.3}As$ QW along with bottom and top barrier layers. The misfit dislocations are predominantly contained in the buffer layer.

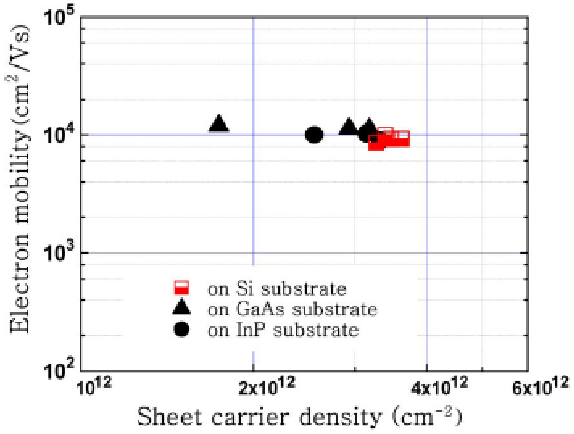
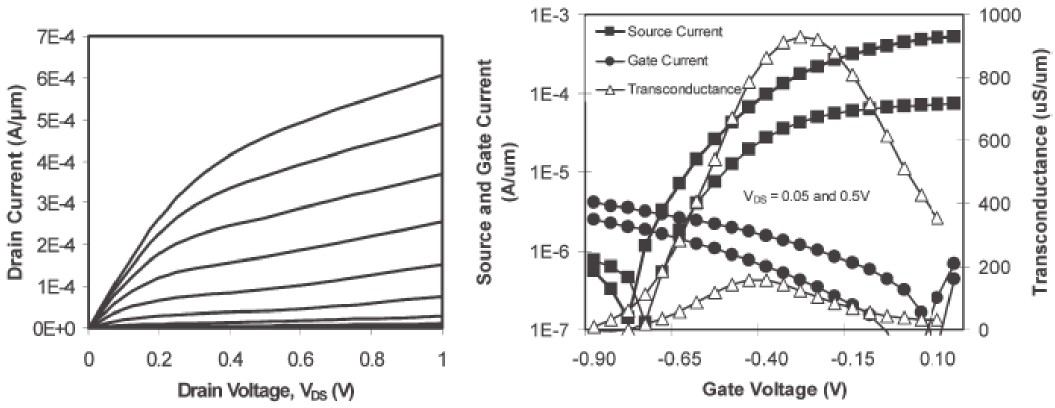


Fig. 2. Electron mobility versus sheet carrier density in n-channel $In_{0.7}Ga_{0.3}As$ QW device layers grown on Si, GaAs, and InP substrates. In all cases, $In_{0.52}Al_{0.48}As$ is the bottom and top barrier layer.

- buffer layer techniques are available
- comparable mobility

Comparable RF-data!



(a) (b)

Fig. 3. (a) Output characteristic for 80-nm L_g In$_{0.7}$Ga$_{0.3}$As QW transistor on 3.2-μm metamorphic buffer on silicon (gate voltage V_G is swept from 0.0 to −0.8 V in −0.1-V steps). (b) Transfer characteristic for 80-nm L_g In$_{0.7}$Ga$_{0.3}$As QW transistor on 3.2-μm buffer on silicon with $V_{\mathrm{DS}} = 0.5$ and 0.05 V. Peak transconductance g_{m} for this device was 930 μS/μm at $V_{\mathrm{DS}} = 0.5$ V.

- well behaved IV characteristics!
- good DC numbers at 80 nm Lg
- comparable RF data to lattice matched devices

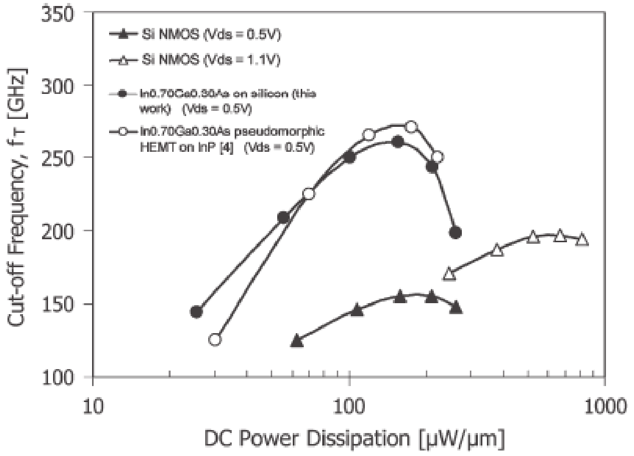
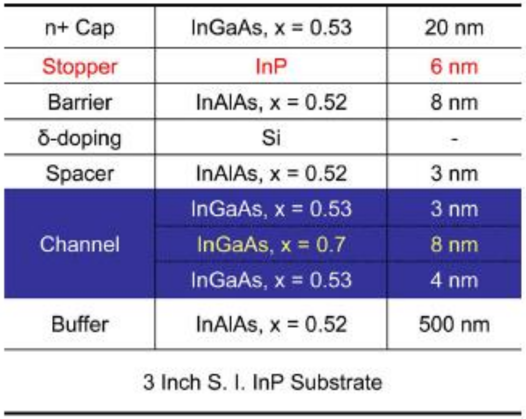


Fig. 4. Plot of deembedded unity gain cutoff frequency as a function of dc power dissipation for 0.5-V V_{DS} 80-nm L_g In$_{0.7}$Ga$_{0.3}$As QW transistors on both silicon and InP substrates, benchmarked against 60-nm L_g silicon NMOS transistors at $V_{\mathrm{DS}} = 0.5$ and 1.1 V.

Logic Suitability of 50-nm $In_{0.7}Ga_{0.3}As$ HEMTs for Beyond-CMOS Applications

Dae-Hyun Kim, Jesús A. del Alamo, Jae-Hak Lee, and Kwang-Seok Seo



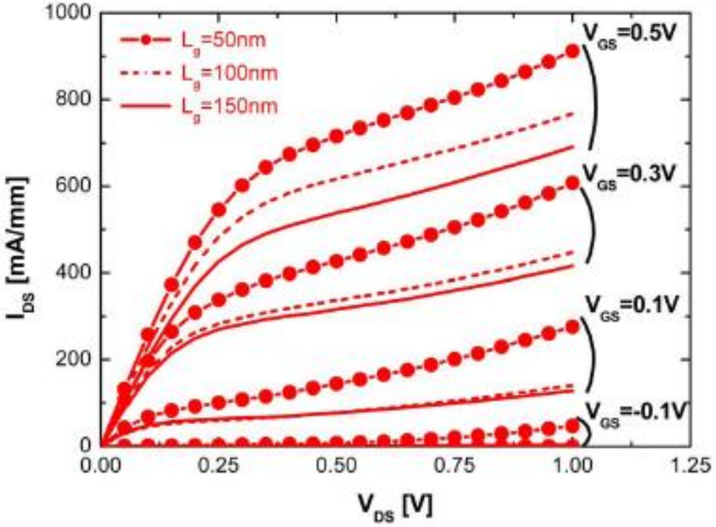
n+ Cap	InGaAs, x = 0.53	20 nm
Stopper	InP	6 nm
Barrier	InAlAs, x = 0.52	8 nm
δ-doping	Si	-
Spacer	InAlAs, x = 0.52	3 nm
Channel	InGaAs, x = 0.53	3 nm
	InGaAs, x = 0.7	8 nm
	InGaAs, x = 0.53	4 nm
Buffer	InAlAs, x = 0.52	500 nm
3 Inch S. I. InP Substrate		

Fig. 1. Epitaxial layer structure of the $In_{0.7}Ga_{0.3}As$ HEMTs that are fabricated in this paper.

TABLE I
DETAILED GATE STRUCTURAL INFORMATION FOR FOUR TYPES OF $In_{0.7}Ga_{0.3}As$ HEMTs THAT ARE FABRICATED IN THIS PAPER

	Type-A	Type-B	Type-C	Type-D
Barrier	$InP/In_{0.52}Al_{0.48}As$	$In_{0.52}Al_{0.48}As$	$In_{0.52}Al_{0.48}As$	$In_{0.52}Al_{0.48}As$
Stack	Ti/Pt/Au	Ti/Pt/Au	Pt/Ti/Mo/Au	Buried-Pt/Ti/Mo/Au
t_{ins} [nm]	17	11	11	7
Φ_B [eV]	~ 0.4	~ 0.6	~ 0.7	~ 0.8

- 4 types of transistors
- Schottky barrier and insulator thickness
- good DC characteristics
- weak scaling with gate length



(d)

Scaling with Schottky barrier and insulator thickness

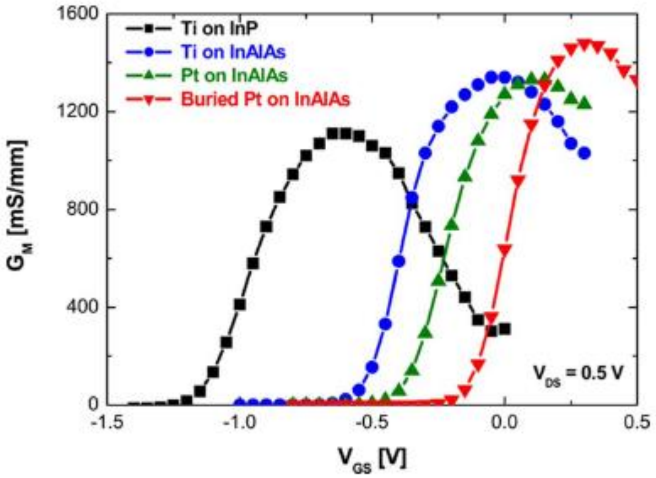


Fig. 5. Transconductance (G_m) characteristics of all 50-nm $In_{0.7}Ga_{0.3}As$ HEMTs at $V_{DS} = 0.5$ V.

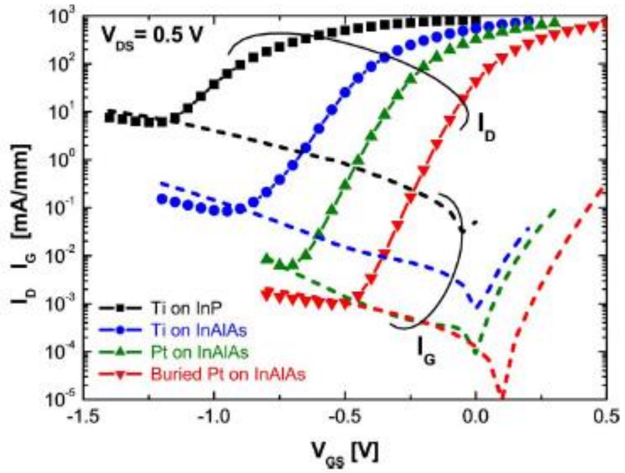


Fig. 6. Semilog plot of I_D and I_G of all 50-nm $In_{0.7}Ga_{0.3}As$ HEMTs at $V_{DS} = 0.5$ V.

- Tight control needed to improve the performance

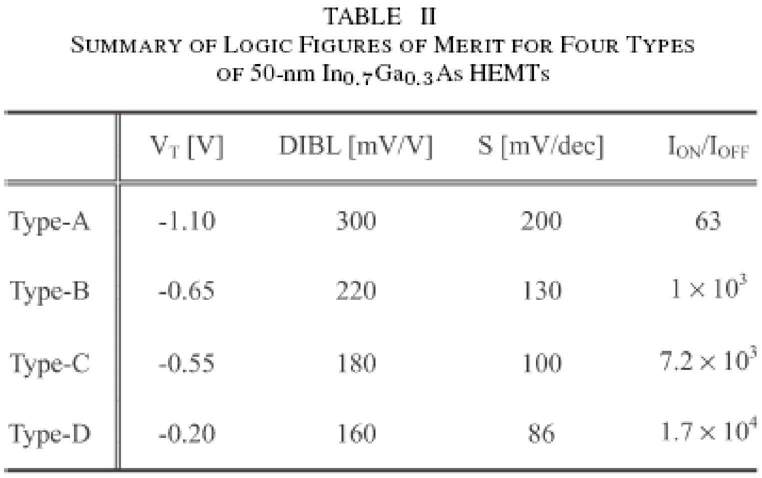


TABLE II
SUMMARY OF LOGIC FIGURES OF MERIT FOR FOUR TYPES OF 50-nm $In_{0.7}Ga_{0.3}As$ HEMTs

	V_T [V]	DIBL [mV/V]	S [mV/dec]	I_{ON}/I_{OFF}
Type-A	-1.10	300	200	63
Type-B	-0.65	220	130	1×10^3
Type-C	-0.55	180	100	7.2×10^3
Type-D	-0.20	160	86	1.7×10^4

Improved speed and/or reduced power consumption

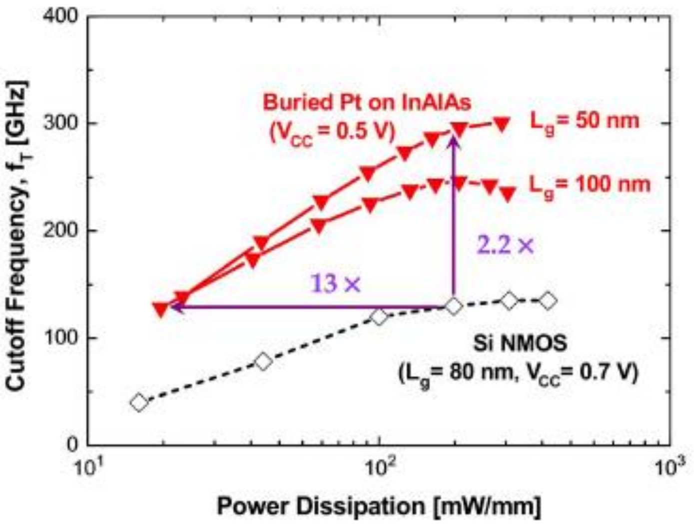


Fig. 11. Cutoff frequency (f_T) of our 50- and 100-nm type D $\mathrm{In_{0.7}Ga_{0.3}As}$ HEMTs and 80-nm Si MOSFETs as a function of the dc power dissipation.

- Depending on bias condition benefits can be found in the areas of speed and/or power dissipation

- Well selected technology is required to maximize Ion/Ioff ratio

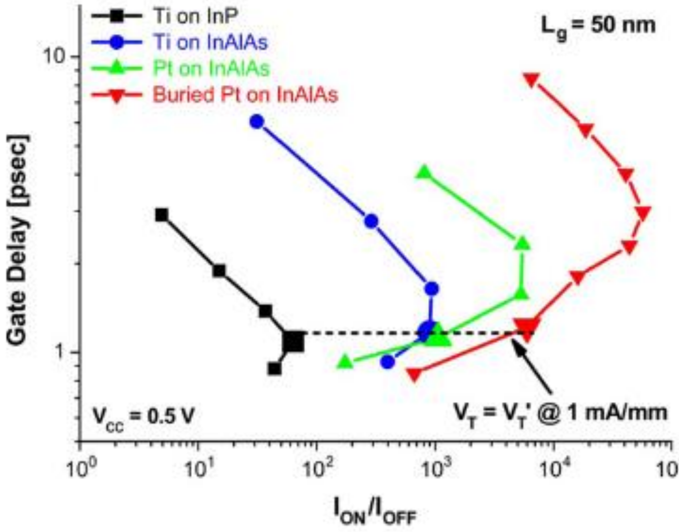


Fig. 14. Gate delay (CV/I) of all 50-nm $\mathrm{In_{0.7}Ga_{0.3}As}$ as a function of $I_{\mathrm{ON}}/I_{\mathrm{OFF}}$.