DOUBLE-POLE COMPENSATION AND THE PUSH-PULL TRANSIMPEDANCE STAGE IN DISCRETE AUDIO FREQUENCY POWER AMPLIFIERS

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Everything should be made as simple as possible—but no simpler! ~ Albert Einstein

Introduction

Sometime ago a fascinating debate ensued[1,2,3,4] in respect of improvements that might be made to the venerable double cascaded differential stages (DCDS) gain block recommended by Hitachi[5] for use with their power MOSFETs.

Alas, there was much missing of the point, as the suggested modifications did not accommodate the essential linearity-enhancing techniques detailed by Douglas Self in his seminal work[6,7,8]. It is demonstrated here that such a topology need not compromise on linearity; however, the increase in complexity and cost may be relatively significant.

The transient and steady state conduct of an amplifier is inextricably linked to the choice of frequency stabilisation. Prominence is therefore given to a first-order analysis of double-pole compensation as a desirable and cost-effective means of reducing forward-path error. A brief overview of loop transmission and its determination in context is also provided. A first-principals approach is preferred and adhered to whenever appropriate.

The Classical Topology

The circuit of **figure 1** is, with some modification, broadly similar to Self's adaptation, for medium power discrete-component audio power amplification, of the two-stage voltage gain topology attributed to J. E. Thompson by Messrs Russell and Solomon[9]. Incidentally, this circuit is sometimes inexplicably and somewhat tendentiously classified[10] as the "Lin" topology after the inventor[11] of the single gain stage quasi-complementary design shown in its entirety in **figure 2**. In fact the only shared feature of significance in the two schemes is the absence of the archaic load-matching transformer first eliminated by Lin's design.

This circuit (**fig. 1**) contains the fundamental elements of virtually all modern high-performance voltage amplifiers, and, thus, it constitutes an invaluable reference against which the merits of alternative approaches may be judged[12]. A thorough appreciation of its virtues and limitations is therefore essential.

It consists of a transadmittance input stage (TAS for concision) in the form of differential pair **T1**, **T2**, with emitter-degeneration resistors, **R1**, **R2**, Widlar's current mirror[13,14] **T3**, **T4** and a so-called tail in the form of *amplified negative feedback* (ANF) current source **T5/T9**. The TAS is effectively a voltage-controlled current source (VCCS) whose output current is proportional to the differential input voltage. At frequencies preceding the amplifier's first non-dominant pole input stage transadmittance gain may, with negligible error, be assumed to be equal to its DC transconductance.

The impedance at **T2**'s collector is negligible, virtually eliminating Miller feedback through its collector-base intrinsic capacitance. This transistor is effectively an emitter follower and, consequently, its comparatively low net input capacitance permits the connection of large feedback network impedances before the pole at its base becomes significant[15].

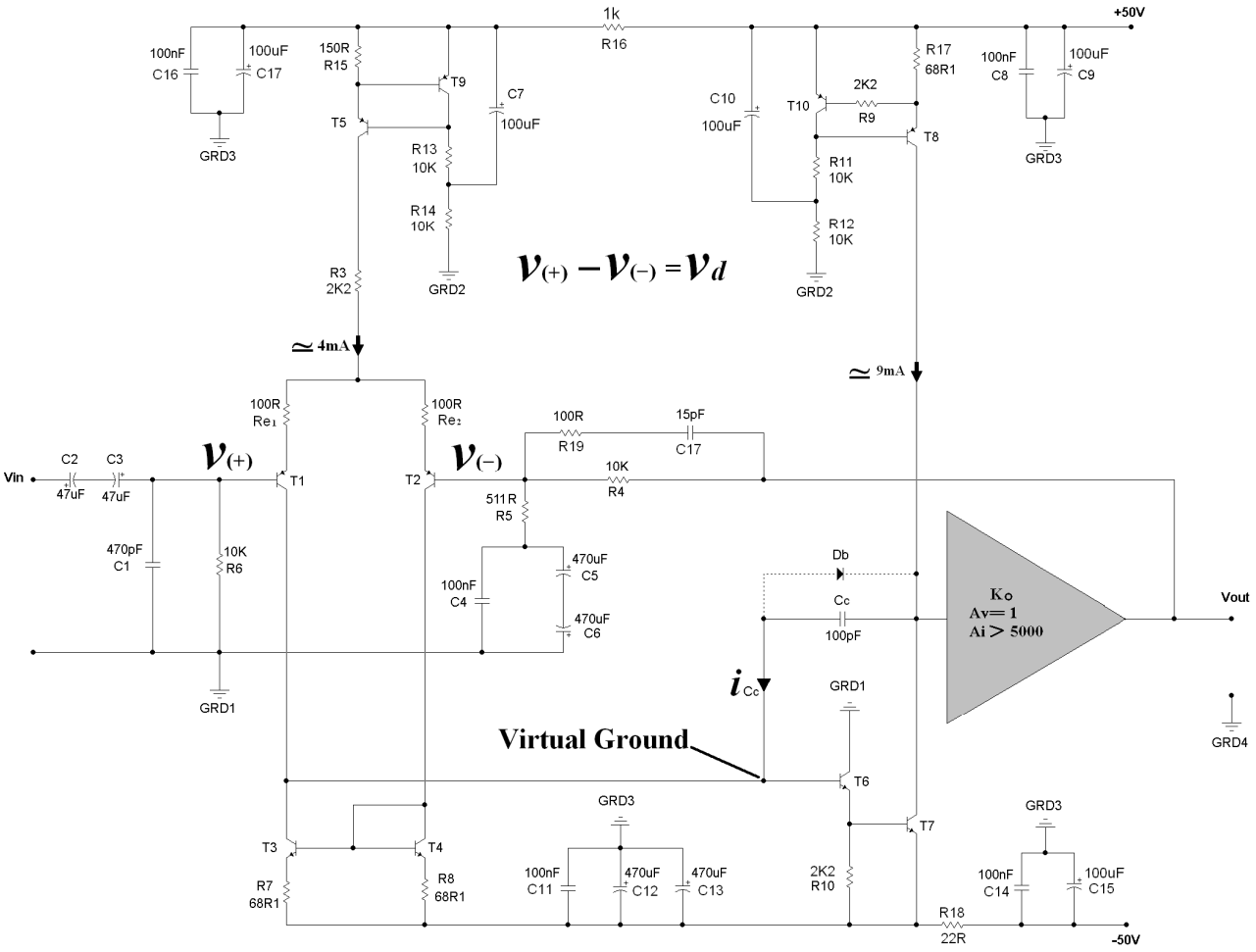


Figure 1. The generic or Thompson topology (or variations thereof) is representative of the majority of commercial designs. The error voltage v_d which drives the amplifiers forward path is merely the difference between the input and feedback voltages. Note that all four grounds are returned independently to the power supply 'star-point'.

Emitter degeneration in the TAS ($\mathbf{R_{e1}}$ and $\mathbf{R_{e2}}$) constitutes series-applied local negative feedback, which trades a measure of transconductance for enhanced linearity, and is conducive for trouble-free stabilisation without mandating the use of an inordinately large slew-rate-sapping Miller feedback capacitor $\mathbf{C_C}$ across the second stage. The gain block $\mathbf{K_o}$ represents the output stage, which is usually (but not exclusively[16,17]) a unity voltage gain complementary symmetry buffer of substantial current gain.

The current mirror facilitates differential-to-single ended conversion and forces equality of collector currents in the differential pair[18]. This minimises DC offset at the output of the amplifier and is a necessary requirement for the elimination of second order distortion generated by the input stage[19]. The mirror also doubles the symmetrical current sourcing and sinking ability of the stage over that obtainable with a resistive load. Degeneration resistors **R7** and **R8** promote equality of currents in the mirror by swamping variations in the base-emitter voltages of its transistors **T3** and **T4**.

The ANF active current source **T9/T5** significantly improves the common-mode and power supply rail rejection ratios of the stage over those attainable with a simple resistive source. However, a resistive load does not amplify its internal noise, and therefore possesses the advantage of producing somewhat less noise than would be generated by the current mirror or active current source.

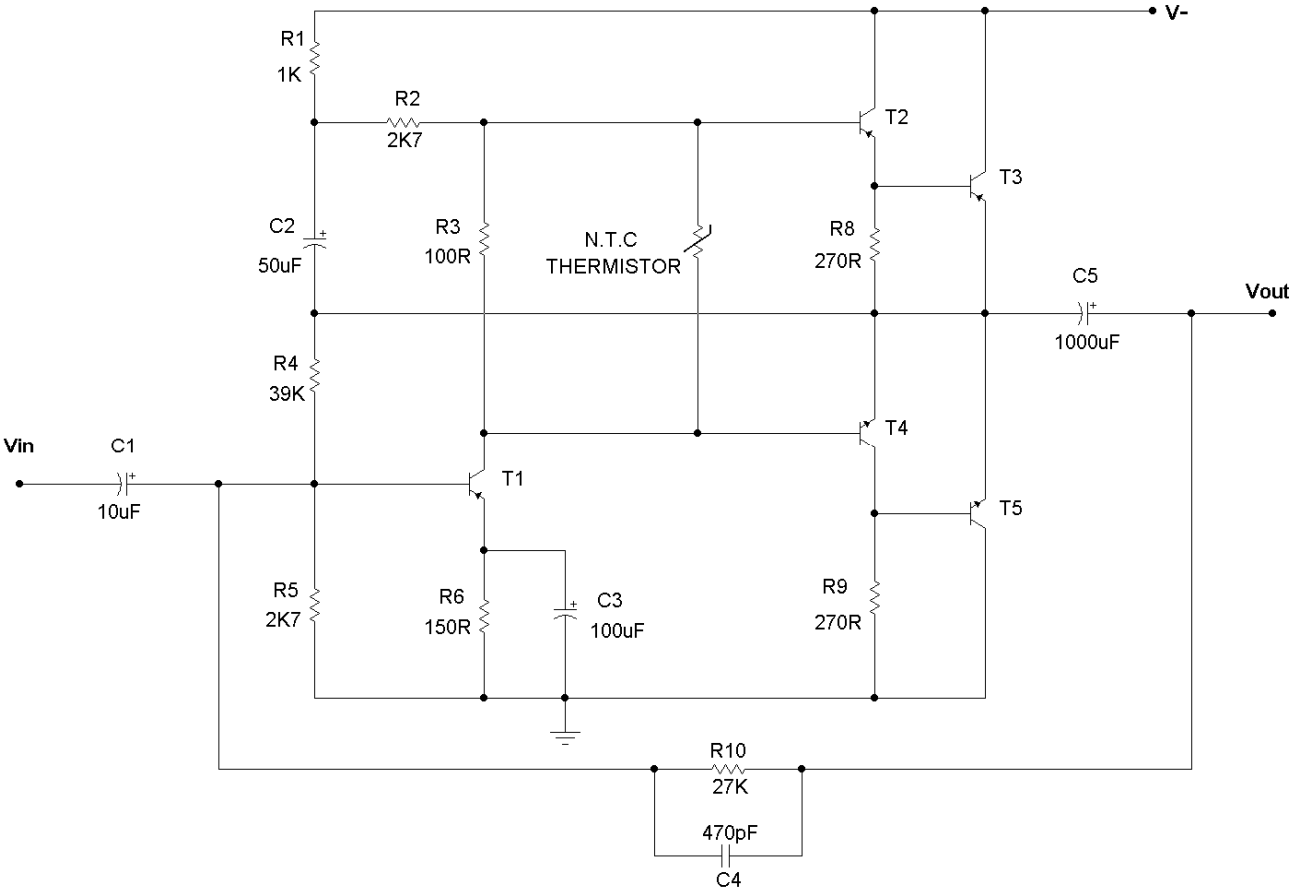


Figure 2. The first 'transformerless' quasi-complimentary power amplifier-due to H. C. Lin.

Capacitor **C7** filters out residual power supply ripple in the bias current established by resistors **R13** and **R14**. The temptation to connect **C7** directly across **T9** should be resisted as it couples supply ripple directly into the current source [20].

The second stage, comprising **T6**, **T7** and ANF current source **T8/T10**, is effectively linearised and converted into a near-ideal transimpedance amplifier stage (TIS) by local shunt (voltage) derived-shunt (current) applied (*viz*. admittance) frequency dependant negative feedback, courtesy of the Miller compensation (or stabilising) capacitor $\mathbf{C_C}$.

The TIS is effectively a current-controlled voltage source (CCVS) at the frequencies of interest, and ideally requires infinitely large source and load impedances for maximal transimpedance gain. These conditions are best realised in practice by employing a first-stage current mirror and a high current-gain output buffer.

Minor loop negative feedback due to $\mathbf{C_C}$ reduces the TIS's input impedance pro rata with increasing frequency, making it negligible (virtually zero) compared to the TAS's output impedance. The local feedback loop also reduces the TIS's output impedance, reducing distortion generated by the non-linear loading of a class-B (or AB) output stage on the second stage [21].

Although the second stage is often [8] referred to as the "voltage amplifier stage" (VAS), this is technically incorrect, as it implies that the stage is a voltage controlled voltage source (VCVS). In fact, a closed-loop VCVS is synthesised by the application of shunt (voltage) derived-series (voltage) applied negative feedback, which clearly does not obtain with the TIS.

Open loop transimpedance gain local to the second stage is, to a good first approximation, merely the product of the stage's current gain, and the effective impedance at its output (**appendix A**). Thus emitter follower **T6** increases local forward-path gain (and therefore local feedback through $\mathbf{C_C}$) by increasing the second stage's effective current gain.

Apart from improved second stage linearity, this is also desirable for enhanced stability margins because the degree to which dominant and first non-dominant poles are separated varies directly as the local open-loop gain of the compound stage enclosed by the compensation capacitor. Note that the emitter follower **T6** may not be included within the minor loop if **T7** is replaced with a cascode, as this is virtually certain to make the local feedback loop unstable (**appendix D**).

A fast recovery (Baker clamp) diode $\mathbf{D_b}$ is often used to prevent **T7** from being driven into saturation by excessive (clipped) negative voltage swings. The diode prevents **T7**'s base-collector junction from being forward-biased, which facilitates rapid recovery from clipping overload by drastically reducing the storage of excess minority charge carriers.

While the Baker clamp is often mandatory in switching applications, its use with the current-gain enhanced TIS of **figure 1** is not recommended in domestic linear audio amplifiers. This is because the non-linear variation of the diode's junction capacitance with output voltage effects a disproportionate deterioration in linearity.

Alternatively, delayed recovery from clipping in **T7** may be avoided by merely using Darlington's arrangement. This is realised by simply connecting the collectors of **T7** and **T6**; the base-collector junction of **T6** then assumes the clamping action of diode $\mathbf{D_b}$. Regrettably, this also increases distortion for the reasons outlined above [22].

A significant reduction in the value of bias resistor **R10** may be considered instead. This expedites the extraction of excess minority carriers from common-emitter transistor **T7** subsequent to being driven into saturation. The smaller the value of **R10**, the faster minority carriers can be removed, and the faster **T7** recovers from saturation.

However, an excessively small value may significantly reduce the compound pair's effective current gain; setting **R10**'s quiescent current to roughly 10% of **T7**'s collector current is a good compromise, while values as high as 50% were found to have no significant adverse effect on linearity. Indeed, if transistors **T3**, **T4** and **T6** are closely matched with respect to current gain, then making **R10**'s standing current roughly equal to that supplied by the TAS's current source reduces collector current mismatch in the mirror due its own base current demands.

Unfortunately, reducing the value of **R10** may not entirely obviate the unpleasant voltage spikes and/or intermittent parasitic oscillation that sometimes accompany prolonged overdrive into saturation. In some applications, such as public address systems, where the amplifier is likely to be frequently driven to clip, diode $\mathbf{D_b}$ may have to be used after all. It will later be demonstrated that a cascode TIS can be used with an anti-saturation diode without compromising linearity.

The base resistor **R9** in the TIS's current source cell is presently fashionable, and is used ostensibly to protect **T10** by limiting its base current in the event of **T8** failing short-circuit. However, this resistor reduces loop transmission local to the current source, and should either be shunted by 1uF, kept small or removed altogether.

Slew–rate Considerations

The majority of domestic applications seldom demand more than $40\mathbf{V}_{[\mathbf{peak}]}$ (200W into 4Ω) swing from a power amplifier. Therefore assuming, as is the custom, a 20Hz~20KHz audio bandwidth, a nominal slew rate of 5.03V/uS should suffice for such an amplifier.

However, Jung [24] recommends a "conservative" [*sic*] factor of up to eight times this figure solely to ameliorate first-stage non-linearity provoked by increased loading with frequency of the TIS's compensation capacitor on the first stage. Such non-linearity is certainly detectable within the audio-band long before the amplifier's slew limit is approached, but need only be of concern in a single-pole Miller-feedback-compensated design with an undegenerated differential input stage [7].

Indeed, Jung's conclusions in his "Hi-Fi Choice" article are based entirely on data from precisely such an operational amplifier-the venerable **LM301A**. This is rather misleading, as no account is taken of the fact that such distortion, in a suitably degenerated differential stage, may be virtually eliminated at audio frequencies by merely replacing the single-pole compensation capacitor with an inexpensive double-pole network. Compared to single-pole compensation, the two-pole method can reduce the current demands of the TIS on the input stage by more than an order of magnitude across the audio band.

Nevertheless, an amplifier with a power bandwidth of 20KHz (~5.03V/uS at $40\mathbf{V}_{[\mathbf{peak}]}$), is unlikely to process audio-frequency stimuli if at some point it is simultaneously driven beyond its slew limits by ultrasonic spuriae [25,26]. Further work by Paul Miller [27] suggests a link exists between the perceived fidelity of an amplifier and its susceptibility to radio frequency interference (RFI). Therefore Jung's criterion of 1V/uS per peak output volt (*viz*. power bandwidth $\mathbf{f}_{\mathbf{pb}} \geq \left[(1/2\pi)\times 10^{6}\right]\mathbf{Hz} \approx 160\mathbf{KHz}$) may be appropriated after all to make an amplifier less prone to being driven into slew limiting by RFI.

Note that providing for a relatively high slew rate merely increases the magnitude of error signal $\boldsymbol{v}_{\boldsymbol{d}}$ required to drive the amplifier to slew overload at ultrasonic frequencies, and does not of itself confer immunity to radio frequency interference. Therefore, such provision does not absolve one from providing rigorous RFI protection for one's design, and should merely be viewed as a desirable complement to established and perforce more effective means such as shielding and filtration of all electrical portals to the amplifier. This is the purpose of capacitor **C1** which, in conjunction with the preamplifier's output impedance, attenuates any radio frequency interference present at the power amplifier's input.

Double-pole Compensation

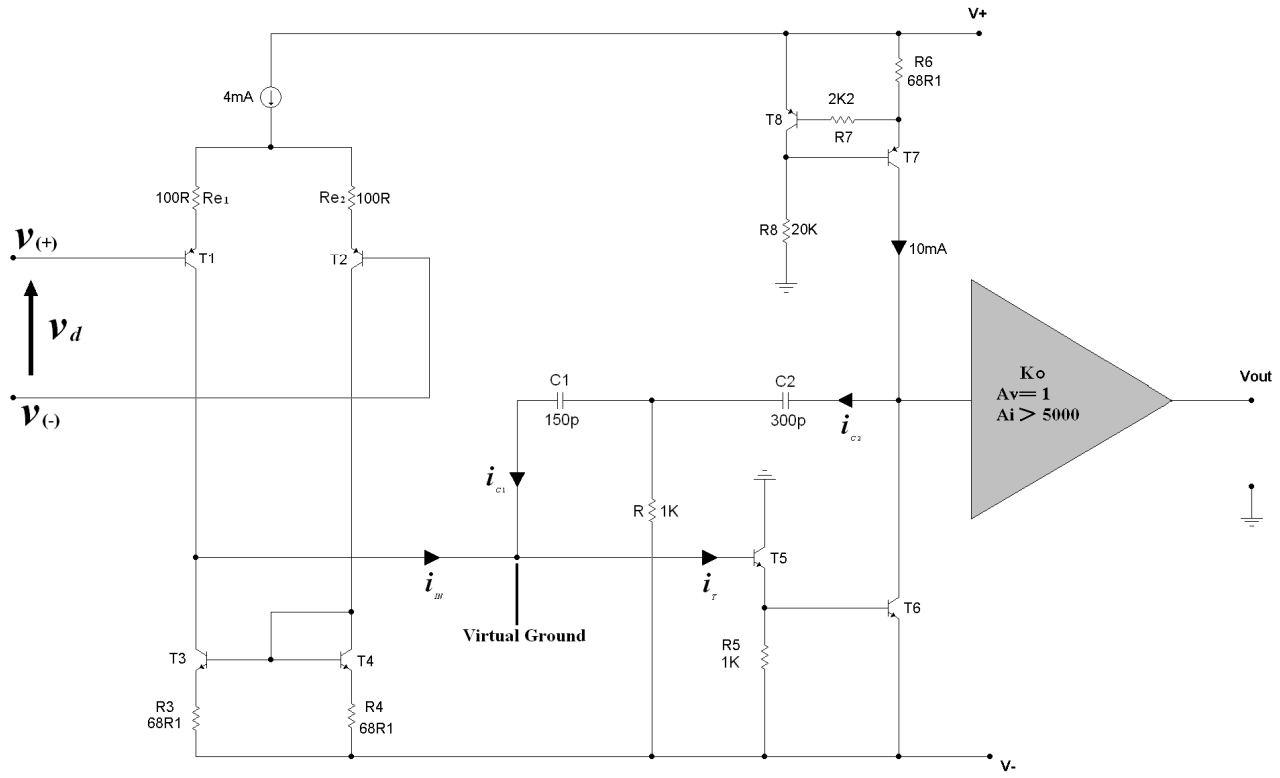


Figure 3. The generic topology with double-pole compensation.

Single pole Miller-feedback compensation usefully enhances forward-path bandwidth over that obtainable if the single-pole roll-off were realised by merely increasing shunt-capacitance at the input or output nodes of the TIS (**appendix A**). Nevertheless, the single-pole roll-off ensures that at high audio frequencies forward-path gain (and therefore loop gain) is reduced to such an extent that non-linearity in the output stage dominates the amplifier's performance.

The double-pole network consisting of $\mathbf{R}$, $\mathbf{C}_1$ and $\mathbf{C}_2$ (**fig. 3)** replaces the single dominant pole with a complex conjugate pole pair, characterized by two coincident breaks of -20 dB/decade (one from each member of the pair), giving a total change in slope of -40 dB/decade (**fig. 5**). The forward-path response then reverts to a single pole roll-off at a zero defined when the impedance modulus of $\mathbf{C}_1$ in parallel with $\mathbf{C}_2$ equals the value of resistor $\mathbf{R}$.

This characteristic allows the dominant pole-pair to be assigned to a vastly higher frequency than is possible with a single dominant pole. Thus, high forward-path gain is maintained over a much wider frequency range without increasing the critical unity-gain frequency. Indeed, with the component values shown (**figs. 3** and **4**), nearly as much forward-path gain is available at 20KHz with the double-pole network as is obtained at 1KHz with single-pole Miller compensation (**fig. 5**).

The generic topology of **figure 3** is modelled in **figure 4** by a differential voltage controlled current source (VCCS) driving a TIS consisting of a current controlled current source (CCCS) and load resistor $\mathbf{R}_{eq}$; the latter is the means by which the TIS's output current is expressed as a voltage.

Resistor $\mathbf{R}_{eq}$ represents the modulus of the effective impedance at the collector of **T6**, and comprises the parallel combination of the TIS's output impedance and the input impedance of the output buffer. TIS current gain $\beta_{eq.}$ is merely the product of the current gains of transistors **T5** and **T6**.

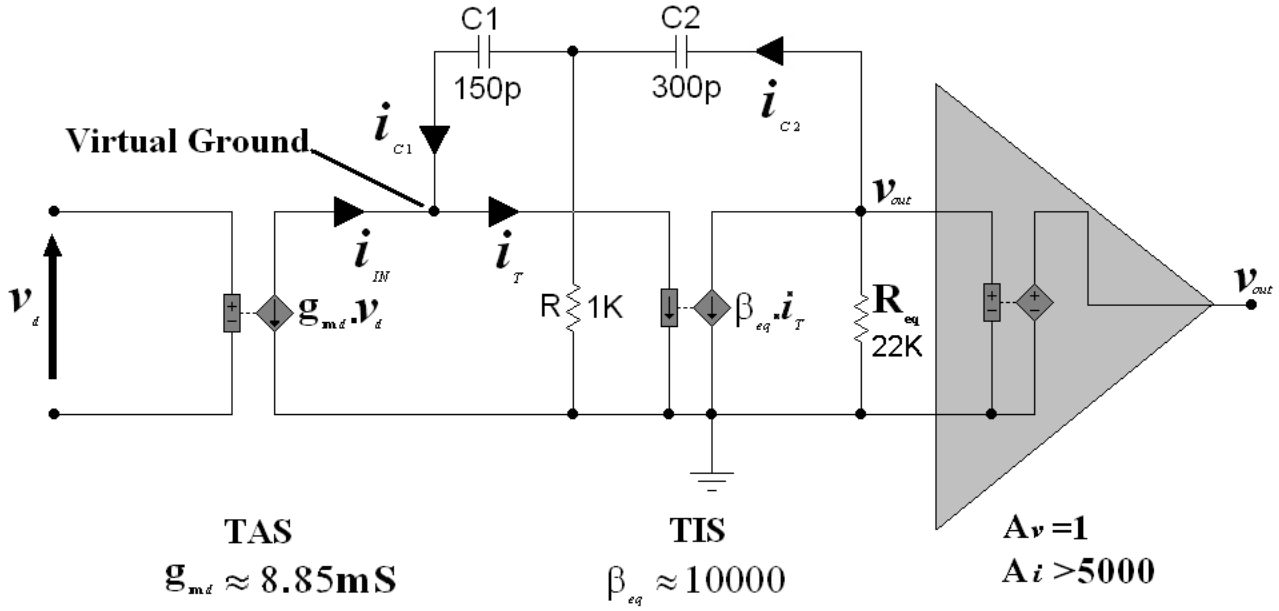


Figure 4. First-order model of the double-pole compensated voltage gain block.

It is assumed here that the local feedback loop enclosed by the double-pole network is stable, and that the amplifier's forward path unity-gain frequency f_U is sufficiently low so that non-dominant poles have negligible effect on its open-loop transfer function.

Invoking Kirchoff's current Law with respect to the output node (**Fig. 4**)

$$-i_{C2} - \beta_{eq} i_T + \frac{(0 - v_{out})}{R_{eq}} = 0$$

$\Rightarrow$

$$i_{C2} + \beta_{eq} i_T + \frac{v_{out}}{R_{eq}} = 0 \qquad (1)$$

Similarly at the TIS's input node

$$i_{in} + i_{C1} - i_T = 0 \qquad (2)$$

It is assumed (with negligible error) that the input to the TIS is a virtual ground at the frequencies of interest. Thus $\mathbf{R}$ and $\mathbf{C}_1$ are effectively in parallel, and

$$i_{C2} = \frac{v_{out}}{1/sC_2 + \frac{R/sC_1}{R + 1/sC_1}} \qquad (3)$$

By current division

$$\boldsymbol{i}_{C1} = \boldsymbol{i}_{C2}\left(\frac{\boldsymbol{R}}{\boldsymbol{R}+1/\boldsymbol{sC}_1}\right) \tag{4}$$

Substituting **(3)** into **(1)**

$$\frac{\boldsymbol{s}^2\boldsymbol{C}_1\boldsymbol{C}_2\boldsymbol{R}\boldsymbol{v}_{out}+\boldsymbol{sC}_2\boldsymbol{v}_{out}}{1+\boldsymbol{sR}(\boldsymbol{C}_1+\boldsymbol{C}_2)}+\beta_{eq}\boldsymbol{i}_T+\frac{\boldsymbol{v}_{out}}{\boldsymbol{R}_{eq}}=0 \tag{5}$$

Substituting **(3)** into **(4)**

$$\boldsymbol{i}_{C1}=\frac{\boldsymbol{s}^2\boldsymbol{C}_1\boldsymbol{C}_2\boldsymbol{R}\boldsymbol{v}_{out}}{1+\boldsymbol{sR}(\boldsymbol{C}_1+\boldsymbol{C}_2)} \tag{6}$$

Substituting **(6)** into **(2)**

$$\boldsymbol{i}_{in}+\frac{\boldsymbol{s}^2\boldsymbol{C}_1\boldsymbol{C}_2\boldsymbol{R}\boldsymbol{v}_{out}}{1+\boldsymbol{sR}(\boldsymbol{C}_1+\boldsymbol{C}_2)}-\boldsymbol{i}_T=0 \tag{7}$$

Equation (7) is multiplied by β_{eq} as a prelude to eliminating $\boldsymbol{i}_T$:

$$\boldsymbol{i}_{in}\beta_{eq}+\frac{\boldsymbol{s}^2\boldsymbol{C}_1\boldsymbol{C}_2\boldsymbol{R}\boldsymbol{v}_{out}\beta_{eq}}{1+\boldsymbol{sR}(\boldsymbol{C}_1+\boldsymbol{C}_2)}-\beta_{eq}\boldsymbol{i}_T=0 \tag{8}$$

Thus, adding equation **(5)** to **(8)** eliminates $\boldsymbol{i}_T$:

$$\boldsymbol{i}_{in}\beta_{eq}+\frac{\boldsymbol{s}^2\boldsymbol{C}_1\boldsymbol{C}_2\boldsymbol{R}\boldsymbol{v}_{out}\beta_{eq}}{1+\boldsymbol{sR}(\boldsymbol{C}_1+\boldsymbol{C}_2)}+\frac{\boldsymbol{s}^2\boldsymbol{C}_1\boldsymbol{C}_2\boldsymbol{R}\boldsymbol{v}_{out}+\boldsymbol{sC}_2\boldsymbol{v}_{out}}{1+\boldsymbol{sR}(\boldsymbol{C}_1+\boldsymbol{C}_2)}+\frac{\boldsymbol{v}_{out}}{\boldsymbol{R}_{eq}}=0$$

$\Rightarrow$

$$\frac{\boldsymbol{v}_{out}}{\boldsymbol{i}_{in}}(\boldsymbol{s})=\frac{-\beta_{eq}\boldsymbol{R}_{eq}\{1+\boldsymbol{sR}(\boldsymbol{C}_1+\boldsymbol{C}_2)\}}{1+\boldsymbol{s}\{\boldsymbol{C}_2\boldsymbol{R}_{eq}+\boldsymbol{R}(\boldsymbol{C}_1+\boldsymbol{C}_2)\}+\boldsymbol{s}^2\boldsymbol{C}_1\boldsymbol{C}_2\boldsymbol{R}\boldsymbol{R}_{eq}(\beta_{eq}+1)}$$

Since $(\beta_{eq}>>1)$ then it may be assumed, with trivial error, that $(\beta_{eq}+1)\approx\beta_{eq}$, such that

$$\frac{\boldsymbol{v}_{out}}{\boldsymbol{i}_{in}}(\boldsymbol{s})\approx\frac{-\beta_{eq}\boldsymbol{R}_{eq}\{1+\boldsymbol{sR}(\boldsymbol{C}_1+\boldsymbol{C}_2)\}}{1+\boldsymbol{s}\{\boldsymbol{C}_2\boldsymbol{R}_{eq}+\boldsymbol{R}(\boldsymbol{C}_1+\boldsymbol{C}_2)\}+\boldsymbol{s}^2\boldsymbol{C}_1\boldsymbol{C}_2\boldsymbol{R}\boldsymbol{R}_{eq}\beta_{eq}} \tag{9}$$

But

$$\boldsymbol{i}_{IN}=-\boldsymbol{g}_{md}\boldsymbol{v}_d$$

Thus the amplifier's forward-path transfer function is given by

$$\boldsymbol{a}(\boldsymbol{s}) = \frac{\boldsymbol{v_{out}}}{\boldsymbol{v_d}}(\boldsymbol{s}) \approx \boldsymbol{g_{md}}\beta_{\boldsymbol{eq}}\boldsymbol{R_{eq}} \cdot \frac{\{1 + \boldsymbol{sR}(\boldsymbol{C_1} + \boldsymbol{C_2})\}}{1 + \boldsymbol{s}\{\boldsymbol{C_2R_{eq}} + \boldsymbol{R}(\boldsymbol{C_1} + \boldsymbol{C_2})\} + \boldsymbol{s^2C_1C_2RR_{eq}}\beta_{\boldsymbol{eq}}} \tag{10}$$

Equation (10) takes the form of the generic second-order transfer function

$$\boldsymbol{a}(\boldsymbol{s}) = \boldsymbol{K} \cdot \frac{(1 + \boldsymbol{s}\tau_0)}{1 + 2\zeta_0\left(\frac{\boldsymbol{s}}{\omega_0}\right) + \left(\frac{\boldsymbol{s}}{\omega_0}\right)^2} \tag{11}$$

Where $\boldsymbol{K}$ is the forward-path gain at DC, ω_0 denotes the system's undamped natural frequency and ζ_0 its damping ratio. By inspection

$$\boldsymbol{K} = \boldsymbol{g_{md}}\beta_{\boldsymbol{eq}}\boldsymbol{R_{eq}} \tag{12}$$

$$\tau_0 = \boldsymbol{R}(\boldsymbol{C_1} + \boldsymbol{C_2}) \tag{13}$$

$$\omega_0 \approx \frac{1}{\sqrt{\boldsymbol{C_1C_2RR_{eq}}\beta_{\boldsymbol{eq}}}} \tag{14}$$

and

$$\zeta_0 \approx \frac{\{\boldsymbol{C_2R_{eq}} + \boldsymbol{R}(\boldsymbol{C_1} + \boldsymbol{C_2})\}}{2\sqrt{\boldsymbol{C_1C_2RR_{eq}}\beta_{\boldsymbol{eq}}}} \tag{15}$$

or

$$\zeta_0 = \frac{\omega_0}{2} \cdot (\boldsymbol{C_2R_{eq}} + \tau_0) \tag{16}$$

The zero restoring the mandatory single-pole roll-off is located at

$$\omega_Z = \frac{1}{\tau_0} = \frac{1}{\boldsymbol{R}(\boldsymbol{C_1} + \boldsymbol{C_2})} \tag{17}$$

The frequency of the zero must be significantly lower than the projected unity-gain bandwidth $\boldsymbol{f_U}$ if residual phase shift introduced by the initial double pole roll-off is to be negligible. Conservative component choice here places the zero nearly forty times lower than unity-gain frequency.

Assuming $\mathbf{R}$, $\mathbf{C_1}$ and $\mathbf{C_2}$ are constants established by these considerations, then it's clear from **equations (14)** and **(15)** that ω_0 and ζ_0 can only increase with decreasing TIS gain. Typically, for the compound TIS of **figure 3**, $0 < \zeta_0 < 1$, which gives an under-damped forward path magnitude response with pronounced peaking at the natural frequency. This is due to the predominant value of $\beta_{\boldsymbol{eq}}$ relative to $\boldsymbol{R_{eq}}$.

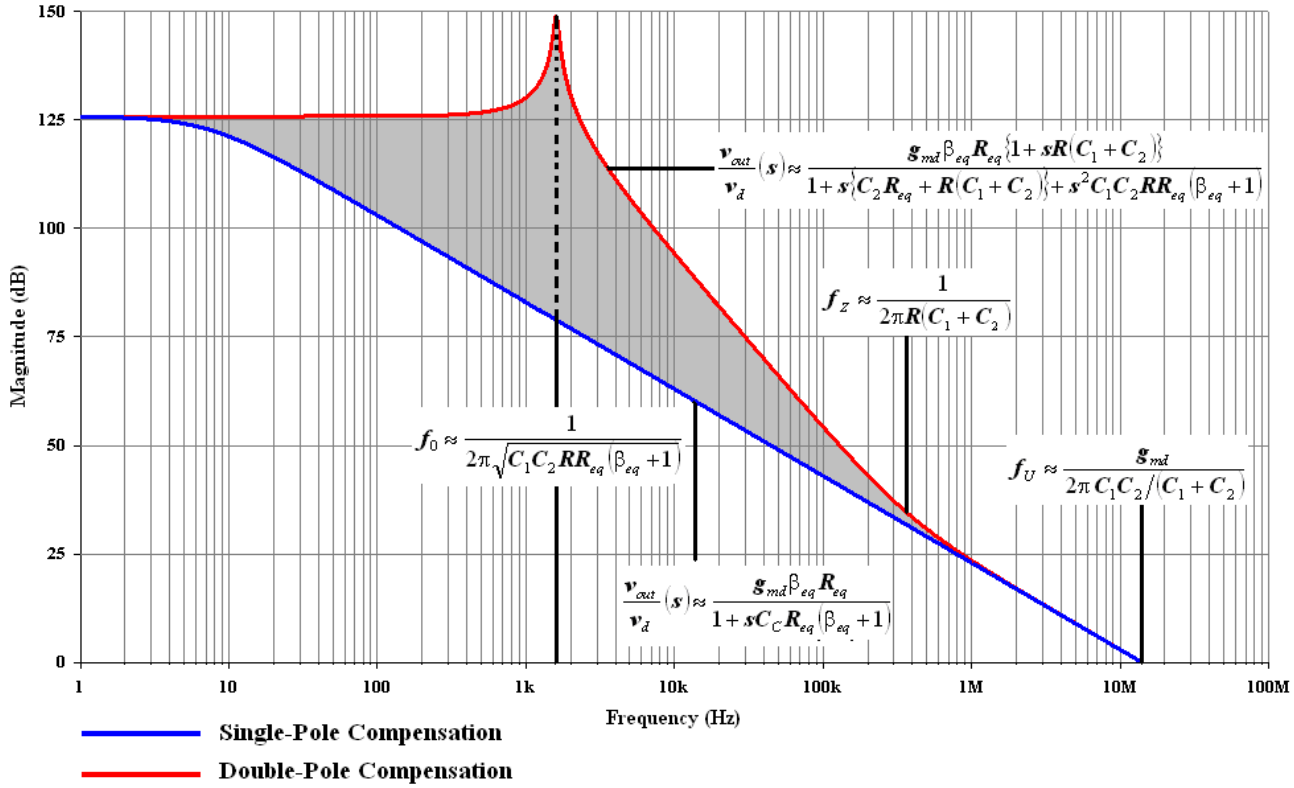


Figure 5. The double-pole characteristic gives a significant improvement in forward-path gain across the audio-band relative to that obtained from the single pole arrangement for the same unity-gain frequency.

The resonant peak has no significant effect on the system's closed loop response, but may be eliminated by increasing ζ_0 which requires an increase in R_{eq} at the substantial expense of β_{eq} (**equation 15**). In practice this may be achieved, as will later be demonstrated, by merely replacing the current gain-enhanced TIS with a cascode arrangement.

For brevity the approximation $(\beta_{eq}R_{eq} \to \infty)$ may be invoked with respect to the forward path transfer function (**equation 10**):

$$\left.\frac{v_{out}}{v_d}(s)\right|_{\beta_{eq}R_{eq}\to\infty} \approx \frac{g_{md}}{C_1C_2R}\cdot\frac{\{1+sR(C_1+C_2)\}}{s^2} \tag{18}$$

This approximation gives gross error over much of the amplifier's pass band and only applies to frequencies well beyond the dominant conjugate poles (**fig. 6**). Nevertheless, determining the forward path unity-gain frequency f_U is facilitated by the truncated transfer function as it may be further assumed $\{sR(C_1+C_2) >> 1\}$ at frequencies beyond the forward-path zero, so that $\{1+sR(C_1+C_2)\} \approx sR(C_1+C_2)$ and **equation 18** becomes

$$\left|\frac{v_{out}}{v_d}(s)\right|_{\beta_{eq}R_{eq}\to\infty} = 1 \approx \frac{g_{md}(C_1+C_2)}{sC_1C_2}$$

$\Rightarrow$

$$f_U \approx \frac{g_{md}}{2\pi C_1C_2/(C_1+C_2)} \tag{19}$$

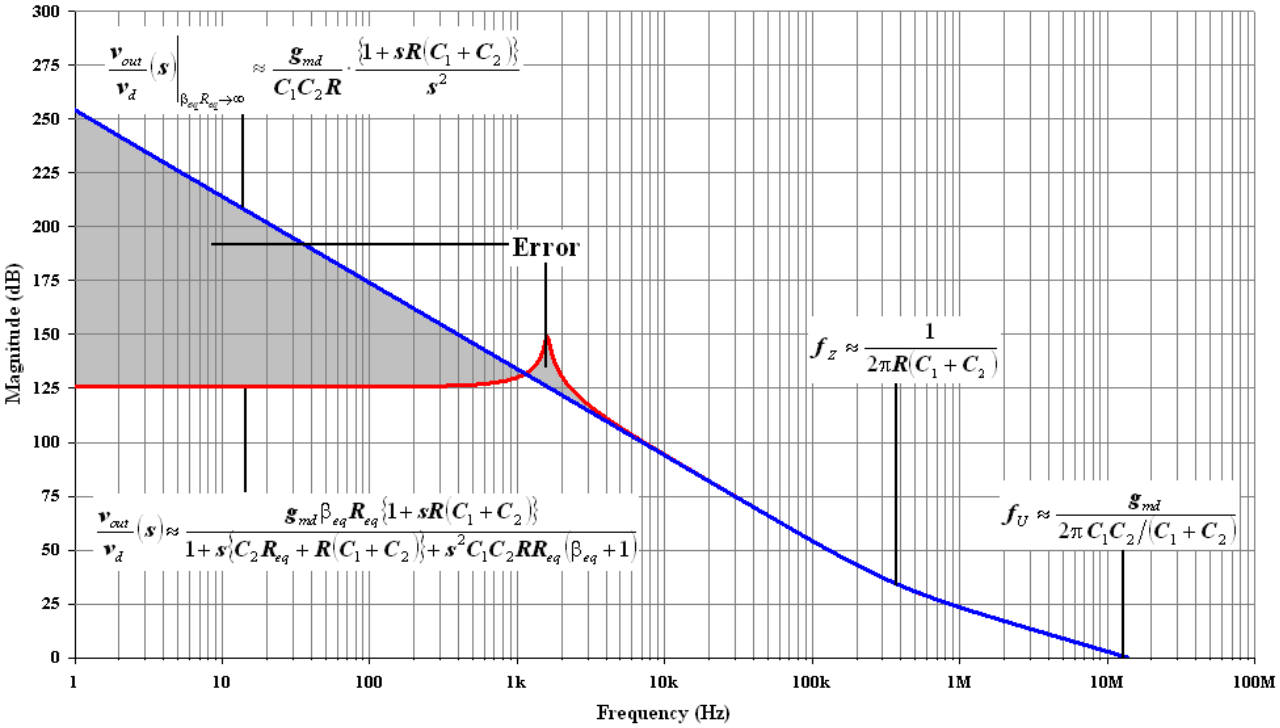


Figure 6. The simplification $(\beta_{eq}R_{eq} \to \infty)$ causes significant error in the forward-path transfer function over much of the audio band.

Thus, if the double-pole network is to yield the same forward path unity-gain frequency as the single-pole capacitor C_C in **figure 1** then, contrary to D. Self's approach [28], the *series* combination of C_1 and C_2 must be equal to C_C:

$$C_1 // C_2 = C_C$$

$$\Rightarrow$$

$$\frac{C_1 C_2}{C_1 + C_2} = C_C \tag{20}$$

Note that the notional condition $(\beta_{eq} R_{eq} \to \infty)$ drives the dominant poles to the origin in the s-plane, which (contrary to Feucht [29]) clearly does not disable the compensator, but merely extends the double pole roll-off to DC (**fig. 6**).

The Double-pole Compensated Major Feedback Loop

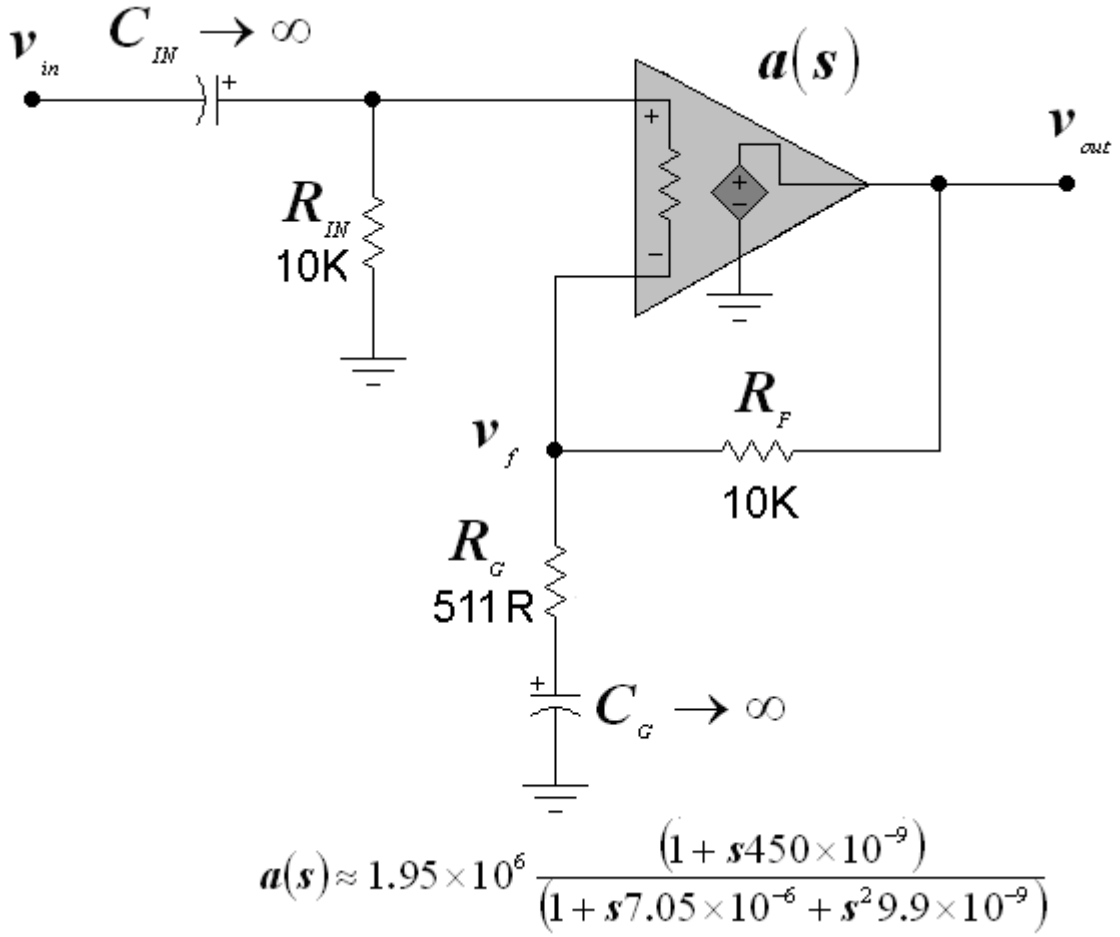


Figure 7. The generic non-inverting (series-shunt feedback) configuration, where a(s) represents the double-pole compensated forward path.

Compared to single-pole compensation, the double-pole arrangement permits the application of at least fifteen times more feedback at the top end of the audio band, which effects a substantial reduction in distortion generated by the output stage[28]. Simultaneously, the attendant reduction in forward-path error (the difference between input and feedback signal) is expressed as an equivalent reduction in the current demand on the TAS, virtually eliminating the later as a source of distortion across the audio band.

At the frequencies of interest $\mathbf{C_{IN}}$ and $\mathbf{C_G}$ (**Fig. 7**) may be considered 'short-circuit', and the loading of the feedback network on the amplifier deemed negligible. Hence

$$v_{out} = a(s)(v_{in} - v_f)$$

$$\Rightarrow$$

$$v_{out} = a(s)v_{in} - \left(\frac{a(s)R_G}{R_F + R_G}\right)v_{out}$$

$$\Rightarrow$$

$$\frac{v_{out}}{v_{in}}(s) = \frac{a(s)}{1 + a(s) \cdot \frac{R_G}{R_G + R_F}} \tag{21}$$

Where loop-transmission or loop-gain $\mathbf{T(s)}$ is given by

$$\boldsymbol{T(s)=a(s)\cdot\frac{R_G}{R_G+R_F}}$$

and return-difference $\lambda(s)$ given by

$$\lambda(s)=1+\boldsymbol{T(s)}$$

$\Leftrightarrow$

$$\lambda(s)=1+\boldsymbol{a(s)\cdot\frac{R_G}{(R_G+R_F)}} \tag{22}$$

Substituting **equation (10)** into **(21)** gives the system's closed-loop transfer function:

$$\frac{\boldsymbol{v_{out}}}{\boldsymbol{v_{in}}}\boldsymbol{(s)}=\frac{\boldsymbol{g_{md}}\beta_{eq}\boldsymbol{R_{eq}(R_G+R_F)}}{\{\boldsymbol{R_F+R_G(1+g_{md}}\beta_{eq}\boldsymbol{R_{eq}})\}}\cdot\frac{\{1+\boldsymbol{sR(C_1+C_2)}\}}{1+\boldsymbol{s}\{\boldsymbol{C_2R_{eq}+R(C_1+C_2)}\}+\boldsymbol{s^2C_1C_2RR_{eq}}\beta_{eq}}\cdot\frac{(\boldsymbol{R_G+R_F})}{\{\boldsymbol{R_F+R_G(1+g_{md}}\beta_{eq}\boldsymbol{R_{eq}})\}}$$

$\Rightarrow$

$$\frac{\boldsymbol{v_{out}}}{\boldsymbol{v_{in}}}\boldsymbol{(s)}=\frac{\boldsymbol{K}}{\lambda}\cdot\frac{\{1+\boldsymbol{sR(C_1+C_2)}\}}{1+\boldsymbol{s}\{\boldsymbol{C_2R_{eq}+R(C_1+C_2)}\}+\boldsymbol{s}^2\frac{\boldsymbol{C_1C_2RR_{eq}}\beta_{eq}}{\lambda}} \tag{23}$$

Where $\boldsymbol{K}$ and λ are the DC forward path gain and return-difference respectively with $\mathbf{C_{IN}}$ and $\mathbf{C_G}$ short-circuited. With $\mathbf{C_{IN}}$ and $\mathbf{C_G}$ *in situ* the ratio $\boldsymbol{K}/\lambda$ tends to unity.

From **equation 12**

$$\boldsymbol{K=g_{md}}\beta_{eq}\boldsymbol{R_{eq}},$$

and

$$\lambda=\frac{\{\boldsymbol{R_F+R_G(1+g_{md}}\beta_{eq}\boldsymbol{R_{eq}})\}}{(\boldsymbol{R_G+R_F})} \tag{24}$$

The closed-loop natural frequency ω_{cl} and damping ratio ζ_{cl} are obtained from a term by term comparison with the normalized second-order transfer function of **equation (11)**:

$$\omega_{cl}=\sqrt{\frac{\lambda}{\beta_{eq}\boldsymbol{R_{eq}RC_1C_2}}} \tag{25}$$

and

$$\zeta_{cl}=\sqrt{\frac{\lambda}{\beta_{eq}\boldsymbol{R_{eq}RC_1C_2}}}\cdot\frac{\{\boldsymbol{C_2R_{eq}+R(C_1+C_2)}\}}{2} \tag{26}$$

or

$$\zeta_{cl} = \frac{\omega_{cl}}{2} \cdot \left(C_2 R_{eq} + \tau_0 \right) \tag{27}$$

The component values in **figure 6** give a closed-loop gain of roughly 26dB at audio frequencies, which is a good compromise between ensuring that adequate feedback is applied at high frequencies without impairing stability, and providing ample input sensitivity to guarantee full power output from the amplifier with a wide range of upstream line-level equipment.

Unfortunately, however, the unalloyed application of a purely resistive global feedback loop to the system of **figure 4** inevitably results in a gain peak at ultrasonic frequencies (**fig. 8**). This, together with an excessive closed-loop bandwidth (>1Mhz), is undesirable as it exacerbates any latent propensity in the amplifier to slew-overload in the presence of RF interference.

Moreover, because the systems closed-loop response is under-damped, a step-input gives significant overshoot at the output (**fig. 9**). The system also promises potentially poorer settling time[15,pg594] than might be expected from a single-pole Miller compensated system of identical unity-gain bandwidth.

This is because the forward-path zero (which remains unaltered in the closed-loop transfer function) and the dominant closed-loop complex poles are in close proximity, and thus constitute a pole-zero doublet with the potential to compromise settling time[30].

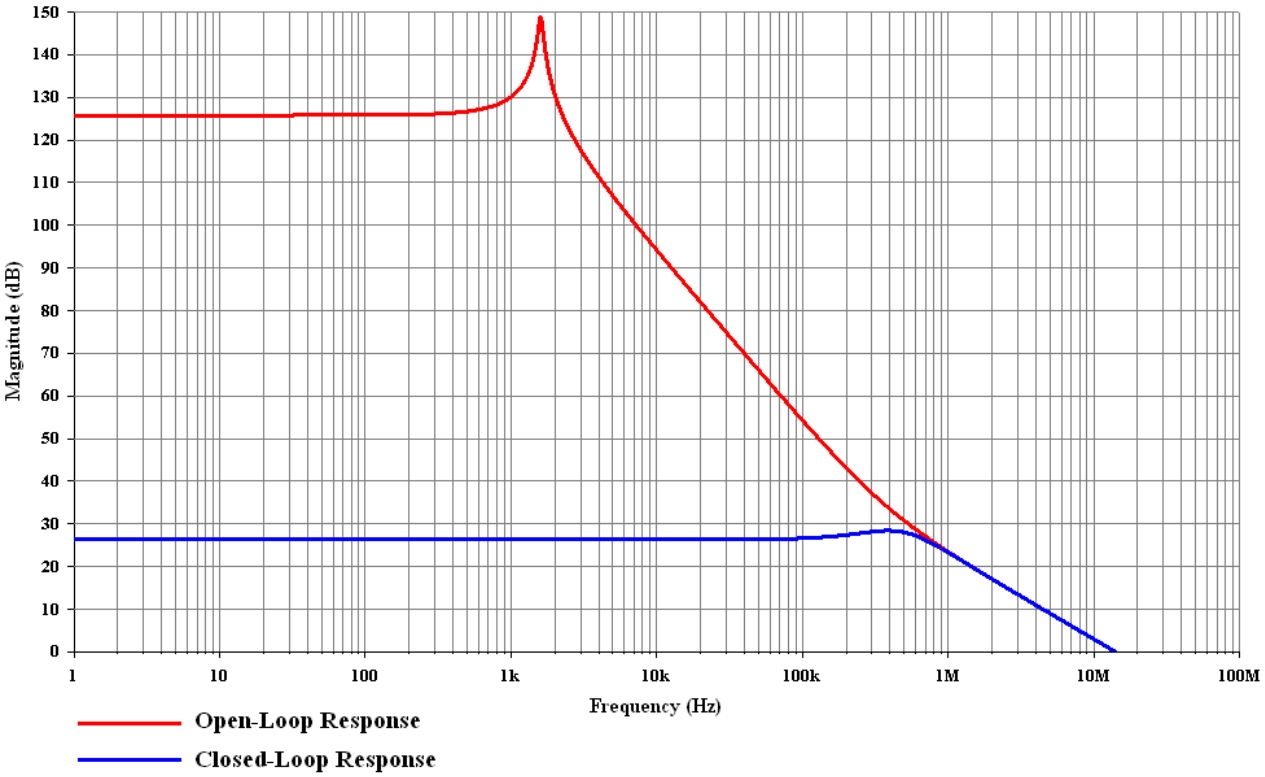


Figure 8. The residual double-pole roll-off in the forward-path's frequency response causes an undesirable peak in the closed loop response.

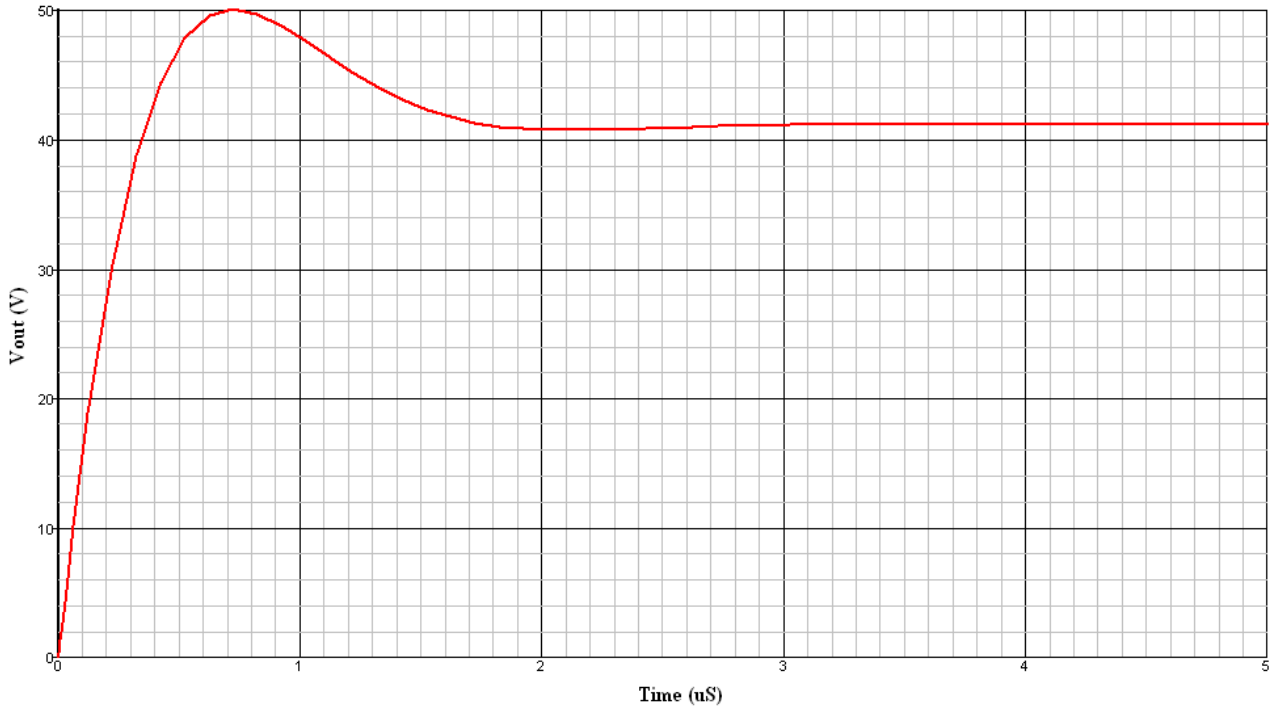


Figure 9. As the systems closed-loop response is under-damped, a step-input gives significant overshoot at the output.

However, Schlarmann et al[31] appear to demonstrate that a complex-pole/zero doublet (as opposed to one constituted solely of real singularities) only effects a significant deterioration in settling time if the zero is located closer to the origin of the s-plane than the pair of complex poles (*viz.* zero/complex-pole doublet).

In any case, contrary to D. Self[8], inordinate preoccupation with settling time in audio power amplifiers, particularly those with an output inductor, is unwarranted as this is unlikely to be of great significance in relation to the large voltage swings involved. This is because normal ringing due to the inductor interacting with the capacitive component in most loudspeaker systems will swamp the effect of the doublet. In audio frequency applications, rapid settling to high accuracy need only be of concern in low power upstream circuitry in general and, specifically, the analogue sections of digital-analogue or analogue-digital conversion systems.

Incidentally, the use of triple gain-stage feed-forward/nested-Miller compensated operational amplifiers in this context (e.g. **NE5532/3/4** or its design antecedent **LM118**) is rather dubious, as the capacitive feedforward path about the second stage cannot guarantee exact cancellation of the second stage pole[32]. Thus, an inevitable forward-path pole-zero (or, indeed, zero-pole) doublet is generated, which gives rise to an often undesirable slow-settling component in the closed-loop transient response.

For the few low-voltage audio frequency applications where post-transient fast and accurate settling is a pressing issue, single or double stage low-distortion designs, such as Analog Devices' **AD797** or Texas Instruments' **OPA627/637**, are often used.

Determining Loop Transmission in SPICE

While much may undoubtedly be gleaned from the forward-path transfer function, of far greater relevance in respect of stability is the system's loop gain or loop transmission with frequency. An amplifier's loop gain may, in principal, be ascertained by first grounding its input (*viz*. setting all independent sources to zero) and disconnecting the feedback loop at an optimal voltage-transfer interface defined by a large (ideally infinite) ratio of test input to loop return impedance.

Changes in loading at the disjuncture may then be deemed negligible, and the feedback loop at this point considered an ideal voltage controlled voltage source (VCVS). The modulus of loop transmission is then merely the ratio of the signal $v_{ret.}$ returned by the loop to the low impedance end of the interface to that applied at the high impedance node by a ground-referenced test voltage $v_{test.}$.

Because the feedback network represents a virtual 'open-circuit' load to the customary voltage follower output stage, the optimal insertion point for the test voltage source may be thought to reside directly between the output stage and the feedback network. This node is unsatisfactory, as the former possesses an appreciable output impedance which, in conjunction with changes in load impedance, compromises accuracy.

In this application, therefore, given a feedback network of relatively low Thevenin impedance, and a degenerated TAS, the optimal voltage-transfer interface is located at the amplifier's inverting input (**fig. 10**) where external loads (if present) have negligible effect on accuracy.

At the frequencies of interest, $\mathbf{C_{IN}}$ and $\mathbf{C_G}$ may be considered 'short-circuit', and the loading of the feedback network on the amplifier's voltage-follower output stage deemed negligible. Loop transmission $\mathbf{T(s)}$, which must be positive for negative feedback (**equation 21)**, is then merely the product of the gains in the forward and feedback paths:

$$T(s) = G(s)\frac{Z_{in}}{Z_{in} + Z_{ret.}} \tag{28}$$

Where

$$G(s) = a(s)\frac{R_G}{R_G + R_F} \tag{29}$$

Note that $\mathbf{a(s)}$ is given by equation (10) and

$$Z_{ret.} = (R_G \,//\, R_F) = \frac{R_G R_F}{R_G + R_F} \tag{30}$$

While the measured voltage return ratio $\rho_v\mathbf{(s)}$ is given by (**fig. 10c**)

$$\rho_v(s) = \frac{v_{ret.}}{v_{test}}$$

Where

$$\boldsymbol{v}_{ret.} = -\boldsymbol{G}(\boldsymbol{s}).\boldsymbol{v}_{test}$$

$$\Rightarrow$$

$$\rho_v(\boldsymbol{s}) = -\boldsymbol{G}(\boldsymbol{s}) \tag{31}$$

Expressing $\rho_v(\mathbf{s})$ in terms of the actual loop gain $\mathbf{T(s)}$ in **equation (28)** gives

$$\rho_v(\boldsymbol{s}) = -\boldsymbol{T}(\boldsymbol{s})\left(1+\frac{\boldsymbol{Z}_{ret.}}{\boldsymbol{Z}_{in}}\right) \tag{32}$$

and

$$\boldsymbol{T}(\boldsymbol{s}) = -\rho_v(\boldsymbol{s})\left(\frac{1}{1+\frac{\boldsymbol{Z}_{ret.}}{\boldsymbol{Z}_{in}}}\right) \tag{33}$$

Thus, if $\boldsymbol{Z}_{in} >> \boldsymbol{Z}_{ret.}$ so that $(\boldsymbol{Z}_{ret.}/\boldsymbol{Z}_{in}) \to 0$, then

$$|\rho_v(\boldsymbol{s})| \to |-\boldsymbol{T}(\boldsymbol{s})|$$

Clearly, since global negative feedback is applied to the amplifier's inverting input, the return ratio's phase response tends to $180^{\mathbf{o}}$ at infrasonic frequencies; therefore, $\mathbf{T(s)}$ is obtained by merely phase-inverting $\rho_v(\boldsymbol{s})$.

This approach is only useful in simulation where the amplifier's DC input offset voltage $\mathbf{V_{os}}$ (measured at the amplifier's inverting input with the feedback loop intact) may be easily and precisely compensated for by connecting a DC voltage source, equal to the DC offset, in series with the grounded AC test source (**fig. 10a**).

With a prototype on the other hand, and in the exceedingly unlikely event that the output doesn't saturate on input noise alone, the DC source would have to consistently maintain its precision to improbable tolerances of the order of 50nV; otherwise the DC error would resolutely drive the amplifier's output to one or other of the supply rails (**appendix B**).

Alternatively, the return ratio ρ_v may be obtained in SPICE by connecting a very large inductor $(\mathbf{L_{oc}} \approx 1\mathbf{GH})$ in series with the loop at the optimal voltage-transfer interface (**fig. 10b**). The inductor $\mathbf{L_{OC}}$ appears 'short-circuit' at DC and 'open-circuit' at test frequencies, while the independent voltage source $\boldsymbol{v}_{test}$ is AC coupled to the amplifier's inverting input by a large capacitance $(\mathbf{C_{CP}} \approx 10\mathbf{KF})$ which preserves the circuit's quiescent conditions.

Note that for the first-order model used here (**fig. 4**), $\mathbf{V_{os}} = 0$ and $(\boldsymbol{Z}_{ret.}/\boldsymbol{Z}_{in}) \to 0$. With the generic circuit of **figure 1**, on the other hand, this approach gives roughly 15% phase error at unity-gain frequency.

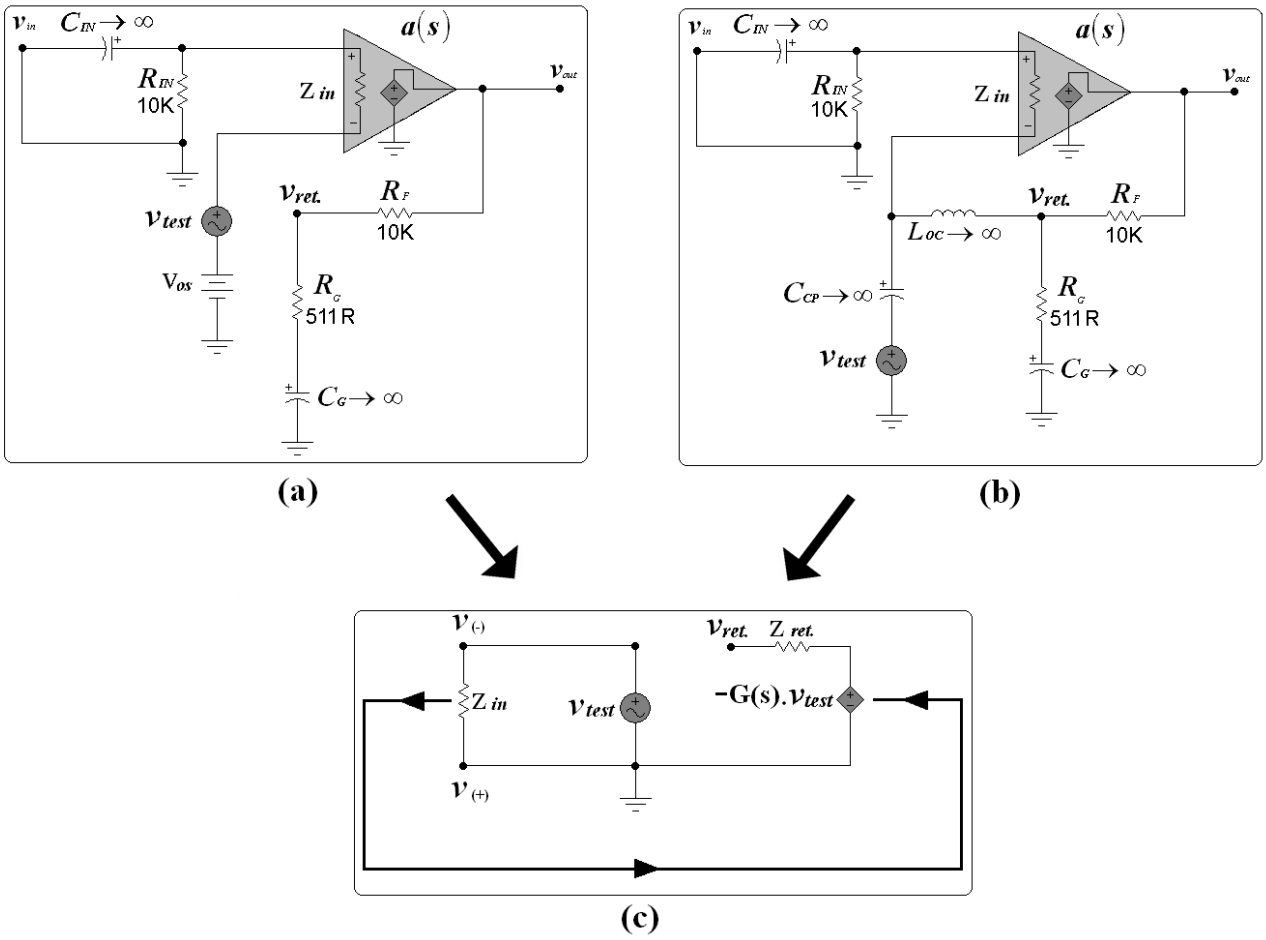


Figure 10. Measuring loop-gain by application of an independent test voltage source at a point where it is assumed $(\mathbf{Z_{ret.}}/\mathbf{Z_{in}}) \to 0$ **.**

For the purist[33], error due to non-ideal impedance ratios at an arbitrary test point may be eliminated by AC-terminating the return end of the loop with the impedance $\mathbf{Z_{in}}$ presented to the test voltage source (**fig. 11a**). Capacitor $\mathbf{C_T}$ ensures that the DC operating point at the return node remains unaffected by $\mathbf{Z_{in}}$. Thus, impedance relationships remain unchanged at the frequencies of interest after the loop is inductively decoupled (**fig. 11b**), and the voltage return ratio $\rho_v\mathbf{(s)}$ is established by inspection:

$$\rho_v(s) = -G(s)\frac{Z_{in}}{Z_{in} + Z_{ret.}} \tag{34}$$

Comparing $\rho_v\mathbf{(s)}$ in **(34)** with the actual loop gain $\mathbf{T(s)}$ in **equation (28)** reveals

$$T(s) = -\rho_v(s) \tag{35}$$

Accuracy with this approach at low frequencies is only limited by the size of decoupling inductor $\mathbf{L_{oc}}$ and coupling capacitor $\mathbf{C_T}$ relative to loop impedances at the test point. This is somewhat academic as in this application only the loop response well beyond audio frequencies is of primary interest.

In any case SPICE and its derivatives usually generate spurious output for very large reactances; in general $\mathbf{L_{oc}}$ and $\mathbf{C_T}$ may not exceed 10GH and 10KF respectively. Moreover, it is often prudent to include a negligibly small resistor (~0R001) in series with $\mathbf{L_{oc}}$ to ensure convergence.

Although frequency domain analysis in SPICE provides the designer with invaluable second-order insight, its results can be misleading. This is because AC analysis computes the circuit's loop-transmission with frequency with respect to an infinitesimal stimulus and at a previously solved and invariant DC operating point. Moreover, all non-linear circuit elements are modelled with linear admittances and transadmittances.

In practice, variation in the circuit's DC parameters with test signal, and the inevitable presence of non-linear components may engender significant error in the system's loop-gain frequency response. For example, the fact that parasitic transistor capacitance (particularly of the reverse biased collector-base junction) varies non-linearly with voltage may present a substantial impediment to stability, but is not accommodated in AC analysis.

Clearly, loop-transmission with frequency may be determined at different operating points by merely applying a suitable corrective DC voltage source in series with the amplifier's DC-coupled input. However, this constitutes only a partial solution since the circuit's non-linear reactances are not exercised.

Higher order verification of loop stability in SPICE may only be obtained in the time domain by examining the transient response of the closed-loop circuit to a fast-edged square wave. For acceptable stability margins, any ringing on the output waveform must be seen to settle in less than four peaks for any anticipated load. Additionally, regardless of the numerical integration method adopted (*viz*. Gear, Trapezoidal, or variations thereof), simulation step size should be at least 100 times smaller than the frequency of the applied test voltage if good accuracy is to be obtained.

The closed-loop circuit may be more rigorously exercised[34] by employing a composite stimulus, consisting of a medium frequency sinusoidal function upon which is superimposed a fast-edged square wave at 10 to 20 times the sinusoid's frequency. In this case simulation step size should be at least 100 times smaller than the frequency of the pulse voltage source.

The sinusoidal generator drives the circuit to rated output while the series pulse voltage source drives the circuit close to clip-overload on negative and positive peaks. The circuit may be deemed to posses adequate margins against instability if any ringing on the output waveform is observed to settle in less than four peaks for any anticipated load.

Ultimately, results from SPICE are only as reliable as the installed device models. *Caveat utilator!*

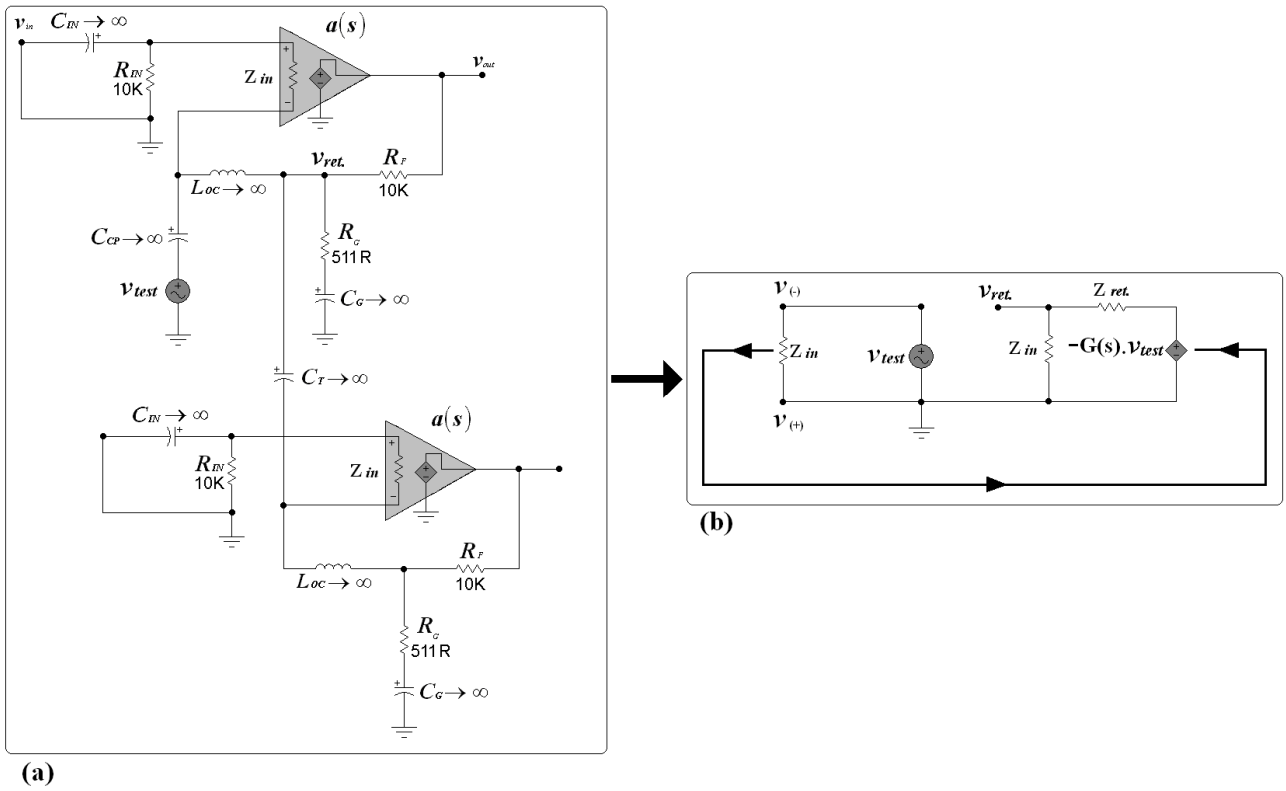


Figure 11. The return end of the AC-decoupled loop is terminated in the impedance Z_{in} that existed at this point before the loop was broken. This is accomplished by AC-coupling the loop to an equivalent point in a copy of the test circuit, and eliminates error due to non-ideal impedance ratios at an arbitrary test point.

The feedback network in **figures 10** and **11** may be deemed purely resistive at the frequencies of interest, with loop transmission singularities identical to those generated by the amplifier's forward path. Comparison between double-pole and the equivalent single-pole loop gain characteristics is facilitated by inserting or removing the double-pole network's resistor **R** as required.

The double-pole network's mandatory forward path zero, which appears unchanged in the loop gain response (**fig. 12**), resides a little more than an octave below unity loop gain frequency. Regrettably, this proximity ensures that residual phase shift from the initial double-pole roll-off degrades phase margin by roughly 25° with respect to the ideal 90° available from the equivalent single-pole response, and is responsible for the small (~11%) mismatch in unity loop gain frequency between the two characteristics (**fig. 13**).

This may at first appear insignificant, as a phase margin of 65° is more than adequate in this application, but this is misleading as, for brevity, the first-order model used here (**equation 10**) assumes stability by excluding non-dominant poles from the transfer function. Moreover, loop-gain phase margin may be further degraded in practice by output stage singularities, particularly if the output stage comprises bipolar power transistors whose unity current gain bandwidth f_T can be as low as 1MHz.

Obviously loop phase margin may be straightforwardly enhanced by merely increasing the value of the resistor in the double-pole network to effect a reduction in the frequency of the forward path zero. This is undesirable, since it is inevitably accompanied by a reduction in loop transmission at the top end of the audio band. Indeed, the circuit ultimately reverts to a single-pole regime as $\mathbf{R} \rightarrow \infty$ in **equation (10)**.

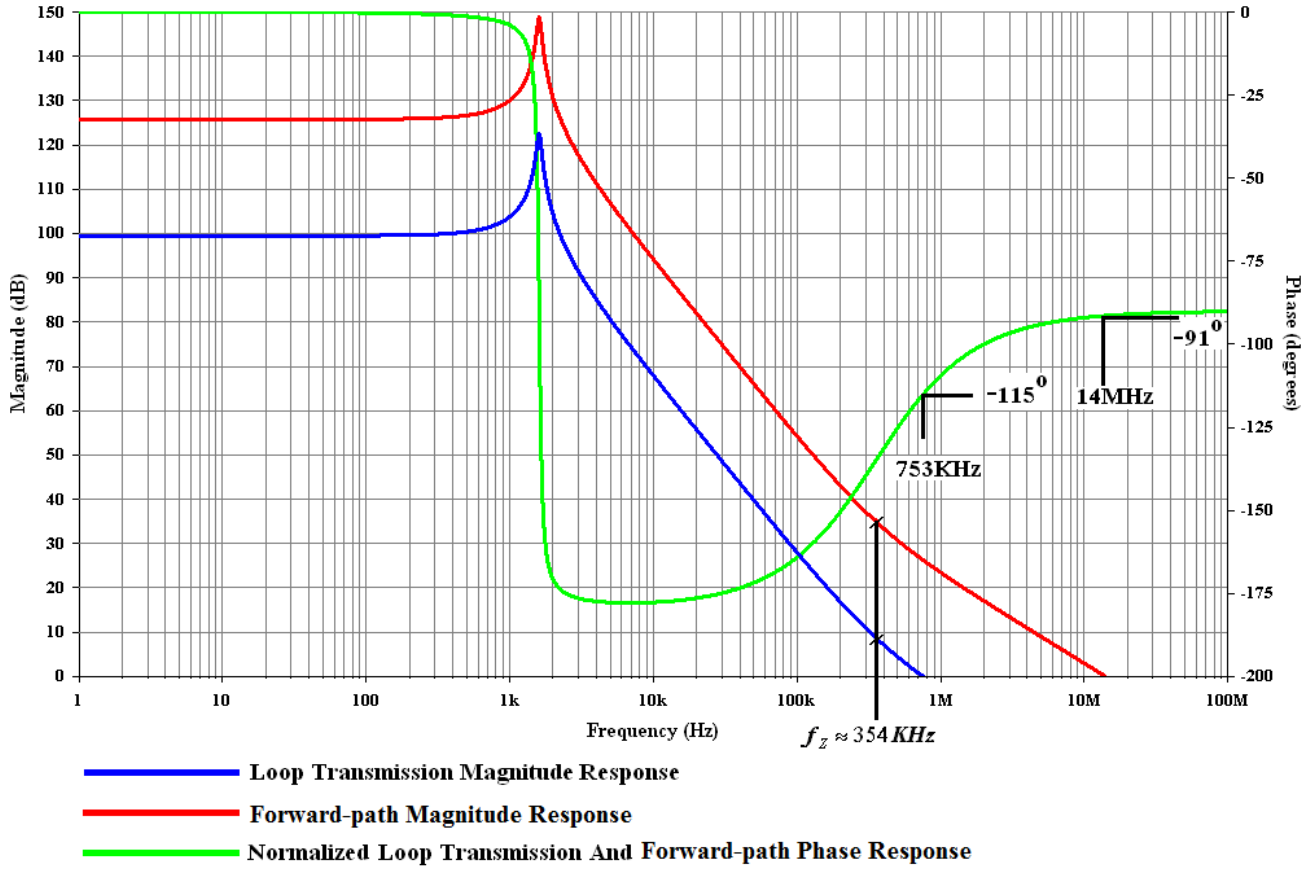


Figure 12. Double-pole loop gain phase margin is compromised by proximity of the forward path zero to unity gain frequency.

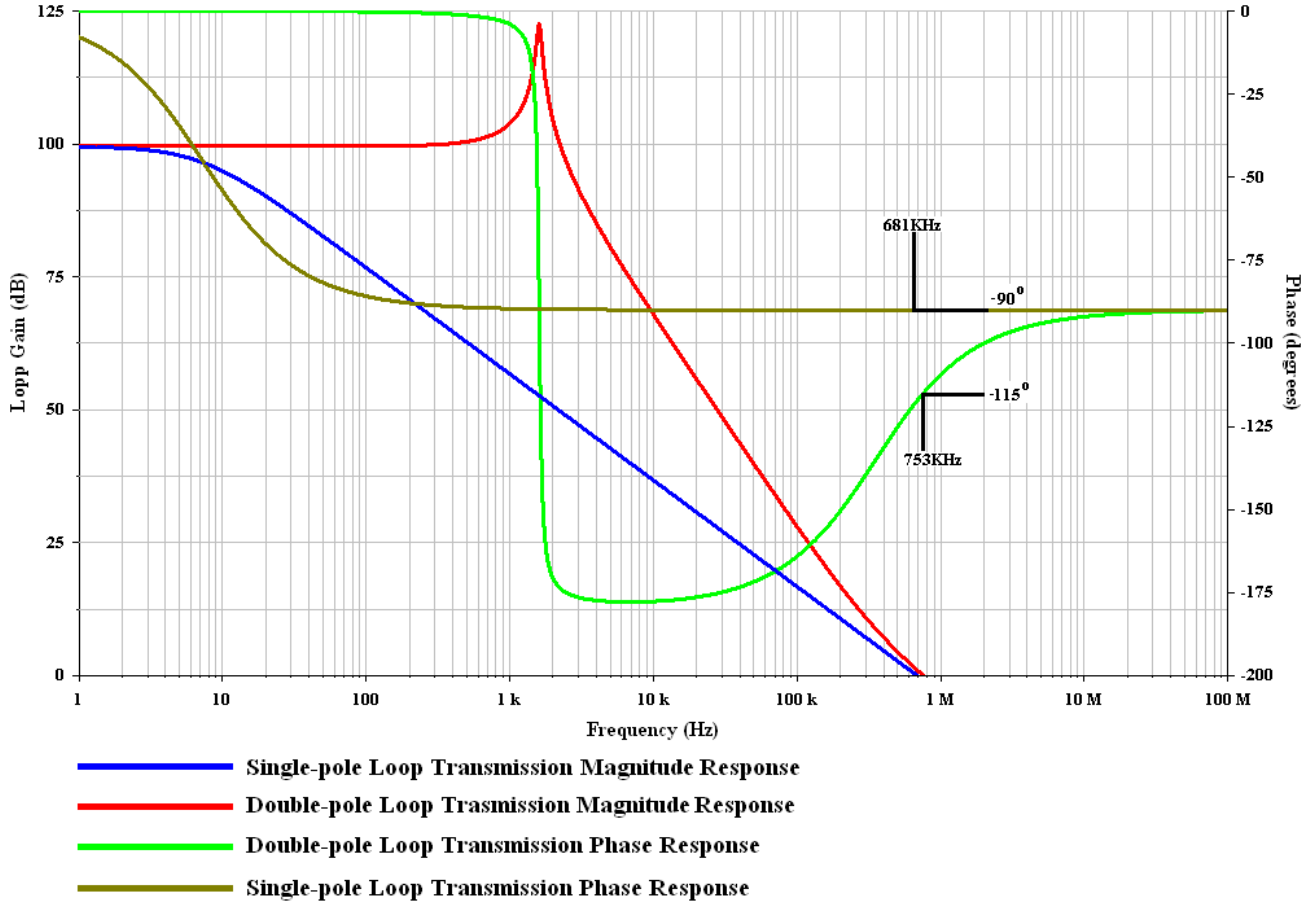


Figure 13. Ideal loop gain frequency response for single and double pole compensation. Closed loop gain (not shown) is roughly 26dB at audio frequencies.

Phase-lead compensation

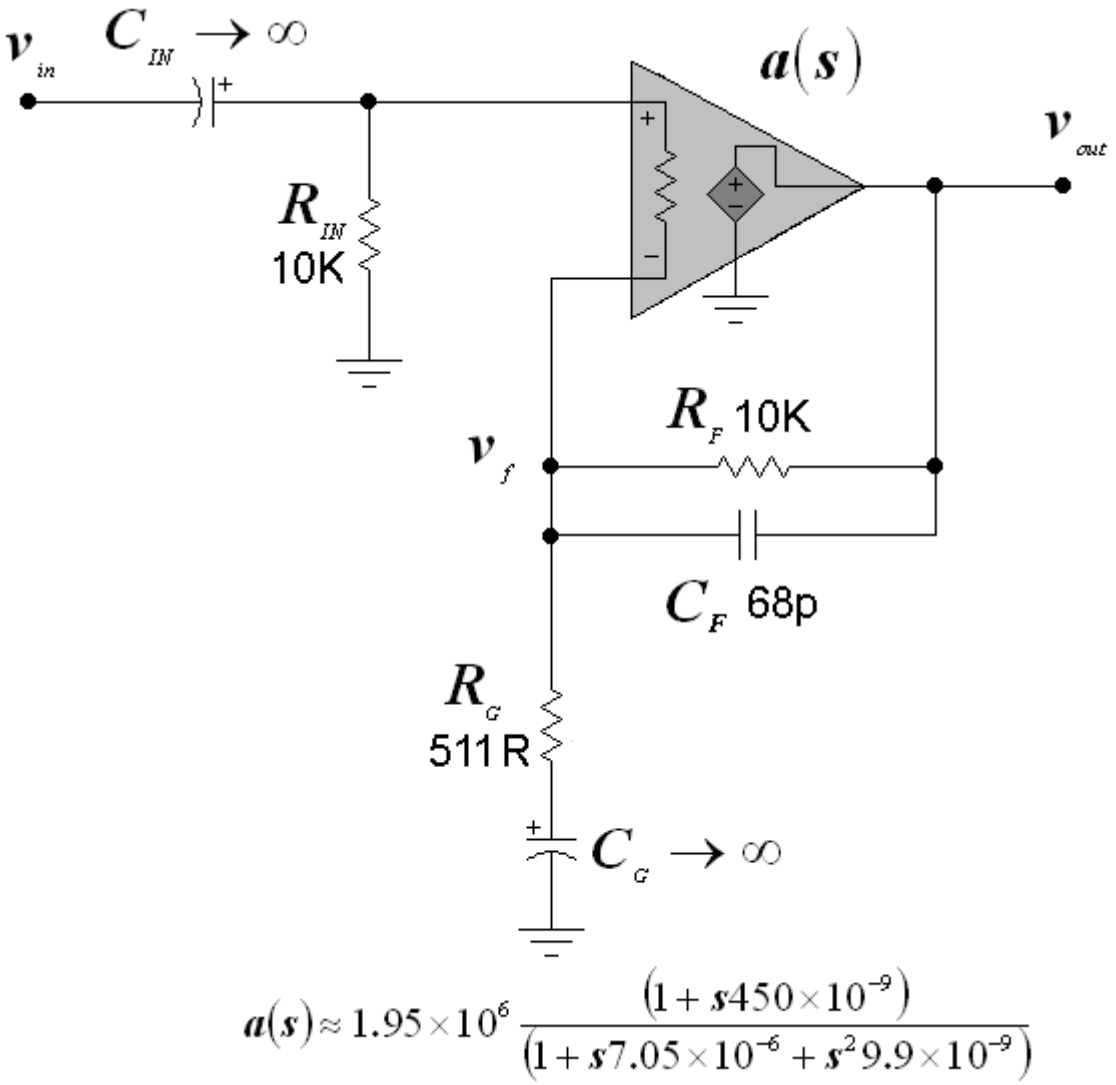


Figure 14. The lead-compensated global feedback loop.

Although **equations 25** and **26** suggest that ω_{cl}, and therefore ζ_{cl}, increase with decreasing closed-loop gain, interfering with the later with a view to ameliorating the residual ultrasonic gain-peak is inelegant, since closed-loop gain is determined by more pressing considerations such as stability, linearity and sensitivity. The ultrasonic peak must therefore be attenuated by sufficiently curtailing closed-loop bandwidth without affecting gain at lower frequencies.

The desired response is obtained by connecting a capacitor $\mathbf{C_F}$ of modest value across feedback resistor $\mathbf{R_F}$ (**fig. 14**); the capacitor incrementally connects the amplifier's inverting input to its output pro rata with frequency which, as intuition suggests, leads to an increase in loop transmission denoted by a zero. This is necessarily accompanied by a reduction in closed-loop bandwidth denoted by a pole at the same frequency as the loop-gain zero (**fig. 15**).

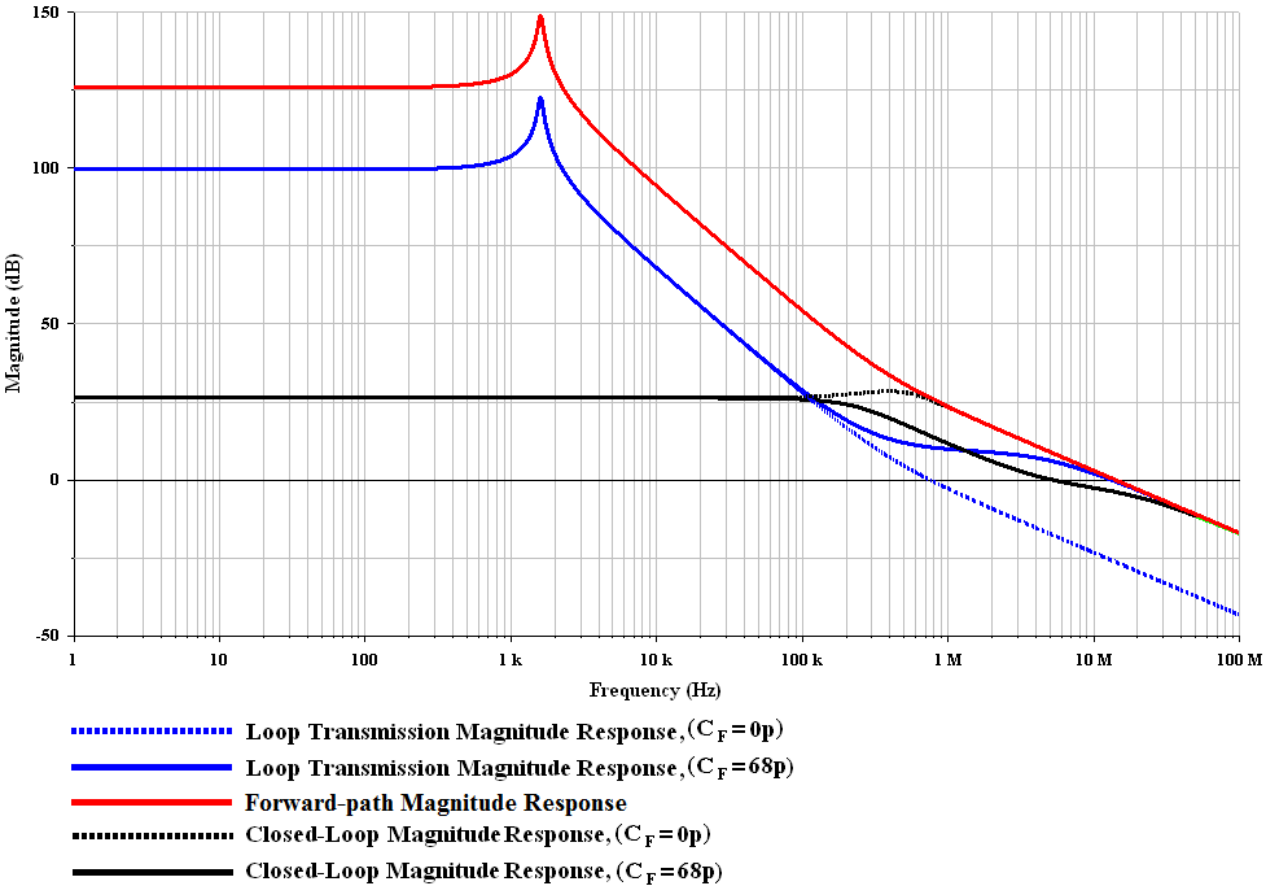


Figure 15. Feedback capacitor C_f eliminates the ultrasonic peak in the closed-loop frequency response by increasing loop transmission at ultrasonic frequencies.

The closed-loop gain is given by

$$\frac{v_{out}}{v_{in}}(s) = \frac{a(s)}{1 + a(s)\dfrac{R_G}{R_G + Z_F}} \tag{36}$$

and loop-transmission $T(s)$ is given by

$$T(s) = a(s) \cdot \frac{R_G}{R_G + Z_F} \tag{37}$$

Where from **equation (10)**

$$a(s) \approx g_{md}\beta_{eq}R_{eq} \cdot \frac{\{1 + sR(C_1 + C_2)\}}{1 + s\{C_2R_{eq} + R(C_1 + C_2)\} + s^2C_1C_2RR_{eq}\beta_{eq}}$$

and

$$Z_F = \frac{R_F}{sC_FR_F + 1} \tag{38}$$

Substituting **equation (38)** into **(36)** for $\mathbf{C_G = 0}$ gives

$$T(s) = a(s) \cdot \frac{R_G}{R_G + R_F} \cdot \frac{(1 + sC_F R_F)}{\left(1 + s\dfrac{C_F R_F R_G}{R_G + R_F}\right)} \tag{39}$$

If $\mathbf{C_G > 0}$ (**fig. 13**), then $\left|(\mathbf{R_G} + 1/\mathbf{sC_G})\right| \to \infty$ at DC, and

$$T(s) = a(s) \cdot \frac{(1 + sC_F R_F)}{\left(1 + s\dfrac{C_F R_F R_G}{R_G + R_F}\right)} \tag{40}$$

Thus, the loop transmission zero eliminates the ultrasonic gain-peak in the closed loop response, while its attendant phase-lead enhances loop phase margin. This makes it unnecessary to reduce the frequency of the forward path zero, or effect a wholesale frequency independent reduction in loop gain to ensure stability.

The loop gain zero is followed by a pole which appears as a zero in the closed loop transfer function; clearly, from **equation (40)**, the respective frequencies of the loop gain singularities are inversely proportional to the value of $\mathbf{C_F}$.

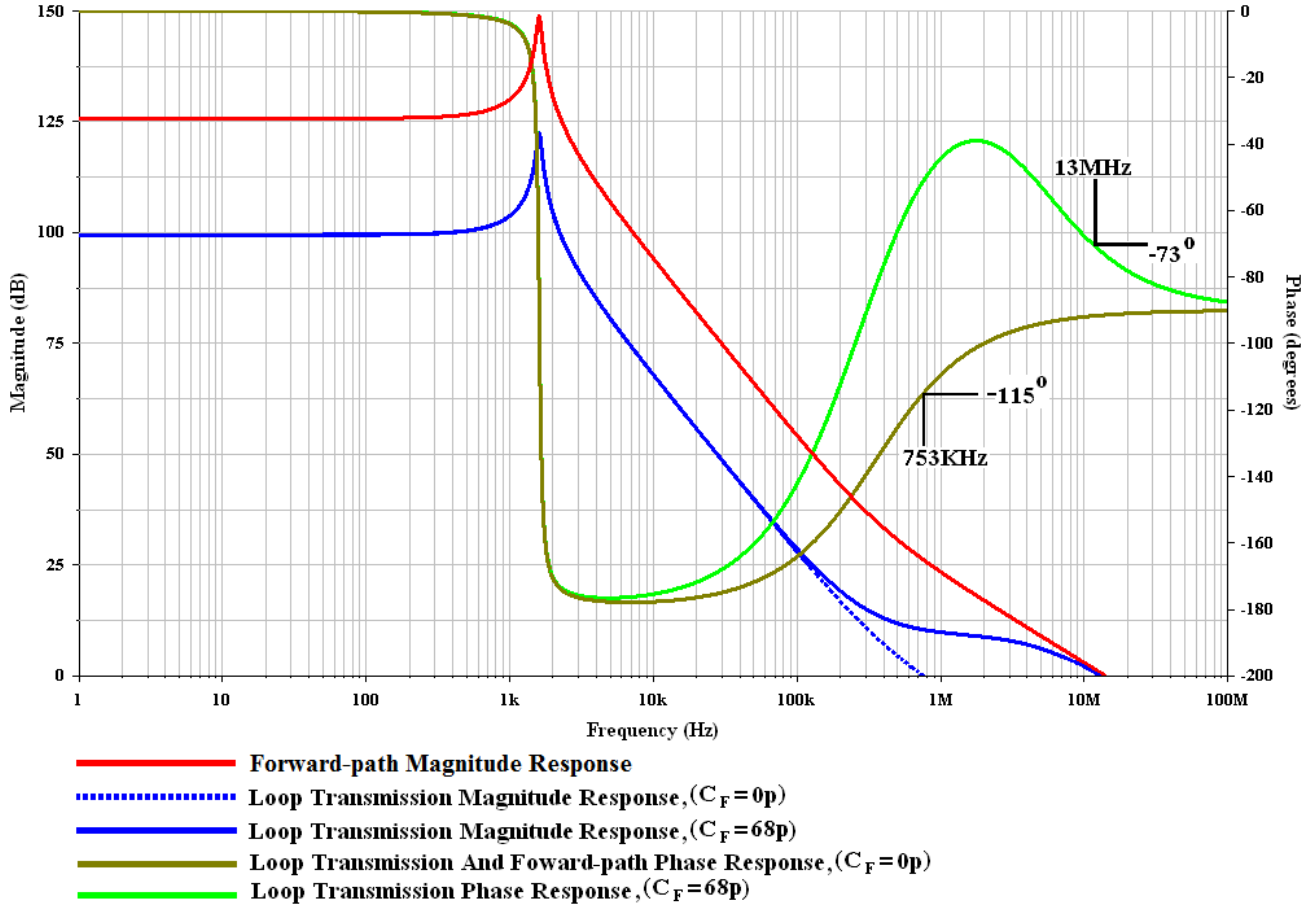


Figure 16. Phase lead compensation increases phase margin by 42^o degrees, to an ostensibly respectable 107^o, but this is now accompanied by an increase in unity loop gain frequency, which is now roughly equal to the forward path unity gain frequency and, together with non-dominant singularities, may again compromise gain margin.

Substituting **equation (10)** and **(38)** into **(36)** gives the closed-loop transfer function:

$$\frac{\boldsymbol{v_{out}}}{\boldsymbol{v_{in}}}(\boldsymbol{s}) = \frac{\boldsymbol{K}}{\lambda} \cdot \frac{\{1+\boldsymbol{s}\boldsymbol{R}(\boldsymbol{C}_1+\boldsymbol{C}_2)\}\left\{\boldsymbol{s}\dfrac{\boldsymbol{C}_F\boldsymbol{R}_F\boldsymbol{R}_G}{(\boldsymbol{R}_G+\boldsymbol{R}_F)}+1\right\}}{\boldsymbol{a}\boldsymbol{s}^3+\boldsymbol{b}\boldsymbol{s}^2+\boldsymbol{c}\boldsymbol{s}+1} \tag{41}$$

Where $\boldsymbol{K}$ and λ are the forward path gain and return-difference respectively at zero frequency, and from **equation (12)**

$$\boldsymbol{K} = \boldsymbol{g}_{md}\beta_{eq}\boldsymbol{R}_{eq},$$

From **equation (20)**

$$\lambda = \frac{\{\boldsymbol{R}_F + \boldsymbol{R}_G(1+\boldsymbol{g}_{md}\beta_{eq}\boldsymbol{R}_{eq})\}}{(\boldsymbol{R}_G+\boldsymbol{R}_F)}$$

The coefficients of the denominator (the characteristic equation) in **equation (41)** are given by

$$\boldsymbol{a} \approx \frac{\beta_{eq}\boldsymbol{R}_{eq}\boldsymbol{R}_F\boldsymbol{R}_G\boldsymbol{C}_F\boldsymbol{R}\boldsymbol{C}_1\boldsymbol{C}_2}{\boldsymbol{R}_F+\boldsymbol{R}_G(1+\boldsymbol{g}_{md}\beta_{eq}\boldsymbol{R}_{eq})} \tag{42}$$

$$\boldsymbol{b} \approx \frac{(\boldsymbol{R}_F+\boldsymbol{R}_G)\beta_{eq}\boldsymbol{R}_{eq}\boldsymbol{R}\boldsymbol{C}_1\boldsymbol{C}_2 + (\boldsymbol{C}_1+\boldsymbol{C}_2)(\boldsymbol{g}_{md}\beta_{eq}\boldsymbol{R}_{eq}\boldsymbol{C}_F\boldsymbol{R}_F\boldsymbol{R}_G\boldsymbol{R}+\boldsymbol{C}_F\boldsymbol{R}_F\boldsymbol{R}_G\boldsymbol{R})}{\boldsymbol{R}_F+\boldsymbol{R}_G(1+\boldsymbol{g}_{md}\beta_{eq}\boldsymbol{R}_{eq})} \tag{43}$$

and

$$\boldsymbol{c} \approx \frac{\boldsymbol{C}_F\boldsymbol{R}_F\boldsymbol{R}_G + \boldsymbol{R}_F\boldsymbol{R}(\boldsymbol{C}_1+\boldsymbol{C}_2) + \boldsymbol{R}_G\boldsymbol{R}(\boldsymbol{C}_1+\boldsymbol{C}_2) + \boldsymbol{g}_{md}\beta_{eq}\boldsymbol{R}_{eq}\boldsymbol{R}_G\boldsymbol{R}_F\boldsymbol{C}_F + \boldsymbol{g}_{md}\beta_{eq}\boldsymbol{R}_{eq}\boldsymbol{R}_G\boldsymbol{R}(\boldsymbol{C}_1+\boldsymbol{C}_2)}{\boldsymbol{R}_F+\boldsymbol{R}_G(1+\boldsymbol{g}_{md}\beta_{eq}\boldsymbol{R}_{eq})} \tag{44}$$

The characteristic equation is a cubic in '$\boldsymbol{s}$', and, therefore, has three roots, one of which must be real. In a stable design the real pole is always located directly after the zero, and denotes the frequency at which the closed-loop magnitude response intersects the forward-path characteristic (**fig. 15**). This pole resides beyond unity-gain frequency, and, as such, its effect on the system's dynamic response is negligible.

The remaining pair of roots are the dominant closed-loop poles, and have the preponderant effect on the systems closed-loop transient and small-signal frequency response. **Equation (41)** may thus be expressed in the generic form:

$$\frac{\boldsymbol{v_{out}}}{\boldsymbol{v_{in}}}(\boldsymbol{s}) = \frac{\boldsymbol{K}}{\lambda} \cdot \frac{(1+\boldsymbol{s}\tau_0)(1+\boldsymbol{s}\tau_z)}{(1+\boldsymbol{s}\tau_{p1})\left\{1+2\zeta_{cl}\left(\dfrac{\boldsymbol{s}}{\omega_{cl}}\right)+\left(\dfrac{\boldsymbol{s}}{\omega_{cl}}\right)^2\right\}} \tag{45}$$

Capacitor $\mathbf{C_F}$ affords comprehensive control over the closed-loop damping ratio ζ_{cl} and hence the dynamic response of the system. As $\mathbf{C_F}$ is increased from zero to just over 100pF, the dominant pole-pair describes one half of an elliptical path about the forward-path zero as its focus (**fig. 17**), ranging from complex (underdamped), to real and equal (critically damped) and finally real and unequal (overdamped).

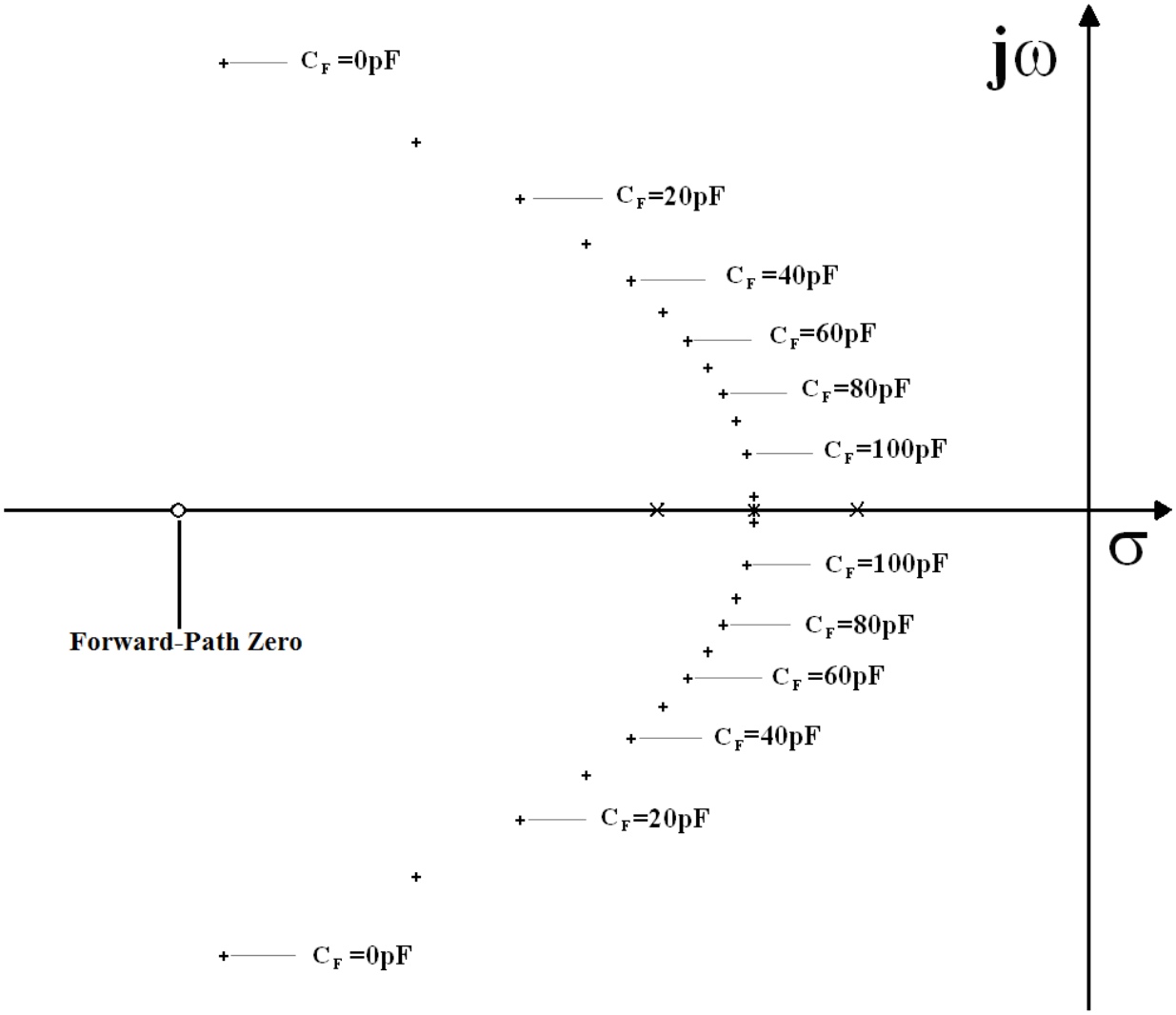


Figure 17. The migration of dominant poles in the closed-loop transfer function (not to scale) as $\mathbf{C_F}$ is increased from 0pF to 110pF; the conjugate poles converge on the real axis when $\mathbf{C_F} > 100\mathbf{pF}$. Non-dominant closed-loop singularities are ignored here in the interest of clarity.

Therefore, it is more useful to express the characteristic equation as the product of three factors depending on the value of $\mathbf{C_F}$. *Viz.*

$$\text{Increasing } \mathbf{C_F} \downarrow$$

$$(\mathbf{s}+\alpha_1)(\mathbf{s}+\delta_1+\mathbf{j}\varphi_1)(\mathbf{s}+\delta_1-\mathbf{j}\varphi_1)=0;(0<\zeta_{\mathbf{cl}}<1) \quad (46)$$

$$(\mathbf{s}+\alpha_2)(\mathbf{s}+\delta_2)(\mathbf{s}+\delta_2)=0;(\zeta_{\mathbf{cl}}=1) \quad (47)$$

$$(\mathbf{s}+\alpha_2)(\mathbf{s}+\delta_2)(\mathbf{s}+\sigma_2)=0;(\zeta_{\mathbf{cl}}>1) \quad (48)$$

In this application the form of **equation (46)** $(0<\zeta_{\mathbf{cl}}<1)$ is satisfactory as it yields a maximally-flat (quasi-Butterworth) closed-loop bandwidth of less than 400KHz (**fig. 18**); this is a good compromise between attenuating the ultrasonic gain-peak, while maintaining an acceptable signal rise-time and reasonably constant group delay across the audio band. Such a response is realised here by selecting $40\mathbf{pF}<\mathbf{C_F}<80\mathbf{pF}$; large values of $\mathbf{C_F}$ cause a reduction in transient overshoot at the cost of increased signal rise-time, and conversely (**fig. 19**).

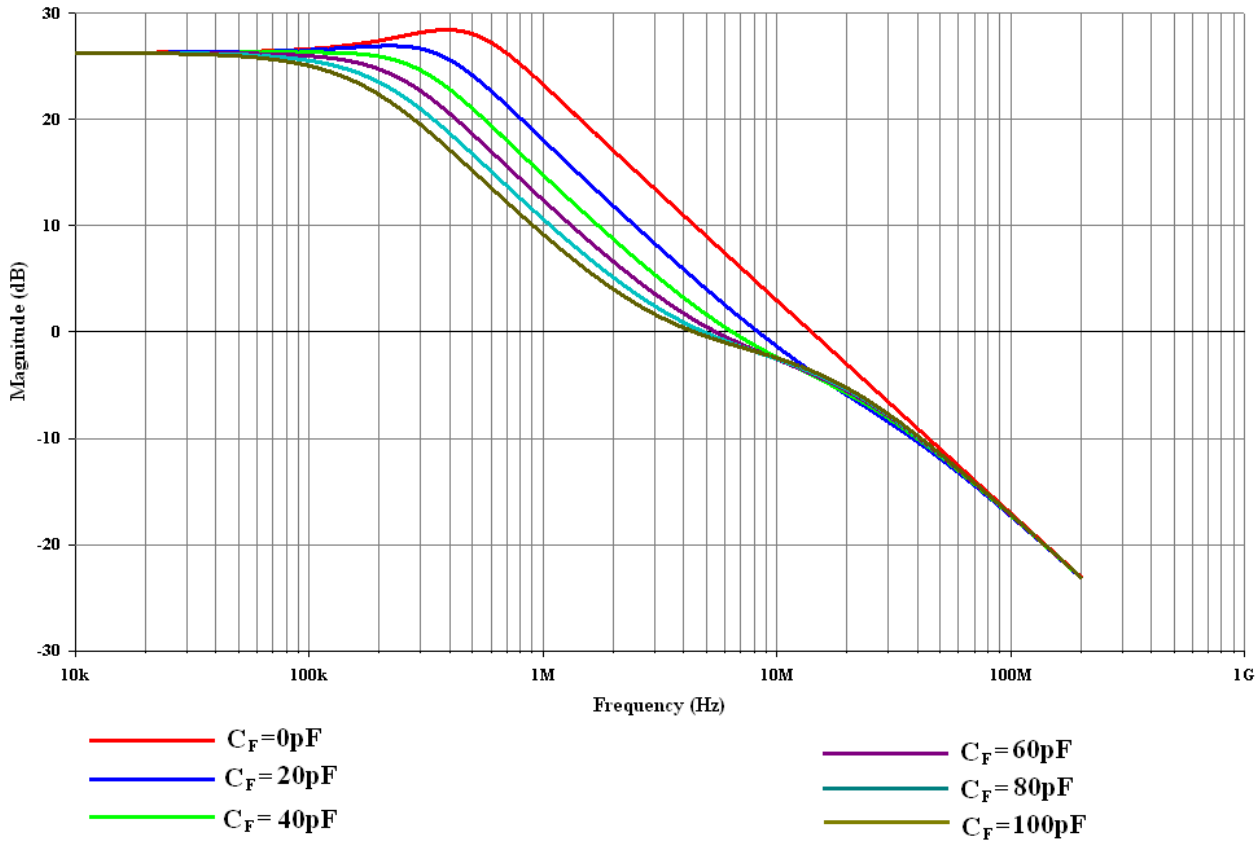


Figure 18. Closed-loop frequency response of the double-pole compensated gain-block for varying $\mathbf{C_F}$.

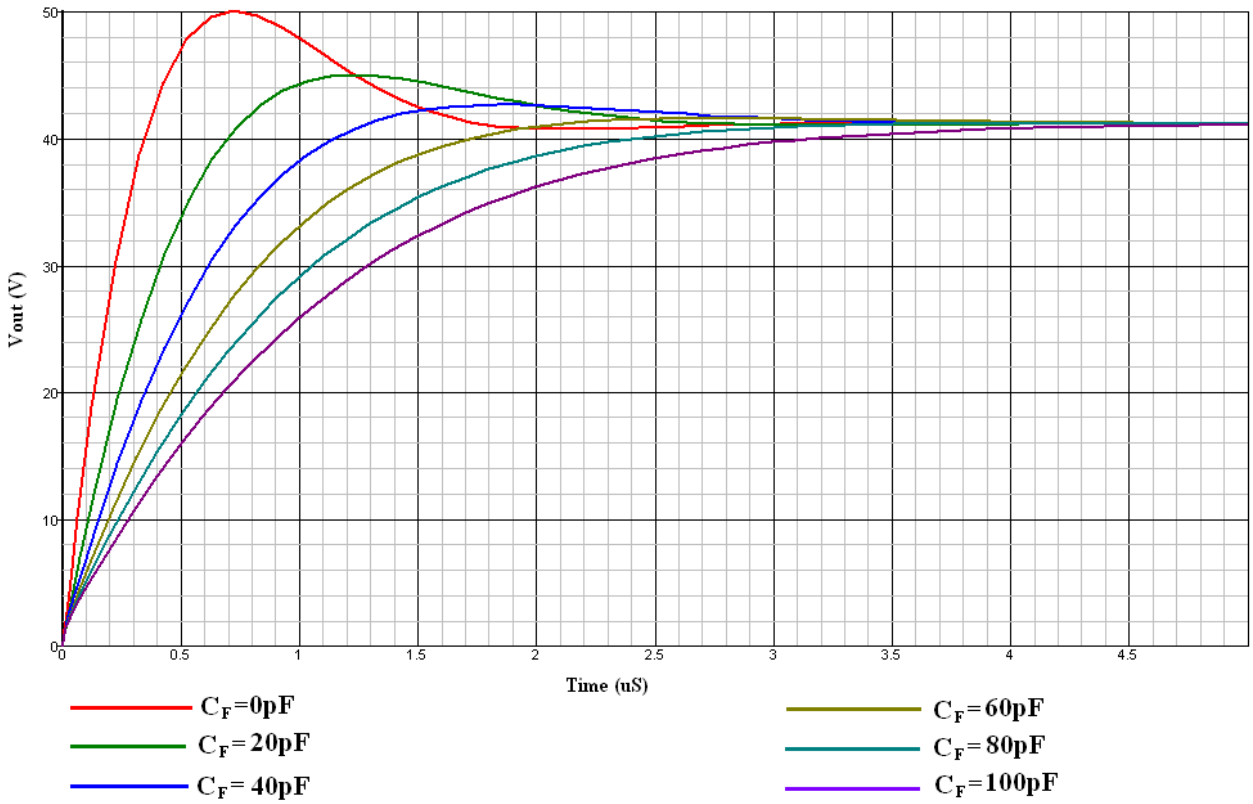


Figure 19. Closed-loop transient response of two-pole compensated gain-block for different values of C_F .

Controlling the Loop-transmission Pole

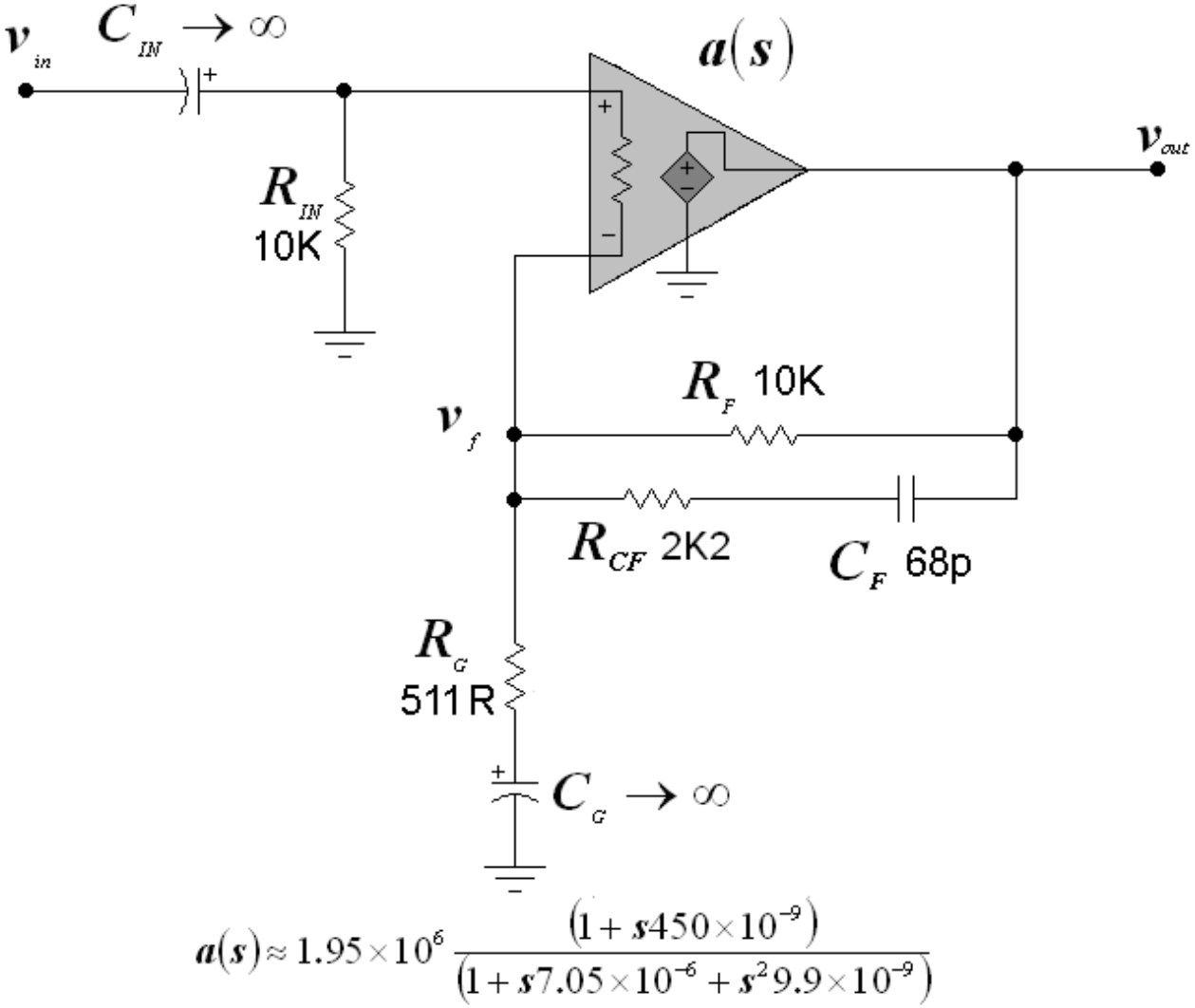


Figure 20. Resistor R_{CF} in series with C_F is included with a view to exerting greater control over location of closed-loop zero, and, in particular, lowering the loop transmission unity-gain frequency.

In respect of loop transmission, the value of C_F in **figure 13** need not exceed 10pF to effectively eliminate the residual excess phase from the initial double-pole roll-off, and ensure a phase margin roughly equal to or greater than the ideal 90^o obtained with single-pole Miller compensation (**fig. 21**). Moreover, the improvement in phase margin is achieved without a significant increase in unity-gain frequency which, in the presence of non-dominant complex singularities, may otherwise erode the system's gain margin.

Unfortunately, selecting $C_F = 10\mathbf{pF}$ gives a closed-loop bandwidth in excess of 700KHz (**fig. 18**) coupled with an inadequately damped transient response (**fig. 19).** Increasing C_F to 68pF eliminates the ultrasonic peak by lowering the frequency of the loop transmission zero (**equation 39**) which reduces closed-loop bandwidth to a satisfactory 244KHz (**fig. 15)**, and simultaneously improves loop phase margin by 42^o (**fig. 16)**.

Increasing C_F, consistent with **equations 39** and **40**, also inevitably reduces the frequency of the loop transmission pole. However, this is not sufficient to prevent an increase in unity loop gain frequency, which is now roughly equal to the forward path unity gain frequency. This is acceptable, as far as stability is concerned, if the forward path's unity-gain frequency resides well below the frequency of the first non-dominant pole.

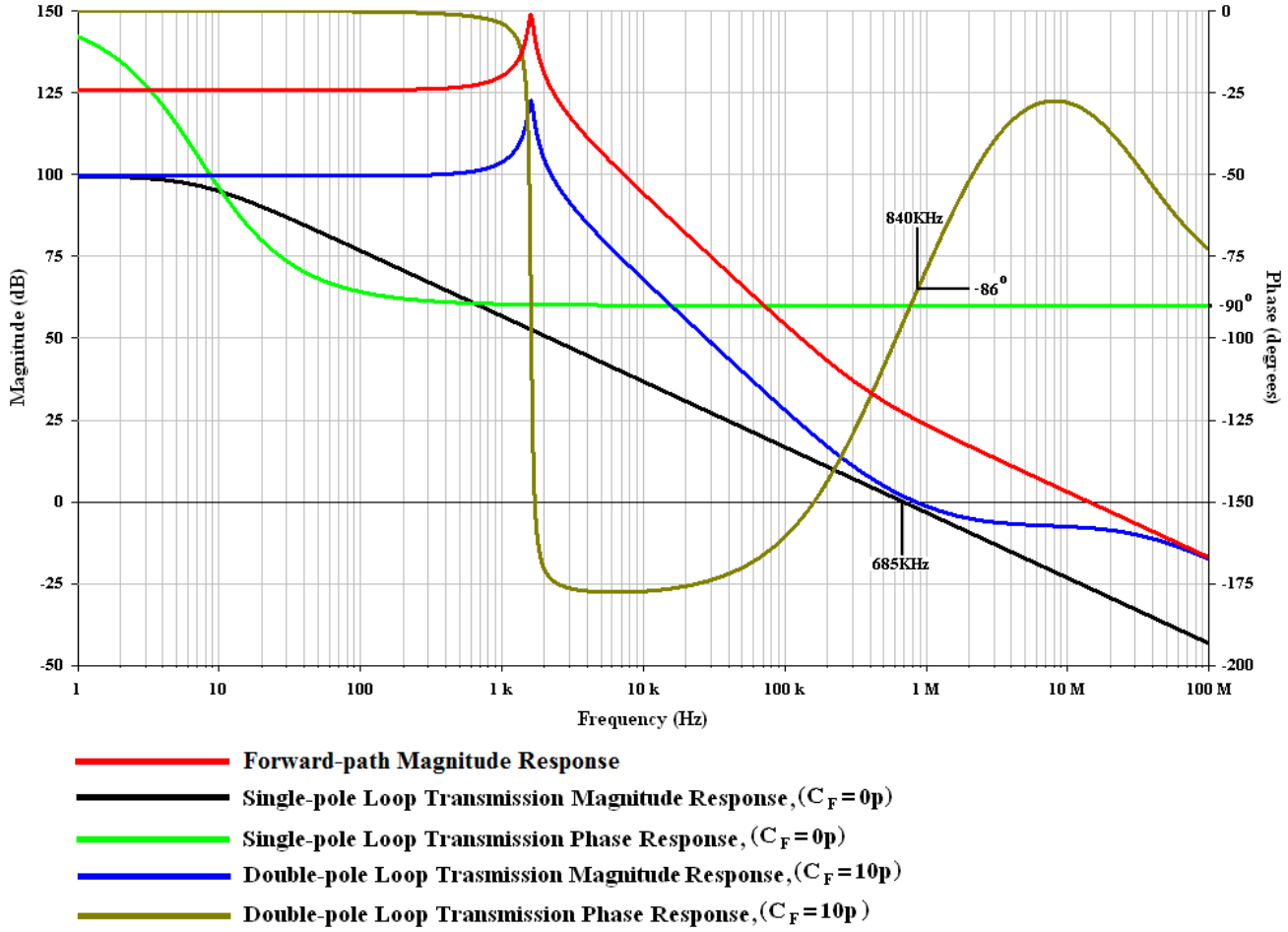


Figure 21. A mere $C_F = 10$pF is sufficient to obviate the residual phase shift from the initial double-pole roll-off, giving a phase margin roughly equal to the notional 90^o phase margin due to single-pole Miller compensation.

However, to maximize loop gain in this application, the forward path's unity-gain frequency is typically situated beyond 10MHz. Residual phase shift due to non-dominant singularities may therefore compromise gain margin, particularly if a low current-gain-bandwidth product bipolar output stage is employed.

Greater control over the location of the loop transmission pole may be exercised by inserting a resistor $\mathbf{R_{CF}}$ in series with $\mathbf{C_F}$ (**fig. 20**). In direct proportion to its value, $\mathbf{R_{CF}}$ lowers the frequency of this pole (**fig. 22**), and therefore provides a secondary means by which the response in the vicinity of the system's unity loop gain frequency may be optimised in the interest of enhanced stability margins.

Since the loop-gain pole appears as a zero in the closed loop transfer function, it follows that $\mathbf{R_{CF}}$ necessarily lowers the frequency of the closed-loop zero introduced by $\mathbf{C_F}$ (**fig. 23**). For practical values the effect of $\mathbf{R_{CF}}$ on the system's dynamic response is negligible.

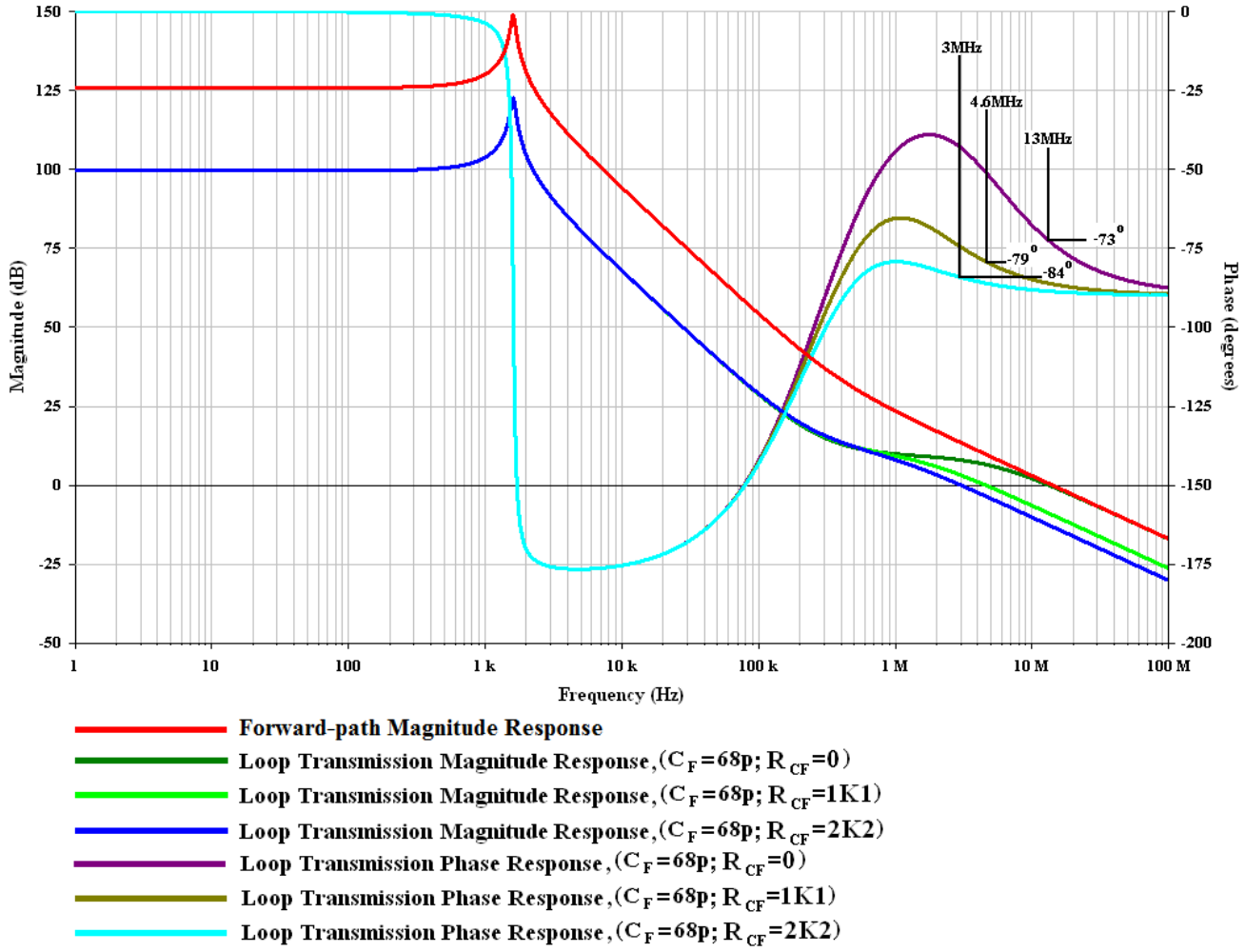


Figure 22. Migration of loop transmission pole for different values of R_{CF}. The later lowers the frequency of the pole, and thus unity-gain crossover without a incurring a significant penalty in respect of phase margin.

From **equation (37)** loop-transmission $T(s)$ is given by

$$T(s) = a(s) \cdot \frac{R_G}{R_G + Z_F}$$

Where

$$Z_F = R_F \cdot \frac{\{sC_F R_{CF} + 1\}}{\{sC_F (R_{CF} + R_F) + 1\}} \tag{49}$$

and, from **equation (10)**,

$$a(s) \approx g_{md} \beta_{eq} R_{eq} \cdot \frac{\{1 + sR(C_1 + C_2)\}}{1 + s\{C_2 R_{eq} + R(C_1 + C_2)\} + s^2 C_1 C_2 R R_{eq} \beta_{eq}}$$

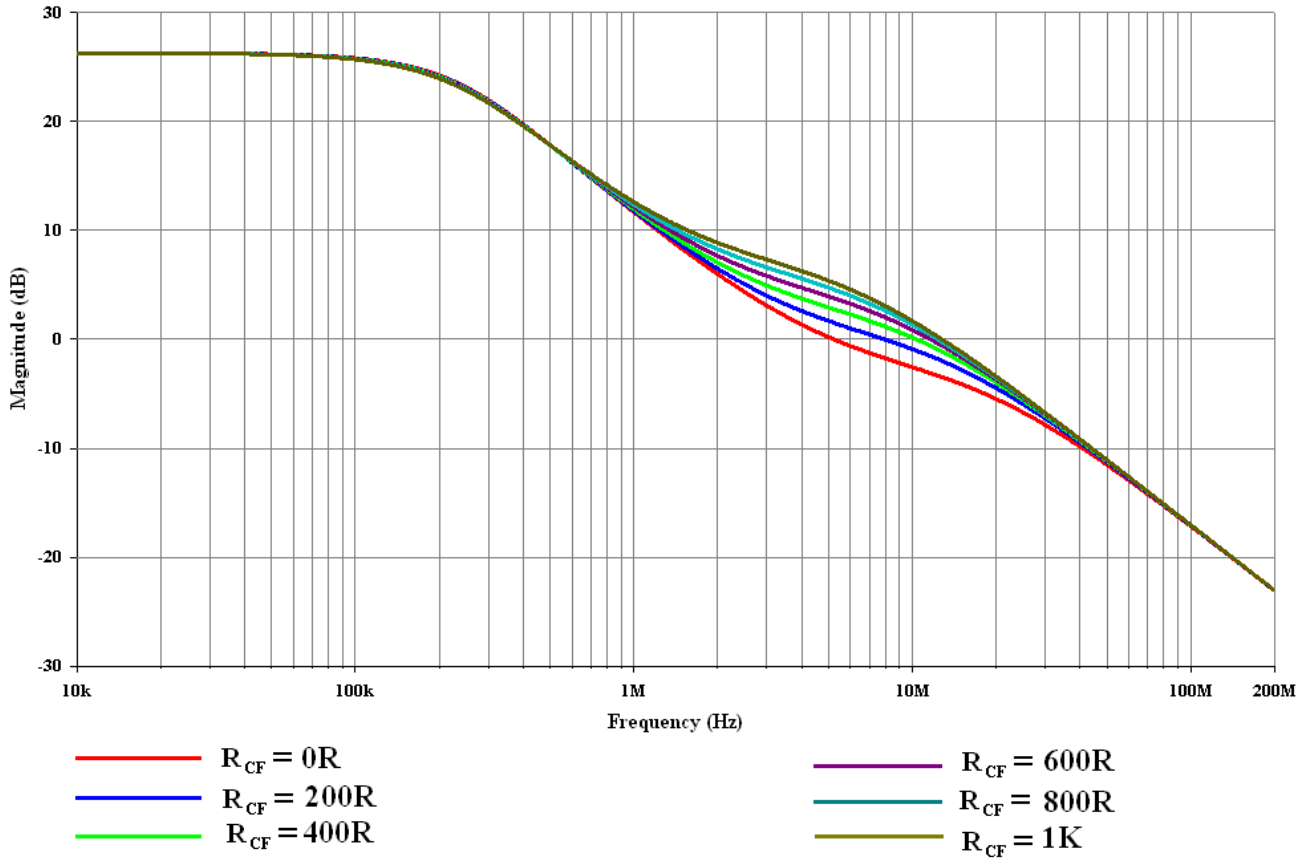


Figure 23. The zero in the closed-loop transfer characteristic migrates to lower frequencies as $\mathbf{R_{CF}}$ is increased. In all cases $\mathbf{C_F} = 68\mathbf{pF}$.

Thus, for $\mathbf{C_G} = 0$

$$\boldsymbol{T(s) = a(s) \cdot \frac{R_G}{R_G + R_F} \cdot \frac{\{sC_F(R_{CF} + R_F) + 1\}}{\left\{sC_F \frac{(R_{CF}R_G + R_F R_G + R_{CF}R_F)}{(R_G + R_F)} + 1\right\}}} \tag{50}$$

If $\mathbf{C_G} > 0$ (**fig. 14**), then $\left|\mathbf{R_G} + 1/\mathbf{sC_G}\right| \to \infty$ at DC, and

$$\boldsymbol{T(s) = a(s) \cdot \frac{\{sC_F(R_{CF} + R_F) + 1\}}{\left\{sC_F \frac{(R_{CF}R_G + R_F R_G + R_{CF}R_F)}{(R_G + R_F)} + 1\right\}}} \tag{51}$$

By comparing **equation (40)** to **equations (50)** and **(51)** it is evident that the factor $\mathbf{R_{CF}}(\mathbf{R_G} + \mathbf{R_F})$ is instrumental in reducing the frequency of the loop transmission pole. For typical values, the effect of $\mathbf{R_{CF}}$ on the loop transmission zero and hence closed-loop half-power frequency is trivial.

Caution is required here as, in practice, output stage singularities and load impedance characteristics, ignored in this first-order analysis, will affect the choice of $\mathbf{C_F}$. Moreover, while curtailing the design's ability to amplify RF spuriae, capacitor $\mathbf{C_F}$ simultaneously introduces a direct short-circuit path for such interference from the output terminals to the input stage, whence it may either drive the forward path into intermittent slew-overload, or be demodulated and returned to the transducer as audio-frequency signal.

An LCR filter is now required (**fig. 24)** to attenuate ultrasonic spuriae acquired by the loudspeaker leads [37,38] before it gets to the first stage by way of $\mathbf{C_F}$ or, indeed, feedback resistor $\mathbf{R_F}$. The reactive components $\mathbf{L_o}$ and $\mathbf{C_o}$ are effectively "short-circuit" and "open-circuit" respectively within the amplifier's pass-band.

The output network also reduces the potential for ultrasonic instability in the amplifier, provoked by capacitive loads, by terminating its output with a nominally constant resistance $\mathbf{R_o}$ at ultrasonic frequencies, where the air-cored inductor $\mathbf{L_o}$ and capacitor $\mathbf{C_o}$ may be considered "open-circuit" and "short-circuit" respectively.

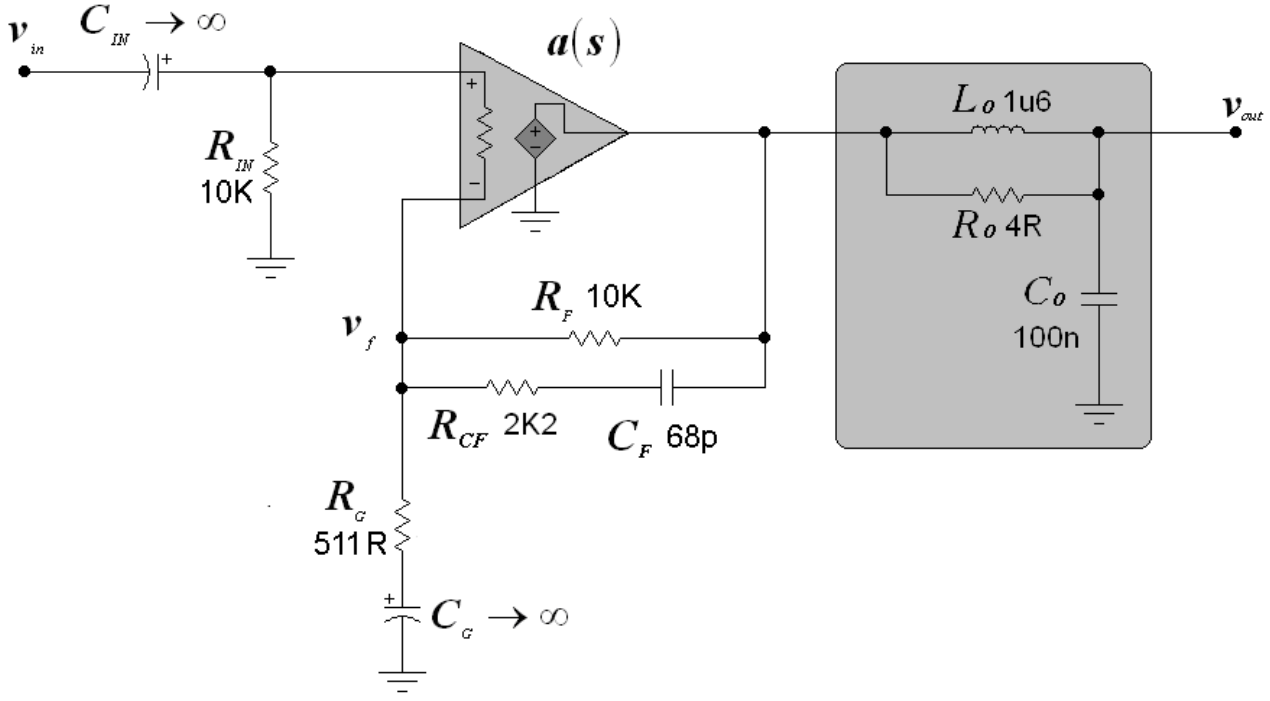


Figure 24. The LCR filter attenuates any RFI on the loudspeaker leads before it's acquired by the input stage.

Slew Rate Issues with Double-pole Compensation

With the TIS's input at virtual ground, due to shunt applied negative feedback, **C1** and **R** are effectively in parallel at the frequencies of interest, and the proportion of **C2** current contributed by **R** decreases substantially beyond the frequency f_z of the forward path zero. Ultimately, at sufficiently high frequencies $(f \geq 10 f_z)$, the resistor may be deemed 'open-circuit' compared to the reactance presented by the parallel combination **(C1+C2)** (**fig. 25**), and virtually all the current demands of **C2** must be met by **C1** alone.

This implies that stimuli at frequencies well beyond the frequency of the zero $(f \geq 10 f_z)$ will provoke a slew response identical to that obtained with single-pole compensation (**equation 20**). Therefore, it is desirable that Jung's criterion (1V/uS per peak output volt) be met for the series combination **(C1//C2)** alone in the absence of resistor **R**.

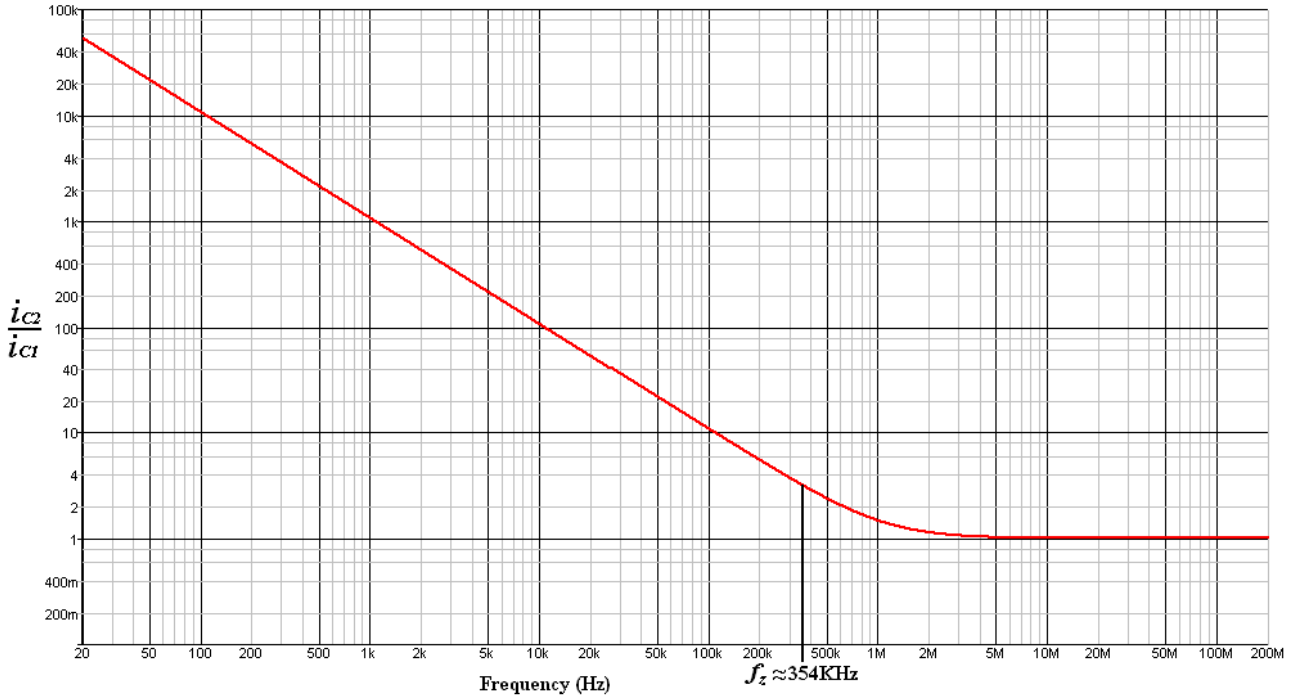


Figure 25. The ratio of current in C2 to that in C1 approaches unity at frequencies greater than 3.5MHz.

However, the double-pole compensator's behaviour at frequencies below the forward-path zero, where the current supplied by **R** is significant, is of particular interest. Clearly (compared with single-pole compensation) the double-pole network's dynamic current demands (**fig. 25**) on the input stage are considerably reduced for $(f < f_z)$. This allows the input stage to operate with greater linearity over a vastly greater frequency range, while the extended forward-path bandwidth simultaneously enhances the system's major-loop transmission.

While a 100pF single-pole compensation capacitor demands $4\mathbf{mA}_{(peak)}$ from the input stage at 160KHz to swing $40\mathbf{V}_{(peak)}$ at the TIS's output, the equivalent double-pole network (**fig. 26)**, whose values give the same forward path unity-gain frequency, will only need $1.7\mathbf{mA}_{(peak)}$ at the same frequency. Indeed, the double-pole compensator will only require $4\mathbf{mA}_{(peak)}$ from the TAS when signal frequency increases to 265KHz. This is roughly equivalent to a *peak* slew rate of $67\mathbf{V\mu S}^{-1}$, which should only decrease to $40\mathbf{V\mu S}^{-1}$ when signal frequency $f \geq (10 f_z = 3.54\boldsymbol{MHz})$ for the same $40\mathbf{V}_{(peak)}$ output swing.

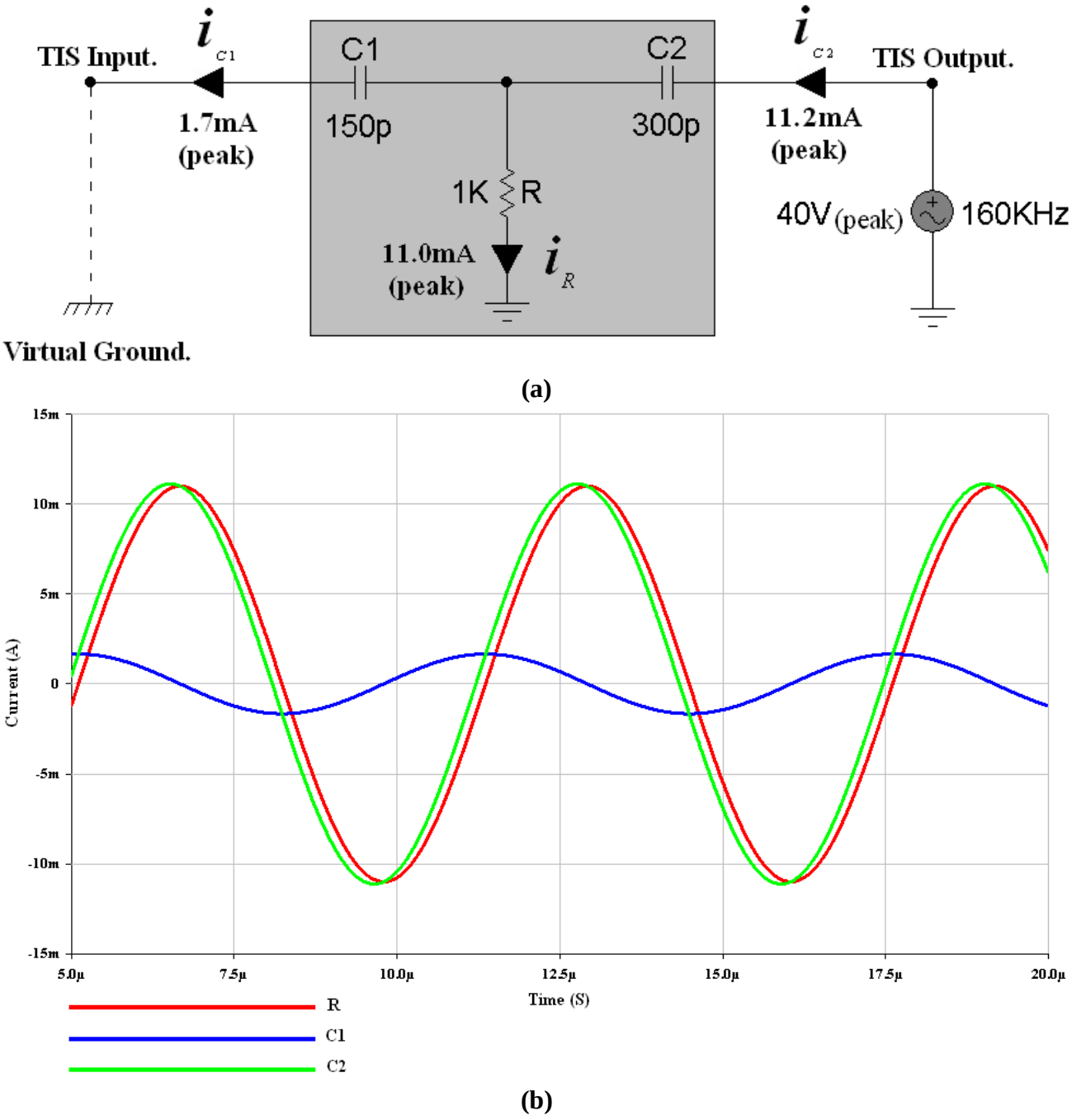


Figure 26. The double-pole network's current demands (a) at 160KHz were determined by merely grounding the input end of the TIS network and driving its output port to the rated output voltage (b).

Unfortunately, the TIS would need to source and sink $11.2\mathbf{mA}_{(peak)}$ respectively to and from the double-pole compensator to swing $40\mathbf{V}_{(peak)}$ at 160KHz; this is more than six times the current demanded of the input stage at this frequency.

Clearly, the second stage must provide peak current in excess of that required to drive the double-pole compensator and the output stage. As such, a nominal quiescent current in the region of 14mA (**fig. 27**) is called for; medium power transistors (TO-126 package) are therefore indicated for the TIS and its current source if long term reliability is to be guaranteed.

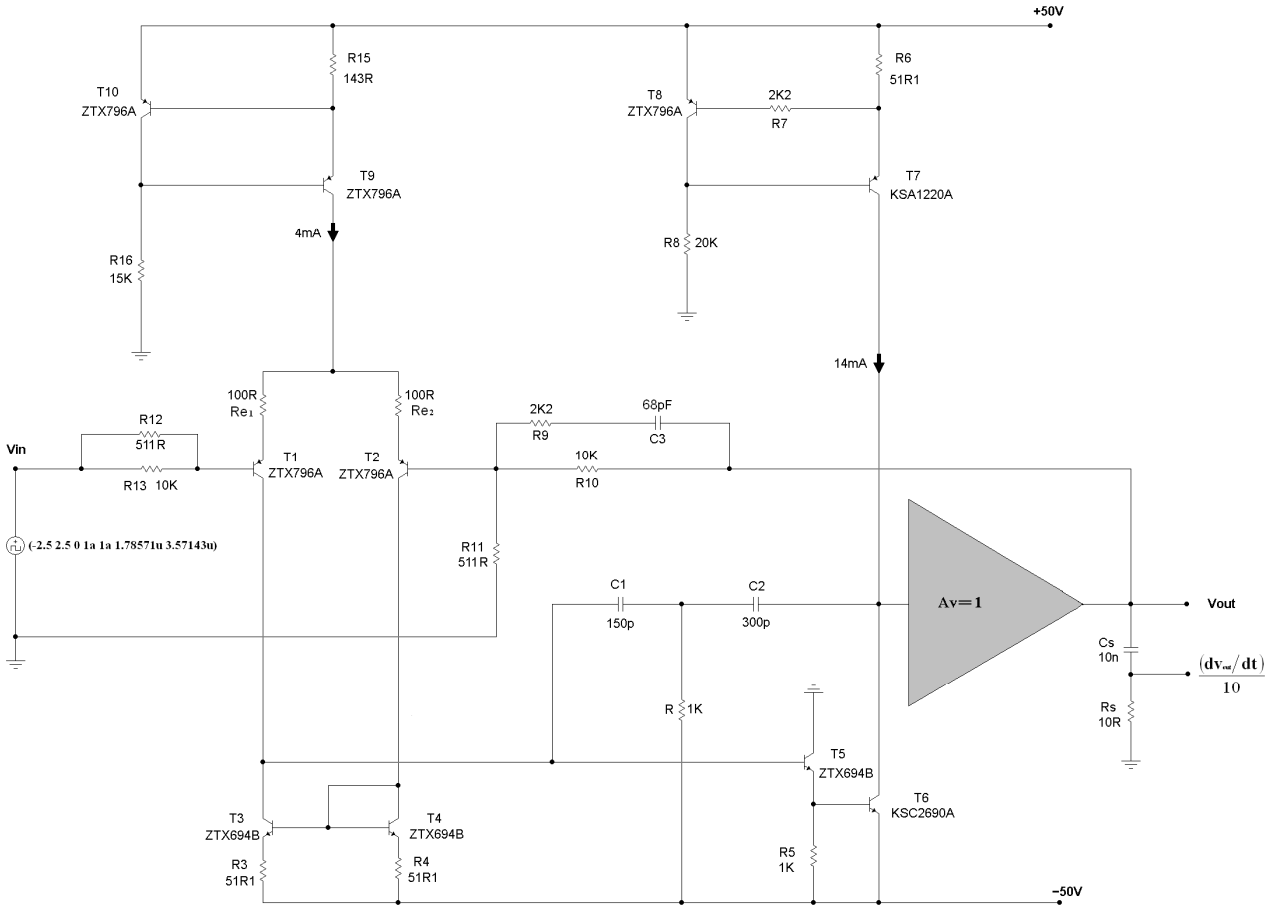


Figure 27. Simulating slew-rate in the double-pole compensated generic topology. An ideal VCVS models the output stage.

Nevertheless, with a thermally acceptable standing current, the TIS's current source **T7** may still be incapable of sourcing the full complement of current required by the compensator at ultrasonic frequencies, inducing a premature limit on positive slew rate.

This is demonstrated in SPICE[39], where slew rate may be straightforwardly determined by instructing the post-processor to return the derivative of the output waveform. Alternatively, with a practical circuit, a simple RC differentiator connected across the output (**fig. 27**) may be used[40].

For good accuracy, this should have a time constant at least 100 times smaller than the period of the input stimulus and, ideally, the reactance of the capacitor at the operating frequency should be at least five times larger than the value of the resistor; the selected values ($\mathbf{R_S} = 10\Omega$ and $\mathbf{C_S} = 10\mathbf{nF}$) give $0.1\mathbf{V_{(peak)}}/\mathbf{V\mu S^{-1}}$. An ideal unity-gain voltage controlled voltage source (VCVS) models the output stage.

The deficiency in slew rate for positive voltage swings (**fig. 28**) occurs because a significant amount of current that would otherwise service the compensator is instead siphoned off by shunt parasitic capacitance to ground at the TIS's output[41,42]. The use of medium power (TO-126) devices, with their relatively large output capacitance, merely exacerbates the problem.

No such impediment exists for negative slew as the second stage transistor **T6** is capable of sinking as much current through the compensator as supplied by the input stage's current source. Thus, the negative slew limit is only defined by the input stage's tail current, and, since the input stage is only required to deliver its maximum current of 4mA at 265KHz, a maximum negative slew rate of approximately $67\mathbf{V\mu S^{-1}}$ for $40\mathbf{V_{(peak)}}$ is realisable.

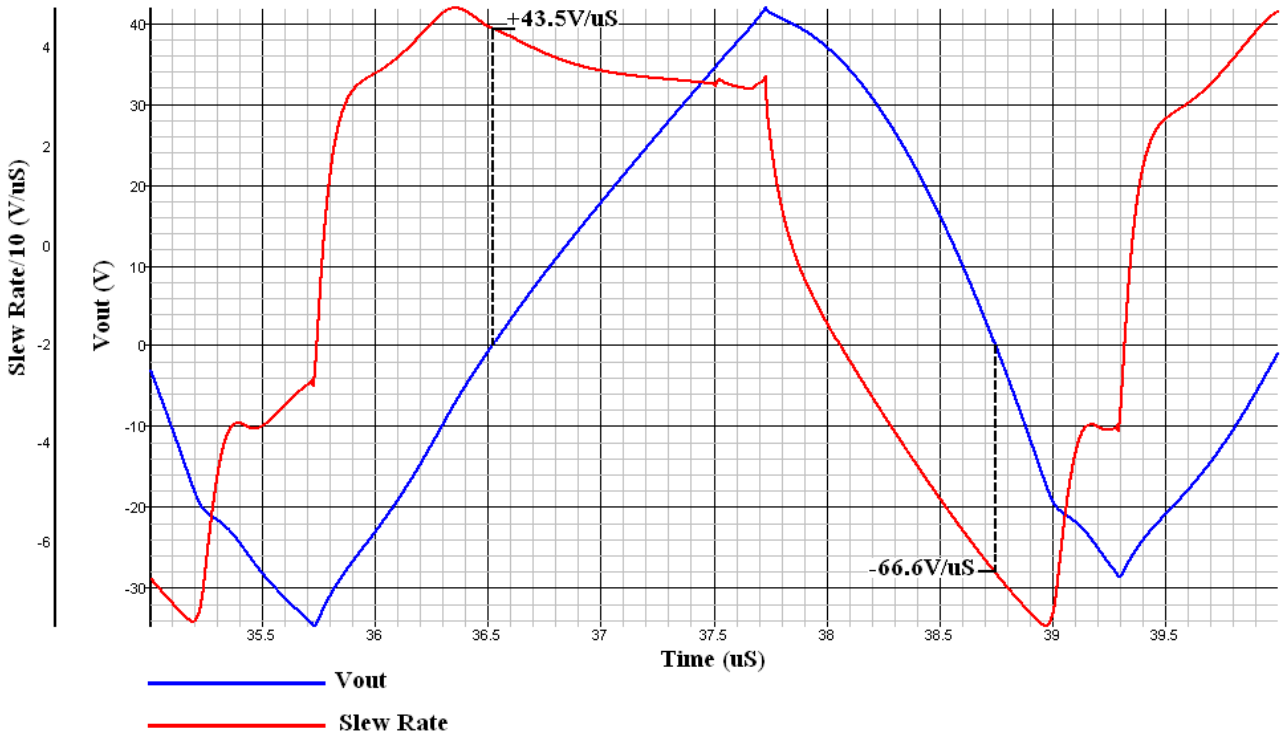


Figure 28. Current that would otherwise service the compensator is instead siphoned off by shunt parasitic capacitance to ground at the TIS's output, giving an asymmetric slew response.

Despite the asymmetry, slew-rate performance (**fig. 28**) comfortably meets the 160KHz power bandwidth requirement. Nevertheless, the purist may prefer to exploit the *peak* 265KHz power bandwidth made available in principal by using double-pole compensation. To this end, the deficiency in positive slew rate may be remedied by merely increasing **T7**'s quiescent current. This is unattractive, as second stage transistors **T6** and **T7** would each dissipate more than 1W, mandating the use of heat sinks.

In "small-signal" (*viz.* line-level) applications, the residual slew asymmetry may be eliminated by merely connecting the compensator to the output of the amplifier[43] where the push-pull output buffer will effortlessly sink and source as much current as required. However, with the loading of the compensation capacitor removed from the second stage, in this application, the minor loop's unity-gain bandwidth (typically >>40MHz) exceeds the current-gain bandwidth product f_t of virtually all high power bipolar devices. In other words, the second stage generates gain substantially greater than unity beyond frequencies at which the phase shift introduced by the output stage's dominant singularities exceeds 180^{o}.

Therefore, this approach is infeasible in a design with a high power bipolar output buffer as its dominant poles would virtually guarantee minor loop instability. Although the local loop may be compensated by connecting substantial shunt capacitance to ground at the TIS's output, this is counterproductive as it merely reintroduces slew asymmetry.

Douglas Self[23] recommends a small *booster* capacitor $\mathbf{C_b}$ (of the order of **T7**'s base-collector parasitic capacitance) connected between **T7**'s collector and **T8**'s base (**fig. 29**). This stimulates push-pull action in **T7** at ultrasonic frequencies, and thus obviates slew asymmetry **(fig. 30)** by reducing bias to **T8**'s base for positive voltage transients, and conversely for negative voltage swings.

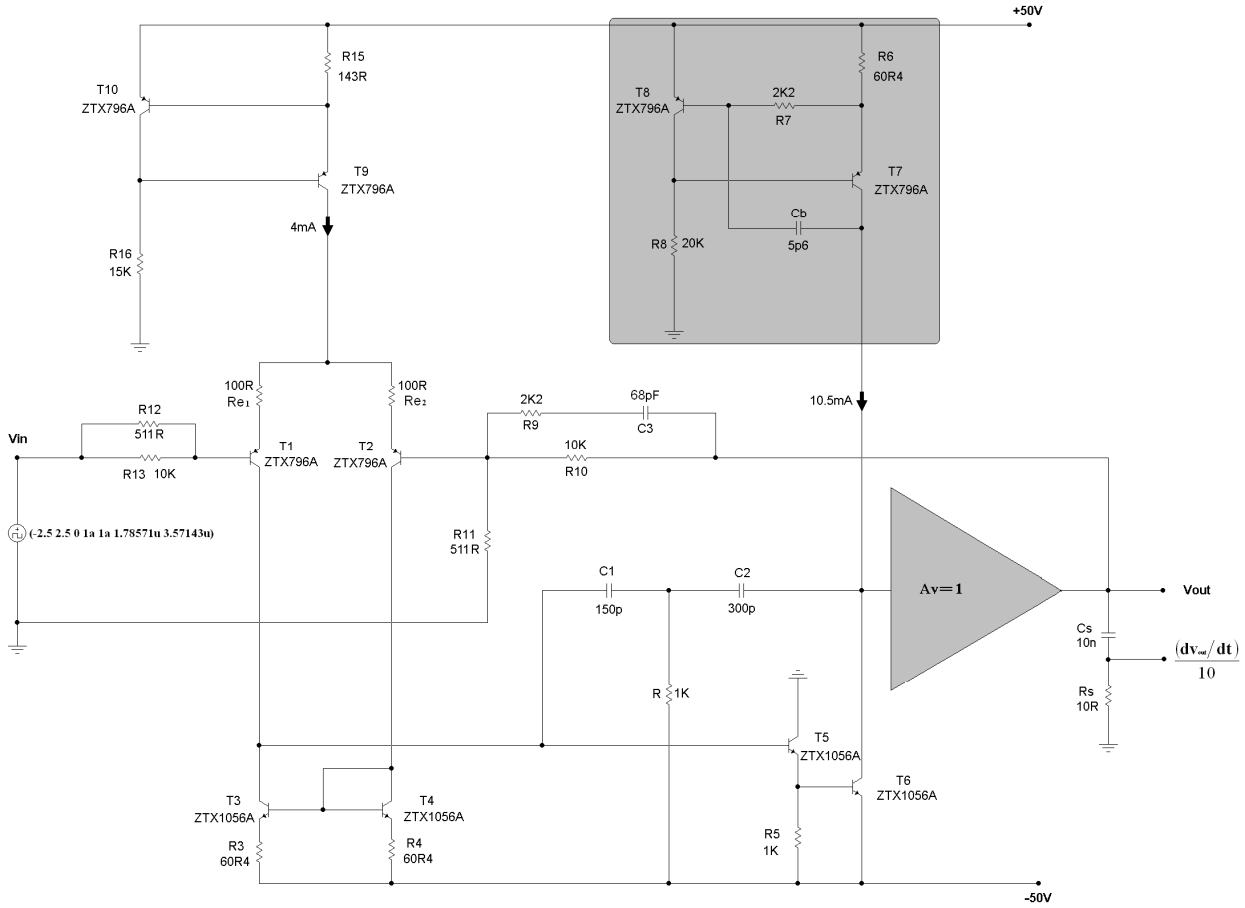


Figure 29. Booster capacitor C_b stimulates push-pull action at ultrasonic frequencies; this obviates slew asymmetry by reducing bias to T8 for positive voltage transients, and conversely for negative voltage swings.

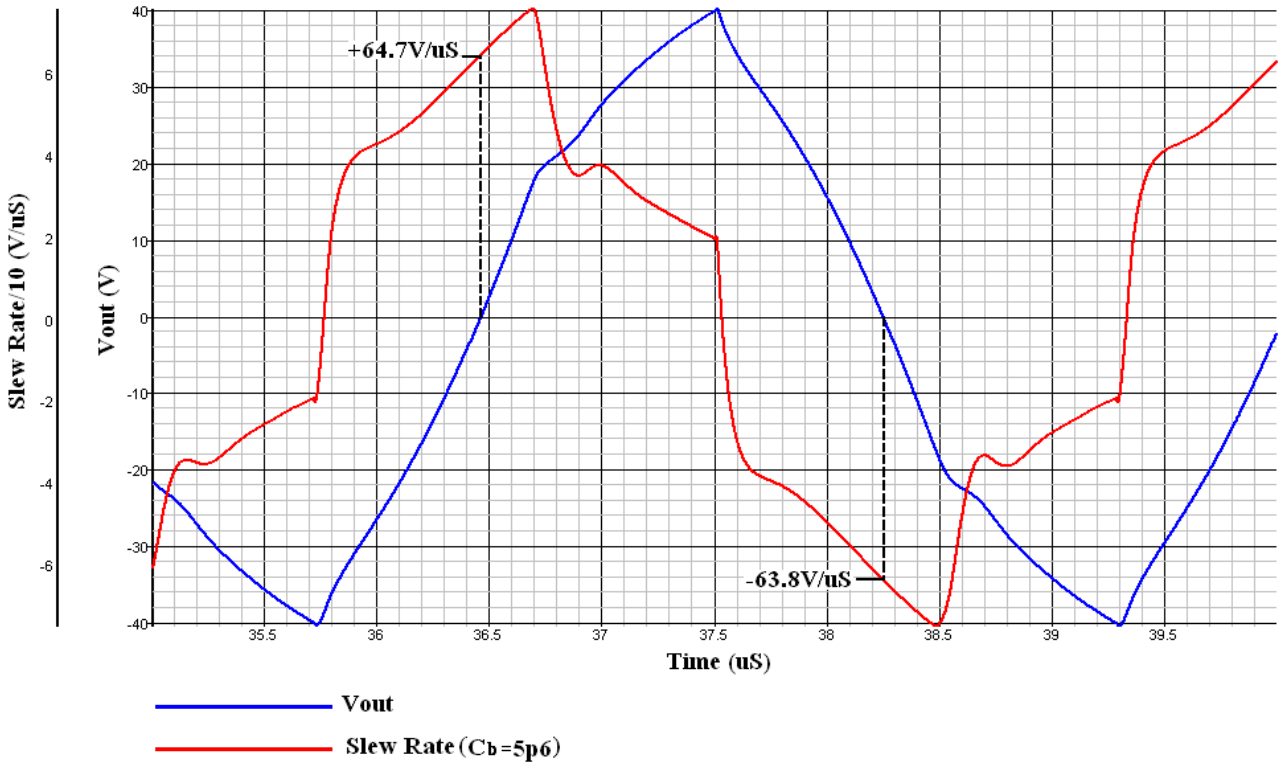


Figure 30. The slew response, with C_b *in-situ*, shows virtually no asymmetry.

In principal, this push-pull mechanism allows the TIS's quiescent current to be reduced to roughly 10.5mA without affecting slew rate. Inexpensive TO-92 (Zetex 'E-line') devices may then be used for **T6** and **T7** since average dissipation in each is less than 500mW. Note that resistor **R7** is now mandatory to isolate $\mathbf{C_b}$ from **T7**'s emitter.

However, values of $\mathbf{C_b}$ as low as 6p2 (with a single-pole compensation capacitor $\mathbf{C_C} = 100\mathbf{p}$) were found to markedly reduce the compensation (minor) loop's stability margins **(fig. 31)** whilst having negligible effect on those of the major loop.

The transition to gross instability in the compensation loop is abrupt and its onset is dependent on transistor type. The threshold was found to be slightly higher for the double-pole network values of **figure 29**. This is because at ultra-sonic frequencies, when capacitor **C2** is effectively short-circuit, the loading of resistor **R** on the TIS's output reduces its forward-path gain so that minor loop transmission falls below unity before loop phase shift exceeds $180^{\mathbf{o}}$.

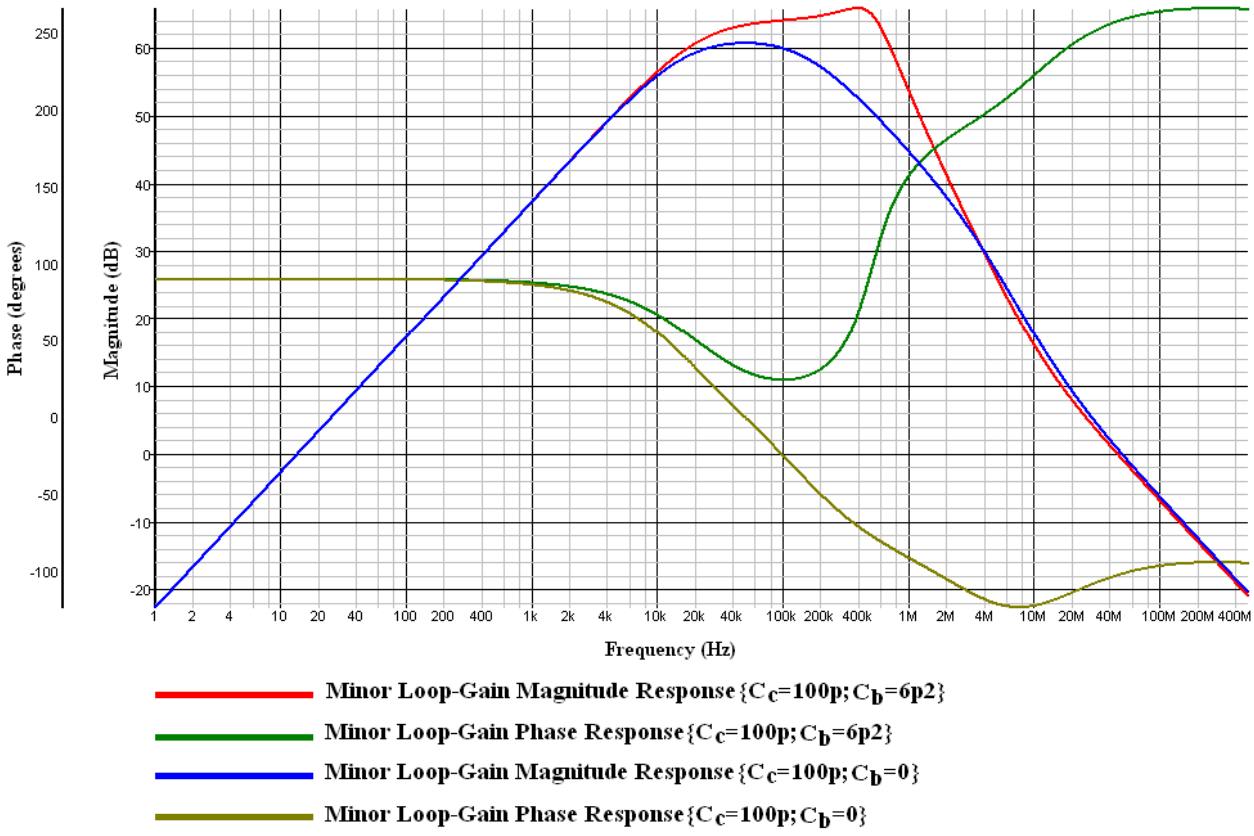


Figure 31. The stability of the compensation loop is compromised by the slew rate booster capacitor $\mathbf{C_b}$.

Moreover, Self's practice of using the TIS's feedback current source, with $\mathbf{C_b}$ *in situ*, as a voltage reference for the input stage current source is devoid of merit (**fig. 32**). This is because positive ultrasonic voltage swings at the TIS collector drive **T8**'s base ***high*** via $\mathbf{C_b}$ inducing a drop in its collector current. This is necessarily accompanied by **T8**'s collector going ***low***, which causes an increase in bias voltage applied to the base of TAS current source **T9** with respect to the positive supply.

Consequently, first stage tail current increases to more than twice its nominal quiescent value, while negative voltage transients at the TIS's collector briefly reduce input stage standing current. Since input stage transadmittance is a function of tail current, the momentary but substantial increase in the tail current leads to an equivalent rise in TAS gain as the positive slew limit is approached.

This may provoke sporadic instability in the major feedback loop as the output is driven positive at high frequencies. Additionally, far from promoting slew symmetry, Self's approach merely exacerbates it, with peak positive slew rate increasing to over 70V/uS, while negative slew rate deteriorates by more than 40% (**fig. 33**).

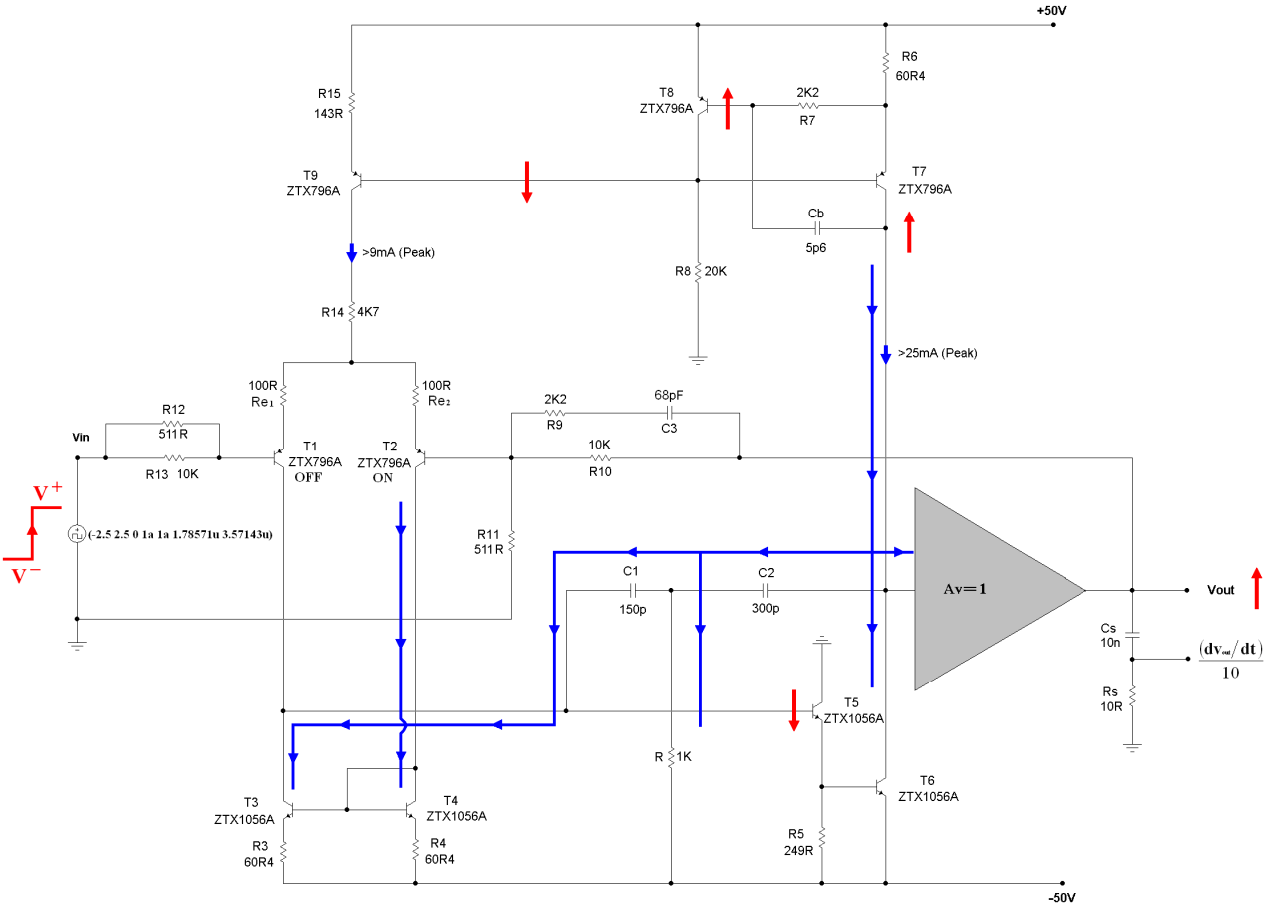


Figure 32. Using a shared voltage reference for first and second stage current sources (with C_b *in-situ*). Instantaneous voltage and current polarities during positive slew are given in red and blue respectively.

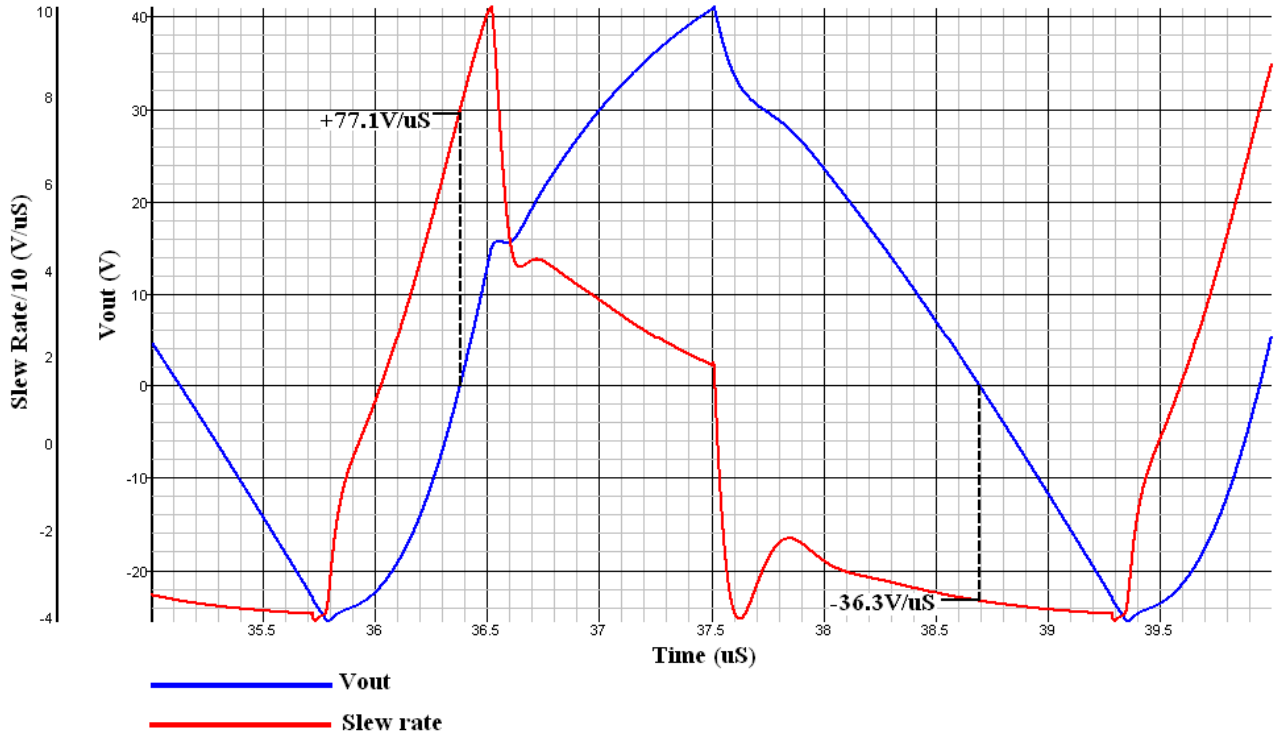


Figure 33. The shared voltage reference between first and second stage current sources merely exacerbates slew-asymmetry.

By merely interchanging **C1** and **C2 (fig. 34)**, the double-pole compensator's current draw on the TIS may be reduced by 50% to well beyond 200KHz, while the current demanded of the input stage remains unchanged. Although ζ_0 is slightly reduced (**equation 15**) the forward path unity-gain frequency remains the same, and minor-loop stability margins also remain virtually unchanged. Notably, the current demanded of the TIS at 160KHz falls by nearly 43% compared to the equivalent single-pole compensator $\mathbf{C_C} = 100\mathbf{p}$.

With this modification, positive slew rate increases from 43.5V/uS **(fig. 28)** to 62.6V/uS **(fig. 35)**. The residual (and trivial) asymmetry may be eliminated with the reduced TIS quiescent current of **figure 29** by using a much smaller value of booster capacitor $\mathbf{C_b} = 2\mathbf{p}2$. This is of the order of PCB parasitic capacitance, and may be realised by merely placing the collector and base traces of the ANF current source transistors (**T7** and **T8**) as close together as practicable.

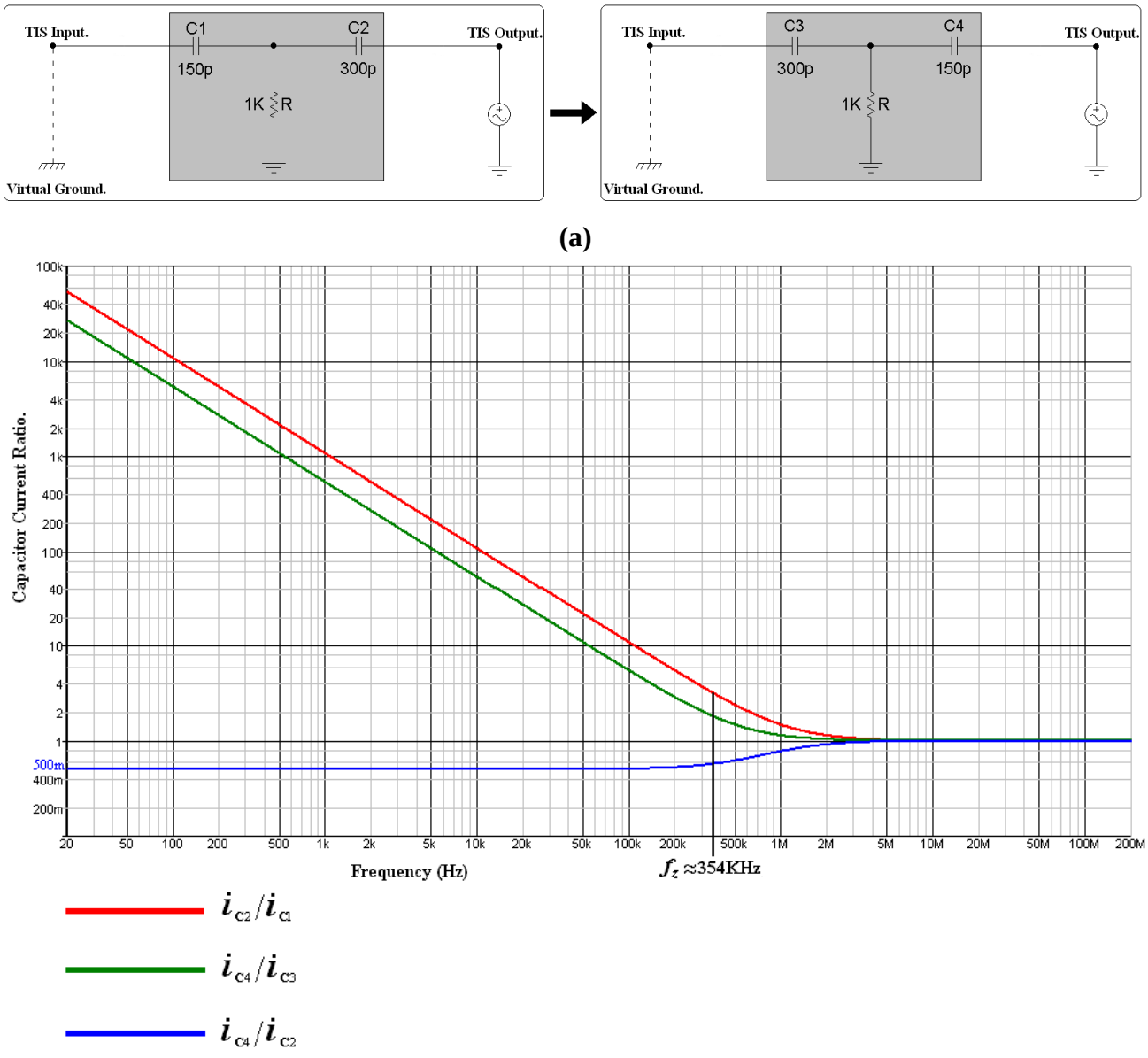


Figure 34. Merely switching C1 and C2 (a) halves the current demands of the compensator on the TIS (b), while the current demanded of the input stage remains unchanged.

However, a capacitor may be preferred instead to facilitate increased trace separation in the interest of inhibiting inductive coupling between these traces; the capacitor's leads should be kept as short as possible to minimise parasitic inductance.

It could well be argued that modifying the generic topology to force symmetry in slew rate is somewhat academic, as one need only reduce **C2** relative to **C1** in the double-pole compensator **(fig. 34)** to meet the 160KHz power bandwidth requirement (*viz*. minimum slew rate ~ $1\mathbf{V\mu S^{-1}} / \mathbf{V_{out[peak]}}$). However, the preceding treatment was deemed necessary to preclude the obviously incorrect but often-made assertion that some desirable feature of this topology may not be improved without having "another collapse into disorder or asymmetry" [25] .

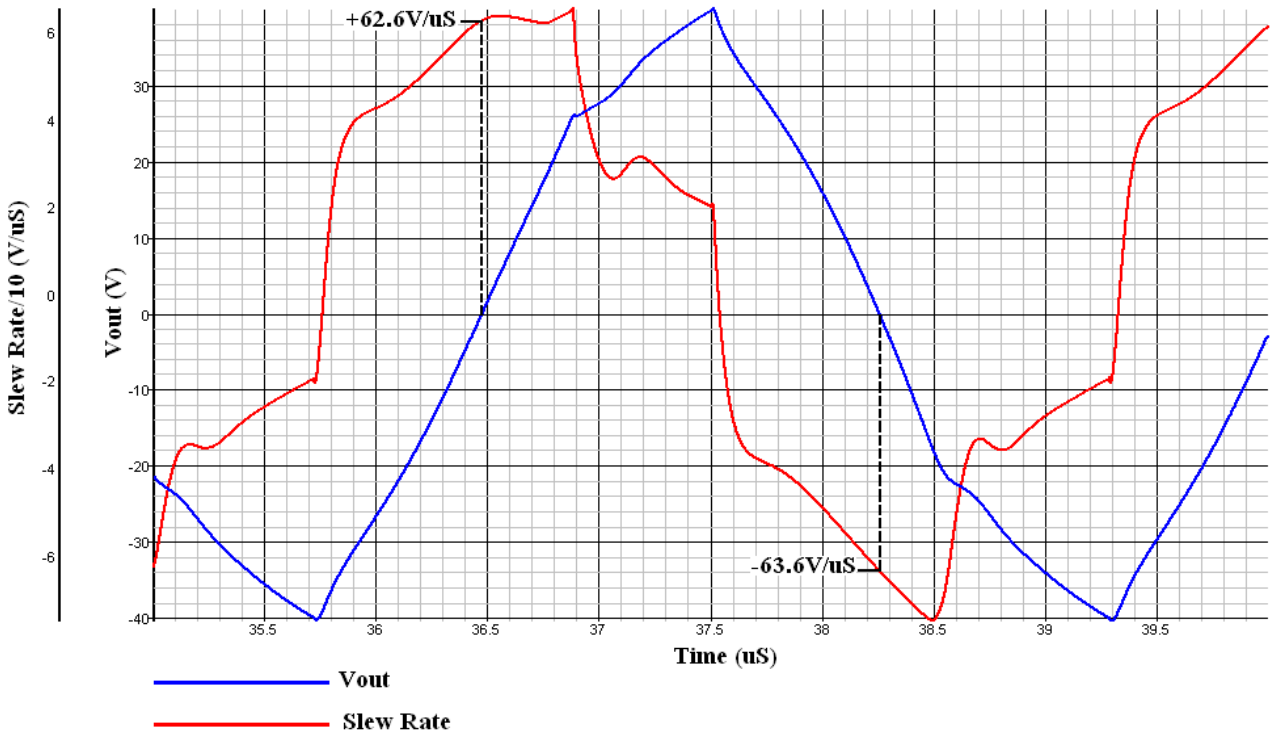


Figure 35. Positive slew-rate improves significantly when C2 is made smaller than C1.

The Double Cascaded Differential Stages (DCDS) Voltage gain Block

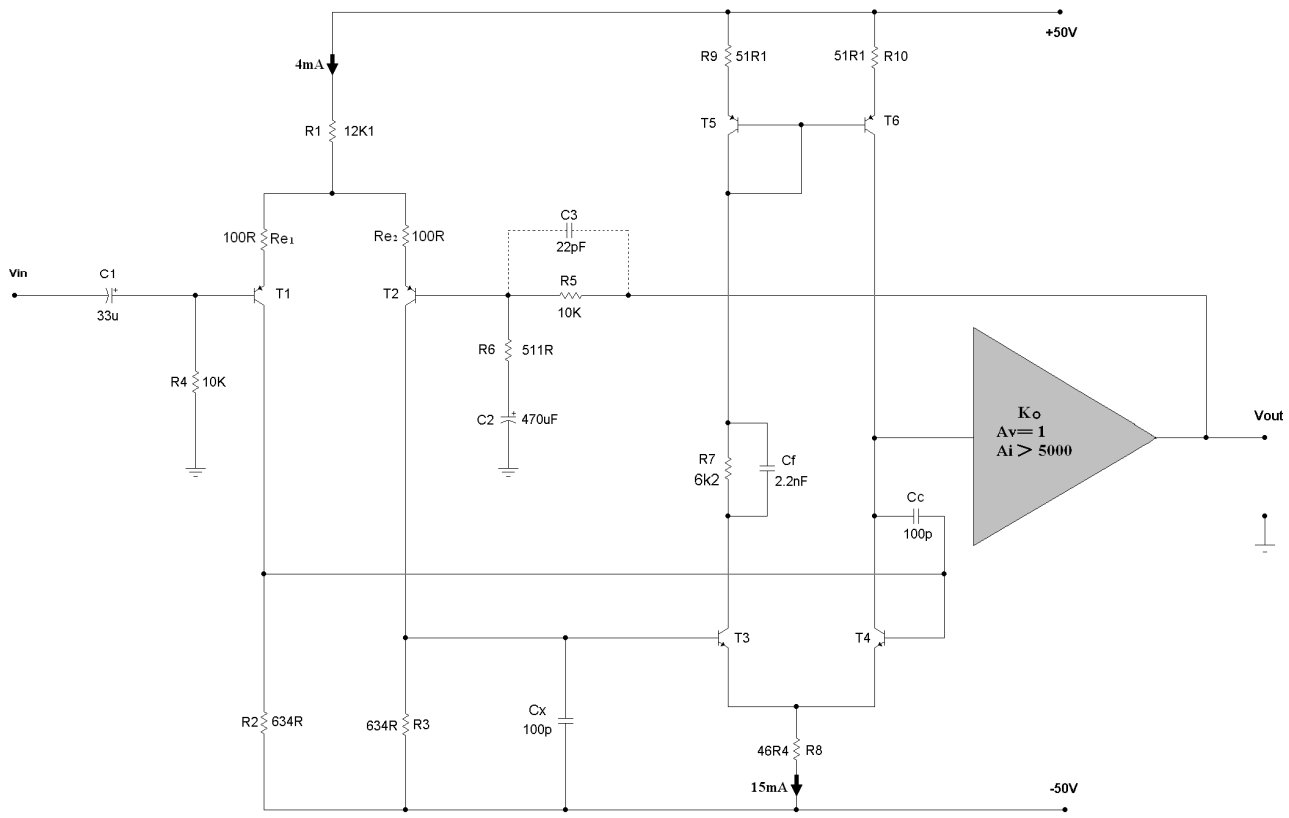


Figure 36. The Mullard-type DCDS voltage gain block popularised by Hitachi.

The circuit of **figure 36**, with typical component values, shows the essential elements of Hitachi's discrete variant of the DCDS topology apparently conceived by Mullard (presently Philips, *circa* 1967). The *raison d'être* of this arrangement is (or should be) to introduce push-pull action to the transimpedance stage by converting **T8** in **figure 1** into a controlled current source. This is desirable because true push-pull action obviates slew-asymmetry, and promises cancellation of even-order harmonics generated by the second stage.

To this end the current mirror is relegated to the second stage (**T5**, **T6**), and a pair of nominally identical resistive loads (**R**2 and **R3**) provide double-ended drive to the second stage. Accordingly, the first stage is required to deliver a voltage output to **T3** and a nominal current output to **T4** at the frequencies of interest.

The second-stage current mirror is effectively a current-controlled current source, with the controlling current provided by a voltage-controlled current sink in the form of level-shifting transistor **T3**. Typically, for maximal voltage efficiency, the quiescent voltage dropped across **R8** and each of the mirror's degeneration resistors, **R9** and **R10**, should not exceed two diode drops (*viz.* ~1.3V).

DCDS-specific Compensation

Although the differential input stage in **figure 36** is resistively loaded, its double-ended output ensures that the effective transconductance of this stage is roughly equal to that delivered by the mirror-loaded TAS in the conventional arrangement (**fig. 1)**. Thus, if roughly the same forward path unity-gain frequency is desired for the same TAS tail current, the compensation capacitor and first-stage degeneration resistors in the DCDS and the generic topology must be equal.

Nevertheless, contrary to popular opinion[8,44], the DCDS gives much lower infrasonic forward-path gain than the conventional approach **(fig. 37a)**. This is principally because its single-transistor TIS inevitably lacks the substantial current gain of the compound arrangement in **figure 1**.

This is exacerbated by the much lower source impedance presented to **T4** by the resistively-loaded first stage. Note that a transimpedance stage takes a current as its input, and therefore requires the large output impedance of a near-ideal current source for maximal current transfer. Thus, in principal, regardless of output stage topology or component values, the circuit of **figure 36** may be expected to generate more than an order of magnitude greater distortion across the audio band than the Thompson design.

Moreover, in contrast to **figure 1**, minor loop compensation due to $\mathbf{C_C}$ in the DCDS topology may not guarantee a single-pole roll-off at frequencies preceding the system's first non-dominant pole. This is because the DCDS arrangement presents the signal with two paths from the input stage to the TIS's output.

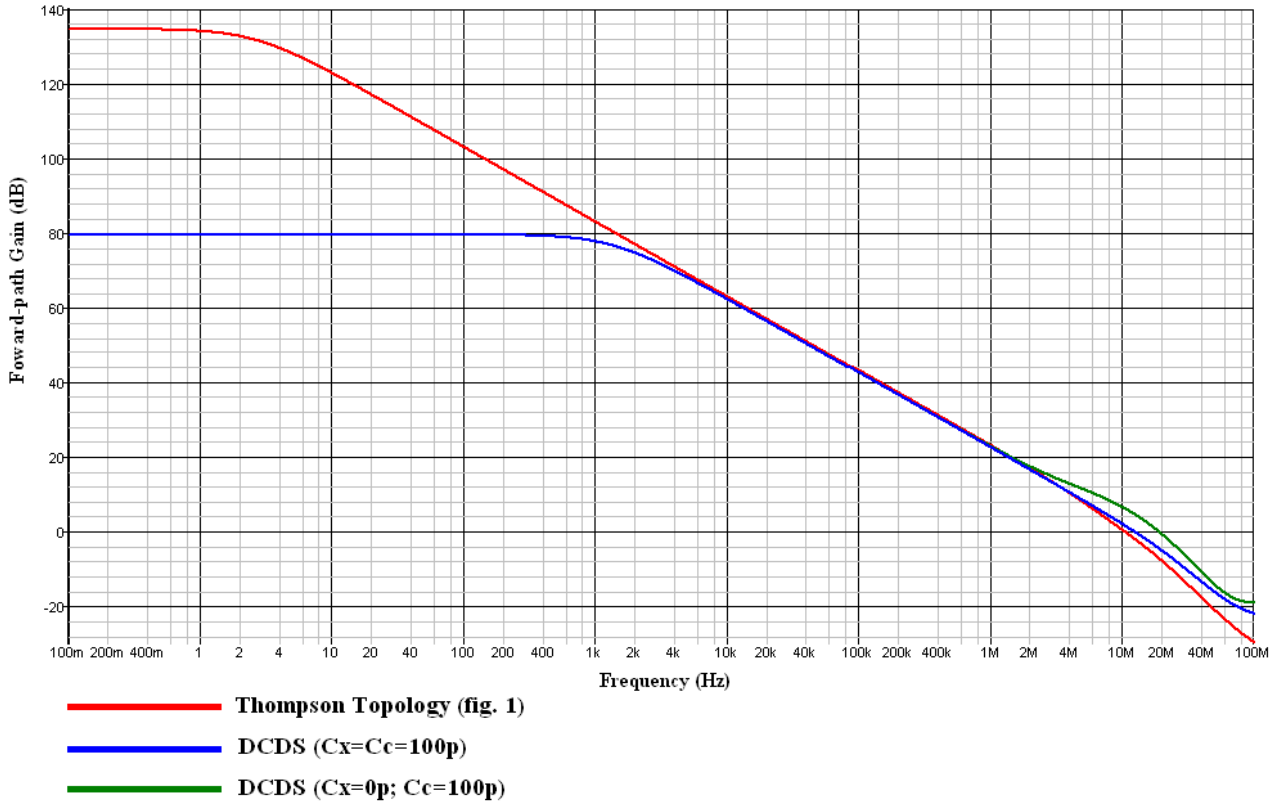
Clearly, minor-loop compensation ensures that the signal path through **T4** (in the absence of $\mathbf{C_X}$) possesses a vastly diminished unity-gain bandwidth compared to the path through **T3**. This discrepancy is expressed as an LHP zero in the vicinity of the system's forward path unity-gain frequency **(figs. 37b**). In general, ***n*** signal paths through an amplifier give rise to ***n-1*** zeros in its forward path transfer function[46].

This zero may seem desirable as the resulting positive phase shift might be expected to improve the amplifier's stability margins. Unfortunately, the positive phase shift is inevitably accompanied by an increase in forward path unity-gain frequency, appreciably greater than that predicted by the single-pole model.

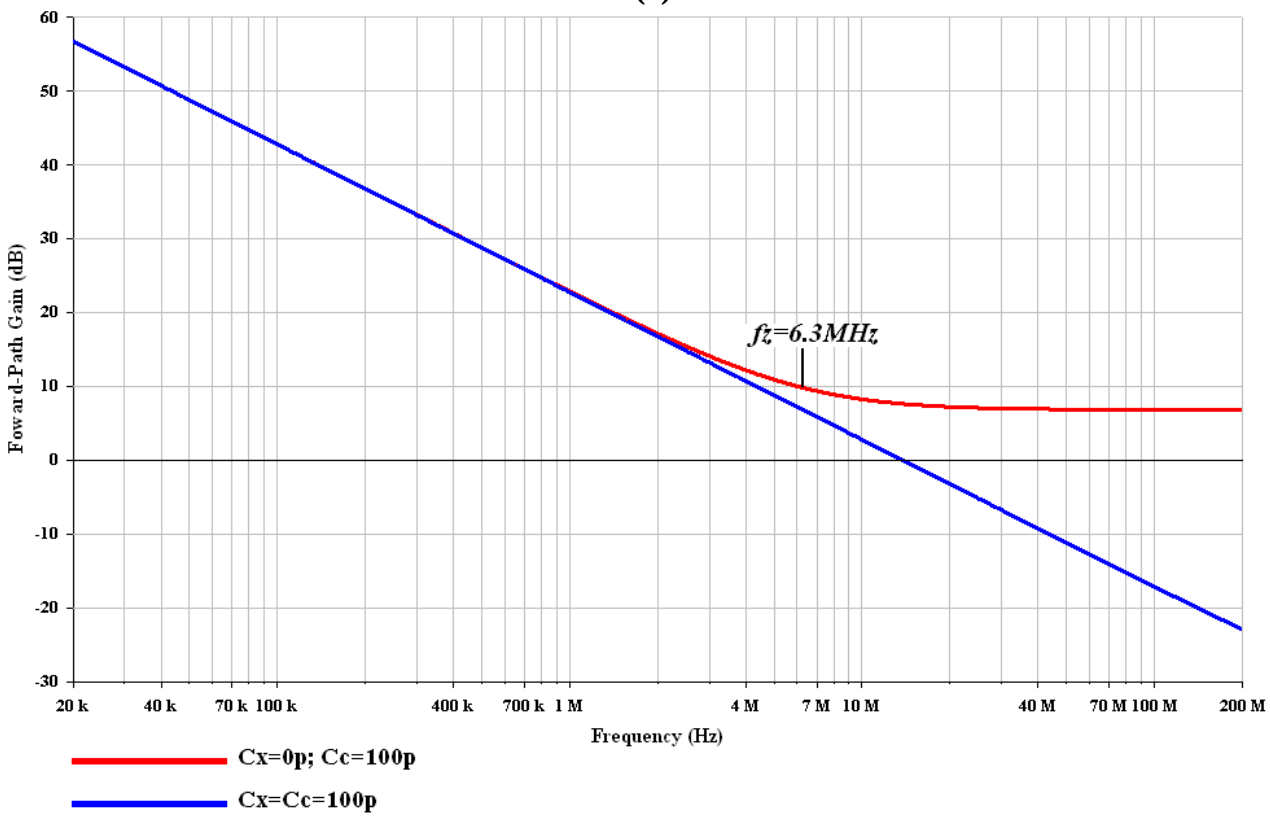
Paradoxically, this increase in unity-gain frequency may result in an inadequate loop gain margin due to gain peaking contributed by non-dominant complex singularities. Although this unlikely to be a problem with single-pole compensation and the relatively low TIS gain of **figure 36**, in variants of the DCDS where local forward-path current gain in the TIS is relatively high, the forward-path zero is often followed by a pair of complex poles in the vicinity of the unity-gain frequency.

Thus, such designs may simultaneously possess an acceptable loop phase margin and a deficient or even negative loop gain margin due to gain peaking beyond unity-gain frequency. Moreover, this is likely to be further exacerbated by the mandatory phase lead network required to limit closed-loop bandwidth with double-pole compensation.

A nominal first-order response is restored by connecting capacitor $\mathbf{C_X}$ (equal to the single-pole compensation capacitor $\mathbf{C_C}$) across **T3**'s input. This introduces a pole at half the frequency (3.1MHz) of the forward path zero, and simultaneously lowers the zero to this frequency causing its cancellation. Gain margin is improved at the expense of a slight deterioration (~5 degrees) in phase margin.



(a)



(b)

Figure 37. (a) The DCDS gives much lower infrasonic forward-path gain than the conventional approach. (b) Using ideal transistors (with zero inter-electrode capacitance) for clarity, SPICE simulation of the DCDS topology reveals the LHP zero (for $C_X = 0p$) at approximately 6.3MHz; this causes the forward path's frequency response to deviate significantly from the desired single-pole characteristic as unity-gain frequency is approached.

In practice, component tolerances preclude exact cancellation of the zero, and a pole-zero doublet ensues. Typically, however, the doublet is located at such a high frequency that its effect on settling time is negligible.

The two signal paths to the TIS output afford a degree of flexibility with respect to frequency compensation that is otherwise unavailable with the generic topology[47]. For example, increasing $\mathbf{C_X}$ to 1nF enhances minor-loop stability and allows $\mathbf{C_C}$ to be halved for roughly the same forward path unity-gain frequency **(fig. 38)**.

Since $\mathbf{C_X}$ has increased by an order of magnitude, the frequency of the pole it introduces is reduced by the same amount to 312KHz. Regrettably, the zero only relocates to 591KHz, creating a conspicuous pole-zero doublet, with the pole at nearly half the frequency of the zero it's supposed to cancel.

The nominal slew rate nearly doubles at the cost of some deterioration (~10 degrees) in phase margin. The conspicuous overshoot in the amplifier's transient response **(fig. 39)** may be controlled by a small phase lead capacitor **C3** across feedback resistor **R5**.

An apparently unknown advantage presented by dual paths to the TIS's output **(fig. 36)** is the elimination of the non-minimum phase (RHP) zero otherwise generated when $\mathbf{C_C}$ short-circuits **T4**; in this case transistor **T3** (through current mirror **T5/T6**) provides the drive required to prevent $v_{out} = 0$.

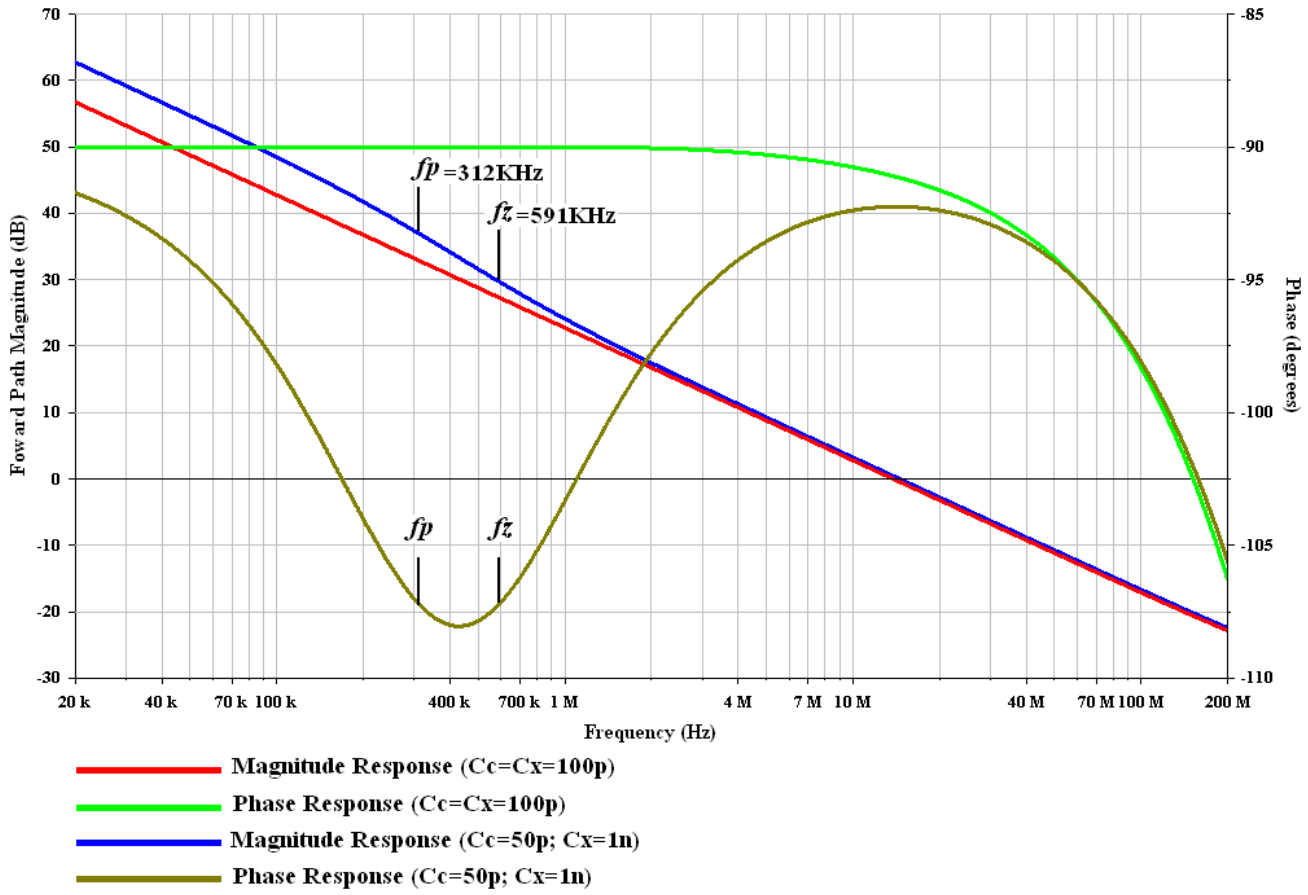


Figure 38. Using ideal BJTs (with zero inter-electrode capacitance) in SPICE reveals the conspicuous pole-zero doublet, due to the mismatch in the values of Cx and Cc, in the forward-path's frequency response.

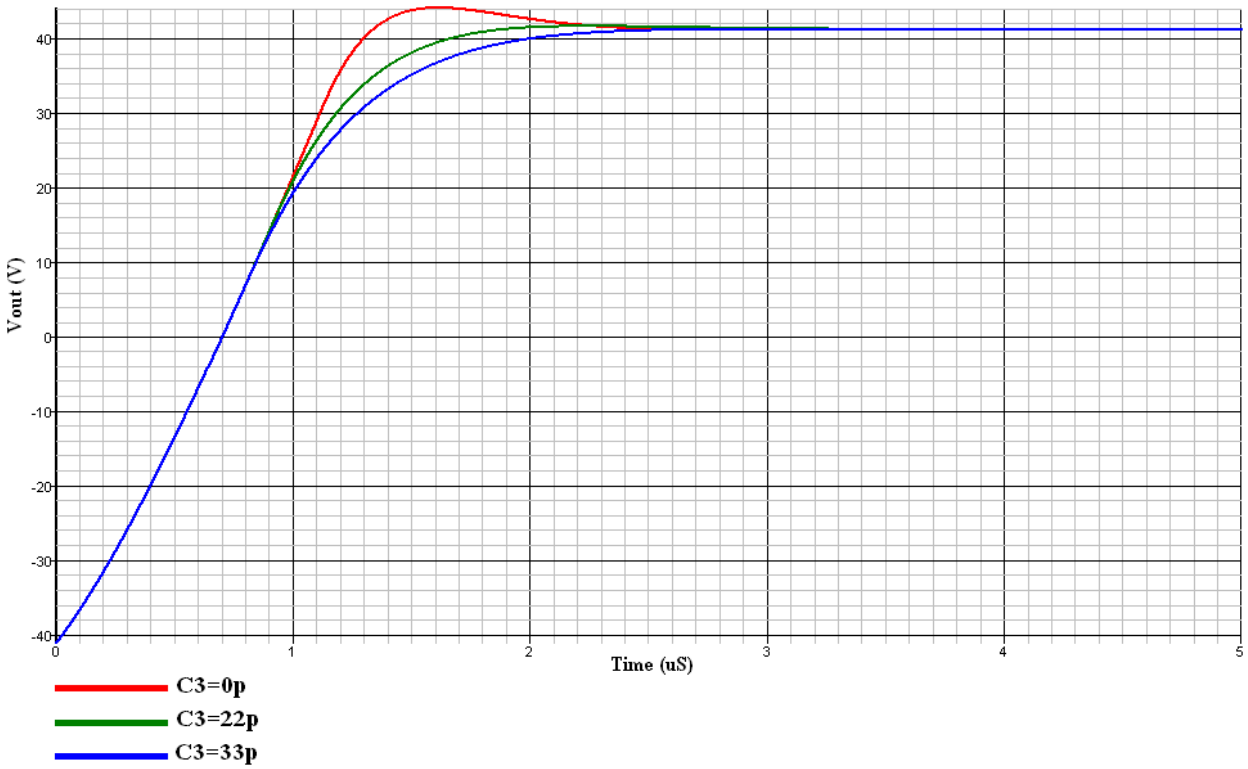


Figure 39. Using feedback lead compensation to inhibit overshoot in the amplifier's transient response.

Clipping Overload Characteristics of the DCDS Topology

While 100% DC negative feedback holds **T4**'s collector close to zero volts in the absence of input stimulus (**fig. 36**), transistor **T3** often requires the inclusion of dummy load **R7** in series with its collector to prevent it from being almost entirely exposed to the magnitude sum of the two supply rails while sinking significant current. Resistor **R7** merely minimises **T3**'s collector dissipation and, contrary to White[1], plays no part in setting second stage quiescent current, which is clearly a function of the voltage dropped across first stage load resistors **R2** and **R3**.

If the circuit is overdriven to negative output voltage clip, transistor **T2** is cut-off, and the entire first-stage tail current diverted to **T1**. The voltage across **R2** virtually doubles, and although **T4** is thus driven into saturation, the current it's required to sink is relatively small since **T3** is reverse-biased, cutting off current mirror **T5**, **T6**.

Similarly, if the circuit is excessively driven to positive voltage clip so that **T1** is cut off, the entire first-stage tail current is diverted to **T2**. Since the current sunk by **R2** through $\mathbf{C_C}$ during positive clipping is negligible, the voltage drop across **R2** is also negligible, and **T4** is therefore reverse-biased.

The voltage across **R3** increases to nearly twice its quiescent value and, because the increase in **T3**'s base-emitter voltage is relatively small, the voltage across **R8** (in the absence of **R7**) nearly triples, increasing from its quiescent value of 690mV to 1.9V. This causes a drastic increase in **T3**'s collector current, from 7.5mA to over 40mA (**fig. 40**), while the voltage across the device hardly falls below 99V throughout the cycle.

Therefore, whilst peak power dissipation amounts to a mere 0.7 watts in **T4** (**fig. 41**), it is of the order of 4 watts in **T3**. Moreover, with the circuit thus overdriven, device voltage and current are more rectangular than sinusoidal.

This causes the average power dissipated in **T3** to approach its peak value and in the absence of **R7**, particularly with sustained low-frequency overdrive, will almost certainly exceed the capabilities of the TO-92 package normally used in this position; a typical specimen, such the **ZTX1056A**, is rated to dissipate no more than 1W at an improbable ambient temperature of $25^0\mathrm{C}$.

The value of **R7** is straightforwardly determined by assuming symmetrical supply rails, with transistor **T4** cut off ("open-circuit") and **T3** in saturation. The voltage drops across **R8** and **R9** may be considered negligible compared to the supply rails.

While it's required to be large enough to protect **T3** from over-dissipation, resistor **R7** has to be sufficiently small to accommodate supply rail sag without adversely curtailing a saturated **T3**'s ability to sink at least the nominal second stage tail current during normal unclipped operation; this is particularly desirable if double-pole compensation is used. These constraints are satisfied by the empirically determined inequality given below, where **(fig. 36)** $\mathrm{I_{Tail2}} = \mathrm{I_{R8}}$.

$$\frac{\mathbf{V}^+}{2\mathbf{I}_{\mathbf{Tail}2}} < \mathbf{R}7 < \frac{2\mathbf{V}^+}{\mathbf{I}_{\mathbf{Tail}2}} \tag{52}$$

The feedforward capacitor $\mathbf{C_f}$ across **R7** eliminates an ill-defined but otherwise significant pole generated at **T3**'s collector by **R7** and **T3**'s parasitic collector-base capacitance. A time constant $\tau = \mathbf{C_f R}_7$ in the range $(10\mu\mathbf{S} < \tau < 100\mu\mathbf{S})$ is sufficient; a smaller value will appreciably degrade stability margins and positive slew, while an excessively generous time constant may expose **T3** to power spikes of sufficient magnitude and duration to impair its long-term reliability.

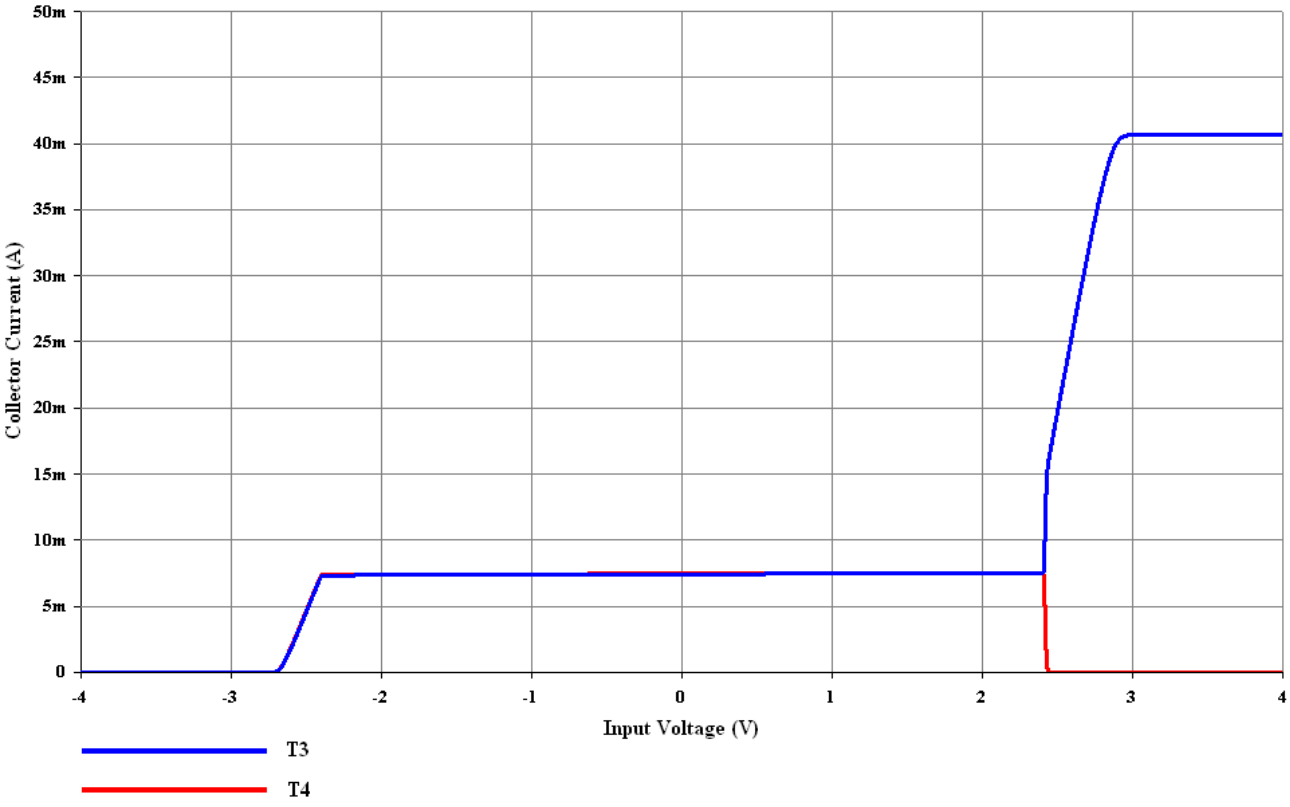


Figure 40. Positive voltage overdrive (in the absence of R7) causes an excessive increase in T3's collector current.

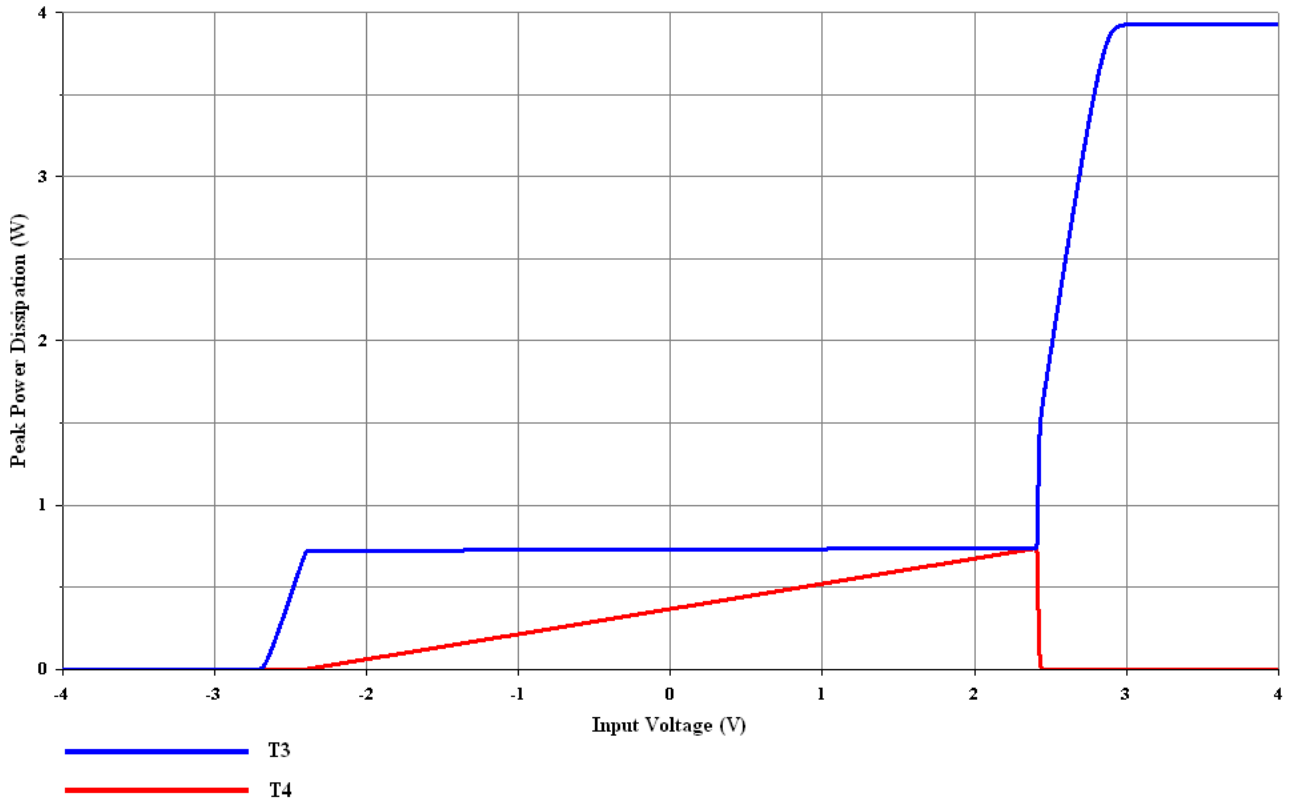


Figure 41. Since T3 (with R7 absent) is exposed to nearly 99V, its instantaneous dissipation during positive voltage overdrive approaches 4W.

Alternatively, the voltage across **T3** may be restrained (**fig. 42**) by replacing **R7** with common-base transistor $\mathbf{T_{C1}}$. The two transistors thus configured constitute a cascode with $\mathbf{T_{C1}}$ in the role of a unity current-gain buffer due to its 100% series (current) derived-shunt (current) applied local negative feedback.

Some means of containing the cascode's overload current may be necessary. In some designs this is achieved by merely returning the emitters of **T3** and **T4** (**fig. 42**) independently to the supply rail by way of two resistors, each twice the value of **R8**; this effectively halves **T3**'s maximum overload current.

Connecting a diode clamp **D1** across the first stage collectors is a rather more elegant solution (**fig. 42)**. During positive clipping, the voltage across **R3** increases, while that across **R2** decreases until diode **D1** is forward biased. Thus, resistor **R3** is effectively shunted by the series combination of **D1** and **R2**.

In other words, the differential input voltage to the second stage is constrained to **D1**'s forward-bias voltage drop, and enough current is now shunted away from **R3** to effect a reduction of the order of fifty percent in the voltage across it. The voltage across **R8** is reduced by the same amount, and causes an equivalent reduction in **T3**'s overload collector current and hence dissipation **(fig. 43)**.

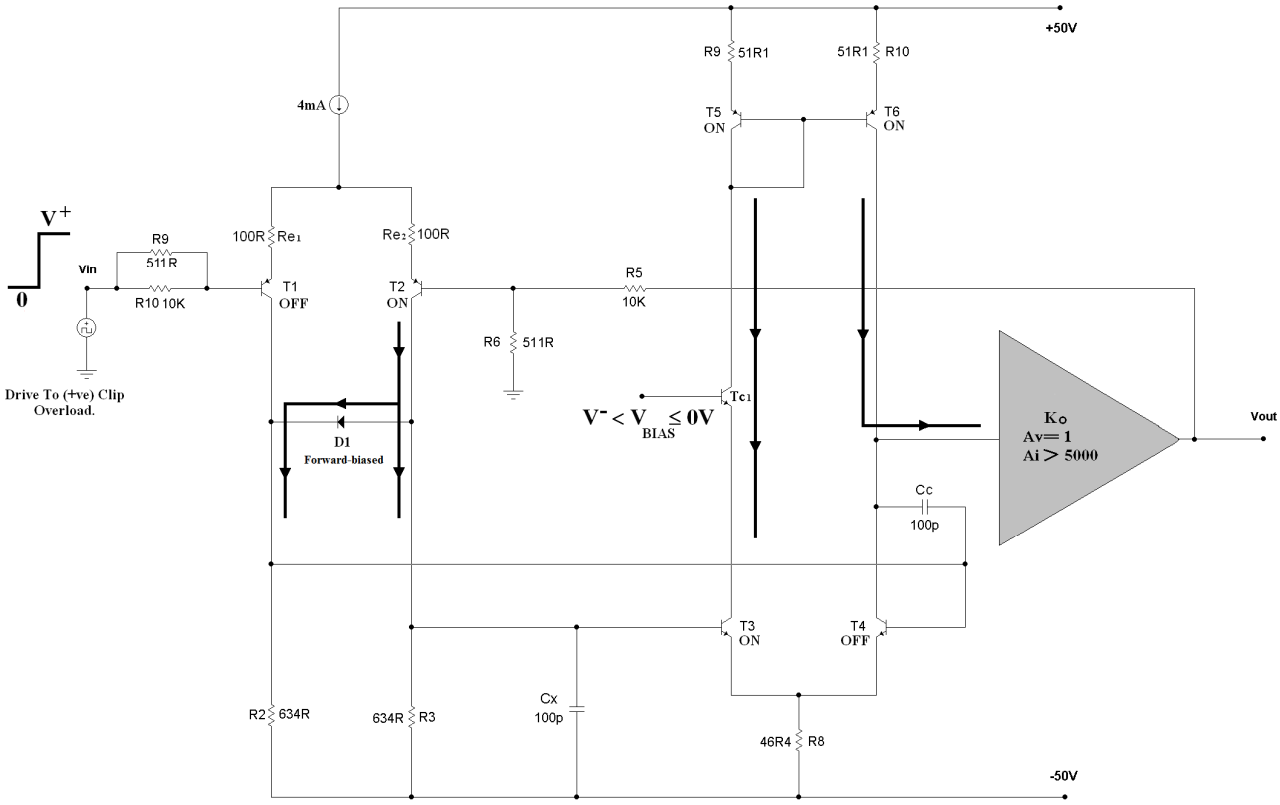


Figure 42. Diode D1 siphons current away from R3 into R2 during positive voltage overload.

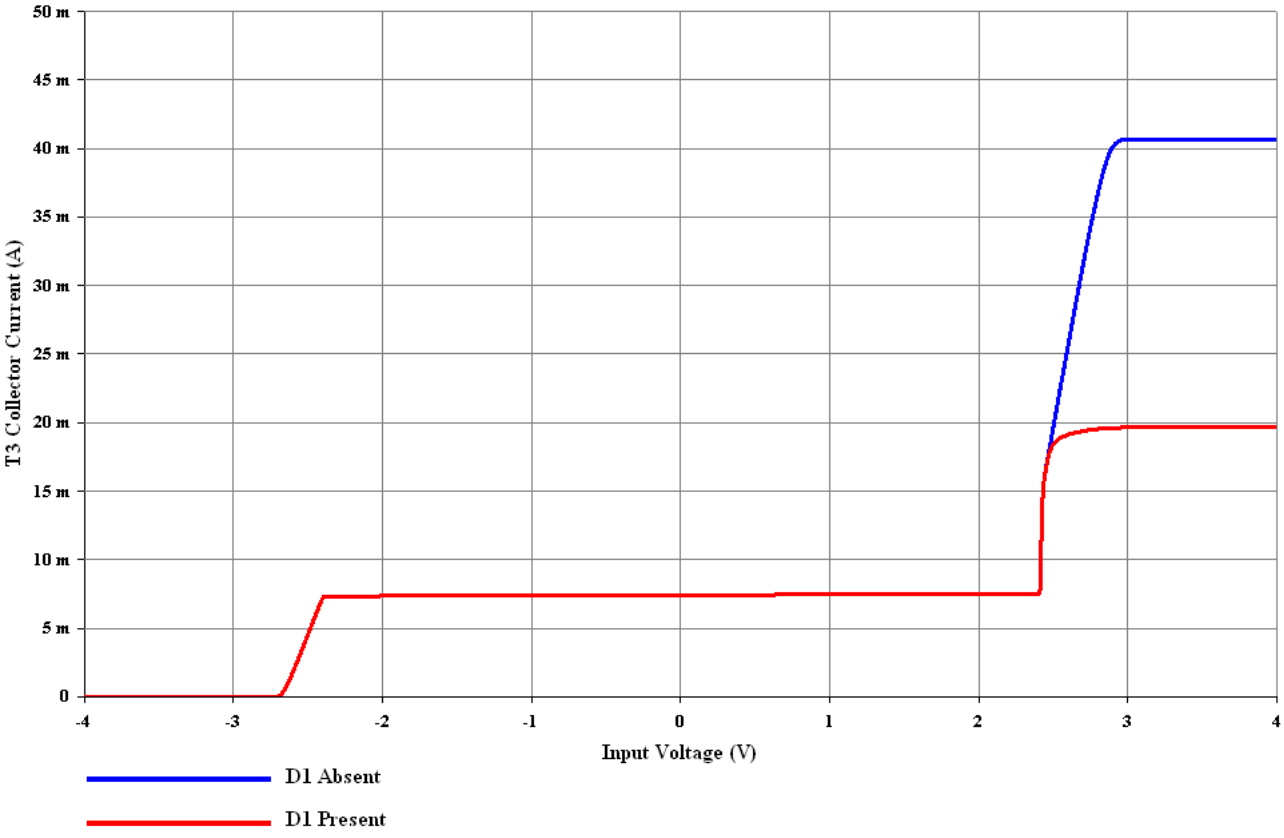


Figure 43. Diode D1 reduces the overload voltage across R8 during positive clip by nearly 50%. This, in turn, causes an equivalent reduction in T3's overload current.

Slew Overload Characteristics of the DCDS Topology

While booster capacitor $\mathbf{C_b}$ (**fig. 29**) only induces push-pull action in the generic topology at high frequencies, the DCDS arrangement is universally considered to stimulate such action at all frequencies of interest. This is conceptually attractive since residual TIS non-linearity in the orthodox topology of **figure 1** is predominantly second harmonic, of which push-pull action should provide cancellation.

Additionally, the DCDS is also thought to eliminate the rather inelegant slew rate asymmetry to which to the Thompson topology is subject as it is presumed that push-pull action provides more than enough current to charge and discharge capacitance at the TIS's collector. That this is not entirely true may be gleaned from the slew characteristics of **figure 46**. Even in the absence of diode **D2**, the DCDS arrangement can only manage +61.3V/uS and -48.9V/uS with the modified double-pole compensation network of **figure 34**.

Negative slew rate falls well short of the theoretical -67V/uS available, and is significantly inferior to that achieved by the Thompson topology (**fig. 35**). This is because a significant amount of tail current that would otherwise service **C1** is wasted in developing the voltage across **R2** required to forward-bias **T4** (**fig. 44**).

Conversely, positive slew rate (**fig. 45**) is defined when **T1** is turned off, and the potential drop across **R2** equals that across **R3**. Assuming the TIS can source all the current required by **C2**, then this limit is only reached when the current sunk by **R2** through **C1** equals the first-stage's tail current (~4mA).

In other words, the current (shunt) applied minor negative feedback loop around **T4** forces **R2** to sink current from **C1** as **T1** is turned off and the output slews positive. Accordingly, the voltages across **R2** and **R3** are in phase, and increase to nearly twice their quiescent values (~2.5V).

Since the increase in the base-emitter voltages of **T3** and **T4** is relatively small, the voltage across the second stage tail resistor **R8** increases nearly three-fold. As a result, second stage tail current peaks at over 40mA; this is well in excess of that required to drive the compensation network.

The trivial deficiency in positive slew rate occurs because both second-stage transistors **T3** and **T4** are driven into saturation, causing the **T4** to siphon current away from **C2**; ideally **T4** should turn off as the amplifier slews positive.

The obvious but unnecessary and misguided temptation to "protect" **T4** during negative clipping overload by using **D2 (fig. 44)** should be resisted. This is because **D2** merely siphons off current from **T1**'s collector that would otherwise drive the compensation network. This accomplishes precisely nothing in the way of protecting **T4** which, as previously established, needs no such protection; negative slew is needlessly reduced by up to 10% **(fig. 46)**.

Note that **D1** is only forward-biased during positive clipping, and remains off during ***unclipped*** positive slew overload **(fig. 45)**. This is because, during the later process, **R2** sinks as much current through the compensation network as is required to make the potential drop across **R2** equal to that across **R3**.

Limiting dissipation in the cascode transistor $\mathbf{T_{C1}}$ during positive slew overload is not strictly necessary as the transistor can sustain higher power at ultrasonic frequencies. However, such protection may be provided at no extra cost, for both positive slew and/or positive clip overload, by merely reconnecting the diode in series with both resistors (**fig. 47**).

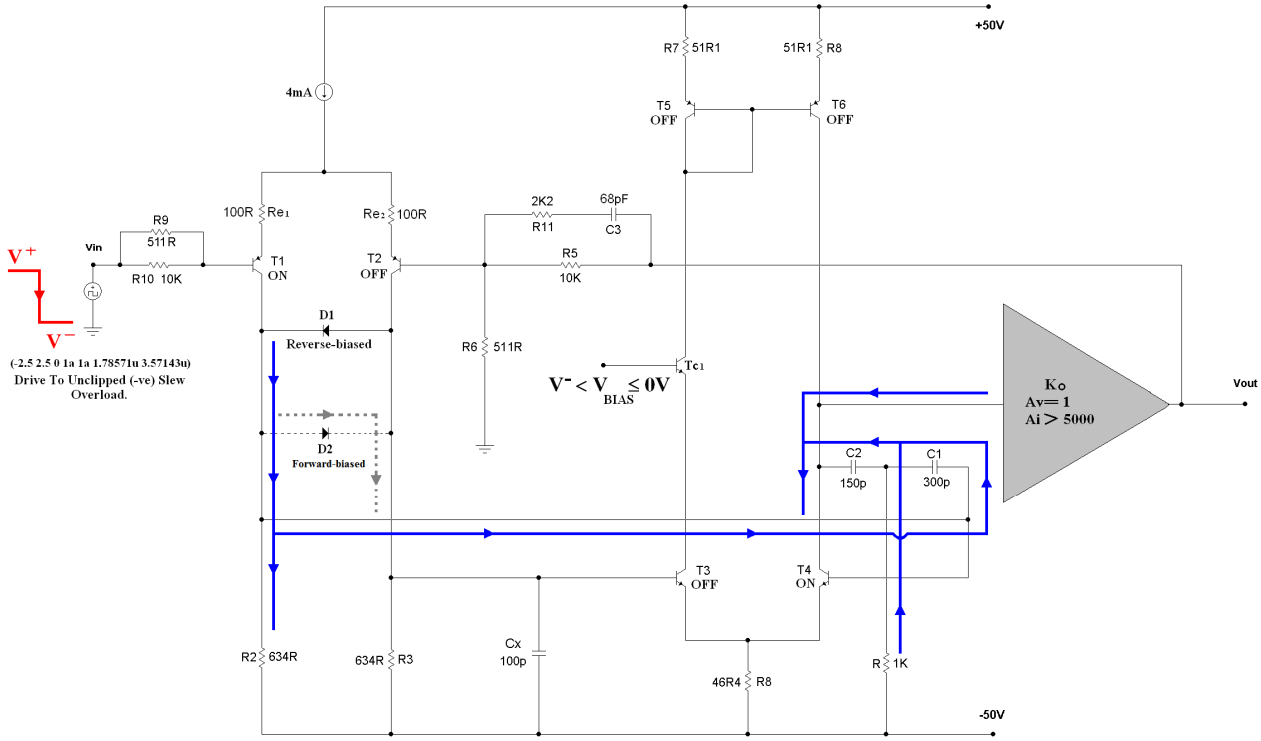


Figure 44. For negative slew, first-stage tail current is wasted in developing the voltage across R2 required to forward-bias T4.

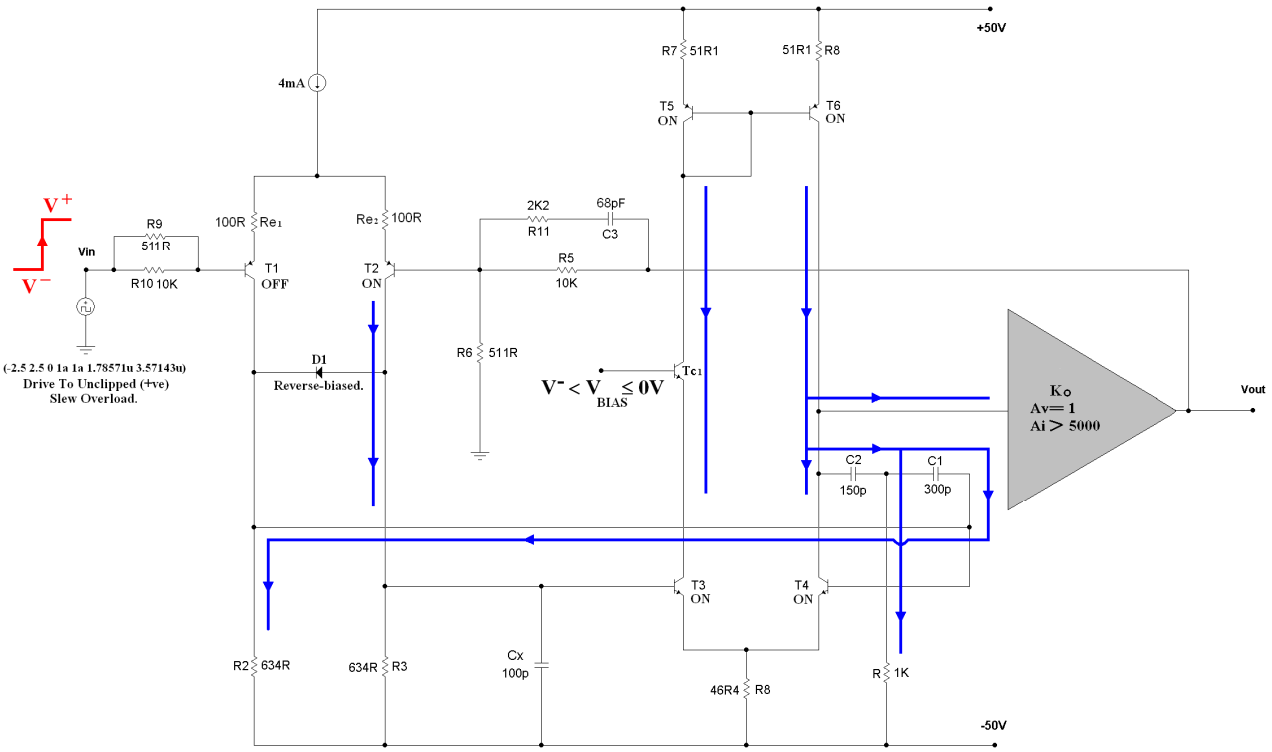


Figure 45. During positive slew, the voltage dropped across R2 by the current sourced from the compensation network drives T4 into saturation, causing it to siphon current away from C2.

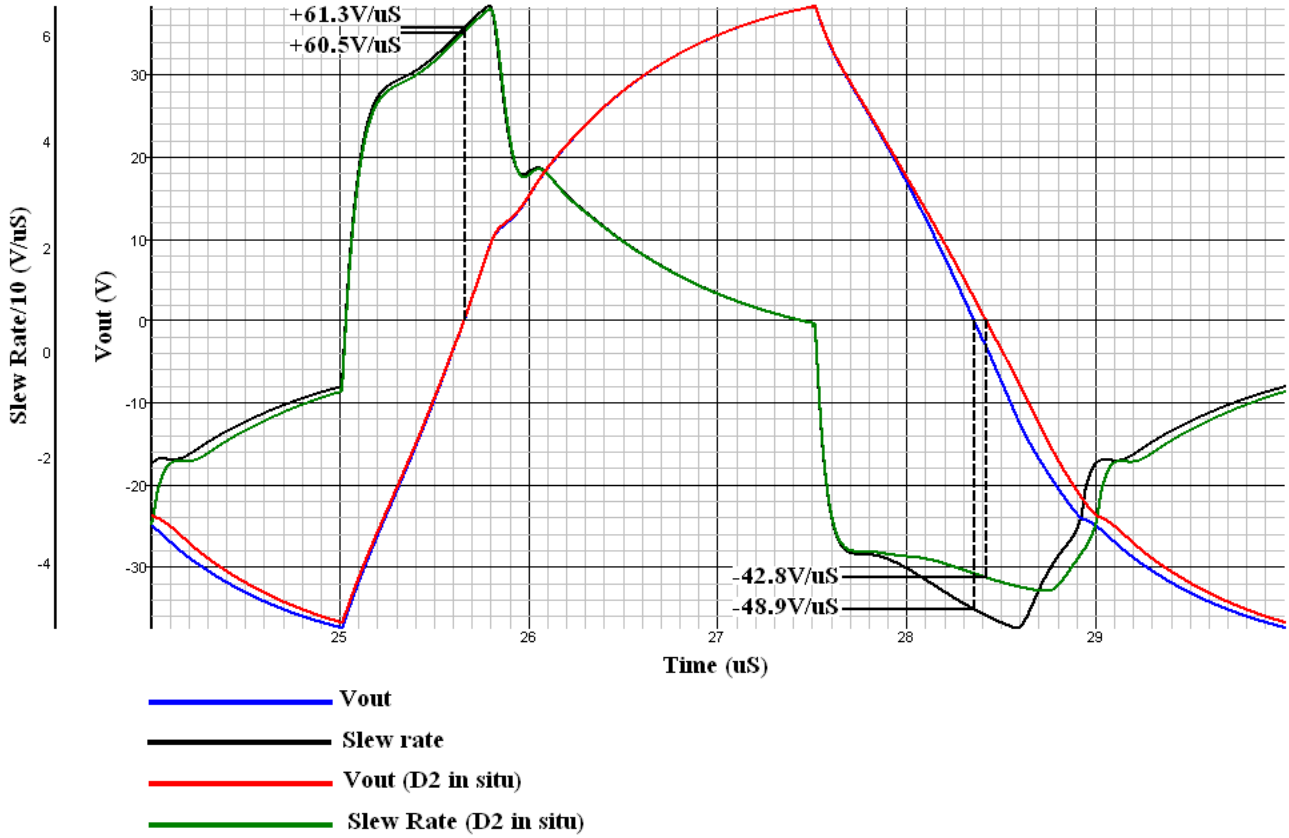


Figure 46. The relatively poor negative slew rate is further compromised by D2 which merely siphons off current from T1's collector that would otherwise drive the compensator.

The diode-connected transistor **T7** permits a reduction in the value of resistors **R2** and **R3** without changing the circuit's nominal quiescent conditions. Since voltage change with current across the diode is insignificant, and the voltage drop across a reduced **R3** during positive clipping and slewing overload (which involves both **R2** and **R3**) is necessarily diminished, a net decrease (of the order of 20%-50% depending on component values) in overload voltage across **R8** is obtained.

This yields a corresponding reduction **(fig. 48)** in **T3**'s overload collector current. Thus, while diode **D1** (**fig. 47**) can only reduce dissipation in the cascode transistor during positive clipping overload, series diode **T7**, which is forward biased during both overload conditions, additionally effects such a reduction for positive slew overload.

The circuit of **figure 47** also possesses the advantage that the voltage drop across **T7** accounts for much of a saturated **T4**'s base-emitter voltage during negative slew. Since (to a first approximation) the voltage drop across diode **T7** is not linearly related to the current through it, slightly less first-stage tail current is wasted in generating **T4**'s base-emitter voltage, and is used instead to service the demands of the compensation network. Thus a small increase in negative slew (of the order of 5%-10%) is realised by the circuit of **figure 47** relative to that of **figure 44**.

The thermal stability of second stage quiescent current may be significantly improved by mounting **T7** as close to **T3** and **T4** as possible. Without **T7**, idling and overload currents may vary about their nominal values by as much as 25%. Using a diode-connected transistor instead of an ordinary diode facilitates close coupling; ideally, these transistors should be bonded together with cyanoacrylate adhesive.

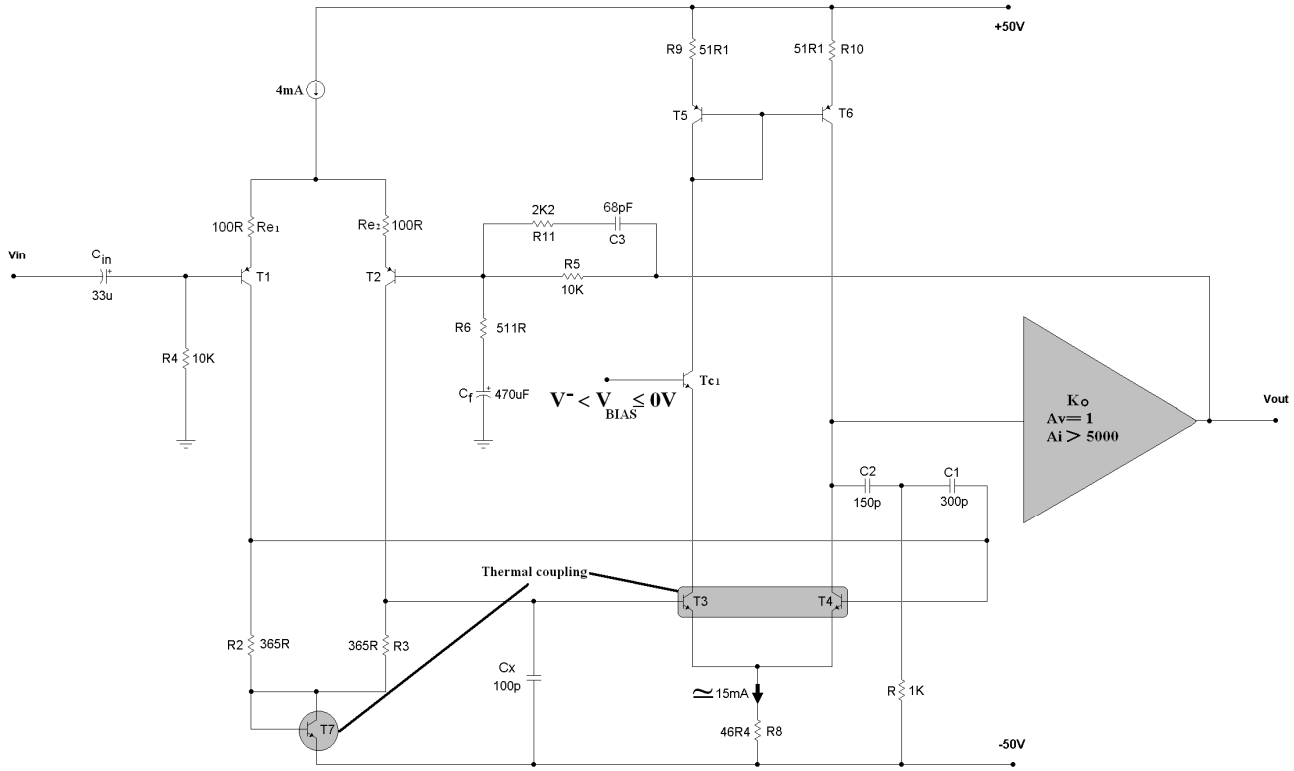


Figure 47. Diode T7 permits R2 and R3 to be reduced. This in turn means the voltage drop across R8 during positive clip and/or slew is also reduced.

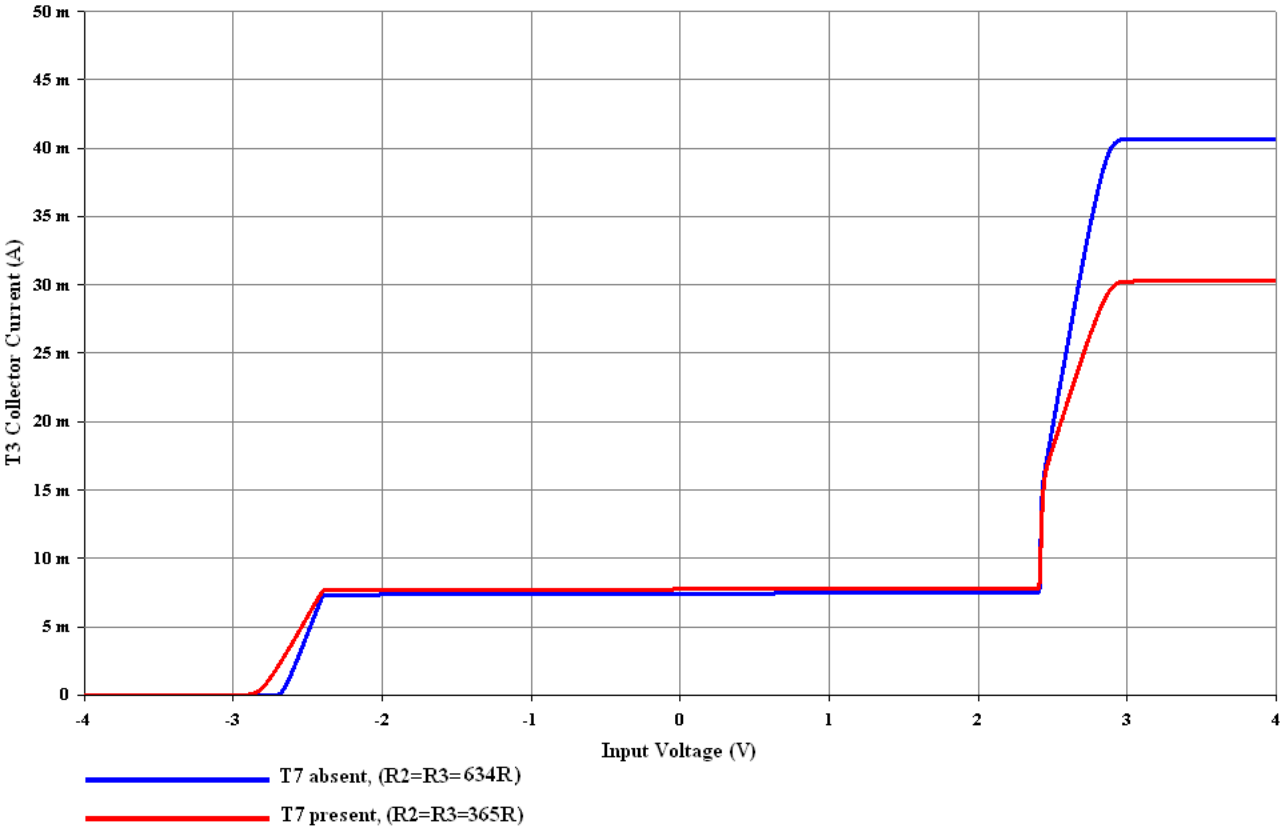


Figure 48. Reduction in positive clip-overload current in T3. A similar reduction is also sustained during positive slew overload.

However, connecting a diode in series with each of the differential stage's collector resistors constitutes an altogether more effective and elegant solution **(fig. 49)** as it facilitates the more straightforward bonding of **T3** to **T8**, and **T4** to **T7**. Additionally, the four transistors should be clustered as close together as possible on the PCB. The excellent 'E-line' packaged medium power devices from **Zetex**® lend themselves particularly well to this task.

Obviously the potentially messy business of bonding four discrete transistors together may be avoided altogether by having them on the same monolithic substrate. However, obtaining such a device with the requisite power handling and comparable electrical characteristics is likely to be difficult; the relative cost is also likely to be unattractive.

The common-base transistor $\mathbf{T_{C1}}$ is often biased by merely connecting its base directly to circuit common, which minimises component count. This is acceptable if well regulated supply rails of modest magnitude ($|\mathbf{V_{Rail}}| << 100\mathbf{V}$) are envisaged. However, using such an invariant bias reference is not recommended for high-power units with unregulated DC supplies as this makes the second stage more vulnerable to failure due to primary supply surges.

Therefore, $\mathbf{T_{C1}}$**'s** bias voltage is bootstrapped to the negative supply rail so that any significant variation of the DC supply is directly impressed on the reference voltage. This is simply realised by a diode string referred to the negative supply rail **(fig. 49)** which effectively ensures that the voltage across **T3** remains constant in the face of non-ideal supply rail fluctuations; PSRR with respect to the negative supply rail is improved by at least an order of magnitude at ripple frequency.

The problem with the cascode is that $\mathbf{T_{C1}}$ now has to be a medium power device, capable of dissipating at least 2W (for example, Fairchild's **KSC2690A**) if its long-term reliability is to be guaranteed. The increased cost and component count may be difficult to justify in view of the fact that there is no appreciable advantage in respect of linearity relative to the simple $\mathbf{R7/C_f}$ combination of **figure 36**.

The latter possesses the elementary but invaluable property that the voltage across **T3** decreases as the current through it increases and conversely—precisely what is required to minimise dissipation. Moreover, with this approach, neither diode clamp **D1** (**fig. 44)** nor series diodes **T7** and **T8** (**fig. 49)** are required.

Nevertheless, by eliminating $\mathbf{C_f}$ from the signal path, the cascode was found to confer a substantially cleaner transient response. The existing diode string may also be used to bias a second common-base transistor $\mathbf{T_{C2}}$ in series with **T4**'s collector which, in contrast with $\mathbf{T_{C1}}$, need only be of the 'small signal' variety.

The resulting cascode TIS eliminates distortion generated by the non-linear variation with voltage of **T4**'s collector-base parasitic capacitance. Additionally, provided the output stage is of sufficiently high input impedance (preferably with current-gain $\mathbf{A_i} > 2\times10^5$), the effective impedance at the output of the cascode TIS is increased.

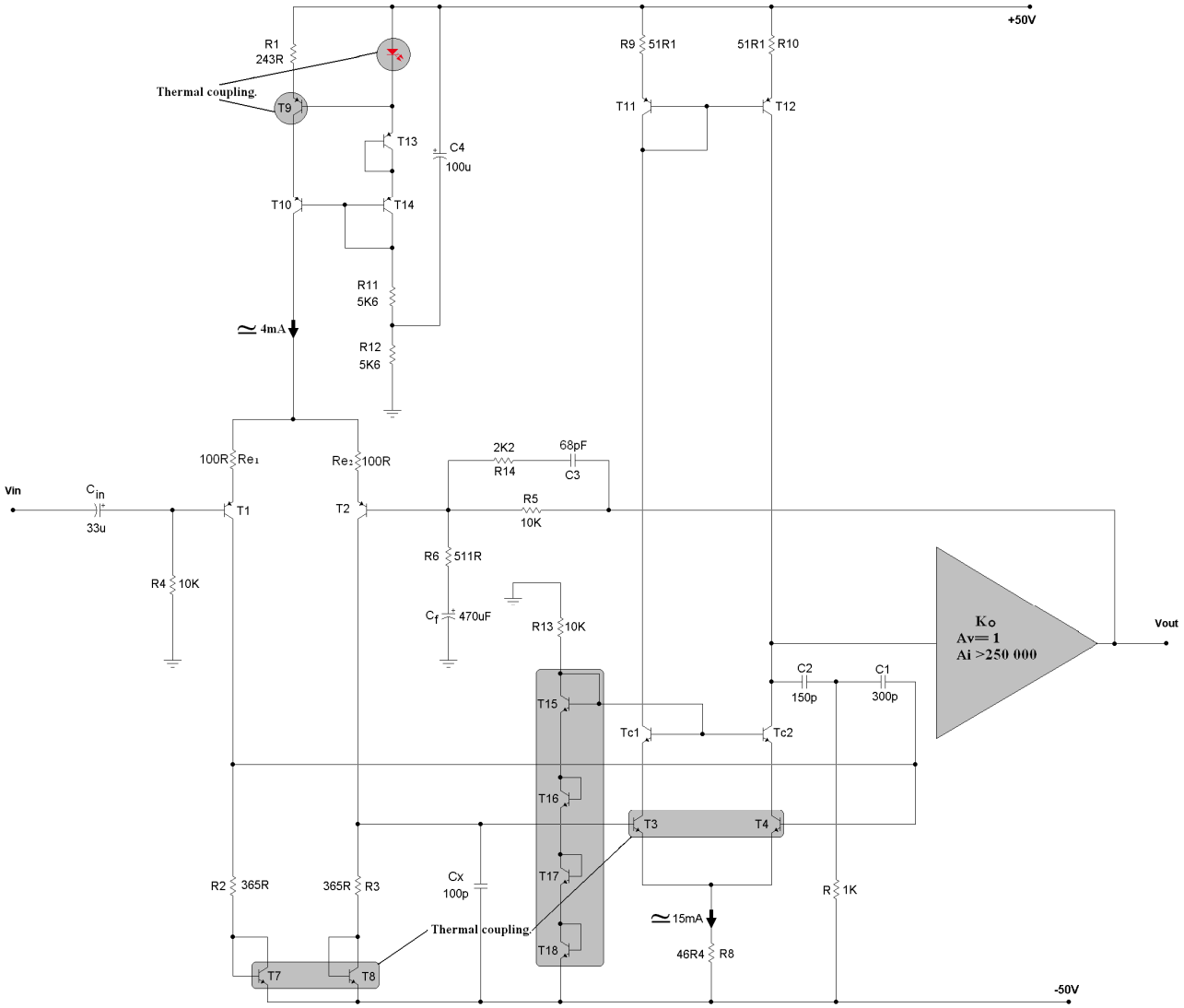


Figure 49. The cascode is biased from the negative supply rail so that the voltage across T3/T4 remains constant in the presence of anomalous voltage variations of the supply rail.

Since local open-loop transimpedance gain is approximately given by the product of transistor current gain and the effective impedance at the TIS's collector, then increasing the impedance at the second stage's output node produces an equivalent increase in the TIS's forward-path gain (**equation 10**). This enhances minor-loop transmission through the compensator, stimulating a significant improvement in TIS linearity [21]. Simultaneously, the increase in overall forward-path gain, *pro rata* with the impedance at $\mathbf{T}_{C2}$'s collector, at frequencies preceding the dominant pole pair ultimately improves the gain block's low frequency closed-loop linearity and PSRR.

The desired current gain may be realised by driving the output stage with a cascade of two cross-coupled complementary emitter followers (**fig. 50**). A further advantage of this arrangement is that the first pair of complementary drivers, **T1** and **T2**, operate in class-A, even when the output stage is biased to operate in class B or AB, provided their cross-coupling resistor, $\mathbf{R}_{cx}$, is made sufficiently small (typically $R_{cx} \leq 1K$).

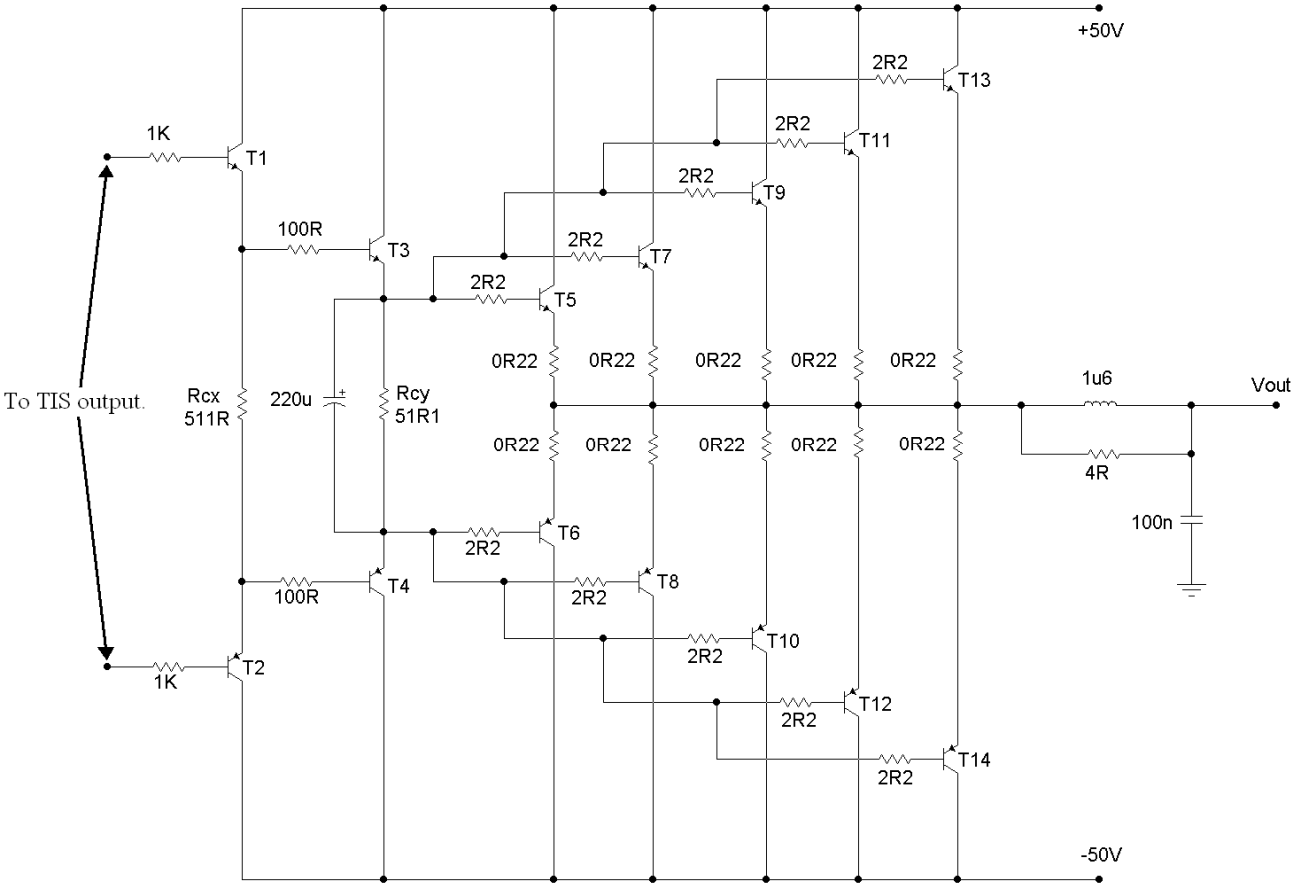


Figure 50. A practical high current output stage (with protection circuitry omitted) in which each transistor in the first pair of drivers (T1 and T2) is biased to conduct throughout the cycle by selecting a sufficiently small cross-coupling resistor (511 Ohms in this case); this virtually eliminates the non-linear loading of the output stage on the TIS. The base ballast resistors provided for each transistor inhibit local parasitic oscillation in the output stage.

Causing the first pair of drivers to conduct throughout the cycle effectively isolates the cascoded TIS from the non-linear loading of the class B (or AB) output stage. Thus, the dedicated class-A emitter follower recommended by D. Self [6] for this purpose is made redundant.

The use of resistive biasing for the input stage in many published designs, such as Hitachi's, means that first stage quiescent current varies with positive supply ripple and extrinsic common mode stimuli. Such poor common mode and power supply rejection also affects the second stage, since its idling current is established by the voltage dropped across first stage collector resistors, **R2** and **R3**.

An active current source for the input stage is therefore essential. For maximal thermal stability of quiescent current, a temperature compensated current source in the form LED-biased transistor **T8** is recommended **(fig. 49)**; the LED should be mounted as close to **T9** as possible.

Transistors **T9** and **T10** together constitute a cascode, which effectively eliminates Early effect in **T9**. This current source gives an improvement in +PSRR of the order of 18dB across the audio band compared to the purely resistive current source **R1** of **figure 36**.

Primary Limitations of the DCDS Topology

The minor feedback loop simultaneously stabilises the global feedback loop and enhances second-stage linearity. Regrettably, it also provokes a fundamental flaw in the conduct of the second stage for normal (unclipped) AC output.

With single-pole compensation (established by simply setting $\mathbf{R} \to \infty$ in the double-pole compensator) the shunt applied negative feedback loop around **T4** forces **R2** to sink current from capacitor **C1** virtually equal to that sunk by $\left(\mathbf{R}3//1/\mathbf{sC}_{\mathbf{X}}\right)$ as the output swings positive. This mechanism opposes **T1**'s attempt to drive its own collector low in response to positive-going stimulus. This is also manifest in the circuit's operation during slew limiting (**fig. 45**).

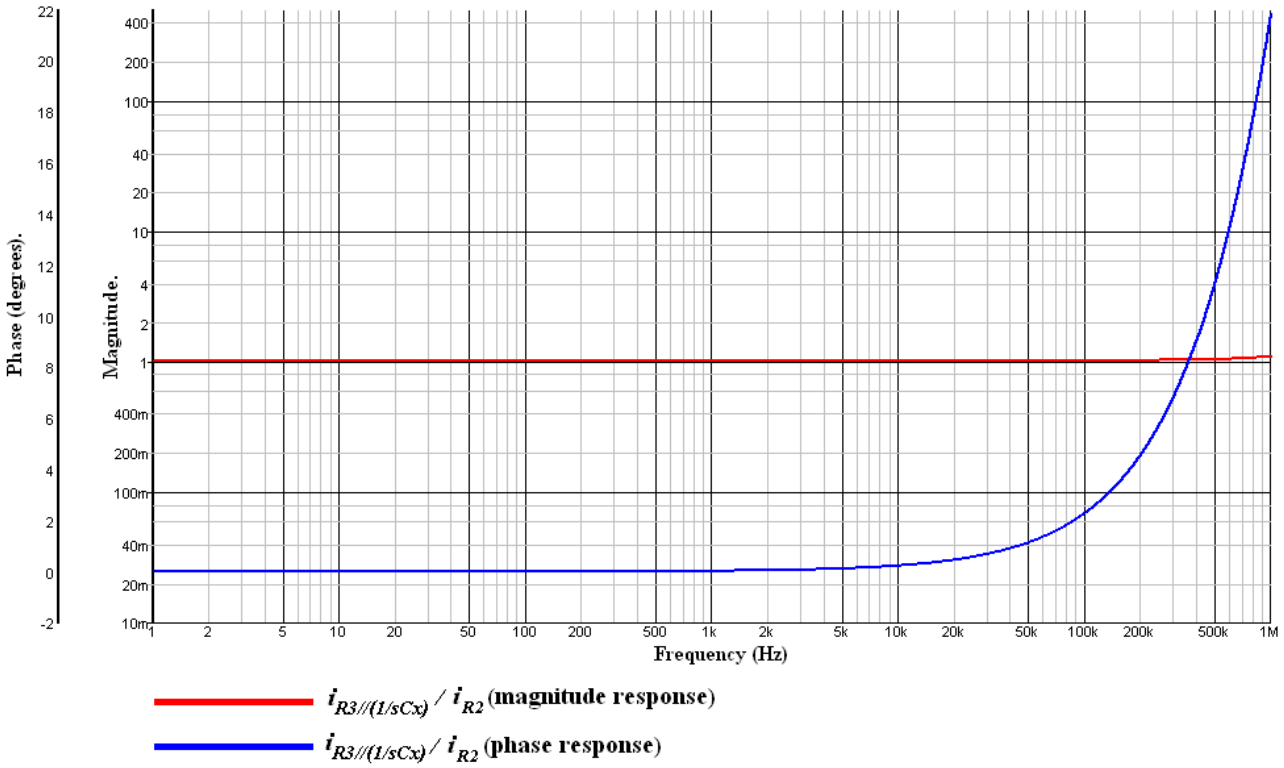
In other words, resistive load **R2** is the means by which **T1**'s collector is pulled high by the compensation network as the voltages across $\left(\mathbf{R}3//1/\mathbf{sC}_{\mathbf{X}}\right)$ and the TIS's output swing positive, and conversely. Accordingly, although **T1** and **T2** collector currents are $180^{\mathbf{o}}$ out of phase, the currents in, and therefore voltages across **R2** and **R3** are in phase at all frequencies of interest (**fig. 51a**), whereas they are required (and apparently universally assumed) to be $180^{\mathbf{o}}$ out of phase to stimulate push-pull action in the second stage. This common-mode mechanism is *intrinsic* to this topology, as it is completely independent of external (or *extrinsic*) common-mode stimulus.

This would be of little import were **R8** an ideal current sink, delivering a constant current irrespective of voltage variation across it. However, the relatively large common-mode voltage across **R2** and **R3** appears directly across resistor **R8**, inducing an increase in second-stage tail current for positive input voltage swings, and conversely for negative voltage vacillations. In other words, the shunt feedback loop about **T4** makes its input impedance much lower than **T3**'s, with the net result that the second stage appears like an emitter-follower (with respect to **R8**) driven from **T2**'s collector.

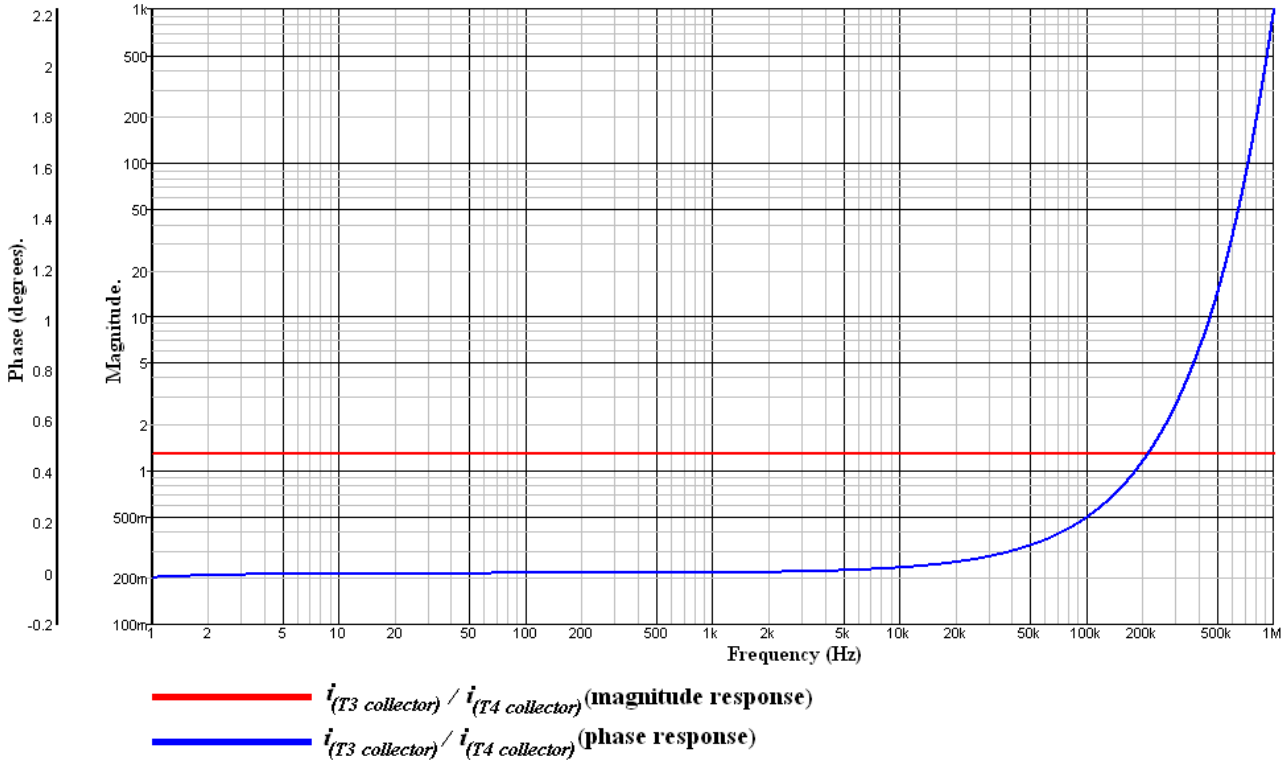
Consequently, resistor **R8**'s integrity as a constant current sink is compromised to such an extent that push-pull action in the second stage is completely overwhelmed. Therefore, contrary to virtually universal opinion, **T3** and **T4**'s collector currents are in phase (**fig. 51b**), and the much vaunted cancellation of even-order harmonics in the second stage does not occur in fact.

Reconnecting **R=1K** restores double-pole compensation, and engenders a marked improvement in performance. At low and medium audio frequencies $\left(\leq 1\mathbf{KHz}\right)$ the current sunk by **R2** from **C1** is reduced by more than 100 times. The common-mode voltage across **R2** and **R3** is reduced by the same amount, such that the currents (and therefore voltages) across **R2** and **R3** are now roughly $180^{\mathbf{o}}$ out of phase (**fig. 52a**).

In other words, **T4**'s input impedance becomes roughly equal to that of **T3** as minor loop transmission about **T4** approaches zero at low frequencies. Thus, in addition to increasing loop transmission, the double-pole compensator facilitates push-pull action in the second stage across much of the audio band (**fig. 52b**).

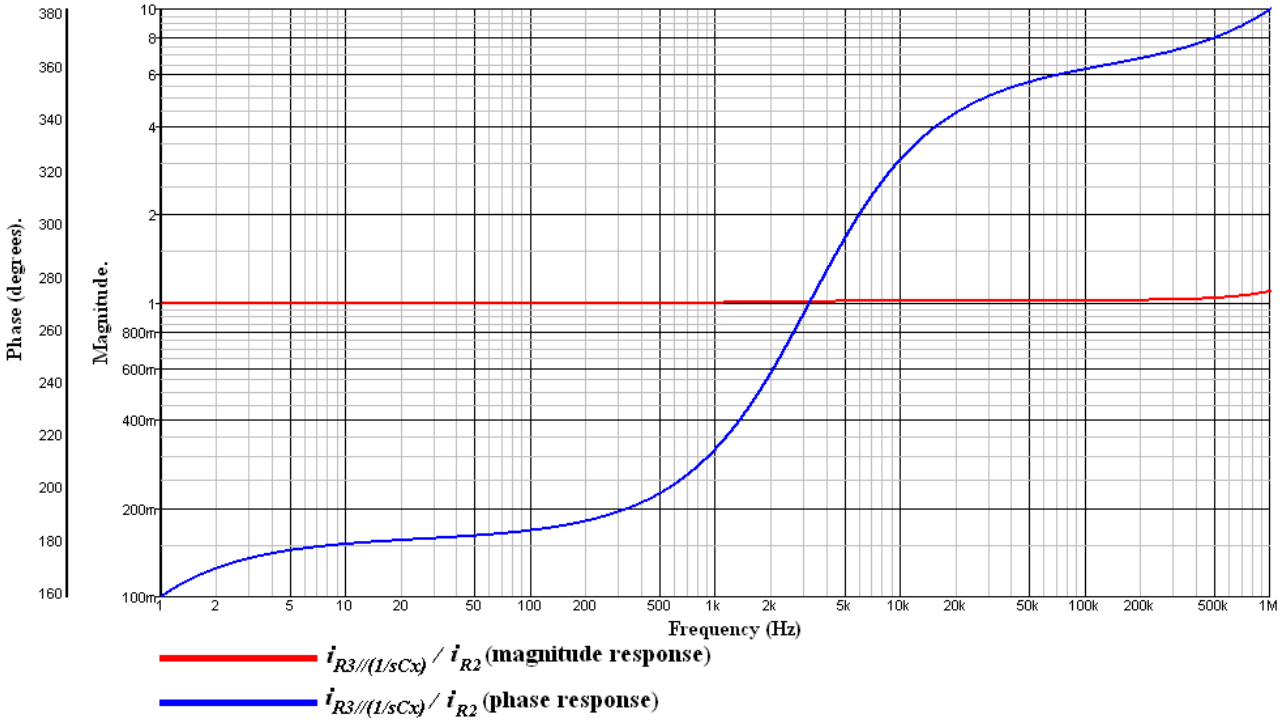


(a)

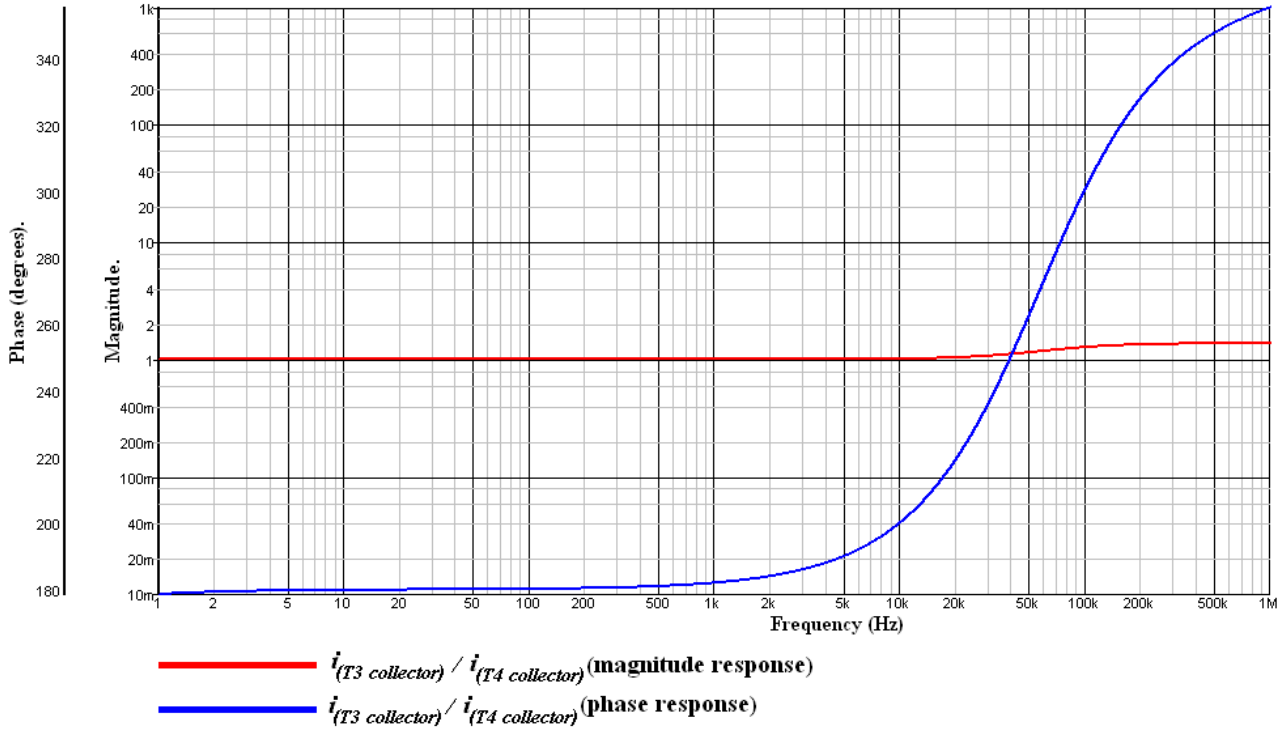


(b)

Figure 51. The currents in, and therefore voltages across R2 and R3 are in-phase across the audio band (a). Consequently, T3 and T4's collector currents are also in-phase and the ratio of their magnitudes deviates appreciably from unity (b).



(a)



(b)

Figure 52. The double-compensator reduces the current sunk by R2 from C1 by several orders of magnitude (a). This facilitates push-pull action in the second stage across much of the audio band (b).

Introducing the TAS Current Mirror

Unfortunately, push-pull action invoked by using double-pole compensation only usefully extends to mid-band frequencies $(\leq 1\mathbf{KHz})$, where major loop-transmission is already substantial. Accordingly, hardly any benefit may be attributed to this mechanism in respect of reduced even-order distortion, particularly at high audio frequencies. Clearly what is required is some means of reducing the common-mode voltage component across **R8** to insignificance over an extended frequency range.

This may be achieved by maintaining a relatively constant voltage across **R8**, irrespective of the magnitude of current swings through the compensation network, and/or providing **T1** with an active collector load whose current bears no direct relationship to the voltage across it. Such a load provides the desired capability of sinking current from **C1** without an attendant increase in voltage across it.

Ultimately, the AC voltage across **R3** is responsible for generating the in-phase voltage component across **R2**. Thus, in principle, if transistor **T7** (**fig. 49**) were employed as an active collector load for **T1** instead of **R2**, and configured as an *inverter* (common-emitter cell) by connecting it's base to **T2**'s collector, then the voltage across **R3** should counteract the common-mode component at **T1**'s collector.

Indeed, the fact that the currents in **R2** and **R3** are in phase suggests that such an inverter may be realised by rearranging these resistors together with transistors **T7** and **T8** into a current mirror (**fig. 53**), which possesses this characteristic in the sense that its collector currents are also in phase. This appears to be the primary design rationale in Texas instruments' **OPA627/637** operational amplifiers.

Analogous to **figure 47**, the biasing requirements of second stage transistors, **T3** and **T4**, are accommodated by diode **T19**. However, in contrast to **figures 47** and **49**, the base-emitter voltages of the current mirror now maintain a relatively constant voltage drop across **R8**. Moreover, transistor **T7** is now capable of sinking current from **C1** without the limitation imposed by the inevitable accompanying voltage drop occasioned by a passive load.

Although replacing resistive loads with a current mirror doubles first-stage transconductance in the generic topology, this is not the case in the DCDS, whose transconductance with a current mirror is identical to that obtained with purely resistive loads, **R2** and **R3**. This is because with the DCDS, unlike the generic topology, a double-ended output is demanded of the input stage regardless of the nature of the collector loads.

Nevertheless, the active load increases the TAS's output impedance (with respect to **T4**'s base) which maximises current transfer from the differential pair to the TIS by reducing inter-stage loading to insignificance; consequently, the circuit's forward-path gain, at frequencies preceding the dominant pole pair, more than doubles. On the other hand, the forward-path unity-gain frequency f_u remains unchanged, since this is only a function of the ratio of first stage transconductance to the series combination of **C1** and **C2 (equation 19)**.

As previously established, the current mirror forces nominal equality of quiescent collector currents in the input cell, which minimises the amplifier's DC output offset, and promotes the cancellation of even-order harmonics in that stage. The available *symmetrical* current sourced and sunk at **T4**'s base also doubles, which virtually eliminates the deficiency in negative slew rate otherwise obtained with passive first-stage loads.

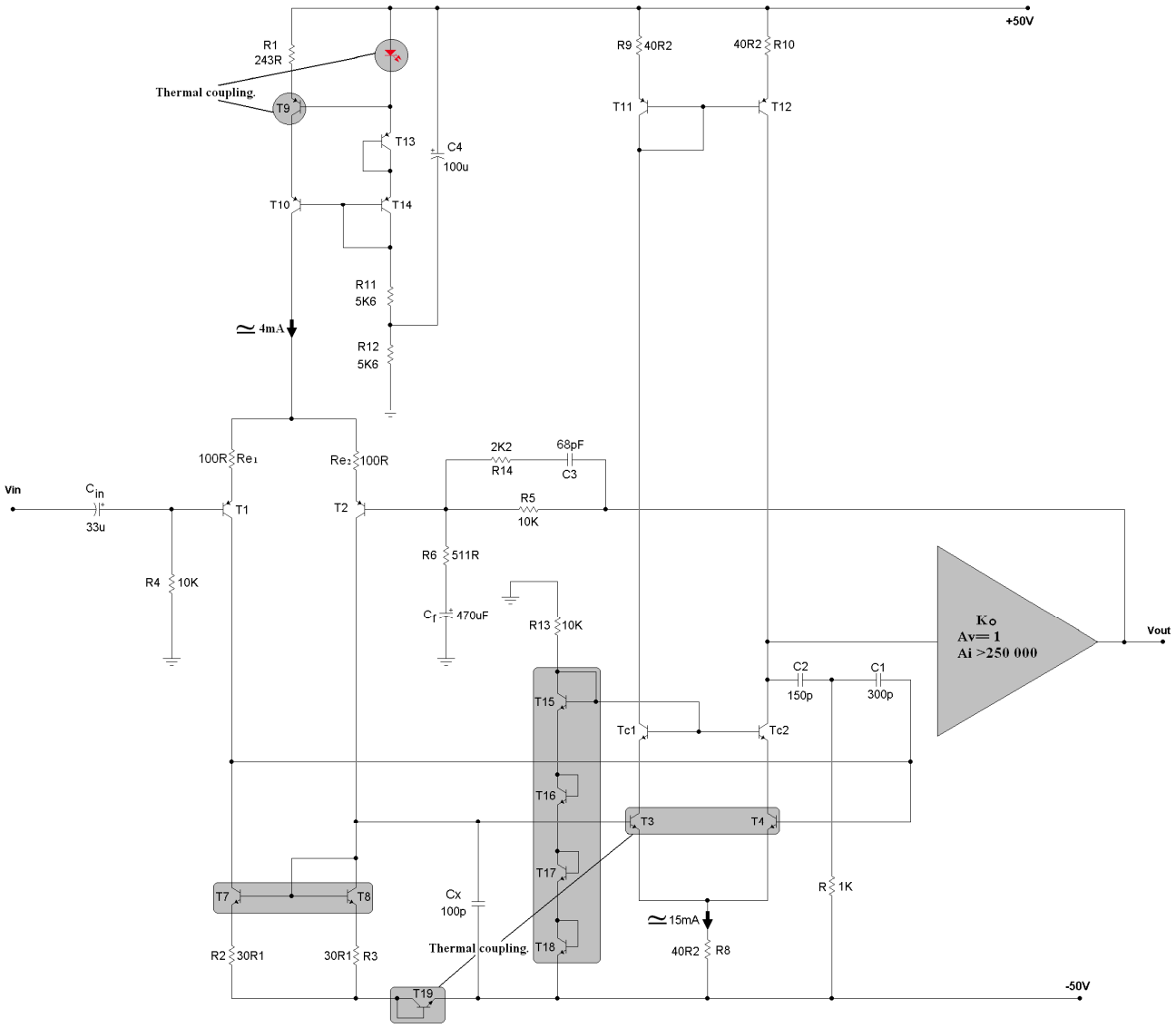


Figure 53. Transistors T3, T4, and tail resistor R8 are effectively biased by two diode voltage drops generated by T7, T8 and T19. Provided R2 and R3 are kept small, the common mode voltage across R8 is reduced to relative insignificance.

Power dissipation during positive clipping overload is significantly reduced as **T3**'s collector current is clamped to a little more than the second stage's nominal tail current. Additionally, the trivial deficiency in positive slew rate, due to **T4** siphoning current away from **C2**, is virtually abolished as **T4** is no longer driven in saturation. Yielding to the obvious desire to replace transistors **T7**, **T8** and **T19** with a Wilson mirror gives no appreciable improvement in linearity.

The new function of resistors **R2** and **R3** is merely to promote equality of collector currents in the mirror by swamping differences in its base-emitter voltages. These resistors must be kept as small as possible as their common-mode voltage again degrades push-push pull action in the second stage by appearing directly across **R8** (**fig. 54**); selecting **R2=R3=150R**, for example, causes significant degradation at ultrasonic frequencies where push-pull action would otherwise make more efficient use of second-stage quiescent current during positive slew.

Predictably, the deterioration is more pronounced with single-pole Miller compensation, with **R2=R3=100R** virtually eliminating push-pull operation at all frequencies of interest; typically, the voltage drop across **R2** and **R3** should not exceed $0.1\mathbf{V_{BE}}$. Provided **T7** and **T8** are thermally coupled, the residual difference in their base-emitter voltages may be deemed negligible.

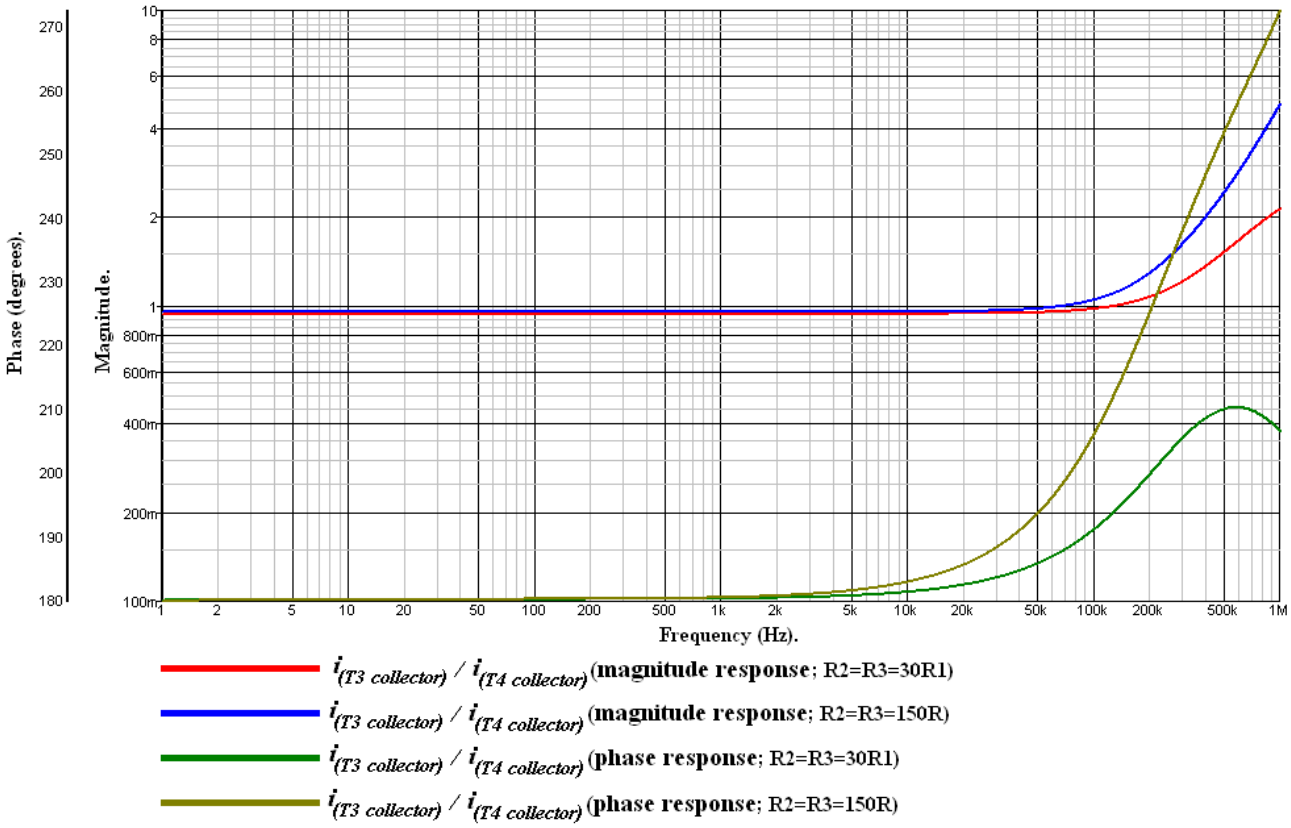


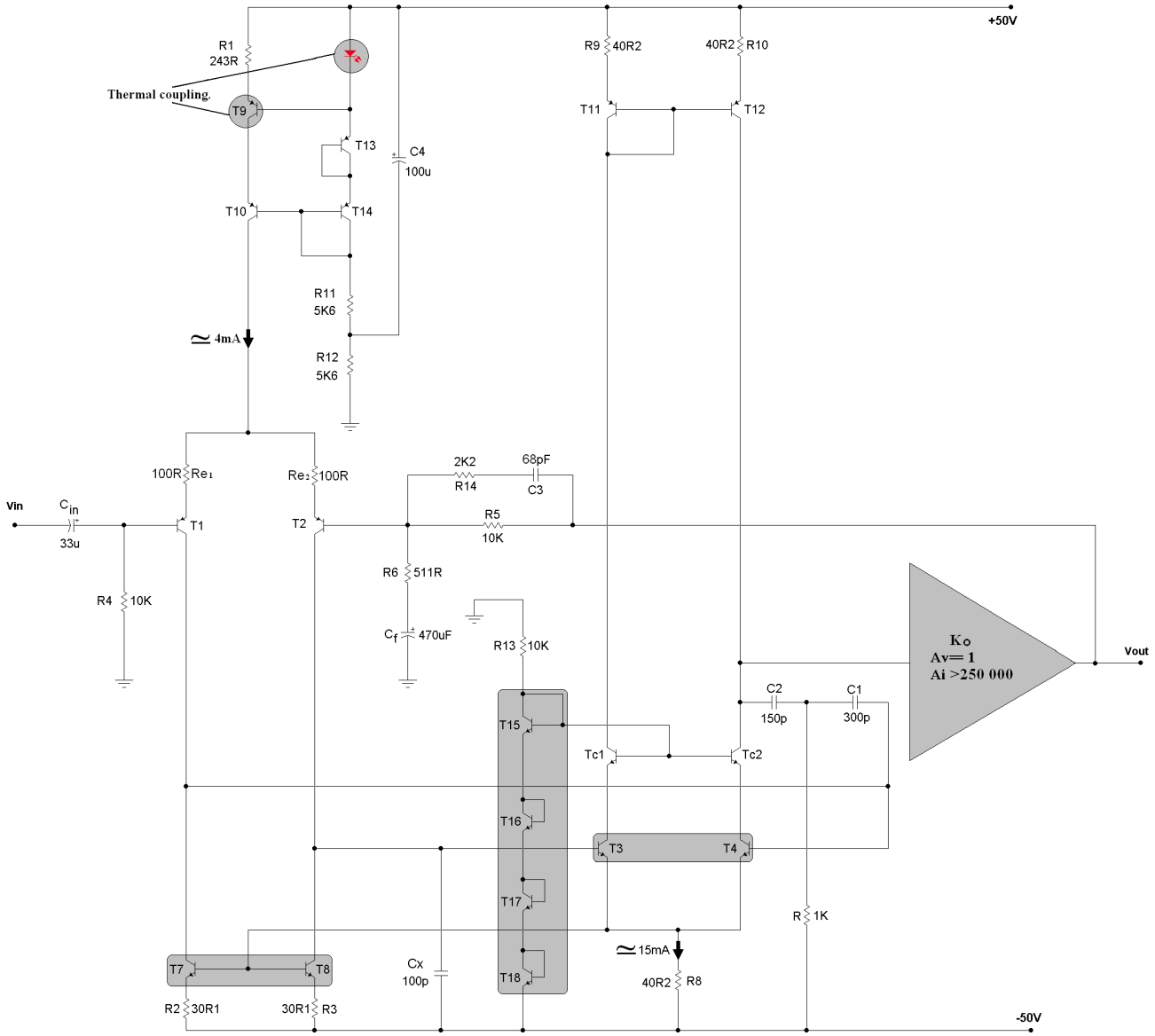
Figure 54. A seemingly trivial increase in the value of R2 and R3 (with double-pole compensation) causes a significant deterioration in push-pull action at high frequencies as the phase-shift between second-stage collector currents strays from the ideal 180^{o}. This effect is much more pronounced with single-pole Miller compensation.

Since the shunt feedback loop about **T4** causes the second stage to appear like an emitter-follower driven from **T2**'s collector (with respect to **R8**), then further simplification may be obtained by using the voltage across **R8** to drive mirror devices **T7** and **T8** (**fig. 55a**). This is analogous to the so-called buffered Widler current mirror frequently used in monolithic designs (**fig. 55b**).

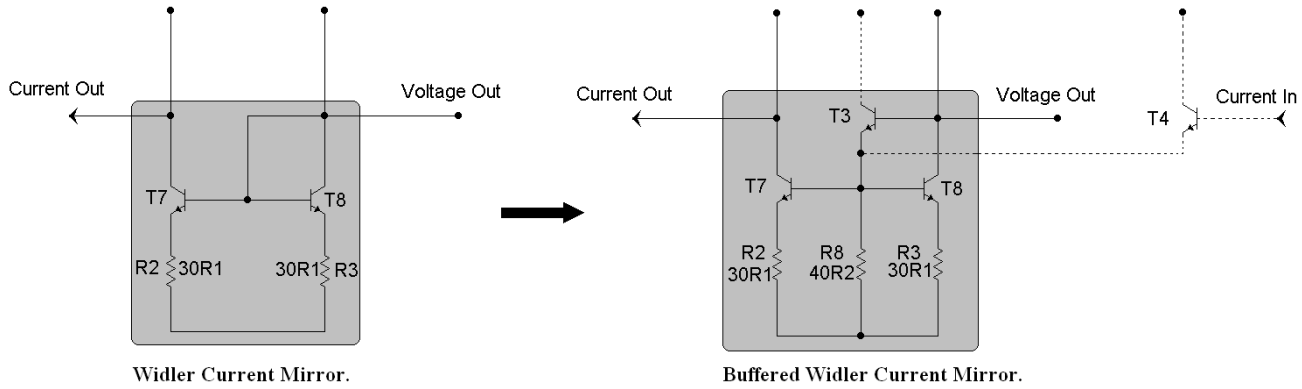
Because **T7**'s and **T8**'s base-emitter voltages now appear directly across **R8**, this arrangement possesses the significant advantage that second stage quiescent current stability is attained without requiring the inter-stage thermal coupling provided by **T19** in **figure 53**.

For *extrinsic* common-mode stimulus, **T1**'s and **T2**'s collector currents are in phase and, moreover, **T1**'s and **T7**'s collector currents are also in phase, which indicates that the voltage swing across the compensation network is negligible. Consequently, transistors **T7** and **T8** operate as independent current sinks, providing *common-mode feedback*[48] by pulling the input stage's collectors low for negative common-mode input voltage swings, and conversely. Note that in this case resistors **R2** and **R3** must also be kept small, otherwise they provide significant degenerative feedback by attenuating the net extrinsic common-mode voltage appearing across **T7**'s and **T8**'s base-emitter junctions.

Clearly this facility (common-mode feedback evoked by extrinsic common-mode excitation) is unavailable in the circuit of **figure 53**, or, indeed, in the Thompson topology of **figure 1**. Nevertheless, given an active current source for the input stage, common-mode gain may be considered negligible in this application. The arrangement of **figure 56** may be used in SPICE to confirm that the CMRR for both embodiments of the DCDS topology is trivially large, being in excess of 80dB across the audio band.



(a)



(b)

Figure 55. From the perspective of T7 and T8, the shunt feedback loop about T4 forces net voltage-follower action from the second stage with respect to T2's collector (a). This is analogous to the buffered current mirror (b) typically used in monolithic circuits to minimise collector current mismatch in the mirror due its own base current demands.

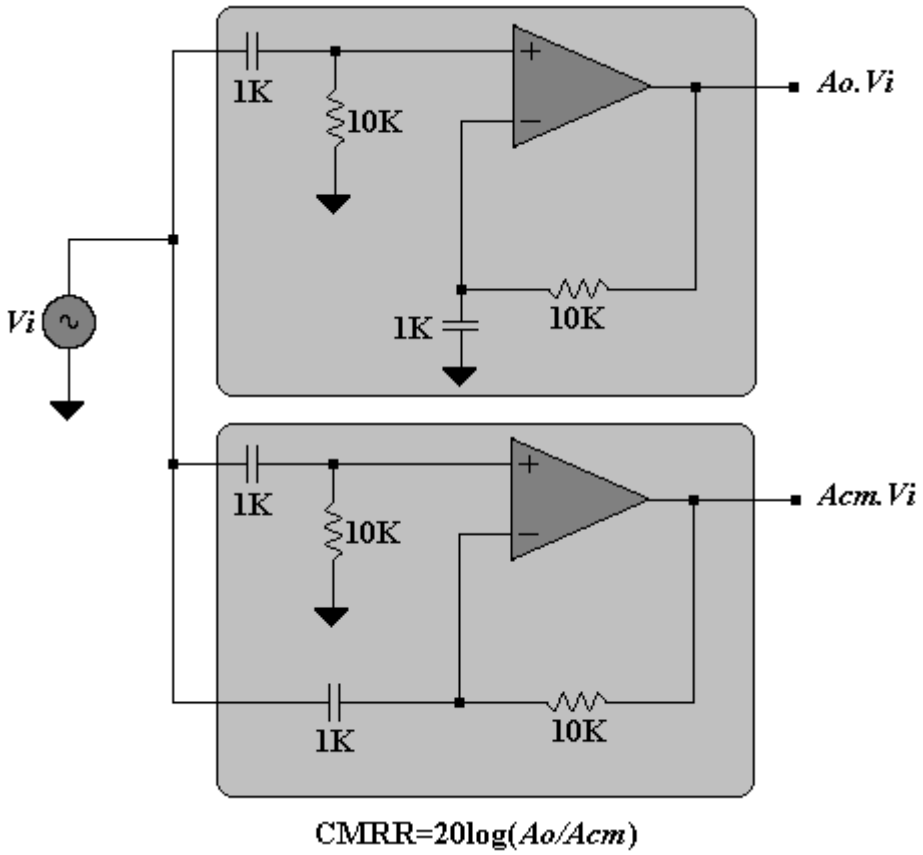


Figure 56. In this SPICE test arrangement, 100% DC negative feedback provided for each unit permits the evaluation of CMRR as a function of frequency without upsetting quiescent operating points.

Miscellaneous Practical Considerations and Enhancements

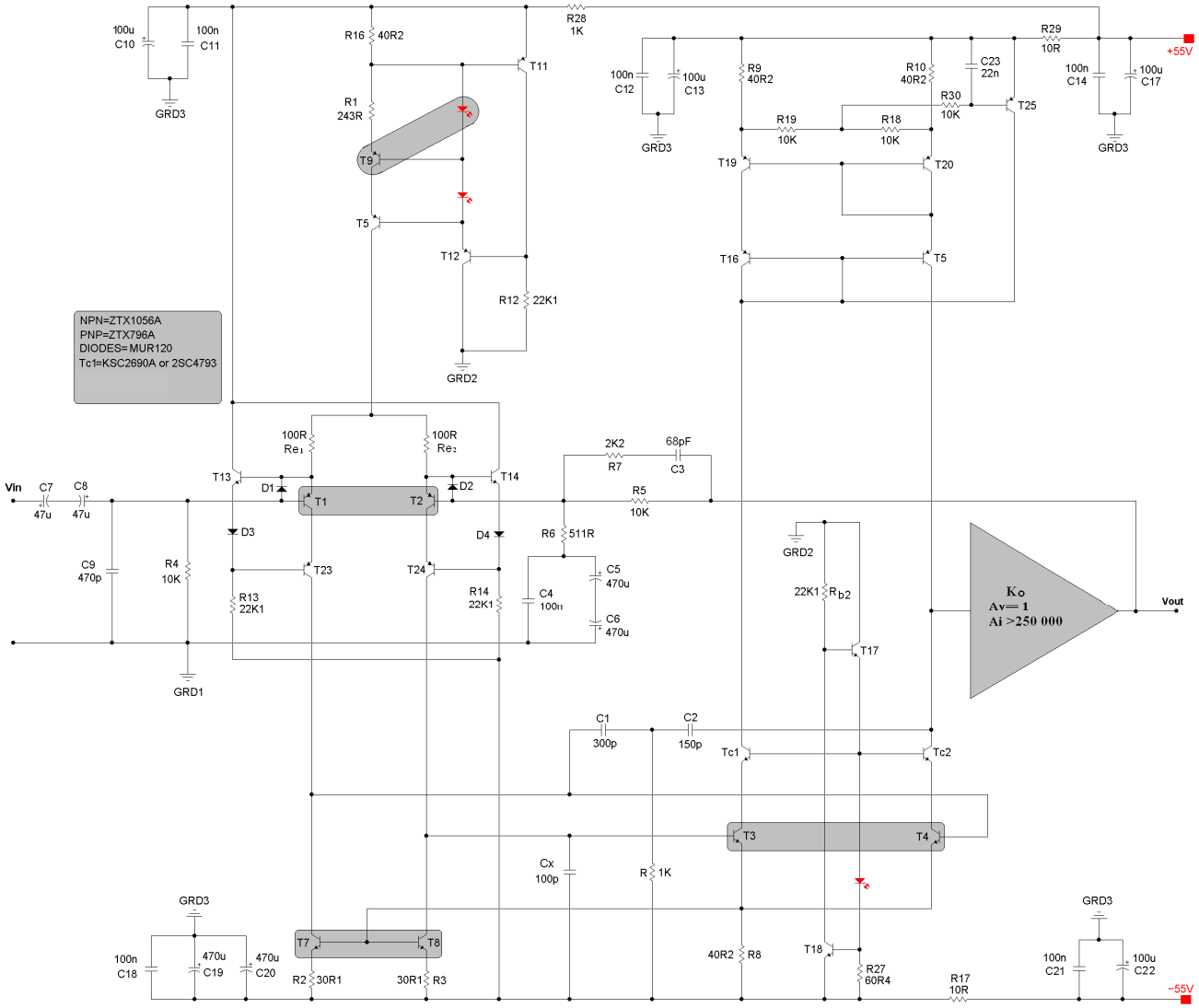


Figure 57. Gain-module "A". Preferred DCDS embodiment with input differential cascode and cascode-enhanced TIS.

For a somewhat reduced voltage compliance, the no-load output impedance of the simple dual-transistor current mirror is roughly an order of magnitude smaller than that of the ANF current source. This deficiency may be ameliorated by merely adopting the Wilson current mirror (**figure 57**).

A modification of the *amplified negative feedback* (ANF) current source is here used to bias the TIS cascode's voltage reference (**fig. 57**). This arrangement gives an output impedance of less than 5 Ohms by acting as an emitter follower (**T17**), which furnishes a nominally constant current, established by resistor **R27**, for the voltage reference—a red LED in this case. Stability of the input stage's current source is reinforced by similarly rearranging an ANF current source to bias its LED references.

The Second Stage Active Current Sink

Replacing **R8** with an active current sink makes the second stage's tail current virtually immune to intrinsic (or indeed extrinsic) common-mode voltage excitation, regardless of the values of mirror degeneration resistors **R2** and **R3** (**fig. 57**).

This guarantees virtually ideal push-pull action for several decades of frequency, even with single-pole Miller compensation, and makes for more efficient use of second stage standing current as the slew limit is approached.

With double-pole compensation, however, the improvement engendered by this modification was found to be negligible in the audio band, being neither reflected in the overall linearity, nor expressed in the PSRR of the design.

This is because (in lieu of the active current sink), provided the voltage across **R2** and **R3** remains small (roughly $0.1\mathbf{V_{BE}}$), the quiescent voltage across resistor **R8** remains relatively constant, causing it to behave like a constant current sink.

Moreover, an extra diode connected in series with and interposed between the negative rail and input stage's current mirror may now be required to accommodate the active current sink's compliance, making this approach somewhat voltage inefficient.

The input stage is here configured as a differential cascode **(fig. 57)** with common-base transistors **T23/T24** bootstrapped to the emitters of **T1/T2** by emitter followers **T12/T13** respectively. Consequently, the input transistors operate at virtually zero collector-base voltage, which obviates their collector-base junction leakage currents [49].

This arrangement increases the circuit's CMRR by shielding the input transistors from common-mode stimulus. Notably, the input transistors are effectively shielded from ripple on the negative power supply, which gives an improvement in –PSRR of more than 50 times at ripple frequency (100Hz), and more than four times at 20KHz **(fig. 58)**. Incidentally, the temptation to use the bootstrap emitter follower with the TIS's cascode biasing arrangement should be resisted as it significantly compromises the dynamic stability of the minor loop.

The input cascode also facilitates the use of high current-gain transistors (typically of low $\mathbf{V_{CE(MAX)}}$); this reduces the amplifier's output DC offset due base current mismatch in the input stage. Indeed, if cost is no object, a matched monolithic pair of low noise BJTs (e.g. **Analog Devices'® SSM-2220**) may be used to ensure output DC offset does not exceed 1mV.

The diode clamps, **D1** and **D2**, protect the input transistor's emitter-base junctions from excessive reverse bias due to anomalous voltage transients which would otherwise degrade their current gain, or destroy them altogether. These diodes are intrinsic to the **SSM-2220** monolithic pair, and may be omitted if this device is used.

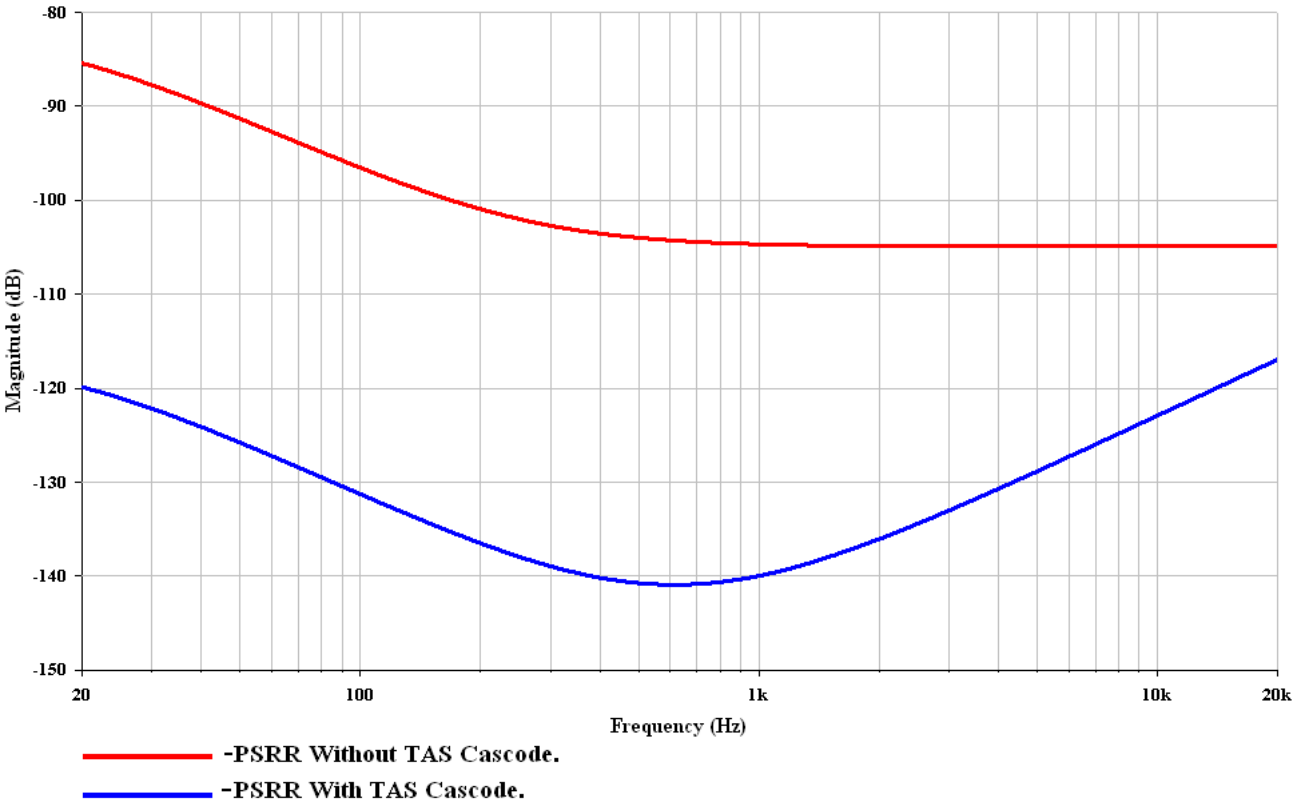


Figure 60. The input stage's bootstrapped cascode improves –PSRR by nearly fifty times at ripple frequency.

Comparative Tests for Linearity

Three gain modules (**A** to **C**) as may be used in a practical amplifier are shown in **figures 57**, **59** and **60** respectively. Module **C** (**fig. 60**) is a modification of the Thompson topology with a cascode TIS. A fourth module, **D**, Hitachi's single-pole compensated variant of the DCDS circuit (**fig. 39**), was used as a reference model against which the linearity of the other modules was evaluated. These circuits were subjected to Fourier analysis in LTSpice, and, in each case, ideal unity-gain voltage-controlled voltage sources (VCVS) were used to buffer the TIS from the feedback network.

Although Fourier analysis in SPICE can be inaccurate in absolute terms, depending on the semiconductor models used and compared with the results obtained with practical amplifiers, it can be quite precise, with a resolution unattainable with even the most advanced audio analysers, when used for comparative studies of model circuits using the same reliable semiconductor SPICE models. Such comparative analysis can be relied upon to give insight into the behaviour of model circuitry that would, in some cases, be impossible to obtain in practice.

The Baker clamp used to prevent saturation in the TIS's current source **T8** in gain module **B** has no significant effect on linearity. The bias resistors **R11** and **R15** in the TIS's ANF current source of gain module **B** are made small enough to prevent the control element **T10** from being deprived of current when diode $\mathbf{D_{b2}}$ is forward-biased during positive voltage clip. Otherwise this may induce unpleasant voltage spikes at the second stage's output, which rather defeats the use of a Baker clamp in the first instance. This is easily prevented by making bias resistors **R11** and **R15** sufficiently small; two resistors are used to spread the dissipation, which is not insubstantial. With both gain modules **B** and **C** transistor **T13**, courtesy of resistor **R9**, is required to limit the current sunk by **T7** when SOA protection with a practical output stage is activated.

If the additional complexity and slight deterioration in voltage efficiency (current source compliance) are not an issue, buffered drive-on-demand for the TIS current source's anti-saturation diode for module **B** may be provided by the nested ANF current source cell of **figure 61.** Since transistor **T1** in this arrangement constrains the current through **R1** to roughly 17mA, then, for example, any inadvertent increase in current through **R2** is necessarily expressed as an increase in the current conducted by **T2**; thus the excess current is siphoned away from **R2** by **T2** via its emitter and nominal quiescent conditions restored. Note that with this arrangement compensation capacitor **C1** may be required to guarantee stability.

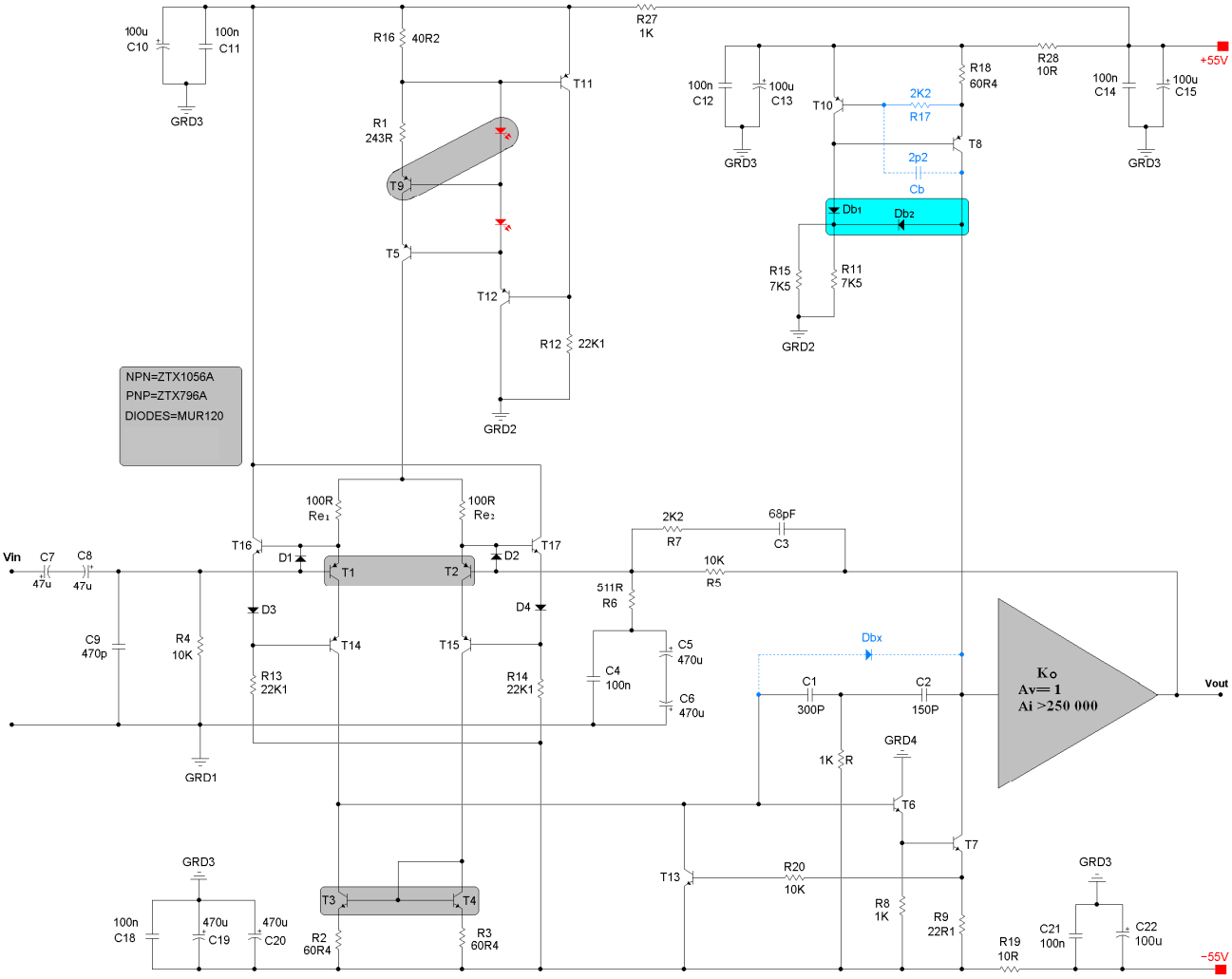


Figure 59. Gain-module "B": Double-pole compensated Thompson topology with enhanced current gain TIS. Booster capacitor C_b and associated resistor R17 are optional.

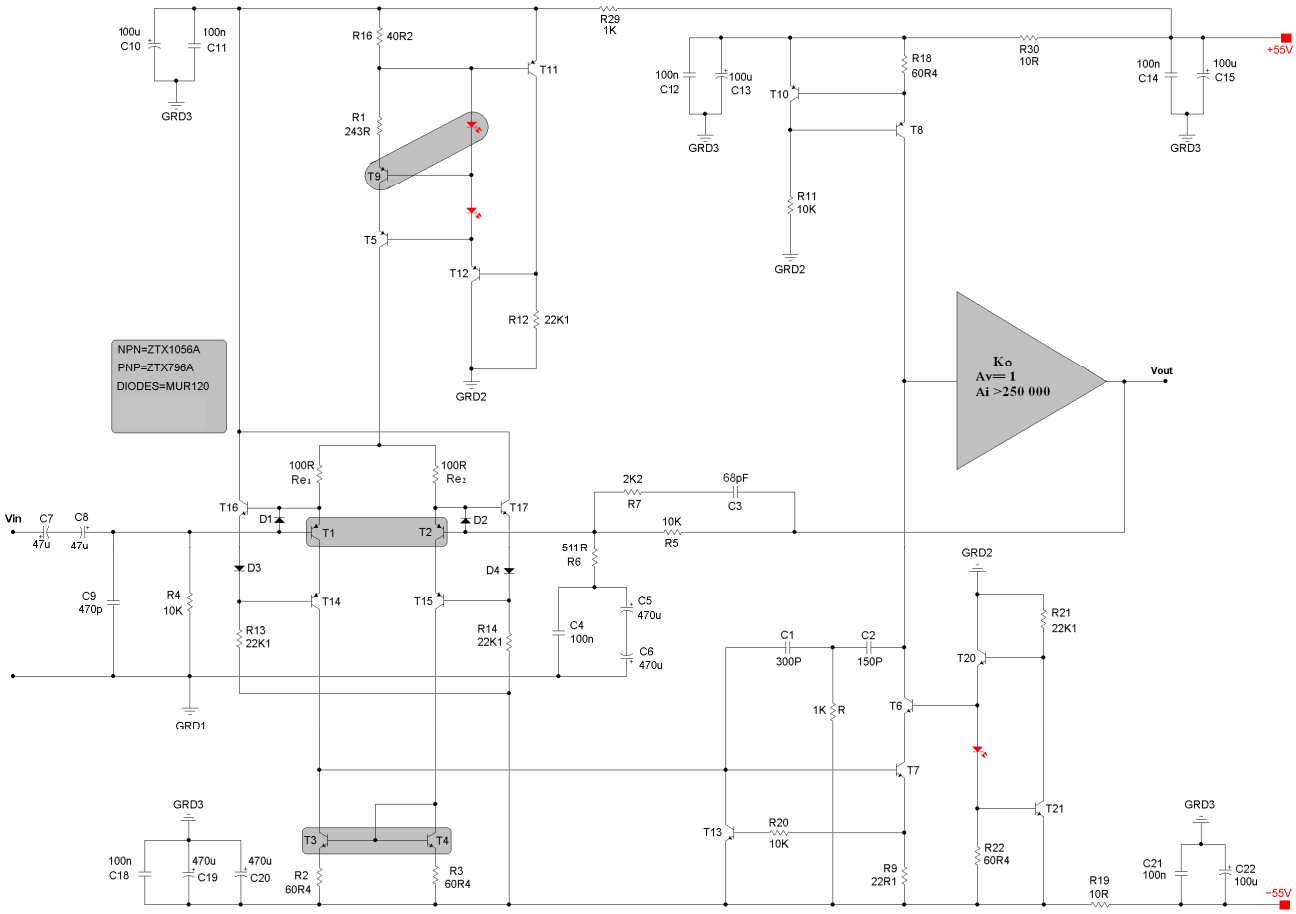


Figure 60. Gain-module “C”: Double-pole compensated Thompson topology with cascode TIS. Transistor T13 and resistor R9 limit the current sunk by T6/T7 when SOA protection circuitry in the output stage is activated.

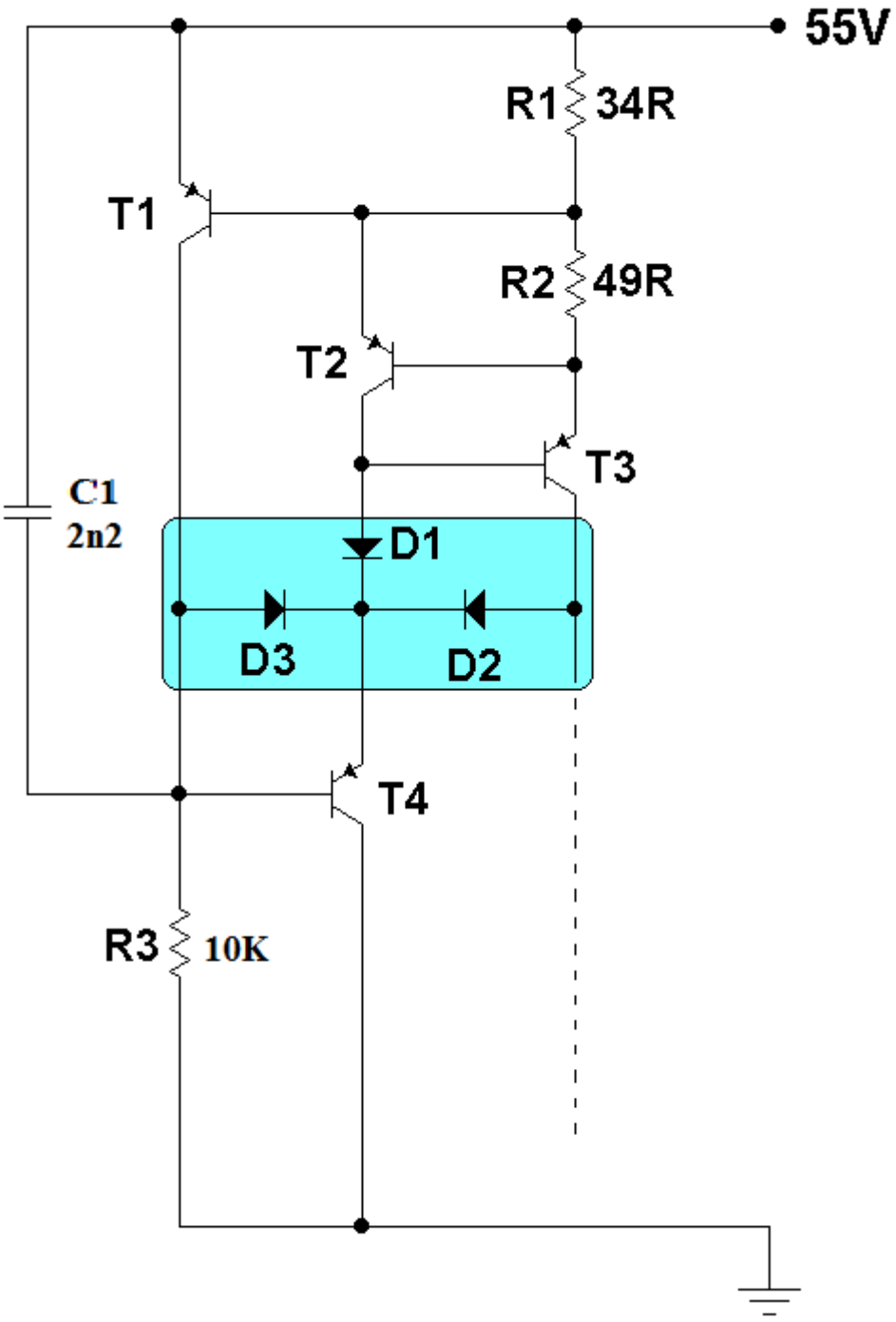


Figure 63. Nested ANF current source cell for the TIS of gain module "B"; transistor T4 sinks current on demand from anti-saturation diode D2 during positive output voltage clipping.

VOLTAGE GAIN MODULE	SPICE (LTSPICE®) THD (20 HARMONICS) @ 1KHZ AND 40V PEAK	SPICE (LTSPICE®) THD (20 HARMONICS) @ 20KHZ AND 40V PEAK
A	0.000005%	0.00013%
B	0.000007% (With Baker Clamp $\mathbf{D_{bx}}$: 0.0029%)	0.00027% (With Baker Clamp $\mathbf{D_{bx}}$: 0.057%)
C	0.000006%	0.00012%
D	0.002%	0.017%

Table 1. Modules A and C give significantly better overall linearity than the enhanced current gain TIS arrangement of module B, whose otherwise good performance is compromised by Miller magnification of the non-linear reverse bias capacitance of anti-saturation diode D_{bx}.

Summary

It is apparent (**Table 1**) that the linearity of the basic DCDS topology (module **D**) is significantly inferior to that of the Thompson arrangement with the cascode TIS (module **C**). Indeed, contrary to Dr White[1] and regardless of local gain distribution or output stage topology, this circuit is incapable of delivering less than 0.01% THD+N at the top end of the audio band.

The otherwise excellent performance of module **B** is compromised by somewhat poor recovery from saturation. Unfortunately, the so-called Baker clamp diode $\mathbf{D_{bx}}$ (**fig. 59**) sometimes used to expedite recovery also provokes a disproportionate deterioration in linearity due its nonlinear reverse-biased junction capacitance being magnified many times by Miller effect.

On the other hand, the modified DCDS voltage gain block with the cascode TIS (module **A**) gives excellent linearity, of the same order as the Thompson arrangement with the cascode TIS (module **C**) across the audio band. This suggests (in the context of a double-pole-compensated forward-path) that the much vaunted contribution of push-pull action in the TIS to overall closed-loop linearity is negligible.

Nevertheless, push-pull action in the second stage (module **A**) virtually guarantees symmetrical slew without recourse to rather dubious current booster capacitor C_b used in the TIS's current source of modules **B** and **C**, and it improves ±PSRR, relative to modules **B** and **C**, by up to an order of magnitude across the audio band. Moreover, the push-pull second stage is instrumental in reducing output DC offset from roughly 50mV (for modules **B** and **C**) to less than 5mV.

Without the aid of anti-saturation diodes, module **A**'s recovery from clipping was almost as immaculate as that of module **C**. Nevertheless, given the relative simplicity of module **C**, and the fact that its closed-loop linearity is on a par with that of module **A**, the additional complexity of module **A** may not be commercially justifiable. Note carefully, however, that, since an ideal output stage was used, the TIS of module **C** is here operating with a near-ideal output impedance, consisting, effectively, of only the output impedance of the TIS in parallel with that of its ANF

current source. Therefore, in a practical circuit, even with a triple push-pull emitter follower output stage, the effective output impedance of the TIS is likely to be significantly reduced. This reduces the forward-path gain as well as the minor-loop feedback and will certainly give greater non-linearity in practice for module **C** than is depicted in **Table 1**.

Be that as it may, far from being inherently incapable of absorbing improvement, Thompson's configuration (modules **B** and **C**) has yet to be superseded in any substantive way by the push-pull TIS of module **A** and its variants. This is particularly true of low-power (<400W into 4ohms) domestic applications, where relatively modest slew rates are acceptable and the residual slew asymmetry is trivial.

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