Matrox® Rapixo CL Pro

Installation and Hardware Reference

Manual no. Y11522-101-0100

August 7, 2020

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Contents

Chapter 1

Introduction

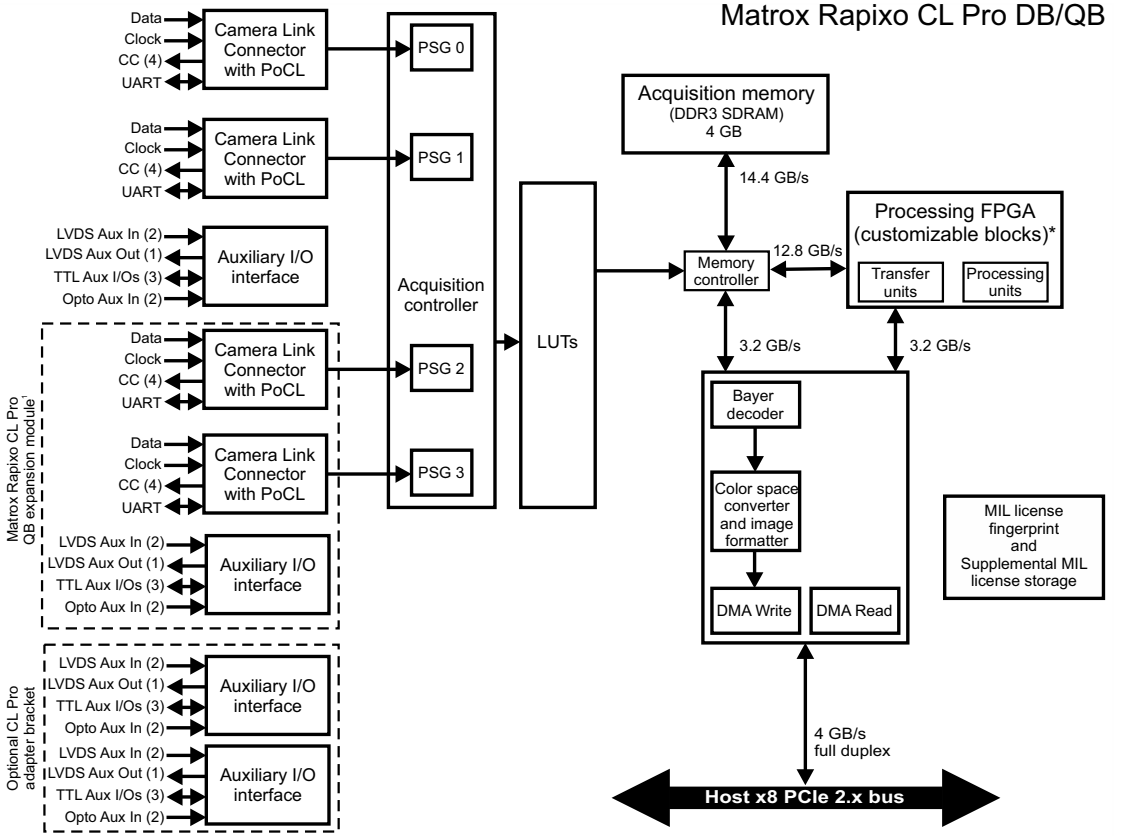
This chapter briefly describes the features of the Matrox Rapixo CL Pro boards, as well as the software that can be used with the boards.

Acquisition with Matrox Rapixo CL Pro

Matrox Rapixo CL Pro is a high-performance PCIe frame grabber that acquires images from video sources compliant with the Camera Link 2.1 specification (or earlier). Matrox Rapixo CL Pro also comes with FPGA-based processing-offload capabilities (a Processing FPGA).

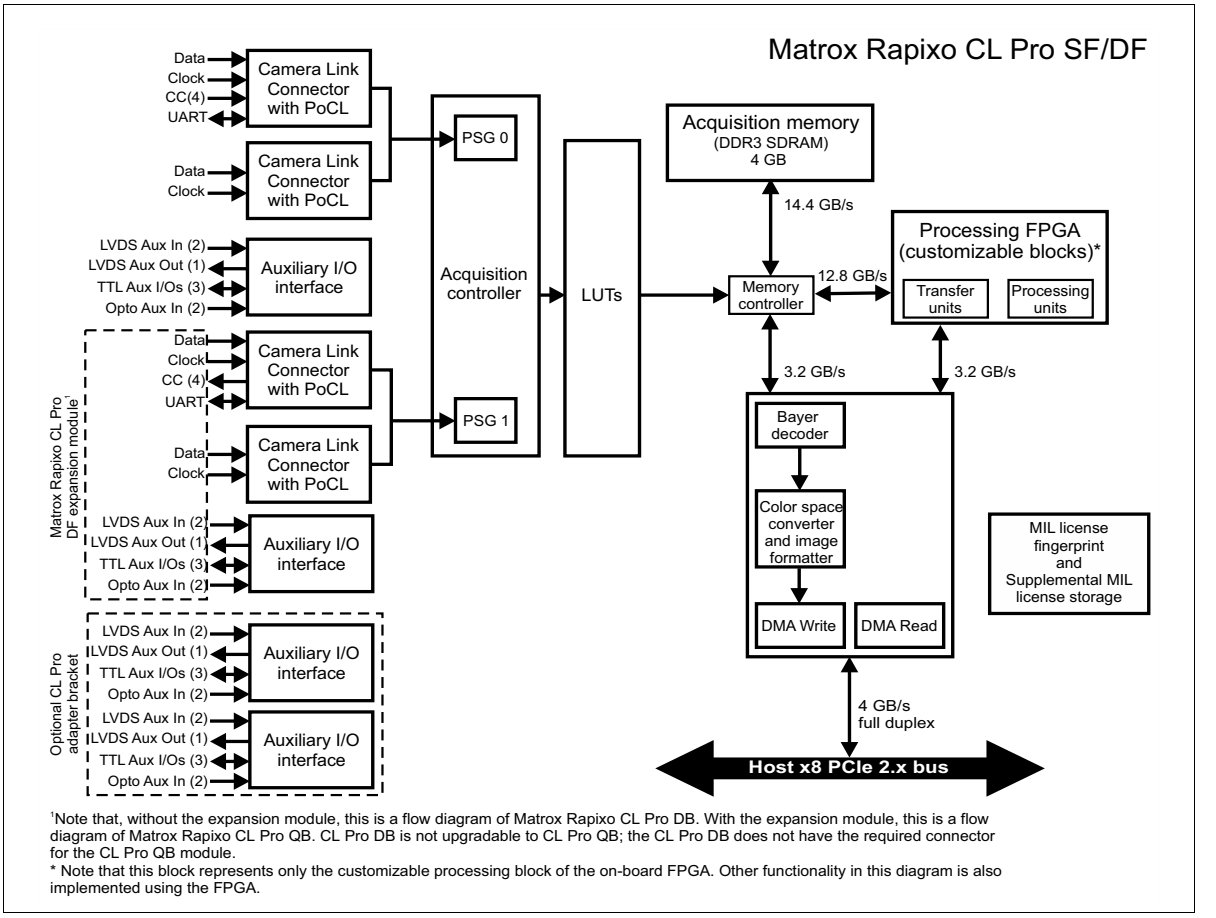
There are four versions of Matrox Rapixo CL Pro: Matrox Rapixo CL Pro SF, Matrox Rapixo CL Pro DF, Matrox Rapixo CL Pro DB, and Matrox Rapixo CL Pro QB. Matrox Rapixo CL Pro DB and QB support acquisition from Camera Link video sources in Base configuration; DB supports simultaneous acquisition from two of these video sources and QB supports four simultaneously. Matrox Rapixo CL Pro SF and DF support acquisition from Camera Link video sources in Medium, Full, 72-bit, or 80-bit configuration; SF supports acquisition from one of these video sources and DF supports two simultaneously.

Matrox Rapixo CL Pro supports power-over-Camera Link (PoCL) compliant video sources and Camera Link frequencies of 20 MHz to 85 MHz.



[1]Note that, without the expansion module, this is a flow diagram of Matrox Rapixo CL Pro DB. With the expansion module, this is a flow diagram of Matrox Rapixo CL Pro QB. CL Pro DB is not upgradable to CL Pro QB; the CL Pro DB does not have the required connector for the CL Pro QB module.

* Note that this block represents only the customizable processing block of the on-board FPGA. Other functionality in this diagram is also implemented using the FPGA.



[1]Note that, without the expansion module, this is a flow diagram of Matrox Rapixo CL Pro DB. With the expansion module, this is a flow diagram of Matrox Rapixo CL Pro QB. CL Pro DB is not upgradable to CL Pro QB; the CL Pro DB does not have the required connector for the CL Pro QB module.
* Note that this block represents only the customizable processing block of the on-board FPGA. Other functionality in this diagram is also implemented using the FPGA.

General acquisition features

Matrox Rapixo CL Pro supports frame-scan (area-scan) and line-scan, monochrome and color video sources. The color video sources can be RGB video sources or video sources with a Bayer color filter. Matrox Rapixo CL Pro can decode Bayer color-encoded images and perform color space conversions while transferring the image to the Host.

Processing capabilities

Matrox Rapixo CL Pro features an on-board real-time processing FPGA device (Processing FPGA), which can be configured to offload and even accelerate the most compute-intensive part of typical image processing applications, without generating additional data traffic within the host computer (Host).

Processing FPGA

The Processing FPGA on Matrox Rapixo CL Pro is a highly customizable Xilinx Kintex 7 FPGA*. The operations performed on-board are controlled using the Matrox Imaging Library (MIL) application-development software. Using MIL, the processing units (PUs) of an FPGA configuration can be rearranged to perform the operations in the required sequence, without having to necessarily generate a new FPGA configuration. You would typically use standard Matrox FPGA configurations. You can also chose to implement processing on your own, using the Matrox FPGA Development Kit (FDK) and C++, or you can employ Matrox's FPGA design services to generate an application-specific FPGA configuration.

Before the Processing FPGA can process grabbed images, they must be stored in on-board memory. If images stored in Host memory are required, they can be streamed directly to the Processing FPGA for processing. Images and other data resulting from processing can be stored in on-board memory or streamed to the Host.

Additional functionality

In addition to the core video capture capabilities, Matrox Rapixo CL Pro incorporates a variety of features to simplify overall system integration. These features include:

- **Color space converter and image formatter.** This can convert data as it is being transferred to the Host. It can convert 8- or 16-bit monochrome or 24- or 48-bit packed BGR data to monochrome, packed BGR, packed BGRa, planar RGB, or YUV (YUYV) format. In addition, it can flip or subsample data sent to the Host.

- **Bayer decoder.** This can convert Bayer-encoded data to RGB using an average demosaicing algorithm. The following Bayer patterns are supported: GRBG, GBRG, BGGR, and RGGB.

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*. The Processing FPGA also includes implementation for other functionality on the board, and is not used for processing only.

- **Auxiliary, multi-purpose signals.** These are non-video signals that can support one or more functionalities (for example, trigger input, rotary/linear encoder input, or timer output), depending on the auxiliary signal.

- **Integrated quadrature decoders.** These can decode input received from a rotary or linear encoder with quadrature output.

- **Programmable lookup tables (LUTs).** These allow Matrox Rapixo CL Pro to map data to precalculated values, before it is stored in memory.

- Matrox Rapixo CL Pro can provide 4.8 W of power per Camera Link connector to any device that supports power-over Camera Link (PoCL). This means that it can provide 4.8 W to a Base camera, or 9.6 W to a Medium or Full camera.

On-board memory

Matrox Rapixo CL Pro is equipped with 4 Gbytes of DDR3 SDRAM on-board memory. This memory is accessed through the memory interface, and is used to store acquired images. The memory controller has multiple input ports, and it has a maximum data transfer rate of 14.4 Gbytes/sec.

Data transfer

Your Matrox Rapixo CL Pro can send data to the Host at a maximum theoretical transfer rate of 4.0 Gbytes/sec. Optimum conditions for high speed transfer include using the board in a PCIe 2.x slot with 8 active lanes, using a 256-byte payload. DMA write performance is chipset and computer dependent, and is slightly affected by the image size and alignment in Host memory (frame start address and line pitch).

To measure the effective available bandwidth of the PCIe slot in your computer with your Matrox Rapixo CL Pro board, Matrox provides the Rapixo CL Bench tool. These tools are integrated in the MILConfig utility, which is shipped with software that supports Matrox Rapixo CL Pro (for example, MIL).

Documentation conventions

This manual refers to all Matrox Rapixo CL Pro boards as Matrox Rapixo CL Pro. When necessary, this manual distinguishes between the boards using their full names. Also note that, when the term Host is used in this manual, it refers to the host computer.

Software

To operate your Matrox Rapixo CL Pro, you can use one or more Matrox Imaging software products that supports the board. These are the Matrox Imaging Library (MIL) and its derivatives (for example, MIL-Lite and Matrox Intellicam). All Matrox software is supported under Windows; MIL is also supported under Linux when using Matrox Rapixo CL Pro. Consult your software manual for supported versions of these operating systems.

MIL

MIL is a high-level programming library with an extensive set of optimized functions for image capture, processing, analysis, transfer, compression, display, and archiving. Image processing operations include point-to-point, statistical, spatial filtering, morphological, geometric transformation, and FFT operations. Analysis operations support camera calibration, are performed with sub-pixel accuracy, and include pattern recognition (normalized grayscale correlation and Geometric Model Finder), blob analysis, edge extraction and analysis, measurement, image registration, metrology, character recognition (template-based and for both normal and dot-matrix text, feature-based), code reading and verification (1D, 2D and composite code types), bead (continuous strips of material) inspection, 3D reconstruction, 3D processing, 3D analysis, classification, and color analysis.

MIL applications are easily ported to new Matrox hardware platforms and can be designed to take advantage of multi-processing and multi-threading environments.

MIL-Lite

MIL-Lite is a subset of MIL. It includes all the MIL functions for image acquisition, transfer, display control, and archiving. It also allows you to perform processing operations that are typically useful to pre-process grabbed images.

Matrox Intellicam

Matrox Intellicam is an interactive Windows program that allows for fast video source interfacing and provides interactive access to all the acquisition features of your Matrox board. Matrox Intellicam also has the ability to create custom digitizer configuration format (DCF) files, which MIL and its derivatives use to interface with specific non-standard video sources. Matrox Intellicam is included with all Matrox Imaging software products.

Essentials to get started

To begin using your Matrox Rapixo CL Pro, you must have a computer with the following:

- An available conventional x8 (or x16) PCIe 2.x or 3.x slot*.
- Processor with an Intel 32-bit or 64-bit architecture, or equivalent.
- A relatively up-to-date PCIe chipset. A chipset that supports the PCIe 2.x standard is preferable. The list of platforms that are known to be compatible with Matrox Rapixo CL Pro is available on the Matrox website, under the board's PC compatibility list.
- MIL or one of its derivatives. This software should be installed after you install your board.

Matrox does not guarantee compatibility with all computers that have the above specifications. Please consult with your local Matrox Imaging representative, local Matrox Imaging sales office, the Matrox web site, or the Matrox Imaging Customer Support Group at headquarters before using a specific computer.

Consult your software package for other computer requirements (for example, operating system and memory requirements).

*. Note that you can also install Matrox Rapixo CL Pro in a x4 PCIe slot that has a mechanical x8 connector; however, the maximum transfer rate between Matrox Rapixo CL Pro and the Host is reduced by 50%.

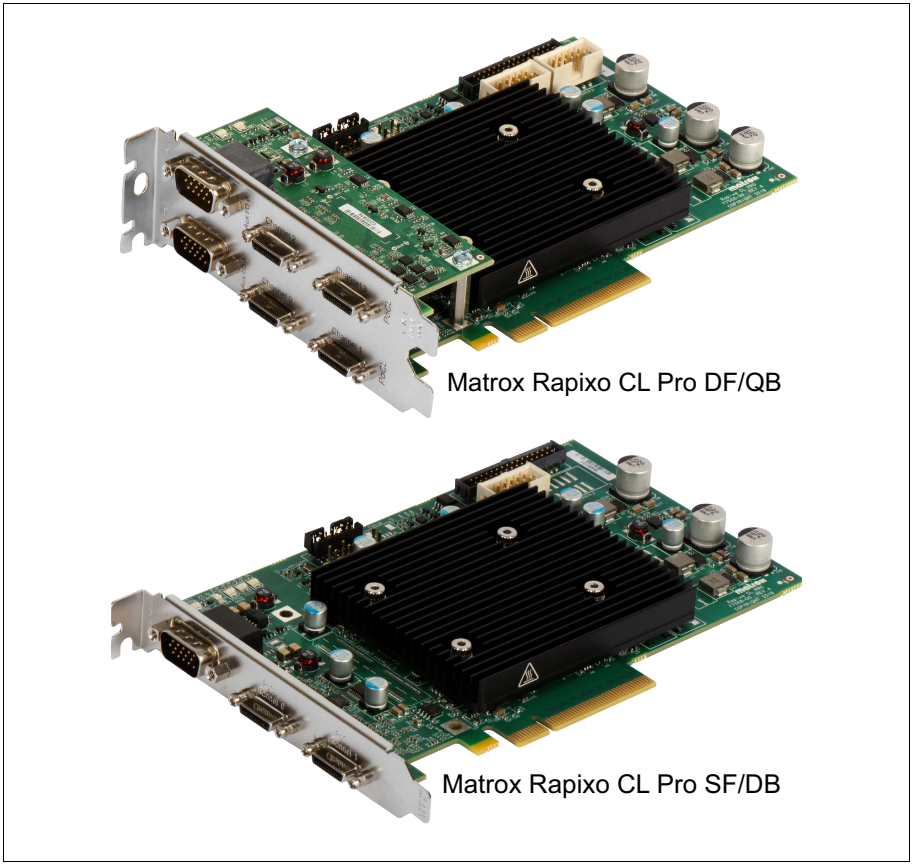
Inspecting the Matrox Rapixo CL Pro package

You should check the contents of your Matrox Rapixo CL Pro package when you first open it. If something is missing or damaged, contact your Matrox representative.

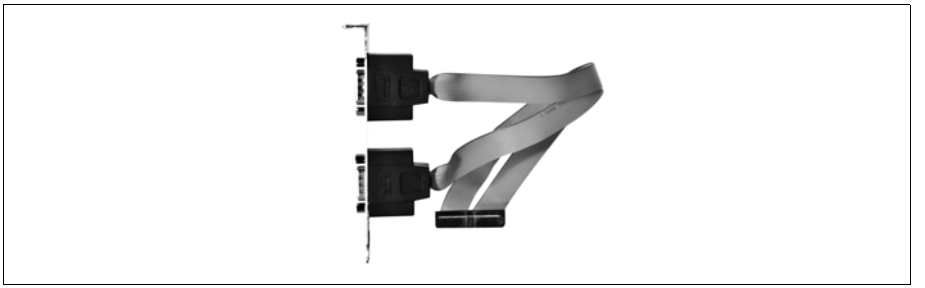
Standard items

You should receive the following items:

- The Matrox Rapixo CL Pro board.



- A HD-15 cable adapter bracket, equipped with two HD-15 auxiliary I/O connectors.



Available separately

You might have also ordered one or more of the following:

- MIL or MIL-Lite. Matrox Intellicam is included with both of these software packages.

Handling components

The electronic circuits in your computer and the circuits on your Matrox Rapixo CL Pro are sensitive to static electricity and surges. Improper handling can seriously damage the circuits. Be sure to drain static electricity from your body by touching a metal fixture (or ground) before you touch any electronic component. In addition, do not let your clothing come in contact with the circuit boards or components.

Warning

Before you add or remove devices from your computer, always **turn off** the power to your computer and all peripherals.

Installation

The installation procedure consists of the following steps:

1. Complete the hardware installation procedure described in *Chapter 2: Hardware installation*.

2. Complete the software installation procedure described in the documentation accompanying your software package.

More information

For information on using multiple Matrox Rapixo CL Pro boards, refer to *Chapter 3: Using multiple Matrox Rapixo CL Pro boards*.

For in-depth hardware information, refer to *Chapter 4: Matrox Rapixo CL Pro hardware reference*; whereas for a summary of this information, as well as environmental and electrical specifications, and connector pinout descriptions, see *Appendix B: Technical information*.

This manual occasionally makes reference to a MIL-Lite function. However, anything that can be accomplished with MIL-Lite can also be accomplished with MIL.

Need help?

If you experience problems during installation or while using this product, refer to the support page on the Matrox Imaging web site: www.matrox.com/imaging/support. This page provides answers to frequently asked questions, as well as offers registered customers additional ways of obtaining support.

If your question is not addressed and you are currently registered with the MIL maintenance program, you can contact technical support. To do so, you should first complete and submit the online Technical Support Request Form, accessible from the above-mentioned page. Once the information is submitted, a Matrox support agent will contact you shortly thereafter by email or phone, depending on the problem.

Chapter

2

Hardware installation

This chapter explains how to install your Matrox Rapixo CL Pro board in your computer.

Installing your Matrox Rapixo CL Pro board

Before you install your Matrox Rapixo CL Pro board, some precautionary measures must be taken. Turn off the power to your computer and its peripherals, and drain static electricity from your body (by touching a metal part of the computer chassis).

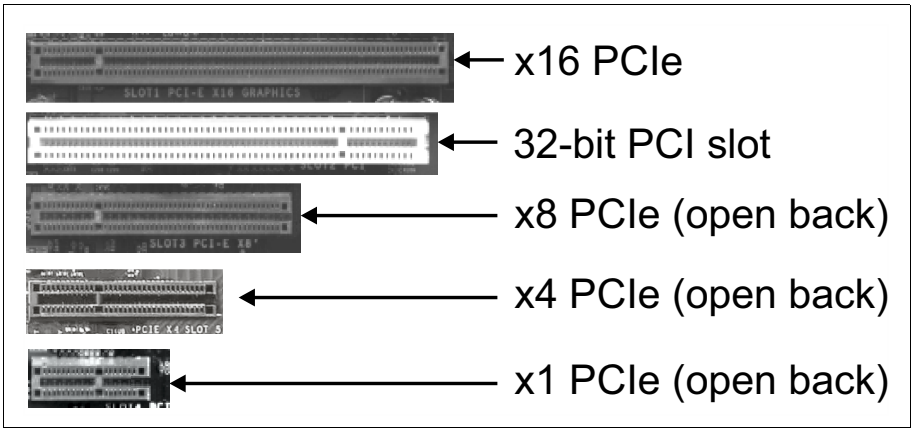
Important

❖ Note that your board should be installed before you install your software.

Proceed with the following steps to install your board:

1. Remove the cover from your computer; refer to your computer's documentation for instructions.

2. Check that you have an empty x8 (or x16) PCIe slot in which to install your Matrox Rapixo CL Pro*. Note that a PCIe 2.x slot and above will ensure the fastest possible transfer of data to the Host.

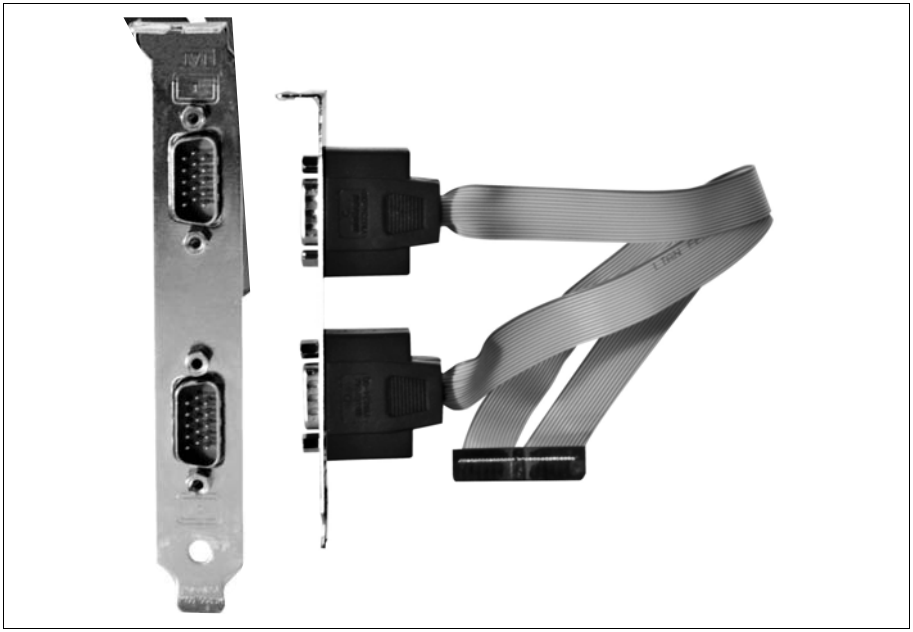


*. Note that you can also install Matrox Rapixo CL Pro in a x4 PCIe slot that has a mechanical x8 connector; however, the maximum transfer rate between Matrox Rapixo CL Pro and the Host is reduced by 50%.

Matrox Rapixo CL Pro might drop frames if the PCIe slot does not have at least 8 active lanes (for example, if the board is connected to a x8 PCIe slot that has only four active lanes*). Verify with your motherboard manufacturer to find out whether your motherboard works efficiently with a x8 PCIe board, such as Matrox Rapixo CL Pro.

If you need to install the HD-15 cable adapter bracket, you will need an additional slot. This slot need not be adjacent to the Matrox Rapixo CL Pro board. In addition, the cable adapter bracket does not plug into a slot's connector; it attaches only to the back of the computer's chassis.

- Note that the external auxiliary I/O connectors on the cable adapter bracket are panel mount connectors. If you don't want to occupy an entire slot for the additional bracket, you can punch out two holes in the computer chassis, and then screw the connectors in the holes.



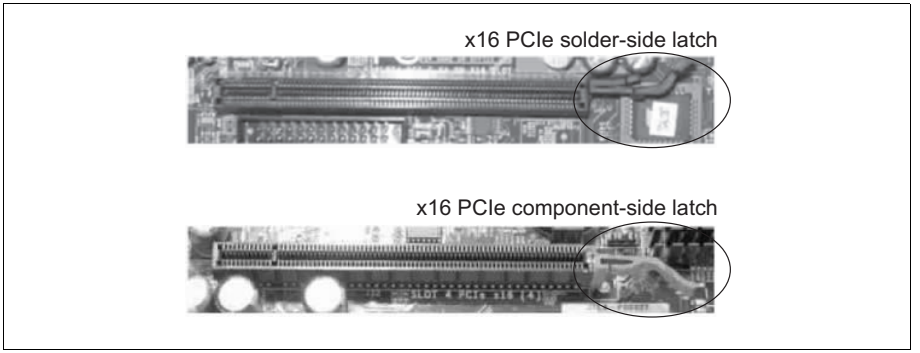
*. After installing the board, you can verify in software the number of PCIe lanes that are currently active, using the MIL-Lite function MsysInquire() with M_PCIE_NUMER_OF_LANES.

3. If there is a metal plate at the back of the selected slots, remove it. Keep the screw from the top of the plate to anchor your board and cable adapter brackets once they are installed.

4. Position your Matrox Rapixo CL Pro board in the selected PCIe slot. Align the connectors of your board with the opening at the back of the slot, and move the board until the connectors pass through the opening.

Important

When installing your Matrox Rapixo CL Pro board in a x16 PCIe slot, special care must be taken to avoid damaging the board. Some x16 PCIe slots have a connector with a retainer. You should avoid touching the latch of this retainer with the board. Alternatively, you can remove the latch from the retainer.



5. Once the input connectors are in the opening of the chassis, press the board firmly but carefully straight down into the connector of the slot.

6. Anchor the board using the screw that you removed in step 3.

7. If required, install the cable adapter brackets, as described in the section *Installing the cable adapter bracket*, later in this chapter.

8. Attach your video sources, as described in the section *Connecting video sources to Matrox Rapixo CL Pro*, later in this chapter.

9. Turn on your computer.

   - When you boot your computer under Windows, Windows' Plug-and-Play system will detect a new Multimedia Video Device and you will be asked to assign it a driver. At this point, you should click on **Cancel**.

     Under Windows and Linux, the driver will be installed during the installation of Matrox Rapixo CL Pro software.

10. Disable active state power management (ASPM) for PCIe devices, to maximize the performance of Matrox Rapixo CL Pro. In the BIOS, disable all ASPM (or equivalent) settings (typically accessible from the **Power management** sub-menu of the **Advanced Configurations** menu). In addition, if the operating system has an **ASPM for PCIe devices** option, disable this option as well. For example, under Microsoft Windows 10, open the **Power** dialog box from the Windows Control Panel. For the currently selected power plan, click on **Change Plan Settings** and then click on **Change Advanced Power Settings**. In the presented dialog, expand **PCI Express**, and then expand **Link State Power Management** and set it to **Off**.

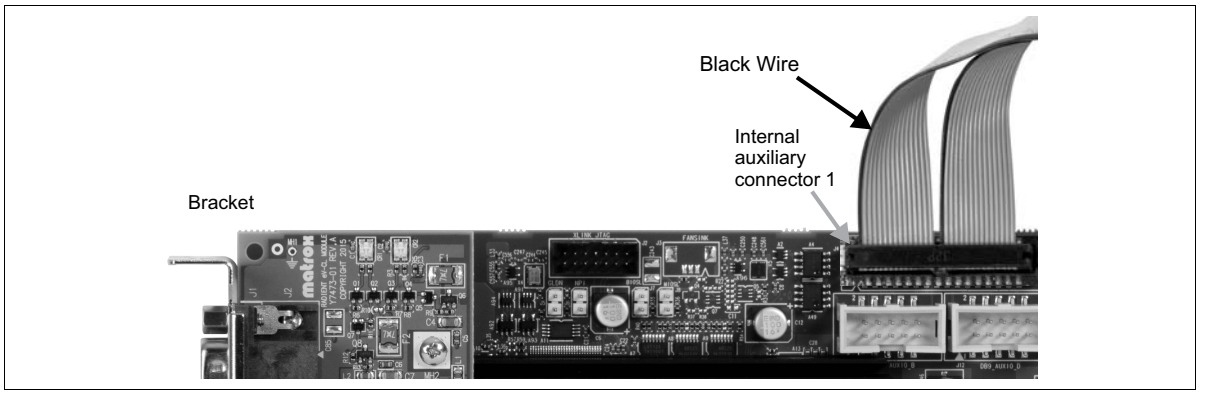
11. Under Microsoft Windows, set the power plan option to high performance to maximize the performance of Matrox Rapixo CL Pro and minimize the possibility of dropped frames. For example, under Microsoft Windows 10, open the **Power Options** dialog box from the Windows Control Panel and set the power plan option to **High Performance**.

Installing the cable adapter bracket

To install the cable adapter bracket, proceed with the following steps:

1. Make sure that your Matrox Rapixo CL Pro board is fastened to the chassis.

2. Attach the cable adapter bracket to the internal auxiliary I/O connectors on the Matrox Rapixo CL Pro board. When attaching the flat ribbon cable of the adapter bracket, position the cable so that the black wire is on the same side as the bracket of the Matrox Rapixo CL Pro board. Matrox Rapixo CL Pro has one internal 32-pin auxiliary I/O connector, and depending on the model, one or two internal 10-pin auxiliary I/O connectors. The 32-pin auxiliary I/O connector (top) is to attach the HD-15 cable adapter bracket, while the 10-pin auxiliary I/O connector (bottom) is to connect a DB-9 cable adapter bracket, if you have one available.



3. Slide the bracket of the cable adapter bracket into the opening at the back of the selected slot.

4. Anchor the bracket to the chassis using the screw that you removed in the previous section.

   Note that the external auxiliary I/O connectors on the cable adapter brackets are panel mount connectors. If you don't want to occupy an entire slot for each additional bracket, you can punch out two holes in the computer chassis, and then screw the connectors in the holes.

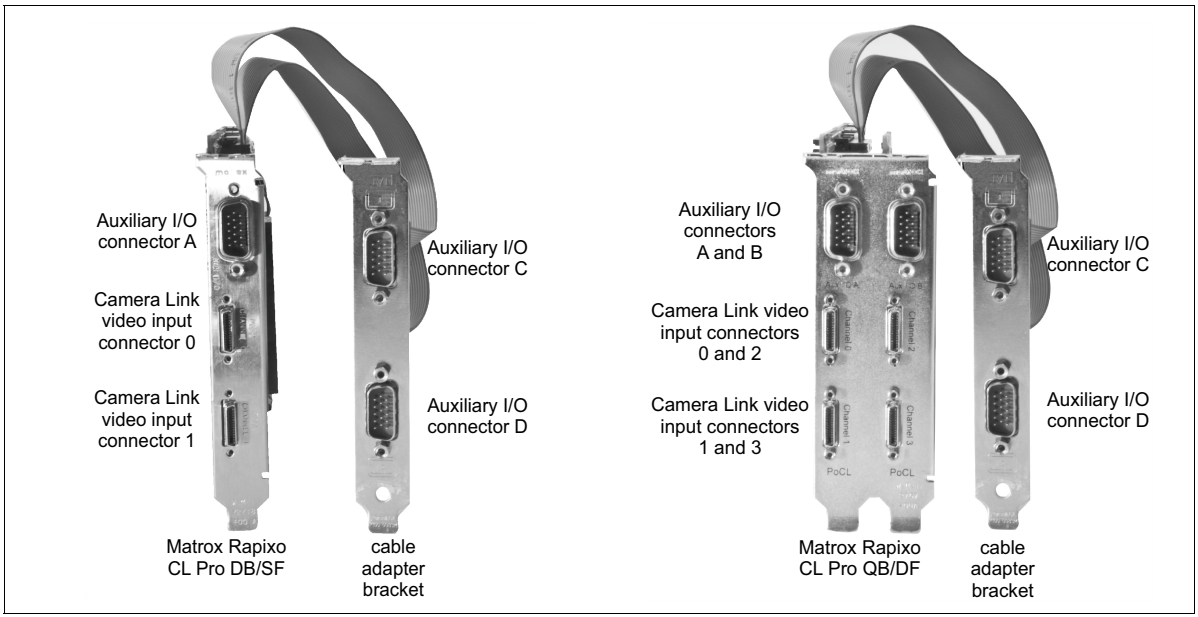
Connecting video sources to Matrox Rapixo CL Pro

The Matrox Rapixo CL Pro board has the following connectors on its bracket(s):

- **Two or four Camera Link-compliant SDR(HDR) video input connectors.** Used to receive video input, timing, and synchronization signals, from the video source. These are also used to transmit/receive communication signals between the video source and the frame grabber through a UART port.
- **External auxiliary I/O connector A and B (HD-15).** Each used to transmit/receive auxiliary signals. Note that B is only available on Matrox Rapixo CL Pro QB and DF

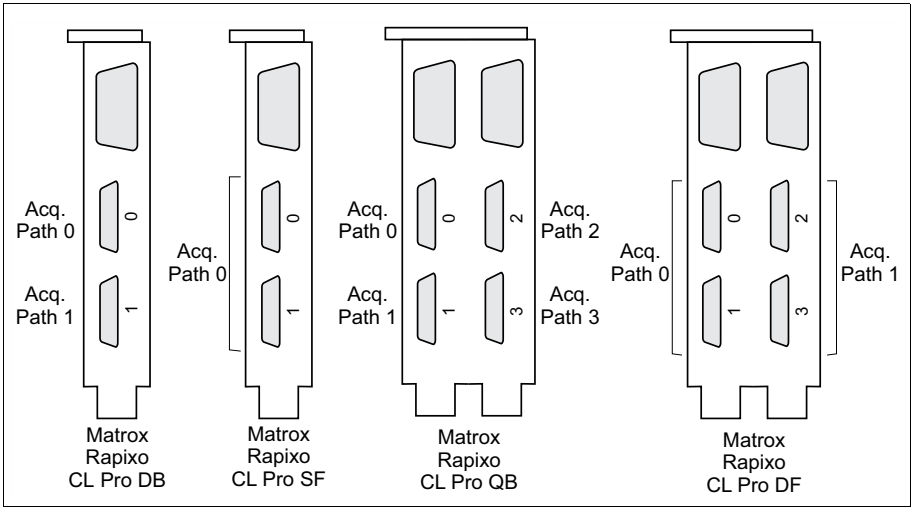
To access the signals of the internal auxiliary I/O connectors, you might have installed a cable adapter bracket. It can have the following connectors:

- **External auxiliary I/O connectors C and D (panel mount HD-15).** Each used to transmit/receive auxiliary signals.



Attach video sources to Matrox Rapixo CL Pro as follows:

Matrox Rapixo CL Pro board	Camera Link connector 0	Camera Link connector 1	Camera Link connector 2	Camera Link connector 3
DB	Video source 0 in Base configuration	Video source 1 in Base configuration	--	--
QB	Video source 0 in Base configuration	Video source 1 in Base configuration	Video source 2 in Base configuration	Video source 3 in Base configuration
SF	Video source 0 in Medium, Full, or 80-bit configuration		--	--
DF	Video source 0 in Medium, Full, or 80-bit configuration		Video source 1 in Medium, Full, or 80-bit configuration	



Warning

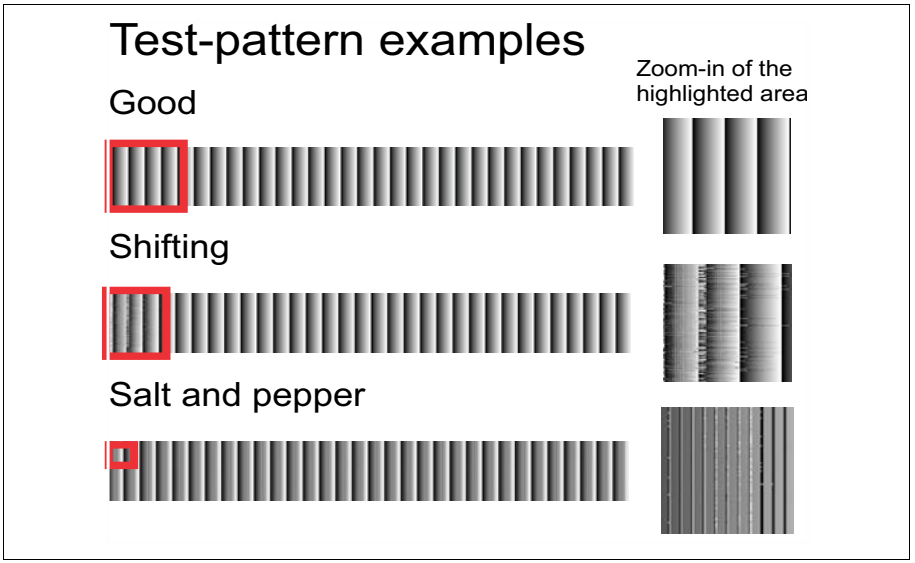
❖ When connecting a video source in Medium, Full, 72-bits, or 80-bit configuration, ensure that you are connecting its cables to the appropriate connector. Accidentally connecting the cables to the wrong connector can damage the board or your video source. The Camera Link connector's pins 2-5 and pins 15-18 are output pins on the top connector (0 and 2), while they are input pins on the bottom connector (1 and 3).

To connect video sources to the Camera Link connectors, use standard Camera Link cables with a 26-pin high-density male mini Camera Link connector (HDR or SDR) at one end. When connecting to PoCL-compliant video sources, you should use PoCL-compliant Camera Link cables (HDR or SDR). Camera Link cables are not available from Matrox; for possible sources, see the *Connectors on Matrox Rapixo CL Pro boards* section in *Appendix B: Technical information*.

❖ If using both Camera Link connectors to connect to the same video source (Medium, Full, 72-bits, or 80-bits configuration), the cables you choose should be of the same type and length. Note, however, if they are not, Matrox Rapixo CL Pro will adapt to any delay caused by reasonable differences in length.

Camera Link cables longer than 7 meters

When using Camera Link cables that are longer than 7 meters with Matrox Rapixo CL Pro and using a pixel clock of 85 MHz, the resulting images from your camera might have either salt and pepper noise or unsynchronized lines (that is, a line is shifted either left or right, and clipped to fit the frame). These errors might be caused by signal degradation due to long cables.



To fix this problem, you must adjust your DCF. To do so:

1. Set your camera to generate images that contain as many different pixel values as possible for every tap (for example, a test pattern containing a horizontal ramp). Refer to your camera's documentation for more information. If your camera does not have a test-pattern mode, select an image similar to a horizontal ramp.

2. Once the test pattern (or sample image) is available, use the **Deseralizer** tool. This tool will adjust values within your DCF to compensate for signal degradation due to the long cables. This tool is available on the **Rapixo CL** page of the MILConfig utility. Follow all on-screen instructions.

   When the process is complete, your camera's DCF is updated. Any MIL application that uses this DCF in the same physical environment should now be able to receive better images (using your camera as a video source).

❖ Note that, if your MILConfig utility does not have the **Deserializer** tool, contact Matrox Technical Support for assistance.

Chapter

3

Using multiple Matrox Rapixo CL Pro boards

This chapter explains how to use multiple Matrox Rapixo CL Pro boards.

Installation of multiple boards

You can install and use multiple Matrox Rapixo CL Pro boards in one computer. Install each additional Matrox Rapixo CL Pro board as you installed the first board (refer to *Chapter 2: Hardware installation*). The number of Matrox Rapixo CL Pro boards that you can install is primarily dependent on the number of physical slots in your computer, and your BIOS; your BIOS establishes how many PCIe devices can be mapped to the PCIe memory space of your computer.

Using MIL-Lite, you have to allocate a MIL system for each board and allocate the resources of each MIL system. For more information, see **MsysAlloc**() with **M_SYSTEM_RAPIXOCL** in the MIL Reference.

Simultaneous image capture from different boards

In addition to capturing images from multiple video sources with a single Matrox Rapixo CL Pro board, you can also simultaneously capture images from video sources attached to multiple Matrox Rapixo CL Pro boards. Note that the number of video sources from which you can simultaneously capture images is limited by the PCIe chipset on your computer.

The use of a high performance PCIe chipset is necessary to sustain PCIe transfers to Host memory. Ideally, at least a PCIe 2.x chipset (or more recent) should be used. A PCIe 2.x or more recent Host bus will optimize the speed of data transmission, and will minimize data loss. The list of platforms that are known to be compatible with Matrox Rapixo CL Pro is available on the Matrox web site, under the board's compatibility list.

To measure the effective available bandwidth of the PCIe slot in your computer with the Matrox Rapixo CL Pro board, you can use the Rapixo CL Bench tool integrated in the MILConfig utility. As a reference point, capturing from a 2K x 2K, 8-bit, 60 frames/sec video source will require a minimum bandwidth of 240 Mbytes/sec, plus an additional bandwidth margin of approximately 20%, for a bandwidth of 288 Mbytes/sec.

Chapter

4

Matrox Rapixo CL Pro hardware reference

This chapter explains the architecture, features, and modes of the Matrox Rapixo CL Pro hardware.

Matrox Rapixo CL Pro hardware reference

This chapter provides information on the Matrox Rapixo CL Pro hardware. It covers the architecture, features, and modes of the board's acquisition section. In addition, the chapter covers the Matrox Rapixo CL Pro hardware related to the formatting and transfer of data. A summary of the features of Matrox Rapixo CL Pro, as well as pin assignments for the various connectors, can be found in *Appendix B: Technical information*.

Acquisition path

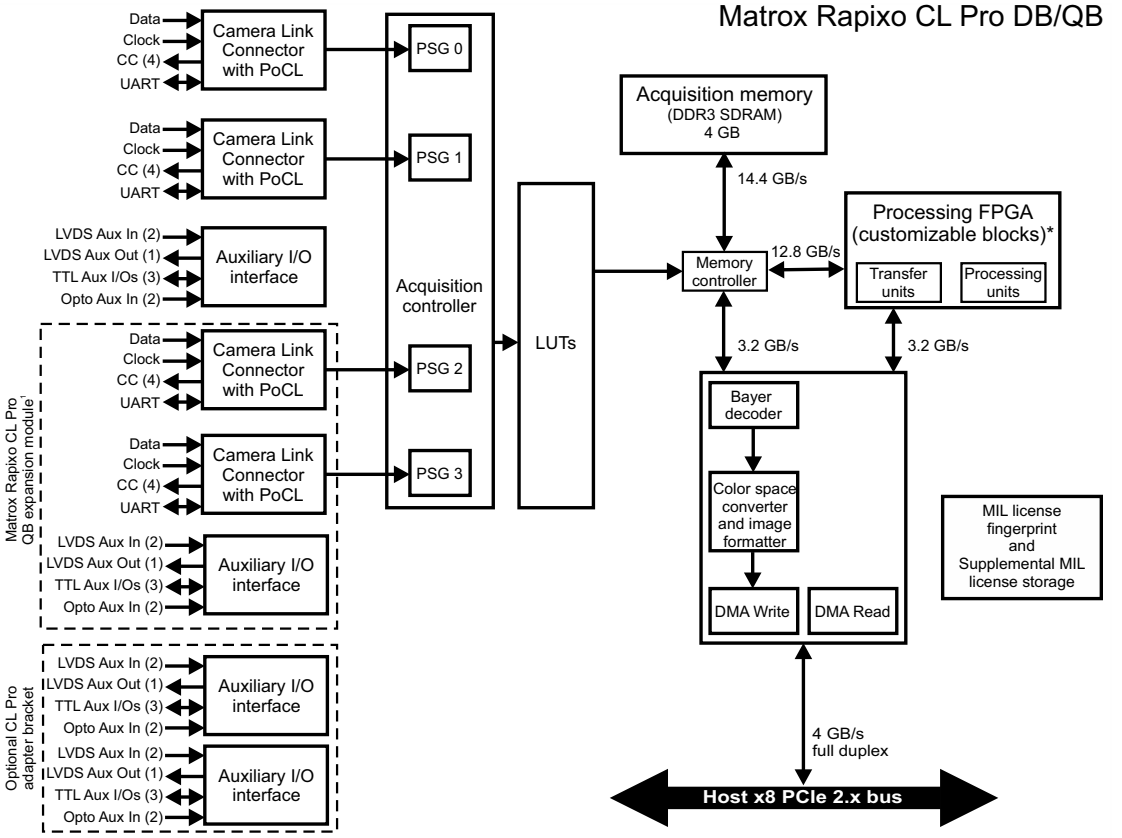
This manual uses the term acquisition path to refer to a path that has the capability to, for example, capture a component or stream of the video input signal. The term *independent acquisition path* is used to refer to an acquisition path that can, if required, acquire data from a video source independently from another such path on the same frame grabber. On Matrox Rapixo CL Pro, there are up to four acquisition paths (depending on the model).

Digitizer

MIL-Lite uses the concept of a MIL digitizer to represent the acquisition path(s) with which to grab from one input source of the specified type. When several MIL digitizers are allocated, their device number along with their DCF identify if they represent the same path(s) (but perhaps for a different input format) or independent path(s) for simultaneous acquisition.

Digitizer configuration format

To program the acquisition section, allocate a MIL digitizer using **MdigAlloc**() with an appropriate DCF (supplied or created) and digitizer device number. If you find a DCF file that is suitable for your video source, but you need to adjust some of the more common settings, you can do so directly, without adjusting the file, using the appropriate MIL-Lite function. For more specialized adjustments, use the Matrox Intellicam program to adjust the DCF file.



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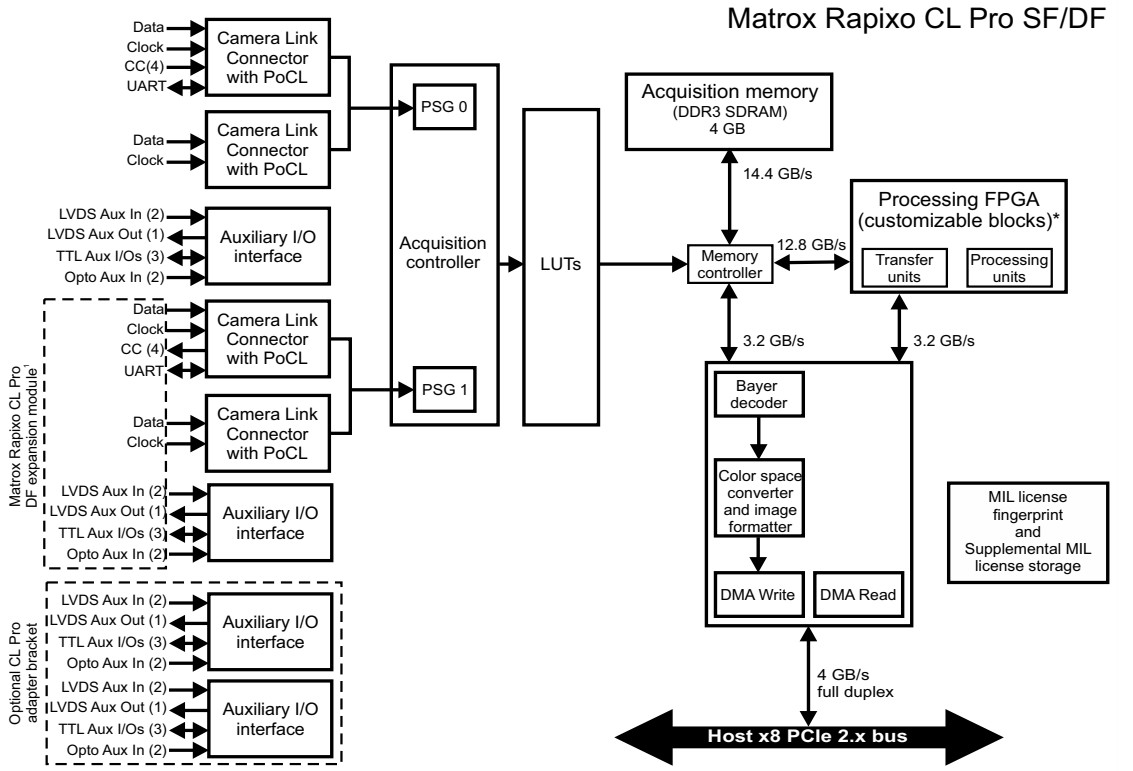

[1]Note that, without the expansion module, this is a flow diagram of Matrox Rapixo CL Pro DB. With the expansion module, this is a flow diagram of Matrox Rapixo CL Pro QB. CL Pro DB is not upgradable to CL Pro QB; the CL Pro DB does not have the required connector for the CL Pro QB module.

* Note that this block represents only the customizable processing block of the on-board FPGA. Other functionality in this diagram is also implemented using the FPGA.

Matrox Rapixo CL Pro acquisition

Matrox Rapixo CL Pro can capture video from digital video sources compliant with the Camera Link 2.1 specification (or earlier). Matrox Rapixo CL Pro can provide power-over-Camera Link to attached video sources.

Matrox Rapixo CL Pro supports frame-scan (area-scan) and line-scan monochrome and color video sources. The color video sources can be RGB video sources or video sources with a Bayer color filter. Matrox Rapixo CL Pro can decode Bayer color-encoded images and perform color space conversions while transferring the image to the Host. Besides standard Camera Link video sources, Matrox Rapixo CL Pro also supports additional types of video sources, including some time-multiplexed video sources.

Operating in Base configuration, Matrox Rapixo CL Pro DB has two independent acquisition paths and Matrox Rapixo CL Pro QB has four independent acquisition paths. Operating in Medium, Full, 72-bit, or 80-bit configuration, Matrox Rapixo CL Pro SF has one acquisition path and Matrox Rapixo CL Pro DF has two independent acquisition paths.

Each acquisition path can grab at Camera Link frequencies of 20 MHz to 85 MHz. Each acquisition path has its own programmable synchronization generator (PSG) and can operate at different acquisition rates.

The acquisition section of Matrox Rapixo CL Pro supports a comprehensive set of general purpose I/O and serial ports to control cameras and other devices.

Performance

The video timing of each acquisition path is as follows:

	Maximum
Number of pixels / line (including sync and blanking)	64 K
Number of lines / frame (including sync and blanking)	64 K
Pixel clock	85 Mhz

The maximum pixel clock frequency is dependent on the length of the cable used. Refer to the *Technical features of Matrox Rapixo CL Pro* subsection of the *Board summary* section in *Appendix B: Technical information*.

Acquisition

A Base-type acquisition path supports up to 24 bits of video data when acquiring from Camera Link-compliant video sources or up to 48 bits when acquiring from non-standard time-multiplexed video sources. Similarly, a Medium-type acquisition path can grab up to 48 bits of video data when acquiring from Camera Link-compliant sources or up to 64 bits when acquiring from non-standard time-multiplexed sources. A Full-type acquisition path supports up to 64 bits of video data when acquiring from Camera Link-compliant video sources. An 80-bit-type acquisition path supports up to 80 bits of video data when acquiring from Camera Link-compliant video sources.

The video sources can be frame-scan (area-scan) or line-scan video sources. Note that the acquisition paths in dual-Base mode are completely independent; therefore, the video sources do not need to be identical when running in these modes.

Supported video sources

The following video sources are supported when running in Base configuration:

	Video sources supported per acquisition path
Camera Link Standard	• One tap 8/10/12/14/16-bit. • Two tap 8/10/12-bit. • One tap 3 x 8-bit (RGB). • Four tap 8-bit with time-multiplexing.
Not Camera Link Standard	• Two tap 14/16-bit with time-multiplexing. • Four tap 10/12-bit with time-multiplexing.

In addition to the above video sources, the following video sources are supported when running in Medium configuration:

	Video sources supported
Camera Link Standard	• Four tap 8/10/12-bit. • One tap 3 x 10/12-bit (RGB).
Not Camera Link Standard	• 8 tap 8-bit with time-multiplexing (using only 2 receivers). • Two tap 14/16-bit. • One tap 3 x 14/16-bit (RGB). • Two tap 3 x 8-bit (RGB) (genlocked).

In addition to the above video sources, the following video sources are supported when running in Full configuration:

	Video sources supported
Camera Link Standard	• Eight tap 8-bit.
Not Camera Link Standard	• Four tap 14-16-bit

In addition to the above video sources, the following video sources are supported when running in 80-bit configuration:

	Video sources supported
Camera Link Standard	• Eight tap 10-bit. • 10 tap 8-bit

Matrox Rapixo CL Pro supports power-over-Camera Link (PoCL) and externally supplied video sources. For compatibility with externally supplied video sources, Matrox Rapixo CL Pro features SafePower mode to supply power only after determining whether the connected video source is PoCL compliant. The PoCL protection on-board fuse can sustain a current of 0.4 A.

Demultiplexers to support time-multiplexed video sources

The acquisition paths of the board feature a demultiplexer. Each can deserialize input from time-multiplexed video sources on a clock cycle basis.
Time-multiplexed video sources can output larger pixel depths and more taps than are possible with non-time-multiplexed video sources in the same configuration, but with a decrease in overall performance. When enabled, the demultiplexer assumes that two video streams share the same data path and that the streams are interleaved based on the clock cycle. The demultiplexer assumes that on one clock cycle, the data is from one stream and that on the next clock cycle, the data is from another stream. The demultiplexer can only deserialize video inputs that, when combined and, if necessary, expanded, total a maximum depth of 64 bits per acquisition path.

Expansion refers to the automatic addition of padding zeros on the most significant bits (MSB) of 10-, 12-, and 14-bit data to create byte aligned 16-bit data.

Communication

For each acquisition path, two LVDS pairs are used to transmit and receive asynchronous serial communication between the video source and the board. These signals are handled by the Universal Asynchronous Receiver/Transmitters (UARTs).

For each acquisition path, four camera control output signals are also available. These are general-purpose signals that are sent to the video source.

UARTs

Matrox Rapixo CL Pro offers an LVDS-compatible Matrox serial interface. Each interface is mapped as a COM port so that it can be accessed through the Microsoft Windows API. Each interface is comprised of both a transmit port and a receive port, permitting the interface to work in full-duplex (bidirectional) mode. The interfaces are located on the Camera Link connectors.

Each interface is controlled by a Universal Asynchronous Receiver-Transmitter (UART)*. Each UART features independently programmable baud rates, supporting all standard baud rates from 300 baud up to 115200† baud.

Acquisition Controller

The acquisition controller is responsible for reconstructing and storing image data in main on-board memory. When writing data to memory, the acquisition controller can perform line and frame reversal; it can flip the image horizontally and/or vertically.

On Matrox Rapixo CL Pro DB/QB, the acquisition controller can write to four non-sequential memory regions (zones) per acquisition path.

On Matrox Rapixo CL Pro SF/DF, the acquisition controller can write to the following number of non-sequential memory regions maximum: 6 for Medium, 8 for Full, 9 for 72-bit, and 10 for 80-bit‡.

Note that the width of each region must be a multiple of the number of taps in that region.

To establish the number of non-sequential memory regions to which your video source must write, refer to the documentation accompanying your video source.

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*. The UART implementation was derived from a design by Daniel Wallner. Please see *Appendix C: Acknowledgments* for copyright information.

†. In addition, the maximum baud rate is highly dependent on the amount of computer resources available.

‡. The 10 non-sequential memory regions in 80-bit configuration are only available with 8-bit taps.

PSGs

For each acquisition path, the acquisition controller provides a programmable synchronization generator (PSG). Each PSG allows for independent acquisition from one video source, since each PSG is responsible for managing all video timing and synchronization signals.

The PSGs are also responsible for managing the camera control and auxiliary signals supported by the board. These signals are configurable signals that can support one or several functions, one of which is user-defined; the table in the next subsection identifies the functions to which the camera control and auxiliary signals can be defined. The PSGs are also responsible for implementing the functionality to which these can be defined.

Auxiliary signals

The following sections describe the auxiliary signals for Matrox Rapixo CL Pro.

Camera control and auxiliary signals for Matrox Rapixo CL Pro DB/QB

The following tables summarize the auxiliary functionality that the PSGs support, and the corresponding signals that the PSGs can receive/generate, for Matrox Rapixo CL Pro DB/QB. The table also documents the MIL constants to use.

		LVDS cam. ctrl				LVDS cam. ctrl				LVDS cam. ctrl				LVDS cam. ctrl			
		Camera Link Connector 0				Camera Link Connector 1				Camera Link Connector 2*				Camera Link Connector 3*			
M_CC_IO*n*	**n**	**1**	**2**	**3**	**4**	**1**	**2**	**3**	**4**	**1**	**2**	**3**	**4**	**1**	**2**	**3**	**4**
for M_DEV*m*†	**m**	**0**	**0**	**0**	**0**	**1**	**1**	**1**	**1**	**2**	**2**	**2**	**2**	**3**	**3**	**3**	**3**
Functionality that can be routed	**Acquisition path**	**CC1**	**CC2**	**CC3**	**CC4**	**CC1**	**CC2**	**CC3**	**CC4**	**CC1**	**CC2**	**CC3**	**CC4**	**CC1**	**CC2**	**CC3**	**CC4**
Timer (M_TIMER*n*†)	0	1/2	1/2	1/2	1/2												
	1					1/2	1/2	1/2	1/2								
	2									1/2	1/2	1/2	1/2				
	3													1/2	1/2	1/2	1/2
User output (bit of Camera Link static-user-output register M_USER_BIT_CC_IO*n*†)	0	0/1	0/1	0/1	0/1												
	1					0/1	0/1	0/1	0/1								
	2									0/1	0/1	0/1	0/1				
	3													0/1	0/1	0/1	0/1

*. Only available on Matrox Rapixo CL Pro QB

†. MIL constant, where *n* and *m* correspond to the number in the row. M_DEV*m* is the required device number of the digitizer (**MdigAlloc()**) that you must use to access this signal.

		TTL Aux I/O												OPTO Aux In								LVDS Aux In								LVDS Aux Out			
		Aux I/O Connector												Aux I/O Connector								Aux I/O Connector								Aux I/O Connector			
		A			C			B*			D			A		C		B*		D		A		C		B*		D		A	C	B*	D
M_AUX_IO*n*	n	8	9	2	8	9	3	8	9	2	8	9	3	6	7	0	1	6	7	0	1	10	11	4	5	10	11	4	5	12	12	13	13
for M_DEV*m*†	m	0	0	0/1	1	1	0/1	2	2	2/3	3	3	2/3	0	0	0/1	0/1	2	2	2/3	2/3	0	0	0/1	0/1	2	2	2/3	2/3	0	1	2	3
Functionality that can be routed or received	Acquisition path‡	TTL_AUX_IO_4	TTL_AUX_IO_5	TTL_AUX_IO_6	TTL_AUX_IO_12	TTL_AUX_IO_13	TTL_AUX_IO_14	TTL_AUX_IO_20	TTL_AUX_IO_21	TTL_AUX_IO_22	TTL_AUX_IO_28	TTL_AUX_IO_29	TTL_AUX_IO_30	OPTO_AUX_IN0	OPTO_AUX_IN1	OPTO_AUX_IN8	OPTO_AUX_IN9	OPTO_AUX_IN16	OPTO_AUX_IN17	OPTO_AUX_IN24	OPTO_AUX_IN25	LVDS_AUX_IN2	LVDS_AUX_IN3	LVDS_AUX_IN10	LVDS_AUX_IN11	LVDS_AUX_IN18	LVDS_AUX_IN19	LVDS_AUX_IN26	LVDS_AUX_IN27	LVDS_AUX_OUT7	LVDS_AUX_OUT15	LVDS_AUX_OUT23	LVDS_AUX_OUT31
Timer (M_TIMER*n*†)	0		1	2																										1/2			
	1					1	2																								1/2		
	2								1	2																						1/2	
	3											1	2																				1/2
Trigger controller affected by input signal§	0	T0	T1	T2			T3							T0	T1	T2	T3					T0	T1	T2	T3								
	1			T2	T0	T1	T3									T0/ T2	T1/ T3							T0/ T2	T1/ T3								
	2							T0	T1	T2			T3					T0	T1	T2	T3					T0	T1	T2	T3				
	3									T2	T0	T1	T3							T0/ T2	T1/ T3							T0/ T2	T1/ T3				
Timer-clock input	0																						0										
	1																								0								
	2																										0						
	3																												0				
Bit of quadrature input**	0																					0	1										
	1																							0	1								
	2																									0	1						
	3																											0	1				
User output (bit of main static-user-output register M_USER_BIT*n*†)	0	2	3	4			5																							0			
	1			4	2	3	5																								0		
	2							2	3	4			5																			0	
	3									4	2	3	5																				0

*. Matrox Rapixo CL Pro DB does not have this connector.

†. MIL constant, where *n* and *m* correspond to the number in the row. M_DEV*m* is the required device number of the digitizer (**MdigAlloc()**) that you must use to access this signal.

‡. Only Matrox Rapixo CL Pro QB has four acquisition paths. For Matrox Rapixo CL Pro DB, only information for acquisition paths 0 and 1 is applicable.

§. Note that there are only 4 trigger controllers per acquisition path.

**. A rotary/linear encoder with quadrature output transmits a two-bit code. The table entries 0 and 1, therefore, denote bit position.

Type of signal	Acquisition path	LVDS cam. ctrl															
		CL connect. 0				CL connect. 1				CL connect. 2				CL connect. 3			
		CC1	CC2	CC3	CC4	CC1	CC2	CC3	CC4	CC1	CC2	CC3	CC4	CC1	CC2	CC3	CC4
VSYNC output	0	1	1	1	1												
	1					1	1	1	1								
	2									1	1	1	1				
	3													1	1	1	1
HSYNC output	0	1	1	1	1												
	1					1	1	1	1								
	2									1	1	1	1				
	3													1	1	1	1
Clock output	0	1	1	1	1												
	1					1	1	1	1								
	2									1	1	1	1				
	3													1	1	1	1

The following table lists the auxiliary input signals (or auxiliary I/O signals set to input) that can be rerouted onto output signals and the output signals onto which they can be rerouted.

			LVDS cam. ctrl																TTL Aux I/O												LVDS Aux Out			
			Camera Link Connector 0				Camera Link Connector 1				Camera Link Connector 2				Camera Link Connector 3				Aux I/O Connector												Aux I/O Connector			
																			A			C			B*			D			A	C	B*	D
M_AUX_IO*x* or M_CC_IO*y* for M_DEV*z*†		x																	8	9	2	8	9	3	8	9	2	8	9	3	12	12	13	13
		y	1	2	3	4	1	2	3	4	1	2	3	4	1	2	3	4																
		z	0	0	0	0	1	1	1	1	2	2	2	2	3	3	3	3	0	0	0/1	1	1	0/1	2	2	2/3	3	3	2/3	0	1	2	3
Auxiliary input signal (or auxiliary I/O signal set to input)	**M_AUX_IO*x***	**Acquisition path**	CC1	CC2	CC3	CC4	CC1	CC2	CC3	CC4	CC1	CC2	CC3	CC4	CC1	CC2	CC3	CC4	TTL_AUX_IO_4	TTL_AUX_IO_5	TTL_AUX_IO_6	TTL_AUX_IO_12	TTL_AUX_IO_13	TTL_AUX_IO_14	TTL_AUX_IO_20	TTL_AUX_IO_21	TTL_AUX_IO_22	TTL_AUX_IO_28	TTL_AUX_IO_29	TTL_AUX_IO_30	LVDS_AUX_OUT7	LVDS_AUX_OUT15	LVDS_AUX_OUT23	LVDS_AUX_OUT31
TTL_AUX_IO_4	8	0	•	•	•	•																												
TTL_AUX_IO_5	9	0																																
TTL_AUX_IO_6	2	0/1	•	•	•	•	•	•	•	•																								
TTL_AUX_IO_12	8	1					•	•	•	•																								
TTL_AUX_IO_13	9	1																																
TTL_AUX_IO_14	3	0/1																																
TTL_AUX_IO_20*	8	2									•	•	•	•																				
TTL_AUX_IO_21*	9	2																																
TTL_AUX_IO_22*	2	2/3									•	•	•	•	•	•	•	•																
TTL_AUX_IO_28	8	3													•	•	•	•																
TTL_AUX_IO_29	9	3																																
TTL_AUX_IO_30	3	2/3																																

		LVDS cam. ctrl																TTL Aux I/O												LVDS Aux Out			
		Camera Link Connector 0				Camera Link Connector 1				Camera Link Connector 2				Camera Link Connector 3				Aux I/O Connector												Aux I/O Connector			
																		A			C			B*			D			A	C	B*	D
M_AUX_IOx or M_CC_IOy for M_DEVz†	x																	8	9	2	8	9	3	8	9	2	8	9	3	12	12	13	13
	y	1	2	3	4	1	2	3	4	1	2	3	4	1	2	3	4																
	z	0	0	0	0	1	1	1	1	2	2	2	2	3	3	3	3	0	0	0/1	1	1	0/1	2	2	2/3	3	3	2/3	0	1	2	3
Auxiliary input signal (or auxiliary I/O signal set to input)	**M_AUX_IOx**	**Acquisition path**	**CC1**	**CC2**	**CC3**	**CC4**	**CC1**	**CC2**	**CC3**	**CC4**	**CC1**	**CC2**	**CC3**	**CC4**	**CC1**	**CC2**	**CC3**	**CC4**	TTL_AUX_IO_4	TTL_AUX_IO_5	TTL_AUX_IO_6	TTL_AUX_IO_12	TTL_AUX_IO_13	TTL_AUX_IO_14	TTL_AUX_IO_20	TTL_AUX_IO_21	TTL_AUX_IO_22	TTL_AUX_IO_28	TTL_AUX_IO_29	TTL_AUX_IO_30	LVDS_AUX_OUT7	LVDS_AUX_OUT15	LVDS_AUX_OUT23	LVDS_AUX_OUT31
OPTO_AUX_IN0	6	0																															
OPTO_AUX_IN1	7	0	•	•	•	•																											
OPTO_AUX_IN8	0	0/1					•	•	•	•																							
OPTO_AUX_IN9	1	0/1	•	•	•	•	•	•	•	•																							
OPTO_AUX_IN16	6	2																															
OPTO_AUX_IN17	7	2									•	•	•	•																			
OPTO_AUX_IN24	0	2/3													•	•	•	•															
OPTO_AUX_IN25	1	2/3									•	•	•	•	•	•	•	•															
LVDS_AUX_IN2	10	0	•	•	•	•																											
LVDS_AUX_IN3	11	0																															
LVDS_AUX_IN10	4	0/1					•	•	•	•																							
LVDS_AUX_IN11	5	0/1	•	•	•	•	•	•	•	•																							
LVDS_AUX_IN18‡	10	2									•	•	•	•																			
LVDS_AUX_IN19‡	11	2																															
LVDS_AUX_IN26	4	2/3													•	•	•	•															
LVDS_AUX_IN27	5	2/3									•	•	•	•	•	•	•	•															

*. Matrox Rapixo CL Pro DB does not have this connector or signal.

†. MIL constant, where *x*, *y*, and *z* correspond to the numbers in the row. M_DEV*z* is the required device number of the digitizer (**MdigAlloc()**) that you must use to access this signal.

‡. Matrox Rapixo CL Pro DB does not have this signal.

Camera control and auxiliary signals for Matrox Rapixo CL Pro SF/DF

The following tables summarize the auxiliary functionality that the PSGs support, and the corresponding signals that the PSGs can receive/generate, for Matrox Rapixo CL Pro SF/DF. The table also documents the MIL constants to use.

		LVDS cam. ctrl				LVDS cam. ctrl			
		Camera Link Connector 0				Camera Link Connector 2*			
M_CC_IO*n*	**n**	**1**	**2**	**3**	**4**	**1**	**2**	**3**	**4**
for M_DEV*m*†	**m**	**0**	**0**	**0**	**0**	**1**	**1**	**1**	**1**
Functionality that can be routed	**Acquisition path**	**CC1**	**CC2**	**CC3**	**CC4**	**CC1**	**CC2**	**CC3**	**CC4**
Timer (M_TIMER*n*†)	0	1/2	1/2	1/2	1/2				
	1					1/2	1/2	1/2	1/2
User output (bit of Camera Link static-user-output register M_USER_BIT_CC_IO*n*†)	0	0/1	0/1	0/1	0/1				
	1					0/1	0/1	0/1	0/1

*. Only available on Matrox Rapixo CL Pro DF.

†. MIL constant, where *n* and *m* correspond to the number in the row. M_DEV*m* is the required device number of the digitizer (**MdigAlloc()**) that you must use to access this signal.

		TTL Aux I/O								OPTO Aux In								LVDS Aux In								LVDS Aux Out	
		Aux I/O Connector								Aux I/O Connector								Aux I/O Connector								Aux I/O Connector	
		A		C		B*		D		A		C		B*		D		A		C		B*		D		A	B*
M_AUX_IO*n*	**n**	8	9	2	3	8	9	2	3	6	7	0	1	6	7	0	1	10	11	4	5	10	11	4	5	12	13
for M_DEV*m*†	**m**	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	1
Functionality that can be routed or received	**Acquisition path‡**	TTL_AUX_IO_4	TTL_AUX_IO_5	TTL_AUX_IO_6	TTL_AUX_IO_14	TTL_AUX_IO_20	TTL_AUX_IO_21	TTL_AUX_IO_22	TTL_AUX_IO_30	OPTO_AUX_IN0	OPTO_AUX_IN1	OPTO_AUX_IN8	OPTO_AUX_IN9	OPTO_AUX_IN16	OPTO_AUX_IN17	OPTO_AUX_IN24	OPTO_AUX_IN25	LVDS_AUX_IN2	LVDS_AUX_IN3	LVDS_AUX_IN10	LVDS_AUX_IN11	LVDS_AUX_IN18	LVDS_AUX_IN19	LVDS_AUX_IN26	LVDS_AUX_IN27	LVDS_AUX_OUT7	LVDS_AUX_OUT23
Timer	0		1	2																						1/2	
(M_TIMER*n*†)	1						1	2																			1/2
Trigger controller affected by input signal§	0	T0	T1	T2	T3					T0	T1	T2	T3					T0	T1	T2	T3						
	1					T0	T1	T2	T3					T0	T1	T2	T3					T0	T1	T2	T3		
Timer-clock input	0																		0								
	1																						0				
Bit of quadrature input**	0																	0	1								
	1																					0	1				
User output (bit of main static-user-output register M_USER_BIT*n*†)	0	2	3	4	5																					0	
	1					2	3	4	5																		0

*. Matrox Rapixo CL Pro SF does not have this connector.

†. MIL constant, where *n* and *m* correspond to the number in the row. M_DEV*m* is the required device number of the digitizer (**MdigAlloc()**) that you must use to access this signal.

‡. Only Matrox Rapixo CL Pro DF has two acquisition paths. For Matrox Rapixo CL Pro SF, only information for acquisition path 0 is applicable.

§. Note that there are only 4 trigger controllers per acquisition path.

**. A rotary encoder with quadrature output transmits a two-bit code. The table entries 0 and 1, therefore, denote bit position.

Type of signal	Acquisition path	LVDS cam. ctrl							
		CL connect. 0				CL connect. 2			
		CC1	CC2	CC3	CC4	CC1	CC2	CC3	CC4
VSYNC output	0	1	1	1	1				
	1					1	1	1	1
HSYNC output	0	1	1	1	1				
	1					1	1	1	1
Clock output	0	1	1	1	1				
	1					1	1	1	1

The following table lists the auxiliary input signals (or auxiliary I/O signals set to input) that can be rerouted onto output signals and the output signals onto which they can be rerouted.

			LVDS cam. ctrl								TTL Aux I/O								LVDS Aux Out	
			Camera Link Connector 0				Camera Link Connector 2				Aux I/O Connector								Aux I/O Connector	
											A			C	B*			D	A	B*
M_AUX_IO*x* or M_CC_IO*y* for M_DEV*z*†	x										8	9	2	3	8	9	2	3	12	13
	y		1	2	3	4	1	2	3	4										
	z		0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	1
Auxiliary input signal (or auxiliary I/O signal set to input)	M_AUX_IO*x*	Acquisition path	CC1	CC2	CC3	CC4	CC1	CC2	CC3	CC4	TTL_AUX_IO_4	TTL_AUX_IO_5	TTL_AUX_IO_6	TTL_AUX_IO_14	TTL_AUX_IO_20	TTL_AUX_IO_21	TTL_AUX_IO_22	TTL_AUX_IO_30	LVDS_AUX_OUT7	LVDS_AUX_OUT23
TTL_AUX_IO_4	8	0	•	•	•	•														
TTL_AUX_IO_5	9	0																		
TTL_AUX_IO_6	2	0	•	•	•	•														
TTL_AUX_IO_14	3	0																		
TTL_AUX_IO_20*	8	1					•	•	•	•										
TTL_AUX_IO_21*	9	1																		
TTL_AUX_IO_22*	2	1					•	•	•	•										
TTL_AUX_IO_30	3	1																		
OPTO_AUX_IN0	6	0																		
OPTO_AUX_IN1	7	0	•	•	•	•														
OPTO_AUX_IN8	0	0																		
OPTO_AUX_IN9	1	0	•	•	•	•														
OPTO_AUX_IN16	6	1																		
OPTO_AUX_IN17	7	1					•	•	•	•										
OPTO_AUX_IN24	0	1																		
OPTO_AUX_IN25	1	1					•	•	•	•										

			LVDS cam. ctrl								TTL Aux I/O								LVDS Aux Out	
			Camera Link Connector 0				Camera Link Connector 2				Aux I/O Connector								Aux I/O Connector	
											A			C	B*			D	A	B*
M_AUX_IO*x* or M_CC_IO*y* for M_DEV*z*†		x									8	9	2	3	8	9	2	3	12	13
		y	1	2	3	4	1	2	3	4										
		z	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	1
Auxiliary input signal (or auxiliary I/O signal set to input)	**M_AUX_IO*x***	**Acquisition path**	**CC1**	**CC2**	**CC3**	**CC4**	**CC1**	**CC2**	**CC3**	**CC4**	TTL_AUX_IO_4	TTL_AUX_IO_5	TTL_AUX_IO_6	TTL_AUX_IO_14	TTL_AUX_IO_20	TTL_AUX_IO_21	TTL_AUX_IO_22	TTL_AUX_IO_30	LVDS_AUX_OUT7	LVDS_AUX_OUT23
LVDS_AUX_IN2	10	0	•	•	•	•														
LVDS_AUX_IN3	11	0																		
LVDS_AUX_IN10	4	0																		
LVDS_AUX_IN11	5	0	•	•	•	•														
LVDS_AUX_IN18‡	10	1					•	•	•	•										
LVDS_AUX_IN19‡	11	1																		
LVDS_AUX_IN26	4	1																		
LVDS_AUX_IN27	5	1					•	•	•	•										

*. Matrox Rapixo CL Pro SF does not have this connector or signal.

†. MIL constant, where *x*, *y*, and *z* correspond to the numbers in the row. M_DEV*z* is the required device number of the digitizer (**MdigAlloc()**) that you must use to access this signal.

‡. Matrox Rapixo CL Pro SF does not have this signal.

Specifications of the auxiliary signals

Matrox Rapixo CL Pro has auxiliary signals in the following formats:

Signal Format	Total # of signals							
	SF		DF		DB		QB	
	No cable bracket	With cable bracket	No cable bracket	With cable bracket	No cable bracket	With cable bracket	No cable bracket	With cable bracket
TTL auxiliary input or output signals	3	9	6	12	3	9	6	12
Opto-isolated auxiliary input signals	2	6	4	8	2	6	4	8
LVDS auxiliary input signals	2	6	4	8	2	6	4	8
LVDS auxiliary output signals	1	3	2	4	1	3	2	4
LVDS camera control output signals	4	4	8	8	8	8	16	16
Total number of auxiliary signals	12	28	24	40	16	32	32	48

When you route an external signal to an auxiliary signal or vice versa, verify that the external signal meets the electrical specifications of the auxiliary signal.

When an auxiliary input signal is received in TTL format directly, it will be clamped at a maximum of 5.7 V and at a minimum of -0.7 V to protect the input buffer. Typically, the signal should have a maximum of 5 V and a minimum of 0 V. A signal over 2 V is considered high, while anything less than 0.8 V is considered low.

The opto-isolated auxiliary input signals pass through an opto-coupler, a device that protects the board from outside surges and different ground levels, and allows the frame grabber to be totally isolated. The voltage difference across the positive and negative components of the signal must be between 4.71 V and 9.165 V for logic high, and between -5.0 V and 0.8 V for logic low.

You can set the direction of an auxiliary I/O signal using the MIL-Lite function **MdigControl**() with **M_AUX_SIGNAL_MODE**.

You can set up the auxiliary signals in the DCF. Alternatively, for most commonly used functionalities, you can configure the auxiliary signals using the MIL-Lite function **MdigControl**() (for example, with **M_IO...**, **M_GRAB_TRIGGER...**, **M_TIMER...**, or **M_ROTARY_ENCODER...**).

Timers

Matrox Rapixo CL Pro has up to eight 24-bit timers (2 per acquisition path), which operate on a specified clock source. Timer output signals allow you to control the exposure time and other external events related to the video source (such as a strobe). A timer output signal can be output on any of the auxiliary output signals or auxiliary I/O signals in output mode.

The timers can use one of the following as a clock source:

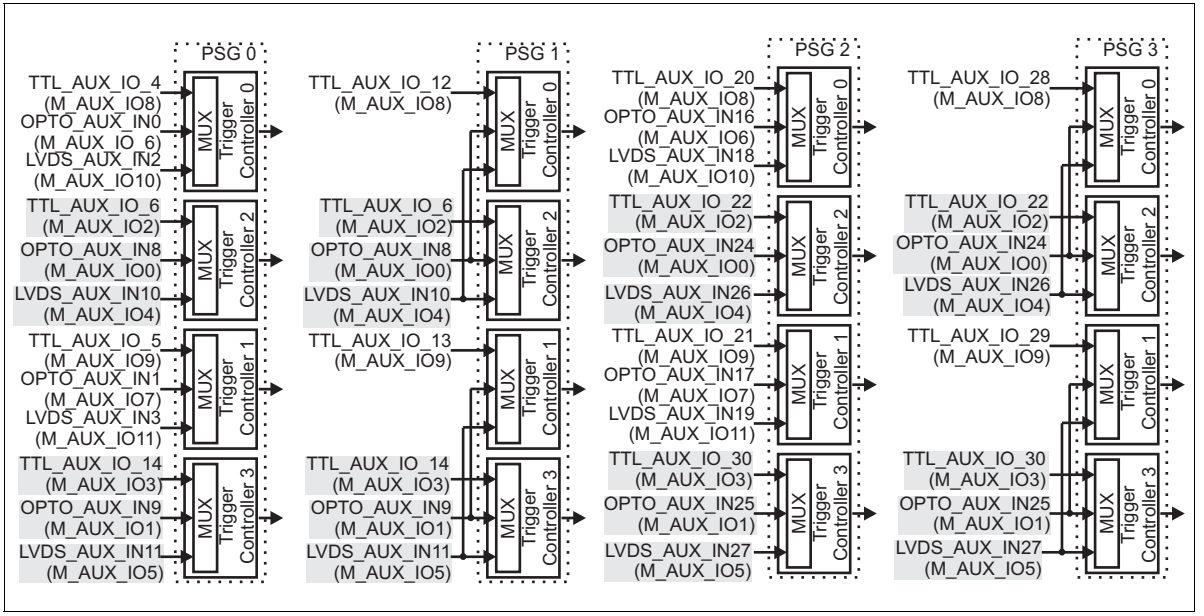
- **A 125 MHz internal clock source.**
- **A clock based on the output of another timer set in continuous mode.**
- **A clock based on the HSYNC or VSYNC signal of your camera.**
- **A clock based on the pixel clock signal of your camera.**

To route a timer output on an auxiliary signal, use the MIL-Lite function **MdigControl**() with **M_IO_SOURCE + M_AUX_IOn** set to **M_TIMERm**. To set up a timer, use **MdigControl**() with **M_TIMER_...**.

Trigger

You can use as a trigger any of the auxiliary input signals (or auxiliary I/O signals in input mode) of Matrox Rapixo CL Pro. A trigger signal can be used to initiate image acquisition, or prompt an on-board event.

Each PSG has 4 trigger controllers. Each trigger controller can trigger the image acquisition, the timers, and/or the synchronization signals of the PSG's acquisition path. Only one auxiliary signal per trigger controller can be programmed as a trigger input signal. The auxiliary signals are restricted to specific trigger controllers.



Timing requirements

When you use an auxiliary input signal as a trigger, the pulse width of the signal must be at least 16 nsec (2 clock periods at 125 MHz).

To enable grabbing upon a trigger, use the MIL-Lite function **MdigControl**() with **M_GRAB_TRIGGER_STATE.** To set the signal used to trigger the grab, use **MdigControl**() with **M_GRAB_TRIGGER_SOURCE.** To start a timer upon a trigger, use **MdigControl**() with **M_TIMER_TRIGGER_SOURCE**.

Quadrature decoder

Matrox Rapixo CL Pro features 4 quadrature decoders. They are used to decode quadrature input received from rotary or linear encoders with a quadrature output. A rotary encoder is a device that provides information about the position and direction of a rotating shaft (for example, that of a conveyor belt); a linear encoder is a device that provides information about the position and direction of a moving sensor along a scale. Encoders with quadrature output transmit a two-bit code (also known as Gray code) on two pairs of LVDS wires for each change in position of the rotating shaft, or of the sensor along the scale. For a given direction, the encoder outputs the code in a precise sequence (either 00 - 01 - 11 - 10 or 00 - 10 - 11 - 01, depending on how the encoder is attached. If the rotating shaft, or sensor moving along the scale, changes direction, the encoder transmits the Gray code in the reverse sequence (00 - 10 - 11 - 01 or 00 - 01- 11 - 10, respectively).

Upon decoding a Gray code, the quadrature decoder increments or decrements its 32-bit internal counter, depending on the direction of movement. You can configure which Gray code sequence represents forward movement and increments the counter; the reverse Gray code sequence will then represent the backward direction and decrement the counter. You can specify the direction of movement occurring when the Gray code sequence is 00 - 01 - 11 - 10, using **MdigControl**() with **M_ROTARY_ENCODER_DIRECTION**.

The quadrature decoder supports encoder frequencies of up to 50 MHz. The LVDS receivers of the Matrox Rapixo CL Pro board support an input voltage from -4 V to +5 V on either LVDS signal, and a maximum differential of 3 V between the two LVDS signals.

- Note that an external source must be used to power the rotary/linear encoder (for example, your computer's 5 V power source).

You can configure the quadrature decoder's settings, using the MIL-Lite function **MdigControl**() with **M_ROTARY_ENCODER...**, or by modifying the DCF file with Matrox Intellicam.

User signals

Auxiliary signals can also be used to transmit or receive application-specific user output and/or input.

If you want to start or stop an external event based on some calculation or analysis, you can manually set the state of any auxiliary output signal (or I/O signal set to output) to high or low. To do so, you set the state (on/off) of a bit in a user settable register (static-user-output register). When the bit is on, its associated auxiliary output signal will be high; when it is off, the auxiliary output signal will be low. This bit is referred to as a user-bit. To route the state of a user-bit to an auxiliary output signal, use **MdigControl**() with **M_IO_SOURCE** and **M_USER_BITn**; to set the state of a user-bit, use **MdigControl**() with **M_USER_BIT_STATE**.

Your application can also act upon and interpret the state of an auxiliary input signal (or I/O signal set to input). The state of an auxiliary input signal is not associated with a user-bit; you poll the state of the signal directly. To poll the state of an auxiliary input signal, use **MdigInquire**() with **M_IO_STATUS**. The state of an auxiliary input signal can also generate an interrupt; to do so, use **MdigControl**() with **M_IO_INTERRUPT_STATE** and then use **MdigHookFunction**() with **M_IO_CHANGE** to hook a function to this event (that is, to set up an event handler).

On-board memory

Matrox Rapixo CL Pro is equipped with 4 Gbytes of DDR3 SDRAM on-board memory. This memory is accessed through the memory controller, and is used to store acquired images and images for or resulting from processing. The memory interface transfers data to and from memory at up to 14.4 Gbytes/sec.

Matrox Rapixo CL Pro has 128 Mbytes of memory mapped onto the PCIe bus. You can use a Host pointer to access this memory, or you can access it directly from another PCIe bus master; this memory is referred to as shared memory. To allocate a buffer in shared memory, use the MIL-Lite function **MbufAlloc...**() with **M_ON_BOARD + M_SHARED**.

Data conversion

The color space converter and image formatter can convert data in the following ways:

- **Subsampling.** Image data can be subsampled.

  The color space converter and image formatter can subsample in the horizontal and vertical directions by integer factors of 1 to 16. The color space converter and image formatter uses nearest-neighbor interpolation.

  You can use any of the following MIL-Lite functions to subsample image data:

  - **MdigControl**() with **M_GRAB_SCALE_X/Y**, using a factor of less than 1.
  - **MimResize**() with ScaleFactorX and ScaleFactorY set to a value less than 1.
  - **MbufTransfer**() with **M_COPY + M_SCALE**, setting the destination buffer size smaller than the original image.

  Note that Matrox Rapixo CL Pro does not support cropping in hardware. However, you can have image data cropped during transfer to Host using **MdigControl**() with **M_SOURCE_SIZE_X/Y** and **M_SOURCE_OFFSET_X/Y.**

- **Flipping.** Images can be flipped horizontally or vertically, using the MIL-Lite function **MdigControl**() with **M_GRAB_DIRECTION_X/Y** or when calling **MimFlip**() from on-board buffer to Host.

- **Color space conversion.** The color space converter and image formatter formats an image based on its type and the bit-depth and color format of the destination buffer. You can set the bit depth and color format of the destination buffer when you allocate it using the MIL-Lite function **MbufAlloc...**(). The format of the source image is established in the DCF.

Image data can be converted as follows:

Input format	Output format							
	8-bit monochrome	**16-bit monochrome**	**24-bit packed BGR**	**32-bit packed BGRa**	**48-bit packed BGR**	**16-bit YUV (YUYV)**	**24-bit RGB planar**	**48-bit RGB planar**
8-bit monochrome	yes		yes	yes		yes	yes	
16-bit monochrome	yes	yes	yes	yes	yes	yes	yes	yes
24-bit packed BGR	yes		yes	yes		yes	yes	
48-bit packed BGR	yes	yes	yes	yes	yes	yes	yes	yes

The equations for the YUV16 conversion are described in the following table. The value of *depth* is either 8 or 16 when converting BGR24 or BGR48 data, respectively. Note that while performing BGR48-to-YUV color space conversion, the operations are carried out on 16-bit data; then, each resulting YUV component is bit-shifted right by 8 bits (>> (*depth* - 8) where the value of *depth* is 16).

Color space conversion	Equations
BGR-to-YUV	• $Y = (0.114B + 0.587G + 0.299R) >> (depth - 8)$ • $U = (0.500B - 0.331G - 0.169R + 2^{(depth-1)}) >> (depth - 8)$ • $V = (-0.081B - 0.419G + 0.500R + 2^{(depth-1)}) >> (depth - 8)$

Processing FPGA

To reduce the number of image processing tasks that the Host CPU must perform, the Matrox Rapixo CL Pro has a Processing FPGA. The Processing FPGA on Matrox Rapixo CL Pro is a highly customizable Xilinx Kintex-7 (325T)*. The Processing FPGA can be configured to offload and even accelerate the most compute-intensive part of typical image processing applications, without generating additional data traffic within the host computer (Host).

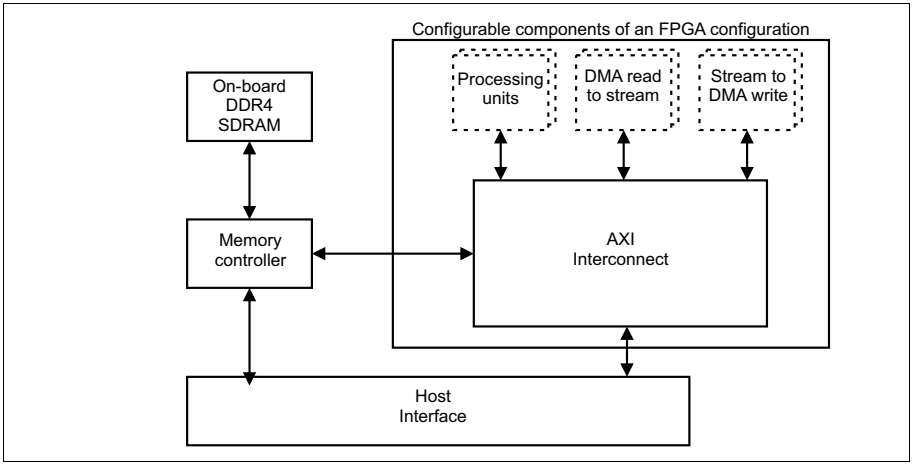
Before the Processing FPGA can process grabbed images, they must be stored in on-board memory. If images stored in Host memory are required, they can be streamed directly to the Processing FPGA for processing. Images and other data resulting from processing can be stored in on-board memory or streamed to the Host.

The maximum peak bandwidth for images streamed directly to/from Host memory is 8 Gbyte/sec, as well as for images streamed to/from on-board memory.

*. Other functionality is also implemented through the FPGA, besides customizable processing, such as the timers and quadrature decoders.

Possible processing operations

To use the Processing FPGA, you must configure it with an FPGA configuration that defines the appropriate functionality. An FPGA configuration is a code segment that is used to program an FPGA.The following diagram shows the configurable FPGA components in an FPGA configuration.



You would typically use standard Matrox FPGA configurations. You can also chose to implement processing on your own, using the Matrox FPGA Developers Toolkit (FDK) and C++. If required, Matrox's FPGA design services can be employed to develop an application-specific FPGA configuration.

Once the Processing FPGA is programmed, you can then make use of its functionality using MIL. Refer to *Using MIL with a Processing FPGA* chapter in the *MIL User Guide* for more information

Host interface

The Matrox Rapixo CL Pro PCIe 2.0 Host interface is capable of high-speed DMA transfers to Host memory, or other memory mapped onto the PCIe bus that are compliant with the PCI Express Base Specification, rev 2.1. The DMA write engine of the Host interface is capable of performing the transfers without the help of the Host CPU.

Matrox Rapixo CL Pro uses PCIe 2.0 technology to communicate with the Host. Under optimum conditions, Matrox Rapixo CL Pro can send data to the Host at a peak transfer rate of up to 4 Gbytes/sec. Optimum conditions include using the board in a PCIe 2.x slot or above with 8 active lanes, using a 256-byte payload.

DMA write performance is chipset and computer dependent, and is slightly affected by the image size and alignment in Host memory.

The Matrox Rapixo CL Pro Host interface has four DMA write contexts, which act independently, simulating four DMA write engines running in parallel. The presence of multiple DMA contexts does not change the maximum bandwidth, but can help reduce latency.

Appendix A: Glossary

This appendix defines some of the specialized terms used in the Matrox Rapixo CL Pro documentation.

Glossary

- **Acquisition path.**

  A path that has the components to, for example, digitize or capture a video input signal. Some video sources require multiple acquisition paths.

- **ASPM.**

  Active State Power Management. A hardware PCIe mechanism that autonomously controls power consumption of the PCIe connectors in a computer. The actual power consumed by a PCIe device depends on the PCIe traffic and on the power-saving level to which the PCIe slot is configured. The power-saving level of the PCIe slot is initialized by the operating system.

- **Auxiliary I/O.**

  Auxiliary input/output. Non-video digital signals that can support one or more functionalities depending on the auxiliary signal (for example, trigger input or timer output).

- **Bandwidth.**

  A term describing the capacity to transfer data. Greater bandwidth is needed to sustain a higher transfer rate. Greater bandwidth can be achieved, for example, by using a wider bus or by increasing the clock frequency at which an interface or a processing core operates (for example, increasing the DDR3 SDRAM clock frequency).

- **Camera Link.**

  A serial communication protocol standard designed for computer vision applications based on the National Semiconductor interface Channel-link. It was designed for the purpose of standardizing scientific and industrial video products including cameras, cables and frame grabbers.

- **Contiguous memory.**

  A block of memory occupying a single, unbroken series of addresses.

- **DCF.**

  Digitizer configuration format. A format that defines how the video source and the frame grabber are configured. The video source and the frame grabber are set to the specified camera mode, which defines the format of transferred data. The DCF can also configure the triggers, timers, and quadrature decoders.

  DCF files have a *.dcf* extension.

- **DDR3 SDRAM.**

  Double-data-rate type 3 synchronous dynamic random-access memory. A type of general purpose consumer RAM. DDR3 SDRAM allows for data transfer at very high speeds, which is important for I/O-bound functions. This type of memory is inexpensive, high density, and very efficient as long as the data is accessed contiguously.

- **Digitizer configuration format.**

  See *DCF.*

- **Dynamic range.**

  The range of values present in a buffer. An unsigned 8-bit buffer, for example, has an allowable range of 0 to 255; its dynamic range can be any range within these values.

- **Exposure time.**

  Refers to the period during which the image sensor of a video source is exposed to light. As the length of this period increases, so does the image brightness.

- **Frame.**

  A single image grabbed from a video source.

- **Grab.**

  To acquire an image from a video source.

- **Latency.**

  The time from when a command is sent to when its operation is started.

- **LVDS.**

  Low-voltage differential signaling. LVDS offers a general-purpose, high bandwidth interface standard for serial and parallel data interfaces that require increased bandwidth at high speed, with low noise and power consumption.

- **PCIe.**

  Peripheral Component Interconnect Express. The standard used for the computer bus that acts as an interface between hardware devices, such as Matrox Rapixo CL Pro and your computer.

- **Payload.**

  The amount of data transmitted to the PCIe bus within each data packet. Common payload sizes are 128, 256, 512, 1024, 2048, and 4096 bytes.

- **Quadrature decoder.**

  A device that decodes input received from a rotary or linear encoder with quadrature output.

- **Real-time processing.**

  The processing of an image at the same speed or faster than the speed at which images are grabbed. Real-time processing ensures that no frames are missed.

  Also known as *live processing*.

- **Rotary encoder.**

  A device used to convert the angular position of a shaft or axle, to an analog or digital code.

- **Timer output.**

  The signal generated by one of the programmable timers of the frame grabber. The timer output can be used to control external hardware. For example, it can be fed to the video source to control its exposure time or can be used to fire a strobe light.

Appendix B: Technical information

This appendix contains information that might be useful when installing your Matrox Rapixo CL Pro board.

Board summary

Global information

- Operating system: See your software manual for supported versions of Microsoft Windows and Linux.

- Minimum computer requirements:

  - x8 (or x16) PCIe 2.x or 3.x slot* or later.

  - Processor with an Intel 32-bit or 64-bit architecture, or equivalent.

  - A relatively up-to-date PCIe chipset. A chipset that supports the PCIe 2.x standard is preferable. The list of platforms that are known to be compatible with Matrox Rapixo CL Pro is available on the Matrox website, under the board's PC compatibility list.

  - A proper power supply. Refer to the *Electrical specifications* section.

  Matrox does not guarantee compatibility with all computers that have the above specifications. Please consult with your local Matrox Imaging representative, local Matrox Imaging sales office, the Matrox web site, or the Matrox Imaging Customer Support Group at headquarters before using a specific computer.

*. Note that you can also install Matrox Rapixo CL Pro in a x4 PCIe slot that has a mechanical x8 connector; however, the maximum transfer rate between Matrox Rapixo CL Pro and the Host is reduced by 50%.

Technical features of Matrox Rapixo CL Pro

- Has a x8 PCIe 2.0 Host interface.
- Supports frame-scan (scan-area) and line-scan video sources compliant with the Camera Link 2.1 specification (or earlier). The minimum and maximum number of pixels per line are 33 and 65535, respectively.
- Matrox Rapixo CL Pro DB has two independent acquisition paths; Matrox Rapixo CL Pro QB has four independent acquisition paths. Each acquisition path supports a video source in the Camera Link Base configuration.
- Matrox Rapixo CL Pro SF has a single acquisition path; Matrox Rapixo CL Pro DF has two acquisition paths. Each acquisition path supports a video source in the Camera Link Medium, Full, 72-bit, or 80-bit configuration.
- Supports video sources with a Bayer color filter. Bayer-encoded data (GRBG, GBRG, BGGR, or RGGB) is converted to RGB.
- Can convert 8- or 16-bit monochrome or 24- or 48-bit packed BGR data to monochrome, packed or planar BGR, packed BGRa, or YUV (YUYV) format.
- Can perform horizontal or vertical flipping.
- Can subsample image data by integer subsampling factors of 1 to 16.
- Supports external 5 V rotary/linear encoders with quadrature output.
- Can provide power-over-Camera Link (PoCL) with SafePower. The PoCL protection on-board fuse can sustain a current of 0.4 A.
- Has four camera control signals (re-routing of specific auxiliary input signals, HSYNC output, VSYNC output, clock output, timer output, or user output) per acquisition path*.

*. See the *Camera control and auxiliary signals for Matrox Rapixo CL Pro DB/QB* and *Camera control and auxiliary signals for Matrox Rapixo CL Pro SF/DF* sections in *Chapter 4: Matrox Rapixo CL Pro hardware reference* chapter for supported functionality.

- Supports extended Camera Link cables, for a cable length of up to 15 m at 85 MHz.

- Has up to 32 auxiliary signals that can be path independent or path dependent, depending on the functionality* selected*. When path dependent, there are:

  - Three TTL auxiliary I/O signals (trigger input or user input, or timer output or user output) per acquisition path.

  - One LVDS auxiliary output signal (timer output or user output) per acquisition path.

  - Two LVDS auxiliary input signals (trigger input, timer-clock input, quadrature input, or user input) per acquisition path.

  - Two opto-isolated auxiliary input signals (trigger input or user input) per acquisition path.

- Has a PoCL LED for each input connector, to identify whether the connector is providing power to the camera or not. Matrox Rapixo CL Pro DB and QB have four PoCL LEDs, while Matrox Rapixo CL Pro SF and DF have two.

- Has three board status LEDs to indicate the status of each of the following: power, firmware configuration, and PCIe (Host) slot.

*. For example, for Matrox Rapixo CL Pro DB and QB, TTL_AUX_IO_14 can be used as a trigger input when grabbing from acquisition path 0 or 1; alternatively, you can configure it as an output signal and route the output of Timer 2 to this signal. You can only route timer 2 of acquisition path 1 to the TTL_AUX_IO_14 signal.

Electrical specifications

The following tables describes the electrical specifications of Matrox Rapixo CL Pro.

Operating voltage and current for Matrox Rapixo CL Pro
Max. PoCL 12.0 V, 1.6 A: 19.2 W* (Current directly drawn from the slot. Power is not dissipated by the board; it is only used by the camera).

*. The PoCL protection fuse on Matrox Rapixo CL Pro can sustain a current of 0.4 A.

I/O Specifications for Matrox Rapixo CL Pro		
	Input signals in LVDS format	100 Ohm differential termination. Input current: -10 µA (min) to +10 µA (max). Common-mode: -4 V (min) to +5 V (max). Differential input: 0.1 V (min) to +3 V (max). Differential threshold: low of -50 mV (negative input voltage); high of +50 mV (positive input voltage).
	Output signals in LVDS format	No parallel termination. Output current: -10 µA to 10 µA. Output voltage: high (V_{oh}) 1.6 V (max), 1.33 V (typ); low (V_{ol}) 0.9 V (min), 1.02 V (typ) Differential output voltage (with load of 100 Ohm): 250 mV (min) to 450 mV (max). Offset voltage (common-mode): 1.125 V (min) to 1.375 V (max). Propagation delay: 2.8 ns (max).
	Input signals in TTL format	No series termination.Doc-10281 Pulled up to 3.3 V with 4.716 K Ohm. Clamped to -0.7 V to +5.7 V. Input current: 5 µA (max). Input voltage: low of 0.8 V (max); high of 2.0 V (min).
	Output signals in TTL format	27 Ohm series termination. High-level output current: -32 mA (max). Low-level output current: +64 mA (max). Output voltage: low of 0.55 V (max); high of 2.0 V (min).
	Opto-coupled input signals*	511 Ohm series termination (connected on the anode inputs of the opto-coupler device). Input current: low: 250 µA (max); high: 5 mA (min (thresholded)) to 15 mA (max) (6.3 to 10 mA recommended). Input voltage: low (V_{il}) of 0.8 V (max); high (V_{ih}) of 4.71 V (min) to 9.165 V (max). Input forward voltage (at 25 degrees C): 1.3 V (min), 1.8 V (max). Propagation delay (at 25 degrees C): 100 ns (max).

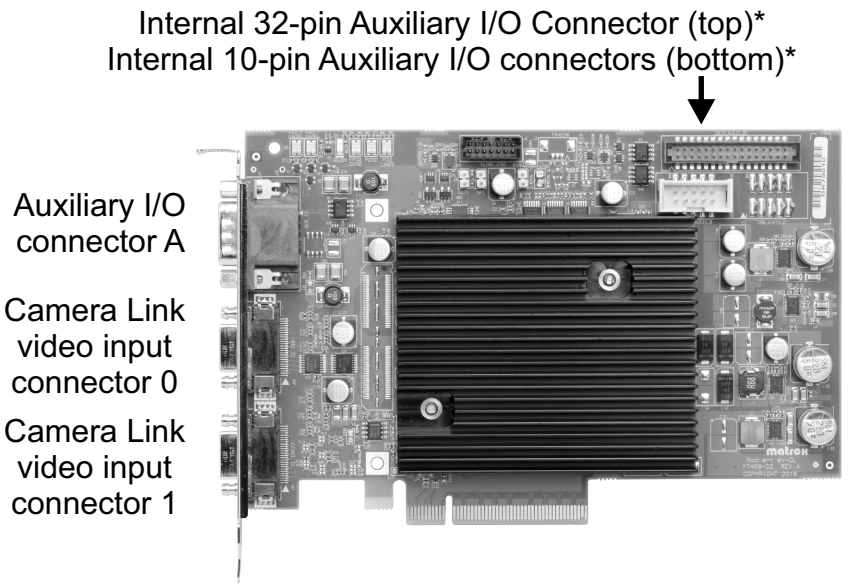
*. The Matrox Rapixo CL Pro opto-couplers are manufactured by Agilent or Avago Technologies (P/N HCPL-0631).

Dimensions and environmental specifications

- Dimensions of Matrox Rapixo CL Pro board SF/DB: 16.76 L x 11.12 H x 1.871 W cm (6.6" x 4.376" x 0.737") from bottom edge of goldfinger to top edge of board. These values respect the dimensions of a PCIe half-length board.
- Dimensions of Matrox Rapixo CL Pro DF/QB: 16.76 L x 11.12 H x 3.903 W cm (6.6" x 4.376" x 1.537") from bottom edge of goldfinger to top edge of board.
- Ventilation: 150 LFM over board(s) (through the heat sink) in a single board configuration. More ventilation may be required in multiple board configurations.
- Minimum/maximum ambient operating temperature: 0°C to 55°C (32°F to 131°F).
- Minimum/maximum storage temperature: -40°C to 75°C (-40°F to 167°F).
- Operating relative humidity: up to 95% relative humidity (non-condensing).
- Storage humidity: up to 95% relative humidity (non-condensing).

Connectors on Matrox Rapixo CL Pro boards

On the Matrox Rapixo CL Pro boards, there are several interface connectors. On the bracket of Matrox Rapixo CL Pro DB and SF, there are two Camera Link video input connectors and an auxiliary I/O connector. On the double bracket of Matrox Rapixo CL Pro QB and DF, there are two pairs of Camera Link video input connectors and two auxiliary I/O connectors. In addition, close to the top edge of the main board, there is an internal auxiliary I/O connector.

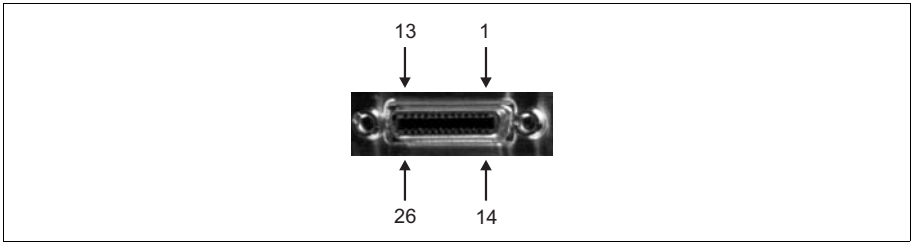


*Use the 32-pin auxiliary I/O connector to connect to the HD-15 cable adapter bracket; Use the 10-pin auxiliary I/O connectors to connect to the DB-9 cable adapter bracket.

On the Matrox Rapixo CL Pro cable adapter bracket, there are two HD-15 auxiliary I/O connectors; these allow you to access the signals of the internal 32-pin auxiliary I/O connector from outside the computer enclosure.

Camera Link video input connectors

The Camera Link video input connectors are 26-pin high-density female mini Camera Link connectors. They are used to receive video input, timing, and synchronization signals and transmit/receive communication signals between the video source and the frame grabber.



The number of Camera Link video input connectors and their pinout depends on the version of Matrox Rapixo CL Pro and the configuration. The pinout of these connectors follows the Camera Link standard.

Matrox Rapixo CL Pro DB and QB

On Matrox Rapixo CL Pro DB, there are two Camera Link connectors; whereas on Matrox Rapixo CL Pro QB, there are four Camera Link connectors. Each Camera Link connector on Matrox Rapixo CL Pro DB and QB supports one video source in Base configuration, and has the same pinout; this pinout is listed in the following table.

Pin	Hardware signal name	MIL constant for auxiliary signal	Description
1	Inner shield		Ground (inner shield), or +12V to camera in PoCL mode.
3+,16-	CC3	M_CC_IO3	Camera control output 3 for acquisition path n, which supports: timer output (M_TIMER1/M_TIMER2 on M_DEVn), user output (M_USER_BIT_CC_IO0/M_USER_BIT_CC_IO1 on M_DEVn), VSYNC, HSYNC, clock output, or rerouting of specific auxiliary input signals*.
5+,18-	CC1	M_CC_IO1	Camera control output 1 for acquisition path n, which supports: timer output (M_TIMER1/M_TIMER2 on M_DEVn), user output (M_USER_BIT_CC_IO0/M_USER_BIT_CC_IO1 on M_DEVn), VSYNC, HSYNC, clock output, or rerouting of specific auxiliary input signals†.
6+,19-	SerTFG		Serial port to frame grabber (UART).
8+,21-	X3		Video input data X3.
9+,22-	Xclk		Clock input X.
10+,23-	X2		Video input data X2.
11+,24-	X1		Video input data X1.
12+,25-	X0		Video input data X0.
13	Inner shield		Ground.
14	Inner shield		Ground.
15+,2-	CC4	M_CC_IO4	Camera control output 4 for acquisition path n, which supports: timer output (M_TIMER1/M_TIMER2 on M_DEVn), user output (M_USER_BIT_CC_IO0/M_USER_BIT_CC_IO1 on M_DEVn), VSYNC, HSYNC, clock output, or rerouting of specific auxiliary input signals†.
17+,4-	CC2	M_CC_IO2	Camera control output 2 for acquisition path n, which supports: timer output (M_TIMER1/M_TIMER2 on M_DEVn), user output (M_USER_BIT_CC_IO0/M_USER_BIT_CC_IO1 on M_DEVn), VSYNC, HSYNC, clock output, or rerouting of specific auxiliary input signals†.
20+,7-	SerTC		Serial port to video source (UART).
26	Inner shield		Ground (inner shield), or +12V to camera in PoCL mode.

*. See the table in the *Auxiliary signals* section of *Chapter 4: Matrox Rapixo CL Pro hardware reference* for more information on which auxiliary input signals (or auxiliary I/O signals set to input) can be rerouted onto the camera control output signals. Also note that for Matrox Rapixo CL Pro DB and QB, n should be replaced by the number of the Camera Link connector to which the video source is connected.

Matrox Rapixo CL Pro SF and DF

On Matrox Rapixo CL Pro SF, there is one pair (0-1) of Camera Link connectors, whereas on Matrox Rapixo CL Pro DF, there are two pairs (0-1 and 2-3) of Camera Link connectors. To each pair of connectors, you can connect one video source in Medium, Full, 72-bit, or 80-bit configuration. Each of the connector pairs uses a single acquisition path. In MIL, the (0-1) connector pair uses acquisition path 0 (M_DEV0), and the (2-3) connector pair uses acquisition path 1 (M_DEV1). The top Camera Link connector of each pair has the pinout described above (except replace n with the number of the acquisition path for the connector pair), while the bottom Camera Link connector of each pair has the following pinout.

Warning

❖ When connecting a video source in Medium, Full, 72-bit, or 80-bit configuration, ensure that you are connecting its cables to the appropriate connector. Also ensure that the orientation of the connector is correct and do not force the connector in. Accidentally connecting the cables to the wrong connector can damage the board or your video source. Pins 2-5 and pins 15-18 are output pins on the top connector (0 and 2), while they are input pins on the bottom connector (1 and 3).

Pin	Hardware signal name	Description
1	GND or PWR_OUT	Ground (inner shield), or +12V to camera in PoCL mode.
2+, 15-	Z3	Video input data Z3.*
3+, 16-	Zclk	Clock input Z.*
4+, 17-	Z2	Video input data Z2.*
5+, 18-	Z1	Video input data Z1.*
6+, 19-	Z0	Video input data Z0.*
7	terminated	Unused.*
8+, 21-	Y3	Video input data Y3.
9+, 22-	Yclk	Clock input Y.
10+, 23-	Y2	Video input data Y2.
11+, 24-	Y1	Video input data Y1.
12+, 25-	Y0	Video input data Y0.
13	Inner shield	Ground.
14	Inner shield	Ground.
20	100 Ω	Unused.*
26	GND or PWR_OUT	Ground (inner shield), or +12V to camera in PoCL mode.

*. When the board is set to the Medium configuration, these pins are reserved.

To interface with the above connectors, use a standard Camera Link cable with a 26-pin high-density male mini Camera Link connector (HDR or SDR) at one end. You can purchase such a cable from your video source manufacturer, Components Express inc., 3M Interconnect Solutions for Factory Automation, Intercon 1, or other third parties. Note that this cable is not available from Matrox.

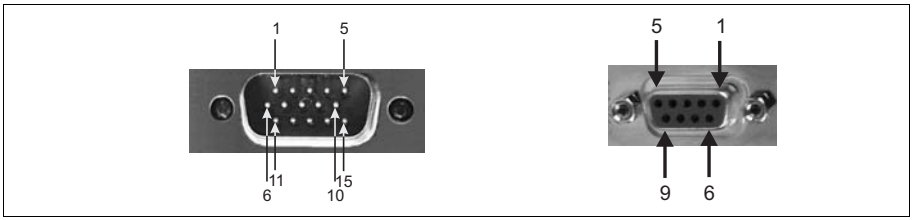
❖ If using both Camera Link connectors to connect to the same video source (Medium configuration or Full configuration), the cables you choose should be of the same type and length. Note, however, if they are not, Matrox Rapixo CL Pro will adapt to any delay caused by reasonable differences in length.

External auxiliary I/O connectors

The external auxiliary I/O connectors on the Matrox Rapixo CL Pro bracket and the cable adapter bracket are high-density D-subminiature 15-pin (HD-15*) male connectors. Alternatively, you can use a cable adapter bracket with a standard D-subminiature 9-pin (DB-9†) female connector for auxiliary I/O connectors B and D. On the cable adapter brackets, the connectors are panel mount connectors. The external auxiliary I/O connectors are used to transmit/receive auxiliary signals.

❖ The auxiliary I/O connectors on Matrox Rapixo CL Pro are not compatible with display devices. Connecting one of the HD-15 connectors on Matrox Rapixo CL Pro to a VGA monitor or any other display device might damage both the device and the Matrox Rapixo CL Pro board.

The auxiliary signals can be path independent or path dependent, depending on the functionality selected. For more information, see the *Camera control and auxiliary signals for Matrox Rapixo CL Pro DB/QB* and *Camera control and auxiliary signals for Matrox Rapixo CL Pro SF/DF* sections in *Chapter 4: Matrox Rapixo CL Pro hardware reference* for supported functionality.



*. Sometimes known as DE-15.
†. More accurately known as DE-9.

Pinouts for auxiliary I/O connectors of Matrox Rapixo CL Pro DB and QB

The pinout for auxiliary I/O connector A is as follows for Matrox Rapixo CL Pro DB and QB.

Pin on DB-15	Hardware signal name	MIL constant for auxiliary signal	Digitizer device number for auxiliary signal	Description
1	TTL_AUX_IO_4	M_AUX_IO8	M_DEV0	TTL auxiliary signal (input/output) for acquisition path 0, which supports: user input, user output (M_USER_BIT2 on M_DEV0), trigger input (trigger controller 0 on acq path 0).
2	TTL_AUX_IO_5	M_AUX_IO9	M_DEV0	TTL auxiliary signal (input/output) for acquisition path 0, which supports: timer output (M_TIMER1 on M_DEV0), trigger input (trigger controller 1 on acq path 0), user input, or user output (M_USER_BIT3 on M_DEV0).
3	TTL_AUX_IO_6	M_AUX_IO2	M_DEV0/ M_DEV1	TTL auxiliary signal (input/output), shared between acquisition paths 0 and 1 for trigger input (trigger control 2 on acq path 0; 2 on acq path 1*), user input, user output (M_USER_BIT4 on M_DEV0/M_DEV1), and dedicated to acquisition path 0 for timer output (M_TIMER2 on M_DEV0).
4+,5-	LVDS_AUX_IN2	M_AUX_IO10	M_DEV0	LVDS auxiliary signal (input) for acquisition path 0, which supports: trigger input (trigger controller 0 on acq path 0), user input, or quadrature input bit 0.
6+,8-	LVDS_AUX_IN3	M_AUX_IO11	M_DEV0	LVDS auxiliary signal (input) for acquisition path 0, which supports: user input, trigger input (trigger controller 1 on acq path 0), timer-clock input, or quadrature input bit 1.
7	GND	N/A	N/A	Ground.
10	GND	N/A	N/A	Ground.
12+,11-	OPTO_AUX_IN1	M_AUX_IO7	M_DEV0	Opto-isolated auxiliary signal (input) for acquisition path 0, which supports: user input or trigger input (trigger controller 1 on acq path 0).
13+,14-	LVDS_AUX_OUT7	M_AUX_IO12	M_DEV0	LVDS auxiliary signal (output) for acquisition path 0, which supports: timer output (M_TIMER1/M_TIMER2 on M_DEV0) or user output (M_USER_BIT0 on M_DEV0).
15+,9-	OPTO_AUX_IN0	M_AUX_IO6	M_DEV0	Opto-isolated auxiliary signal (input) for acquisition path 0, which supports: user input or trigger input (trigger controller 0 on acq path 0).

*. Trigger controller 2 on acq path 1 is only supported on Matrox Rapixo CL Pro DB (for hardware signal TTL_AUX_IO_6).

The pinout for auxiliary I/O connector B is as follows for Matrox Rapixo CL Pro QB.

Pin on DB-15	Hardware signal name	MIL constant for auxiliary signal	Digitizer device number for auxiliary signal	Description
1	TTL_AUX_IO_20	M_AUX_IO8	M_DEV2	TTL auxiliary signal (input/output) for acquisition path 2, which supports: user input, user output (M_USER_BIT2 on M_DEV2), or trigger input (trigger controller 0 on acq path 2).
2	TTL_AUX_IO_21	M_AUX_IO9	M_DEV2	TTL auxiliary signal (input/output) for acquisition path 2, which supports: timer output (M_TIMER1 on M_DEV2), trigger input (trigger controller 1 on acq path 2), user input, or user output (M_USER_BIT3 on M_DEV2).
3	TTL_AUX_IO_22	M_AUX_IO2	M_DEV2/ M_DEV3	TTL auxiliary signal (input/output), shared between acquisition paths 2 and 3 for trigger input (trigger controller 2 on acq path 2; 2 on acq path 3), user input, user output (M_USER_BIT4 on M_DEV2/M_DEV3), and dedicated to acquisition path 2 for timer output (M_TIMER2 on M_DEV2).
4+,5-	LVDS_AUX_IN18	M_AUX_IO10	M_DEV2	LVDS auxiliary signal (input) for acquisition path 2, which supports: trigger input (trigger controller 0 on acq path 2), user input, or quadrature input bit 0.
6+,8-	LVDS_AUX_IN19	M_AUX_IO11	M_DEV2	LVDS auxiliary signal (input) for acquisition path 2, which supports: user input, trigger input (trigger controller 1 on acq path 2), timer-clock input, or quadrature input bit 1.
7	GND	N/A	N/A	Ground.
10	GND	N/A	N/A	Ground.
12+,11-	OPTO_AUX_IN17	M_AUX_IO7	M_DEV2	Opto-isolated auxiliary signal (input) for acquisition path 2, which supports: user input or trigger input (trigger controller 1 on acq path 2).
13+,14-	LVDS_AUX_OUT23	M_AUX_IO12	M_DEV2	LVDS auxiliary signal (output) for acquisition path 2, which supports: timer output (M_TIMER1/M_TIMER2 on M_DEV2) or user output (M_USER_BIT0 on M_DEV2).
15+,9-	OPTO_AUX_IN16	M_AUX_IO6	M_DEV2	Opto-isolated auxiliary signal (input) for acquisition path 2, which supports: user input or trigger input (trigger controller 0 on acq path 2).

The pinout for auxiliary I/O connector C is as follows for Matrox Rapixo CL Pro DB and QB. It can be accessed through either a DB-15 or DB-9 connector using one of the two adapter brackets.

Pin on DB-15	Pin on DB-9	Hardware signal name	MIL constant for auxiliary signal	Digitizer device number for auxiliary signal	Description
1	1	TTL_AUX_IO_12	M_AUX_IO8	M_DEV1	TTL auxiliary signal (input/output) for acquisition path 1, which supports: user input, user output (M_USER_BIT2 on M_DEV1), or trigger input (trigger controller 0 on acq path 1).
2	-	TTL_AUX_IO_13	M_AUX_IO9	M_DEV1	TTL auxiliary signal (input/output) for acquisition path 1, which supports: timer output (M_TIMER1 on M_DEV1), trigger input (trigger controller 1 on acq path 1), user input, or user output (M_USER_BIT3 on M_DEV1).
3	-	TTL_AUX_IO_14	M_AUX_IO3	M_DEV0/ M_DEV1	TTL auxiliary signal (input/output), shared between acquisition paths 0 and 1 for trigger input (trigger controller 3 on acq path 0; 3 on acq path 1), user input, user output (M_USER_BIT5 on M_DEV0/M_DEV1), and dedicated to acquisition path 1 for timer output (M_TIMER2 on M_DEV1).
4+,5-	8+,3-	LVDS_AUX_IN10	M_AUX_IO4	M_DEV0/ M_DEV1	LVDS auxiliary signal (input), shared between acquisition paths 0 and 1 for trigger input (trigger controller 2 on acq path 0; 2 or 0 on acq path 1) or user input, and dedicated to acquisition path 1 for quadrature input bit 0.
6+,8-	-	LVDS_AUX_IN11	M_AUX_IO5	M_DEV0/ M_DEV1	LVDS auxiliary signal (input), shared between acquisition paths 0 and 1 for trigger input (trigger controller 1 or 3 on acq path 1; 3 on acq path 0) or user input, and dedicated to acquisition path 1 for timer-clock input or quadrature input bit 1.
7	6	GND	N/A	N/A	Ground.
10	-	GND	N/A	N/A	Ground.
12+,11-	4+,5-	OPTO_AUX_IN9	M_AUX_IO1	M_DEV0/ M_DEV1	Opto-isolated auxiliary signal (input), shared between acquisition paths 0 and 1 for trigger input (trigger controller 1 or 3 on acq path 1; 3 on acq path 0) or user input.
13+,14-	-	LVDS_AUX_OUT15	M_AUX_IO12	M_DEV1	LVDS auxiliary signal (output) for acquisition path 1, which supports: timer output (M_TIMER1/M_TIMER2 on M_DEV1) or user output (M_USER_BIT0 on M_DEV1).
15+,9-	7+,2-	OPTO_AUX_IN8	M_AUX_IO0	M_DEV0/ M_DEV1	Opto-isolated auxiliary signal (input), shared between acquisition paths 0 and 1 for trigger input (trigger controller 0 or 2 on acq path 1; 2 on acq path 0) or user input.
-	9	NC			Not connected.

The pinout for auxiliary I/O connector D is as follows for Matrox Rapixo CL Pro QB. It can be accessed through either a DB-15 or DB-9 connector using one of the two adapter brackets.

Pin on DB-15	Pin on DB-9	Hardware signal name	MIL constant for auxiliary signal	Digitizer device number for auxiliary signal	Description
1	1	TTL_AUX_IO_28	M_AUX_IO8	M_DEV3	TTL auxiliary signal (input/output) for acquisition path 3, which supports: user input, user output (M_USER_BIT2 on M_DEV3), or trigger input (trigger controller 0 on acq path 3).
2	-	TTL_AUX_IO_29	M_AUX_IO9	M_DEV3	TTL auxiliary signal (input/output) for acquisition path 3, which supports: timer output (M_TIMER1 on M_DEV3), trigger input (trigger controller 1 on acq path 3), user input, or user output (M_USER_BIT3 on M_DEV3).
3	-	TTL_AUX_IO_30	M_AUX_IO3	M_DEV2/ M_DEV3	TTL auxiliary signal (input/output), shared between acquisition paths 2 and 3 for trigger input (trigger controller 3 on acq path 2; 3 on acq path 3), user input, user output (M_USER_BIT5 on M_DEV2/M_DEV3), and dedicated to acquisition path 3 for timer output (M_TIMER2 on M_DEV3).
4+,5-	8+,3-	LVDS_AUX_IN26	M_AUX_IO4	M_DEV2/ M_DEV3	LVDS auxiliary signal (input), shared between acquisition paths 2 and 3 for trigger input (trigger controller 0 or 2 on acq path 3; 2 on acq path 2) or user input, and dedicated to acquisition path 3 for quadrature input bit 0.
6+,8-	-	LVDS_AUX_IN27	M_AUX_IO5	M_DEV2/ M_DEV3	LVDS auxiliary signal (input), shared between acquisition paths 2 and 3 for trigger input (trigger controller 1 or 3 on acq path 3; 3 on acq path 2) or user input, and dedicated to acquisition path 3 for timer-clock input or quadrature input bit 1.
7	6	GND	N/A	N/A	Ground.
10	-	GND	N/A	N/A	Ground.
12+,11-	4+,5-	OPTO_AUX_IN25	M_AUX_IO1	M_DEV2/ M_DEV3	Opto-isolated auxiliary signal (input), shared between acquisition paths 2 and 3 for trigger input (trigger controller 1 or 3 on acq path 3; 3 on acq path 2) or user input.
13+,14-	-	LVDS_AUX_OUT31	M_AUX_IO12	M_DEV3	LVDS auxiliary signal (output) for acquisition path 3, which supports: timer output (M_TIMER1/M_TIMER2 on M_DEV3) or user output (M_USER_BIT0 on M_DEV3).
15+,9-	7+,2-	OPTO_AUX_IN24	M_AUX_IO0	M_DEV2/ M_DEV3	Opto-isolated auxiliary signal (input), shared between acquisition paths 2 and 3 for trigger input (trigger controller 0 or 2 on acq path 3; 2 on acq path 2) or user input.
	9	NC			Not connected.

Pinouts for auxiliary I/O connectors of Matrox Rapixo CL Pro SF and DF

The pinout for auxiliary I/O connector A is as follows for Matrox Rapixo CL Pro SF and DF.

Pin on DB-15	Hardware signal name	MIL constant for auxiliary signal	Digitizer device number for auxiliary signal	Description
1	TTL_AUX_IO_4	M_AUX_IO8	M_DEV0	TTL auxiliary signal (input/output) for acquisition path 0, which supports: user input, user output (M_USER_BIT2 on M_DEV0), trigger input (trigger controller 0 on acq path 0).
2	TTL_AUX_IO_5	M_AUX_IO9	M_DEV0	TTL auxiliary signal (input/output) for acquisition path 0, which supports: timer output (M_TIMER1 on M_DEV0), trigger input (trigger controller 1 on acq path 0), user input, or user output (M_USER_BIT3 on M_DEV0).
3	TTL_AUX_IO_6	M_AUX_IO2	M_DEV0	TTL auxiliary signal (input/output), for acquisition paths 0, which supports: trigger input (trigger control 2 on acq path 0), user input, user output (M_USER_BIT4 on M_DEV0), or timer output (M_TIMER2 on M_DEV0).
4+,5-	LVDS_AUX_IN2	M_AUX_IO10	M_DEV0	LVDS auxiliary signal (input) for acquisition path 0, which supports: trigger input (trigger controller 0 on acq path 0), user input, or quadrature input bit 0.
6+,8-	LVDS_AUX_IN3	M_AUX_IO11	M_DEV0	LVDS auxiliary signal (input) for acquisition path 0, which supports: user input, trigger input (trigger controller 1 on acq path 0), timer-clock input, or quadrature input bit 1.
7	GND	N/A	N/A	Ground.
10	GND	N/A	N/A	Ground.
12+,11-	OPTO_AUX_IN1	M_AUX_IO7	M_DEV0	Opto-isolated auxiliary signal (input) for acquisition path 0, which supports: user input or trigger input (trigger controller 1 on acq path 0).
13+,14-	LVDS_AUX_OUT7	M_AUX_IO12	M_DEV0	LVDS auxiliary signal (output) for acquisition path 0, which supports: timer output (M_TIMER1/M_TIMER2 on M_DEV0) or user output (M_USER_BIT0 on M_DEV0).
15+,9-	OPTO_AUX_IN0	M_AUX_IO6	M_DEV0	Opto-isolated auxiliary signal (input) for acquisition path 0, which supports: user input or trigger input (trigger controller 0 on acq path 0).

The pinout for auxiliary I/O connector B is as follows for Matrox Rapixo CL Pro DF.

Pin on DB-15	Hardware signal name	MIL constant for auxiliary signal	Digitizer device number for auxiliary signal	Description
1	TTL_AUX_IO_20	M_AUX_IO8	M_DEV1	TTL auxiliary signal (input/output) for acquisition path 1, which supports: user input, user output (M_USER_BIT2 on M_DEV1), or trigger input (trigger controller 0 on acq path 1).
2	TTL_AUX_IO_21	M_AUX_IO9	M_DEV1	TTL auxiliary signal (input/output) for acquisition path 1, which supports: timer output (M_TIMER1 on M_DEV1), trigger input (trigger controller 1 on acq path 1), user input, or user output (M_USER_BIT3 on M_DEV1).
3	TTL_AUX_IO_22	M_AUX_IO2	M_DEV1	TTL auxiliary signal (input/output), for acquisition paths 1 which supports trigger input (trigger controller 2 on acq path 1), user input, user output (M_USER_BIT4 on M_DEV1), and timer output (M_TIMER2 on M_DEV1).
4+,5-	LVDS_AUX_IN18	M_AUX_IO10	M_DEV1	LVDS auxiliary signal (input) for acquisition path 1, which supports: trigger input (trigger controller 0 on acq path 1), user input, or quadrature input bit 0.
6+,8-	LVDS_AUX_IN19	M_AUX_IO11	M_DEV1	LVDS auxiliary signal (input) for acquisition path 1, which supports: user input, trigger input (trigger controller 1 on acq path 1), timer-clock input, or quadrature input bit 1.
7	GND	N/A	N/A	Ground.
10	GND	N/A	N/A	Ground.
12+,11-	OPTO_AUX_IN17	M_AUX_IO7	M_DEV1	Opto-isolated auxiliary signal (input) for acquisition path 1, which supports: user input or trigger input (trigger controller 1 on acq path 1).
13+,14-	LVDS_AUX_OUT23	M_AUX_IO12	M_DEV1	LVDS auxiliary signal (output) for acquisition path 1, which supports: timer output (M_TIMER1/M_TIMER2 on M_DEV1) or user output (M_USER_BIT0 on M_DEV1).
15+,9-	OPTO_AUX_IN16	M_AUX_IO6	M_DEV1	Opto-isolated auxiliary signal (input) for acquisition path 1, which supports: user input or trigger input (trigger controller 0 on acq path 1).

The pinout for auxiliary I/O connector C is as follows for Matrox Rapixo CL Pro SF and DF. It can be accessed through either a DB-15 or DB-9 connector using one of the two adapter brackets.

Pin on DB-15	Pin on DB-9	Hardware signal name	MIL constant for auxiliary signal	Digitizer device number for auxiliary signal	Description
1	1	RESERVED			Reserved. Do not connect.
2	-	RESERVED			Reserved. Do not connect.
3	-	TTL_AUX_IO_14	M_AUX_IO3	M_DEV0	TTL auxiliary signal (input/output), for acquisition path 0, which supports: trigger input (trigger controller 3 on acq path 0), user input, or user output (M_USER_BIT5 on M_DEV0).
4+,5-	8+,3-	LVDS_AUX_IN10	M_AUX_IO4	M_DEV0	LVDS auxiliary signal (input), for acquisition path 0, which supports: trigger input (trigger controller 2 on acq path 0) or user input.
6+,8-	-	LVDS_AUX_IN11	M_AUX_IO5	M_DEV0	LVDS auxiliary signal (input), for acquisition path 0, which supports: trigger input (trigger controller 3 on acq path 0) or user input.
7	6	GND	N/A	N/A	Ground.
10	-	GND	N/A	N/A	Ground.
12+,11-	4+,5-	OPTO_AUX_IN9	M_AUX_IO1	M_DEV0	Opto-isolated auxiliary signal (input), for acquisition path 0,which supports: trigger input (trigger controller 3 on acq path 0) or user input.
13	-	RESERVED			Reserved. Do not connect.
14	7+,2-	RESERVED			Reserved. Do not connect.
15+,9-	-	OPTO_AUX_IN8	M_AUX_IO0	M_DEV0	Opto-isolated auxiliary signal (input), for acquisition path 0, which supports: trigger input (trigger controller 2 on acq path 0) or user input.
-	9	NC			Not connected.

The pinout for auxiliary I/O connector D is as follows for Matrox Rapixo CL Pro DF. It can be accessed through either a DB-15 or DB-9 connector using one of the two adapter brackets.

Pin on DB-15	Pin on DB-9	Hardware signal name	MIL constant for auxiliary signal	Digitizer device number for auxiliary signal	Description
1	1	RESERVED			Reserved. Do not connect.
2	-	RESERVED			Reserved. Do not connect.
3	-	TTL_AUX_IO_30	M_AUX_IO3	M_DEV1	TTL auxiliary signal (input/output), for acquisition path 1, which supports: trigger input (trigger controller 3 on acq path 1), user input, or user output (M_USER_BIT5 on M_DEV1).
4+,5-	8+,3-	LVDS_AUX_IN26	M_AUX_IO4	M_DEV1	LVDS auxiliary signal (input), for acquisition path 1, which supports: trigger input (trigger controller 2 on acq path 1) or user input.
6+,8-	-	LVDS_AUX_IN27	M_AUX_IO5	M_DEV1	LVDS auxiliary signal (input), for acquisition path 1, which supports: trigger input (trigger controller 3 on acq path 1) or user input.
7	6	GND	N/A	N/A	Ground.
10	-	GND	N/A	N/A	Ground.
12+,11-	4+,5-	OPTO_AUX_IN25	M_AUX_IO1	M_DEV1	Opto-isolated auxiliary signal (input), for acquisition path 1, which supports: trigger input (trigger controller 3 on acq path 1) or user input.
13	-	RESERVED			Reserved. Do not connect.
14	7+,2-	RESERVED			Reserved. Do not connect.
15+,9-	-	OPTO_AUX_IN24	M_AUX_IO0	M_DEV1	Opto-isolated auxiliary signal (input), for acquisition path 1, which supports: trigger input (trigger controller 2 on acq path 1) or user input.
-	9	NC			Not connected.

To build your own cable, you can purchase the following parts:

	Mating information
Manufacturer:	NorComp, Inc.
Connector:	180-015-203L001
Backshell:	970-015-010-011

These parts can be purchased from third parties such as Digi-Key Corporation (www.digikey.com).

LEDs on Matrox Rapixo CL Pro

Matrox Rapixo CL Pro has a series of LEDs to display the status of the PoCL connections, the on-board power, the board configuration, the PCIe (Host) slot, and the firmware configuration.

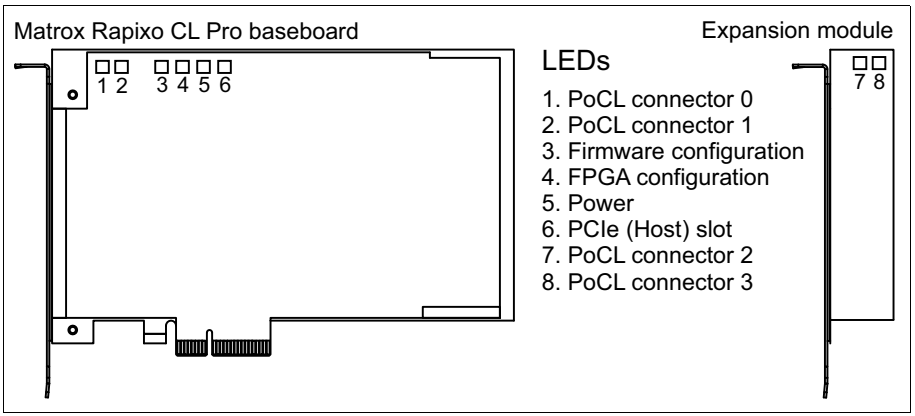
PoCL LEDs

The Matrox Rapixo CL Pro main board has two PoCL LEDs. In addition, Matrox Rapixo CL Pro DF and QB have 2 PoCL LEDs on the Matrox Rapixo CL Pro expansion module. Each LED indicates the status of the PoCL device attached to that connector.

LED color and state	Description
Off	Matrox Rapixo CL Pro is not providing power to the camera.
Red, solid	Matrox Rapixo CL Pro is sensing for a PoCL-compliant device.
Green, solid	Matrox Rapixo CL Pro is providing power to the camera.

Board status LEDs

Matrox Rapixo CL Pro main board has four additional status LEDs to indicate the status of each of the following: the firmware configuration, the FPGA configuration, the power, and PCIe (Host) slot.



The table below outlines the possible colors for each LED, and their definitions.

LED type	LED color and state	Description
3. Firmware configuration	Off	The board is configured with the recommended user's firmware.
	Red	The board is configured with the golden firmware (a fall-back configuration).
4. FPGA configuration	Green	The FPGA is configured.
	Red	The FPGA is not configured.
5. Power	Off/Red	One or more of the on-board voltage regulators did not start. If your computer is on and this LED state occurs, there is an issue with the voltage regulators on your Matrox Rapixo CL Pro. Contact Matrox technical support.
	Green	All of the on-board voltage regulators are working properly.
6. PCIe slot	Off	The type of slot cannot be established. The PCIe link is down.
	Red, solid	Slot is PCIe Gen 1, x8
	Red, blinking	Slot is PCIe Gen 1, x1, x2, or x4
	Orange, solid	Slot is PCIe Gen 2, x8
	Orange, blinking	Slot is PCIe Gen 2, x1, x2, or x4
	Green, solid	Slot is PCIe Gen 3, x8
	Green, blinking	Slot is PCIe Gen 3, x1, x2, or x4

Appendix C: Acknowledgments

This appendix lists the copyright information regarding third-party material used to implement components on the Matrox Rapixo CL Pro board.

UART copyright information

The following is the copyright notice for the UART design used on the Matrox Rapixo CL Pro boards.

Appendix D: Listing of Matrox Rapixo CL Pro boards

This appendix lists the key feature changes to the Matrox Rapixo CL Pro boards.

Key feature changes

Part number	Version	Description
RAP 4G CL DB P325	000	First shipping version of Matrox Rapixo CL Pro DB.
RAP 4G CL SF P325	000	First shipping version of Matrox Rapixo CL Pro SF.
RAP 4G CL QB P325	000	First shipping version of Matrox Rapixo CL Pro QB.
RAP 4G CL DF P325	000	First shipping version of Matrox Rapixo CL Pro DF.

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Regulatory Compliance

FCC Compliance Statement

Warning

Changes or modifications to these units not expressly approved by the party responsible for the compliance could void the user's authority to operate this equipment.

The use of shielded cables for connections of these devices to other peripherals is required to meet the regulatory requirements.

Note

These devices comply with Part 15 of FCC Rules. Operation is subject to the following two conditions:

1. These devices may not cause harmful interference, and
2. These devices must accept any interference received, including interference that may cause undesired operation.

This equipment has been tested and found to comply with the limits for Class A digital devices, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of these devices in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his/her own expense.

Innovation, Science and Economic Development Canada Compliance Statement

These digital apparatuses do not exceed the Class A limits for radio noise emission from digital apparatuses set out in the Radio Interference Regulations of Innovation, Science and Economic Development Canada (ISED).

Ces appareils numériques n'émettent pas de bruits radioélectriques dépassant les limites applicables aux appareils numériques de Classe A prescrites dans le Règlement sur le brouillage radioélectrique édicté par Innovation, Sciences et Développement Économique Canada (ISDE).

EU Notice (European Union)

WARNING: These are class A products. In a domestic environment these products may cause radio interference in which case the user may be required to take adequate measures.

AVERTISSEMENT: Ces appareils sont des produits informatiques de Classe A. Lorsque ces appareils sont utilisés dans un environnement résidentiel, ces produits peuvent entraîner des interférences radioélectriques. Dans ce cas, l'usager peut être prié de prendre des mesures correctives appropriées.

This device complies with Directive 2014/30/EU for Class A digital devices. They have been tested and found to comply with EN55032/CISPR32 and EN55024/CISPR24 when installed in a typical class A compliant host system. It is assumed that these devices will also achieve compliance in any Class A compliant system.

Ces unités sont conformes à la Directive 2014/30/EU pour les unités numériques de Classe A. Les tests effectués ont prouvé qu'elles sont conformes aux normes EN55032/CISPR32 et EN55024/CISPR24 lorsqu'elles sont installées dans un système hôte typique de la Classe A. On suppose qu'ils présenteront la même compatibilité dans tout système compatible de la Classe A.

Directive on Waste Electrical and Electronic Equipment (WEEE)

Europe

(English) European user's information – Directive on Waste Electrical and Electronic Equipment (WEEE)

Please refer to the Matrox Web site (**www.matrox.com/environment/weee**) for recycling information.

(Français) Informations aux utilisateurs Européens – Règlementation des déchets d'équipements électriques et électroniques (DEEE)

Se référer au site Web de Matrox (**www.matrox.com/environment/weee**) pour l'information concernant le recyclage.

(Deutsch) Information für europäische Anwender – Europäische Regelungen zu Elektro- und Elektronikaltgeräten (WEEE)

Bitte wenden Sie sich an dem Matrox-Website (**www.matrox.com/environment/weee**) für Recycling Informationen.

(Italiano) Informazioni per gli utenti europei – Direttiva sui rifiuti di apparecchiature elettriche ed elettroniche (RAEE)

Si prega di riferirsi al sito Web Matrox (**www.matrox.com/environment/weee**) per le informazioni di riciclaggio.

Limited warranty

Refer to the warranty statement that came with your product.