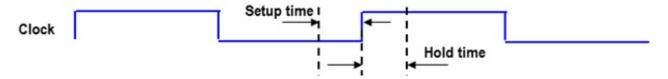
SETUP AND HOLD TIME DEFINITION

Setup and hold checks are the most common types of timing checks used in timing verification. Synchronous inputs (e.g. D) have Setup, Hold time specification with respect to the clock input. These checks specify that the data input must remain stable for a specified interval before and after the clock input changes

- ★ **Setup Time:** the amount of time the data at the synchronous input (D) must be stable before the active edge of clock
- **Hold Time:** the amount of time the data at the synchronous input (D) must be stable after the active edge of clock.



Both setup and hold time for a flip-flop is specified in the library.

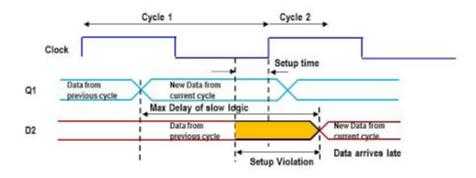
12.1. Setup Time

Setup Time is the amount of time the synchronous input (D) must show up, and be stable before the capturing edge of clock. This is so that the data can be stored successfully in the storage device.

Setup violations can be fixed by either slowing down the clock (increase the period) or by decreasing the delay of the data path logic.

Setup Time

- · Data should be stable before the clock edge
- Setup Time is the amount of time the synchronous input (D) must show up, and be stable before the capturing edge of clock.
- This is so that the data can be stored successfully in the storage device.
- Setup violations can be fixed by either slowing down the clock (increase the period) or by decreasing the delay of the data path logic.



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Clock

Clock

Setup time

Clock

Setup time

Cutent cycle

Max Delay of slow logic

Data from

Cutent cycle

Setup Violation

Setup Violation

Setup Violation

Setup Violation

Transf

setup information .lib:

timing () {

57

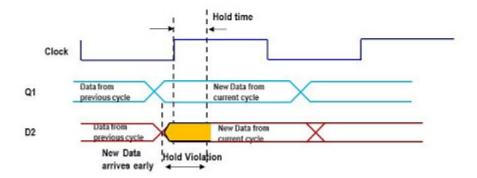
12.2. Hold Time

Hold Time is the amount of time the synchronous input (D) stays long enough after the capturing edge of clock so that the data can be stored successfully in the storage device.

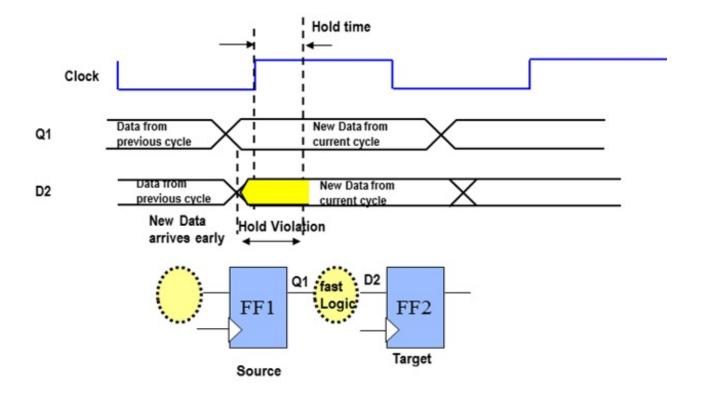
Hold violations can be fixed by increasing the delay of the data path or by decreasing the clock uncertainty (skew) if specified in the design.

Hold Time

- · Data should be stable after the clock edge
- Hold Time is the amount of time the synchronous input (D) stays long enough after the capturing edge of clock so that the data can be stored successfully in the storage device.
- Hold violations can be fixed by increasing the delay of the data path or by decreasing the clock uncertainty(skew) if specified in the design.



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Hold Information n .lib:

```
timing () {
```