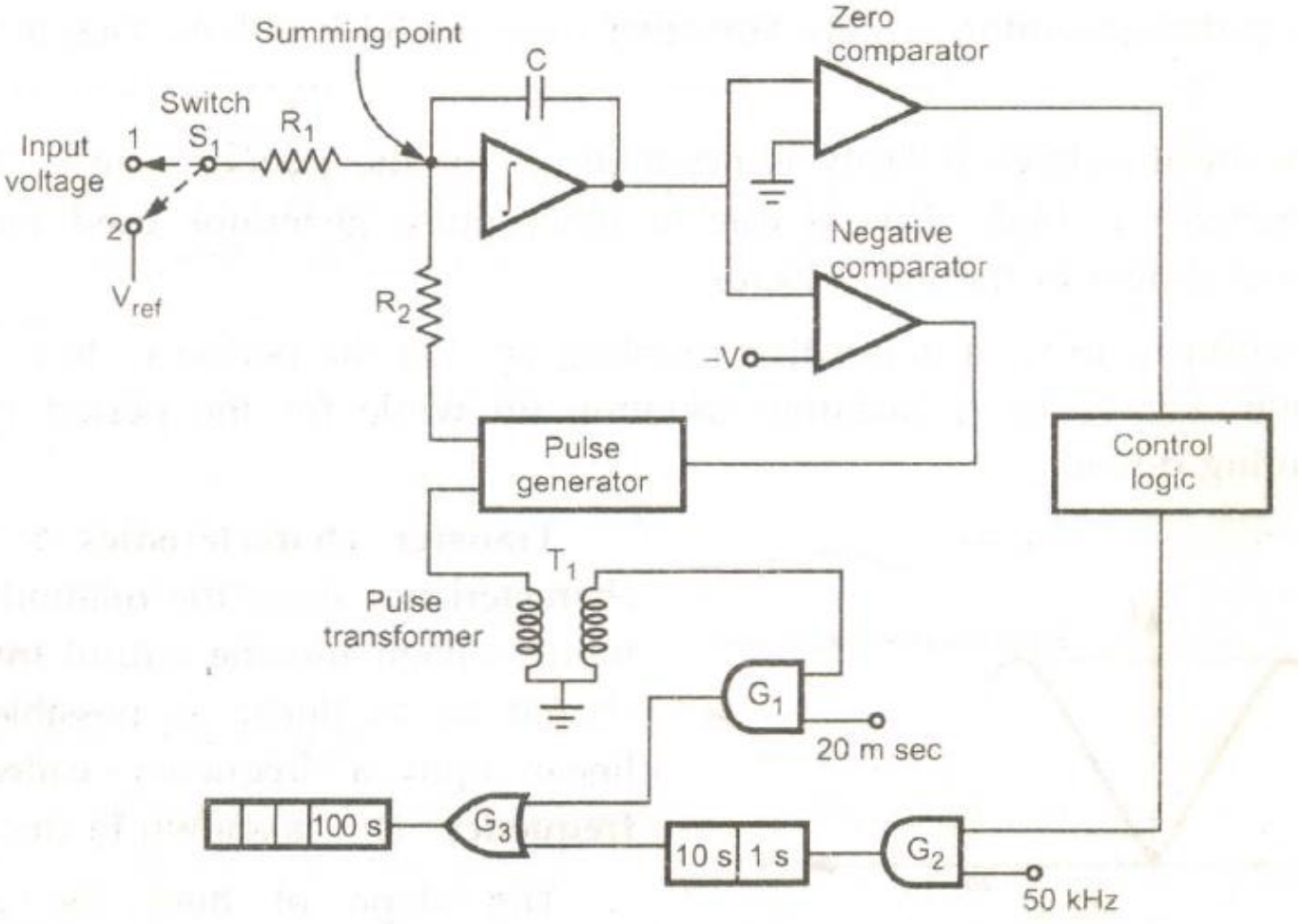
INTERPOLATING INTEGRATING AND SUCCESSIVE APPROXIMATION TYPE DVM

The block diagram of interpolating integrating DVM is shown in the Fig.

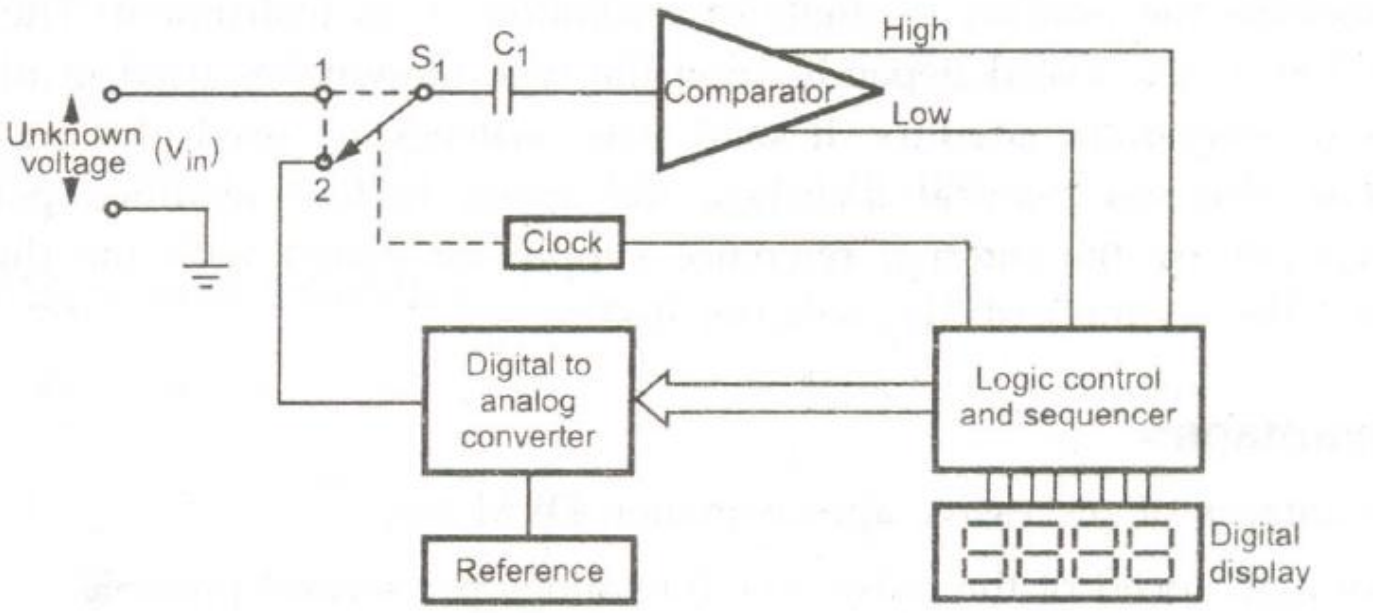
This is a modified version of V*If* integrating DVM. A zero comparator is the additional circuitry in the DVM. The zero comparator ensures that the charge on the capacitor is zero. During first 20 msec, the operation is exactly similar to the normal V*If* integrating DVM. However during this time the pulses are directed to the 100 s decade. Here each pulse is equivalent to the 100 counts.

After 20 msec, the switch SI is moved from position 1 to 2 and Vrer of opposite polarity is offered. Some charge is still present on the capacitor. The opposite polarity Vrer helps to remove the remaining charge at a constant rate. When the charge reaches zero, the zero comparator provides a pulse to the control logic. When the switch is moved from position 1 to 2, at the same time gate G2 is also opened. Hence the pulses from 50 kHz oscillator can reach to Is decade. When the zero comparator provides a pulse, the gate G1 is closed. This completes the reading operation.



Successive approximation type DVM:

In successive approximation type DVM, the comparator compares the output of digital to analog converter with the unknown voltage. Accordingly, the comparator provides logic high or low signals. The digital to analog converter successively generates the set pattern of signals. The procedure continues till the output of the digital to analog converter becomes equal to the unknown voltage.



The capacitor is connected at the input of the comparator. The output of the digital to analog converter is compared with the unknown voltage, by the comparator. The output of the comparator is given to the logic control and sequencer. This unit generates the sequence of code which is applied to digital to analog converter. The position 2 of the switch 51 receives the output from digital to analog converter. The unknown voltage is available at the position 1 of the switch S1. The logic control also drives the clock which is used to alternate the switch S1 between the positions 1 and 2, as per the requirement.

Resolution and sensitivity:

If n is the number of full digits then the resolution of a DVM is given by,

$$R = \frac{1}{10^n}$$

where R = Resolution

Thus for 3 digit display, n = 3

$$\therefore \quad R = \frac{1}{10^3} = 10^{-3} = 0.001 \text{ or } 0.1\%$$

The sensitivity is the smallest change in the input which a digital meter should be able to detect. Hence, it is the full scale value of the lowest range multiplied by the resolution of the meter.

$$S = (fs)_{min} \times R$$

where S = Sensitivity

$(fs)_{min}$ = Full scale value on minimum range.

R = Resolution expressed as decimal.

Source : http://elearningatria.files.wordpress.com/2013/10/ece-iii-electronic-instrumentation-10it35-notes.pdf