Design and Implementation of Optimized Dual Port Register File Bit Cell

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Abstract- The memory bit cell is the most important block of any memory. It defines memory specifications and occupies a major portion of the area in any memory. Power performance & Area (PPA) are industry wide parameters which are used to evaluate a memory configuration. Larger the memory size larger is its power consumption. But designing the memory bit cell effectively minimizes the area consumption of the memory and the chip.

Based on applications memories are designed to be of different types like high density, high performance, and low power. These memory flavours differ in the type of bitcell used for storing the data. In this project our aim is to design and implement Dual port Register-file memory bitcells. We later optimize the register file bit cell design for faster access time and lower chip area. These bit-cells will be characterized and the performance of this two bit-cells is compared against each other. The characterization will be done using HSPICE simulations and the schematics will be created in a schematic editor tool. BSIM4 models will be used for the transistors in the design.

Index Terms- Register file, high density, high performance, dynamic power, static noise margin, Read/Write Simulation.

I. INTRODUCTION

Register file is a key component of many processors or SoC applications. Not only its access time dominates the application speed but also its area and power occupies most part of chip in high performance processor design. In order to achieve sufficient bandwidth, designers increase the port number on bit-cell in conventional register file design [1]. However, such approaches make the bit-cell have larger area, worse noise margin, longer access time and limited operation voltage. To address these issues, many techniques were investigated to reduce the port number [2]. Increasing register file size cannot always improve the performance and in a specific size the performance improvement will be saturated [3].

Analysis and Design of High Performance, Low Power Multiple Ports Register Files [4] by et all proposes about how to analyze and design high performance low power multiple-ports register file circuitry, which is mostly used on µ-P and DSP chip. Here the basics concepts and different types of register file architectures are described. The design tradeoffs among the approaches are then analyzed and compared.

Reducing Register File Size through Instruction Pre-Execution Enhanced by Value Prediction by Tanaka Y ET all [5].TSD is is an architectural scheme, which enhances memory-level parallelism (MLP) by pre-executing instructions. Ideally, the TSD allows MLP under the unlimited number of physical registers to be exploited, and consequently only a small register file is necessary for MLP. In practice, however, the amount of MLP exploitable is limited, because there are cases where pre-execution is not performed or timing of pre-execution is delayed. This is caused by data dependencies among the pre-executed instructions. The authors propose the use of value prediction to solve the problems and reduce the use only 75% of the register file size.

A Low-Power Cell-Based-Design Multi-Port Register File in 65nm CMOS Technology Johannes Uhlig et all [6] proposes the design of a register file with 4 write and 6 read ports for an SDR multiprocessor in 65nm CMOS technology. A cell-based design (CBD) methodology is employed in which the circuit is partitioned into complex sub-cells, optimized on transistor level and layout. Each cell is completely characterized concerning timing and power for seamless integration into a semi-custom design flow. The CBD implementation shows 30% savings of power and 40% of area compared to a conventional semi-custom solution. The average power is 2.7mW from 1.0V supply and 300MHz operating frequency which is superior to previously published designs.

In this paper, we design a dual port register file bit cell and optimize the design by varying the transistor width for faster access time and lower fabrication area. The rest of this paper is organized as follows: Section II describes the architecture of Dual port Register file. Section III shows the simulations and analysis Section IV shows simulation results, and conclusions are given in Section V

There are two basic architecture of register file circuit, namely, single read/write port and multiple read/write ports.

Figure 1 shows the single read/write port architecture, which consists of three parts: the first block is the decoder. Its function is to decode the read/write address. There are two decoders, write decoder and read decoder. The second block is storage cell bank. It has bit line pre-charge circuit, memory cells and sense amplifiers. The third block is the control circuit, which has sleep control, in/out data control and flip-flops. Designing the storage element is the most critical issue in register file. It affects the performances and area of the final design

Single read/write port architecture only can read or write for one cell once. It will become a problem if the system wants to read/write for the multiple data at the same time. To solve this issue we can either add more single port cells or use multiple read/write ports architecture. For area, using multiple ports architecture is more efficient solution.

Figure 2 shows a multiple (2R1W) read/write ports architecture. Similarly, this circuit is composed of three blocks with a little difference. The 2R1W read/write register file must add a read decoder, controller, sense amplifier, and also storage cell need to add two pull down NMOS for additional read port. Therefore it can achieve the goal of multiple read/write, with a little bit of increased area. In the next section we will analyze two different read ports structures of register file.

II. DUAL PORT REGISTER FILE BIT CELL

Figure 3 shows the schematic of Dual port Register file circuit. The 8T register file bit cell consists of two ports viz., Port-A and Port-B. Register file bit cell differs from SRAM bit cell in a way that there are separate dedicated ports for read and write operations. Port-A is always used for read operation and Port-B for write operation.

In Read operation, the address decoder decodes the address line and put the address on the word line A (WLA). When this word line goes high the pass gate turns on and exposes the internal storage node (cored) to the bit line A (BLA) which is initially pre-charged to logic 1 by the bit cell pre-charge circuit.
In write operation, the data is driven by write drivers into the bit line B (BLB). When clock in enabled and write enable is activated the address decoders decode the address and turn on WLB

This pass gate when turned on exposes BLB to cored. The strength of write driver is higher than the pull down device in the bit cell. Hence the data is written onto the internal node

III. SIMULATION AND ANALYSIS

This section contains the Write and Read waveforms, Dynamic power, Leakage power and Static noise margin for faster access design and low fabrication area design.

Table 1: Transistor sizes

Transistors	Transistor Width 1	Transistor width 2
P1	3.3e-07	2.2e-07
P2	3.3e-07	2.2e-07
N1	2.25e-06	1.49e-06
N2	2.25e-06	1.49e-06
Pg1	6.3e-07	4.2e-07
Pg2	6.3e-07	4.2e-07
Pg3	6.3e-07	4.2e-07
Pg4	6.3e-07	4.2e-07

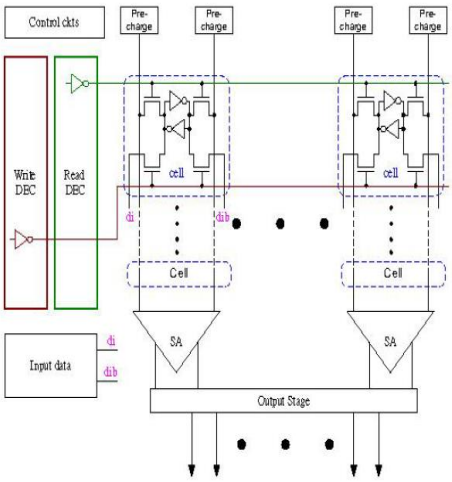

Figure 1: Single Read/Write Port Architecture

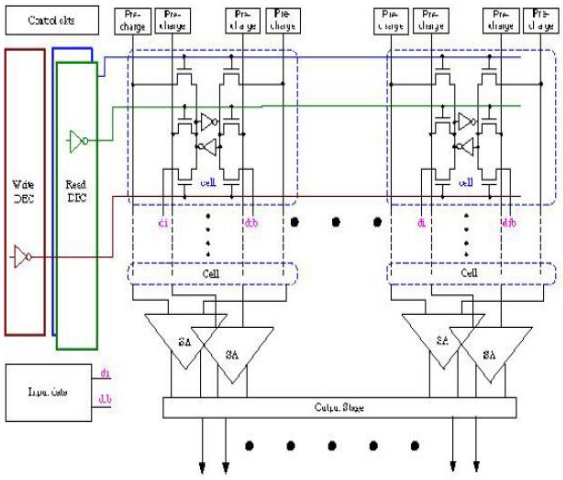

Figure 2: Multiple Read/Write Port Architecture

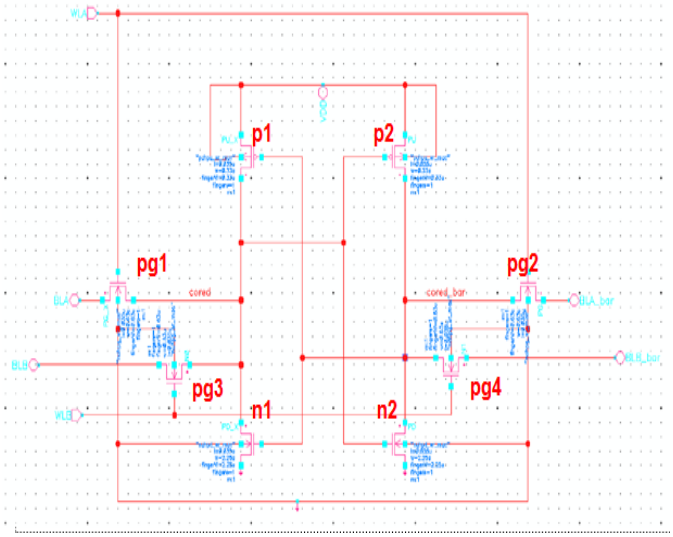

Figure 3: 8T Register File Bit Cell

Table 1 show the transistor sizes which are used to optimize the designed register file for faster access time and for low fabrication area.

IV. RF DESIGN USING TRANSISTOR WIDTH 1

i. Read Simulation

Read time is measured as the delay from word line reaching 50% of its final value to the time it takes the bit line differential to reach its threshold at power supply of 1.8V as shown in Figure 4. Tread= 5.722e-12sec, Iread=3.684e-05A.

ii. Write Simulation

Write time is measured as the time delay from word line WLB rise to the time it takes for the internal nodes to change state as shown in Figure 5. Twrite= 1.870e-10sec.

iii. Dynamic Power

Dynamic read power is the power drawn by the bitcell when the bit cell is subjected to a real-time read operation times the supply voltage. Here we model the bit cell into a read functional mode and then measure the current drawn by it from VDD. Dynamic write power is the powers drawn by the bitcell when the bit cell is subjected to a real-time write operation times the supply voltage. Here we model the bit cell into a write functional mode and then measure the current drawn by it from VDD as shown in Figure 6. Pdynamic_write= 6.6312e-05W, Ppeak_write= 1.713e-03W, Pdynamic_read= 3.51E-05W, Ppeak_read= 3.4524e-03W.

iv. Leakage Power

Leakage read power is the power drawn by the bitcell when subjected to a non-functional mode the bit cell is turned off i.e., bit lines are floating and word lines are at logic '0' times the supply voltage. Leakage write power is the power drawn by the bitcell when subjected to a non-functional mode. The bit cell is turned off i.e., bit lines are floating and word lines are at logic '0' times the supply voltage.
Leak power = 145.9pW

v. Static Noise margin

In this project we designed 8T register file which has separate read and write ports. In each RF cell design writing is done by using eight transistors and during writing data we disabling the Read port so Static Noise Margin (SNM) is not affecting during hold and Read mode. During writing we use the same writing configuration in the design so the write margin (least bitline voltage required to change the state of RF cell) is not affected by the Read port. By using the proposed design the worst case stability condition encountered in 8T RF cell is avoided and high Read SNM is retained. We modelled noise as a voltage source at the internal node of the cell and increased it gradually in the steps of 100mV. The SNM plot is shown in Figure 8.

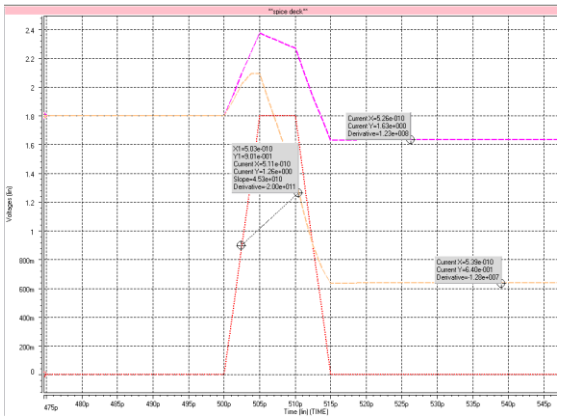

Figure 4: Read Simulation for Transistor width 1

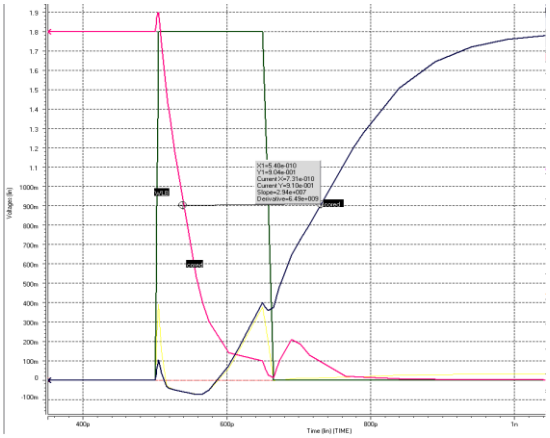

Figure 5: Write Simulation for Transistor width 1

The results show that there was no change of state of internal nodes up to a noise of 600mV but the cell changes the state when a noise of 700mV is introduced. Hence we can safely conclude that the noise margin is 600mV

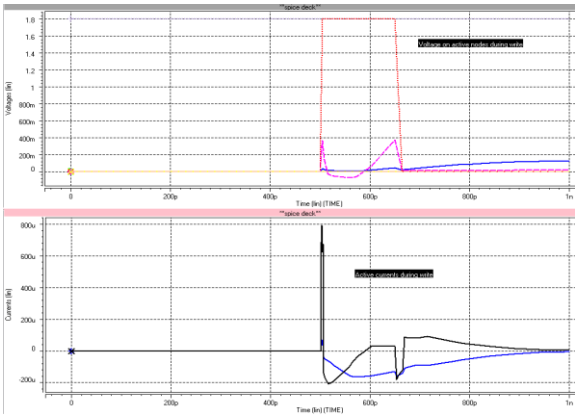

Figure.6 Dynamic Power for Transistor width 1

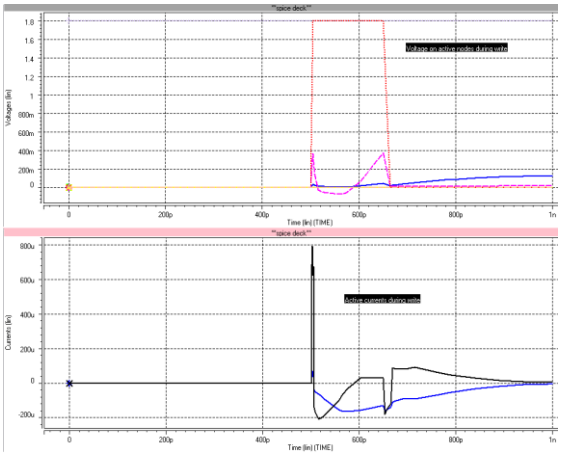

Figure 7: Leakage Power for Transistor width 1

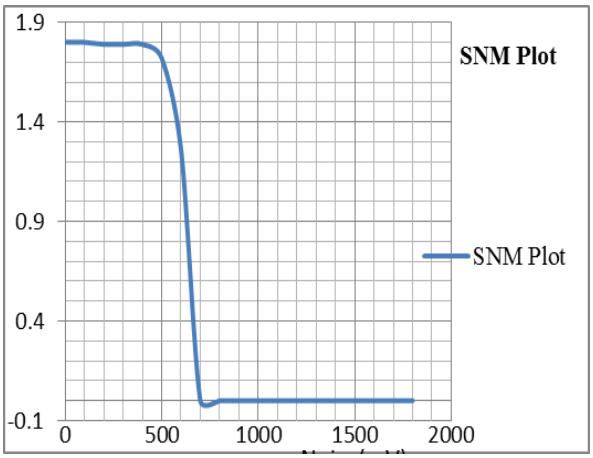

Figure 8: Static Noise margin for Transistor width 1

V. RF DESIGN USING TRANSISTOR WIDTH 2

i. Read Simulation

Read time is measured as the delay from word line reaching 50% of its final value to the time it takes the bit line differential to reach its threshold at power supply of 1.8V as showin in Figure 9. Tread= 5.603e-12sec, Iread=5.207e-05A,)

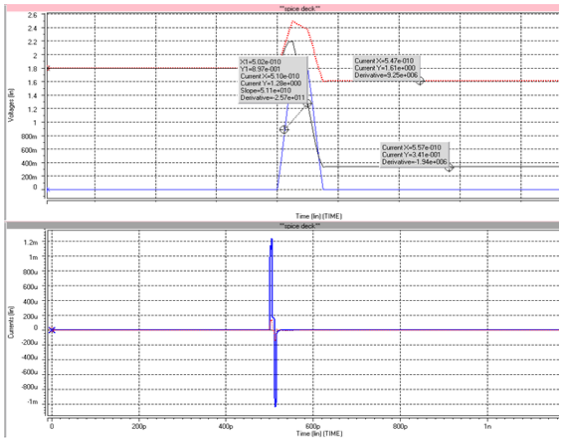

Figure 9: Read Simulation for Transistor width 2

ii. Write Simulation

Write time is measured as the time delay from word line WLB rise to the time it takes for the internal nodes to change state as shown in Figure 10.
Twrite= 1.978e-10sec

iii. Dynamic Power

Dynamic read power is the power drawn by the bitcell when the bit cell is subjected to a real-time read operation times the supply voltage. Here we model the bit cell into a read functional mode and then measure the current drawn by it from VDD. Dynamic write power is the powers drawn by the bitcell when the bit cell is subjected to a real-time write operation times the supply voltage. Here we model the bit cell into a write functional mode and then measure the current drawn by it from VDD as show in Figure 11. Pdynamic_write= 1.89e-05W, Ppeak_write= 2.3148e-03W, Pdynamic_read= 9.3726e-05W, Ppeak_read= 4.3092e-03W.

iv. Leakage Power

Leakage read power is the power drawn by the bitcell when subjected to a non-functional mode, the bit cell is turned off i.e., bit lines are floating and word lines are at logic ‘0’ times the supply voltage. Leakage write power is the power drawn by the bitcell when subjected to a non-functional mode. The bit cell is turned off i.e., bit lines are floating and word lines are at logic ‘0’ times the supply voltage.
Leak power = 175.3pW

v. Static Noise margin

In this project we designed 8T register file which has separate read and write ports. In each RF cell design writing is done by using eight transistors and during writing data we disabling the Read port so Static Noise Margin (SNM) is not affecting during hold and Read mode. During writing we use the same writing configuration in the design so the write margin (least bitline voltage required to change the state of RF cell)

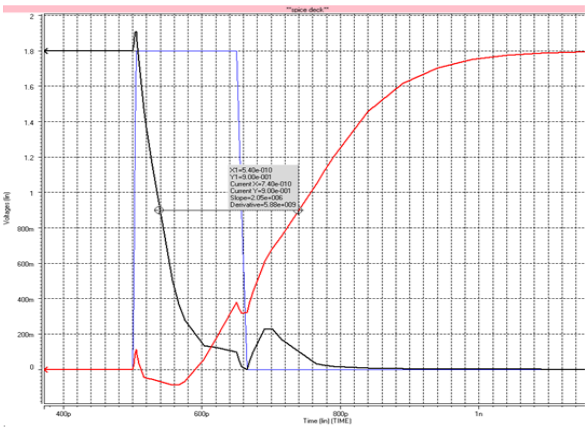

Figure 10: Write Simulation for Transistor width 2

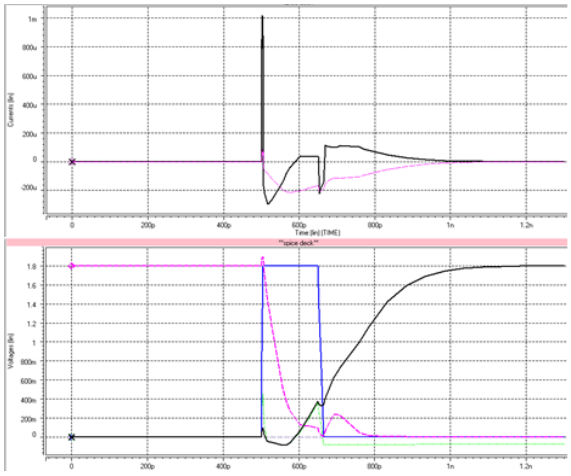

Figure 11: Dynamic Power for Transistor width 2

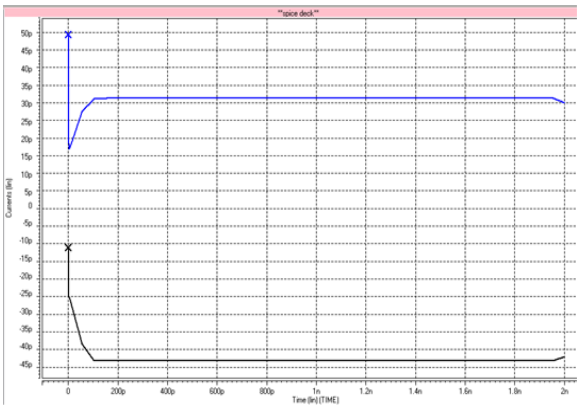

Figure 12: Leakage Power for Transistor width 2

We modeled noise as a voltage source at the internal node of the cell and increased it gradually in the steps of 100mV. The results show that there was no change of state of internal nodes up to a noise of 600mV but the cell changes the state when a noise of 700mV is introduced. Hence we can safely conclude that the noise margin is 600m. The SNM plot is showin in Figure 13.

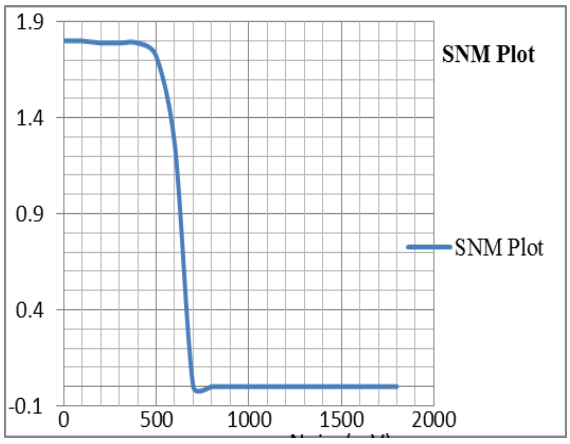

Figure 13: Static Noise margin for Transistor width 2

VI. RESULTS

Table 2: Simulation results

Parameter	RF design using Transistor width 1	RF design using Transistor width 2
Twrite (s)	1.870e-10	1.978e-10
Tread (s)	5.722e-12	5.603e-12
Iread(Amps)	3.684e-05	5.207e-05
SNM	600mV	600mV
Leakage Power (pW)	145.9	175.3
Dynamic Read Power (W)	3.51E-05	9.3726e-05
Dynamic Write Power (W)	6.6312e-05	1.89e-05
Peak Read Power (W)	3.4524e-03	4.3092e-03
Peak Write Power (W)	1.713e-03	2.3148e-03

The Table 2 shows the simulation results of the designed register file bit cells for two different transistor widths. The table indicates that the time taken for read and write operation by the register file bit cell using transistor width 1 is more than the register file bit cell using transistor width 2.

We can clearly see the trade offs resulting from the designs. Transistor Width 1design has more transistor count but it slower compared to Transistor Width 2. The design with Transistor Width 1 can be used when reducing the chip area is the motive. On the other hand Transistor Width 2 design is faster but need more power requirements and also have higher leakage currents.Transistor width 2 design can be used for when increasing the performance is the motive.

VII. CONCLUSIONS

A dual port register file bit cell is designed and implemented at 180nm technology and we observed that based on the requirement the RFs can be optimized to obtain the target parameters. If a faster access time RF is needed then the sizes of the transistors can be optimized in such a way that a high read current is achieved which reduced the access time of the memory. Alternatively if low fabrication area RF is the requirement of the application then the sizes of the transistors in the bit cell can be reduced to meet the area requirements. Reduced area of the bit cell in turn reduces the sizes of its control circuitry as well. Reducing the operating voltage is also an effective way to reduce integrated circuit power consumption but it degrades the noise margin. We then compare the two topologies in terms both write and Read operations, Leakage power, Dynamic Power (read and write power) and Static Noise margin and the measurements are tabulated.

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