Pre Charge Free, Ternary Content Addressable Memory

Venkata Ramana Datti, P.V.Sridevi

Abstract— For searching the data parallely the most widely used hardware is Ternary Content addressable memory (TCAM).The parallel searching gives high speed but also consumes high power. For higher search speed applications, NOR type matchline TCAMs are useful and NAND type matchline TCAMs are useful for low power applications. The NOR-type matchline TCAM requires high power, therefore, the reduction of its power consumption is the objective of many described designs. Here, a novel precharge free TCAM is proposed .The proposed TCAM power consumption is 20% less than the NOR type matchline TCAM. Simulations performed with cadence 45-nm technology.

Index Terms: Ternary Content addressable memory (TCAM) cell, low power, NOR-type matchline, precharge.

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1 INTRODUCTION

Now a days, internet is becoming the part of day to day life. Speed of the internet is mainly depends on its searching algorithms. But searching speed of software based search algorithms is low. So for high speed applications Ternary Content addressable memories are used. For a TCAM, input is the content and output is the address in which the content is stored. TCAM designers objective is to increase the search speed and to reduce the power consumption.
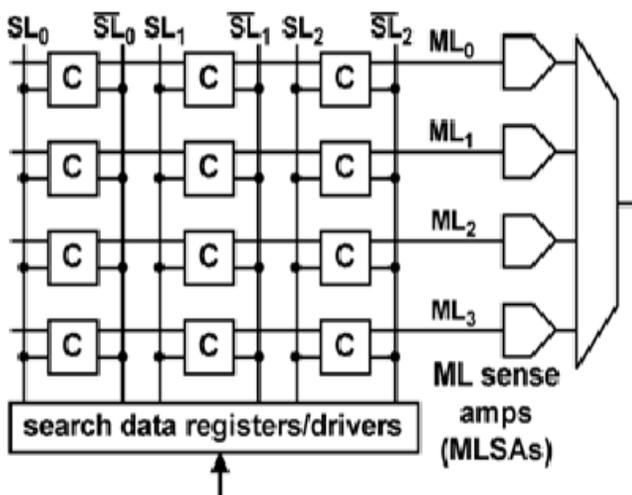

Figure 1: TCAM Architecture

TCAM is a memory element in which the information is stored in rows and search happens in parallel. Content addressable memory, takes content as an input and gives address as an output. If stored data matches with the search data then it gives address in which the data stored. A match or mismatch information is accessed by the sense amplifier. As shown in figure 1, every TCAM cell in a wordline is connected to a

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common matchline (ML). Initially all matchlines are charged to high voltage. ML value maintains at high voltage if there is a match. Otherwise the respective matchline discharges. To start a new search, all matchlines should be at high voltage. Thus, the frequent charging and discharging happens in content addressable memories. Because of this power dissipation will be more. In the proposed architecture, there is no need of frequent charging and discharging of matchline [1]. So there will be low power dissipation. Conventional TCAM is shown in figure.1[2].TCAMs are used in a number of routing applications and hardwares such as network router, cache memories[3][4][5][6].

2. TERNARY CONTENT ADDRESSABLE MEMORY

There are two types of content addressable memories. One is binary content addressable memory and the other one is ternary content addressable memory. Logic "0" and Logic "1" can be placed in binary CAM although in TCAM Logic "0", Logic "1", and don't care as well be placed . Binary CAM applications are limited compared to TCAM. TCAM cells are of NOR and NAND type. NOR type TCAM cells offers high speed but it needs more power. NAND type TCAM cells needs low power but speed is also less. Hence, on the whole NOR type cells are chosen instead of NAND type.
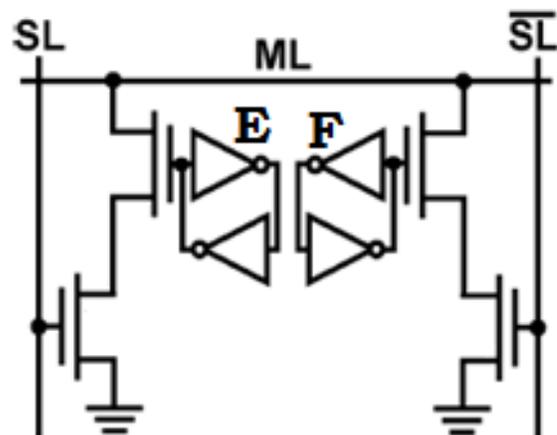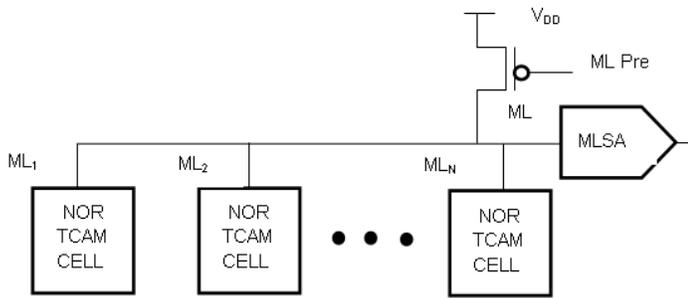

Figure 2: TCAM cell of NOR type

Figure 3: *Matchline TCAM of NOR type*

Table 1: *Encoding for NOR type ternary cell*

Stored Value	Stored	
	E	F
0	0	1
1	1	0
X	1	1

TCAM cell of NOR type is presented in Figure 2. Table 1 gives the information about its encoding. Irrespective of type of TCAM cell, it needs 2-SRAM cells which enables to store 3-states. In a TCAM, logic "0" is kept by setting E = 0 and F = 1, Logic "1" by setting E =1 and F = 0 and don't care (X) by setting E = 1 and F = 1. Here E= 0 and F = 0 is vacant state. In a TCAM, logic "0" is explored by keeping SL = 0 and $\overline{SL}$ = 1, a Logic "1" by keeping SL = 1 and $\overline{SL}$ = 0 and also don't care(X) by keeping SL = 1 and $\overline{SL}$ = 1 . Matchline TCAM structure of NOR type is presented in Figure 3. In Figure 3, TCAM cells of NOR type are connected in parallel . Conventionally, CAM operation is distributed into three parts. Namely matchline preharge, content write, and content search. At first, every matchline is charged to voltage V_{DD} by connecting low voltage to " ML Pre". Mismatch causes matchline to discharge. Therefore, for each new search, matchlines are needed to charge to V_{DD}. Because of this power dissipation is more.

3.   PROPOSED   TERNARY   CONTENT ADDRESSABLE MEMORY

The proposed architecture power consumption is less compared to existing design. Figure 4 shows the suggested TCAM cell. The ternary encoding of suggested cell is similar to traditional cell. Loading data into TCAM cell is possible by making write enable is active. T_1 and T_2 transistors are in On condition while write enable in high state. Therefore, E and F values will enters into corresponding SRAM cells.
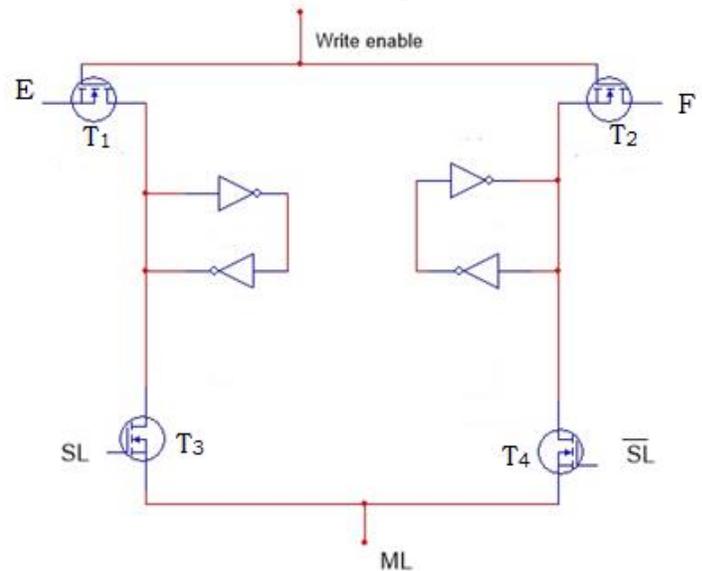

Figure 4: *Proposed TCAM cell*

If E = 0 and F = 1 means logic '0' is kept in TCAM. When SL = 0 and $\overline{SL}$ = 1 TCAM searches for logic'0'. Hence T_3 is OFF and T_4 is in On state. Therefore, ML voltage value is at logic '1' because F is at logic '1'. It indicates match. Similarly, search for logic '1' is possible by keeping SL = 1 and $\overline{SL}$ = 0 in figure 4. Here T_3 transistor is On and transistor T_4 is in OFF state. Here, ML value is at logic '0' because E is at logic '0'. In the same way, logic '1' is kept in cell by keeping E is at logic'0' and F is at logic'1'. It shows mismatch. ML Pre charging is not required here. ML logic value is decided by input logic values. By using the suggested CAM cell a new architecture is proposed. Figure 5 shows the proposed TCAM without precharge phase.
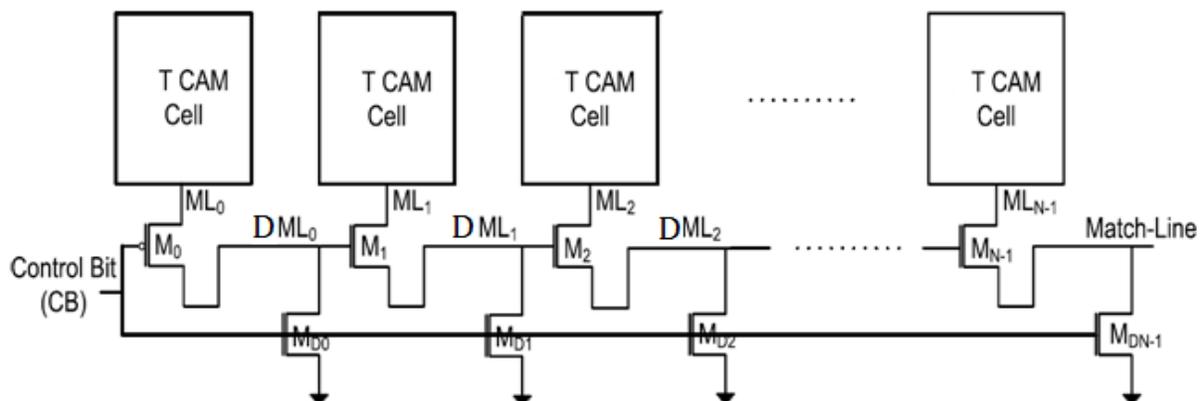

Figure 5: *Suggested TCAM without precharge logic*

Proposed TCAM operation is restricted only to two parts, Namely content write and content search. The search operation initiates by keeping control bit at logic '0'. If control bit is at logic '0' , M_0 transistor will be in ON condition and M_{D0}, M_{D1}……. M_{DN-1} transistors are in OFF condition. Suggested TCAM is explained with the help of two bit content. ML_0 is at logic '1' if first bit matches. Since ML_0 is at logic '1' , DML_0 is also at logic '1' due to pass transistor action of MOSFET M_0. Due to the value of DML_0 , M_1 is said to be in ON condition. If next bit is also ties, then DML_1 is at logic '1', therefore matchline is said to be at logic '1' which shows content match. If there is a match in the first bit and mismatch in the second bit, then ML_0 , DML_0 is at logic '1' but DML_1 is at logic'0' because ML_1 is at logic '0'. It shows data mismatch. Likewise, If there is a mismatch in the first bit and match in the second bit, then ML_0 , DML_0 is at logic '0' and DML_1 is also at logic '0' since M_1 is in OFF condition. It also shows, mismatch in data. If two bits don't match, then ML_0 , ML_1 ,DML_0, DML_1 is at logic '0' which also shows data mismatch. To avoid false match, Before performing a new search the values of DML_0 , DML_1,….. DML_{N-1} must be at low value. For this, control bit should be at logic '1'. If control bit is at logic '1' , M_{D0}, M_{D1}……. M_{DN-1} is in ON state , so the values of DML_0 , DML_1,….. DML_{N-1} is at low value.

3. RESULTS AND DISCUSSION
The conventional TCAM and proposed TCAM were simulated for 2 bits using cadence 45 nano meter technology. Simulated waveforms of conventional TCAM and proposed TCAM is presented in Figures 6 and 7 respectively. With the help of the average power waveforms, it has been noticed that the average power consumption of conventional TCAM is 26.5μW and for proposed TCAM is 22.1μW.
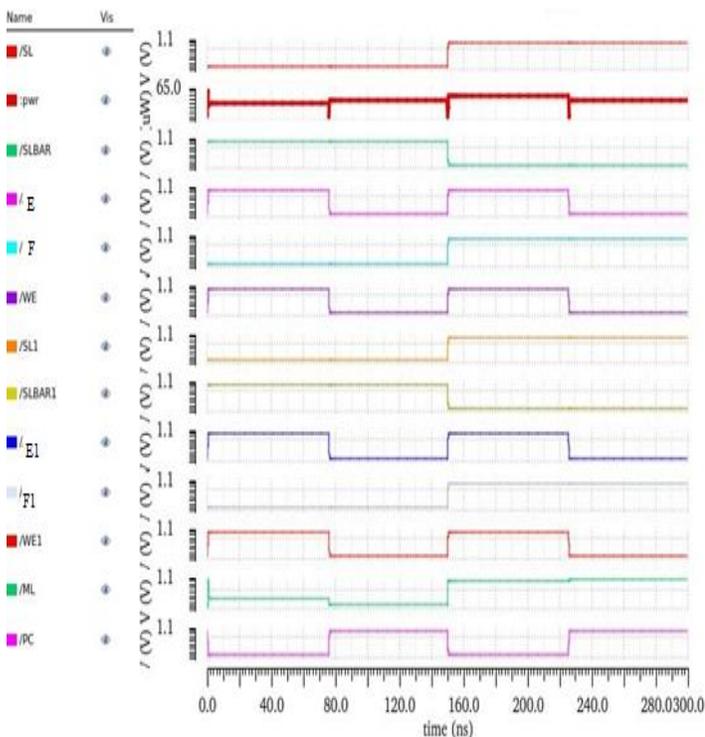

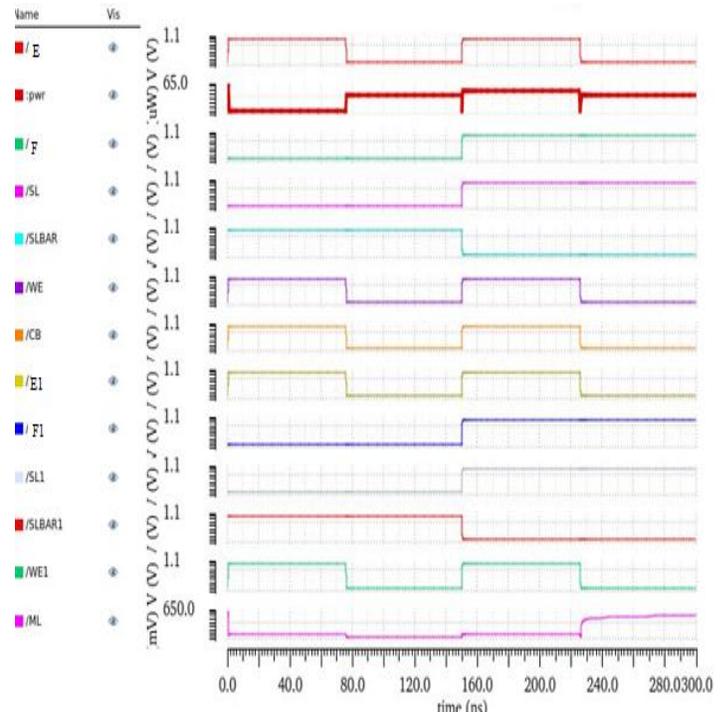**Figure 6:** *waveforms of conventional 2 bit TCAM*

Figure 7 : *waveforms of suggested 2 bit TCAM*

4. CONCLUSION
Traditional NOR type 2 bit Ternary CAM is simulated and noticed that it needs more power. The suggested TCAM is having two extra transistors per cell. The proposed 2bit TCAM is also simulated with the help of cadence and noticed that it takes 20% lesser power than the traditional. In the suggested TCAM there is no precharge phase. But the proposed TCAM is relatively less speed than conventional.

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