**PUBLIC RECORD VERSION**

**In the Matter of Rambus, Inc.**
**Docket No. 9302**

**OPINION OF THE COMMISSION**

By HARBOUR, Commissioner, for a unanimous Commission.

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## I. INTRODUCTION[1]

Rambus Inc. is a developer and licensor of computer memory technologies. For more than four years during the 1990s, Rambus participated as a member of the Joint Electron Device Engineering Council (JEDEC), an industrywide standard-setting organization (SSO) that operated on a cooperative basis. Through a course of deceptive conduct, Rambus exploited its participation in JEDEC to obtain patents that would cover technologies incorporated into now-ubiquitous JEDEC memory standards, without revealing its patent position to other JEDEC members. As a result, Rambus was able to distort the standard-setting process and engage in anticompetitive "hold up" of the computer memory industry. Conduct of this sort has grave implications for competition. The Federal Trade Commission (FTC or Commission) finds that Rambus's acts of deception constituted exclusionary conduct under Section 2 of the Sherman Act, and that Rambus unlawfully monopolized the markets for four technologies incorporated into the JEDEC standards in violation of Section 5 of the FTC Act.

Standard setting occurs in many industries and can be highly beneficial to consumers. Standards can facilitate interoperability among products supplied by different firms, which typically increases the chances of market acceptance, makes the products more valuable to consumers, and stimulates output. But standard setting also poses some risks of harm to competition. By its very nature, standard setting displaces the competitive process through which the purchasing decisions of customers determine which interoperable combinations of technologies and products will survive.

Typically, the procompetitive benefits of standard setting outweigh the loss of market competition. For this reason, antitrust enforcement has shown a high degree of acceptance of, and tolerance for, standard-setting activities. But when a firm engages in exclusionary conduct that subverts the standard-setting process and leads to the acquisition of monopoly power, the procompetitive benefits of standard setting cannot be fully realized.

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[1] This opinion uses the following abbreviations:

CA - Complaint Counsel's Appendix
CE - Order Granting Complaint Counsel's Motion for Collateral Estoppel
CCAB - Complaint Counsel's Appeal Brief
CCRB - Complaint Counsel's Reply Brief
CX - Complaint Counsel's Exhibit
DX - Demonstrative Exhibit
ID - Initial Decision of the Administrative Law Judge (ALJ)
IDF - Numbered Findings of Fact in the ALJ's Initial Opinion
JX - Joint Exhibits
RA - Respondent's Appendix
RB - Respondent's Brief on Appeal and Cross-Appeal
RFF - Respondent's Proposed Findings of Fact
RRB - Respondent's Rebuttal Brief
RX - Respondent's Exhibit
Tr. - Transcript of Trial before the ALJ.

At the beginning of a standard-setting process, if there are a number of competing technologies, and if any one of them could win the standards battle, then no single technology will command more than a competitive price. Once the standard has been set, however, the dynamic changes. Soon after a standard is adopted, industry participants likely will start designing, testing, and producing goods that conform to the standard. Early in the process of implementing a standard, industry members still might find it relatively easy to abandon one technology in favor of another. But as time passes, and the industry commits greater levels of resources to developing products that comply with the standard, the costs of switching to alternative technologies begin to rise. Industry members may find themselves "locked in" to the standardized technology once switching costs become prohibitive. Once lock-in occurs, the owner of the standardized technology may be able to "hold up" the industry and charge supracompetitive rates.

Many SSOs have taken steps to mitigate the risk of hold-up by avoiding unknowing lock-in to a technology that may command supracompetitive rates. Many SSOs, for example, require their members to reveal any patents and/or patent applications that relate to the standard. These types of disclosures enable SSO members to evaluate potential standards with more complete information about the likely consequences, before the standard is finalized. Some SSOs also require members to commit to license their patented technologies on reasonable and nondiscriminatory (RAND) terms, which may further inform SSO members' analysis of the costs and benefits of standardizing patented technologies.

JEDEC operated on a cooperative basis and required that its members participate in good faith. According to JEDEC policy and practice, members were expected to reveal the existence of patents and patent applications that later might be enforced against those practicing the JEDEC standards. In addition, JEDEC members were obligated to offer assurances to license patented technologies on RAND terms, before members voted to adopt a standard that would incorporate those technologies. The intent of JEDEC policy and practice was to prevent anticompetitive hold-up.

Rambus, however, chose to disregard JEDEC's policy and practice, as well as the duty to act in good faith. Instead, Rambus deceived the other JEDEC members. Rambus capitalized on JEDEC's policy and practice – and also on the expectations of the JEDEC members – in several ways. Rambus refused to disclose the existence of its patents and applications, which deprived JEDEC members of critical information as they worked to evaluate potential standards. Rambus took additional actions that misled members to believe that Rambus was not seeking patents that would cover implementations of the standards under consideration by JEDEC. Rambus also went a step further: through its participation in JEDEC, Rambus gained information about the pending standard, and then amended its patent applications to ensure that subsequently-issued patents would cover the ultimate standard. Through its successful strategy, Rambus was able to conceal its patents and patent applications until after the standards were adopted and the market

was locked in. Only then did Rambus reveal its patents – through patent infringement lawsuits against JEDEC members who practiced the standard.[2]

The Commission finds that Rambus violated Section 5 of the FTC Act by engaging in exclusionary conduct that contributed significantly to the acquisition of monopoly power in four relevant and related markets. We further find a sufficient causal link between Rambus's exclusionary conduct and JEDEC's adoption of the SDRAM and DDR-SDRAM standards (but not the subsequent DDR2-SDRAM standard). Questions remain, however, regarding how the Commission can best determine the appropriate remedy. Accordingly, the Commission orders additional briefing for further consideration of remedial issues.

## II. BACKGROUND

### A. Technology Background

The dispute before us involves four relevant product markets: (1) latency technology; (2) burst length technology; (3) data acceleration technology; and (4) clock synchronization technology. These markets include technologies that, beginning in 1993, have been incorporated into the JEDEC standards for computer memory, and over which Rambus now claims patent rights.[3]

#### 1. The Function of Computer Memory

Main memory – often referred to as random access memory, or RAM – consists of integrated circuits that hold temporary instructions and data for the central processing unit (CPU), the central "brain" of a computer system.[4] The CPU performs each command given by a computer user by extracting instructions from the computer's memory, then decoding and

[2] Complaint Counsel also allege that Rambus engaged in spoliation of evidence. Rambus instituted a document retention policy that entailed the systematic destruction of a large volume of documents. This destruction policy included documents related to Rambus's participation in JEDEC and Rambus's patent prosecution files. As discussed in greater detail *infra*, Section V, however, we need not resolve the spoliation question because our findings are firmly grounded on the surviving evidence.

[3] Rambus has not contested the definition of the four relevant product markets delineated by Complaint Counsel. *See infra* note 394. Nor does Rambus contest Complaint Counsel's allegation, or the ALJ's finding (which we adopt), that the relevant geographic market is worldwide. Complaint ¶ 117; IDF 1016-17; ID 250.

[4] Rhoden, Tr. 271-72; RA 3. Most types of RAM are volatile, which means they lose all data when the power is turned off or the system shuts down. CA A-3; RA 3.

executing them. Most computers use a type of RAM known as dynamic random access memory (DRAM),[5] which stores and processes information while the computer is on.[6]

DRAM is only one piece in the computer hardware infrastructure. A typical personal computer is built around a motherboard – the main circuit board upon which many of the important components of a computer system are fastened. The motherboard includes, for example, the CPU, chipset, and graphics and sound cards. A computer system also includes a system clock, a power supply, mass storage devices (such as hard drives or CD ROM drives), assorted controllers that enable the computer to connect to external peripheral devices (such as monitors, printers, and scanners), and a main memory system (containing DRAM). The main memory circuits typically attach to the memory module (a small printed circuit board that plugs into the motherboard).[7] Communications between the main memory circuits and the CPU are managed by a memory controller, which generally is part of the chipset.[8] DRAM must be compatible and interoperable with other components in the same computer system.[9]

### 2. Evolution of RDRAM and SDRAM Memory Technologies: Breaking Through the Memory Bottleneck

In the early 1980s, an imbalance emerged in the speed at which CPU technology was developing relative to memory technology.[10] CPU speeds have doubled every eighteen months for the past two decades,[11] while memory speeds have increased more slowly. This "memory

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[5] DRAM is "dynamic" because it must be refreshed every fraction of a second to prevent memory loss. Rhoden, Tr. 266-67.

[6] Rhoden, Tr. 267-68. DRAM also is incorporated into other electronic devices such as servers, printers, and cameras. IDF 3; Rhoden, Tr. 298; RA 3.

[7] Rhoden, Tr. 269, 272-73; RA 4.

[8] Rhoden, Tr. 275-76; CA A-1; RA 2.

[9] *See, e.g.*, IDF 6.

[10] IDF 27-40.

[11] Farmwald, Tr. 8068 (describing "Moore's law," based on observations by Intel co-founder Gordon Moore regarding the rate of increase in CPU speeds).

bottleneck problem"[12] became a widely recognized concern in the computer hardware industry during the early 1990s.[13] The industry considered several different solutions.[14]

One of those solutions – Rambus DRAM, or RDRAM – was developed by Rambus.[15] Rambus was founded in March 1990 by two professors who wanted to commercialize their concept for a new DRAM design that would break the "memory bottleneck."[16] Rambus develops, secures patents on, and licenses technologies to companies that manufacture semiconductor memory devices. Rambus is not a manufacturing company; rather, Rambus earns its revenue through the licensing of its patents.[17]

A month after its founding, on April 18, 1990, Rambus filed Patent Application No. 07/510,898 (the '898 application) with the U.S. Patent Trademark Office (PTO).[18] This application described many of the technologies developed and integrated into the initial RDRAM design. The '898 application also is the original source of the patents that Rambus has asserted with regard to the four technologies at issue in this case. The PTO issued a restriction requirement in late 1990, requiring Rambus to decide which of the multiple claimed inventions it wished to pursue in the '898 application. On March 5, 1992, Rambus responded to the PTO's demand by filing ten divisional applications.[19]

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[12] One of Rambus's founders, Paul Michael Farmwald, testified that the "memory bottleneck" problem was a potential bottleneck in which memory chip performance could limit computer performance. Farmwald, Tr. 8068-69, 8071-73.

[13] IDF 36-40.

[14] *See, e.g.*, CX 711 at 1; Sussman, Tr. 1359-60, 1364; G. Kelley, Tr. 2584-85. In the last decade most DRAMs have been synchronized with the system clock, in order to maximize the number of instructions a CPU can process in a given time. This design is called "synchronous DRAM," or SDRAM (as distinguished from earlier, asynchronous DRAMs). Jacob, 5394-95; CA A-4; RA 5.

[15] RDRAM reflected innovations with respect to bus width, the interface between the bus and computer chips, and the DRAM. IDF 86-90; CA A-4; RX 81 at 3,7; Horowitz, Tr. 8618-20; Rhoden, Tr. 400-401. Buses essentially are a computer's highway system. A memory bus comprises the lines that connect each memory device to the memory controller. Computer buses, like highways, can vary by width, which means they can have a differing number of lines linking the computer's components (just as highways may have more or fewer lanes to carry traffic). The speed at which a computer operates is affected by its buses. Rhoden, Tr. 275-76; CA A-1.

[16] IDF 27-48, 58; CX 533 at 8; CX 545 at 7; Farmwald, Tr. 8089-93; Horowitz, Tr. 8486.

[17] Parties' First Set of Stipulations, Item 2 (April 23, 2003); *see also* CX 2106 (Farmwald FTC Dep.) at 220 (*in camera*) ("[r]oyalties are the lifeblood of Rambus").

[18] CX 1451.

[19] A restriction requirement forces a patent applicant to separate each distinct invention or group of inventions into separate applications known as "divisionals." Nusbaum, Tr. 1509-11.

Beginning in 1990, Rambus tried to license its RDRAM technology to manufacturers of DRAM chips and DRAM-compatible microprocessors.[20] Rambus attempted to position RDRAM as the *de facto* standard.[21] Rambus made numerous presentations on RDRAM to the major DRAM manufacturers in an effort to persuade them to adopt the technology.[22] Rambus also tried to develop relationships with major systems companies, and pursued commitments from these companies to introduce systems using RDRAM technology.[23] RDRAM failed to achieve significant market success, however, at least in part because manufacturers were reluctant to pay royalties and licensing fees to Rambus.[24]

These manufacturers rejected RDRAM and instead turned to standards promulgated by JEDEC. JEDEC was a semiconductor engineering standardization body within the Electronic Industries Association (EIA). It comprised manufacturers and purchasers of DRAM, as well as producers of complementary products and computer systems.[25] JEDEC's JC 42.3 committee was responsible for RAM issues, and, in particular, for the development of DRAM standards.[26]

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[20] *See* CX 533 at 9-10. Major DRAM manufacturers included Samsung Electronics Co., Micron Technology, Inc., Hyundai Electronics Industries (subsequently, Hynix Semiconductor Inc.), LG Semicon Ltd., NEC Corporation, Siemens AG (subsequently, Infineon Technologies AG), Toshiba, Mitsubishi Electric Corporation, and Hitachi, Ltd. *See* CX 2747 at 7.

[21] *Id.* at 3.

[22] *See, e.g.*, Sussman, Tr. 1429-31; CX 535 at 1, 4-5; CX 543a at 11; CX 2107 at 63 (Oh FTC Dep.) (*in camera*).

[23] *See, e.g.*, Kellogg, Tr. 5049-54; Bechtelsheim, Tr. 5816-19; CX 535 at 2, 5-6.

[24] *See, e.g.*, Rapp, Tr. 10248-49 (RDRAM sales represented less than 2% of the market for at least six years following the adoption of SDRAM) (providing market-share statistics); JX 36 at 7 ("Some Committee members did not feel that the Rambus patent license fee fit the JEDEC requirement of being reasonable."); CX 961 at 1 (September 1997 Intel e-mail to Rambus Chief Executive Officer (CEO) Geoff Tate, stating that, upon analyzing the royalty obligations attached to RDRAM, the industry would develop alternatives); RX 1482 at 12 (post-1996 Rambus Strategic Review stating, "Memory manufacturers need to focus on cost reduction to restore profitability" and describing RDRAM as "a guaranteed bad bet for margin enhancement").

[25] *See* J. Kelly, Tr. 1774-75; Rhoden, Tr. 293-94; Landgraf, Tr. 1685; JX 18 at 1-3. Between 1991 and 1996, JEDEC was an organization within the EIA. IDF 222; J. Kelly, Tr. 2075. EIA engages in a variety of different activities in support of the electronics industry in the United States, including government relations, marketing research, trade shows, and standard setting. J. Kelly, Tr. 1750-51, 1764. In 1998, EIA was renamed the Electronic Industries Alliance, and JEDEC became an EIA division. CX 302 at 11. By the first quarter of 2000, JEDEC became separately incorporated, but remained contractually affiliated with EIA. J. Kelly, Tr. 1752; CX 302 at 11.

[26] Rhoden, Tr. 284-85, 288; Williams, Tr. 763; J. Kelly, Tr. 1769. JEDEC was divided into several committees. Each committee focused on a particular aspect of the semiconductor and solid state electronics industries, and was subdivided into several subcommittees.

At issue here are three generations of DRAM standards developed and adopted by JEDEC: synchronous DRAM (SDRAM),[27] DDR SDRAM,[28] and DDR2 SDRAM.[29] In the course of designing these standards and determining which technologies would be incorporated, the JEDEC members evaluated numerous technologies relating to various aspects of main memory, including the technologies that comprise the four relevant product markets in this case. Rambus eventually claimed that its patents cover the specific versions of these four technologies that ultimately were adopted by JEDEC for the SDRAM, DDR SDRAM, and DDR2 SDRAM standards.

### 3. The Four Relevant Technology Markets

#### a. Latency Technology

Latency is a measure of the amount of time between a request and a response.[30] Memory latency is the length of time between the memory's receipt of a read request and its release of data corresponding with the request.[31] Latency technology comprises those technologies used to control the length of this time period.[32]

In the early 1990s, several types of latency technology were available, including programmable latency, fixed latency, blowing a fuse on a DRAM, and dedicated pins. These

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[27] JEDEC designed the SDRAM standard during the early 1990s and first published it in 1993. IDF 297-315, 355-56. By 1998, JEDEC-compliant SDRAM was the most widely used type of memory device. IDF 370; CA A-5. The SDRAM standard incorporated technologies from the latency and burst length markets. IDF 355; 1013; RA 5. Rambus has asserted that its patents cover the implementations of these two technologies in the SDRAM standard. IDF 1022-29.

[28] DDR SDRAM was a second-generation standard promulgated by JEDEC. RA 2. DDR SDRAM included some of the features of SDRAM, and also incorporated new technologies that increased the speed and efficiency of the memory system. IDF 430; CA A-1. JEDEC first published DDR SDRAM in 1999. IDF 427-29; RA 2. JEDEC-compliant DDR SDRAM was forecast to overtake SDRAM as the predominant memory device by 2002-03. *See* McAfee, Tr. 7227 (presenting DX 141), 7430-31 (presenting DX 219). DDR SDRAM incorporated technologies from the latency, burst length, data acceleration, and clock synchronization markets. Rambus has asserted that its patents cover the implementations of these four technologies in the DDR SDRAM standard. IDF 1022-29.

[29] DDR2 SDRAM is the third-generation standard that JEDEC developed using SDRAM technology. RA 2; CA A-1. By the time of the 2003 trial, JEDEC had published to its members preliminary specifications for this standard that retained the latency, burst length, data acceleration, and clock synchronization technologies that Rambus has claimed infringe its patents. RA 2.

[30] IDF 114.

[31] Horowitz, Tr. 8529-30.

[32] McAfee, Tr. 7348.

alternative solutions are discussed in greater detail below.[33] JEDEC first incorporated programmable column address strobe (CAS) latency into its SDRAM standard and retained the technology in its DDR SDRAM and DDR2 SDRAM standards.[34] Programmable CAS latency controls data output timing by determining the number of clock cycles that should be allowed to elapse after a defined point.[35] Programmable CAS latency provides users of DRAMs with flexibility, *i.e.*, a single part can be programmed so as to provide the optimal latency in a variety of systems.[36]

Rambus claims that its patents cover JEDEC's implementation of programmable CAS latency technology.

b. Burst Length Technology

Burst length technology controls the amount of data transferred between the CPU and memory in each transmission. JEDEC's SDRAM, DDR SDRAM, and DDR2 SDRAM standards adopted programmable burst length technology, which provides a means for varying the number of cycles of data that are transmitted to the memory controller in response to an individual command.[37] Programmable burst length technology is similar to programmable CAS latency technology in that it allows DRAM customers to use one part for many different types of machines that require different burst lengths.[38]

In the early 1990s several alternatives to programmable burst length were available, as discussed in greater detail below.[39] One alternative was the use of fixed burst length parts.[40] Another alternative was to use "burst terminate commands," which establish a long burst length

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[33] *See infra* Section IV.C.3.b.

[34] IDF 355, 433; RA 2, 5.

[35] CA A-3.

[36] Soderman, Tr. 9346-47, 9433-34; Kellogg, Tr. 5140.

[37] CA A-3.

[38] *See, e.g.*, G. Kelley, Tr. 2550-51 ("The programmable [burst length] feature allowing you to make that selection when the PC or computer powered up was a nice feature because it allowed you to use devices that were common from multiple suppliers, put them into many different types of machines. . . . One part number fits many applications.").

[39] *See infra* Section IV.C.3.b.

[40] Jacob, Tr. 5398-99.

as the default and use the memory controller to terminate the burst if a shorter burst length is desired.[41]

Rambus claims that its patents cover JEDEC's implementation of programmable burst length technology.

### c. Data Acceleration Technology

Data acceleration technology determines the speed at which data are transmitted between the CPU and memory. JEDEC's DDR SDRAM and DDR2 SDRAM standards adopted one particular type of data acceleration technology, known as dual-edge clocking, which captures data off both the rising and falling edges (the "tick" and the "tock") of the clock.[42] This technology enables twice the amount of data to be sent in each clock cycle compared to single-edge clocking, by which data are sent only on one edge of the clock.[43]

When JEDEC was considering whether to adopt dual-edge clocking technology as part of its DDR SDRAM standard, several alternatives were available. As discussed in greater detail below,[44] alternative technologies included interleaving ranks on the module (using different clock signals for separate groups of DRAM chips), double clock frequency (operating a single-edge clock at twice the frequency of a dual-edge clock[45]), and toggle mode (which, as formulated by IBM, combined synchronous and asynchronous features[46]).

Rambus claims that its patents cover JEDEC's implementation of dual-edge clocking technology.

### d. Clock Synchronization Technology

Clock synchronization technologies coordinate the internal clock on each DRAM chip with the timing of the computer's system clock. Phase lock loop (PLL) and delay lock loop (DLL) technologies use circuits to align more closely the timing of the internal clock on each

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[41] Jacob, Tr. 5409-10.

[42] RA 3.

[43] CA A-2.

[44] *See infra* Section IV.C.3.b.

[45] Jacob, Tr. 5433-34.

[46] *See* Jacob, Tr. 5608, 5416-17; Soderman, Tr. 9398; G. Kelley, Tr. 2514.

DRAM with the system clock.[47] Rambus developed a technology that places a PLL/DLL[48] on the SDRAM chip itself.[49] On-chip PLL/DLL clock synchronization technology was incorporated into JEDEC's DDR SDRAM and DDR2 SDRAM standards.

One alternative approach to on-chip PLL/DLL involved placing a PLL/DLL circuit on the memory controller that synchronizes all DRAMs.[50] Another approach involved placing one or more PLL/DLL circuits on the memory module.[51] Still other alternatives involved the use of vernier circuits, which introduce static delays on a signal to reduce timing uncertainties in a memory system, or reliance on a data strobe to signal the memory controller the timing of data capture.[52] These alternatives, which were considered by JEDEC prior to its adoption of on-chip PLL/DLL, are discussed in greater detail below.[53]

Rambus claims that its patents cover JEDEC's implementation of on-chip PLL/DLL technology.

## B. Procedural History

### 1. History of FTC Matter

The Complaint in this matter was issued on June 18, 2002. The Complaint charged that Rambus: (1) monopolized certain memory technology markets through a pattern of anticompetitive and exclusionary conduct; (2) attempted to monopolize these markets; and (3) engaged in unfair methods of competition.[54]

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[47] Jacob, Tr. 5442-43; Kellogg, Tr. 5150-55; RA 4; CA A-3. PLLs use voltage oscillators to synchronize the internal clock with the system clock. *See* Jacob, Tr. 5443, 5616-17; Soderman, Tr. 9401. In contrast, DLLs introduce a variable amount of delay into the internal clock to synchronize that clock with the system clock. *See* Jacob, Tr. 5443, 5616-17; Soderman, Tr. 9401.

[48] Horowitz, Tr. 8607 (Rambus co-founder testified that, under his usage of the terms, "a PLL is the generic term for any circuitry that adjusts phase, so a DLL is a kind of PLL").

[49] Farmwald, Tr. 8117-18; Horowitz, Tr. 8503-05; 8521-22, 8527-28.

[50] Jacob, Tr. 5445.

[51] Jacob, Tr. 5448-49.

[52] Jacob, Tr. 5450, 5456-57.

[53] *See infra* Section IV.C.3.b.

[54] *See* Complaint ¶¶ 122-24.

The Complaint's allegations focused on Rambus's participation in JEDEC. It alleged that Rambus deceived JEDEC's members by, for example, concealing the fact that it

> was actively working to develop, and did in fact possess, a patent and several pending patent applications that involved specific technologies proposed for and ultimately adopted in the relevant standards. By concealing this information – in violation of JEDEC's own operating rules and procedures – and through other bad-faith, deceptive conduct,

Rambus allegedly conveyed the "materially false and misleading impression that it possessed no relevant intellectual property rights"[55] and that it had no plans to enforce any intellectual property rights that might later become relevant, leaving a materially misleading impression of its intellectual property ownership and plans.[56] The Complaint further alleged that Rambus's conduct resulted in anticompetitive effects including: increased royalties; increased prices for memory products compliant with JEDEC standards; decreased incentives to produce memory using JEDEC-compliant memory technology; and decreased incentives to participate in, and rely on, standard-setting organizations and activities.[57] According to the Complaint, Rambus gave no notice that it intended to claim patent rights over technologies used in JEDEC's DRAM standards, and, by failing to do so, likely affected the content of those standards and/or the terms on which Rambus later licensed its patent rights.[58]

a. Pre-Trial Orders

The case was first assigned to Administrative Law Judge (ALJ) James P. Timony and, upon his retirement, was reassigned to Chief ALJ Stephen J. McGuire.[59] Before retiring, ALJ Timony issued two orders on February 26, 2003: first, an Order Granting Complaint Counsel's Motion for Collateral Estoppel; and second, an Order on Complaint Counsel's Motions for Default Judgment and for Oral Argument. Both orders influenced the trial and ALJ McGuire's Initial Decision.

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[55] *See* Complaint ¶ 2; *see also id.* ¶¶ 54 (alleging deception and bad-faith conduct), 71 (alleging that Rambus conveyed "a materially false and misleading impression").

[56] *See* Complaint ¶¶ 70-78.

[57] *See* Complaint ¶¶ 119-120.

[58] *See* Complaint ¶¶ 62, 65, 69, 70-78, 86.

[59] All references within this opinion to "the ALJ," unless otherwise specifically identified, will refer to ALJ McGuire.

On February 12, 2003, Complaint Counsel filed a motion seeking recognition of the collateral estoppel effect of prior factual findings that Rambus had destroyed material evidence. ALJ Timony granted the motion, thus barring Rambus from re-litigating certain findings of fact made by the district court in prior private litigation, *Rambus Inc. v. Infineon Technologies AG*.[60] Those findings included:

1. When Rambus instituted its document retention policy in 1998, it did so, in part, for the purpose of getting rid of documents that might be harmful in litigation.

2. Rambus, at the time it implemented its document retention policy, … [c]learly … contemplated that it might be bringing patent infringement suits during this timeframe if its efforts to persuade semi-conductor manufacturers to license its JEDEC-related patents were not successful.

3. Rambus's document destruction was done in anticipation of litigation.[61]

Complaint Counsel also moved for default judgment as a remedy to counter Rambus's intentional destruction of documents. ALJ Timony denied the motion, but set forth seven rebuttable adverse presumptions against Rambus. The presumptions included:

1. Rambus knew or should have known from its pre-1996 participation in JEDEC that developing JEDEC standards would require the use of patents held or applied for by Rambus;

2. Rambus never disclosed to other JEDEC participants the existence of these patents; [and]

3. Rambus knew that its failure to disclose the existence of these patents to other JEDEC participants could serve to equitably estop Rambus from enforcing its patents as to other JEDEC participants.[62]

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[60] 155 F. Supp. 2d 668 (E.D. Va. 2001), *aff'd in part and rev'd in part*, 318 F.3d 1081 (Fed. Cir. 2001). The district court's findings, upon which ALJ Timony relied, were not raised on appeal to the Federal Circuit.

[61] CE at 5 (internal quotations omitted).

[62] Order on Complaint Counsel's Motions for Default Judgment and for Oral Argument at 9 (Feb. 26, 2003).

Four additional presumptions addressed the foreseeability of litigation and Rambus's document retention program.[63]

b. ALJ McGuire's Initial Decision

On February 17, 2004, ALJ McGuire issued his Initial Decision and Proposed Order dismissing the Complaint in its entirety. Specifically, although he noted that Section 5 of the FTC Act authorizes the FTC to define and proscribe unfair methods of competition, the ALJ determined that Complaint Counsel had established no basis for finding a violation of Section 5.[64] He concluded that Complaint Counsel's arguments lacked a reasonable basis in law,[65] and ruled that Complaint Counsel's factual showing was insufficient to establish a violation even if the legal theories had been deemed adequate.[66]

The ALJ found that the adverse presumptions entered by ALJ Timony were not material to the disposition of the case. The ALJ found no indication that Rambus had destroyed any relevant and material documents. He found that the first and second presumptions were moot because Rambus was not required to disclose its patents or patent applications.[67] He also rejected the second presumption on the ground that Rambus's conduct raised sufficient red flags to put members of JEDEC on notice that Rambus had applications pending.[68] The ALJ then found the remaining five adverse presumptions to be irrelevant to the material issues of the case.

The ALJ found that there was no causal link between JEDEC's adoption of Rambus's technology into its standards and Rambus's acquisition of monopoly power. Rather, the ALJ found that Rambus acquired its monopoly power as a result of superior technology and market preferences.[69] Moreover, the ALJ found that JEDEC, and many members of the DRAM industry, were aware of Rambus's patent portfolio. Thus, according to the ALJ, no member of JEDEC

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[63] *Id*. (announcing presumptions that Rambus's document retention program failed to provide adequate guidance and direction to its employees and that Rambus knew or should have known that litigation over the enforcement of its patents was reasonably foreseeable).

[64] ID at 254.

[65] ID at 254-60.

[66] ID at 259-61.

[67] ID at 244.

[68] ID at 244-45.

[69] ID at 300-04.

reasonably could have relied on any misrepresentation or omission by Rambus in its dealings with JEDEC.[70] The ALJ found no basis for ascribing to Rambus an intent to deceive.[71]

The ALJ concluded that the challenged conduct did not result in any anticompetitive effect because Complaint Counsel failed to prove there were viable alternatives to Rambus's technologies.[72] Furthermore, according to the ALJ, Complaint Counsel did not demonstrate that Rambus's conduct had resulted in higher prices to consumers.[73] In contrast, the ALJ found that Rambus had put forth legitimate business justifications for its conduct. He agreed with Rambus that its secrecy regarding its patent applications constituted normal and legitimate protection of trade secrets. The ALJ concluded that this business justification precluded a finding of exclusionary conduct.[74]

Finally, the ALJ found that the DRAM industry never became locked into using Rambus's technologies as incorporated into the JEDEC standards, because "economic evidence shows that switching costs and coordination issues would not prevent the DRAM industry from going to alternatives."[75]

### c. Questions Raised on Appeal/Cross Appeal

Complaint Counsel filed a notice of appeal on March 1, 2004. They challenge virtually all of the ALJ's rulings and ask that the Initial Decision be set aside in its entirety. They contend that Rambus acquired monopoly power by pursuing a secret and deliberate pattern of conduct to obtain patents covering JEDEC standards. According to Complaint Counsel, Rambus's course of conduct undermined the fundamental purpose of JEDEC to adopt open standards; contravened JEDEC's procedures for adopting patented technologies only on the basis of full information and after securing a commitment to reasonable licensing terms; breached Rambus's duty of good faith; and also violated Rambus's specific obligation, as a member of JEDEC, to disclose patents and patent applications that might be involved in JEDEC's work.[76] Complaint Counsel claim that the facts and a proper application of the law show that Rambus violated Section 5 of the FTC Act, and they offer a proposed cease and desist order to remedy the alleged violation.

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[70] ID at 304-09.

[71] ID at 295-300, 331-32.

[72] ID at 312-16.

[73] ID at 323-26.

[74] ID at 287-89.

[75] ID at 328, 326-29.

[76] CCAB at 27-28.

Rambus filed a cross appeal arguing that the ALJ erred by applying a "preponderance of the evidence" standard to the government's case, rather than requiring Complaint Counsel to meet a "clear and convincing" burden of proof. Rambus contends that the heightened burden of proof is required due to an "inherent tension" between the interests served by the patent and antitrust laws, as well as by similarities to cases that have required clear and convincing evidence in assessing alleged failures to disclose material information and bad faith enforcement of patents. Rambus also argues that the nature of the remedy sought by Complaint Counsel (which Rambus views as essentially terminating its patent rights), and important policy considerations implicated by SSOs, merit application of the clear and convincing standard.

#### d. Re-Opening of the Record Before the Commission

The ALJ closed the record on October 9, 2003. The Commission later reopened the record to admit supplemental evidence – entering orders on May 13, 2005, July 20, 2005, and February 2, 2006 – after finding compelling circumstances. The first two orders reopened the record to allow the admission of documents produced in the *Infineon* litigation relating to Rambus's alleged spoliation of evidence, as well as the submission of amended proposed findings of fact and conclusions of law in light of this supplemental evidence. In the third order, the Commission reopened the record to admit documents on Rambus's back-up tapes, described as newly found, from discovery produced during the *Hynix* litigation.[77]

#### e. Motion for Sanctions

On August 10, 2005, Complaint Counsel moved for sanctions, asserting that Rambus had committed spoliation of evidence. Complaint Counsel asked for entry of default judgment or such other relief as the Commission deems appropriate. Rambus replied on August 17, 2005, arguing that Complaint Counsel failed to prove that Rambus acted in egregious bad faith when it adopted its document retention policy or that the effect of that policy has been to deprive Complaint Counsel of the ability to obtain a full and fair adjudication of this case.

### 2. Non-FTC Judicial Developments Relating to this Proceeding

Rambus is engaged in myriad litigations involving its efforts to enforce patents it claims cover JEDEC's DRAM standards. Rambus has sued, or been sued by, several of the major DRAM manufacturers, including Samsung, Hynix, Infineon, and Micron.[78] Although Rambus

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[77] For discussion of the *Infineon* and *Hynix* litigation, *see infra* Section II.B.2.

[78] These actions include a variety of patent infringement and antitrust-related allegations. *See, e.g.*, Hynix Semiconductor Inc. v. Rambus Inc., No. CV-00-20905 RMW (N.D. Cal.); Rambus Inc. v. Hynix Semiconductor Inc., *et al.*, No. CV-05-00334 RMW (N.D. Cal.); Rambus Inc. v. Samsung Electronics Co., No. CV-05-02298 RMW

and Infineon settled their litigation in 2005, all of the actions involving other companies are ongoing. In addition, the U.S. Department of Justice (DOJ) is investigating whether the major DRAM manufacturers engaged in price fixing in the DRAM market; four of those manufacturers have entered plea agreements.[79] While we will not discuss each of these non-FTC actions in detail, we will highlight certain relevant information.

In late 2000, Rambus sued Infineon Technologies AG, a manufacturer of semiconductor memory devices, in the U.S. District Court for the Eastern District of Virginia for infringement of four patents. Infineon counterclaimed, alleging Rambus committed fraud under Virginia state law by failing to disclose to JEDEC its patents and patent applications related to the organization's SDRAM and DDR SDRAM standards, as required by JEDEC's rules. During trial, Judge Payne granted judgment as a matter of law (JMOL) for Infineon, holding that Infineon did not infringe Rambus's patents. The jury later found Rambus liable for fraud associated with JEDEC's standard-setting activities on SDRAM and DDR SDRAM technologies. In response to post-trial JMOL motions by Rambus, the court set aside the jury's verdict of fraud regarding the DDR SDRAM technology, but let stand the fraud verdict regarding the SDRAM technology.[80] The court then issued an injunction against Rambus and awarded attorney fees to Infineon. Both Rambus and Infineon appealed to the Federal Circuit.

In a 2-1 opinion, the U.S. Court of Appeals for the Federal Circuit vacated the JMOL of noninfringement and remanded the case for consideration under a revised claim construction.[81] In addition, the court reversed the denial of JMOL that had allowed the SDRAM fraud verdict to stand, holding that clear and convincing evidence did not support the implicit jury finding that Rambus breached a duty to disclose its patents or patent applications as required by JEDEC's rules. Finally, the Federal Circuit upheld the district court's decision to set aside the DDR SDRAM fraud verdict. These holdings rendered the injunction against Rambus moot, and required the Federal Circuit to vacate and remand the award of attorney fees for reconsideration.

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(N.D. Cal.); Samsung Electronics Co. v. Rambus, Inc., No. 3:05-CV-00406-REP (E.D. Va.); Micron Technology, Inc. v. Rambus Inc., No. 3:06-CV-00132-REP (E.D. Va.); Rambus Inc. v. Micron Technology, Inc., No. CV-06-00244 RMW (N.D. Cal.); Micron Technology, Inc. v. Rambus Inc., No. CV-00-792-KAJ (D. Del.); Rambus Inc. v. Micron Technology, Inc., *et. al.*, No. 04-431105 (San Francisco Super. Ct.).

[79] *See* Plea Agreement, United States v. Samsung Electronics Co., No. CR 05-0643 (PJH) (N.D. Cal. Nov. 30, 2005), *available at* http://www.usdoj.gov/atr/cases/f213400/213483.pdf; Plea Agreement, United States v. Hynix Semiconductor Inc., No. CR 05-249 (PJH) (N.D. Cal. May 11, 2005), *available at* http://www.usdoj.gov/atr/cases/f209200/209231.pdf; Plea Agreement, United States v. Infineon Techs. AG, No. 04-299 (PJH) (N.D. Cal. Oct. 20, 2004), *available at* http://www.usdoj.gov/atr/cases/f206700/206700.pdf; *cf.* Information, United States v. Elpida Memory, Inc., No. CR 06-0059 (MMC) (N.D. Cal. Jan. 30, 2006), *available at* http://www.usdoj.gov/atr/cases/f214300/214342.pdf.

[80] Rambus, Inc. v. Infineon Techs. AG, 164 F. Supp. 2d 743 (E.D. Va. 2001).

[81] Rambus, Inc. v. Infineon Techs. AG, 318 F.3d 1081 (Fed. Cir. 2003).

Following remand, Infineon moved to compel production of various documents that Rambus was withholding on the basis of attorney-client and work product privileges. Specifically, the motion was a continuation of an earlier motion to compel under the "crime/fraud exception" to the attorney-client privilege. In ruling on the earlier motion, the district court had concluded that "Rambus implemented a 'document retention policy,' in part, for the purpose of getting rid of documents that might be harmful in litigation."[82]

On May 18, 2004, the district court entered a second order compelling Rambus to produce additional documents.[83] Under this order, the court held that the crime/fraud exception extends to materials or communications created in planning, or in furtherance of, spoliation of evidence.[84] The court also found that Rambus's intentional destruction of documents was "an integral part of its licensing and litigation strategy."[85] The court then required Rambus to produce certain documents that Rambus had claimed were privileged, and allowed Infineon to conduct discovery on the appropriate sanctions for Rambus's behavior.[86]

In March 2005, at the conclusion of a bench trial, Judge Payne orally dismissed Rambus's patent claims against Infineon. The court found that Infineon had proven, by clear and convincing evidence, that Rambus possessed unclean hands and that Rambus had engaged in extensive spoliation of evidence.[87] Before Judge Payne issued a written opinion setting forth his findings, however, Rambus and Infineon settled all of their pending litigation, including the case before Judge Payne.

As mentioned above, the *Infineon* litigation was only one of many actions involving Rambus and the major semiconductor companies. The other cases have yet to reach a resolution, but there have been some developments worth noting. In *Hynix Semiconductor, et al. v. Rambus Inc.*, the federal district court for the Northern District of California held a two-week trial on Hynix's unclean hands defense to Rambus's patent infringement claims. Judge Whyte issued an opinion on January 4, 2006, concluding that Hynix's defense failed, after finding that Rambus "did not engage in unlawful spoliation of evidence" and that "the evidence presented does not

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[82] *See* Rambus, Inc. v. Infineon Techs. AG, 155 F. Supp.2d 668, 682 (E.D. Va. 2001).

[83] Rambus, Inc. v. Infineon Techs. AG, 222 F.R.D. 280 (E.D. Va. 2004).

[84] *Id.* at 290.

[85] *Id*. at 298.

[86] *Id*. at 299.

[87] *See* Samsung Elecs. Co. v. Rambus, Inc., 398 F. Supp. 2d 470, 473 (E.D. Va. 2005) (discussing Judge Payne's ruling).

bear out Hynix's allegations that Rambus adopted its Document Retention Policy in bad faith."[88] On April 24, 2006, a jury found that Hynix had infringed Rambus's patents and awarded Rambus damages of $307 million.[89] On July 17, 2006, Judge Whyte granted summary judgment to Rambus on Hynix's claims based on breach of contract, promissory estoppel, and constructive fraud but denied summary judgment for Rambus on Hynix's claims based on allegations of actual fraud.[90] The court also determined that "breach of the JEDEC disclosure policies, without more, cannot give rise to antitrust liability," but it ruled that "Hynix is not barred from asserting that Rambus's overall course of conduct, which may include the circumstances and intent behind its decision to not disclose its patents and patent applications, violated antitrust laws."[91] Hynix's remaining contentions that the patents are unenforceable have not yet been tried.

In *Micron v. Rambus*, currently pending in the U.S. District Court for the District of Delaware, a Special Master recently issued recommendations to the court on the disposition of Micron's motion to compel. Micron sought the production of certain privileged documents pursuant to the crime/fraud exception. In his report to the judge, the Special Master found that the exception did not apply, in part because there was no evidence of fraud. That finding, in turn, rested on an analysis of JEDEC's rules, similar to the analysis set forth in the Federal Circuit's *Infineon* decision.[92] The district court affirmed that analysis and conclusion, based on Virginia state fraud law.[93]

Finally, in *Samsung v. Rambus*, the U.S. District Court for the Eastern District of Virginia recently concluded that Rambus had engaged in spoliation of evidence by destroying documents likely to be relevant at a time when Rambus anticipated or reasonably should have anticipated

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[88] Hynix Semiconductor Inc. v. Rambus Inc., No. CV-00-20905 RMW, 2006 WL 565893, at *25, *28 (N.D. Cal. Jan. 5, 2006).

[89] *See* Special Verdict Form, Hynix Semiconductor Inc. v. Rambus Inc., No. CV-00-20905 RMW (N.D. Cal. Apr. 24, 2006), *available at* www.cand.uscourts.gov/cand/judges.nsf/bc83a5777591b96f88256d480060b73c/3db5d3212d350fc88825715a005f7b13/$FILE/00-20905.pdf. The court subsequently ordered a new trial on the issue of damages, but gave Rambus the option of accepting damages in the amount of $134 million. Hynix Semiconductor Inc. v. Rambus Inc., No. CV-00-20905 RMW, 2006 WL 1991760 (N.D. Cal. July 14, 2006).

[90] Hynix Semiconductor Inc. v. Rambus Inc., No. CV-00-20905 RMW, 2006 WL 2038357, at *5-9 (N.D. Cal. July 17, 2006).

[91] *Id.* at *12.

[92] Special Master's Report and Recommendations on Motion of Micron Technology to Compel Defendant Rambus to Produce Certain Documents, Testimony and Pleadings, Micron Tech., Inc. v. Rambus Inc., CV-00-792-KAJ (D. Del. Mar. 6, 2006).

[93] Memorandum Order, *Micron v. Rambus*, CV-00-792-KAJ, 2006 WL 1653136 (D. Del. June 15, 2006).

litigation.[94] Ruling in the context of Samsung's motion for an award of attorney's fees, the court found that Rambus planned for litigation throughout 1998 and 1999 and, "as part of the plan . . . implemented a pervasive document destruction program" that targeted "discoverable documents."[95] The court deemed the contrary ruling in *Hynix* "not persuasive."[96]

## III. STANDARD OF REVIEW

We review the record *de novo* by considering "such parts of the record as are cited or as may be necessary to resolve the issues presented and . . . exercis[ing] all the powers which [the Commission] could have exercised if it had made the initial decision."[97] *De novo* review is particularly appropriate in this case because we must consider supplemental evidence, as well as new proposed findings of fact and conclusions of law, that were unavailable to the ALJ.[98] In light of our plenary review, we set aside all findings and conclusions of the ALJ, other than those that are expressly cited and relied upon.

### A. Standard of Proof: The Preponderance of the Evidence Standard Applies in FTC Adjudications

FTC enforcement actions typically are governed by the preponderance of the evidence standard.[99] The Supreme Court has held that Section 7(c) of the Administrative Procedure Act (APA), which is applicable to administrative adjudicatory proceedings unless otherwise provided by statute, establishes "a standard of proof and . . . the standard adopted is the traditional preponderance-of-the evidence standard."[100] Furthermore, the preponderance of the evidence

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[94] Samsung Elecs. Co. v. Rambus Inc., No. 3:05-CV-00406-REP, 2006 WL 2038417 (E.D.Va. July 18, 2006).

[95] *Id*. at *42.

[96] *Id*. at *38.

[97] 16 C.F.R. § 3.54 (2005).

[98] The record was reopened on separate occasions after the Initial Decision to admit documents relating to Rambus's alleged spoliation of evidence and documents on Rambus's newly found backup tapes. *See supra* Section II.B.

[99] *See, e.g.*, In re Adventist Health System West, 117 F.T.C. 224, 297 (1994) ("Each element of the case must be established by a preponderance of the evidence"); FTC v. Abbott Laboratories, 853 F. Supp. 526, 535 (D.D.C. 1994) (government must show "by a preponderance of the evidence that [respondent's] action was the result of collusion with its competitors").

[100] Steadman v. SEC, 450 U.S. 91, 95-102 (1981) (considering standard of proof in SEC proceedings adjudicating alleged violations of the anti-fraud provisions of the securities laws).

standard generally applies in civil suits to enforce federal statutes such as the antitrust laws.[101] Rambus acknowledges that the preponderance of the evidence standard applies in most agency adjudicatory proceedings, including FTC adjudications.[102] Nevertheless, Rambus advances four arguments why the Commission should apply the clear and convincing evidence standard in this matter.[103]

### 1. Relationship between Patent and Antitrust Law in Cases Involving Fraud on the Patent Office or Patent Enforcement Initiated in Bad Faith

Rambus argues that "Complaint Counsel should bear the burden of proving the essential elements of their claims by clear and convincing evidence"[104] because of what it terms the "inherent tension between the patent and antitrust laws."[105] Rambus's attempt, however, to broaden the applicability of the clear and convincing evidence standard based on "inherent tension" between the patent and antitrust laws is unavailing. Patents are not inherently in tension with antitrust law. Patents do not necessarily create market power.[106] More fundamentally, competition and patent policy both are aimed at encouraging innovation that benefits consumers, and generally work well together in doing so.[107]

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[101] *See* Herman & MacLean v. Huddleston, 459 U.S. 375, 387-91 (1983).

[102] RB at 134.

[103] RB at 134-40.

[104] RB at 140.

[105] RB at 134.

[106] Ill. Tool Works, Inc. v. Indep. Ink, Inc., 126 S. Ct. 1281 (2006); *see also* U.S. DEP'T OF JUSTICE & FED. TRADE COMM'N, ANTITRUST GUIDELINES FOR THE LICENSING OF INTELLECTUAL PROPERTY ¶ 2.2 (1995) [hereinafter IP GUIDELINES], *available at* http://www.ftc.gov/bc/0558.pdf.

[107] *See* Atari Games Corp. v. Nintendo of America, Inc., 897 F.2d 1572, 1576 (Fed. Cir. 1990) ("[T]he aims and objectives of patent and antitrust laws may seem, at first glance, wholly at odds. However, the two bodies of law are actually complementary, as both are aimed at encouraging innovation, industry and competition."); IP GUIDELINES, supra note 106, ¶ 1.0 (the patent and antitrust laws "share the common purpose of promoting innovation and enhancing consumer welfare"); FED. TRADE COMM'N, TO PROMOTE INNOVATION: THE PROPER BALANCE OF COMPETITION AND PATENT LAW AND POLICY, ch. 1 at 7-9 (2003) [hereinafter FTC INNOVATION REPORT], *available at* http://www.ftc.gov/os/2003/10/innovationrpt.pdf. When market power does result, "Antitrust law recognizes that a patent's creation of monopoly power can be necessary to achieve a greater gain for consumers." *Id.* at 9. Correspondingly, "[T]he Patent Clause itself reflects a balance between the need to encourage innovation and the avoidance of monopolies which stifle competition without any concomitant advance in the 'Progress of Science and useful Arts.'" Bonito Boats, Inc. v. Thunder Craft Boats, 489 U.S. 141, 146 (1989) (quoting Article 1, Section 8 of the Constitution).

Nevertheless, Rambus suggests that two cases, in particular, support an extension of the clear and convincing standard to the facts in this proceeding. Neither case creates such a broad rule. The first case Rambus relies on is the Supreme Court's decision in *Walker Process Equipment v. Food Machinery & Chemical Corp.*[108] In *Walker Process*, the Supreme Court held that a patentee may be liable for violation of the antitrust laws if it enforces a patent obtained by knowing and willful fraud on the PTO, and if all other elements of a violation of Section 2 of the Sherman Act are established.[109] The rationale for this holding was to achieve "a suitable accommodation" between policies of the patent and antitrust laws by enjoining enforcement of a patent that conferred monopoly power when the patent was "procured by deliberate fraud."[110] Complaint Counsel in this case do not, however, allege that Rambus procured its patents through fraud on the PTO. Rather, it is alleged that Rambus manipulated the JEDEC standard-setting process by engaging in deceptive conduct, resulting in the unknowing adoption of standards that included Rambus's lawfully patented technologies.

Rambus's reliance on *Handgards, Inc. v. Ethicon, Inc.*[111] is similarly misplaced. The plaintiff there based a monopolization claim on allegations that the patentee pursued infringement actions in bad faith – with the knowledge that the patents, though lawfully obtained, were invalid.[112] To provide a "means whereby the bad faith infringement action can be identified post hoc with a sufficiently high degree of certainty," the court held that an infringement suit presumptively is filed in good faith, and that the presumption can be rebutted only by clear and convincing evidence.[113] The court acknowledged that the clear and convincing standard is "not one intended to be utilized in antitrust litigation generally," and expressly limited its holding on

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[108] 382 U.S. 172 (1965).

[109] *Id*. at 172, 175-77.

[110] *Id*. at 189-90 (J. Harlan, concurring); *see also id*. at 176; Nobelpharma AB v. Implant Innovations, Inc., 141 F.3d 1059, 1068-69 (Fed. Cir. 1998) (discussing the context in which the Supreme Court established the requirement of knowing and willful fraud). Subsequent cases established that, in *Walker Process* contexts, knowing and willful fraud on the PTO must be proven by clear and convincing evidence. *See* C. R. Bard, Inc. v. M3 Systems, Inc., 157 F.3d 1340, 1365 (Fed. Cir. 1998) (indicating that clear and convincing evidence is necessary because of "the ease with which routine patent prosecution may be portrayed as tainted conduct"); Caphote Corp. v. DeSoto Chemical Coatings, Inc., 450 F.2d 769, 772 (9th Cir. 1971) (justifying the clear and convincing evidence standard for finding *Walker Process* fraud on grounds of the "tortuous" road to the Patent Office and the complexity of patent litigation).

[111] 601 F.2d 986 (9th Cir. 1979).

[112] 601 F.2d at 986, 993-94 (noting that bad faith "is a subjective state of mind the existence of which, while not susceptible to certain proof, easily can spring from suggestive and weakly corroborative circumstances").

[113] *Id*. at 993, 996 (noting that the clear and convincing standard in *Walker Process* and *Handgards* is commensurate with the statutory presumption of patent validity, 35 U.S.C. § 282). *See also* CVD, Inc. v. Raytheon Co., 769 F.2d 842, 850 (1st Cir. 1985) ("a patentee who has a good faith belief in the validity of a patent will not be exposed to antitrust damages even if the patent proves to be invalid, or the infringement action unsuccessful"), *cert. denied*, 475 U.S. 1016 (1986).

the use of the clear and convincing standard to "proceedings in which the alleged violation of the antitrust law consists solely of one or more infringement actions initiated in bad faith."[114] This case, however, involves allegations of deceptive conduct in the context of SSO activities; Rambus is not accused of initiating infringement actions in bad faith.

In short, the cases cited by Rambus do not support its assertion that the clear and convincing standard applies to the elements of this antitrust case because it happens to involve a patent. The Commission is not charged with deciding whether Rambus committed fraud on the PTO, or whether Rambus initiated its infringement actions in bad faith. The issue in the case before the Commission is whether Rambus, through its participation in JEDEC and in the context of JEDEC's standard-setting processes, engaged in a deceptive course of conduct under Section 5 of the FTC Act.[115] No court has held that clear and convincing evidence is required to establish Section 5 deception.[116] To the contrary, as previously stated, the Supreme Court held that Section 7(c) of the APA establishes "a standard of proof and that the standard adopted is the traditional preponderance-of-the evidence standard."[117]

2. Standard of Proof Should Be Commensurate With Proposed Remedy

Rambus's second argument – that a heightened standard of proof is necessary because Complaint Counsel seek to bar enforcement of Rambus's patents under certain circumstances – in effect would allow one potential remedy to determine the standard for establishing whether a violation of the antitrust laws occurred. The potential remedy should not influence the standard

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[114] *Id*. Other cases cited by Rambus arose in similar contexts. *See* Loctite Corp. v. Ultraseal, Ltd., 781 F.2d 861, 876-77 (Fed. Cir. 1985) (requiring a clear and convincing showing that a plaintiff brought a patent infringement suit in bad faith, knowing that there was no infringement), *overruled on other grounds*, Nobelpharma AB v. Implant Innovations, Inc. 141 F.3d 1059, 1068 (Fed. Cir. 1998); *CVD*, 769 F.2d at 849-51 (requiring an antitrust plaintiff to prove bad faith assertion of trade secrets – with knowledge that no trade secrets existed – by clear and convincing evidence).

[115] *See, e.g.*, Complaint ¶¶ 2, 122-24.

[116] *See generally* FTC v. Algoma Lumber Co., 291 U.S. 67, 78-81 (1934) (holding that proof of fraud is not required to prove Section 5 deception).

[117] *See* Steadman v. SEC, 450 U.S. 91, 95-102 (1981).

of proof for liability.[118] To the extent Rambus's arguments might be relevant to our consideration of particular remedies, we will address them in that context.

We note, however, that even a remedy barring enforcement of a patent does not necessarily require a heightened standard of proof. The equitable estoppel defense to patent infringement provides an example. A patentee's infringement claim may be barred if an alleged infringer establishes the elements of equitable estoppel (*i.e.*, misleading conduct, reliance, and material prejudice). The Federal Circuit has held that these elements ordinarily must be proven only by a preponderance of the evidence, noting that the clear and convincing standard applies to civil cases only when special circumstances are present.[119]

### 3. Chilling Participation in SSOs

We are unpersuaded by Rambus's third argument that a heightened burden of proof is necessary to avoid chilling procompetitive participation in standard-setting activities. This argument implicitly assumes that the usual burden of proof, if applied to antitrust claims involving SSOs, somehow will reduce incentives to engage in beneficial standard-setting activities. Rambus provides, and we find, no basis for that assumption.

Rambus's argument ignores the potentially serious chilling effect of deceptive conduct in the SSO context. The Complaint alleged that Rambus deliberately sought to acquire a monopoly by using a standard-setting process to engage in patent hold-up. That conduct, if established, might itself chill participation in cooperative standard-setting activities.[120] The success of

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[118] None of the cases cited by Rambus in its briefs support this contention. *See* CVD v. Raytheon Co., 769 F.2d 842 (1st Cir. 1985) (appeal to set aside jury verdict; no ruling that remedy sought should determine standard of proof); Livingstone v. North Belle Vernon Borough, 91 F.3d 515 (3d Cir. 1996) (action to determine voluntariness of an oral release-dismissal agreement that waived all civil claims in exchange for dismissal of criminal case; holding that "clear and convincing" evidentiary standard should apply in narrow context of evaluating voluntariness of oral release-dismissal agreements); Shepherd v. Am. Broad. Cos., Inc. , 62 F.3d 1469 (D.C. Cir. 1995) (appeal of judicial sanctions; "clear and convincing" evidentiary standard not used to determine merits of the case); Lindahl v. Office of Personnel Management, 470 U.S. 768 (1985) (addressed issue of whether a federal worker may appeal an agency's denial of disability retirement claim to the Federal Circuit; no ruling that "clear and convincing" evidentiary standard should apply to determine merits of federal worker's underlying claim).

[119] *See* A.C. Aukerman Co. v. R.L. Chaides Constr. Co., 960 F.2d 1020, 1045-46 (Fed. Cir. 1992) (because no "special considerations are implicated by the defense of equitable estoppel as we defined it, we adopt the preponderance of the evidence standard in connection with the proof of equitable estoppel factors, absent special circumstances, such as fraud or intentional misconduct"). The antitrust case before the Commission does not entail the types of circumstances that have supported the requirement of clear and convincing evidence in other cases.

[120] *See, e.g.*, CX 2384 (letter from G. Kelley of IBM regarding a member's failure to disclose patents to JEDEC, stating: "I am and have been concerned that this issue can destroy the work of JEDEC. If we have companies leading us into their patent collection plates, then we will no longer have companies willing to join the work of creating standards"); Appleton, Tr. 6331-32 (if a company enforced a patent after failing to disclose it to JEDEC, it would "very much affect whether Micron participated [in JEDEC] or not"); Rhoden, Tr. 535-38

cooperative standard setting depends on some assurance that other participants will not exploit the process by acting deceptively.[121] Requiring a heightened burden of proof when analyzing deception in the SSO context would diminish that assurance.

4. Reliance on Testimony Rather than Contemporaneous Written Evidence

Rambus's fourth argument – that clear and convincing evidence should be required because Complaint Counsel rely on "strained and faded memories"[122] – lacks both legal and factual support. Rambus has not identified a single judicial opinion to support its claim that delayed testimony triggers a heightened evidentiary standard, even though delayed testimony is hardly unusual in litigation. The absence of such opinions is unsurprising: the rule proffered by Rambus would reward defendants/respondents who engage in protracted deception and then foster pre-trial delays. In any event, Complaint Counsel in this case rely on contemporaneous documentary evidence in addition to the testimony of numerous witnesses. Many of Complaint Counsel's documentary exhibits are discussed throughout this Opinion.

* * * * *

In sum, Rambus failed to establish a basis for the Commission to impose a heightened "clear and convincing" evidentiary standard to determine liability in this case. Rather, Complaint Counsel have the burden to prove the necessary elements of liability by a preponderance of the evidence, in keeping with the normal rules applicable in FTC adjudications.[123]

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(Rambus's suits to enforce its patents relating to the JEDEC standards would cause "a fundamental shift away from open industry standardization"); Bechtelsheim, Tr. 5889 (if the "trust into the nature of an open standards process is violated, it makes it very difficult for me to rely on the standards groups developing standards").

[121] *Cf.* HERBERT HOVENKAMP ET AL., II IP AND ANTITRUST § 35.6 at 35-53 (Supp. 2003) (terming a standard-setting organization's desire "to make a fully informed decision on whether to adopt a particular standard" a "presumptively legitimate reason for requiring" disclosure of intellectual property).

[122] *See* RB at 140, RRB at 5.

[123] Although the ALJ rejected Rambus's proposed clear-and-convincing standard, he achieved much the same result by citing United States v. United States Gypsum Co., 333 U.S. 364 (1948), for the proposition that "where trial testimony is in conflict with contemporaneous documents, the trial testimony is entitled to little weight." *See* ID at 264-65. *Gypsum* actually was considerably more limited. After noting that "counsel were permitted to phrase their questions in extremely leading form, so that the import of the witnesses' testimony was conflicting" and that the testimony dealt with whether known conduct had involved actions taken in concert, the Court ruled, "Where such testimony is in conflict with contemporaneous documents, we can give it little weight, particularly when the crucial issues involve mixed questions of law and fact." 333 U.S. at 395-96. The ALJ ignores *Gypsum*'s limits and misapplies its rule. We find no inconsistency between the documents and testimony sufficient to invoke broad usage of the rule in *Gypsum*.

The ALJ found the *Gypsum* rule "especially appropriate here, where witnesses would directly benefit from the outcome of this litigation because they work for companies that either manufacture or use DRAMS that may

## IV. MONOPOLIZATION CLAIM[124]

Section 2 of the Sherman Act makes it unlawful to "monopolize, or attempt to monopolize, or combine or conspire with any other person or persons, to monopolize any part of the trade or commerce among the several States, or with foreign nations . . . ."[125] The Supreme Court has identified the basic elements of the offense:

> The offense of monopoly under § 2 of the Sherman Act has two elements: (1) the possession of monopoly power in the relevant market and (2) the willful acquisition or maintenance of that power as distinguished from growth or development as a consequence of a superior product, business acumen, or historic accident.[126]

The fundamental issues in this case are: (1) whether Rambus engaged in exclusionary conduct; (2) whether Rambus acquired monopoly power; and (3) whether there is a causal link between Rambus's conduct and its monopoly power. We consider each of these issues in turn.

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infringe Rambus's patents, work for entities that are entirely controlled by DRAM manufacturers, or are committed to developing technologies that will compete with Rambus's technologies." ID at 265. This standard would call into question the utility and reliability of trial procedures in virtually all antitrust cases. In antitrust litigation, witnesses inevitably are "interested," in the sense that they represent one economic actor or another. In this proceeding, *both* Rambus's and Complaint Counsel's witnesses have an interest in the outcome; depreciating their evidence on that basis indicts all live witness testimony. Economic interest gives us no basis to find that trial procedures – such as requiring a foundation for evidence and subjecting witnesses to cross-examination – are inadequate to compile a reliable record. Therefore, absent a specific reason to question the credibility or reliability of a specific witness or a specific statement, we find no basis to discredit any of the testimony in the record.

[124] Because we find that Rambus unlawfully monopolized the four relevant markets delineated by Complaint Counsel (and whose definition was not contested by Rambus), we need not consider the further allegations that Rambus attempted to monopolize those markets or that Rambus's conduct otherwise constituted an unfair method of competition.

[125] 15 U.S.C. § 2. The Commission's authority under Section 5 of the FTC Act reaches conduct that violates the Sherman Act. *See, e.g.*, FTC v. Cement Inst., 333 U.S. 683, 694-95 (1948); Fashion Originators' Guild of America v. FTC, 312 U.S. 457, 463 (1941); Polygram Holdings, Inc., 5 Trade Reg. Rep. (CCH) ¶ 15,453 at 22,452 n.11 (FTC 2003), *available at* http://www.ftc.gov/os/2003/07/polygramopinion.pdf (slip op. at 13 n.11), *enforcement ordered*, Polygram Holding, Inc. v. FTC, 416 F.3d 29 (D.C. Cir. 2005).

[126] United States v. Grinnell Corp., 384 U.S. 563, 570-71 (1966); *see also* Verizon Communs., Inc. v. Law Offices of Curtis V. Trinko, 540 U.S. 398, 407 (2004) (terming the *Grinnell* formulation "settled law").

## A. Exclusionary Conduct

### 1. Framework for Analysis

From the earliest days of Section 2 jurisprudence, courts have held that unilateral conduct, absent an "anticompetitive" or "exclusionary" element, is benign – even if it creates or maintains monopoly power, or is dangerously likely to do so – because "the successful competitor, having been urged to compete, must not be turned upon when he wins."[127] As the Supreme Court noted in *Spectrum Sports, Inc. v. McQuillan*,[128] "[t]he law directs itself not against conduct which is competitive, even severely so, but against conduct which unfairly tends to destroy competition itself."[129]

Exclusionary conduct is "conduct other than competition on the merits – or other than restraints reasonably 'necessary' to competition on the merits – that reasonably appear[s] capable of making a significant contribution to creating or maintaining monopoly power."[130] Stated differently, if "a firm has been attempting to exclude rivals on some basis other than efficiency," it is engaging in exclusionary conduct.[131] The focus, at all times, is on harm to competition, not merely harm to competitors.[132]

The exclusionary element alleged here is that Rambus engaged in a course of deceptive conduct.[133] Complaint Counsel assert that Rambus created the misimpression that it was not seeking relevant patents, thereby misleading JEDEC members regarding the price of Rambus's

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[127] United States v. Alcoa, 148 F.2d 416, 430-31 (2d Cir. 1945). *See also Verizon v. Trinko*, 540 U.S. at 407 ("To safeguard the incentive to innovate, the possession of monopoly power will not be found unlawful unless it is accompanied by an element of anticompetitive conduct.") (emphasis omitted).

[128] 506 U.S. 447 (1993).

[129] *Id.* at 458.

[130] III PHILLIP E. AREEDA & HERBERT HOVENKAMP, ANTITRUST LAW ¶ 651f, at 83-84 (2d ed. 2002). Several courts have relied on this definition. *See, e.g.*, Aspen Skiing Co. v. Aspen Highlands Skiing Corp., 472 U.S. 585, 605 n.32 (1985); Multistate Legal Studies, Inc. v. Harcourt Brace Jovanovich Legal & Prof'l Publ'ns, Inc., 63 F.3d 1540, 1550 (10th Cir. 1995), *cert. denied*, 516 U.S. 1044 (1996); Town of Concord v. Boston Edison Co., 915 F.2d 17, 21 (1st Cir. 1990), *cert. denied*, 499 U.S. 931 (1991).

[131] *See Aspen Skiing*, 472 U.S. at 605 ("If a firm has been 'attempting to exclude rivals on some basis other than efficiency,' it is fair to characterize its behavior as predatory") (footnote omitted), quoting ROBERT H. BORK, THE ANTITRUST PARADOX 138 (1978).

[132] *See, e.g.*,, Nynex Corp. v. Discon, Inc., 525 U.S. 128, 139 (1998) (requiring harm to "the competitive process"); *Town of Concord*, 915 F.2d at 21-22 (requiring harm to "the competitive process" such as by obstructing the achievement of lower prices, better products, or more efficient production methods); III AREEDA & HOVENKAMP, ANTITRUST LAW ¶ 651c, at 78-79.

[133] Complaint, ¶¶ 2, 122-24.

technology and thwarting their ability to make informed choices. This sort of deceptive conduct is not competition on the merits. Just as "false or misleading advertising has an anticompetitive effect,"[134] distorting choices through deception obscures the relative merits of alternatives and prevents the efficient selection of preferred technologies.[135]

The courts have established that deception may constitute "exclusionary conduct" that will support a Section 2 claim in appropriate circumstances.[136] In *United States v. Microsoft*, for example, the United States Court of Appeals for the District of Columbia Circuit found that Microsoft's deception with respect to Java applications was exclusionary.[137] As discussion of the legal and factual circumstances and the nature of Rambus's conduct makes clear, proof of the deceptive conduct alleged in this case would establish the exclusionary element required by Section 2.

We stand on familiar ground when we evaluate whether Rambus engaged in a deceptive course of conduct. Section 5 of the FTC Act proscribes, *inter alia*, deceptive acts and practices, and accordingly, the Commission has developed special expertise to determine whether conduct is deceptive.[138] Lest there be any doubt as to the elements of deceptive conduct under Section 5, those elements were spelled out in the Commission's 1983 Policy Statement on Deception (Policy Statement),[139] which the courts have treated as the definitive description of those elements under the FTC Act.[140]

According to the Policy Statement, for conduct to be found deceptive, there must have

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[134] Cal. Dental Ass'n v. FTC, 526 U.S. 756, 771 n.9 (1999).

[135] *Cf.* FTC v. Ind. Fed'n of Dentists, 476 U.S. 447, 461-62 (1986) (describing the anticompetitive consequences of "an effort to withhold (or make more costly) information desired by consumers for the purpose of determining whether a particular purchase is cost justified").

[136] *See* Conwood Co., LP v. U.S. Tobacco Co., 290 F.3d 768 (6th Cir. 2002) (maintaining monopoly power by, *inter alia*, providing misleading market data to retailers in order to distort their purchasing decisions violated Section 2); Caribbean Broad. Sys. Ltd. v. Cable & Wireless PLC, 148 F.3d 1080, 1087 (D.C. Cir. 1998); International Travel Arrangers, Inc. v. Western Airlines, 623 F.2d 1255, 1262-63, 1270 (8th Cir.), *cert. denied*, 449 U.S. 1063 (1980).

[137] *See* United States v. Microsoft Corp., 253 F.3d 34, 76-77 (D.C. Cir. 2001); s*ee also infra* Section IV.A.1.b. (discussing the *Microsoft* case).

[138] FTC v. Colgate-Palmolive Co., 380 U.S. 374, 391-92 (1965); Kraft, Inc. v. FTC, 970 F.2d 311 (7th Cir. 1992).

[139] Federal Trade Commission, *Policy Statement on Deception* (1983), *reprinted in* 4 Trade Reg. Rep. (CCH) ¶ 13,205 at 20,911-12 [hereinafter *Policy Statement*].

[140] Novartis Corp. v. FTC, 223 F.3d 783 (D.C. Cir. 2000); FTC v. Pantron I Corp., 33 F.3d 1088 (9th Cir. 1994), *cert. denied*, 514 U.S. 1083 (1995).

been a "misrepresentation, omission or practice" that was "material" in that it was likely to mislead "others acting reasonably under the circumstances" and thereby likely to affect their "conduct or decision[s]." Thus, in order to determine whether conduct (including a course of conduct) is deceptive, we must consider "the circumstances" in which the alleged "misrepresentation, omission or practice" occurred. We analyze the legal circumstances, factual circumstances, and nature of the conduct itself in assessing Rambus's conduct.

a. Legal Circumstances

Because this is a monopolization case, Rambus's allegedly deceptive conduct ultimately must be analyzed under Section 2 of the Sherman Act.[141] That requires two modifications to the analysis articulated by the Policy Statement. First, under the Policy Statement, the respondent's state of mind is irrelevant in determining whether the respondent engaged in deceptive conduct under Section 5. Under Section 2, however, the defendant must act "willfully" in acquiring or maintaining monopoly power. Thus, for Rambus's allegedly deceptive course of conduct to be actionable under the Sherman Act, Rambus must have acted "willfully," as opposed to inadvertently or even negligently.[142]

Second, the Policy Statement does not require proof of competitive harm for a respondent's conduct to be deemed deceptive under Section 5. However, under Section 2, in order to be condemned as "exclusionary," defendant's conduct must harm the competitive process, and that anticompetitive harm must outweigh the conduct's procompetitive benefits, if any.[143] Thus, for Rambus's alleged deceptive course of conduct to be actionable under Section 2, the conduct must have an anticompetitive effect that outweighs any procompetitive benefit.

Rambus argues that we should apply the "sacrifice test" as the framework for our analysis. That is, its conduct should be deemed exclusionary only if it would have been unprofitable to the defendant – if the defendant would have sacrificed profits – "but for" the expectation that the conduct would exclude rivals and permit the defendant to recoup its losses

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[141] Whatever the potential breadth of Section 5 of the FTC Act in these circumstances, our analysis in this opinion rests on the traditional criteria for evaluating allegations of monopolization under Section 2 of the Sherman Act.

[142] Some commentators have noted that the term "willful" often provides only limited guidance: "every firm 'willfully' maintains its profits or market share . . . ." III AREEDA & HOVENKAMP, ANTITRUST LAW, *supra* note 130, ¶ 651 at 76. They posit that courts often have "focused on conduct while talking about intent." *Id*. In the context of deceptive conduct, however, willfulness helps in determining "whether the challenged conduct is fairly characterized as 'exclusionary' or 'anticompetitive,'" Aspen Skiing, Co. v. Aspen Highlands Skiing Corp., 472 U.S 585, 602 (1985), by distinguishing intentionally deceptive conduct from conduct that, while misleading, is merely inadvertent or negligent.

[143] United States v. Microsoft Corp., 253 F.3d 34, 58-59 (D.C. Cir. 2001).

via the acquisition of long-run monopoly power.[144] Stated more generally, the so-called sacrifice test condemns conduct that would not make "economic sense" but for the elimination or lessening of competition.[145] Rambus contends that keeping information about its patent applications secret and refusing to share that information with competitors was beneficial to Rambus, regardless of what happened at JEDEC, and therefore could not be exclusionary.[146] The ALJ concurred.[147] We believe this was error both as a matter of law and as a matter of fact.

As a matter of law, we recognize that the sacrifice test may be well-suited to certain types of Section 2 claims where the risk of interfering with vigorous competitive activity is heightened,[148] but the test is not appropriate here. It misses conduct that reduces consumer welfare, but happens to be inexpensive to execute, and therefore does not involve a significant profit sacrifice. For example, defrauding the PTO in order to secure a patent that confers a monopoly demands little profit sacrifice, yet the Supreme Court has held that such fraud can violate Section 2.[149] Likewise, in this case, without reducing prices, forgoing sales, or even spending substantial funds beyond what it otherwise would have spent, Rambus's conduct may have imposed substantial costs on rivals and contributed significantly to the creation of monopoly power. In cases such as this, the *Microsoft* analysis – with its focus on determining "whether the monopolist's conduct on balance harms competition"[150] – is the proper lens for scrutinizing allegedly exclusionary conduct.[151]

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[144] RB at 110-12.

[145] *See* A. Douglas Melamed, *Exclusive Dealing Arrangements and Other Exclusionary Conduct – Are There Unifying Principles?*, 73 ANTITRUST L.J. 375, 389-403 (2006) (stating views of counsel for Rambus in this proceeding).

[146] RB at 113-15.

[147] *See* ID at 286-87, 289, 292.

[148] Some court decisions have employed the test's underlying concept in the context of predatory pricing. *See, e.g.*, Matsushita Elec. Indus. Co. v. Zenith Radio Corp., 475 U.S. 574, 588-89 (1986) (explaining that pricing below competitive levels entails forgoing profits and that, to make this rational, there must be a reasonable expectation of later recoupment through monopoly profits); Concord Boat Corp. v. Brunswick Corp., 207 F.3d 1039, 1062 ( Cir. 2000); Conoco Inc. v. Inman Oil Co., 774 F.2d 895. 905-06 (8th Cir. 1985). Other court decisions have applied similar thinking to unilateral refusals to deal with rivals. *See, e.g.*, Morris Communications v. PGA Tour, 364 F.3d 1288, 1295 (11th Cir.), *cert. denied*, 125 S.Ct. 87 (2004); *cf.* Verizon Communs., Inc. v. Law Offices of Curtis V. Trinko, 540 U.S. 398, 409 (2004) (explaining that in the *Aspen Skiing* refusal-to-deal case, "[t]he unilateral termination of a voluntary (*and thus presumably profitable*) course of dealing suggested a willingness to forsake short-term profits to achieve an anticompetitive end") (emphasis original).

[149] *See* Walker Process Equipment, Inc. v. Food Mach. & Chem. Corp., 382 U.S. 172 (1965).

[150] *Microsoft*, 253 F.3d at 58-59.

[151] *See* Caribbean Broad. Sys. Ltd. v. Cable & Wireless PLC, 148 F.3d 1080, 1087 (D.C. Cir. 1998) (noting that anticompetitive conduct takes "many different forms" and is highly "dependent on context"). Although

b. Factual Circumstances

The factual context in which the alleged conduct occurred is critical. For example, in *Microsoft*, the D.C. Circuit concluded that Microsoft violated Section 2 by making misleading statements to Independent Software Vendors (ISVs) in a context in which the ISVs reasonably could have expected that Microsoft would *not* mislead them. Specifically, Microsoft publicly committed to cooperate with Sun Microsystems (Sun), and also offered ISVs a set of "Java implementation tools" that ostensibly would enable them to develop cross-platform applications.[152] Thus, there was a reasonable expectation that the relationship between Microsoft and Sun and, more importantly, between Microsoft and the ISVs, would be characterized by cooperation, not deception. The record showed, however, that Microsoft sought to use unwitting ISVs to generate Windows-dependent applications that were incompatible with other platforms. To that end, Microsoft surreptitiously included in its implementation tools certain key words or directives that could be executed solely by Microsoft's version of the Java runtime environment for Windows.[153] In light of the expectations of a cooperative relationship, Microsoft's deceptive conduct was opaque. Consequently, countermeasures were hard, if not impossible, to implement, and there was a substantial threat of competitive harm.

In contrast, deceptive conduct in competitive environments is less likely to be actionable under Section 2, because misrepresentations, deceptive practices, or omissions in the context of competitive relationships are less likely to be material. For example, we agree with the reasoning in two recent appellate cases finding that misleading statements in the advertising contexts there at issue were not grist for Section 2 claims.[154] Those decisions make sense in the "rough and tumble" of the competitive marketplace because the allegedly misleading hyperbole was transparent to rivals, who generally could protect themselves by engaging in their own counter-

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Rambus highlights FTC/DOJ support for the sacrifice test in various briefs, the agencies have made it clear that exclusionary conduct "need not always entail economic sacrifice." Brief of Amici Curiae United States & Federal Trade Commission on Writ of Certiorari at 11 n.2 (Dec. 2002), Verizon v. Trinko, 540 U.S. 398 (No. 02-682). Indeed, the agencies suggested a standard that would condemn conduct with harm to competition "disproportionate" to its benefits – along the lines of *Microsoft's* balancing test – for purposes of assessing opportunistic behavior in the standard-setting process. Brief of Amici Curiae United States & Federal Trade Commission at 14-15 (May 2003), *Trinko* (No. 02-682). The agencies urged reserving the "sharper focus" provided by the sacrifice test for situations such as the refusal-to-aid-rivals claim presented in *Trinko*, for which antitrust interference was thought likely to offer "infrequent pro-competitive benefits" and "frequent anticompetitive risks." *Id*. at 15, 17.

[152] 253 F. 3d at 76.

[153] *Id*.

[154] *See* Am. Council of Certified Podiatric Physicians & Surgeons v. Am. Bd. of Podiatric Surgery, 323 F.3d 366, 370-72 (6th Cir. 2003) (applying a rebuttable presumption that effect on competition of misleading advertising material was *de minimis*); Am. Prof'l Testing Services v. Harcourt Brace Jovanovich Legal & Prof'l Publ'ns, Inc., 108 F.3d 1147, 1152 (9th Cir. 1997) (same).

advertising. Therefore, there was a relatively low risk that significant anticompetitive effects would occur in that context.

Unlike those advertising cases, the very different circumstances presented here suggest that deceptive conduct could have caused lasting competitive harm by obscuring crucial information, known only to one industry member, until it was too late to counteract the consequences. In this context, we cannot stress too strongly the importance we place on the fact that the challenged conduct occurred in the context of a standard-setting process in which members expected each other to act cooperatively. We recognize that standard setting of the type sponsored by JEDEC potentially yields significant efficiencies[155] – especially when the standards facilitate interoperability among various components, to the likely benefit of industry participants as well as consumers.[156] Although standard setting displaces the normal process of selection through market-based competition – by which, without any agreement, the purchasing decisions of customers determine which interoperable combinations of products and technologies ultimately will survive – the efficiency benefits of consensus standard setting easily can outweigh that loss of competition.

Even under the best of circumstances, however, the standard-setting process has a unique potential to skew the competitive process by aligning supply and demand in a prescribed direction.[157] The risk of competitive harm is heightened in the face of exclusionary conduct that does not constitute competition on the basis of efficiency and that interferes with the cooperative nature of the standard-setting process. Exclusionary conduct such as deception may distort the selection of technologies and evade protections designed by SSOs to constrain the exercise of monopoly power, with substantial and lasting harm to competition.[158] Additionally, unlike misleading statements made in advertising – which can be corrected quickly by a competitor's counter-advertising – there are fewer "quick fixes" available to correct the competitive harm caused by deception in the SSO context, once a standard has been chosen and the industry has become locked in. If exclusionary conduct reduces or destroys the efficiencies to be gained through consensus standard setting, it may cause considerable harm to competition. If the anticompetitive harm exceeds any remaining efficiencies, standard setting is no longer beneficial on balance.

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[155] *See* Moore v. Boating Indus. Ass'n, 819 F. 2d 693, 695 (7th Cir. 1987); *cf.* United States Dep't of Justice and Federal Trade Comm'n, Antitrust Guidelines for Collaborations Among Competitors (2000) *reprinted in* 4 Trade Reg Rep. (CCH) ¶ 13,160, *available at* http://www.ftc.gov/os/2000/04/ftcdojguidelines.pdf.

[156] *See, e.g.*, Williams, Tr. 763; Calvin, Tr. 994; Polzin, Tr. 3972.

[157] *See* Standard Sanitary Mfg. Co. v. United States, 226 U.S. 20, 41 (1912); FTC Bureau of Consumer Protection, Standards and Certification Final Staff Report, at 28, 34 (April 1983); Michael Katz & Carl Shapiro, *Systems Competition and Network Effects*, 8 J. ECON. PERSPECTIVES 93, 105-06 (1994); Richard Gilbert, *Symposium on Compatibility: Incentives and Market Structure*, 40 J. INDUS. ECON. 1 (1992).

[158] *See infra* Sections IV.C.1, IV.C.2, and IV.C.3.c., d.

Consequently, courts have scrutinized conduct related to standard setting.[159] For example, the Supreme Court has condemned efforts to bias the standard-setting process by "stacking" the decision making body with voters interested in excluding a competing product.[160] The Court also has recognized that the power to distort the interpretation of standards is the "power to frustrate competition in the marketplace."[161] Likewise, prior Commission enforcement efforts have targeted distortions of standard-setting processes that have led to the creation of market power.[162]

Antitrust scrutiny of possibly deceptive conduct in the standard-setting context is especially warranted when the standard-setting body has determined to carry out its work in an environment ostensibly characterized by cooperation, rather than rivalry – in other words, when the circumstances closely resemble those in *Microsoft* (as distinguished from the competitive environment in the Section 2 advertising cases mentioned above). In a consensus-oriented context, participants in the standard-setting process are likely to be less wary of deception; they are less likely to detect and take countermeasures to counteract it, and anticompetitive effects therefore are more likely to result. The magnitude of potential anticompetitive consequences may also be as substantial as it was in *Microsoft*, given the potential for a standard to create market or monopoly power.[163]

We do not hold, and our decision should not be read to mandate, that all SSOs should require disclosure of relevant intellectual property. An SSO may choose not to require such disclosures. If, however, an SSO does require such disclosures, then non-disclosure – followed by adoption of a standard incorporating the intellectual property, and royalty demands against

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[159] *See* Allied Tube & Conduit Corp. v. Indian Head, Inc., 486 U.S. 492, 500 (1988) ("Agreement on a product standard, is after all, implicitly an agreement not to manufacture, distribute, or purchase certain types of products. Accordingly, private standard setting associations have traditionally been objects of antitrust scrutiny."); Am. Soc'y of Mech. Engineers, Inc. v. Hydrolevel Corp., 456 U.S. 556, 571 (1982).

[160] *See Allied Tube*, 486 U.S. at 508 ("petitioner was at least partially motivated by the desire to lessen competition and . . . stood to reap substantial economic benefits from making it difficult for respondent to compete"), 511.

[161] *See Am. Soc'y of Mech. Engineers*, 456 U.S. at 571.

[162] *See* Union Oil Co., Dkt. No. 9305, Decision & Order, ___ F.T.C. ___, 2005 WL 2003365 (2005), *available at* http://www.ftc.gov/os/adjpro/d9305/050802do.pdf (consent order resolving allegations that Unocal illegally had acquired monopoly power by misrepresenting to a state standard-setting board that certain research was non-proprietary while pursuing patent claims that would have enabled Unocal to charge royalties for low-emission gasoline compliant with the standard); Dell Computer Corp., 121 F.T.C. 616 (1996) (consent order resolving allegations that, after certifying that it had no relevant patents, Dell sought to enforce patents adopted by a standard-setting organization).

[163] *See* HOVENKAMP ET AL., II IP AND ANTITRUST, *supra* note 121, at § 35.5b at 35-43 (Supp. 2006) ("the competitive risk is that the misrepresentation [defined to include omissions] will cause a standard-setting organization to adopt a standard it otherwise would have rejected, and that the adoption of that standard will in turn confer on the defendant market power it would not otherwise have obtained.").

those practicing the standard – may be considered a material omission and may constitute deceptive conduct under Section 5. If an SSO chooses not to require such disclosures, SSO members still are not free to lie or to make affirmatively misleading representations. In either case, whether the SSO requires disclosure should be judged not only by the letter of its rules, but also on how the rules are interpreted by its members, as evidenced by their behavior as well as by their statements of what they understand the rules to be.

c. Nature of the Conduct

In order to assess fully the circumstances under which the alleged deception occurred, we also must understand the nature of the allegedly deceptive course of conduct, which combined the acquisition and exploitation of patents with a cooperative standard-setting process. A patent holder's market power may be materially enhanced once the patented technology is incorporated into a standard, as alternatives become less attractive relative to the chosen technology and less able to constrain its price.[164] For this reason, Rambus's alleged course of conduct, if established, could be especially pernicious to the competitive process.

An SSO may elect to require disclosure of patent positions before standardization decisions are made, because this enables SSO participants to make their choices with more complete knowledge of the consequences – including the potential that those practicing the standard may be liable for patent infringement, unless they negotiate licenses and pay royalties. If the SSO members prefer a given technology, notwithstanding the prospect of royalties, they can vote to incorporate it into the standard. If, in light of likely royalty payments, members prefer an alternative technology, they can vote against inclusion of the patented technology.

Disclosure of potential patent liability also helps avoid the possibility of hold-up by enabling SSO participants to seek protection from excessive royalties "*ex ante*" – *i.e.*, before choosing which technologies to incorporate into the standard. For example, an SSO member expecting to sell products that conform to the standard, who gains knowledge of potential patent exposure, may have powerful economic incentives to negotiate a license *before* the technology becomes standardized, based on the lower, *ex ante* value of the patented technology.[165] Similarly,

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[164] *See* Dell Computer Corp., 121 F.T.C. 616, 624 (1996) (Statement of the Federal Trade Commission); McAfee, Tr. 7494-95.

[165] Complaint Counsel's economic expert sets out the basis for this reasoning in greater detail. *See* McAfee, Tr. 7260-75. 7294-7308; *see also* Brief Amicus Curiae of Economics Professors and Scholars at 6-7 (presenting the views of six university economists). Rambus's economic expert, Richard Rapp, has acknowledged that "[s]tandard setting has the potential to create market power and enhance the market value of a technology by reducing the number of close substitutes." Richard T. Rapp & Lauren J. Stiroh, Testimony at FTC/DOJ Hearings Regarding Competition and Intellectual Property Law and Policy in the Knowledge-Based Economy, at 2 (Apr. 18, 2002), *available at* http://www.ftc.gov/opp/intellect/020418rappstiroh.pdf. Rapp continued, "In the absence of knowledge about proprietary IP rights in the technologies under consideration, manufacturers may find themselves the victims of opportunism after the standard has been set." *Id*. at 5. (Rapp's testimony identified a number of conditions that he argued must be met for anticompetitive harm to occur. We quote his statements for their

the owner of the patented technology may prefer to offer an *ex ante* license – even at a lower *ex ante* rate – knowing that the other SSO participants otherwise might engage in a cost/benefit analysis and opt to standardize an entirely different technology. Indeed, under certain circumstances, members of an SSO may even collectively negotiate these types of *ex ante* licenses, without necessarily running afoul of the antitrust laws.[166]

In sum, standard setting can function as an efficient substitute for selecting interoperable technologies through direct competition. Rambus's course of conduct allegedly impaired these processes within JEDEC. Complaint Counsel argue that Rambus deprived other JEDEC members of information needed to make an efficient selection of the "best" technologies for SDRAM standards, based on an analysis of likely costs as well as benefits. Rambus's conduct also purportedly prevented other JEDEC members from avoiding exposure to monopoly pricing by securing commitments regarding future royalty rates at a time when alternative technologies still offered unblunted competition. Under the Policy Statement, these circumstances are relevant to our analysis of whether Rambus's course of conduct constituted deception in violation of Section 5 of the FTC Act. Under Section 2 case law, these circumstances suggest exclusionary conduct: deceptive behavior that hides the price of a patented technology is not "competition on the merits,"[167] and deception that thwarts informed choice is not competition on the "basis [of] efficiency."[168]

### 2. Rambus's Course of Conduct

Applying the analytical framework to the facts of this case, we first consider whether Rambus engaged in a course of conduct in its JEDEC activities that included potentially deceptive conduct – *i.e.*, "misrepresentations, omissions, or practices."[169] There is little room for

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agreement with Complaint Counsel's general theory, not as representative of any concession that anticompetitive conduct occurred in this case.)

[166] *See* Chairman Deborah Platt Majoras, Recognizing the Procompetitive Potential of Royalty Discussions in Standard Setting, Remarks Before Standardization and the Law: Developing the Golden Mean for Global Trade (Stanford, Cal., Sept. 23, 2005), *available at* http://www.ftc.gov/speeches/majoras/050923stanford.pdf.

[167] *See, e.g.*, Aspen Skiing Co. v. Aspen Highlands Skiing Corp., 472 U.S. 585, 605 n.32 (1985); Multistate Legal Studies, Inc., v. Harcourt Brace Jovanovich Legal & Prof'l Publ'ns, Inc., 63 F.3d 1540, 1550 (10th Cir. 1995), *cert. denied*, 516 U.S. 1044 (1996); Town of Concord v. Boston Edison Co., 915 F.2d 17, 21 (1st Cir. 1990), *cert. denied*, 499 U.S. 931 (1991).

[168] *See Aspen Skiing*, 472 U.S. at 605 ("If a firm has been 'attempting to exclude rivals on some basis other than efficiency,' it is fair to characterize its behavior as predatory") (footnote omitted), quoting ROBERT H. BORK, THE ANTITRUST PARADOX 138 (1978).

[169] *Policy Statement, supra* note 139, at 20,911-12.

dispute about what Rambus did, because much of the evidence in the record regarding Rambus's conduct came from Rambus's own documents and witnesses.[170]

Based on that evidence, we find that Rambus concealed the patent applications it filed, and the patents it obtained, until JEDEC had adopted its SDRAM and DDR SDRAM standards. Once those standards were adopted, Rambus abused their adoption by suing firms that practiced the standards for patent infringement. Rambus also used information derived from JEDEC meetings to develop a patent portfolio that would cover JEDEC's SDRAM standards – a practice which, although it may not be clearly "deceptive" standing alone, nonetheless facilitates hold-up in a cooperative standard-setting context.

The record reveals the following chronology of events.

### a. The Chronology of Concealment

***1991.*** JEDEC was in the early stages of work on the SDRAM standard[171] when Rambus attended its first JEDEC meeting and joined JEDEC in December 1991.[172] Within a few days of that JEDEC meeting, Rambus's Executive Vice President (EVP), Allen Roberts, called Lester Vincent, Rambus's outside patent counsel, to speak with him about "patent deadlines"; Roberts also informed staff that a Rambus goal for the first quarter of 1992 was "patent filing."[173]

***1992.*** Rambus engineer William Garrett represented Rambus at its first JEDEC meeting as a member in February 1992. Following the meeting, Garrett reported to his supervisors that SDRAMs were inevitable and that SDRAM could be standardized sooner than expected.[174] Shortly afterwards, on March 5, 1992, Rambus responded to the PTO's restriction requirement[175]

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[170] Of course, documents destroyed by Rambus might have provided additional details regarding Rambus's activities. *See infra* Section V.

[171] Fully synchronous DRAM initially was proposed to JEDEC in May 1991. IDF 297. Rambus's patented versions of two of the relevant technologies are included in the SDRAM standard: programmable CAS latency and programmable burst length. Rambus's patented versions of the other two relevant technologies – dual-edge clocking and on-chip PLL/DLL – were included in the next generation of SDRAM, called DDR-SDRAM. All of these technologies were considered for inclusion into the SDRAM standard.

[172] CX 602 at 1-3. Rambus already had met with a number of DRAM manufacturers in an effort to convince them to license RDRAM. *See supra* Section II.A.

[173] CX 1705 at 34.

[174] CX 672 at 1 ("SDRAMs will happen.").

[175] *See supra* note 19 and accompanying text.

by filing ten divisional applications, all claiming priority based on the 1990 filing date of the original '898 application.[176]

On March 25, 1992, EVP Roberts and outside counsel Vincent discussed the steps Rambus would need to take to be in a position to accuse manufacturers of JEDEC-compliant SDRAM of infringement.[177] Two days later, Roberts and Richard Crisp (an engineer who served as Rambus's primary JEDEC representative from May 1992 until Rambus withdrew from JEDEC membership)[178] met with Vincent again to discuss Rambus's patent position as a member of JEDEC. Vincent advised both Roberts and Crisp that "there could be [an] equitable estoppel problem if Rambus creates an impression on JEDEC that it would not enforce its patent or patent appln [application]," but that the case would be "less clear cut if Rambus is merely silent."[179]

Early in April 1992, Crisp requested and received from Vincent abstracts of Rambus's current patent applications.[180] In April 1992, Crisp attended a JEDEC task group meeting that focused on SDRAMs. Reporting back to Rambus executives on the meeting's events, Crisp discussed the technologies under consideration, stressed the JEDEC members's concern with price, and concluded that "the group is pretty set on using the SDRAMs."[181]

On May 2, 1992, Roberts met with Vincent to discuss claims that Crisp wanted to add to Rambus's patent applications, including a claim covering programmable latency and, if needed, a claim involving programmable burst length – two technologies eventually incorporated into the SDRAM standard.[182] After attending a JEDEC meeting later that month, Crisp spoke with

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[176] The patents that Rambus has asserted against SDRAM and DDR SDRAM manufacturers each derive from continuations of the '898 application or from continuations of one of these divisional applications. *See supra* Section II.A; IDF 171; Nusbaum, Tr. 1511-12.

[177] According to Vincent's notes, Roberts told Vincent with regard to JEDEC that Rambus "need[s] preplanning before accus[ing] others of infringement." CX 1941 at 1.

[178] Crisp, Tr. 2929.

[179] CX 1942. Equitable estoppel is a defense against infringement under patent law. It generally means that, if a patent holder's actions justify a belief that he has no intent to enforce the patent, then he is prevented (*i.e.*, equitably estopped) from enforcing the patent at a later date. *See, e.g.*, Stambler v. Diebold, 11 U.S.P.Q.2D (BNA) 1709 (E.D.N.Y. 1988). Vincent also advised that Rambus would be better able to defend against an equitable estoppel claim if Rambus abstained from voting at JEDEC. CX 1942.

[180] CX 1945 at 1; Crisp, Tr. 3050.

[181] CX 1708.

[182] CX 1946; Crisp, Tr. 3057-58. Vincent's notes state "Add claims to mode register to control latency output timing depending upon clock – specify clock cycle" and "check whether original application has block s . . (?)." The latter is a reference to programmable burst length. *See* Horowitz, Tr. 8661-62 (stating that he uses "variable block size" and "variable burst length" interchangeably); Geilhufe, Tr. 9642-43 ("variable block size" and "programmable burst length" are "[d]ifferent terms describing the exact same function"). Crisp was unable "at

Vincent to discuss adding claims to the divisional applications.[183] In that same month, Rambus CEO Tate called a meeting with Rambus executives, including Crisp and Roberts, to discuss: (1) how JEDEC SDRAMs might infringe Rambus's patents ("What patents do synchronous DRAMs violate of ours?"); (2) how Rambus might add claims to cover JEDEC standards ("What extensions should we be filing to add claims based on original inventions?"); and (3) the nature of Rambus's disclosure duties to JEDEC ("What obligation do we have to advise JEDEC that we have filed but unissued patents that sync do/may infringe?").[184]

In June and July 1992, members of the JC 42.3 subcommittee, including Rambus, voted on whether the SDRAM standard should include a programmable mode register to set CAS latency and burst length.[185] The ballot asked the representative of each voting member whether he or she was aware of any relevant patents.[186] The ballot also asked members voting against the proposal to explain their reasons and asked specifically about any patent issues. IBM, which voted against the proposal, noted that "patent issues need to be cleaned up before we proceed."[187] Rambus omitted to disclose the existence of any pending or issued patents,[188] even though Rambus was working on claims relating to the mode register, programmable latency, and burst length at the time.[189] Rambus voted against the proposal, citing technical reasons (*e.g.*, an inadequate number of power pins).[190]

One week after the June 1992 ballot was circulated, Rambus CEO Tate forwarded to the firm's executives a "specific" business plan that outlined a patent strategy regarding SDRAMs:

> [W]e believe that Sync DRAMs [SDRAMs] infringe on some claims in our filed patents, and that there are additional claims we can file for our patents that cover features of Sync DRAMs. Then we will be in position to request patent licensing (fees and royalties) from any manufacturer of Sync DRAMs. Our action plan is to

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this point in time" (*i.e.*, at trial) to remember what the reference – misread to him by trial counsel as "blocks" – dealt with, but he acknowledged that he was "unsure whether we had claims in that area" and that he had "suggested to Mr. Roberts that if we didn't, we should have some claims in those areas, including blocks." Crisp, Tr. 3059.

[183] CX 34 at 1, 59; CX 1947.

[184] *See* CX 5101 (Tate e-mail, asking questions under the heading "JEDEC").

[185] CX 252a.

[186] *Id*. at 2.

[187] JX 13 at 9.

[188] *Id*.

[189] *See* CX 1946; CX 1947.

[190] Crisp, Tr. 3080; JX 13 at 9.

determine the exact claims and file the additional claims by the end of Q3/92. Then to advise Sync DRAM manufacturers in Q4/1992.[191]

In August 1992, Rambus specifically assigned JEDEC representative Crisp responsibility for overseeing development of amended patent claims to "provide better coverage" against SDRAMs.[192] Crisp followed up with outside counsel Vincent regarding the status of the planned amendments.[193] In September 1992, Crisp requested that Vincent file an amendment adding claims relating to "DRAM - multiple open row addresses" and "DRAM - programmable latency via control reg" to Rambus's pending applications.[194] Crisp requested these additional claims to "cause problems with synch DRAM."[195] Crisp agreed to provide Vincent with a copy of the "synch DRAM spec."[196] Crisp and Vincent also discussed adding claims relating to on-chip PLLs on DRAMs, in response to a formal presentation at JEDEC.[197] In November 1992, Crisp met with Vincent to follow up on claim amendments and received copies of Rambus's pending patent applications.[198] A December 1992 Rambus planning document noted intentions to "get a copy of the SDRAM spec and check it for features we need to cover as well as features which violate our patents."[199]

***1993.*** In January 1993, Rambus CEO Tate scheduled an "Objectives meeting" to discuss, among other things, "patents – vs. SDRAM."[200] In February 1993, per Crisp's instructions, Rambus worked on adding claims relating to programmable latency and on-chip PLL/DLL.[201]

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[191] CX 543a at 14-17 (Rambus 1992-97 Business Plan, devoting a majority of discussion of competition to SDRAM).

[192] *See* CX 5104 at 1 (Rambus CEO Tate's "Notes from 8/26 Strategy Meeting" stating, "Richard [Crisp] will work to add modifications to our patents to provide better coverage, if possible, for Masters and against Ramlink/Sync DRAMs.").

[193] *See* Crisp, Tr. 3087-88; CX 1930 at 42.

[194] Crisp, Tr. 3097, 3099-3100; CX 1949.

[195] CX 1949 at 1.

[196] *Id*. at 4.

[197] *Id*. at 1, 5-7.

[198] CX 682; CX 1930 at 59; CX 1951 at 1.

[199] CX 1821 at 24.

[200] CX 5106.

[201] CX 686; Crisp, Tr. 3121-22 (explaining that Crisp provided Rambus engineer Fred Ware with a list of possible claim amendments including "DRAM with programmable access latency . . . [and] DRAM using PLL/DLL

The following month, the JC 42.3 subcommittee voted to send its proposed SDRAM standard, which included programmable CAS latency and burst length, to the JEDEC Council for approval.[202]

On May 17, 1993, while the proposed SDRAM standard was awaiting final approval by the JEDEC Council, Rambus filed a preliminary amendment to another of its divisional applications.[203] Rambus engineer Fred Ware shortly afterwards described the amendment, which involved programmable CAS latency, as "directed against SDRAMs."[204] Crisp agreed.[205]

One week after Rambus filed its amendment, on May 24, 1993, the JEDEC Council formally adopted the SDRAM standard.[206] The SDRAM standard incorporated programmable CAS latency and programmable burst length, two of the technologies that Rambus claims are covered by its patents.[207]

After the SDRAM standard was adopted, the JC 42.3 subcommittee turned to work on the next generation of SDRAM, which became DDR SDRAM.[208] At the same time, Rambus continued to amend its patent applications to cover JEDEC-compliant products. In June 1993, Rambus engineers worked with Vincent to amend Rambus's patent applications with claims specifically directed against SDRAMs or future SDRAMs.[209] On June 18, 1993, an e-mail from Ware to Crisp and others noted that a claim for "DRAM with PLL clock generation" that was "directed against future DRAMs" was "partially written up" and needed to be finished and

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circuit to reduce input buffer skews"). Crisp and Vincent continued to communicate regarding patent application amendments during the following months. *See* CX 1930 at 83; CX 1957.

[202] IDF 351; JX 15 at 14.

[203] CX 1456 at 198-210 (amending Patent Application No. 07/847,651).

[204] CX 1959 (June 18, 1993 Ware e-mail); Crisp Tr. 3153-56. Years later, in preparation for Micron's litigation against Rambus, Ware examined the preliminary amendment and concluded that the scope of the claims was not as broad as he originally had thought. CX 2103 (Ware *Micron* Dep.) at 100 (*in camera*).

[205] CX 703.

[206] IDF 354-356.

[207] IDF 355; JX 56 at 114.

[208] *See, e.g.*, Rhoden, Tr. 460-63, 1200; Williams, Tr. 820; Sussman, Tr. 1402, 1429; G. Kelley, Tr. 2567, 2585-87.

[209] S*ee* CX 1959.

filed.[210] Crisp responded that this "sounds really good [and] matches what I have requested and what I believe has happened."[211]

***1994.*** Rambus executives continued to correspond and meet with Vincent in early 1994 to "talk about patent strategies."[212] In March 1994 Rambus President David Mooring called for an "IP maximization strategy" to be put in place by the next quarter.[213]

Throughout 1994, Rambus continued to work on amending its applications, focusing on SDRAMs or future SDRAMs such as DDR. In May of that year, Roberts requested that Vincent consider ways to add or strengthen claims covering programmable CAS latency and dual-edged clocking, which subsequently became features of DDR SDRAM.[214] Rambus CEO Tate monitored the progress of Rambus's patent activity and asked for progress reports, particularly regarding the claims "that read directly on current/planned sdrams."[215]

In September 1994, JEDEC participants made formal presentations relating to on-chip PLL/DLL technology for later-generation SDRAM (which became known as DDR SDRAM).[216] Although Crisp knew that Rambus had been pursuing patent claims covering on-chip PLL, he omitted to disclose any patents or patent applications at this meeting.[217] His report to Rambus management on the meeting stated, "Obviously we need to think about our position on this for potential discussion with NEC regarding patent issues here."[218] Crisp e-mailed Roberts that he thought Rambus eventually would bring infringement actions in areas such as "PLL on a DRAM

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[210] CX 1959. *Compare* Nusbaum, Tr. 1584 *with* Fliesler Tr. 8867 (disagreeing as to whether claims filed on June 28, 1993 actually covered a subsequent PLL proposal).

[211] CX 703.

[212] CX 718 (e-mail dated January 5, 1994, setting up meeting with Vincent for January 12, 1994).

[213] CX 726 (e-mail dated March 15, 1994). Mooring's e-mail also proposed that Rambus "kick-off another patenting spree focused on the controller side of things" to take advantage of "a window of opportunity left while we still have confidential information . . . ." *Id*.

[214] CX 734.

[215] CX 740 (June 1994 e-mail from Tate to Roberts requesting "a list of which claims we are making that read directly on current/planned sdrams and on what most might be, so i can track progress from lester's [Vincent's] periodic status lists").

[216] At the JC 42.3 meeting on September 13-14, 1994, NEC made a presentation that proposed "putting a PLL on board their SDRAMs to improve the output delay." CX 711 at 36. This presentation led Crisp to conclude that "others are seriously planning inclusion of PLLs on board SDRAMs." *Id*. at 37.

[217] Crisp, Tr. 3316.

[218] CX 711 at 36.

. . . programmable access latencies and host of other areas."[219] In that same month, September 1994, Rambus amended its 08/222,646 application (the '646 application) to add claim 151, relating to dual-edged clocking.[220]

***1995.*** In April 1995, Rambus CEO Tate reiterated objectives of "get[ting] royalties from competitive memory" that used just one or a few of Rambus's technologies; called for verification that "all ideas we have requested to be filed as general patents re [SDRAM] have been [filed]"; and directed that Rambus "hold on patent issuances till then."[221] In May 1995, Crisp recommended that Rambus continue to keep its patent position secret, explaining that "it makes no sense to alert them [JEDEC] to a potential problem they can easily work around."[222] Through the summer, Crisp participated in work "on enhancing claim coverage."[223] In October 1995, Rambus amended one of its patent applications to insert claims relating to on-chip PLL/DLL technology.[224] One week after filing these amendments, Rambus received a JC 42.3 survey ballot on "Future Synchronous DRAM Features." The ballot asked whether members believed that "on chip PLL or DLL is important to reduce the access time from the clock for future generations of SDRAMs," and whether "future generations of SDRAMs could benefit from using BOTH edges of the clock for sampling inputs."[225] Rambus did not vote, and it failed to disclose the existence of any application that related to either on-chip PLL/DLL or dual-edge clocking.[226] At the meeting at which the ballot results were discussed, JEDEC member MOSAID disclosed that it had applied for a patent applicable to PLLs/DLLs; Crisp acknowledged that

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[219] CX 757 at 1. A few weeks later, another Crisp e-mail to Rambus executives described on-chip PLL as "one of our key technology patents" and emphasized, "If it is allowed, we need to be able to collect on it." CX 763. *See also* CX 766 (October 1994 Crisp e-mail suggesting a strategy for encouraging "the SDRAM boys" to make use of on-chip PLLs so that Rambus could then sue them for infringement).

[220] CX 1493 at 183-85. *Compare* Nusbaum, Tr. 1597-98 *with* Fliesler, Tr. 8858 (both observing that claim 151 involved receiving data in response to both the rising and falling edges of a clock signal but disagreeing as to further implications). Roberts previously had circulated to Rambus executives drafts of the claim amendments, which Roberts described as "[Lester Vincent's] attempt to work the claims for the MOST/SDRAM defense." CX 746 at 1.

[221] CX 5110 at 2-3.

[222] CX 711 at 73.

[223] CX 5112.

[224] IDF 963; CX 1502 at 233-39.

[225] CX 260 at 12 (emphasis original); JX 28 at 45.

[226] Crisp, Tr. 3341; JX 28 at 45 (listing firms that provided responses).

"even after seeing this disclosure of a patent application," he "did not say anything with respect to any Rambus patent application concerning PLLs or DLLs."[227]

Crisp advised management in September 1995 that Rambus should "redouble [its] efforts to get the necessary amendments completed, the new claims added and make damn sure this ship is watertight before we get too far out to sea."[228] In fall 1995, Rambus's new in-house counsel, Anthony Diepenbrock, outlined Rambus's patent strategy at a company-wide retreat.[229] Diepenbrock's presentation described Rambus's "offensive" patent strategy as "find[ing] key areas of innovation in our IP that are essential to creating a competing device" and "claim[ing] these areas as broadly as possible within the scope of what we invented."[230] The first two examples cited in Diepenbrock's presentation were DLLs and dual-edge clocking.[231]

Meanwhile, Diepenbrock advised Crisp – just as Vincent had in 1992 – that Rambus faced a risk of equitable estoppel based on its participation in JEDEC.[232] Diepenbrock urged that Rambus withdraw from JEDEC.[233] At his next JEDEC meeting, in December 1995, Crisp made private inquiries regarding JEDEC's patent policy.[234] Based on these discussions, as summarized in an e-mail to Rambus executives, Crisp stated that it was unacceptable "to not speak up when we know that there is a patent issue, to intentionally propose something as a standard and quietly have a patent in our back pocket we are keeping secret that is required to implement the standard and then stick it to them later (as WANG and SEEQ did)."[235]

Later that month, Vincent sent Diepenbrock "materials relating to the proposed [FTC] consent order involving Dell computer," which resolved allegations of unfair methods of competition based on Dell's assertion of patent rights after its representative had certified to an

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[227] Crisp, Tr. 3341-44. Crisp promptly reported MOSAID's disclosure to Rambus management. *See* CX 711 at 192.

[228] CX 837 at 2.

[229] Diepenbrock, Tr. 6129-30.

[230] CX 1267; Diepenbrock, Tr. 6131.

[231] CX 1267; Diepenbrock, Tr. 6132-33.

[232] Crisp, Tr. 3442.

[233] *Id*. at 3442-43.

[234] *Id*. at 3440-44, 3447-48; CX 711 at 188 (Crisp e-mail describing conversations with Sanyo's Howard Sussman and VLSI Technology's Desi Rhoden). Crisp testified that he sought this information because Rambus was considering making a presentation regarding a proposed technology. Crisp, Tr. 3440-41, 3447-48.

[235] CX 711 at 188. Crisp's e-mail adds, "I am unaware of us doing any of this or of any plans to do this." *Id*.

SSO that a standard under consideration did not infringe any Dell patents.[236] Vincent's notes from the period conclude that there should be "no further participation in any standards body . . . do not even get close!!"[237]

***1996.*** On January 11, 1996, Vincent met with Rambus executives – including Tate, Crisp, and Diepenbrock – to discuss *Dell* and other matters.[238] Rambus attended no JEDEC meetings after this date.[239] According to Crisp, Rambus was concerned that attendance at future meetings could leave Rambus in a vulnerable position in future litigation.[240]

During this period, however, Rambus continued to build its patent portfolio. On October 6, 1995, the PTO had sent Rambus's attorney a notice of allowability on the '646 application, which had claims relating to dual-edged clocking.[241] According to Diepenbrock, this meant that "the patent office has reason to believe or believes that the claims should go to issuance."[242] Rambus paid the issuance fee on January 5, 1996, and the ensuing patent, No. 5,513, 327 ("the '327 patent") issued on April 30, 1996.[243] Issuance of this patent was a noteworthy event within Rambus.[244]

On June 17, 1996, Rambus sent a letter to JEDEC, signed by Crisp, stating that Rambus was not renewing its membership.[245] Rambus enclosed "a list of Rambus U.S. and foreign patents" and stated that "Rambus has also applied for a number of additional patents in order to protect Rambus technology."[246] The letter emphasized that "Rambus reserves all rights regarding

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[236] CX 1990. *See* Dell Computer Corp., 121 F.T.C. 616 (1996).

[237] CX 1928 (emphasis original).

[238] CX 3126 (Vincent *Infineon* Dep.) at 536-38 (*in camera*).

[239] Rambus Answer, ¶ 41.

[240] CX 858 at 2 ("the current plan is to go to no more JEDEC meetings due to fear that we have exposure in some possible future litigation"); Crisp, Tr. 3358.

[241] CX 1482; Diepenbrock, Tr. 6190. *See supra* note 220.

[242] Diepenbrock, Tr. 6151.

[243] *Id*. at 6185, 6192; CX 1494.

[244] Diepenbrock, Tr. 6194.

[245] CX 887.

[246] *Id*.

its intellectual property."[247] Rambus omitted from the list that it provided to JEDEC the only then-issued patent that Rambus believed covered technology under consideration by JEDEC – the '327 patent.[248]

Rambus's June 1996 withdrawal letter also omitted information that would have allowed JEDEC members to adopt standards that would avoid infringing Rambus's intellectual property. While the letter mentioned inconsistency between JEDEC and Rambus with respect to the "terms" of licensing, and purported to reserve Rambus's rights respecting its intellectual property, Rambus omitted to disclose that it had used information gleaned during JEDEC meetings to develop a patent portfolio covering JEDEC's SDRAM and DDR SDRAM standards, and also omitted to disclose the patent applications Rambus had filed to implement its strategy. To the contrary, the letter stated, "To the extent that anyone is interested in the patents of Rambus, I have enclosed a list of Rambus U.S. and foreign patents."[249] Rambus's list identified *only* patents unrelated to JEDEC's work.[250] Rambus's letter stated that Rambus had applied for "a number of additional patents" but the letter did not suggest that future patents would be any more applicable to JEDEC's DRAM standards than were the issued patents on the list.

***1997 and subsequent years.***[251] Although Rambus terminated its JEDEC membership in 1996, Rambus continued to receive information on the activities of JEDEC after 1996. Beginning in 1997, Crisp received information from a source that he referred to as "deep

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[247] *Id*.

[248] *See* CX 5013 (designated R401208-09) (Joel Karp presentation regarding "Enforcement Scenario for 1999," stating, " '327 – covers DDR (dual-edged clocking)"). (The "R" designation refers to Bates stamp numbers that appear on this and other exhibits admitted into this record from the *Infineon* litigation.)

[249] CX 887.

[250] Although some of the listed patents derived from the '898 application, none of them applied to JEDEC's SDRAM and DDR SDRAM work, Jacob Tr. 5365-66, 5501-02, and none was named in Rambus's infringement complaints or counterclaims against DRAM manufacturers. *Compare* CX 887 at 2 (Rambus's list of issued patents) *with* CX 1855 (complaint against Hitachi), CX 1867 (complaint against Infineon), CX 1878 at 13-14 (counterclaims against Hyundai), CX 1891 at 2 (claims asserted against Hyundai/Hynix), *and* CX 1880 at 29-38 (counterclaims against Micron).

[251] By including herein a discussion of Rambus's post-resignation conduct, we do not mean to suggest that a firm that never participated in a standard-setting process – or that did so without deception, then resigned from the SSO – would be at risk of Section 2 liability if it monitored the standard-setting process from the outside and developed a patent portfolio covering standards it believed would be adopted. Rambus's post-resignation conduct was quite different. It represented the continuation, albeit in a different form, of a deceptive course of conduct that began more than four years before Rambus formally "resigned" from JEDEC. Rambus's "resignation" did nothing to cure its prior course of conduct. If anything, the resignation operated to conceal further Rambus's course of conduct, because Rambus's resignation letter left the impression that Rambus had disclosed what was relevant when, in fact Rambus had done nothing of the sort. Under these circumstances, treating Rambus's post-resignation conduct as benign could invite further abuses of standard-setting processes that otherwise might be procompetitive.

throat."[252] Crisp also received information from three other unsolicited sources known as "Mixmaster," a reporter called "Carroll Contact," and "secret squirrel."[253] According to Crisp, these sources provided information on the features of devices being proposed for standardization.[254] Crisp shared the information he obtained from these inside sources with Rambus's executives and engineers,[255] and this information was used in the continuing process of filing and amending Rambus's patent applications.[256]

Additionally, although no longer a JEDEC member, Rambus continued to conceal its relevant patent applications. Rambus CEO Tate, for example, stated in a February 1997 e-mail to Rambus executives, "do *NOT* tell customers/partners that we feel DDR may infringe – our leverage is better to wait."[257] Likewise, a July 1997 e-mail by Rambus Chairman of the Board Bill Davidow stated that "[o]ne of the things we have avoided discussing with our partners is intellectual property problem [infringement by SyncLink and SDRAM/DDR SDRAM] . . . . We are hoping that they will either drop their competitive efforts or discover for themselves that they have violated Rambus patents and will conclude that getting around them will be either extremely difficult or impossible and will take a lot of time."[258] And in its October 1998 "strategy update," Rambus stated, "We should not assert patents against Direct partners until ramp reaches a point of no return."[259] In sum, after leaving JEDEC, Rambus strategically maintained its silence, thereby prolonging the misimpression created by its prior conduct.

By March 1998, a DDR SDRAM standard incorporating all four of the technologies that Rambus claims are covered by its patents had been approved by the JC 42.3 committee.[260] The JEDEC Council approved that standard, and it was published as a JEDEC standard in August

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[252] CX 929; CX 932.

[253] IDF 280-81; Crisp Tr. 3412-18.

[254] Crisp Tr. 3417.

[255] CX 935 at 1; CX 929 at 1; CX 973 at 1; CX 979 at 1; CX 1014 at 1.

[256] Crisp Tr. 3418. *See generally* CX 5115 (November 1996 Tate e-mail announcing plans for an "IP strategy" panel to discuss Rambus efforts to use intellectual property "in process" to "block . . . SDRAM-2 . . . .").

[257] CX 919.

[258] CX 938 at 1.

[259] CX 5011 at 3 (designated R401155).

[260] IDF 380; JX 40 at 7-8; CX 375.

1999.[261] By November 1999, Rambus had obtained all four patents cited in its first complaint against JEDEC-compliant uses (filed against Hitachi) in January 2000.[262]

b. Rambus's "Notice" to JEDEC

Rambus claims that it twice gave notice to JEDEC of its patents and patent applications through responses to questions. Based on our review of the evidence regarding those incidents, we find that, far from giving notice, Rambus's responses were evasive and, indeed, misleading.

The first incident, in May 1992, was an outgrowth of concerns held by IBM and Siemens regarding possible Rambus patents on dual-bank designs. In the course of a discussion of that technology at a JEDEC meeting, some of the participants noted the possibility that Rambus and Motorola might have patents on multi-bank designs (a technology that is not at issue here).[263] Motorola's representative promised to check and to get back to JEDEC with an answer.[264] Expressing concern that Rambus might have a patent on multi-bank designs, and noticing that Rambus had stayed silent, Siemens's Meyer asked the DRAM task group chairman, Gordon Kelley of IBM, to pose a direct question to Rambus.[265] Kelley asked whether Rambus wanted to comment.[266] Rambus's representative, Crisp, shook his head "no."[267] Crisp did not explain whether that gesture meant that Rambus lacked such a patent, whether he did not know the

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[261] IDF 381; CX 234.

[262] CX 1855. Rambus followed this initial suit with a complaint against Infineon, filed in August 2000, CX 1867, and with counterclaims against Hyundai/Hynix, CX 1878, and Micron, CX 1880, filed in February 2001, all alleging infringement based on JEDEC-compliant uses. Rambus quickly induced other industry members to enter licenses covering production of JEDEC-compliant products. *See* CX 1391a at 8 (November 2000 Tate "Big Picture Update," stating that more than 40% of the "SDRAM/DDR market" had already accepted Rambus licenses); CX 1154 (November 2000 Tate e-mail noting that SDRAM/DDR SDRAM and RDRAM licenses already gave Rambus royalties from close to half of the entire DRAM market); CX 1689 (*in camera*) (December 2000 SDRAM/DDR SDRAM license with Mitsubishi).

[263] *See* RX 297 at 4-5; CX 2089 at 133 (Meyer *Infineon* Trial Tr.) (*in camera*).

[264] *See* CX 2089 at 133 (Meyer *Infineon* Trial Tr.) (*in camera*).

[265] *See* CX 673; CX 2089 at 133, 164 (Meyer *Infineon* Trial Tr.) (*in camera*).

[266] *See* Crisp, Tr. 3066 (Kelley "asked me if I cared to comment and I declined to comment"); CX 673 (Crisp e-mail stating, "Gordon Kell[e]y of IBM asked me if we would comment which I declined."); CX 2089 at 136 (Meyer *Infineon* Trial Tr.) (*in camera*) (Kelley formulated the question as, "Do you want to give a comment on this"). *But cf.* G. Kelley, Tr. 2543 (unable to recall whether he had said anything to Rambus and suggesting that it was Meyer who asked Rambus whether it had patentable material).

[267] *See* CX 673; CX 2089 at 135-37 (Meyer *Infineon* Trial Tr.) (*in camera*) ("he just shook his head"); Calvin, Tr. 1068-70 (Crisp responded in the negative); RX 290 at 3 ("NO RAMBUS COMMENTS"); RX 297 at 5 ("No comments given").

answer to the question posed, or something else. He did *not* say that the gesture meant that Rambus would not disclose relevant patents or patent applications, and the record shows that those present did not read that into his gesture.[268]

The second incident relates to a May 1995 JEDEC subcommittee discussion of the SyncLink memory technology. This is not a technology at issue here.[269] A number of companies were asked whether they had relevant patents. Intel's Sam Calvin asked whether Rambus had patents relevant to SyncLink, and then DRAM task group chairman, IBM's Gordon Kelley, addressed to Crisp a request that Rambus provide a statement as to whether Rambus had patents that covered SyncLink.[270]

At the next JEDEC subcommittee meeting on September 11, 1995, Rambus furnished a written response that focused on its patents and patent applications relevant to SyncLink alone.[271] Indeed, except for the concluding sentence, the entire statement referred exclusively to SyncLink. The record shows that the JEDEC meeting attendees interpreted the statement as relating to SyncLink only and therefore of no moment.[272] Moreover, Rambus took additional steps to

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[268] Intel's Calvin testified that the incident gave him no concern. Calvin, Tr. 1070-71. Meyer and Kelley ultimately concluded that Rambus had no relevant patents. CX 2089 at 151-52 (Meyer *Infineon* Trial Tr.) (*in camera*); G. Kelley, Tr. 2545-46, 2562. Only IBM's Kellogg termed the lack of response by Rambus a concern, Kellogg, Tr. 5323, but he also testified that the May 1992 meeting did not cause him to understand that Rambus had intellectual property applicable to SDRAM. *Id.* at 5056.

[269] Crisp agreed that "the SyncLink proposal was similar to the Rambus architecture in a number of places." Crisp, Tr. 3254-55. SyncLink, like RDRAM but unlike SDRAM and DDR SDRAM, involved a narrow-bus technology, using multiplexing and packetization for command and address information. *See, e.g.,* Becker, Tr. 1203-04; Sussman, Tr. 1405 (SyncLink a "totally different architecture" from SDRAM and DDR SDRAM); G. Kelley, Tr. 2573; Crisp, Tr. 3254 (SyncLink packetized); CX 1069 (same); Kellogg, Tr. 5090-91 and 5095 (SyncLink involved a narrow bus and packetization; it had some similarities to RDRAM); Tabrizi, Tr. 9119. RamLink, from which SyncLink evolved, used a narrow-bus, packetized, and fully multiplexed architecture, as did RDRAM. *See id.* at 9116-17, 9119; *see generally* RX 555 at 5 (April 1995 Crisp letter noting that RamLink and RDRAM "work in a very similar manner").

[270] *See* CX 711 at 73 (Crisp's meeting report, indicating that "Kelley asked to have us state whether or not Rambus knows of any patents especially ones we have that may read on Synchlink"); Crisp, Tr. 3266-67 (agreeing that Kelley asked for a report as to whether "Rambus knows of any patents that may read on SyncLink"); G. Kelley, Tr. 2578. JEDEC minutes of the meeting provide no specifics. *See* JX 26 at 10 (stating only, "Patent issues were a concern in this proposal.").

[271] *See* JX 27 at 26.

[272] *See* Sussman, Tr. 1411-13; Kellogg, Tr. 5093-96. Indeed, JEDEC's minutes described the discussion entirely in terms of SyncLink and its predecessor, RamLink. *See* JX 27 at 4 ("SyncLink/ RamLink patents were discussed. Rambus noted at the general meeting their position (see [the message presented by Crisp]).").

Between April and August 1995, Crisp told several people that SyncLink and RamLink likely violated Rambus's patents. *See* RX 555 at 5 (statement to Hyundai regarding RamLink); CX 711 at 73 (statement to Intel representatives regarding SyncLink), 80 and 90-91 (statement to JEDEC consultant regarding RamLink, forwarded

deflect attention from the potential breadth of the statement's final sentence.[273] After Kelley commented that Rambus had not said anything, Crisp re-framed the final sentence in terms of SyncLink: "I reminded them . . . that our silence was not an agreement that we have no IP *related to SycLink* (sic). . . ."[274] In addition, Crisp reminded the members that Rambus previously had reported a patent to JEDEC, suggesting that this placed Rambus in the category of JEDEC members who had disclosed patents.[275]

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The record demonstrates that Rambus's course of conduct included two species of potentially deceptive conduct set forth in the Policy Statement:

- Rambus made potentially deceptive omissions via its continuing concealment of its patents and patent applications until after the DDR SDRAM standard was in place; and

- Rambus made outright misrepresentations when it gave evasive and misleading responses to questions about its conduct.

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by recipient to IBM and Hewlett Packard (HP) JEDEC participants, among others), 104-05 (statement to HP JEDEC participant regarding RamLink and SyncLink); RX 592 at 2 (August 1995 statement to SyncLink Consortium regarding RamLink and SyncLink). Although the ALJ treated Crisp's SyncLink/RamLink disclosures as giving notice regarding JEDEC standards, ID at 280-81, the record shows only that the disclosures raised concerns regarding SyncLink. For example, on June 12, 1995 – two days after receiving a copy of Crisp's statement regarding Rambus patents covering RamLink, CX 711 at 90 – IBM's Gordon Kelley called for an IBM review of possible Rambus patents on SyncLink. RX 575 at 6-7.

In this context, Rambus's September 1995 message sounded no alarm. As Crisp phrased it, subcommittee chairman Kelley's reaction was that "he heard a lot of words, but did not hear anything said." CX 711 at 166. Similarly, Motorola's meeting report termed the Rambus letter a "non-statement statement." RX 615 at 1. Crisp even encouraged the reaction that Rambus was revealing nothing new. *See* RX 576 at 2 (June 1995 Crisp e-mail to an HP JEDEC participant, noting that Crisp already had shared his personal opinion that Rambus patents would cover SyncLink and RamLink, and that in September Rambus would provide an "official" response to JEDEC's request "to report on our patent coverage relative to SyncLink").

[273] Rambus's statement ends, "Our presence or silence at committee meetings does not constitute an endorsement of any proposal under the committee's consideration nor does it make any statement regarding potential infringement of Rambus intellectual property." JX 27 at 26.

[274] CX 711 at 167 (emphasis added).

[275] CX 711 at 167; Crisp, Tr. 3312-13. During its membership, Rambus disclosed no patent applications and only one issued patent to JEDEC, U.S. Patent No 5,243,703 ("the '703 patent"), which Rambus disclosed in September 1993. Crisp, Tr. 3173, 3176; CX 1801 at 3; Parties' First Set of Stipulations, Item 11. None of the claims of the '703 patent covered SDRAM or DDR SDRAM. *See* Parties' First Set of Stipulations, Item 10 (stating that as of January 1996 Rambus held no issued U.S. patents essential for compliance with any JEDEC standard); Crisp, Tr. 3173-74; Jacob, Tr. 5498-99.

In addition, Rambus used information gained through its participation in JEDEC to help shape a patent-filing strategy that included filing patent applications covering key parts of the SDRAM and DDR SDRAM standards.

This course of conduct was intentionally pursued, in accordance with a strategy that was spelled out in Rambus's own internal documents and e-mails. We conclude that Rambus's course of conduct had the potential to be deceptive and, under the circumstances of this case, exclusionary.

### 3. The JEDEC Environment

Next, we consider the standard-setting environment at JEDEC. The ALJ focused on whether JEDEC's rules imposed on JEDEC members an affirmative duty to disclose their patents and patent applications. Finding that the rules did not expressly contain such a requirement, the ALJ concluded that Rambus had no duty to disclose its patent filings and, therefore, that Rambus had not engaged in any wrongful conduct.[276] We respectfully find that this analysis and conclusion were erroneous. The Complaint in this case alleged not just a breach of a duty to disclose under JEDEC rules, but a course of conduct that was materially deceptive under *all* of the circumstances in which the standard setting occurred.[277]

In order to determine whether Rambus's course of conduct actually was deceptive, we need to consider the totality of the circumstances in which that conduct occurred. For the reasons discussed below, we find that JEDEC's policies (including the policies of its parent, EIA) and practices, considered as a whole, gave JEDEC's members reason to believe the standard-setting

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[276] *See* IDF 766-85, 902, 939-82; ID at 260-79.

[277] We recognize that the Federal Circuit in *Infineon* found Rambus not liable, ruling that Rambus had not breached a duty to disclose. However, the case before the Federal Circuit in *Infineon* was very different from the case here. In particular, the claim before the Federal Circuit was a state law fraud claim. Rambus, Inc. v. Infineon Tech. AG, 318 F.3d 1081, 1084, 1087 (Fed. Cir. 2003). In contrast, this case involves a federal antitrust claim alleging exclusionary, deceptive conduct. *See* FTC v. Freecom Commc'ns., Inc., 401 F.3d 1192, 1203 n.7 (10th Cir. 2005) ("A § 5 claim simply is not a claim of fraud as that term is commonly understood . . . ."). The standards of proof for these claims are different. To prove a fraud case in Virginia, the plaintiff had to meet a clear and convincing evidence standard. *Id* at 1096. Here, Complaint Counsel must satisfy a lower preponderance of the evidence burden. *See supra* Section III.

Not only are the claims and evidentiary standards different, but so are the records. We take note that the joint appendix that presented the evidentiary record on which the Federal Circuit relied contained the testimony of only *two* industry witnesses (other than witnesses from Rambus and Infineon and the parties' experts) – AMI-2's Desi Rhoden (previously employed by HP and then by VLSI) and IBM's Gordon Kelley. In contrast, the record in this proceeding, from which we have assessed the industry's understandings and expectations, contains testimony from approximately 30 non-Rambus, industry witnesses. Our record includes testimony from five DRAM manufacturers and from major DRAM customers and developers of systems and complementary components, such as Sun, Compaq, Cray, Cisco, Intel, AMD, ATI, nVIDEA, Texas Instruments, and Sanyo, in addition to multiple witnesses from HP and IBM.

process would be cooperative and free from deceptive conduct. In that environment, we find that Rambus's course of conduct was likely to be "material" because it was likely to infect the decisions of JEDEC members with respect to the SDRAM standards to be adopted.

### a. EIA/JEDEC Policies and their Dissemination

The record shows that although EIA/JEDEC policies are not a model of clarity, a duty of good faith underlies the standard-setting process under those policies. Specifically, under the EIA/JEDEC rules, "[a]ll EIA standardization programs . . . shall be carried on in good faith under policies and procedures which will assure fairness and unrestricted participation . . . ."[278] Another general EIA regulation provides that EIA standardization programs "shall not be proposed or indirectly result in . . . restricting competition, giving a competitive advantage to any manufacturer, excluding competitors from the market . . . except where required to meet one or more of the" enumerated "legitimate public interest" objectives.[279]

To accomplish that EIA goal, as the majority opinion in *Rambus v. Infineon Technologies A.G.* declared,[280] JEDEC's Manual of Organization and Procedure (the JEDEC manual) expressly obligated the subcommittee chairperson to remind members to inform the meeting of any patents or applications "that might be involved in the work" being undertaken.[281] EIA General Counsel/JEDEC legal counsel John Kelly testified that JEDEC's rules required disclosure of patents and patent applications.[282] For most of the time that Rambus was a member

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[278] CX 204 at 5.

[279] *Id*.

[280] 318 F. 3d 1081, 1098 (Fed. Cir. 2003).

[281] CX 208 at 19 (JEP21-I, JEDEC Manual of Organization and Procedure) (Oct. 1993). Although Rambus and the ALJ question whether this manual was officially adopted, *see* RB at 15-16, IDF 627-28, the record does not support that speculation. *See* CX 205 at 15 (establishing procedure for amending predecessor manual 21-H); CX 54 at 7, G. Kelley, Tr. 2428, and J. Kelly, Tr. 1925 (together establishing that the specified steps occurred). For present purposes, however, the important point is that manual JEP21-I was operative – it shaped JEDEC members' expectations. Numerous JEDEC members understood that the JEP21-I manual set out JEDEC's disclosure policies. *See, e.g.*, Rhoden, Tr. 311-13; Sussman, Tr. 1349; Landgraf, Tr. 1702-04; G. Kelley, Tr. 2408-09. Indeed, when Crisp requested a copy of JEDEC's patent policies in 1995, JEDEC sent him JEP21-I. CX 2104 at 215–16 (deposition transcript at 851-52) (Crisp *Micron* Dep.) (*in camera*).

[282] *See* J. Kelly, Tr. 1903-04 (disclosure "not optional"), 1925-27 (a "requirement to disclose"), 1870 (EIA Publication EP-3 means that participants need to disclose known patents and patent applications), 1894 (Kelly always understood "patent" to include applications), 1897 (coverage of applications was necessary to make the protections effective), 1931-33 (JEP21-I was an effort "to make it abundantly clear" and "to be emphatic, to pound the table" after WANG had argued that JEDEC patent policy did not reach applications), 1935-36 ("patentable" in sign-in sheets refers to applications). John Kelly served as General Counsel of EIA and legal counsel for JEDEC from September 1990 through the time of the Commission's trial. *Id*. at 1750, 1754. He also became President of JEDEC in early 2000. *Id*. at 1751. Kelly was responsible for providing "legal guidance relating to standardization

of JEDEC, the JC 42.3 sub-committee chairman was James Townsend. Townsend created and delivered presentations designed to advise members of JEDEC's patent policy at each JC 42.3 subcommittee meeting, as well as at other JC 42 subcommittee meetings.[283] He also delivered this presentation to new members during their orientation.[284]

Furthermore, JEDEC's policies expressly required those disclosing relevant patents or patent applications to supply full technical information and to provide RAND assurances (*i.e.*, that royalties on patents covering any standard would be reasonable and non-discriminatory) before their patents were incorporated into JEDEC standards. As presented in Appendix E to the JEDEC manual, "Standards that call for use of a patented item or process may not be considered by a JEDEC committee unless all of the relevant technical information covered by the patent or pending patent is known to the committee, subcommittee, or working group," and the patent holder submits written assurance that it will license without charge or under "reasonable terms and conditions that are demonstrably free of any unfair discrimination."[285]

### b. Rambus's Understanding of JEDEC's Policies

Following the lead of the Federal Circuit's *Infineon* opinion, we look to the behavior, understandings, and expectations of JEDEC members, including Rambus, to inform our understanding of the JEDEC environment.[286] Rambus's own documents and witnesses indicate that the company believed it should have disclosed its patent filings. For example, Rambus's JEDEC representative, Crisp, understood that "[t]he job of JEDEC is to create standards which

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activities," including dealing with questions regarding "the patent policy of EIA and JEDEC." *Id.* at 1813-14. He testified that he had the "last word" within EIA on how rules were to be interpreted and applied and the "final word" in interpreting and applying JEDEC's separate rules. J. Kelly, Tr. 1822, 1915. Others supported Kelly's descriptions. *See* Rhoden, Tr. 313-14, 345; Sussman, Tr. 1348-49 (people with questions regarding patent policy were referred to Kelly); Grossmeier, Tr. 10957 (same); CX 208 at 18 (JEDEC manual stating, "EIA Legal Counsel can advise the Council and committees from time to time concerning interpretation of legal guides."); CX 306 (EIA/JEDEC Meeting Attendance Roster, referencing EIA patent policy and stating, "Consult the EIA General Counsel about any doubtful question.").

[283] *See, e.g.*, Rhoden, Tr. 324-25, 330; Williams, Tr. 771, 785; Calvin, Tr. 1007-08; Landgraf, Tr. 1694-95; CX 42 at 3. The JC 42 committee and its subcommittees met four to eight times per year, and these meetings lasted several days. Rhoden, Tr. 340. The subcommittee meetings were staggered, permitting Townsend to make his patent presentation at multiple subcommittee meetings. If a JEDEC member participated in more than one subcommittee, the member would hear Townsend's patent presentation multiple times. *Id.* at 338-42.

[284] Rhoden, Tr. 337-42.

[285] CX 208 at 27; *see also* J. Kelly, Tr. 1885-86; CX 208 at 19 (noting that "the word 'patented' also includes items and processes for which a patent has been applied and may be pending"); CX 203a at 11 (EIA Engineering Publication EP-3-F) (1981); CX 207a at 8 (EIA Engineering Publication EP-7-A) (1990); JX 55 at 28 (EIA Engineering Publication EP-7-B) (1995).

[286] *See* Rambus, Inc. v. Infineon Techs. AG, 318 F.3d 1081, 1098 (Fed. Cir. 2003).

steer clear of patents which must be used to be in compliance with the standard whenever possible."[287] Rambus was aware of JEDEC's disclosure policy through written manuals and oral presentations.[288] Crisp understood that disclosure of patents was mandatory,[289] and as early as December 1992, he acknowledged that he understood that patent applications had to be disclosed under JEDEC's policies at least "in some circumstances."[290]

### c. Other JEDEC Participants' Understanding of JEDEC's Policy Objectives

Other witnesses besides Crisp testified that JEDEC had determined that prompt disclosure of relevant intellectual property was important for its standard-setting process to work.[291] Absent such disclosure, JEDEC members would face the possibility of patent hold-up. A member possessing relevant intellectual property could stay silent while JEDEC adopted a standard. Then, after a standard had been adopted and it had become expensive to switch to what initially were good alternatives, the patentee could assert its patent and "hold up" the industry by charging higher royalties than could have been extracted before the standard was set. Witnesses testified that early disclosure of intellectual property helped to identify potential hold-up situations while there still was time to avoid the problem.[292]

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[287] CX 903 at 2; Crisp, Tr. 2941-42.

[288] Crisp attended a JEDEC meeting at which revisions subsequently incorporated into the JEDEC manual – including specific references to pending patents and to the participants' obligation to disclose – were presented. *See* JX 14 at 1, 3, 25 (minutes of JC 42.3 meeting, December 9-10, 1992, providing text with proposed changes underlined); Rhoden, Tr. 312; G. Kelley, Tr. 2418.

[289] Crisp, Tr. 3477-78 (stating that "[n]on-presenters were obligated to disclose any known patents they had at the time of the committee letter ballot if those patents were required to – were required by the standard" and that presenters were required to disclose patents and applications earlier); *see also* CX 868 (February 1996 Crisp e-mail stating, with reference to a presentation to JEDEC by Micron, "I think we should have a long hard look at our IP and if there is a problem, I believe we should tell JEDEC there is a problem.").

[290] Crisp, Tr. 2978, 2982, 3477-78. *See also* CX 5105 (December 1992 Crisp e-mail stating "I know that JEDEC takes the position that we should disclose," but commenting, "Of course, we believe that we do not want to do this [disclose patent applications] yet.").

[291] *See, e.g.*, Rhoden, Tr. 536 (describing a "fundamental premise inside JEDEC" that standards that are developed are "either free of intellectual property or at least all intellectual property is known at the time of creation of the standard"); Calvin, Tr. 1002 ("you at least needed to understand the [e]ffect of patents upon things that you were standardizing"); Landgraf, Tr. 1694 ("the purpose of the policy is to disclose and make sure that standards do not have any conflicts down the road with their potential use").

[292] *See* Landgraf, Tr. 1694 ("The worst thing to have is a standard and products made according to that standard and then later you find an infringement . . ."); J. Kelly, Tr. 1908 ("It's essential to know what impediments there are to the process, what issues there are going forward, and to know when it's necessary to obtain the written assurances."). Even if the standard later could, in theory, be revised to avoid patent issues, that would entail added

For example, EIA General Counsel/JEDEC legal counsel John Kelly testified that JEDEC sought to prevent members with patents covering JEDEC standards from exercising "unbridled discretion to license that IP on any terms and conditions that they elect."[293] He explained:

> Having the technology included in the standard is a privilege, and the condition for that – for having that privilege is to agree to a restriction on licensing. That in turn allows the marketplace to know that they're dealing with a standard that anyone can comply with on a – on a reasonable basis without – without being, if you'll excuse the expression, gouged in terms of IP licensing royalties.[294]

Other witnesses agreed that JEDEC wished to secure knowledge of potential patents and protections against the unrestricted exercise of patent rights.[295]

### d. Disclosure Expectations of JEDEC Members

A number of witnesses besides Crisp testified that they understood that the disclosure of *patents* and *patent applications* was expected. For example, witnesses from Micron,[296] NEC/Sanyo,[297] AMI-2,[298] Intel,[299] and Hewlett Packard (HP),[300] among other JEDEC

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cost and potentially crippling delay. *See* Rhoden, Tr. 299-300 ("delay is not a viable market option. . . . You have to move in real time at the time that technology is being developed to create the standards.").

[293] J. Kelly, Tr. 1777.

[294] *Id*. at 1782.

[295] *See, e.g.*, Williams, Tr. 771-72, 794; Calvin, Tr. 1002; Sussman, Tr. 1333. Rambus suggests that a portion of the EIA Legal Guides rejects any goal of avoiding hold-up. RB at 9-10; *see also* ID at 261-62. According to those Guides, "Standards are proposed or adopted by EIA without regard to whether their proposal or adoption may in any way involve patents . . . ." CX 204 at 4. The Initial Decision correctly construes this as a "non-liability disclaimer," IDF 633 – the next sentence of the EIA Legal Guides states that EIA does not assume any obligation to parties adopting EIA standards. CX 204 at 4; *see also* J. Kelly, Tr. 1836-37. Treating this as evidence that JEDEC had no goal of avoiding hold-up stretches a mere disclaimer beyond its limits. The language reveals a willingness to accept patented technologies for standardization under stated conditions, but that does not negate a parallel objective to protect against hold-up whenever patented technologies are adopted. *See* J. Kelly, Tr. 1837-40.

[296] *See* Williams, Tr. 771-72, 774 (members "had to" disclose), 788-89, 791-96 (disclosure of applications required during 1991-93 period); Lee, Tr. 6595-96 (from the time that he started attending JEDEC meetings in the mid-1990s, disclosure of applications was required); Lee, Tr. 6695-96 ("a requirement to disclose").

[297] *See* Sussman, Tr. 1333, 1346 (disclosure "required," not voluntary), 1333-34 (disclosure of applications required), 1341-42 (requirement to disclose applications antedated JEP21-I by at least 10 years).

[298] *See* Rhoden, Tr. 309, 317-19, 344-45 ("everyone had the obligation to disclose"), 619 ("you were obligated to disclose"), 627, 317 (disclosure of applications was always required), 320-21, 332 (Townsend would

participants,[301] consistently testified that JEDEC members were "obligated" or "required" to disclose both patents and applications.[302]

Several of these witnesses also testified to an expectation that members would disclose planned amendments to pending applications. One witness testified that there was an obligation to disclose "everything that is in the patent process . . . if you intend to seek protection of your intellectual property as it relates to the standard . . . ."[303] Similarly, another witness testified that the disclosure obligation focused on the reasonable possibility that a firm's "invention" might apply to what was being discussed within JEDEC, "no matter what stage a patent might be."[304] As stated succinctly by a former HP employee, "the expectation was that members would disclose anything they're working on that they potentially wanted to protect with patents down the road."[305]

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always say disclosure of applications was required), 357 (duty to disclose covered applications), 637 (same).

[299] *See* Calvin, Tr. 1003-04 ("anyone who was aware of patent – patented items, that could affect policy, had an obligation to bring that awareness to the group); 1006-07 (a requirement to disclose patent applications), 1012-13 (same).

[300] Landgraf, Tr. 1693-95 (from the time that he started attending JEDEC meetings in 1994, disclosure of applications was required).

[301] *See, e.g.*, CX 3135 at 102 (Chen FTC Dep.) (*in camera*); McGrath, Tr. 9245 (during the 1992-96 period there was "an expectation that patent applications would be disclosed"); CX 2089 at 142-43 (Meyer *Infineon* Trial Tr.) (*in camera*) (JEDEC disclosure rules covered applications in April-July 1992).

[302] IBM's Gordon Kelley believed that the understanding that disclosure of applications was mandatory may have developed over time, with two JEDEC Committees, JC 42 and JC 16, requiring disclosure of applications by 1991 and JEDEC as a whole doing so by 1993. *See* G. Kelley, Tr. 2667-70, 2685-86, 2690-92. A witness from Mitsubishi presented varying descriptions. *See* CX 3135 at 16 (Chen FTC Dep.) (*in camera*) (disclosure of applications was one step beyond requirements; Mitsubishi had disclosed applications "multiple times"), 102 (disclosure of applications was required), 111. One other witness stated that it was his understanding that applications did not have to be disclosed if any ensuing patents would be made available under reasonable and nondiscriminatory terms, but that that "may have been wrong." Wiggers, Tr. 10591.

[303] Rhoden, Tr. 317-21, 636.

[304] Williams, Tr. 788, 791.

[305] Landgraf, Tr. 1698-99. *See also* Sussman, Tr. 1341 ("something that you're about to apply for"); G. Kelley, Tr. 2406-07 (there was an obligation to disclose "material that would probably become a patent"). EIA General Counsel/JEDEC legal counsel John Kelly explained that the need to disclose when making plans to amend derived from the *present* "interpretation of the original patent or patent application," not from "the future plan, as such." J. Kelly, Tr. 1995. *But see* CX 3136 at 28-29 (Meyer *Infineon* Trial Tr. 110-11) (*in camera*) (stating his understanding that disclosure of plans to modify applications was not required, but explaining that he drew this conclusion only from an absence of discussion of the issue and that he could not state whether or not this was JEDEC's policy).

e. The Behavior of JEDEC Participants

The expectation that members would disclose their patents and patent applications was supported by their actions. Although JEDEC's members were not expected to disclose if they did not plan to enforce their patents against JEDEC-compliant standards,[306] there were numerous examples of JEDEC members disclosing patents and applications relevant to the standards under consideration. For example, in February 1992, during Rambus's first JEDEC meeting as a member, Fujitsu disclosed a patent application, as described by initial Rambus JEDEC representative Garrett in a memorandum to Rambus staff.[307]

JEDEC and its members reacted negatively when members sought enforcement after failing to disclose that a patent was issued or pending, and without providing the necessary RAND assurances. The record reveals three such instances – all of which were known to Crisp and thus to Rambus.[308]

The first instance occurred in the late 1980s and early 1990s involving then-JEDEC member Wang Laboratories. Wang held a patent application relating to memory modules.[309] During its membership, Wang helped JEDEC set a standard relating to memory modules, but failed to disclose its intellectual property.[310] After the standard was adopted, Wang sought to

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[306] For example, Micron's Terry Lee testified that Micron had failed to disclose patent activity in or around 2000 when it had "no intent on enforcing the patent against the standard." Lee explained, "My understanding was that if they failed to disclose the patent that may relate to the work of the committee and if it was adopted into the standard, that they would forego their right to enforce the patent against the standard." Lee, Tr. 6599. Micron also disclosed three burst EDO patent applications in April 1996, after the standard already had been issued. *See* Williams, Tr. 937-40. A Micron representative testified that Micron never intended to enforce patents on burst EDO against firms that might practice JEDEC's burst EDO standard. *Id*. at 960-62. *But cf.* CX 364 (Micron letter disclosing the patents to JEDEC and affirming that "[i]n accordance with EIA/JEDEC patent policy" if a patent issued, Micron would license under RAND terms). Burst EDO died, and the standard never became a factor in the market. Williams, Tr. 961-62. Another example was Hitachi's failure to disclose a patent that was never enforced. Sussman, NEC/Sanyo's JEDEC representative, testified that, " . . . Hitachi has never tried to apply the patent, so some engineer has a few extra dollars, and basically a [sic] don't care." Sussman, Tr. 1337-38.

[307] CX 672 at 1; *see also* JX 22 at 14-16 (patent tracking list showing disclosure of both issued patents and applications); CX 42 at 16-17 (same); JX 28 at 6 (minutes describing MOSAID's December 1995 disclosure of "a patent pending on DLL"); CX 711 at 169 (Crisp's description of Fujitsu's disclosure of an application in September 1992); RX 1559 at 2 (Micron's January 2000 disclosure of an application); CX 3135 (Chen FTC Dep.) (*in camera*) at 16-17 (Mitsubishi disclosed patent applications "multiple times"), 111.

[308] *See* CX 711 at 188 (Crisp e-mail discussing incidents involving Wang and SEEQ); CX 346 (JEDEC minutes reporting on JEDEC members' reaction to Texas Instruments's conduct).

[309] IDF 689. *See* J. Kelly, Tr. 1931-32.

[310] IDF 690.

enforce its patents against the industry.[311] Considerable litigation ensued, and the incident generated concern and discussion among JEDEC participants about the need to prevent the problem from recurring.[312]

The second instance involved a proposal by a company called SEEQ, which sought adoption of a standard regarding silicon signature.[313] SEEQ had two patents or applications relating to the technology, but disclosed, and provided licensing assurances for, only one.[314] JEDEC learned of the second item when it was recommending standardization of the SEEQ technology, and it sought RAND assurances, which SEEQ apparently refused.[315] Ultimately, JEDEC chose an alternative technology.[316] Although the events traced to 1989, they left "a negative taste in our mouth" that was still "almost current" in 2003.[317]

The third occurrence involved an attempt by Texas Instruments (TI) to enforce an undisclosed patent on Quad CAS technology. After JEDEC learned of the patent in 1993, the JC 42.3 subcommittee placed a ballot covering the technology on hold,[318] and voted to withdraw a preexisting standard.[319] It took the ballot off hold and dropped the withdrawal of the standard only after TI had provided satisfactory assurances of compliance with JEDEC's licensing policies.[320] A witness from Micron testified that TI's actions led to "a great uproar" and that TI's representative was "pummeled in th[e] meeting for his failure to disclose."[321] Crisp reported to his superiors that TI was "chastised" for not reporting the patent and that discussion was

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311 Williams, Tr. 787; Sussman, Tr. 1338; Landgraf, Tr. 1697-98.

312 J. Kelly, Tr. 1932; Grossmeier, Tr. 10954.

313 Sussman, Tr. 1338.

314 *Id*. at 1338-39.

315 CX 3 at 4; CX 711 at 188.

316 *See* Sussman, Tr. 1338-39.

317 *See* Sussman, Tr. 1339 ("[W]e were making nasty comments about SEEQ for years . . . .").

318 JX 17 at 6-7.

319 JX 18 at 7-9.

320 JX 25 at 5.

321 Williams, Tr. 776-77.

"nasty."[322] In the course of the dispute, IBM's Gordon Kelley, chairman of JC 42.3's DRAM Task Group, addressed TI in the strongest of terms:

> I am and have been concerned that this issue can destroy the work of JEDEC. If we have companies leading us into their patent collection plates, then we will no longer have companies willing to join the work of creating standards . . . . If we allow JC-42 standards to be used for patent collection purposes, then we do a great disservice to the very industry that feeds us.[323]

JEDEC's responses to the SEEQ, Wang, and TI incidents evidence that JEDEC members believed that these firms had acted in ways contrary to JEDEC's policies and members' expectations.

### f. Knowledge of JEDEC Participants

The ALJ concluded[324] that since 1989 the DRAM industry has been aware of Rambus's inventions in the relevant markets and its plans to seek patent protection. Rambus points to presentations regarding its technologies made to several JEDEC members before and during its membership.[325] Rambus also cites, and the ALJ highlighted, Rambus's publication in the early 1990s of technical descriptions of its inventions, as well as Rambus's 1992 distribution of marketing brochures describing its technology in conjunction with the public announcement of its business plan.[326] Rambus further argues that statements during its campaign to convince various industry players to adopt and license RDRAM placed the industry on notice regarding Rambus's intellectual property.[327]

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[322] Crisp, Tr. 2969, CX 710 at 1. *See also* CX 346.

[323] CX 2384 (G. Kelley letter to TI of January 14, 1994).

[324] ID at 305-09.

[325] *See, e.g.*, RX 273 (Rambus presentation to IBM in April 1992). These presentations were covered by nondisclosure agreements, required by Rambus from each company that was exposed to RDRAM technology. *See* Parties' First Set of Stipulations, Items 3-7 (noting nondisclosure agreements with NEC, Sony, Toshiba, HP, and Samsung); Kellogg, Tr. 5053 (stating that Rambus met with International Business Machines (IBM) and required "a nondisclosure agreement of sorts"); Bechtelsheim, Tr. 5816-19 (noting that Rambus met with Sun Microsystems (Sun) and required nondisclosure agreements); CX 535 at 1 (stating Rambus's intention to secure nondisclosure agreements from "all parties exposed to the [Rambus] technology"). These nondisclosure agreements barred those hearing the presentations from sharing Rambus information with other firms.

[326] RB at 37; IDF 109-21, 130-34, 144-58; ID at 306.

[327] *See* RB at 36-37.

The only information that Rambus made available, however, was that it was claiming patent rights with regard to technologies in *RDRAM* – not with respect to SDRAM, DDR SDRAM, or any JEDEC-based successors. The prevailing view in the industry was that RDRAM, with its narrow-bus architecture and its multiplexing and packetization, was quite different from the SDRAM and DDR SDRAM standards that were being developed by JEDEC.[328] JEDEC representatives who viewed an RDRAM presentation emerged with the view that RDRAM bore little or no resemblance to JEDEC-compliant SDRAM.[329] For example, IBM's Gordon Kelley testified that after Rambus presented its technology to IBM in April 1992, he believed that "the Rambus DRAM [RDRAM] was so different from the synchronous DRAM being discussed at JEDEC that [he] just did not believe that anything that Rambus had on the RDRAM might apply to the SDRAM or to JEDEC."[330] Indeed, Rambus's own Joel Karp highlighted the extent to which the industry perceived fundamental differences between RDRAM and SDRAM/DDR SDRAM when, in May 1999, he stated, "They probably think they avoid our IP if they don't go 'packet based.'"[331] Under these circumstances, an awareness that Rambus held or likely would seek patents covering RDRAM did not equate to any contemplation that Rambus could or would obtain patents on SDRAM or DDR SDRAM.

The ALJ and Rambus also rely on the publication in October 1991 of Rambus's international patent application, known as the PCT application, to show that the industry had notice that Rambus might acquire patents covering SDRAM and DDR SDRAM.[332] Rambus

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[328] *See, e.g.*, Rhoden, Tr. 402-03; (RDRAM was multiplexed and packetized); Sussman, Tr. 1431-33 (same); Lee, Tr. 6602-03 (RDRAM used narrow bus and was multiplexed); Farmwald, Tr. 8275 (RDRAM packetized); Horowitz, Tr. 8617-18 and 8620 (RDRAM multiplexed), 8621 (RDRAM packetized); CX 1451 at 9, 43 ('898 application describing a "narrow, multiplexed (time-shared) bus"); RX 81 at 7 (1992 Rambus Corporate Backgrounder describing Rambus technology as "a narrow, high-speed bus"). (Although the initial idea behind RDRAM was to use a narrow bus, Horowitz, Tr. 8619-20, as time went by RDRAM's bus widened. *See* Farmwald, Tr. 8143-44.)

In contrast, SDRAM and DDR SDRAM had a wider bus, little or no multiplexing, and were not packetized in the same sense as RDRAMs. *See, e.g.*, Rhoden, Tr. 400-01 (SDRAM had a wider bus than RDRAM); Sussman, Tr. 1439 (same); G. Kelley, Tr. 2573-74 (JEDEC DRAMS were not packetized); Kellogg, Tr. 5298 (JEDEC did not consider narrow bus, packetized architecture); Jacob, Tr. 5462-64 and 5470-71 (JEDEC-based DRAMs used wider buses), 5464-67 (SDRAMs used separate buses for data, control, and address information and were not packetized in same way as RDRAMs); Bechtelsheim, Tr. 5841 (RDRAM used a packet transaction format, and SDRAM did not); Tabrizi, Tr. 9119 (JEDEC DRAMS were not multiplexed).

[329] *See* G. Kelley, Tr. 2538; Sussman, Tr. 1439-40; Kellogg, Tr. 5053; Lee, Tr. 6602-03.

[330] G. Kelley, Tr. 2537-38.

[331] CX 1069.

[332] *See* RB at 39-41, 117; ID at 298, 307. This application, filed pursuant to the Patent Cooperation Treaty ("PCT"), CX 1454 at 1; IDF 826, was virtually identical to the '898 application, the parent application for the patents that Rambus has asserted against SDRAM and DDR SDRAM manufacturers. *See* IDF 826; Fliesler, Tr. 8811; CX 1451; CX 1454; Parties' First Set of Stipulations, Item 22.

similarly relies on its September 1993 disclosure to JEDEC of the '703 patent, which had substantially the same written description as the PCT and '898 applications.[333]

We find that these materials did not provide notice that Rambus might seek to enforce patent rights covering the standards under consideration by JEDEC. None of the original 150 claims in the '898 patent application – which were reproduced in the PCT application – covered SDRAM or DDR SDRAM;[334] nor did any claims in the '703 patent.[335] Although notice might come from the written descriptions as well as from the claims, those descriptions, like Rambus's RDRAM marketing efforts, suggested that claims would be confined to the RDRAM architecture – with a narrow bus, multiplexing, and packetization. Several JEDEC members reviewed Rambus's PCT application or '703 patent and concluded that they had no relevance to JEDEC's standards. Thus, when Infineon's Meyer read the PCT application and the '703 patent, he understood them to relate to RDRAM, including, specifically, its multiplexing.[336] And when Micron's Terry Lee reviewed Rambus's patent abstracts and the '703 patent in 1995, he concluded that the patents "seemed to apply kind of specifically to this bus architecture, to this RDRAM product. . . . the narrow bus with the command/address/data multiplexed with this Rambus architecture and Rambus signaling scheme."[337] Even Rambus's own JEDEC representative, Crisp, initially read the '898 application as limited to multiplexed, packetized architectures, *i.e.*, to RDRAM.[338]

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[333] IDF 181; Jacob, Tr. 5500-01.

[334] Nusbaum, Tr. 1526; Jacob, Tr. 5494; Parties' First Set of Stipulations, Item 9 (discussing SDRAM).

[335] Parties' First Set of Stipulations, Item 10; *see also* Crisp, Tr. 3173-74; Jacob, Tr. 5498-99.

[336] *See* CX 2089 at 147-48 (Meyer *Infineon* Trial Tr.) (*in camera*).

[337] Lee, Tr. 6610-11; *see also* Sussman, Tr. 1445, 1449-54 (stating that he found no connection between the PCT application and JEDEC's work). *But cf.* Sussman, Tr. 1467-68 (concluding that a portion of the PCT application highlighted by Rambus counsel did relate to dual-edge clocking).

Rambus argues that because Mr. Lee in 1997 informed JEDEC that a Rambus patent might relate to JEDEC's work, he could not have believed that the Rambus architecture mattered. RB at 41. The technology that Mr. Lee identified to JEDEC was a loop-back clocking scheme, Lee, Tr. 6956-64, one of only two aspects of the '898 application that *did not* contain the multiplexed bus limitation that distinguished Rambus's architecture from JEDEC's work. Nusbaum, Tr. 1520, 1528. Rambus also points to an incomplete translation of Mitsubishi's analysis of the PCT application; the translation shows awareness that the application covered relevant technologies, and found "similar[ity] to SDRAM's latency control," but it also includes several references to "packets" or "packetize[d] bus" and does not indicate whether claims could extend beyond the RDRAM architecture. *See* RX 379a and RX 2213a. Mitsubishi subsequently recommended concentrating on "a wide-bus approach" because "Narrow-bus is Rambus look alike," suggesting that Mitsubishi still believed that avoiding RDRAM architecture mattered. RX 852 at 1.

[338] Crisp, Tr. 2926-27. Crisp added that over time his view of the scope of Rambus's application changed. *Id.* at 2927-28. Rambus's expert witnesses asserted that the written descriptions would have given notice of the potential reach of Rambus's claims, *see, e.g.*, Fliesler, Tr. 8788-89, 8810; Geilhufe, Tr. 9556-59, but Complaint

Rambus attempts to transform its argument into a matter of law by presenting the following syllogism: (1) the PTO may only approve patents when their written description covers their claims; and (2) the PTO issued the patents that Rambus has sued upon; so that (3) the written description in the '898/PCT applications and the '703 patent necessarily must have given adequate notice to the world of every claim that eventually issued.[339] This miscasts an inquiry designed for application with hindsight as a test for the reasonable bounds of foresight. The ability, after the fact, to determine from a written description that at the time of filing an applicant "*was* in possession" of a particular invention "*now* claimed"[340] is not the same thing as the ability to predict, prior to their publication, the potential scope of future claims.[341] Rambus's own patent expert regarded the unrevealed claims of a published application as "the family jewels."[342] Rambus avoided displaying those jewels to JEDEC members, and we find that, without knowledge of Rambus's eventual claims, JEDEC members were unable to foresee the implications of the pending applications.

Finally, the ALJ and Rambus point to two incidents – one involving IBM and Siemens in 1992, the other involving Rambus licensing negotiations in 1995 – to demonstrate the industry's awareness of Rambus's relevant patents and patent applications. The IBM/Siemens incident involved a conference call on April 29, 1992, recorded as follows in Siemens's notes: "RAMBUS has announced a claim against Samsung for USD 10 million due to the similarity of the SDRAM with the RAMBUS storage device architecture."[343] The only concern, however, was that Rambus might have a patent on a technology outside any of the alleged relevant product

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Counsel's experts stated the opposite. *See* Nussbaum, Tr. 1642-43; Jacob, Tr. 5460-67; 54576-85, 5490, 5493, 5498-501.

[339] RB at 39-40.

[340] *See* Vas-Cath, Inc. v. Mahurkar, 935 F.2d 1555, 1563-64 (Fed. Cir. 1991) (describing patent law's written description requirement) (emphasis added).

[341] Rambus acknowledges this distinction, averring that "[a] patent application continues to hold valuable trade secrets even after the written description becomes public . . . . Disclosure of the written description does not reveal the *claims* in the pending application." RB at 87 (emphasis original).

[342] Fliesler, Tr. 8896. Fliesler agreed that "[a]n engineer or a patent lawyer could not have known for certain what Rambus would claim from reading the '898 specification," *id*. at 8902, although he nonetheless insisted that the '898 application "indicat[ed]" that Rambus had invented the four relevant technologies as used in SDRAM and DDR SDRAM. *Id*. at 8904-05.

[343] RX 286a at 2. The record does not provide details regarding this claim which, had it existed, would have antedated Rambus's first issued patent by more than a year. Parties' First Set of Stipulations, Item 11; CX 1460 at 1.

markets in this case.[344] Ultimately, IBM and Siemens both concluded that Rambus posed no patent problems for SDRAM.[345]

The other incident involved Rambus meetings with LG Semiconductor, Samsung, NEC, and Oki in 1995, at which Rambus CEO Tate claimed he announced that Rambus was seeking patents on DDR SDRAM.[346] In his testimony, Tate did not indicate the specific information that he purportedly conveyed. While his testimony names on-chip PLL and dual-edge clocking as the likely technologies at issue, nowhere does he state that he identified those technologies to the outside firms.

Other evidence suggests that any information conveyed by Rambus would have been opaque. Indeed, a 1997 Tate e-mail indicates that LG continued to believe that DDR SDRAM was a "royalty-free alternative[]" to RDRAM.[347] Moreover, Rambus President Mooring admitted that, to the best of his knowledge, Rambus did not inform any DRAM manufacturer that [Rambus intellectual property covered SDRAM and did not tell anyone that on-chip PLL might infringe a Rambus patent until late 1999.[348] Similarly, Rambus's Senior Vice President Gary Harmon testified that any discussion relating to the [scope of Rambus's patents in the course of 1993-96 licensing negotiations, including those with all four firms identified by Tate, would have been "just a passing reference" and that, even in the case of the one firm with which discussions were more extensive, "I don't believe we ever specifically

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[344] *See* RX 297 at 5 (showing that a few days later, in the course of discussing two-bank designs at JEDEC's May 4-8, 1992 meetings, Siemens and Philips indicated that they were "concerned about [the] patent situation" with regard to Rambus and Motorola); *see also* RX 303 (June 1992 presentation by Gordon Kelley to IBM and Siemens engineers listing "cons" for SDRAMs to include "Patent Problems? (*Motorola/Rambus*)") (emphasis added); CX 2089 at 41-44 (Meyer *Infineon* Trial Tr.) (the concern in May 1992 for Meyer was the possibility that Rambus might obtain patents covering two-bank synchronous DRAM design); RX 289 at 1 (Siemens document prepared by Meyer on May 6, 1992, stating concern that "2-BANK SYNC MAY FALL UNDER RAMBUS PATENTS"). Although the ALJ also cites an IBM "Rambus Assessment" as revealing IBM's concern that Rambus might have patents over SDRAM, IDF 791-95, ID at 307, the document says nothing about such patents. RX 279.

[345] G. Kelley, Tr. 2537-38, 2545-46; CX 2089 at 151-52 (Meyer *Infineon* Trial Tr.) (*in camera*).

[346] CX 2111 at 313-21 (Tate FTC Dep.) (*in camera*).

[347] CX 957 at 1. Tate did not correct LG's misimpression, despite having an incentive to do so if he already had chosen to inform LG of Rambus's patent position on DDR SDRAM.

[348] CX 2112 at 172-73, 179-80 (deposition transcript at 171-72, 178-79) (Mooring FTC Dep.) (*in camera*). Rambus apparently did tell Intel in late 1997 or early 1998 that Rambus might have patent applications related to DDR, but Rambus provided "no specifics" and gave "nothing concrete" as to what the applications covered. MacWilliams, Tr. 4905.

stated that we had intellectual property that applied to – outside of the Rambus-compatible area]."[349]

JEDEC members repeatedly testified that they were unaware of Rambus's patent position when they adopted the standards. NEC/Sanyo's Sussman testified that prior to 1999 Rambus never suggested or did anything that put him on notice that its patents might relate to either SDRAM or DDR SDRAM.[350] HP's Landgraf stated that while he was at JEDEC (from 1994 through 1998), he "did not know of patents or patent applications with regard to dual edge clock or PLL on chip" and believed that the DDR SDRAM standard was free of undisclosed patents.[351] Cisco's Bechtelsheim termed Rambus's infringement suits "a complete surprise"; when asked whether before 2000 he had ever heard any rumor or suggestion that Rambus might have patents that would extend to SDRAM or DDR SDRAM, Bechtelsheim answered, "I did not."[352] Similarly, IBM's Gordon Kelley testified that when he voted to include programmable CAS latency and burst length in SDRAM, he had no understanding that Rambus might have relevant patents.[353]

Contemporaneous views support this testimony. In October 1993, when Willibald Meyer prepared documentation for Siemens of the status of work regarding SDRAM, he concluded that "we had managed to define a public domain version" of the next generation DRAM, free of intellectual property.[354] Hyundai's July 1997 "DRAM Product Roadmap" described DDR SDRAM as the most "cost effective" next generation DRAM with an "open architecture without

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[349] CX 2070 at 42-47 (Harmon *Micron* Dep.) (*in camera*). In addition, a 1997 e-mail from the Chairman of Rambus's Board of Directors, William Davidow, stated that "[o]ne of the things we have avoided discussing with our partners is [the] intellectual property problem," which he identified as the fact that "SLDRAM and SDRAM-DDR infringe our patents." CX 938.

Even assuming *arguendo* that certain JEDEC representatives who observed Rambus's presentations were aware of the extent of Rambus's patent portfolio, each representative's company was prohibited by non-disclosure agreements from discussing the content of Rambus's license presentations. *See, e.g.*, RX 24 at 2-3 (nondisclosure agreement between Rambus and IBM); RX 570 (nondisclosure agreement between Rambus and NEC); Rhoden, Tr. 521 (HP); Kellogg, Tr. 5052-53 (IBM); Bechtelsheim, Tr. 5818-19 (Sun); CX 673 (Crisp, interpreting NEC's nondisclosure agreement to bar circulation of a published international patent application). JEDEC members would not have been able to discuss the implications of Rambus's patents, absent disclosure by Rambus itself. *See, e.g.*, CX 993 (Tate 1998 e-mail stating, "[O]ur partners employee's [sic] working on competitive products, e.g., DDR, might have access to our confidential information. [T]hey might even go to committees like jedec to discuss DDR. BUT they are obligated as employees of our partners' [sic] to keep our confidential information secret . . . .").

[350] Sussman, Tr. 1455-56.

[351] Landgraf, Tr. 1711-12.

[352] Bechtelsheim, Tr. 5880-81.

[353] G. Kelley, Tr. 2561-62.

[354] CX 2089 at 151-52 (Meyer *Infineon* Trial Tr.) (*in camera*).

royalties or fees."[355] A 1998 Siemens presentation compares RDRAM's "Proprietary solution (Royalties, License fees)" unfavorably with SDRAM II's "Open standard."[356]

In addition, it makes little sense that JEDEC members – which had, for example, "chastised" TI during a "nasty" discussion when it attempted to enforce an undisclosed patent[357] and which cared deeply about cost[358] – would, if they had known about Rambus's patents and patent applications, simply have ignored them and, knowingly and without discussion or hesitation, adopted a standard incorporating Rambus's technology. At a minimum, we would expect the members to have confronted Rambus and demanded RAND terms (even if, as Rambus argues, its technology was so superior that JEDEC had no choice but to adopt it).[359]

Rambus's own documents evince the belief that it had kept secret its patent position relative to JEDEC's standards. In August 1997, Rambus CEO Tate remarked, "[W]e already have the 327 patent but few people are aware of what it means," continuing, "[O]ur policy so far has been NOT to publicize our patents and i think we should continue with this."[360] In May 1999, Rambus Intellectual Property Vice President Karp surmised, "They probably think they avoid our IP if they don't go 'packet based.'"[361] In November 1999, Rambus named its IP initiative "Lexington 'The Shot Heard Around the World,'"[362] which Karp thought fitting because, "We fully anticipated at that point that once people became aware that we had IP covering sync DRAM, DDR, that it was going to make some noise."[363] Even in December 1999 Tate was still directing that, if asked whether DDR SDRAM infringes Rambus IP, "it's important

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[355] CX 2294 at 15. Similarly, Hyundai's 1998 cost comparison between DDR SDRAM and Direct RDRAM listed "Direct Rambus Royalty" as a "Cost Adder." CX 2303 at 16. And Hyundai's April 1999 presentation to the PC Platform APAC Technology Forum contrasts the benefits of DDR SDRAM's open standard with the negative impact of RDRAM's royalty cost. CX 2334 at 25, 27.

[356] CX 2442 at 36. Although Rambus cites a 1997 internal Micron e-mail as evidence that an Intel employee had told Micron's Intel account representative that Rambus might claim patent coverage over DDR SDRAM, Micron regarded the rumor as "typical" of "misinformation" and "overstatements" that were circulating in advance of Rambus's initial public offering and did not credit it. *See* Lee, Tr. 6700-10, discussing RX 920 at 1-2.

[357] *See supra* note 322 and accompanying text.

[358] *See infra* notes 404-408 and accompanying text.

[359] *See infra* Section IV.C.3.b. (concluding that Rambus has not demonstrated its claims of superior technology).

[360] CX 942; *see also* CX 919; CX 987 at 4.

[361] CX 1069 (commenting on an article entitled "Industry group will push DDR DRAMs").

[362] CX 5002 (designated R401047).

[363] CX 5069 at 54 (deposition transcript at 563) (Karp 2004 *Infineon* Dep.).

NOT to indicate/hint/wink/etc what we expect the results of our [infringement] analysis to be!!!"[364]

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We find nothing in the record to suggest that, in the cooperative environment prevailing at JEDEC, the incidents to which the ALJ and Rambus have pointed were sufficient to put JEDEC members on notice that Rambus would pursue a deceptive course of conduct to obtain patents covering JEDEC's standards, then engage in patent hold-up to extract royalties on terms of Rambus's choosing.

4. Rambus's Conduct Was Deceptive

JEDEC's policies (fairly read) and practices, as well as the actions of JEDEC participants, provide a basis for the expectation that JEDEC's standard-setting activity would be conducted cooperatively and that members would not try to distort the process by acting deceptively with respect to the patents they possessed or expected to possess. Those policies rested on an express duty of good faith, as well as an objective of avoiding creation of unnecessary competitive advantages. The policies also included rules to ensure that members periodically were reminded to disclose patents and patent applications, and that patented technologies would be included in standards only after receipt of RAND assurances. JEDEC thus presented the type of consensus-oriented environment in which deception is most likely to contribute to competitive harm.

JEDEC's members expected disclosure of both patents and patent applications that might be applicable to the work JEDEC was undertaking, if the patents ever were going to be enforced against JEDEC-compliant products. These expectations were fostered by JEDEC's policies and were reflected by the behavior and understandings of JEDEC participants. Rambus's own descriptions of its understanding of the SSO's objectives and requirements reinforce that conclusion.

Rambus's course of conduct played on these expectations. Rambus sat silently when other members discussed and adopted technologies that became subject to Rambus's evolving patent claims. Rambus voted and commented on inclusion of programmable CAS latency and burst length without revealing that it was seeking patent coverage of those technologies, despite language on the ballot that called for disclosure of relevant patents. Rambus twice evaded direct questions about its patent portfolio, coupling a nonresponsive answer with a reminder that it previously had disclosed a patent (which lacked any claims then relevant to JEDEC's work). Rambus even provided JEDEC with a list of its patents that omitted the one patent Rambus believed covered JEDEC's work.

[364] CX 1089.

At the same time that Rambus was avoiding disclosure of its patent activity, Rambus was engaged in a program of amending its applications to develop a patent portfolio that would cover JEDEC's standards. Rambus made full use of information gleaned from its JEDEC participation to accomplish this objective. Rambus's JEDEC representative was charged with overseeing development of patent claims that would provide better coverage of products compliant with JEDEC's SDRAM standards, and Rambus's CEO asked for progress reports on claims that would cover the JEDEC standards.

Rambus argues that amending patent applications based on competitive information is a legitimate business practice condoned by the patent laws.[365] Rambus cites *Kingsdown Medical Consultants, Ltd. v. Hollister, Inc.*[366] and its progeny as establishing that there is nothing improper in amending claims to cover a competitor's product that the applicant learns about during the patent prosecution process. The cases relied upon by Rambus find no impediment, from a *patent law* perspective, to prosecuting or enforcing a claim developed under those circumstances.[367] These cases do not, however, involve either facts or law relevant here. None considers how the applicant learned of the competing product, or whether the applicant used that information in ways inconsistent with the understandings of other participants in a cooperative standard-setting environment. None of those cases examines the competitive consequences of the conduct.

In contrast, our concern in this proceeding is harm to competition, not to the patent system. Here, Rambus used information gained through participation in cooperative JEDEC processes by tailoring its patent claims to facilitate hold-up, while deceiving other JEDEC members regarding its patent position. The abuse of industrywide standard-setting efforts, and the competitive harms that may ensue, were not at issue in the cases cited by Rambus – but these factors are central to determining whether Rambus's actions constituted exclusionary conduct.

We find that Rambus's course of conduct constituted deception under Section 5 of the FTC Act. Rambus's conduct was calculated to mislead JEDEC members by fostering the belief that Rambus neither had, nor was seeking, relevant patents that would be enforced against JEDEC-compliant products. Rambus's silence, in the face of members' expectations of disclosure, created a misimpression that Rambus would not obtain and/or enforce such patents. When suspicions arose, Rambus allayed them with the reminder that it had made a prior disclosure. The message that Rambus reasonably conveyed – in a context in which it had been asked about its patent position, and in which other members expected disclosure of patents and

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[365] RB at 89-91.

[366] 863 F.2d 867 (Fed. Cir. 1988), *cert. denied*, 490 U.S. 1067 (1989).

[367] *See, e.g., Kingsdown*, 863 F.2d at 869, 872, 874 (considering a patent applicant's actions in terms of the "deceitful intent" element of purported "inequitable conduct before the [PTO]"); Emerson Electric Co. v. Spartan Tool, LLC, 223 F.Supp. 2d 856 (N.D. Ohio 2002) (refusing to infer that an applicant had deceived the patent examiner by amending a claim without highlighting all ramifications of the change).

applications – was that Rambus would have disclosed if it had had anything relevant to reveal. Even Rambus's withdrawal letter misleadingly conveyed the impression that it was listing its issued patents, while failing to disclose the one patent that might have mattered to the other JEDEC members. Under the circumstances, JEDEC members acted reasonably when they relied on Rambus's actions and omissions and adopted the SDRAM and DDR SDRAM standards.

Rambus withheld information that would have been highly material to the standard-setting process within JEDEC. JEDEC expressly sought information about patents to enable its members to make informed decisions about which technologies to adopt, and JEDEC members viewed early knowledge of potential patent consequences as vital for avoiding patent hold-up. Rambus understood that knowledge of its evolving patent position would be material to JEDEC's choices, and avoided disclosure for that very reason.[368] We thus find that Rambus engaged in representations, omissions, and practices that were likely to mislead JEDEC members acting reasonably under the circumstances, to their substantial detriment, and we conclude that Rambus intentionally and willfully engaged in deceptive conduct.

As discussed in detail in Sections IV.B. and IV.C. below, Rambus's course of deceptive conduct contributed significantly to Rambus's acquisition of monopoly power by distorting JEDEC's technology choices and undermining JEDEC members' ability to protect themselves against patent hold-up. This conduct caused harm to competition. In sum, the record establishes a *prima facie* case that Rambus engaged in exclusionary conduct.

### 5. Rambus's Procompetitive Justification for its Conduct

Our finding that Complaint Counsel established a *prima facie* case of exclusionary conduct shifts the burden to Rambus to establish a nonpretextual, procompetitive justification for its conduct.[369] Rambus must prove "that its conduct is indeed a form of competition on the merits because it involves, for example, greater efficiency or enhanced consumer appeal."[370]

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[368] Rambus now argues that disclosure would not have changed JEDEC's decision because of the superiority of Rambus's technologies. We address that argument *infra* in Section IV.C.3.b.

[369] A respondent may rebut a *prima facie* case of exclusionary conduct by introducing evidence of a procompetitive justification for its actions. *See* United States v. Microsoft Corp., 253 F.3d 34, 59 (D.C. Cir.), *cert. denied*, 534 U.S. 952 (2001).

[370] *See id.* For example, the D.C. Circuit found that Microsoft had "valid technical reasons" to cause its Windows operating system to ignore user-chosen browser defaults in certain circumstances. The court then found that the plaintiffs had failed either to rebut that justification or to demonstrate that the anticompetitive effect of the challenged action outweighed it. *Id.* at 67.

Deceptive conduct is extraordinarily difficult to justify.[371] Rambus tries to avoid this challenge by characterizing its conduct as a refusal to deal with its competitors or a failure to "share its trade secrets with others."[372] Rambus then defends its conduct on the grounds that it preserved the secrecy of Rambus's patent applications, which contained confidential information about Rambus's inventions.[373] Rambus's characterization ignores much of its deceptive course of conduct, as well as the context in which that conduct occurred.

As discussed above, Rambus engaged in a deliberate course of deceptive conduct that included selective omissions and outright misrepresentations relating to its intellectual property.[374] Indeed, Rambus used information obtained via its participation in JEDEC to help shape and refine the very patent applications it now claims it was seeking to protect.[375] Rambus's supposed desire to maintain the secrecy of its intellectual property does not justify the totality of its deceptive conduct in the standard-setting context.

We weigh Rambus's justification in the context of its conduct. In the competitive marketplace, companies generally are justified in choosing not to disclose or share their unpublished patent applications and trade secrets.[376] The ALJ (and Rambus), citing Rambus's patent law expert, found three reasons why, in a competitive context, the non-disclosure of this information serves legitimate and procompetitive purposes.[377] However valid these justifications might be in the abstract – or when applied within a competitive marketplace – they do not fit the record facts or the context that existed here. Further, if protecting trade secrets was critical to Rambus, it had the option to refrain from participating in JEDEC.

First, Rambus argued that withholding of information was justified because disclosure of that information "shows which inventions the applicant is seeking to protect, and thus reveals both technical information and the applicant's business strategies." Preserving trade secrets by preventing access by rivals in a competitive marketplace often may be procompetitive, particularly when that information is not otherwise protected from free-riding by those rivals. However, the technical information comprising Rambus's inventions (as opposed to its

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[371] *Id*. at 77 ("[u]nsurprisingly, Microsoft offers no procompetitive explanation for its campaign to deceive developers.")

[372] RB at 113.

[373] *See* RB at 86-88, 114-15.

[374] *See supra* Section IV.A.

[375] *Id*.

[376] The PTO held patent applications in confidence during the period that Rambus belonged to JEDEC. In 1999, the law changed to require publication of most patent applications 18 months after filing. 35 U.S.C. § 122.

[377] ID at 288-89; RB at 87.

intentions to claim that those inventions covered technologies in JEDEC's DRAM standards – which, as discussed above,[378] could not be divined until the ultimate claims became public) already had been disclosed with publication of the written descriptions of the inventions in the PCT application and the '703 patent. Morever, Rambus has claimed in its numerous infringement actions that the patent laws provide full protection against unlicensed use of its technical inventions, at least for periods after Rambus's patents issued.

It is true that if Rambus had disclosed its relevant patent applications to JEDEC members, the disclosure might have exposed Rambus's business strategy to obtain patents covering JEDEC's DRAM standards – but Rambus does not explain how keeping that strategy secret would be procompetitive given the cooperative atmosphere of the SSO. To the contrary, disclosure would have enabled other participants in the standard-setting process to make their decisions based on knowledge that Rambus's business strategy was to enforce its patents and demand royalties if they were incorporated in standards adopted by JEDEC. As one treatise summarizes, withholding information as to the existence of patent applications in such a setting "would be most valuable as a tool for deception."[379]

Second, Rambus argued that disclosure "could jeopardize the applicant's ability to obtain foreign patents" by "enabl[ing] a competitor to win the 'race'" to foreign patent offices, most of which have "a 'first to file' rule."[380] But under typical first-to-file rules, patents go to the first *inventor* to file.[381] If a competitor merely read or heard Rambus's disclosure, copied its application, and filed first in a foreign jurisdiction, the competitor would not have invented the technology and would not be entitled to a patent.[382] Rambus failed to identify any foreign jurisdiction in which its ability to obtain patent protection would have been threatened by disclosures within JEDEC. Under these circumstances, and on this record, the only effect of Rambus's behavior was to prevent JEDEC participants – who expected Rambus to conduct itself

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[378] *See supra* notes 328-338 and accompanying text.

[379] II HOVENKAMP ET AL., IP AND ANTITRUST § 35.5 at 35-40 n. 17.11 (2006 Supp.).

[380] RB at 87_88.

[381] *See* Gerald J. Mossinghoff, *The First-To-Invent Rule in the U.S. Patent System has Provided No Advantage to Small Entities*, 87 J. PAT. & TRADEMARK OFF. SOC'Y 514 (2005) ("As between two true inventors claiming the same invention – as contrasted to copiers – *every* nation in the world, except the United States, grants the patent to the inventor who first undertakes to use the patent system . . . . In shorthand, this is called a first-to-file system of priority, but it is more appropriately called a first-inventor-to-file system.") (emphasis original); MARTIN J. ADELMAN *et al.*, CASES AND MATERIALS ON PATENT LAW 160 (2003) (under a first-to-file system, "the *inventor* who first files a patent application obtains the patent, even if another actually invented the technology first") (emphasis added); Fliesler, Tr. 8839 (explaining the first-to-file race in terms of "*inventor* A and *inventor* B who are conceiving and reducing to practice and working independently, but simultaneously on the same invention") (emphasis added).

[382] *See* Fliesler, Tr. 8839 (the first one to file "that is otherwise entitled to a patent" prevails).

cooperatively and without deception – from making their standard-setting decisions with knowledge of the consequences. That is not procompetitive.

Third, we are not persuaded that Rambus's non-disclosure of its patent applications was justified because disclosure "may enable a competitor to slow down or interfere with the patent application process," such as by "enabl[ing] a competitor to provoke an 'interference' at the Patent Office by claiming the same invention in one of the competitor's applications."[383] This, too, is a hypothetical justification. There is no evidence in this record that Rambus's patent position in the United States or elsewhere would have been jeopardized in that fashion.

Finally, Rambus cites Crisp's trial testimony and an e-mail he sent to Rambus executives to support its claim regarding the protection of trade secrets.[384] Crisp testified that Rambus's outside patent counsel advised him that patent applications should be confidential; however, Crisp did not state that counsel's advice was tied to Rambus's course of conduct in the JEDEC standard-setting context.[385] Moreover, although Crisp's e-mail mentioned the desirability "of not disclosing our trade secrets any earlier than we are forced to," the context suggested that this comment reflected Rambus's desire for leverage over its customers.[386] There is abundant additional evidence in the record that Rambus's conduct was motivated by a desire to anticompetitively bias the standard-setting process.[387] In short, there is nothing to support Rambus's claim except the claim itself.

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We find that Rambus did not carry its burden of establishing that its conduct served procompetitive purposes. The record establishes that the purpose and effect of Rambus's deceptive conduct was to manipulate the standard-setting process at JEDEC and gain market power. Furthermore, even if we were to credit Rambus's proffered justification, we find that it would not outweigh the anticompetitive effects of Rambus's exclusionary conduct, particularly in light of the potential to distort industrywide standard setting.

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[383] RB at 87.

[384] *See id*. at 49-50, 98-99.

[385] Crisp, Tr. 3473, 3495-96. Other, more specific advice from Rambus counsel (Diepenbrock as well as Vincent) identified the equitable estoppel risks associated with Rambus's JEDEC membership. *See* CX 837 at 1; CX 1942; CX 3125 at 320-21 (Vincent *Infineon* Dep.) (*in camera*).

[386] Crisp's same e-mail also referenced the need "to get the necessary amendments completed [and] the new claims added," and "make damn sure the ship is watertight," before making disclosures. *See* CX 837 at 2.

[387] *See, e.g.*, CX 711at 73 ("it makes no sense to alert them to a potential problem they can easily work around."); CX 919 ("do *NOT* tell customers/partners that we feel DDR may infringe – our leverage is better to wait."); CX 1277a at 2 ("do not tell them :-").

## B. Possession of Monopoly Power

Monopoly power may be established either by direct evidence of such power – *i.e.*, the power to raise price above competitive levels or to exclude competition – or by indirect evidence, such as a high market share in a properly defined relevant market with high barriers to entry.[388] In order to support a Section 2 violation, such monopoly power must be durable. When barriers to entry are low, any attempt to exercise monopoly power (even by a firm with 100 percent market share) quickly would be countered by competition from new entrants.[389]

As discussed above,[390] the alleged relevant product markets involve technologies that are incorporated in DRAM for use in current and recent-generation electronic memory devices.[391] The four alleged relevant technology markets are: (1) the latency technology market; (2) the burst length technology market; (3) the data acceleration technology market; and (4) the clock synchronization technology market. With respect to each of these four technology markets, the product market comprises alternative technologies available to address a given technical issue arising in the course of DRAM design.[392] The alleged relevant geographic market for each of these four technologies is the world.[393] Rambus accepts these market definitions.[394]

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[388] *See, e.g.*, United States v. Dentsply Int'l, Inc., 399 F.3d 181, 187 (3d Cir. 2005) ("monopoly power may be inferred from a predominant share of the market"); United States v. Microsoft Corp., 253 F.3d 34, 51 (D.C. Cir.), *cert. denied*, 534 U.S. 952 (2001) ("monopoly power may be inferred from a firm's possession of a dominant share of a relevant market that is protected by entry barriers").

[389] *See, e.g.*, Tops Markets, Inc. v. Quality Markets, Inc., 142 F.3d 90, 99 (2d Cir. 1998) ("We cannot be blinded by market share figures and ignore market place realities, such as the relative ease of competitive entry"); United States v. Syufy Enters., 903 F.2d 659, 665-66 (9th Cir. 1990) ("In evaluating monopoly power, it is not market share that counts, but the ability to *maintain* market share.").

[390] *See supra* Section II.A.

[391] IDF 1010-15.

[392] The Initial Decision also identifies a "cluster market" for synchronous DRAM technologies, which contains these four product markets. IDF 1014. In view of our findings regarding the four separate product markets, we need not separately consider the cluster market.

[393] IDF 1016-17. *See* IDF 1017 ("The relevant geographic market for each relevant product market is the world because: buyers of technology typically do not care about the geographic source of technology; technologies tend to be licensed worldwide; technologies tend to flow across national borders; downstream products are produced and used worldwide; and transportation costs of both technology and DRAMs are negligible.").

[394] *See* IDF 1013, 1015 ("Respondent does not challenge Complaint Counsel's product market definitions. Respondent's economic expert . . . testified the 'relevant market is not crucial to understanding competition and market power in this setting.'").

Rambus held over 90 percent of the market share in the relevant markets.[395] JEDEC's standards have been ubiquitous in the computer industry: from 1998 on, the decided majority of DRAMs sold have complied with the JEDEC SDRAM and DDR SDRAM standards.[396] Rambus claims that its patents are necessary to make, use, or sell DRAMs that comply with the JEDEC standards.[397] Courts typically find such a high market share sufficient to infer the existence of monopoly power.[398] The ALJ determined that Rambus possessed monopoly power in the four key technology markets alleged, and Rambus does not dispute his findings in this respect.[399] We reach the same conclusion, and find that Rambus did acquire a monopoly position.

Rambus argues, however, that its monopoly power was not durable because the industry could have switched to alternative technologies relatively easily without incurring significant additional costs. We must therefore determine whether Rambus's deceptive and exclusionary conduct in the standard-setting context enabled Rambus to acquire durable monopoly power. We address that question below, as part of our broader analysis of causation issues.[400]

### C. Causation

Having concluded that Rambus engaged in a deceptive course of conduct that constituted exclusionary conduct, and having found that Rambus acquired a monopoly position in the

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[395] *See* IDF 1020-21; CX 1386 at 4 ("We are on the cusp of achieving our original BHAG [Big Hairy Audacious Goal] • SDRAM + DDR + RDRAM > > 90% of the DRAM market"); CX 2112 at 310-11 (deposition transcript at 309-10) (Mooring FTC Dep.); McAfee, Tr. 7430 (testifying that the percentage of worldwide commercial DRAM production exposed to Rambus's patent claims was "in the upper nineties").

[396] *See* CX 35 at 14-15 ("This JEDEC standardization process creates the structure from which all DRAM designs begin . . . JEDEC is the fulcrum for DRAM standards in Asia, the Americas and Europe").

[397] CX 2067 at 171 (Davidow *Infineon* Dep.) (*in camera*) ("Q. So am I right, then that it's Rambus's position [] that any SDRAM or RDRAM being used in main memory PCs today [January 31, 2001] are covered by their patents? . . . [A.] I would say that it is highly likely that is true."); McAfee, Tr. 7427-28 ("JEDEC standards have dominated the DRAM industry"), 7432-33; Rapp, Tr. 10248-49 (presenting market share statistics).

[398] *See* Eastman Kodak Co. v. Image Technical Servs. 504 U.S. 451, 481 (1992) (80% market share, with no readily available substitutes, sufficient to survive summary judgment on the possession of monopoly power); United States v. Grinnell Corp., 384 U.S. 563, 571 (1966) (87% of the relevant market left no doubt that defendants had monopoly power); United States v. E.I. du Pont de Nemours & Co., 351 U.S. 377, 379, 391 (1956) (control of 75% of a relevant market would constitute monopoly power); American Tobacco Co. v. United States, 328 U.S. 781, 797 (1946) (control of over two-thirds of the market is a monopoly).

[399] "Complaint Counsel have demonstrated that Respondent has monopoly power in the relevant markets." IDF at 252; *see also* IDF 1010-15. Rambus's economic expert, Rapp, testified that Rambus possessed market power. Rapp, Tr. 10046 ("[I]t is the case isn't it, that, in your view, Rambus today possesses market power in each of the relevant markets defined by [Complaint Counsel's expert] Professor McAfee? A. Yes.").

[400] *See especially infra* Section IV.C.3.d. (discussion of lock-in).

relevant markets, we turn to the critical issue of causation – *i.e.*, whether Rambus's exclusionary conduct was linked to its monopoly position.

We find that the same evidence establishing that Rambus engaged in exclusionary conduct and that it acquired monopoly power respecting the four key technologies incorporated into JEDEC's SDRAM standards contributes to a *prima facie* showing of a causal link between Rambus's conduct and its power. More specifically, we conclude that the evidence (1) links Rambus's conduct to JEDEC's adoption of SDRAM standards incorporating Rambus's patents and (2) links JEDEC's adoption of those standards to Rambus's acquisition of monopoly power.

1. Link between Rambus's Conduct and JEDEC's Standard-Setting Decisions

Rambus's strategy was to cause JEDEC to adopt SDRAM and DDR SDRAM standards incorporating its patents, and then to charge those practicing the standards royalties of its choosing. Although purpose is not a substitute for effect in a monopolization case, it is well-settled that "[e]vidence of the intent behind the conduct of a monopolist is relevant . . . to the extent it helps us understand the likely effect of the monopolist's conduct."[401] As the Supreme Court explained, "[K]nowledge of intent may help the court to interpret facts and to predict consequences."[402] Thus, we initially infer from the evidence respecting Rambus's purpose that, but for Rambus's deceptive course of conduct, JEDEC either would have excluded Rambus's patented technologies from the JEDEC DRAM standards, or would have demanded RAND assurances, with an opportunity for *ex ante* licensing negotiations. Indeed, the one time that JEDEC members had advance knowledge that a Rambus patent was likely to cover a standard under consideration, the members took deliberate steps to avoid standardizing the Rambus technology.[403]

JEDEC members – DRAM manufacturers and customers – were highly sensitive to costs, and that keeping costs down was a major concern within JEDEC.[404] As a report by Rambus's

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[401] United States v. Microsoft Corp., 253 F.3d 34, 59 (D.C. Cir.), *cert. denied*, 534 U.S. 952 (2001).

[402] Chicago Board of Trade v. United States, 246 U.S. 213, 238 (1918). *See also* United States Football League v. NFL, 842 F.2d 1335, 1359 (2d Cir. 1988) ("Evidence of intent *and* effect helps the trier of fact to evaluate the actual effect of challenged business practices in light of the intent of those who resort to such practices.") (emphasis original).

[403] In March 1997, when NEC proposed a "loop-back" clock system, some members expressed concern that it might be covered by Rambus's '703 patent, the one patent that Rambus had disclosed while it was a member of JEDEC. JX 36 at 7. The JEDEC committee immediately dropped the proposal and turned to consideration of technologies that it believed avoided Rambus's patent. *See* Rhoden, Tr. 527-28; Lee, Tr. 6695-96; CX 368 at 2.

[404] *See, e.g.*, G. Kelley, Tr. 2562 ("The overriding factor on all of my votes on DRAM was low cost"); Bechtelsheim, Tr. 5814 (JEDEC's "overarching goal" was "a cost-effective solution" for memory interfaces); CX 2107 at 136-37 (Oh FTC Dep.) (*in camera*) (avoiding costs, including royalties or fees, was important to

Crisp put it, "Compaq (Dave Wooten) like the others, stressed that price was the major concern for all of their systems. They didn't particularly seem to care if the SDRAMs had 1 or two banks so long as they didn't cost any more than conventional DRAMs . . . Sun echoed the concerns about low cost. They really hammered on that point."[405] More succinctly, Crisp explained, "[T]hey want cheap, cheap, cheap."[406]

JEDEC members considered the potential cost of patents in weighing different alternatives. Witnesses, including representatives from DRAM manufacturers and their major customers, testified that knowledge of patents was an important factor in their decisions as JEDEC members.[407] For example, after testifying that the potential for royalty-bearing patents would have been relevant in analyzing programmable CAS latency and programmable burst length as compared to alternatives, Andreas Bechtelsheim added, "I personally and Sun [Microsystems] as a company would have strongly opposed the use of royalty-bearing elements in an interface patent – in an interface specification."[408] The total cost of payments for Rambus's

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Hyundai); CX 34 at 31 (IBM: "LOW COST!!! (<5% more than [previous generation] DRAM)"); CX 711 at 1 (Crisp e-mail reporting, "Desi [Rhoden of Advanced Memory International (AMI-2)] added that if the SDRAM doesn't cost less than 5% more than [previous generation] DRAM they will not be used"); CX 2383 (Sun letter to JEDEC members stating, "[S]ince we are very cost conscious we are willing to drop features that add too much cost or complexity"); CX 2777 (Micron: "[T]he age old rule for DRAMs still appl[ies]. Customers will take as much performance as we can give them for absolutely no added cost over the previous technology. They will not pay extra for increased DRAM performance."). An October 1994 internal Rambus e-mail summarized, "Our industry is very cost sensitive." CX 5109 at 4.

[405] CX 1708 at 2.

[406] CX 711 at 34 (explaining that "customers are willing to leave performance on the table in exchange for having lower cost systems").

[407] *See, e.g.*, Sussman, Tr. 1417 (Sanyo's JEDEC representative testifying, "If I understood that there was IP on the programmable, I would have voted – changed my direction and voted to take the fixed one."); Landgraf, Tr. 1714 (HP's JEDEC representative testifying that if Rambus had disclosed its patent applications, "If we knew in advance that they were not going to comply with the JEDEC patent policy, we would have voted against it."); G. Kelley, Tr. 2576 (IBM's JEDEC representative noting that "[p]atent issues are a concern on every JEDEC proposal" and that when a technology was considered for the first time "it was especially valuable to have the consideration of patents so that we could possibly avoid them"); Lee, Tr. 6686, 6717 (knowledge of Rambus's patent applications would have caused Micron to oppose on-chip PLL/DLL and dual-edge clocking); *see also* JX 5 at 4 (JEDEC minutes stating, "The important thing is disclosure. If it is known that a company has a patent on a proposal then the Committee will be reluctant to approve it as a standard.").

[408] Bechtelsheim, Tr., 5813-14. JEDEC members' response to Rambus's proprietary RDRAM technology reflected similar cost sensitivity. *See, e.g.*, JX 36 at 7 ("Some Committee members did not feel that the Rambus patent license fee fit the JEDEC requirement of being reasonable."); CX 961 at 1 (September 1997 Intel e-mail to Rambus CEO Tate stating the concern that, for at least the low end of the market, "absolute cost is the critical factor" and alternatives "need not be equivalent performance" and warning that, upon analyzing the royalty obligations attached to RDRAM, the industry would develop alternatives); RX 1482 at 12.

undisclosed patents could amount to several billion dollars,[409] with some individual DRAM manufacturers each paying hundreds of million of dollars.[410] Numbers of this magnitude are not easily overlooked.

Alternative technologies were available when JEDEC chose the Rambus technologies, and could have been substituted for the Rambus technologies had Rambus disclosed its patent position.[411] Some of the major firms in the industry found these alternatives viable, and even preferable.[412] JEDEC members – the principal buyers of the relevant technologies – gave these alternatives serious, searching consideration; in fact, the technologies as to which Rambus subsequently revealed patent claims sometimes were chosen only after prolonged debate.[413]

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[409] *See* McAfee, Tr. 7653-54 (*in camera*) (estimating royalty payments to Rambus of $600 million per year); CX 527 at 1 (*in camera*) (projecting annual Rambus royalty revenue on SDRAM and DDR SDRAM of $2.1 billion dollars by 2005); CX 1391 at 32 (*in camera*) (suggesting that Rambus DRAM royalties could total more than $8 billion over the six years between 2000 and 2005); CX 1401 at 10 (*in camera*) (Rambus business plan projecting that DDR SDRAM royalties in 2005 would range from several hundred million dollars up to as much as $2.5 billion).

[410] *See* Appleton, Tr. 6390-92 (Rambus's requested royalty would cost Micron hundreds of millions of dollars; Rambus royalties would be the equivalent of 25-50% of Micron's R&D expenditures).

[411] S*ee, e.g.*, G. Kelley, Tr. 2548-49 and Jacob, Tr. 5370-93 (alternatives to programmable CAS latency); Kellogg, Tr. 5110-11, 5131-32 and Jacob, Tr. 5397-5412 (alternatives to programmable burst length); Jacob, Tr. 5416-38 (alternatives to dual-edge clocking); Jacob, Tr. 5443-58 and Lee, Tr. 6655, 6664-67, 6676-78 (alternatives to on-chip PLL/DLL). *See generally* Bechtelsheim, Tr. 5786 ("in typical design activity one can make any number of choices, including choosing an interface that was not encumbered by a patent or royalty").

[412] For example, Samsung advocated the use of fixed, rather than programmable, CAS latency, JX 10 at 71; Rhoden, Tr. 425-27; Kellogg, Tr. 5099-100, and Cray proposed the use of fuses to set latency, CX 34 at 149, Kellogg, Tr. 5104. For setting burst length, Cray proposed using fuses, CX 34 at 149; Sussman, Tr. 1388-89; Kellogg, Tr. 5103-05, and Mitsubishi proposed using pins. Rhoden, Tr. 430-34; Kellogg, Tr. 5102; JX 10 at 5, 74. Samsung proposed fixed, rather than programmable, burst length. Rhoden, Tr. 425-27; JX 10 at 71. With regard to data acceleration, TI proposed doubling the frequency of a single-edge clock in place of dual-edge clocking. Lee, Tr. 6711-14; CX 371 at 3. As alternatives to on-chip PLL/DLL, Samsung proposed placing a single PLL on the memory controller, Rhoden, Tr, 513-14; Lee, Tr. 6691; JX 31 at 71; IBM proposed using vernier circuits, Kellogg, Tr. 5155; and Micron proposed using what it termed an "echo clock," Lee, Tr. 6655-56; 6664-67; JX 29 at 4, 17-22. Both Micron and Silicon Graphics also presented proposals for using data strobes in place of on-chip DLLs. CX 368 at 1-2, 4; CX 370 at 2-3; Lee, Tr. 6666-67, 6682-83.

[413] As to CAS latency and burst length, NEC/Sanyo's Sussman testified, "I had a lot of arguing to do to get the degree of programmable features into the part." Sussman, Tr. 1380. AMI-2's Rhoden explained that using fuses to set CAS latency and burst length "was one of the options that was considered for a very long time, until we finally settled on the [programmable] register." Rhoden, Tr. 429-30. Subsequently, sentiment for moving to fixed CAS latency and burst length remained strong: the SDRAM Lite task group proposals for reducing the cost of SDRAM included fixed CAS latency and burst length. *See* Rhoden, Tr., 475-76; Lee, Tr. 6626. Indeed, results of the SDRAM Lite survey ballot announced in January 1996 showed consensus support for fixed CAS latency of three and for fixed burst length of four, but no consensus for an additional latency or burst length. *See* Lee, Tr. 6627-32; JX 29 at 13-15.

The ALJ rejected this evidence regarding JEDEC's cost sensitivity and technology debates because, in his opinion, it was based on "the subjective perceptions of JEDEC members at the time," reasoning that while it "may speak to whether JEDEC would have selected a [substitute] technology, it does not go to whether an alternative is equal or superior in objective terms."[414]

The ALJ's analysis misses the point of the causation inquiry. Evidence that a properly-informed JEDEC may have selected a substitute technology suggests a causal link between Rambus's deceptive course of conduct and JEDEC's decision-making process. This evidence – combined with the evidence of Rambus's strategy, JEDEC members' overriding concern with costs, and the magnitude of the potential royalties in the absence of RAND assurances or the opportunity to negotiate *ex ante* – is enough to show that JEDEC's adoption of the SDRAM and DDR SDRAM standards was linked to Rambus's exclusionary conduct.

2. Link Between JEDEC's Standards and Rambus's Monopoly Power

JEDEC's adoption of standards incorporating Rambus's patented technologies is linked to Rambus's monopoly power. More specifically, as previously stated, the record shows: (1) that Rambus claims that its patents are necessary to make, use, or sell DRAMs that comply with the JEDEC standards; (2) that most DRAMs sold complied with the JEDEC SDRAM and DDR

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Dual-edged clocking held only "mixed support" within JEDEC. JX28 at 35 (results of 1995 survey ballot). (This confirms a 1991 report from NEC's Sussman, finding a split between those who preferred high-speed, single-edge clocking and those who preferred dual-edge clocking at lower speeds. *See* Sussman, Tr. 1368-72; CX 20 at 1.) Debate over on-chip PLL/DLL reflected "differing viewpoints," with some JEDEC members preferring to use a data strobe and finding on-chip PLL/DLL unnecessary, but others wanting the latter feature; the result was "a compromise . . . to do both but provide the ability to turn off the DLL." *See* Lee, Tr. 6682-83; Sussman, Tr. 1404 (summarizing the on-chip PLL/DLL debate, "Ten engineers; 12 opinions."). *See also* CX 2713 at 2 and Lee, Tr. 6654 (1997 Micron e-mail arguing to JC 42.3 members that on-chip DLL has "more disadvantages than advantages" and should be eliminated); MacWilliams, Tr. 4918-20 (Intel study found on-chip DLL unnecessary at speeds under consideration).

[414] ID at 317.

SDRAM standards;[415] and (3) that Rambus acquired 90 percent market shares in all four of the relevant markets.[416]

These market results were a natural consequence of DRAM industry attributes. In part, the results reflected the nature and composition of JEDEC, a broad-based organization that included essentially all the DRAM manufacturers and their largest customers.[417] Once JEDEC reached a consensus as to which technologies to standardize, it is hardly surprising that those same manufacturers produced, and those same customers bought, products conforming to the standard they had adopted.[418]

The market results also reflected the nature of the DRAM product itself, which drove standardization in the DRAM industry. DRAMs must interoperate with complementary components, which provided a compelling incentive to develop DRAM specifications that ensured compatibility.[419] JEDEC provided the necessary mechanism for coordinating the evolution of DRAMs and their complements.[420] Moreover, customers desired a commodity

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[415] In each year from 1994 through 2002, products compliant with JEDEC standards captured between 87-97% of DRAM revenues. *See* Rapp, Tr. 10099-100, 10248-49; Prince, Tr. 9020-21; CX 2112 at 310-11 (deposition transcript at 309-10) (Mooring FTC Dep.) (*in camera*). Rambus argues that multiple DRAM standards may and do exist at any given time, but almost without exception, the "multiple standards" in the market have been succeeding generations of JEDEC standards. *See* Rapp, Tr. 10248-49. Only with RDRAM in 2001-02 did any non-JEDEC-compliant DRAMs capture more than 3% of revenues. *Id*. Indeed, customers expressed reluctance to purchase anything other than JEDEC-compliant DRAMs for commodity applications. Rambus President Mooring, for example, testified that HP, Apple, and Sun all told him in 1991 that "we only use memories approved by JEDEC." CX 2054 at 47-48 (Mooring *Infineon* Dep.) (*in camera*). "[I]n the DRAM business, the only standard is JEDEC." CX 2079 at 118 (Mooring *Micron* Dep.) (*in camera*). *See also* Becker, Tr. 1152-53 (Infineon makes only JEDEC-compliant DRAMS because "that's all our customers are willing to buy").

[416] *See supra* Section IV.B.

[417] *See* Rhoden, Tr. 293-94; Peisl, Tr. 4453; JX 18 at 1-3.

[418] *See* Rhoden, Tr. 297-98 ("working with the customer inside an area like JEDEC . . . when everyone agrees, then they have essentially an automatic market . . . basically a presold customer base just by complying and working with the standard"); Macri, Tr. 4596.

[419] *See, e.g.*, Williams, Tr. 763 (Micron's customers "require that they are able to buy products from multiple sources and that these products interoperate, and JEDEC is the body that sets those standards by which there [is] interoperability"); Calvin, Tr. 994; G. Kelley, Tr. 2387-88; Polzin, Tr. 3943-44 ("It was crucial that we had a common standard that would allow interoperability"), 3972; Peisl, Tr. 4382 (standards "enable[] essentially the whole industry to develop products that work together in more or less a predefined manner"), 4386, 4408-10; McAfee, Tr. 7189-90, 11218.

[420] *See, e.g.*, Calvin, Tr. 994; Polzin, Tr. 3946-47 ("JEDEC was the natural forum and process for resolving the numerous differences."); Peisl, Tr. 4410 ("You have to make sure that your part is fully compliant with all the specifications of the other chips. This is why everybody is working towards the JEDEC specification. That's the common denominator."); McAfee, Tr. 11301-02.

DRAM market whereby multiple DRAM suppliers could supply interchangeable DRAMs; standardization made this possible.[421]

These considerations strongly suggest that the market was likely to coalesce around a standardized choice.[422] Joined with the historical record of the predominant market position of DRAMs compliant with the JEDEC standards, these industry attributes support our finding that JEDEC's choice of standards significantly contributed to Rambus's monopoly power.

### 3. Rambus's Claims That The Chain of Causation Was Broken

Rambus claims that its course of conduct and its acquisition of monopoly power cannot be linked for four principal reasons.

#### a. Rambus's Intel Claim

First, Rambus argues (and the ALJ agreed) that Intel's technology choices,[423] not any conduct in which Rambus engaged, caused the monopoly position Rambus enjoyed with respect to SDRAM technologies.[424] If we were to accept this conclusion, implicitly we would be assigning to Complaint Counsel the burden of proving that Rambus's conduct was the *sole* cause of Rambus's monopoly position. This is error as a matter of law.

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[421] *See, e.g.*, Rhoden, Tr. 298-99; Williams, Tr. 763; Becker, Tr. 1152-53 ("[customers like Dell, IBM, and Compaq] want to be able to buy my parts or Samsung's parts or Micron's parts and use them interchangeably, and through the standards process, they get that benefit"); Sussman, Tr. 1328; Landgraf, Tr. 1692-93; G. Kelley, Tr. 2387-88; Heye, Tr. 3641 ("Apple thought it was very, very important to have multiple suppliers"); Polzin, Tr. 3973; Peisl, Tr. 4408-10; Goodman, Tr. 6013; McAfee, Tr. 7225-26; Farmwald, Tr. 8296; CX 1354 at 5 (1999 Tate presentation stating, "Customers want multiple sourced, compatible DRAMs").

[422] *See* McAfee, Tr. 11228-29. Indeed, outside the litigation context, Rambus recognized this very point. *See* CX 533 at 9 (1989 RamBus Business Plan noting "[t]he DRAM industry's penchant for standardization)"; CX 1284 at 28 (1989 RamBus Technology Overview stating, "There is real value in having a world DRAM standard").

[423] In late 1996, Intel announced that its future chipsets – the "gatekeeper" or "traffic cop" components that link CPUs with main memory – would support RDRAM exclusively. *See* IDF 1058; Crisp, Tr. 3432-33; Tabrizi, Tr. 9134-35; RX 1532 at 2. By March 1999, however, Intel determined that "a strategy that puts our chipset and value processor line dependent, solely on Rambus is no longer viable." CX 2527 at 2. In June 1999, Intel announced it might discontinue its exclusive support of RDRAM, and two months later, Intel confirmed that it would also support main memory compliant with JEDEC's SDRAM standard. Tabrizi, Tr. 9201-03; CX 1077; CX 2338 at 57 (*in camera*). By October 1999, Intel informed Rambus that it had "been forced to re-architect its chipset roadmap to accommodate additional SDRAM products." CX 2541 at 2; *see* CX 2540 at 1.

[424] RFF 1538-47; ID at 303-04. Rambus did not raise this argument in its appeal or rebuttal briefs to the Commission.

Exclusionary conduct need not be the exclusive cause of the monopoly position. In an equitable enforcement action, it is sufficient that the exclusionary conduct "reasonably appear[s] capable of making a significant contribution to creating or maintaining monopoly power."[425] As Professors Areeda and Hovenkamp explain:

> [B]ecause monopoly will almost certainly be grounded in part in factors other than a particular exclusionary act, no government seriously concerned about the evil of monopoly would condition its intervention solely on a clear and genuine chain of causation from an exclusionary act to the presence of monopoly.[426]

Further, as the U.S. Court of Appeals for the District of Columbia Circuit reasoned in *Microsoft*, requiring Section 2 plaintiffs "to reconstruct the hypothetical marketplace absent a defendant's anticompetitive conduct would only encourage monopolists to take more and earlier anticompetitive action."[427]

Moreover, the record does not support Rambus's claim as a matter of fact. Intel first announced and then withdrew exclusive support for RDRAM, and RDRAM never became a major factor in the DRAM market.[428] Intel, acting alone, did *not* successfully impart monopoly power on its temporarily anointed choice; nor was the withdrawal of its support the sole reason for the proliferation of SDRAM technologies. Rather, the record shows that JEDEC's standards captured the market. JEDEC adopted standards that included programmable CAS latency and burst length, dual-edged clocking, and on-chip DLL/PLL, and these technologies succeeded. JEDEC did not adopt other aspects of RDRAM, and they became insignificant. Thus, the record shows that JEDEC's adoption made the difference, and significantly contributed to Rambus's acquisition of monopoly power.

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[425] United States v. Microsoft Corp., 253 F.3d 34, 79 (D.C. Cir.), *cert. denied*, 534 U.S. 952 (2001), citing language currently appearing at III AREEDA & HOVENKAMP, ANTITRUST LAW, ¶ 651f at 83-84; *see also* Einer Elhauge, *Defining Better Monopolization Standards*, 56 STAN. L. REV. 253, 331-32 (2003).

[426] III AREEDA & HOVENKAMP, ANTITRUST LAW, ¶ 651f at 83. *See also Microsoft*, 253 F.3d at 79 (finding no case standing for the proposition that "as to § 2 *liability* in an equitable enforcement action, plaintiffs must present direct proof that a defendant's continued monopoly power is precisely attributable to its anticompetitive conduct") (emphasis original).

[427] *Microsoft*, 253 F.3d at 79.

[428] During the period of Intel's exclusive support, RDRAM accounted for .5% (in 1996), 1.3% (in 1997), 1.6% (in 1998), 1.1% (in 1999), and 3% (in 2000) of DRAM revenues. Rapp, Tr. 10248-49. Its share was 12.5% in 2001, *id*. at 10249, and then fell below 10% by 2002. CX 2112 at 309-10 (Mooring FTC Dep.) (*in camera*).

b. Rambus's Inevitability/Superiority Claim

Second, Rambus argues (and the ALJ agreed) that any monopoly power it obtained from the incorporation of its technologies into the JEDEC DRAM standards resulted from the superiority of Rambus's technology, not from its conduct. We also reject this claim. To begin with, Rambus and the ALJ assumed that Complaint Counsel had the burden of proof on this claim. That is error. As noted by Professors Areeda and Hovenkamp:

> In addition to proving [monopoly] power, the plaintiff generally has the burden of pleading, introducing evidence, and presumably proving by a preponderance of the evidence that anticompetitive behavior has contributed significantly to the achievement or maintenance of the monopoly. *The defendant may, of course, introduce its own proof of inevitability, superior skill*, or business justification…."[429]

The court in *Microsoft* essentially reached the same conclusion. There the plaintiff met its threshold burden by showing that Microsoft unlawfully had maintained its monopoly position by "engag[ing] in anticompetitive conduct that reasonably appear[s] capable of making a significant contribution to . . . maintaining monopoly power."[430] The court then inferred causation – ruling, in essence, that the plaintiff had met its burden without a particularized reconstruction of what would have occurred in the but-for world. Rather than requiring the plaintiff "to reconstruct the hypothetical marketplace absent a defendant's anticompetitive conduct," the court explained, "To some degree the defendant is made to suffer the uncertain consequences of its own undesirable conduct."[431]

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[429] III AREEDA & HOVENKAMP, ANTITRUST LAW, ¶ 650c at 69 (emphasis added).

[430] *Microsoft*, 253 F.3d at 79 (citation to Areeda & Hovenkamp treatise omitted).

[431] *Id*. *See also* Morgan v. Ponder, 892 F.2d 1355, 1363 (8th Cir. 1989) ( "[w]e need not determine the exact cause of [plaintiffs's firm's] demise. Nor must plaintiffs systematically eliminate all possible non-predatory causes.") (*dictum*). *Cf*. Hecht v. Pro-Football, Inc., 570 F.2d 982, 991 (D.C. Cir. 1977) (holding that *defendants* bear the burden of proof when they seek to avoid charges of monopolization by asserting that their monopoly power results from natural monopoly).

Rambus argues that in a standard-setting case, the plaintiff "must establish that the standard-setting organization adopted the standard in question, and *would not have done so but for* the misrepresentation or omission." RB at 121, citing II HOVENKAMP ET AL., IP AND ANTITRUST, § 35.5b at 35-40 (emphasis added by Rambus). The treatise, however, only states that such analysis should apply when the SSO has (1) "no policy with respect to intellectual property ownership in the standards they promulgate" or (2) "a history of promulgating standards even when they are aware that the proposer owns intellectual property rights in the standard." *Id*. at 35-40 to 35-41. Neither of those factors is relevant to the question of product superiority. Indeed, when the treatise does discuss what Rambus portrays as the fact pattern – when "a standard would have become dominant anyway in a *de facto* standards competition" and the patent "confers an economic monopoly because of the absence of feasible noninfringing alternatives" – the treatise is silent as to the burden of proof. *Id* at 35-41 to 35-42.

Rambus argues that, even in light of full disclosure, JEDEC still would have standardized Rambus's technologies, because they were superior to all alternatives on a cost/performance basis. We find that the evidence does not establish that Rambus's technologies were superior to all alternatives on a cost/performance basis.[432] Although Complaint Counsel argue that at least six alternative technologies were available in each of the relevant product markets, we focus, with one exception,[433] on the technologies that Rambus's economic expert, Richard Rapp, analyzed. Because Rambus has failed to prove that its patented technologies were superior to all of these technologies, we need not examine additional alternatives.[434]

***Latency Technology.*** As discussed above,[435] latency technologies control the length of time between the memory's receipt of a data request and its release of responsive data.[436] The JEDEC DRAM standards incorporated programmable CAS latency technology, which Rambus now claims is covered by its patents. Alternatives available in the early 1990s included fixed CAS latency, blowing a fuse on a DRAM, and dedicated pins.

Rambus compares the variable cost of programmable CAS latency with the variable cost of each of these three alternative technologies. Based on this comparison, Rambus concludes that the alternatives were more costly even when Rambus's royalties were taken into

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[432] Unless stated otherwise, all subsequent references in this section to the superiority of a given technology reflect an overall assessment based on a mix of cost and performance characteristics.

[433] Rapp did not analyze the cost information about toggle mode (a possible alternative to Rambus's dual-edge clocking) because he concluded that this technology's performance suffered above certain clock speeds. Rapp, Tr. 9856-57. We examine toggle mode because Rapp failed to explain why, as an economic expert, he made a judgment based on engineering attributes of this technology, but did not evaluate the performance implications of other technologies.

[434] Rapp excluded two categories of alternatives from consideration on dubious grounds. First, he did not consider any alternative that Donald Soderman, one of Rambus's engineering experts, identified as potentially subject to a Rambus patent. Rapp, Tr. 9831, 10215, 10217. The mere identification of possible patent infringement by Rambus's own expert witness – an engineer who lacked legal training – is an insufficient reason to exclude an alternative technology.

Second, Rapp excluded alternatives that Complaint Counsel's economic expert, McAfee, failed to find commercially viable. Rapp, Tr. 9810, 9841. In only one instance, however, did McAfee actually determine that an alternative was not commercially viable. In other instances, he merely concluded that he lacked sufficient information to reach a judgment one way or the other, or else stated that he was "agnostic" as to an alternative's commercial viability. *See* McAfee, Tr. 7362-63, 7372, 7385, 11354-56. Given that Rambus bears the burden of proving product superiority, McAfee's statements did not justify Rapp's decision to omit such alternatives from his comparison.

[435] *See supra* Section II.A.3.a.

[436] McAfee, Tr. 7348; Horowitz, Tr. 8529-30.

consideration.[437] However, Rambus's cost estimates are unreliable for at least two reasons. First, Rambus assumes, without demonstrating, that alternatives to programmable CAS latency would have provided support for three latency values.[438] Considerable evidence indicates that JEDEC would have required only one or two latency values if it had standardized one of the alternatives.[439] Second, Rambus fails to take account of ways in which the alternative technologies may have reduced costs.[440]

Fixed CAS Latency: A fixed CAS latency part sets a single latency value.[441] Rambus did not present any evidence that this technology had any performance issues. Nevertheless, Rambus argues that fixed CAS latency was not a viable alternative, estimating that it would have increased per-unit costs by three cents for reduced yields and two cents for inventory (while simultaneously reducing per-unit costs by one cent for improved testing).[442] Rambus potentially overstates the inventory costs because it assumes that three latencies would have been supported – a premise that, as discussed above, is not established by the evidence.[443] Rambus also fails to

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[437] *See* Rapp, Tr. 9813-18, 9831-33.

[438] *See* Geilhufe, Tr. 9578. Rambus's other engineering expert presented general testimony that different latencies provided optimal performance with different bus speeds and that users benefitted from the flexibility afforded by programmable CAS latency. Soderman, Tr. 9347, 9350-51.

[439] *See* McAfee, Tr. 11245-48. The record establishes that SDRAMs primarily used only two CAS latency values in main memory. *See* Rhoden, Tr. 394; Lee, Tr. 11004-05, 11063-67, 11097 (testifying that while Micron did produce a part that used a third CAS latency value, this was a small-volume part targeted to the graphics industry). JEDEC standards frequently have required only two latency values. IDF at 1140. In 1991, Samsung advocated a fixed CAS latency of two. JX 10 at 71; Rhoden, Tr. 425-27; Kellogg, Tr. 5099-5101. In 1995, discussion of SDRAM Lite within JEDEC focused on supporting one or two values. Lee, Tr. 6629-32, 11007-08.

[440] Complaint Counsel's engineering expert, Professor Bruce Jacob, testified that shifting to alternatives for programmable CAS latency would have enabled partial elimination of the mode register. *See* Jacob, Tr. 5376-77, 5384, 5388, 5593-95. One of Rambus's engineering experts acknowledged that this simplification could have reduced costs. *See* Soderman, Tr. 9419, 9515.

[441] Jacob, Tr. 5371.

[442] IDF at 1161-62.

[443] Using two latencies, instead of three, would have reduced inventory cost by one cent, which means that the total variable cost increase for this technology would have been three cents. Moreover, according to Complaint Counsel's engineering expert, some manufacturers used inventory systems that would have supported the use of fixed CAS latency without any cost increase. Jacob, Tr. 5592-93 (some manufacturers already assigned different part numbers to different latencies).

consider any factors that might have improved yield,[444] even though its expert's testimony indicated that yield problems tended to be solved "very quickly."[445]

Blowing a Fuse on DRAM: Latency parts can include two CAS latency circuits, each of which can set a different latency value and has a fuse attached.[446] DRAM manufacturers can apply electric or laser technology to blow one of the fuses and prevent the use of the associated latency circuit.[447] Once blown, the DRAM manufacturer would have a fixed latency part with the desired latency value.[448] Rambus's engineering experts testified that electrically-blown fuses were less reliable than laser-blown fuses.[449] However, witnesses from Micron, IBM, and Infineon all testified that their companies used electric fuse-blowing technology.[450]

Rambus argues that programmable CAS latency was superior, in terms of both cost and performance, to setting CAS latency by blowing fuses.[451] As discussed above, Rambus has failed to establish the need to support three latency values or to demonstrate its predicted yield cost increase. Rambus also failed to rebut the testimony of Complaint Counsel's engineering expert, Professor Bruce Jacob, that computer system OEMs themselves could blow the electric fuses, enabling the DRAM manufacturers to sell a single part,[452] thereby holding down inventory costs.

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[444] *See* Geilhufe, Tr. 9577-78.

[445] While explaining how the cost of a DRAM could fall approximately 90% in 12 to15 months, Geilhufe stated that engineers "solve yield problems very quickly. You know, hundreds of engineers work on what is causing yield problems. So we get down the learning curve very, very quickly." *Id.* at 9586-87. *See also* Lee, Tr. 11013 (testimony by Micron's director of advanced technology and strategic marketing that fixed CAS latency parts were less complex than programmable CAS latency and therefore would have improved yields).

[446] Jacob, Tr. 5378-80.

[447] *Id.*

[448] Soderman, Tr. 9354; Geilhufe, Tr. 9585-86.

[449] Soderman, Tr. 9356-57; Geilhufe, Tr. 9581-82 (Intel discontinued using electric fuses on certain products for reliability reasons).

[450] *See* Lee, Tr. 11022, 11170 (*in camera*) (Micron had been using such fuses since 1989 and included a substantial number in its SDRAM products); Kellogg, Tr. 5130; Soderman, Tr. 9525-26 (*in camera*); *see also* Jacob, Tr. 5595-96.

[451] Geilhufe testified that this alternative to programmable CAS latency would have increased per-unit costs by three cents for reduced yield, two cents for inventory (covering three latency values), and one cent for certain testing. Geilhufe, Tr. 9584-86, 9589. *See also* Soderman, Tr. 9354.

[452] *See* Jacob, Tr. 5379-81.

Dedicated Pins: Dedicated pins can determine latency during DRAM operation.[453] A single dedicated pin can store two CAS latency values, setting one CAS latency under a high voltage and the other latency under a low voltage.[454]

Rambus argues that programmable CAS latency enjoyed cost and performance advantages over dedicated pins. The record does not establish this argument. First, Rambus again fails to show that any alternative to programmable CAS latency would have had to support three latency values.[455] As discussed above, numerous witnesses disagreed with Rambus on this point. Rambus also fails to rebut testimony that, under most circumstances, the implementation of dedicated pins might have been considerably more cost-effective than Geilhufe's predictions.[456]

In terms of performance, Rambus's engineering expert testified that implementing dedicated pins would have required additional wiring and "quite possibl[y]" could have created a "noise glitch."[457] However, IBM's engineer, Mark Kellogg, testified that such wiring would not have been necessary;[458] and the chief platform architect of Advanced Micro Devices (AMD), Steve Polzin, testified that pin-based solutions "probably could have been made to work just fine."[459] Rambus does not demonstrate that its contrary assertions deserve greater weight.

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[453] Jacob, Tr. 5386-87; Soderman, Tr. 9463.

[454] *See* Jacob, Tr. 5386-87; Polzin, Tr. 3991-92. Rambus's engineering expert agreed that two latencies can be supported with a single pin. Soderman, Tr. 9463.

[455] Geilhufe testified that the use of dedicated pins would have increased per-unit costs by four cents, reflecting the fact that four dedicated pins would have been required to replace the range of latency values available with programmable CAS latency. Geilhufe, Tr. 9590. An alternative that supported two latency values would have required the addition of at most two pins (given that pins must be added in pairs). *See generally* Polzin, Tr. 3991-92 (use of pins to set latency would "[c]ertainly" be "no more costly" than programmable CAS latency).

[456] According to both Jacob and Lee, many JEDEC-compliant configurations included pins that served no existing function and could be used to set latency. Jacob, Tr. 5387, 11106 ("[n]early all" JEDEC pin-out diagrams had two extra pins available" and "most" had two or more); Lee, Tr. 11030, 11037 (extra pins "almost always" provided); CX 234 at 80-142. If JEDEC had used these extra pins to set latency, there would have been no cost increase for this alternative to programmable CAS latency. Geilhufe's counter-testimony was limited; he argued only that extra pins were unavailable "in the highest density cases." Geilhufe, Tr. 9722-23.

[457] Soderman, Tr. 9361-62.

[458] Kellogg, Tr. 5126-27.

[459] Polzin, Tr. 3991-92.

***Burst Length Technology.*** As discussed above,[460] burst length technology controls the amount of data transferred between the CPU and memory in each transmission. The JEDEC DRAM standards adopted programmable burst length technology, which Rambus now claims is covered by its patents.

Rambus's economic expert, Rapp, analyzed the costs associated with two alternatives to programmable burst length: fixed burst length and burst terminate commands. Rambus claims that programmable burst length was superior to any alternative because it allowed DRAM users to use one part for different types of machines that required different burst lengths, providing important flexibility.[461] However, Rambus assumes that JEDEC would have required more than two burst length values if it had adopted an alternative. The record does not establish that point.[462] Rambus has not shown that additional burst length flexibility was critical to DRAM technology.[463]

Fixed Burst Length: A fixed burst length part sets a single burst length.[464] Rambus argues that fixed burst length technology was not a cost-effective alternative to programmable burst length. According to Rambus, the use of fixed burst length would have increased inventory costs by three cents per unit, while decreasing certain test costs by one cent.[465] However, Geilhufe's inventory cost estimate assumed that four burst length values would have been provided.[466] If, instead, he had assumed that only two burst lengths would have been supported,

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[460] *See supra* Section II.A.3.b.

[461] *See* Soderman, Tr. 9368-70; G. Kelley, Tr. 2550-51 ("The programmable [burst length] feature allowing you to make that selection when the PC or computer powered up was a nice feature because it allowed you to use devices that were common from multiple suppliers, put them into many different types of machines. . . . One part number fits many applications.").

[462] For example, Intel only used a burst length of four. Polzin, Tr. 3994. AMD, another microprocessor manufacturer, designed its microprocessors based on a single burst length of eight. *Id.*; *see also* Lee, Tr. 11048-54, 11095. JEDEC's preliminary specification for DDR2 SDRAM required only a burst length value of four, Macri, Tr. 4673-74, but subsequently was amended to include a burst length of eight to accommodate AMD. *See* Polzin, Tr. 3994; Lee, Tr. 11048-54, 11095.

[463] JEDEC required burst lengths of four and eight when it first published the SDRAM standard in 1993. *See* JX 56 at 114; Williams, Tr. 801-03; Lee, Tr. 11013-14. Ten years later, the proposed specification for DDR2 SDRAM required the same two burst length values. *See* RX 2099-14 at 21; RX 2099-39 at 20; Soderman, Tr. 9369; Rhoden, Tr. 411-12.

[464] Jacob, Tr. 5398-99.

[465] Geilhufe, Tr. 9593-96.

[466] *See* Geilhufe, Tr. 9595.

his entire projected cost increase would have disappeared. Geilhufe also failed to consider cost savings that would have resulted from partial elimination of the mode register.[467]

Burst Terminate Commands: Burst terminate command technology uses long, fixed burst lengths that can be terminated by the memory controller if a shorter burst length is desired.[468] Rambus argues that this technology was not a viable alternative because it could support only a narrow range of burst lengths and therefore would have limited DRAM performance.[469] We are unconvinced. As noted above, Rambus has failed to establish that JEDEC likely would have required more than the two burst lengths supportable with burst terminate commands.

Rambus also argues that the burst terminate command technology causes system inefficiencies.[470] However, several witnesses questioned the significance of these inefficiencies.[471] Furthermore, those witnesses explained that the problems would have been minimized, or avoided, by supporting just two burst length values – such as four and eight.[472] On this record, Rambus has failed to demonstrate serious performance issues with burst terminate command technology.[473]

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[467] *See* Jacob, Tr. 5401-10, 5593-95 (either fixed burst length or a burst terminate command would have enabled elimination of part of the mode register and the circuitry required to initialize it).

[468] Jacob, Tr. 5409-10.

[469] Soderman, Tr. 9377 (implementation of burst terminate in DDR2 SDRAM was limited because it could support only burst length values of four and eight); Geilhufe, Tr. 9598 (questioning whether a burst terminate command could support a burst length value of one).

[470] *See* Soderman, Tr. 9374-76 (a burst terminate command causes inefficiencies when a read burst interrupts a write burst or vice versa); Polzin, Tr. 4038-40; CX 392 at 5; CX 415 at 10 ("an internal device timing nightmare").

[471] *See* Jacob, Tr. 5411 (problem not very significant), 5604-06 (might affect bus efficiency by up to 10-15% in a "hypothetical worst case situation[]"), 11109-10 (type of inefficiency at issue is common and inherent in the DDR protocol).

[472] *See* Jacob, Tr. 11142-46; Macri, Tr. 4774-76 (*in camera*) (limiting interruptions to a precise place and under precise conditions makes burst terminate commands "much easier"; "there's a slight burden to the designer, but, you know, in the big scheme of things, this is a trivial thing . . . .); RX 2099-39 at 20, 63. Even Rambus's engineering expert acknowledged that limiting burst terminate commands to specific conditions avoids timing problems. Soderman, Tr. 9377.

[473] Rambus acknowledges that use of burst terminate commands would not have increased costs. *See* Rapp, Tr. 9826.

***Data Acceleration Technology.*** As discussed above,[474] data acceleration technology determines the speed at which data are transmitted between the CPU and memory. JEDEC's DDR SDRAM and DDR2 SDRAM standards adopted dual-edge clocking technology – a technology Rambus now claims is covered by its patents.

Interleaving ranks on the module, double clock frequency, and toggle mode were some of the alternatives to dual-edge clocking considered by JEDEC. Rambus argues that all three of these alternatives had significant cost and performance limitations. We agree that interleaving ranks on the module had such limitations. However, Rambus has not adequately supported is conclusions regarding double clock frequency and toggle mode.

Interleaving Ranks on the Module: DRAM chips on the memory module can be partitioned into two separate groups that operate on independent system clock signals.[475] This approach – known as interleaving ranks on the module – can double the rate at which data are transmitted between the CPU and memory.[476]

Rambus argues that dual-edge clocking enjoyed performance and cost advantages over this alternative. Rambus cites evidence that both Intel and AMD found signal integrity problems during preliminary evaluations of the interleaving-ranks technology.[477] Complaint Counsel do not rebut this evidence. Rambus's engineering expert testified that this alternative offered less flexible memory increments and was not appropriate for every application.[478] Complaint Counsel offer only a partial rebuttal. The record also shows that interleaving ranks would have resulted in increased costs because it would have required additional technology and hardware.[479] Complaint Counsel again fail to rebut the evidence. Finally, Kentron in 1999 informed JEDEC that it had a patent pending on this technology.[480] Complaint Counsel's economic expert, McAfee, acknowledged that this technology might require royalty payments.[481]

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[474] *See supra* Section II.A.3.c.

[475] Jacob, Tr. 5426-27.

[476] *Id.*

[477] *See* RX 1976 at 49 (*in camera*); Polzin, Tr. 4035-36.

[478] Soderman, Tr. 9389-91.

[479] Soderman, Tr. 9389-91; Goodman, Tr. 6082. Geilhufe testified that the necessary hardware would have increased costs by 25 cents per DRAM. Geilhufe, Tr. 9605-06; *see also* Goodman, Tr. 6046-47, 6083 (each module would have required eight switches at $1 per switch).

[480] *See* CX 150 at 110.

[481] *See* McAfee, Tr. 7404-05.

Based on the totality of the evidence, we find that Rambus has established the superiority of dual-edge clocking over this particular technology.[482]

Double Clock Frequency: Double clock frequency involves operating a single-edge clock at twice the frequency of a dual-edge clock.[483] Rambus has failed to demonstrate that this technology was an unacceptable alternative to dual-edge clocking.

Rambus argues that double clock frequency raises clock distribution problems,[484] requires that the internal circuitry operate at twice the speed of a dual-edge clock,[485] and presents electromagnetic interference concerns.[486] However, these performance concerns were rebutted by Micron's Lee, IBM's Kellogg, and Complaint Counsel's expert witness, Jacob.[487] Other testimony portrayed double clock frequency as a technologically satisfactory alternative to dual-edge clocking.[488] TI clearly found double clock frequency desirable: in 1997 it proposed that JEDEC adopt double clock frequency for its standards.[489]

Rambus's expert testified that double clock frequency would increase per-unit costs by 28 cents,[490] including 24 cents for a clock on the dual in-line memory module (DIMM), which he believed would be necessary.[491] However, the record does not support Rambus's assertion that

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[482] Because we conclude that Rambus has not established the superiority of dual-edge clocking over double clock frequency and toggle mode, however, a showing of superiority over interleaving ranks matters little. Absent a sufficient showing regarding the remaining alternatives, Rambus has not demonstrated that its monopoly power resulted from the superiority of its technology, rather than from its failure to disclose its patent position.

[483] Jacob, Tr. 5433-34.

[484] Soderman, Tr. 9393-94.

[485] Soderman, Tr. 9394-95.

[486] Soderman, Tr. 9395; 9500-01 (asserting that this interference might breach Federal Communications Commission guidelines).

[487] *See* Jacob, Tr. 5433-34, 11115, 11128-29 (slightly reducing voltage mitigates the interference problem); Lee, Tr. 11039-40; Kellogg, Tr. 5182-83 (engineers reduce electromagnetic interference over time).

[488] *See* Kellogg, Tr. 5182, 5184-85; Macri, Tr. 4779-80 (*in camera*) (identifying a "huge" benefit from single-edge clocking).

[489] *See* Lee, Tr. 6711-14; CX 371 at 3.

[490] Geilhufe, Tr. 9610.

[491] Geilhufe, Tr. 9609-10 (speaking in terms of "on-DIMM clock circuitry, possibly on-DIMM PLL/DLL"), 9715 (speaking in terms of an "[o]n-DIMM PLL or DLL circuit, maybe more than a PLL/DLL").

an on-DIMM clock would be needed.[492] Moreover, considerable evidence suggests that Rambus's estimates for the cost of an on-DIMM clock are unreliable.[493] Finally, Rambus fails to consider design, construction, and testing cost savings that would have resulted from substituting a single-edge clock for Rambus's dual-edge clock.[494]

Toggle Mode: Toggle mode was designed by IBM and uses synchronous technology for outputs but asynchronous technology for inputs.[495] JEDEC considered toggle mode in 1990 and 1991.[496] Rambus's contention that IBM's asynchronous design could not achieve the same performance as synchronous technology[497] was contradicted by other evidence.[498] Rambus's

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[492] Geilhufe neither spoke to anyone to confirm the assumption, nor conducted his own timing analysis. Geilhufe, Tr. 9715, 9729. In contrast, a July 28, 1997 TI proposal for using a high-frequency clock made no mention of an on-DIMM PLL/DLL. *See* CX 371. According to Micron's Lee, this proposal would have required "some changes to the bus topology," but not the addition of clock circuitry or a DLL to the module, and "would not have any additional cost over what we were doing." Lee, Tr. 6713-14, 11040. Indeed, Rambus's other engineering expert, Soderman, did *not* claim that on-DIMM clock circuitry would be needed. *See* Soderman, Tr. 9393-95.

[493] Geilhufe testified that an on-DIMM clock costs $3.80 per module (which, allocated over 16 DRAMs, increases cost 24 cents per unit). Geilhufe, Tr. 9606, 9609-10. Geilhufe acknowledged that 16 DRAMs was "the smallest number of units" over which the cost of on-DIMM clock circuit could be allocated. Geilhufe, Tr. 9605-06. For computers with more than 16 DRAMS, this calculation would overstate the clock-circuitry cost per DRAM.

On cross-examination, Geilhufe was shown a document stating that a Kentron PLL circuit cost $2, rather than the $3.80 that he had assumed. Geilhufe acknowledged that he had unsuccessfully sought cost information about the Kentron PLL. *See* CX 2613 at 7; Geilhufe, Tr. 9718-19. Kentron's CEO, Robert Goodman, stated that a standard PLL costs around $1, Goodman, Tr. 6049. Lee testified that Micron pays only 90 cents for PLLs used on register memory modules. Lee, Tr. 11179 (*in camera*); *see also id.* at 11180-81 (*in camera*) (mounting would add further cost but would be "much less" than the cost of the PLL itself). Geilhufe testified that he "did not review specifically the costs for register [memory modules]," but he did not explain why he had not done so. Geilhufe, Tr. 9719. Rambus seeks to dismiss the PLL cost data by suggesting that the Micron PLLs might not operate at the appropriate frequency, but fails to demonstrate that this was so.

[494] *See* Jacob, Tr. 5420-25, 5433-34.

[495] *See* G. Kelley, Tr. 2514; Jacob, Tr. 5608; CX 34 at 32. With asynchronous technology, the internal clock on each DRAM is not coordinated with the computer system clock. *See* IDF 284; Rhoden, Tr. 368. In contrast, operations in DRAMs that use synchronous technology are coordinated with the system clock, which facilitates rapid communication between the CPU and memory. *See supra* note 14.

[496] *See* CX 251 at 1; CX 314 at 1; CX 315 at 1-3; CX 318 at 1.

[497] *See* Soderman, Tr. 9398-99.

[498] *See* Jacob, Tr. 5417. Rambus introduced evidence that an IBM researcher had described toggle mode as "very big, very hot, and very nonstandard," which are "disastrous" attributes "in the commodity market." *See* RX 2099-7 at 16; Soderman, Tr. 9399-9400. Rambus omits that the researcher also found toggle mode "very fast" and, for some purposes, desirable. *See* RX 2099-7 at 16. All of the researcher's conclusions were confined to the "cumulative effect" of combining toggle mode with a specific "low multibit piecepart architecture" and did not

engineering expert also testified that the toggle mode alternative would increase per-unit costs by ten cents due to reduced yields and by two cents for design costs and an additional pin.[499] As mentioned above, Rambus's same expert testified that engineers "solve yield problems very quickly,"[500] which casts doubt on this predicted yield cost increase.

***Clock Synchronization Technology.*** As discussed above,[501] clock synchronization technology coordinates the timing of a computer system clock with the internal clock in each DRAM. JEDEC's DDR SDRAM and DDR2 SDRAM standards adopted technology that uses on-chip PLL/DLL circuits to align more closely the timing of the two clocks. Rambus now claims that its patents cover on-chip PLL/DLL as implemented in JEDEC-compliant products.

Rapp analyzed four alternatives to on-chip PLL/DLL technology: placing DLL circuits on the memory controller; placing DLL circuits on the memory module; using vernier circuits instead of on-chip PLL/DLL circuits; and relying on the DQS strobe rather than the system clock to align timing.[502] Rambus presents scant evidence on the cost or performance limitations of placing DLL circuits on the memory controller or the module, and therefore fails to meet its burden of demonstrating the superiority of its on-chip PLL/DLL technology. Rambus presents slightly more evidence regarding the performance limitations of vernier circuits, but not enough to sustain its burden of proof. The record as to possible performance limitations of the DQS strobe is mixed.

DLL on the Memory Controller: One alternative to on-chip PLL/DLL involves placing a single DLL circuit on the memory controller to synchronize the DRAM's internal clock with the system clock.[503] Rambus presented no cost evidence relating to this alternative, but it did present expert engineering testimony as to potential performance limitations.[504] Complaint Counsel's expert provided equally plausible rebuttal testimony as to performance, and also identified cost advantages from placing the DLL on the memory controller.[505] Other evidence reflected

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extend to toggle mode more generally. *See id*.

[499] Geilhufe, Tr. 9562-64, 9610-12.

[500] Geilhufe, Tr. 9587.

[501] *See supra* Section II.A.3.d.

[502] *See* Rapp, Tr. 9841-42.

[503] *See* Jacob, Tr. 5445.

[504] Soderman testified that DLL circuits on the memory controller fail to address timing differences among individual DRAMs and therefore impair high-speed performance. *See* Soderman, Tr. 9405-06.

[505] *See* Jacob, Tr. 5446-47 (placing the DLL on the memory controller could potentially eliminate outbound, inbound, and return delays, and thereby enable operation at higher rates of speed than on-chip DLLs;

contemporaneous beliefs that this alternative was workable and desirable. For example, in March 1996, Samsung presented a proposal to JEDEC that involved removing the PLL circuit from the DRAM chip and placing it on the memory controller.[506] In light of the evidence as a whole, Rambus has not carried its burden with respect to this alternative.

DLL on the Module: Another alternative to on-chip PLL/DLLs involves placing one or more DLL circuits on the memory module to synchronize the internal clock on each DRAM with the system clock. Rambus argues that DLLs on the module fail to address timing differences among individual DRAMs,[507] but Jacob countered that DLLs would account for internal delay.[508]

Rambus estimates that an on-DIMM DLL would cost $3.80.[509] We find that Rambus has failed to adequately support this estimate for the same reasons described above with respect to its estimate of the cost of double clock frequency.[510] Rambus's own economic expert assigned no cost to this alternative to on-chip PLL/DLL because he found a "paucity . . . of information."[511] Although Rambus's expert was certain there would be some additional costs, he determined that "it seemed sensible . . . to simply assume there would be no cost penalty" for purposes of his calculations.[512]

Vernier Circuits: Verniers are a type of circuit that – similarly to PLLs and DLLs – can be placed on a DRAM.[513] Vernier circuits introduce a fixed-amount delay into the DRAM's internal clock to synchronize that clock with the system clock.[514] Rambus claims that vernier

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placing the DLL on the memory controller also would lower testing and manufacturing costs and reduce the power consumption of DDR SDRAMs).

[506] *See* JX 31 at 71; Rhoden, Tr. 513-514; Lee, Tr. 6691.

[507] Soderman, Tr. 9406-10.

[508] Jacob, Tr. 5449.

[509] *See* Geilhufe, Tr. 9613. Both Jacob and Geilhufe testified that on-module DLLs would reduce other costs. *See* Jacob, Tr. 5450 (on-module DLLs reduce DRAM power consumption, costs, and design time); Geilhufe, Tr. 9612-13.

[510] *See supra* note 493.

[511] *See* Rapp, Tr. 9848.

[512] *Id.* at 9878, 10228 (it "seemed fairer in some sense to assume zero").

[513] *See* Jacob, Tr. 5450-51.

[514] *Id.*

circuits do not perform well enough to be viable alternatives to on-chip PLL/DLL.[515] However, several witnesses testified as to the advantages of vernier circuits.[516]

Rambus notes that the SyncLink consortium considered designing the SLDRAM chip using verniers, without PLLs or DLLs on the DRAM, but ultimately included both verniers *and* DLLs on the DRAM.[517] Rambus argues that this example demonstrates that verniers were not viable alternatives to on-chip DLL/PLL, but the record offers competing explanations for why Synclink included DLLs in SLDRAM.[518]

Rambus further asserts that Micron and SLDRAM hold patents that cover the use of verniers,[519] but provides no element-by-element analysis – indeed, no evidence beyond the bare text of the patents – to support this contention.[520] Rambus makes no argument about the implications of these patents for the viability of vernier circuits as an alternative to on-chip DLL/PLL.

DQS Strobe: A DQS strobe, also referred to as a data strobe, signals to the memory controller the timing of data capture.[521] In doing so, the DQS strobe purportedly makes it unnecessary to align the internal clock with the system clock.[522] Rambus presented no cost evidence relating to this alternative technology, but claims that DQS strobes are insufficient for

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[515] *See* RFF 1103-11.

[516] Complaint Counsel's expert stated that verniers potentially could eliminate outbound, internal, and return delays, Jacob, Tr. 5451, and that periodic recalibrations could compensate for fluctuations in temperature and voltage. *Id*. at 5450-53. IBM viewed verniers as the optimal solution for data capture purposes; IBM implemented verniers on a memory card and promoted the use of verniers at JEDEC meetings. *See* Kellogg, Tr. 5168, 5157, 5153-54. Micron's advanced technology director testified that he had considered verniers to be an acceptable alternative to on-chip DLLs in the 1996-97 time frame. Lee, Tr. 6676-78. A March 1997 VLSI presentation to JEDEC included the use of verniers. JX 36 at 7, 58, 64.

[517] *See* RX 2099-43 at 158; Soderman, Tr. 9412-14.

[518] *Compare* Soderman, Tr. 9414-15 (DLLs were included "to provide a stable reference for input sampling d[el]ay lines" (describing RX 2099-11 at 5)) *with* Jacob, Tr. 5620-21 *and* Lee, Tr. 11044-46 (DLLs were included to provide tight timing on the bus, not to assist in data capture), 11092.

[519] *See* RFF 1105, 1111.

[520] *See* RFF 1111 (citing RX 1701; RX 1479).

[521] Jacob, Tr. 5456-57; Kellogg, Tr. 5158-59.

[522] *See* Jacob, Tr. 5456-57; Lee, Tr. 6681-83.

high speed performance.[523] The record contains conflicting evidence, however, suggesting that most JEDEC members believed this technology offered adequate performance.[524] Indeed, DQS strobes are part of the DDR SDRAM standard and were included in proposed specifications for DDR2 SDRAM.[525]

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We conclude that Rambus has failed to meet its burden of demonstrating that JEDEC would have standardized Rambus's technologies even if Rambus had disclosed its patent position. With regard to performance attributes, the testimony of Rambus's experts was offset by conflicting testimony from Complaint Counsel's experts, which called into question the significance of Rambus's performance concerns. In many instances, testimony from JEDEC members and evidence of their prior actions in sponsoring the alternative technologies substantially buttressed Complaint Counsel's case.

With regard to costs, Rambus failed to demonstrate that alternatives would have been more expensive. Rambus's economics expert, Rapp, compared the added variable costs associated with the alternatives, based on Geilhufe's cost estimates, to the costs of paying royalties for Rambus's patented technologies. Rapp testified that the least costly alternatives would add .82 percent to the selling price of SDRAM and 5.65 percent to the selling price of DDR SDRAM.[526] He concluded that these costs exceeded Rambus royalties of .75 percent of selling price for SDRAM and 3.5 percent for DDR SDRAM.

Rapp's calculations are fraught with uncertainty and potential for error. They are based on Geilhufe's admittedly imprecise cost estimates. Geilhufe acknowledged that his cost

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[523] *See, e.g.*, Soderman, Tr. 9415-17; RX 1040 (e-mail prepared by HP JEDEC representative Hans Wiggers explaining his preference for using DLLs at high speeds, in response to a message entitled, "Death to DLLs"); RX 1086 at 1 (*in camera*).

[524] *See* Lee, Tr. 6682-83; Kellogg, Tr. 5158-59; CX 368 (Micron proposal that JEDEC standardize DQS strobes in DDR SDRAM without DLLs); CX 370 (Silicon Graphics proposal that JEDEC standardize data strobes without DLLs); RX 911 at 3 (SyncLink's design included a data strobe); CX 711 at 72 (noting Hyundai's belief that strobes eliminate need for PLLs/DLLs); *cf.* Jacob, Tr. 5456-57 (presenting DQS strobe alternative).

[525] JX 57 at 5; RX 2099-14 at 3; RX 2099-39 at 5. On-chip DLLs can be disabled in DDR SDRAM but are needed for normal DDR operation. *See* Lee, Tr. 6680-81, 6683; CX 234 at 176; JX 57 at 5, 16.

[526] Rapp, Tr. 9831-32, 9850-54. To compare the dollar figures calculated for cost increases with the percentage figures used in stating Rambus's royalties, Rapp projected an average selling price over the expected lifetimes of the products, calculating an average selling price of $4.87 for SDRAM and $5.13 for DDR SDRAM. *Id.* at 9816-17, 9845. Rapp then translated the increased variable costs of the alternatives into a percentage of average selling price. *Id.* at 9816-17, 9845.

estimates were approximations and he assigned them a sizeable 25 percent margin of error.[527] Yet a 25 percent reduction of Rapp's estimate of the least-costly alternative to SDRAM would bring that estimate well below the level of SDRAM royalties.[528] Moreover, Geilhufe drew many of his estimates from personal experience, without verification by actual cost data or substantiation by supporting record evidence.[529] As to DDR SDRAM, Rapp had to premise his comparisons on projections of future DRAM selling prices and sales volumes.[530]

Rapp's cost estimates drop considerably when revised to reflect different assumptions. For example, recalculating Rapp's estimate of a least-cost alternative to Rambus technologies in SDRAM based on support of two, rather than three, latencies[531] yields total increased cost of .62 percent of selling price, which is less than the .75 percent SDRAM royalty paid to Rambus.[532] Similarly, applying Rapp's methodology to alternatives to Rambus technologies in DDR SDRAM yields costs well below Rambus royalty levels.[533] Moreover, Rapp's calculations, like Geilhufe's estimates, wholly ignore several possibilities for cost reductions from adoption of the alternative technologies.[534]

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[527] *See* Geilhufe, Tr. 9665.

[528] A 25% margin of error for SDRAM equates approximately to .21% of selling price.

[529] *See* Geilhufe, Tr. 9665-67. Geilhufe acknowledged that he did not seek actual cost data from DRAM manufacturers to verify his cost estimates. *Id*. at 9666-67.

[530] Rapp had to estimate future DRAM prices over the expected life of DDR SDRAM, then weight those prices by estimating sales volumes for each of the future years. *Id*. at 9816-17. Rapp acknowledged that for DDR SDRAM, with limited historical data, the numbers were "mostly estimate." *Id*. at 9845.

[531] *See supra* note 439 and accompanying text.

[532] *See supra* notes 443 and 473 (showing a total cost increase of only $.03 per unit for a combination of fixed CAS latency and burst terminate commands).

[533] If, as the record suggests, no clock-circuitry was needed for double clock frequency, *see supra* note 492, total increased cost for a combination of fixed CAS latency, burst terminate commands, double clock frequency, and a clock synchronization technology would have been seven cents, or 1.36% of DDR SDRAM selling price, which is far below Rambus's 3.5% royalty. (Like Rapp, we assign no added cost for alternative clock synchronization technology.) If clock-circuitry was necessary, the record shows that PLLs sold for between 90 cents and $2. *See supra* note 493. Even based on the *highest* price, the increased cost for the combination of alternatives to Rambus's four patented technologies would have exceeded Rambus's royalty by less than Geilhufe's admitted margin of error.

[534] *See supra* notes 440, 445, 452, 456, 467, and 494 and accompanying text.

In sum, Rambus has not shown that all alternatives would have been more costly than its royalties and has not carried the burden of establishing its inevitability/superiority defense.[535]

### c. Rambus's Claim that the Link between its Conduct and the Standards Did Not Matter

Rambus backstops its inevitability/superiority claim by asserting that even if its conduct distorted the decisionmaking process at JEDEC, that did not have the effect of harming competition because the interests of JEDEC and it members were not necessarily aligned with the interests of the public as a whole.[536] We reject that argument. As discussed above, JEDEC comprises a broad range of industry participants – including, most importantly, the principal purchasers of both DRAM technologies and DRAMs. The technology choices made by the JEDEC members during the standard-setting process reflect the opinions of virtually the entire spectrum of economic actors who are directly impacted by JEDEC's standard-setting decisions. Courts and commentators long have recognized that a fair, honest, and consensus-based standard-setting process can be beneficial to consumers, while substantial competitive concerns may arise when the standard-setting choices of the SSO's participants are distorted.[537] Rambus offers no logical explanation, and cites no supporting precedent, for why the interests of JEDEC and its members would be inconsistent with a procompetitive result, or why we should overlook conduct that distorted the decisions of JEDEC.

Rambus also argues that because standard setting is a "winner-take-all" process, a "but for world" in which Rambus had disclosed its patent position would have been no better than the real world in which JEDEC adopted standards incorporating Rambus's patented technologies.[538] We reject this claim, too. Payment of royalties on memory interfaces has been very much the

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[535] Rambus also argues that the decision of three JEDEC members, with knowledge of Rambus's patents, to develop and manufacture a DRAM chip known as RLDRAM, using programmable CAS latency and burst length and dual-edge clocking, was evidence of the superiority of Rambus's technologies. RB at 59-60. RLDRAM, however, was a high-price, niche product used for specialty applications such as high-speed routers. *See* Bechtelsheim, Tr. 5867, 5870-71 (RLDRAM is priced "several times higher than commodity DRAM"); McAfee, Tr. 7428-31 (showing that RLDRAM sales were very small); Prince, Tr. 9021-22 (omitting mention of RLDRAM when asked to name "any DRAM" that had not been standardized by JEDEC or IEEE). Given RLDRAM's niche nature, a willingness to absorb Rambus royalties for RLDRAM tells little about JEDEC members's preferences for high-volume, low-cost, main memory purposes.

[536] RB at 126-28.

[537] *See, e.g.*, Allied Tube & Conduit Corp. v. Indian Head, Inc., 486 U.S. 492, 500-01, 510 (1988); II HOVENKAMP ET AL., IP AND ANTITRUST, §§ 35.4(a)(4), 35.5.

[538] RB at 126.

exception, rather than the rule, in the computer industry.[539] JEDEC could have turned to unpatented alternative technologies in each of the relevant product markets.[540] But even assuming, *arguendo*, that JEDEC still would have been willing to adopt Rambus's patented technologies after disclosures had been made, JEDEC and EIA policies would have prohibited the standardization of those technologies unless Rambus committed to licensing on RAND terms.[541] If Rambus had refused to provide the requisite RAND assurances, JEDEC would have been bound by its rules to avoid Rambus's patented technologies.[542]

Alternatively, Rambus might have acceded to JEDEC's licensing policies, and JEDEC members then would have had the benefit of RAND terms. Moreover, JEDEC members at least would have had the opportunity to seek specific royalty commitments from Rambus through *ex ante* negotiations; it was not up to Rambus to preclude that possibility.[543] No matter what the

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[539] *See, e.g.*, Heye, Tr. 3918 (AMD has not paid royalties on memory interfaces to anyone other than Rambus).

[540] *See supra* Section IV.C.3.b. For example, the record contains no suggestion that using fixed CAS latency or fixed burst length, setting CAS latency with fuses or pins, or setting burst length with fuses or burst terminate commands, would have raised patent issues. Nor does the record suggest that using double clock frequency or toggle mode, or relying on data strobes, or putting DLLs on the module or memory controller, would have involved proprietary technology.

[541] *See supra* note 285 and accompanying text (citing JEDEC and EIA rules that prohibited the standardization of patented technologies without first securing "all relevant technical information" and assurances that the patent holder will license on RAND terms).

[542] Rambus highlights the decision of a different EIA unit, the Consumer Electronics Association (CEA), to refrain from requiring a RAND assurance from Echelon Corporation. CEA chose not to invoke its licensing rule – potentially permitting Echelon to block a standard by non-compliance – but only after Echelon had announced its intention to block the standard; had engaged in a pattern of efforts over time to halt the standard development effort; and had "been unable to explain or document how the [CEA] standard refer[red] to or require[d] use of any of Echelon's patented technology." RX 2299 at 2; *see* J. Kelly, Tr. 2155-70 (EIA never received a response from Echelon as to how its patent related to the standard under development; CEA "could see no relevance whatsoever between the patent" and its standard-setting work); RX 2300.

Additionally, Rambus claims that JEDEC itself has adopted standards without seeking RAND assurances. Rambus cites only brief notations in JEDEC minutes, indicating that JEDEC approved ballots on which patent issues had been raised. The minutes – generally just one- or two-word notations – do not explain how the patent issues were resolved. They do not establish that the suspected patents actually existed, much less that they applied to the standards. Nor do the minutes indicate whether the patentee ever intended to enforce the patents against JEDEC-compliant products. The minutes do not even state that RAND assurances were not, in fact, offered. *See* JX 15 at 5-6, 8-9,14; JX 25 at 10. Rambus elicited no testimony to clarify these issues.

[543] Rambus nonetheless asserts that any incentive for the DRAM manufacturers to negotiate royalties *ex ante* would have been "very weak" because, under JEDEC's requirement of "non-discriminatory" terms, all DRAM manufacturers would have been affected uniformly. RB at 71-72. Rambus's sole record support is testimony from its economic expert, David Teece. *Id.* Teece, however, did not deny that DRAM manufacturers possessed incentives to negotiate *ex ante*. Rather, he characterized what he viewed as the practical difficulties of such

specific outcome might have been, the consequences of incorporating Rambus's patented technologies into the standards would have been identified and weighed *before* the standards were adopted, *when Rambus's technologies were competing with the alternatives.* That "but for world" would have been more competitive than the current DRAM marketplace, in which Rambus has monopoly power and can charge whatever royalties it chooses.

### d. Rambus's "No Lock-In" Claim

Rambus claims that, even if it did acquire any monopoly power by virtue of the incorporation of the four key patented Rambus technologies into the JEDEC standards, this monopoly power was not enduring because industry participants who practiced the standards were not "locked in." In effect, Rambus claims that there were no barriers to entry to rivals wishing to challenge its monopoly position.[544] The ALJ agreed with this argument, concluding

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negotiations as counter-incentives. *See* Teece, Tr. 10349, 10352-54 (stating that "firms have got incentives to do lots of things that they don't do"), 10360 ("because of these costs and difficulties, you're incented not to incur those costs and difficulties [associated with *ex ante* negotiation]"); Elsewhere, Teece has given credence to the incentive to seek *ex ante* negotiations. *See* David Teece & Edward Sherry, *The Interface Between Intellectual Property Law and Antitrust Law: Standards Setting and Antitrust*, 87 MINN. L. REV. 1913, 1993-94 (2003) ("one would expect that, at least when the royalty rates are negotiated ex ante (prior to the adoption of the standard), the patent holder would moderate its royalty demands").

Rambus further contends that an opportunity to negotiate would have been meaningless because it is "all but impossible" to negotiate licenses for patent applications, which are shrouded in uncertainty. RB at 72. If so, then the record demonstrates that Rambus itself achieved the unattainable. Rambus had entered into RDRAM license agreements with three firms by 1992 – despite having only patent applications at that time. *See* RX 538 at 9, 13, 42 (1991 Rambus license to NEC); CX 543a at 11 (1992 Rambus business plan referencing RDRAM licenses with Toshiba, Fujitsu, and NEC); Parties' First Set of Stipulations, Item 11 (Rambus's first issued patent was the '703 patent); CX 1460 at 1 (the '703 patent issued in 1993). Rambus also granted numerous RDRAM, SDRAM, and DDR SDRAM licenses that included patent applications. *See* CX 1600 at 3-4, 6-7 (Hyundai license covering all DRAMs using all or part of Rambus's interface technology); CX 1609 at 3, 6 (Mitsubishi RDRAM license); CX 1617 at 4, 7 (Siemens RDRAM license); CX 1646 at 3, 6 (Micron RDRAM license); CX 1680 at 12, 19, 24 (*in camera*) (Toshiba SDRAM/DDR SDRAM license); CX 1681 at 2-3, 10 (*in camera*) (Hitachi SDRAM/DDR SDRAM license); CX 1683 at 2, 7, 10 (*in camera*) (OKI SDRAM/DDR SDRAM license); CX 1685 at 2, 8, 12 (*in camera*) (NEC SDRAM/DDR SDRAM license); CX 1686 at 2, 7, 11 (*in camera*) (Elpida SDRAM/DDR SDRAM license); CX 1687 at 2, 8, 11-12 (*in camera*) (Samsung SDRAM/DDR SDRAM license); CX 1689 at 2, 7-8, 13-14 (*in camera*) (Mitsubishi SDRAM/DDR SDRAM license).

[544] In contrast, internal Rambus documents described the DRAM industry as susceptible to lock-in. *See, e.g.*, CX 533 at 15 ("Once a DRAM or vend[or] [has] committed to an architecture [it is] unlikely to change"). Rambus's principal engineer, Ware, similarly observed that once a DRAM controller manufacturer begins using a technology – even if not essential to the part – "it becomes more difficult [for that company] to not use it once you have put it in your design"). CX 2115 at 135 (deposition transcript at 134) (Ware FTC Dep.) (*in camera*). *See also* CX 5011 (designated R401155) (1998 Rambus Strategy Update stating, "We should not assert patents against Direct partners until ramp reaches a point of no return (TBD)").

that Complaint Counsel had failed to establish that the DRAM industry had become locked into the JEDEC standards.[545]

Our analysis necessarily is anchored by timing. Lock-in must be assessed as of the time that JEDEC members gained sufficient information to know that Rambus had relevant patents and could have taken responsive action. JEDEC members lacked knowledge of Rambus's patent position until Rambus filed its first infringement suit against a producer of JEDEC-compliant DRAMs in early 2000. After that, it took some time for the information to be disseminated and evaluated. Each JEDEC member individually needed to explore alternatives – such as licensing and possible design changes – and to determine how it preferred to proceed. At that point, the JEDEC members could begin in earnest to try to agree on a revised standard.[546]

If the DRAM industry had become locked into Rambus's technology by the time that industry participants were apprised of, and able to take action in response to, Rambus's enforcement efforts, Rambus would have achieved durable monopoly power. If, however, the industry still had the practical ability to avoid Rambus's patents by switching to alternative technologies, Rambus would not have obtained durable monopoly power.[547]

We find that the DRAM industry was locked into the SDRAM and DDR SDRAM standards by 2000, by which time the JEDEC members were, in theory, in a position to take actions to avoid Rambus's patents. The record does not, however, establish a sufficient causal link between Rambus's exclusionary conduct and JEDEC's adoption of DDR2 SDRAM.

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[545] ID at 326-29.

[546] *See, e.g.*, CX 1855 (January 2000 Rambus complaint alleging that Hitachi's SDRAM and DDR SDRAM products infringed four Rambus patents but not identifying the specific claims or technologies at issue). Rambus revealed the nature of its claims to additional JEDEC members during the second quarter of 2000. CX 1109 at 1; CX 1127; CX 1129; CX 1371; CX 2559 at 3; Crisp, Tr. 3435-36. Some JEDEC members quickly recognized the implications of Rambus's patent enforcement efforts. *See, e.g.*, Rhoden, Tr. 532-33; CX 2459 at 1 (indicating that initial work-around proposals regarding programmable CAS latency were presented in March 2000). Other JEDEC members needed additional time before they gained a detailed understanding of Rambus's claims. *See* Krashinsky, Tr. 2782 (stating that he learned that Rambus claimed a patent on programmable CAS latency "midyear or so" in 2000); Polzin, Tr. 3987 (stating that he learned that Rambus claimed patents on technologies used by AMD in "late summer 2000 " and that he conducted an analysis of the Rambus patents at that time). Discussions of possible ways to avoid Rambus's patents on dual-edge clocking for purposes of DDR2 SDRAM began in a JEDEC task group in late October 2000 and reached the JC 42.3 Committee in December 2000. Krashinsky, Tr. 2827-28; Lee, Tr. 6800-02; CX 426; JX 52 at 45-50.

[547] This issue also is one of causation. We could find that Rambus's deceptive course of conduct caused the ensuing anticompetitive effects because JEDEC members had become locked in before they could take effective countermeasures, and thus were unable to avoid Rambus's royalties. If, on the other hand, JEDEC members had obtained the necessary knowledge of Rambus's patent position at a time when they still were economically capable of switching technologies – but deliberately chose not to switch – the chain of causation would have been broken, and Rambus's monopoly power would not be attributable to its deceptive course of conduct.

***SDRAM.*** The SDRAM standard was first published by JEDEC in 1993. Rambus claims patent protection over technology from the latency and burst length product markets that was incorporated into the standard.

Complaint Counsel's economic expert, McAfee, described lock-in as "something that grows over time. It's certainly been accomplished by the time that ramp-up starts."[548] McAfee reasoned that before the time DRAM production ramps up, most of the sunk investments in complementary goods must have been made, because "in order to deploy the standardized [DRAM] product in volume, it requires those complementary goods."[549] The progressive accumulation of switching costs gradually contributes to lock-in,[550] and most of the switching costs for both DRAM manufacturers and producers of complements accrue by the time DRAM production ramps up.[551]

Manufacturers ramped up SDRAM production around 1996.[552] SDRAM represented 78.4 percent of DRAM revenues by 2000.[553] DRAM manufacturers, component manufacturers, and systems OEMs testified that changing SDRAM to work around Rambus's patents in 2000 would have presented significant financial and technical difficulties.[554] For example, a witness

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[548] McAfee, Tr. 7444-45. McAfee defined ramp-up as the time "when the volume [of DRAM production] starts to dramatically increase." *Id*. at 7445.

[549] McAfee, Tr. 7445-46 ("they're not going to produce the DRAM for inventory in any large volumes and just sit on them hoping that the complementary goods would be provided in the future").

[550] Switching costs accumulate for manufacturers of DRAMs and of compatible, complementary components as they move from the standard-setting process, to designing chips and products that conform to the standard; testing and verifying those designs; building, testing, and qualifying prototypes; and ramping up production on a commercial scale. At each stage the manufacturers make sunk investments that have to be repeated in order to switch to an alternate design. *See* McAfee, Tr. 7444, 7453-54; Shirley, Tr. 4152-54.

[551] *See* Peisl, Tr. 4452-53 (a change to SDRAM that would have been "relatively easy" in 1992 would have been "near impossible" in 2000).

[552] McAfee, Tr. 7442 (ramp-up for SDRAM was "roughly 1995 or 1996"); *id*. at 7446 ("[T]he volume production start[ed] in the 1996-1997 time frame. And so that corresponds to the ramp-up."). SDRAM accounted for less than 2.9% of DRAM revenue in 1995, 4.3% in 1996, and 33.5% in 1997. Rapp, Tr. 10248. Revenues, of course, lag behind production. *See also* Rambus Inc.'s Response to Complaint Counsel's Proposed Findings of Fact, No. 577 (Oct. 1, 2003) ("Although SDRAM represented a relatively small percentage of the DRAM market in 1996, it was certainly 'volume' production.").

[553] Rapp, Tr. 10100-01.

[554] Witnesses from Infineon and Micron, respectively, stated that by 2000 the level of SDRAM development and implementation made substantial changes "very costly and . . . near impossible," Peisl, Tr. 4443-44, and "virtually impossible," Appleton, Tr. 6399. CPU manufacturer AMD stated that changing SDRAM to work around Rambus patents in 2000 would have introduced "a whole host of problems" and would have been "a major, major concern for AMD." Heye, Tr. 3731-34. Cisco Systems explained that changes to memory in 2000 would

from HP testified that by the time he learned of Rambus's patent claims in 2000, changing SDRAM to avoid Rambus's patent enforcement efforts would have been "[w]ay too expensive" for HP, whose SDRAM-based server

> was already out, qualified and you know, we sold to customers and you cannot change something like this after it was designed and already shipped, and if you do change it, you're talking about millions and millions of dollars in expenses. It wasn't even going to be considered.[555]

Similarly, an IBM e-mail from April 2000 states, "we have gone way too far with SDR [SDRAM] to even consider talking about" switching to fixed latency.[556] Redesigning programmable burst length at that time would have presented similar difficulties.[557]

The issue of timing was particularly critical in the DRAM market: the time it would take to redesign SDRAMs and their complements to avoid Rambus's claimed patents would have been prohibitive. Rambus's engineering expert, Geilhufe, indicated that the changes could have been implemented in six to eighteen months.[558] Most of the previous design projects cited in the

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have imposed "tremendous cost to Cisco to redesign the existing boards and systems Cisco was shipping." Bechtelsheim, Tr. 5881-82. Graphics processor/chipset designer nVIDIA stated that changing SDRAM in 2000 would have put it through a "painful process" of changing its development plan and redesigning its products. Wagner, Tr. 3862-63.

[555] Krashinsky, Tr. 2782-83. According to the HP witness, providing multiple latencies without using programmable CAS latency would have required changes to the memory module, the motherboard, and the memory controller. *Id*. at 2784-87. He characterized changing programmable CAS latency "a major change," *id*. at 2788, although he indicated that significantly less change would have been required if a fixed CAS latency would have sufficed. *Id*. at 2804-05. Joe Macri of ATI Technologies (ATI) stated that graphics system designer ATI would have incurred "a huge burden" if JEDEC had changed to fixed latency. Macri, Tr. 4764-65 (*in camera*). *See also* Jacob, Tr. 5377-78, 5569 (use of multiple fixed latencies would have caused compatibility problems absent either greater user understanding as to which latency value was needed or development of a more sophisticated memory controller).

[556] RX 1626 at 3. When the possibility of changing the SDRAM standard regarding programmable CAS latency was discussed within JEDEC in March 2000, it was "very poorly received" because of lock-in concerns. *See* Rhoden, Tr. 533; Kellogg, Tr. 5196-200; RX 1626 at 2.

[557] *See* Peisl, Tr. 4450-53 (removing programmable burst length in 2000 would have been "nearly impossible," with a "huge impact" on DRAM customers). Using a burst terminate command to set burst length would have required "an enormous amount of redesign"; it may have required "almost a full redesign of the graphics pipeline" and at a minimum would have meant design modifications and a "big disruption of [ATI's] engineering plans." Macri, Tr. 4776-77 (*in camera*). *See also* Jacob, Tr. 5572-73 (switching to fixed burst length would introduce incompatibilities in some systems and would have design implications similar to those for switching to fixed CAS latency).

[558] *See* Geilhufe, Tr. 9615. *See also id*. at 9675 (stating that the changes could be accomplished in a six to twelve month time frame).

record indicate that at least a year likely would have been needed.[559] However, these estimates do not account for additional delays inherent in the standard-setting process itself. Even assuming perfect knowledge of Rambus's patent claims, manufacturers could not have begun immediately to design and implement responsive changes. The industry would have had to agree on how the standard would be changed.[560] This could have added a year or more to whatever time would have been required to make the changes.[561] Such delays would have meant missed opportunities, which firms in the industry found unacceptable.[562]

We are unpersuaded by Rambus's argument that switching costs were insufficient to establish lock-in. Rambus attempted to quantify the switching costs for DRAM manufacturers to design around its patents on SDRAMs. Rambus's experts testified that a DRAM manufacturer would incur switching costs of $4.3 million to convert from programmable CAS latency and programmable burst length to fixed CAS latency and fixed burst length.[563] Rambus's economic

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[559] *See* Bechtelsheim, Tr. 5884 (Cisco would need at least a year to redesign its products to accommodate new memory standards); Reczek, Tr. 4341-45, summarized in DX 45 (estimating "24 months plus" to design, assemble, test and qualify a new DRAM); Peisl, Tr. 4375-77 (Infineon's reworking of a flawed SDRAM design took approximately one year to repeat various steps); Heye, Tr. 3673-74, 3677-78, 3767-69 (it typically takes AMD between 15 months and two years to design and implement a new chipset and other complementary infrastructure for its microprocessors); Polzin, Tr. 4016-18 (AMD developed a chipset in 9 months and ushered a new motherboard to mass production in 18 months). Rambus cites testimony that Hyundai made the initial transition from SDRAM to DDR in nine months, *see* CX 2108 at 45 (deposition transcript at 237) (Oh FTC Dep.) (*in camera*), but Complaint Counsel cite documentary evidence indicating that it actually took 15 months, *see* CX 2334 at 20.

[560] *See* Krashinsky, Tr. 2792 ("It has to be defined as a standard and be accepted by the industry as a standard before HP would adopt it and we'll start spending money on doing it."), 2817 (designing can begin once specifications are well enough settled that further changes will not affect the design). No individual DRAM or component manufacturer likely would have been able to adopt non-compliant technology. *See, e.g.*, Macri, Tr. 4768 (*in camera*) (explaining that if graphics system producer ATI changed its controller to conform to an alternative to programmable CAS latency, "we would essentially have a nice paperweight" absent "a device to talk to").

[561] *See* Krashinksy, Tr. 2792 (passing a revised SDRAM standard likely would take "a year or longer even"); Heye, Tr. 3736 ("it's hard to get a consensus of change . . . all of that takes time"); Peisl, Tr. 4453 ("JEDEC is traditionally a very slowly moving consortium . . . because there's so many companies involved . . . so to try to reach consensus at JEDEC, based on my experience, [would] have been incredibly hard and tough."). *See generally* Geilhufe, Tr. 9675 (stating that his time estimate included no allowance for JEDEC consideration).

[562] *See, e.g.*, Wagner, Tr. 3862-63 (explaining that eliminating programmable CAS latency and programmable burst length would have delayed introduction of its graphics products that were "aligned to the timelines" of new computer games: "If we can't release the chip because we have to go redesign for some new technology, then, you know we miss the opportunity to align with this new game . . . ."); Heye, Tr. 3736 ("all of that takes time, and time is something that you don't have in this market"); Shirley, Tr. 4208-09 (*in camera*); Macri, Tr. 4600 ("Time to market is extremely critical in this world"); Kellogg, Tr. 5199; Lee, Tr. 6635, 6684; McAfee, Tr. 7457 ("delay is in itself inherently costly").

[563] According to Geilhufe, each fixed latency or burst length part would require $100,000 in design costs, $50,000 for photo tools (masks), and $250,000 for qualification. Geilhufe, Tr. 9575-79, 9594-95. Rapp calculated that matching the three latencies and four burst lengths found in JEDEC's SDRAM specifications would require

expert, Rapp, argued that $4.3 million is small in relation to the royalties that are being charged by Rambus.[564] The ALJ accepted both Rambus's switching cost estimate and Rapp's conclusions about the economic impact of these costs.[565]

Rambus's $4.3 million figure substantially understates switching costs for three principal reasons. First, Rambus understates or omits certain individual switching cost elements, including mask costs,[566] inventory costs,[567] and opportunity costs.[568] Second, Rambus's figure covers only the switching costs of a single manufacturer at a single plant for a single product. It overlooks – as Rapp acknowledged – that each DRAM manufacturer typically offers components with as

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seven new designs, twelve sets of tools, and twelve qualifications, for a total $4.3 million. Rapp, Tr. 9885-86. A lower estimate would flow from Rapp's methodology if the alternative supported fewer latencies or fewer burst lengths than SDRAM. Although we have suggested that two latencies and two burst lengths may have been a reasonable alternative at the time the SDRAM standard was adopted, *see supra* Section IV.C.3.b., subsequent commitments to particular latency or burst length values would have to have been considered in 2000. The Initial Decision, for example, identifies three latency values and three burst lengths in use for main memory or graphics purposes. *See* IDF 1146, 1220, 1223. *See also* RX 1626 at 3.

[564] Rapp, Tr. 9887 ("a small price to pay").

[565] IDF 1652-55.

[566] In contrast to Geilhufe's estimate of $50,000 to switch masks, Micron's Brian Shirley testified that the mask set for a specific DDR SDRAM revision design in 2001 cost $334,000, Shirley, Tr. 4205 (*in camera*); that the cost of Micron's mask sets in 2002 ranged from $162,000 to $950,000, *id*. at 4231-32 (*in camera*); that the $162,000 figure would have been the same in 1998-99, *id*. at 4279 (*in camera*); and that multiple mask sets typically were required to maintain full production. *Id*. at 4154 (high-volume products require 25-45 mask sets to run in production), 4234-35 (*in camera*). This last consideration may be very significant in a setting where production already has ramped up; the switching costs necessary to reach the same stage with an alternative technology would have to take production needs into account.

[567] Rambus's experts failed to consider any costs for inventory left unsold at the time of a transition. Such inventories could be substantial: Micron, for example, typically held three weeks of finished goods inventory, Shirley, Tr. 4238 (*in camera*), as well as significant quantities of stock in production. *See* Shirley, Tr. 4153 (estimating that it typically took 45-55 days to move from wafer start to completion). Although a phased transition to a new technology might reduce the loss of inventory, the failure to consider any inventory costs whatsoever appears to be a significant omission.

[568] To undertake a product redesign, DRAM or component manufacturers may need to divert resources, such as engineers, from other projects, potentially delaying the introduction of new products. *See, e.g.*, Heye, Tr. 3745; Macri, Tr. 4769 (*in camera*); Appleton, Tr. 6402-03. Rambus takes no account of opportunity costs beyond the salaries of the affected engineers. *See* Rapp, Tr. 10156-58. This fails to consider that engineers' specialized knowledge or team arrangements could make their diversion to a different design project particularly disruptive and could give rise to opportunity costs in excess of their salaries. *See* Shirley, Tr. 4207-09 (*in camera*); McAfee, Tr. 11292-95. Even Rapp acknowledged the possibility that his analysis could miss some surplus value earned by the employer over an engineer's salary. *See* Rapp, Tr. 10158.

many as three densities,[569] and would incur switching costs separately for each density.[570] The figure also ignores – as Rapp conceded – that manufacturers with multiple plants might incur some of these costs at each facility.[571] Moreover, Rapp agreed that each affected DRAM manufacturer separately would bear these switching costs and that, as of 1995, there were five to ten major DRAM manufacturers.[572] Multiplying Rambus's $4.3 million estimate – by the number of manufacturers, then by the average number of densities, and then by a figure reflective of the costs that would have to be duplicated in multiple plants – suggests that total costs to DRAM manufacturers could have reached hundreds of millions of dollars. Adjusting for understatements of cost elements would increase that total even more.

Most significantly, Rambus's $4.3 million figure focuses solely on DRAM manufacturers. If JEDEC changed SDRAM, OEMs and manufacturers of complementary components would face substantial switching costs in redesigning their own products.[573] Rambus's estimate omits these costs, although even Rapp conceded that the switching costs of component manufacturers could exceed those of DRAM manufacturers.[574] As a consequence, Rambus's estimate wholly disregards a major source of lock-in. For all of the foregoing reasons, we find Rambus's switching cost estimates to be flawed.

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[569] *See* Rapp, Tr. 10144.

[570] *See* Rapp, Tr. 10143-46 ("whatever the switching costs were . . . would be multiplied by the number of parts that they were starting off with").

[571] *See* Rapp, Tr. 10123. Many DRAM manufacturers own multiple manufacturing facilities. *See, e.g.*, Appleton, Tr. 6267-69 (Micron operates five fabrication facilities); CX 2466 at 2 (Infineon operates three manufacturing facilities).

[572] *See* Rapp, Tr. 10124 ("You could multiply this as needed by the number of manufacturers"), 10146. *See also* CX 2747 at 7 (Micron DRAM Update presenting market shares of 18 DRAM manufacturers in early 1999), 15 (showing 16 DRAM manufacturers remaining in September 1999); Gross, Tr. 2309 (8-10 was a "generous" estimate of DRAM manufacturers in 2003); Appleton, Tr. 6259, 6276-6277 (the DRAM industry had consolidated from approximately 20-25 DRAM manufacturers in the early 1980s to 5-6 major DRAM manufacturers and 2-3 smaller manufacturers as of 2003).

[573] Complementary components – such as memory controllers, memory modules, and motherboards – must be compatible with industry-standard DRAM. *See, e.g.*, Peisl, Tr. 4382, 4410, 4402-03; Macri, Tr. 4589 ("A DRAM alone doesn't really do anything. It needs to talk to other things . . . ."); Heye, Tr. 3655-65, 3715; Polzin, Tr. 3954; CX 1075 at 1. For example, changing programmable CAS latency in SDRAM would require HP to redesign and generate "a whole new chip" for its proprietary memory controller. Krashinsky, Tr. 2786. Designing around Rambus's patents may have required changes to the memory controller, the motherboard, the memory module, and the BIOS (basic input/output system, *i.e.*, the built-in software that provides some computer functions without accessing programs from a disk). Heye, Tr. 3733-34, 3742-43; CA A-4.

[574] Rapp, Tr. 10130-31 (adding, however, that component manufacturers' switching costs were likely of the same order of magnitude as those of DRAM manufacturers).

Rambus also argues that the DRAM industry was not susceptible to lock-in because DRAM manufacturers "routinely redesign their products" and the entire industry "quickly and seamlessly" switches between sub-standards.[575] These sorts of changes, however, were not comparable to the revisions that would have been required to avoid patented Rambus technologies. The "redesigns" referenced by Rambus generally involved shrinking the dimensions or changing the density of DRAM chips.[576] The sub-standards were merely addenda to JEDEC standards.[577] The changes for most redesigns and for switches between sub-standards were more easily accomplished than changes in the DRAM technologies upon which the JEDEC

[575] RB at 76-79. *See also* ID at 326-28.

[576] For example, Rambus cites its Proposed Finding 1292, which counts Infineon's various die shrinks and density changes. RB at 76 n. 36; *see also* IDF 1608 (relying on the same evidence). *See* Becker, Tr. 1141 (explaining that density refers to the capacity of a memory chip, the number of pieces or bits of memory it can hold), 1153-54, 1156-57; Reczek, Tr. 4304.

[577] Addenda were add-ons that filled some of the gaps that JEDEC had not specified. Peisl, Tr. 4411-12. They evolved in response to changes in speed of operation. *See* Becker, Tr. 1142; Heye, Tr. 3676-77. Large DRAM customers such as Intel sponsored addenda for varied reasons, such as preventing industry participants from developing incompatible parts, *see* MacWilliams, Tr. 4908-09 (explaining that different manufacturers had introduced "very subtle" differences because they had needed to draw upon a series of JEDEC ballots rather than a comprehensive specification) or to add details relevant to their design needs. *See* Shirley, Tr. 4138-40 (describing Intel's PC100 specification as adding "a low level of detail"); Peisl, Tr. 4411.

standards were based.[578] More importantly, the types of changes cited by Rambus raised fewer compatibility issues and, therefore, fewer lock-in implications.[579]

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[578] *See, e.g.*, CX 2108 at 65-66 (deposition transcript at 257-58) (Oh FTC Dep.) (*in camera*) (describing additional design work required for changing circuitry as opposed to conducting a shrink); CX 2334 at 3 (April 1999 Hyundai presentation stating, "PC100 to PC133 – The Same Die as PC100"). An Infineon witness explained that changes in DRAM type took longer than shrinks and, with consideration of the need to make revisions and to repeat steps, often took longer than changes of density. Reczek, Tr. 4304, 4309, 4336-38, 4341-45, 4350-51 (noting that Infineon needed three major revisions to produce a satisfactory DDR SDRAM device). Although the difference in effort required for individual changes was not large, *id.* at 4341-45, a change to the JEDEC-standardized technologies would have required *multiple* revision projects – for example, revising each distinct density of SDRAM and DDR SDRAM – and the total cost would have been some multiple of the cost for an individual change. *See* Rapp, Tr. 10143-44 (agreeing that DRAM manufacturers would "need to make changes to each of the densities of SDRAM or DDR").

Rambus claims that Complaint Counsel's economics expert "admitted that switching cost to avoid Rambus's technologies would be no greater than those routinely absorbed by the industry." RB at 79. McAfee testified that transitions between sub-standards involved the same "categor[ies] of costs" as transitions between JEDEC standards but that "the size of those costs are substantially less" with the former. McAfee, Tr. 7715. He also testified that the cost of changing interface technologies exceeded the cost of die shrinks. *Id* at 7718-19. Rambus also relies on a 1996 Micron e-mail, RX 836 at 2-3, which does not establish that routine changes in chip size, density, and speed involved the same level of cost and difficulty as changes in JEDEC-standardized technologies.

Rambus further contends that a switch to alternatives for its technologies "could be "piggyback[ed]" on a redesign, and the ALJ agreed. *See* RB at 76; IDF 1656. The only support comes from Rambus's own expert witnesses. *See* Soderman, Tr. 9418; Geilhufe, Tr. 9615, 9675. Witnesses representing DRAM manufacturers, however, consistently testified that they would not normally combine interface technology changes with redesigns. Infineon's Henry Becker, for example, explained, "Typically when you do a shrink, you like to do it on a product that you're already producing so that you don't create – you don't change too many things at once." Becker, Tr. 1157-58. *See also* Reczek, Tr. 4304-05 (testifying that shrinks, density revisions, and changes to the type of DRAM generally were not combined "because if you mix up two different steps, you might run into severe problems, not finding out what the reason for not functioning in the chip is"); CX 2108 at 65 (deposition transcript at 257) (Oh FTC Dep.) (*in camera*) (stating that Hyundai normally did not change internal circuitry at the time of a shrink).

[579] Redesigns and transitions between sub-standards typically affected the dimensions, amount, and speed of main memory, but were less likely to affect compatibility between main memory and other computer components. The JEDEC interface standards, in contrast, were essential to compatibility. They governed, for example, the timing of release of data, the amount of data, and the speed and alignment of transmissions of data transferred between main memory and other computer components. *Compare* IDF 41; CX 1388 at 8; Peisl, Tr. 4382; Heye, Tr. 3769-71; Bechtelsheim, Tr. 5958; McAfee, Tr. 7718-19 (all highlighting the role of Rambus's technologies as part of an interface and describing the resulting compatibility requirements) *with* Becker, Tr. 1157 (from the customer perspective shrinks don't matter – different sizes "all function the same, he gets the same reliability, same performance"); MacWilliams, Tr. 4887 ("we [Intel] made sure [PC100] was backwards compatible with the 66 megahertz"); Polzin, Tr. CX 2334 at 3 (April 1999 Hyundai presentation stating, "PC100 to PC133 . . . – Using Existing Infrastructure of PC100"); CX 2728 at 2 (December 1998 Micron comments to Dell, stating, "PC133 are backwards compatible with PC100" but for DDR, companies are either "in progress with" or "looking to start" DDR chipset designs). *But cf.* Gross, Tr. 2351-53 (stating variously that she was "not sure," "d[id] not recall," and "believe[d] . . . probably" that PC100 was not backward compatible with PC66).

We find that high direct switching costs, combined with significant delays from revising standards and reworking products, rendered infeasible a change in SDRAM to avoid Rambus's patented technologies in 2000 and conferred durable monopoly power with respect to SDRAM.

***DDR SDRAM.*** JEDEC first published the DDR SDRAM standard in 1999. Rambus claims patent protection over technology incorporated into the standard relating to dual-edge clocking and on-chip PLL/DLL, in addition to the programmable CAS latency and burst length technologies that carried over from SDRAM.

The DRAM industry was significantly locked in to DDR SDRAM by 2000. DRAM manufacturers had begun production of DDR SDRAMs by that time,[580] and their representatives consistently testified that changes no longer were feasible.[581] Furthermore, the necessary complementary components had to be in place before substantial sales were possible.[582] AMD, for example, launched a DDR-based system in October 2000; the general manager of its microprocessor unit, Richard Heye, testified that product development had gone too far to change DDR SDRAM by the time that a response to Rambus's patents could have been considered:

> We were planning a launch in the fall of 2000, October. By that time frame, the chipset was for all intents and purposes complete, we were in the validation testing, the DDR, the DIMMs, the memory was done, the DIMMs were being manufactured, the memory folks were actually starting production and waiting for it to start . . . .[583]

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[580] Hyundai began mass production of its first DDR chip by March 1999. *See* CX 2108 at 45 (deposition transcript at 237) (Oh FTC Dep.) (*in camera*); CX 2334 at 20. Infineon completed design of its 256-megabit DDR SDRAM at the end of 1999. Peisl, Tr. 4377-79 (explaining that enough was known about DDR SDRAM specifications to begin designing even before the standard was finalized, deferring some aspects until JEDEC made the last of its choices), 4454. Infineon was ramping production of its first DDR product by 2000. *Id.* at 4455. *See also* Crisp, Tr. 3432 (DDR SDRAM was in production in 1998); CX 2726 at 3 (64 Mb DDR SDRAM was available as early as 1998); RX 885A at 1 (Samsung planned to begin mass production of 64 Mb DDR in 1998, and Fujitsu was on a similar schedule). *See generally* CX 2158 at 2 ("Micron Demonstrated DDR in a PC in Fall 99"); CX 2387 (January 1998 IBM e-mail stating that engineering hardware would be available for IBM DDR SDRAMs by the second quarter of 1998, with qualification expected by the end of 1998); G. Kelley, Tr. 2589-91 (IBM began design of DDR SDRAM features selected by JEDEC in late 1996 or the first half of 1997); CX 957 at 2 (LG Semiconductor was working on DDR SDRAM by 1997 – it had assigned its SDRAM team to DDR tasks). DDR SDRAM revenues rose rapidly from .4% of DRAM revenue in 2000 to 5.3% in 2001. Rapp, Tr. 10248-49. Because revenues lag behind production, the market share data are consistent with a significant production ramp in 2000.

[581] *See, e.g.*, Peisl, Tr. 4443-44; Appleton, Tr. 6386-87, 6399-401.

[582] *See* CX 2747 at 58-60 (September 1999 Micron DRAM Update stating that DDR controllers for graphics purposes were already available and that multiple chipset vendors were "developing support"); Peisl, Tr. 4455-57 (by 1999-2000 the "customers had progressed in their designing of platforms and have SDR and DDR quite a bit already. There were DDR chipsets available."); McAfee, Tr. 7445.

[583] Heye, Tr. 3737. *See also id.* at 3738 (stating that AMD by 2000 was in the midst of testing DDR memory from all the vendors to ensure that all combinations were going to work with its chipset); CX 2158 at 2

Similarly, HP's Krashinsky testified that DDR SDRAM already had been installed in HP server prototypes by about the third quarter of 2000.[584] Cisco's Bechtelsheim stated that a change in DRAM design in response to Rambus's assertion of patents in 2000 would have imposed "a tremendous cost to Cisco to redesign the existing boards and systems Cisco was shipping to accommodate this new type of memory."[585]

The adoption of programmable CAS latency and burst length in the DDR SDRAM standard raises the same issues as in SDRAM. The cost and delay associated with changing these technologies in SDRAM were equally applicable to DDR SDRAM.[586] Indeed, JEDEC rejected a March 2000 proposal to move to fixed latency in DDR SDRAM, and lock-in concerns were a significant factor.[587]

The DDR SDRAM standard adopted two additional technologies that Rambus now claims to have patented: dual-edge clocking and on-chip PLL/DLL. As to dual-edge clocking, Complaint Counsel's engineering expert testified that redesigning DDR SDRAM to avoid Rambus's patents would have required changes to the clock chip and the memory controller.[588] Producers of complements and OEMs voiced lock-in concerns. For example, AMD's Polzin testified that, by the summer of 2000, the firm was in the middle of a production ramp for DDR-based controllers and motherboards, and "[i]t would have been impossible for us to stop and change" the dual-edge clocking mechanism.[589] Likewise, Krashinsky explained that HP did not seek a change in JEDEC's DDR SDRAM standard, even after learning of Rambus's patent claims on dual-edge clocking, because HP already had developed a server prototype dependent

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(June 2000 AMD e-mail stating, "AMD powered on the first K7 DDR chipset (IGD4) in Dec 99"). *But cf.* Heye, Tr. 3750 (noting that the infrastructure of DDR-based complements was still developing in 2000 and had not yet been established in the marketplace).

[584] Krashinsky, Tr. 2793. Krashinsky added that if HP had needed to change the chipset that was designed for use with DDR in this server, it would have had to change all of the other products that also used that chipset. *Id.* at 2797.

[585] Bechtelsheim, Tr. 5881. Bechtelsheim estimated that redesigning and requalifying its products in order to accommodate changes in DRAM technology would cost between $500,000 and $1 million for each distinct PC board assembly, so that total cost to Cisco "could approach or exceed $1 billion." *Id.* at 5882.

[586] *See, e.g.*, Wagner, Tr. 3862-63; Peisl, Tr. 4450-53; Macri, Tr. 4764-65 (*in camera*), 4775-77 (*in camera*); Kellogg, Tr. 5196-200. *See generally* Polzin, Tr. 3992-94 ("The problem was, we'd have to change everything in the middle of this production ramp.").

[587] *See* Rhoden, Tr. 532-33 (stating that his proposal to change to fixed latency "was very poorly received within the committee, because there were products shipping in pretty high volume at that time").

[588] Jacob Tr. 5413, 5433, 5575-76.

[589] Polzin, Tr. 3980, 3989, 3995-96. *See also* Macri, Tr. 4649-51 (removing dual-edge clocking in 2000 would mean "you're shaking the foundations . . . of the standard and not changing a minor piece").

on DDR SDRAM, HP was "counting on" that standard, and "HP does not want to support changes that will cause a lot of expenses to HP."[590]

The record also establishes that on-chip PLL/DLL was similarly locked-in at this time. AMI-2's Rhoden testified that a proposal in 2000 to change DDR SDRAM to replace on-chip DLL would have been a waste of time in view of "wide industry use and high volume production."[591] Joe Macri of ATI Technologies (ATI), speaking in terms of the subsequent DDR2 SDRAM standard, described removal of on-chip DLL as "not something you can change in a trivial manner," adding, "You really need a gun to your head."[592]

Consideration of DDR SDRAM also introduces concerns regarding backward compatibility, especially with reference to dual-edge clocking. Backward compatibility requires that it be economically feasible to produce complementary components capable of supporting both an old and a new generation of DRAM. As witnesses explained, it would have been difficult to design a memory controller that would be compatible both with existing DDR SDRAMs and with any revised version that avoided dual-edge clocking. Micron's Lee termed this "a very difficult design to accommodate,"[593] and ATI's Macri stated that switching to single-edge clocking would have had "a big impact" from "a design point of view."[594] Macri cited the need to retain backward compatibility as a reason why avoidance of Rambus's patents was not feasible.[595]

Rambus argues that, despite this evidence, the industry was not locked into DDR SDRAM in 2000. Rambus provides no estimates of the switching costs for changing dual-edge clocking and on-chip PLL/DLL. Rather, Rambus argues, and the ALJ agreed, that the fact that JEDEC actively considered alternatives for the Rambus technologies in 2000 shows that JEDEC could not have been locked in.[596] We disagree. JEDEC ultimately *rejected* all of the alternatives.

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[590] Krashinsky, Tr. 2793-94.

[591] Rhoden, Tr. 533.

[592] Macri, Tr. 4649. *See also* Jacob, Tr. 5577-78 (compatibility dependent on system design), 5617-18 (compatibility dependent on data arriving at the controller in the appropriate timing window).

[593] *See* Lee, Tr. 6805-06.

[594] Macri, Tr. 4780-81 (*in camera*).

[595] Macri, Tr. 4765, 4767-68, 4773, 4780-81 (all *in camera*). *See generally* Krashinsky, Tr. 2829 (members deemed switching to a single-edge clock "too dramatic" a change).

[596] IDF 1585; RB at 75. The ALJ's finding of fact cited only Complaint Counsel's economic expert. McAfee, however, actually offered much more limited testimony – though he would not "take it as proof," he would not expect JEDEC members to "spend a lot of time discussing technologies in 2000" unless "at least some significant number of members" thought those technologies were commercially viable. McAfee, Tr. 7571.

In view of the record as a whole, the fact that the industry was aware of alternatives, but did not switch to them after the adoption of the standard, supports our finding that JEDEC members decided that expenses and delays rendered switching infeasible.

Rambus asserts that switching from DDR SDRAM in 2000 would have been easy. In addition to arguments based on the relative ease of developing new DRAM sizes, densities, and speed grades,[597] Rambus cites an April 2000 Hitachi e-mail stating that "it's not too late for minor, carefully considered changes" to the DDR SDRAM standard.[598] We find that this single e-mail, which addressed only programmable CAS latency,[599] does not accurately reflect the costs and delays described by other industry participants.

In summary, we conclude that lock-in was significant by 2000 with regard to DDR SDRAM and gave rise to Rambus's durable monopoly power.

***DDR2 SDRAM.*** The record does not support a finding that lock-in conferred durable monopoly power over DDR2 SDRAM by 2000. There is evidence that work on DDR2 SDRAM was underway by spring 1998.[600] Macri, the JEDEC representative from ATI and chairman of the task group responsible for developing a successor to DDR SDRAM, testified that in April 1998 the group began to engage in the "initial set of discussions on the DDR2 standard" and "things came in, things came out, but by June 2000, we, you know, we had hit a – kind of a stable point."[601] He added that the technical details for the proposed standard were fleshed out between

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[597] *See supra* notes 575 through 579 and accompanying text.

[598] RX 1626 at 4 (e-mail dated April 10, 2000 by Hitachi employee Bob Fusco stating "For DDR-1, it's not too late for minor, carefully considered changes, so I'm open to either proposal [for eliminating programmable CAS latency]"). At the time this e-mail was written, Rambus recently had commenced suit against Hitachi for willful infringement. CX 1855 at 6, 8-9, 11. It is possible that any post-complaint Hitachi documents memorializing an openness to explore non-infringing alternatives may have been influenced by Hitachi's litigation posture.

[599] The e-mail states nothing about changes to programmable burst length, dual-edge clocking, or on-chip PLL/DLL. RX 1626 at 4. Of course, programmable CAS latency was only one of multiple technologies included in the JEDEC standards and later subject to Rambus's patent claims.

[600] Macri, Tr. 4582; CX 376a (March 1998 e-mail announcing "Future dram task group kickoff"); CX 379a (April 1998 Future DRAM Task Group meeting notes).

[601] Macri, Tr. 4598.

June 2000 and June 2001.[602] JEDEC published the DDR2 SDRAM standard to its members in 2002, but final revisions still were being completed in June 2003.[603]

DDR2-based product design and development was in its early stages by 2000. For example, Micron started design work on DDR2 SDRAMs in late 1999,[604] and its first DDR2 design was "taped out" (*i.e.*, ready for initial transfer to masks) in January 2002.[605] The head of JEDEC's Future DRAM Task Group characterized JEDEC deliberations as fluid until first reaching a "stable point" in June 2000.[606] An April 2000 e-mail by Hitachi's Bob Fusco stated, "For DDR-2, we have no legacy to live with, so I like the Micron proposal [to avoid programmable CAS latency]."[607] Complaint Counsel point out that some firms had begun work on DDR2-based products by 2000.[608] However, the scope and extent of DDR2-related efforts is unclear, particularly when one contrasts the unambiguous statements that work had progressed too far to permit change to the SDRAM and DDR SDRAM standards. The evidence suggests that there would have been DDR2 switching costs by 2000, but provides little sense of their magnitude.

Some component manufacturers had started work on DDR2-based complements by 2000. For example, initial JEDEC-level work on the attributes of DDR2-based memory modules began as early as February 1999.[609] However, IBM's Bill Hovis wrote in April 2000 e-mail that, as to DDR2 SDRAM, "[o]bviously here, the situation with the system is that I am not currently locked in . . . ."[610] nVIDIA started work on the first product that it thought might prove DDR2-

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[602] *See* Macri, Tr. 4598-99 ("during June of 2000 to June of 2001, we were adding the meat, you know, the real description that an engineer would need to truly understand these – these concepts").

[603] *See* Rhoden, Tr. 411-12; Polzin, Tr. 4046.

[604] Shirley, Tr. 4211 (*in camera*). IBM's Gordon Kelley explained that design work may begin on aspects of the DRAM that are not covered by JEDEC standards. G. Kelley, Tr. 2590.

[605] Shirley, Tr. 4228 (*in camera*).

[606] Macri, Tr. 4598.

[607] RX 1626 at 4.

[608] *See, e.g.*, Macri, Tr. 4648 (by September 2000 "there were already companies in design on both the DRAM and the systems side"), 4649 (changes at this time would have affected "earliest adopters"), 4650-51; Kellogg, Tr. 5201 (in September 2000 IBM was "moving down the path" of designing its first DDR2-based memory controllers), 5204 (eliminating dual-edge clocking likely would mean "measurable schedule delay" for IBM's memory controller project).

[609] *See* Kellogg, Tr. 5194-95; CX 393.

[610] RX 1626 at 3. The e-mail addressed only issues regarding CAS latency. *Id.* at 3-4.

compatible in late 2000 or early 2001.[611] AMD's Polzin stated that, as of the time of his June 2003 testimony, AMD still had not started to develop an infrastructure for DDR2 SDRAM.[612]

Complaint Counsel stress the industry's desire to maintain backward compatibility. Several industry witnesses expressed concerns that changing DDR2 SDRAM to avoid Rambus's patents would have disrupted backward compatibility.[613] One witness testified that an effort to maintain backward compatibility after eliminating dual-edge clocking would have had "a big impact" from the perspective of design and that a desire to maintain backward compatibility was the reason that a sub-unit of JEDEC's task group in October 2000 chose to maintain dual-edge clocking.[614] Contemporaneous documents confirm that backward compatibility was a general goal, but do not conclusively establish that the decisions to retain Rambus's patented technology resulted from that factor.[615] One such example is the minutes of an October 2000 conference call among members of a sub-unit of JEDEC's Future DRAM Task Group, in which elimination of dual-edge clocking was discussed. The minutes conclude, "Single data rate clock is preferred provided that we can make it work."[616] Although "mak[ing] it work" might have encompassed considerations of backward compatibility, the minutes do not expressly state this. Follow-on testimony from the proponent of the change indicated that ultimately "there was not a lot of

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[611] Wagner, Tr. 3866-67.

[612] Polzin, Tr. 4043-44.

[613] *See, e.g.*, Macri, Tr. 4678 (changing to fixed latency would have been a disruptive departure from DDR SDRAM base), 4624 (on-chip DLL retained "to keep the backwards compatibility"), 4647-48 (similar), 4649 (Macri did not propose eliminating dual-edge clocking because of backward compatibility concerns), 4678-79 (JEDEC task group thought eliminating dual-edge clocking would have been "disruptive"); Kellogg, Tr. 5192-93 (describing consensus desire in 1998 to achieve an "evolutionary solution" that would sustain backward compatibility); Lee, Tr. 6805-06 (very difficult to design a controller that would be compatible with both dual-edge and single-edge clocking).

[614] *See* Macri, Tr. 4640-42, 4780-81 (*in camera*); *cf.* Krashinsky, Tr. 2829 (JEDEC task group rejected alternative to dual-edged clocking because of "the cost that it would be to implement one versus the other" and because the change in clocking rate would have been too "revolutionary").

[615] These documents show that the Future DRAM Task Group decided early on that the next generation of DRAM should "stay backward compatible if at all possible with DDR," CX 392 at 3, and reflect the desire to provide a "migration path" for producers of controllers, CX 379a at 9. The references, however, are too general to reveal how much those considerations shaped the group's specific technology choices. *See also* CX 132 at 4, CX 379a at 9, and CX 2745 at 7 (all indicating that DDR2 SDRAM should be based on DDR SDRAM); CX 2717 at 8, 13 (March 1998 Transmeta Corporation paper urging that change be "evolutionary" and that backward compatibility with DDR SDRAM be maintained).

[616] CX 426 at 4. Macri subsequently interpreted this to mean that "*if* we were to go and do . . . large-scale change" – which, presumably, would have sacrificed backward compatibility – the preference was for eliminating dual-edge clocking. Macri, Tr. 4690-91 (emphasis added).

support," but did not explain the underlying reasons why dual-edge clocking was retained.[617] Based on the existing record, it is difficult to assess how substantially backward compatibility concerns contributed to lock-in in 2000.

In summary, there certainly is evidence that eliminating Rambus's patented technologies from the DDR2 SDRAM standard would have entailed some switching costs for some stakeholders, including, but not limited to, switching costs associated with the desire to preserve backward compatibility.[618] However, the record shows that JEDEC published the DDR2 SDRAM standard in 2002. The causal link between Rambus's course of conduct and the incorporation of its patented technology in the DDR2 SDRAM standard in 2002 is not as well-defined as it is for the SDRAM and DDR SDRAM standards for several reasons.

First, the record as to the magnitude of DDR2 switching costs is not clear; evidence is imprecise and mixed. On the whole, the record fails to establish that most stakeholders had invested heavily in the DDR2 standard by 2000, when Rambus's intentions and patents were disclosed. Second, the circumstances when JEDEC published the DDR2 standard in 2002 were materially different from what they were when the SDRAM and DDR SDRAM standards were adopted. To begin with, Rambus had disclosed both its patents and its intent to enforce them in 2000, at least two years before the DDR2 standard was published. By 2002, Rambus had largely lost the *Infineon* litigation in the trial court.[619] Consequently, the prospect of substantial royalty costs did not loom as the threat it likely would have posed in earlier years (or the threat that it later posed after the Federal Circuit reversed the *Infineon* district court in January 2003).[620] Thus, it seems likely that the DDR2 decisions of JEDEC members would have been impacted by a then-current perception that incorporation of Rambus's allegedly patented technology in JEDEC's DDR2 standard would be relatively costless.

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[617] *See* Lee, Tr. 6802; JX 52 at 45-50.

[618] These considerations rebut the claim that JEDEC's inclusion of Rambus technologies in DDR2 SDRAM demonstrates that those technologies were superior to all alternatives. *See* RB at 52-59; ID at 322-23. Even Rambus recognizes that revealed preference arguments of this nature require that "all other things be[] equal." RB at 60 n.29. Yet in the case of DDR2 SDRAM, other things were *not* equal. Switching costs were present, and JEDEC's choice, at most, revealed a preference for Rambus technologies over alternatives handicapped by those switching costs. Moreover, uncertainties over the breadth and enforceability of Rambus's patents further blurred the comparisons on which Rambus relies. *See infra* notes 619-620 and accompanying text.

[619] The trial court granted Infineon judgment as a matter of law on May 2, 2001. *See* Rambus, Inc. v. Infineon Techs. AG, 318 F.3d 1081, 1086 (Fed. Cir. 2003).

[620] Even then, patent enforceability remained uncertain.

We conclude that the record does not establish a causal link between Rambus's exclusionary conduct and JEDEC's adoption of DDR2 SDRAM.[621]

4. Rambus's Claim that its Acquisition of Monopoly Power Did Not Matter

Finally, Rambus claims that even if its course of conduct enabled it to acquire monopoly power, it cannot be held liable because Complaint Counsel failed to prove competitive harm in the form of supracompetitive (or "unreasonable") prices for consumers. Rambus argues that the royalties paid by DRAM manufacturers are mere wealth transfers, suggesting that the royalties impose only private costs that are irrelevant to overall social welfare. We reject this argument. It fails to acknowledge any decline in DRAM output that might result from higher DRAM prices. Reduced output would constitute a deadweight loss that decreases overall social welfare and raises competitive concerns – as even Teece, Rambus's economic expert, has acknowledged elsewhere.[622]

Rambus also argues that its conduct had no anticompetitive effect because its royalty rates have been reasonable.[623] Substantial record evidence shows that Rambus's royalty rates are

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[621] Although we do not, on this record, find durable monopoly power as to DDR2 SDRAM, neither do we rule it out. It is possible that Rambus did, in fact, obtain durable monopoly power over DDR2 SDRAM. We might have found lock-in with respect to DDR2 SDRAM if the record had demonstrated, for example, that backward compatibility concerns were a substantial determinative factor in JEDEC's DDR2 SDRAM standard-setting decisions.

[622] *See* Teece & Sherry, *supra* note 543, at 1931 n.74 (deadweight loss must be weighed against any real-resource cost savings from use of a patented technology).

The ALJ carried that error one step farther. The Initial Decision relies on a purported admission by Complaint Counsel's economic expert, McAfee, that Rambus's conduct "has had no impact on DRAM prices, no effect on consumers, and no effect on the PC market as of the time of trial . . . ." IDF 1053; ID at 323-24. This misses the point of McAfee's testimony. McAfee actually testified that, although he did not believe there had been an impact on DRAM prices "as of today," (1) Rambus's conduct had substantially increased price in the relevant technology markets and (2) "in the long run . . . those royalty costs would be passed on to consumers" with "the effect of lowering output in the downstream DRAM market" and "the effect of increasing the price." McAfee, Tr. 7175-76, 7565-66. McAfee reasoned that, in the short run, DRAM manufacturers face such high fixed costs that they will maximize the output of their facilities irrespective of royalty levels, but in the long run, higher royalty costs will lead to less DRAM production capacity and higher DRAM prices. *Id*. at 7175-76, 7208, 7749-50; *see also* CX 839 at 2 (1995 Crisp e-mail indicating that Hyundai, a DRAM manufacturer, stated "that they pass on license fees and royalties to their customers"); CX 2107 at 140-41 (Oh FTC Dep.) (*in camera*) (Hyundai's DRAM prices to customers were a function of production costs). Neither the ALJ nor Rambus cite any authority for the proposition that a showing of long-run DRAM output reductions and price increases is insufficient to demonstrate competitive harm. Thus, we find no basis in McAfee's testimony for rejecting Complaint Counsel's showing of competitive harm.

[623] RB at 72-74.

*not* reasonable.[624] Ultimately, however, we need not rest on this evidence. Deceptive conduct that confers durable market power by its very essence harms competition, and claims that the offender has not yet behaved like a monopolist provide no shelter.[625] We therefore reject this argument as a matter of law.

## V. SPOLIATION

Allegations that Rambus engaged in the spoliation of evidence have permeated these proceedings, as well as several private actions relating to Rambus's patent enforcement efforts.[626]

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[624] A comparison of Rambus royalty rates for DDR SDRAM and RDRAM strongly suggests that Rambus's DDR royalties have not been reasonable. Rambus has charged at least a 3.5% royalty on DDR SDRAM, *see, e.g.*, Rapp, Tr. 9853; CX 1680 at 4 (*in camera*), but generally has negotiated royalties between 1.0% and 2.0% for RDRAM. *See, e.g.*, CX 1592 at 21-23 (Samsung RDRAM License); CX 1646 at 10-11 (Micron RDRAM License); RX 538 at 20-22 (NEC RDRAM License); CX 1612 at 4-5 (Hyundai RDRAM License); CX 547 at 12; CX 1057. (RDRAM royalties cover all four of the technologies at issue in this proceeding, as well as additional proprietary technologies. *See, e.g.*, Horowitz, Tr. 8547-48; RX 2183; RX 81 at 8.) Thus, Rambus's 3.5% royalty for DDR SDRAM far exceeds the royalties that were negotiated for RDRAM in a setting in which licensees were aware of Rambus's patent position from the start and, consequently, were sheltered from hold-up.

Rambus attempts to establish the reasonableness of its royalties by comparing them to royalty rates charged for *other* technologies. *See* RB at 73; Teece, Tr. 10422-51. Rambus CEO Tate, however, testified that comparing royalty rates for different technology licenses mixes "apples and oranges" because "[t]he royalty rate for one patent and the royalty rate for another patent, even in the [semiconductor] industry, can vary tremendously based on the value of the patent and the applications involved." CX 2060 at 158 (Tate *Infineon* Dep.) (*in camera*). Rambus fails to provide a basis for treating the referenced licensing arrangements as comparable to licenses for the technologies at issue in the present case. *See* Teece, Tr. 10465-66 (unable to identify any comparative data that involved royalties on DRAM interface technologies), 10644-46, 10659-60 (acknowledging "a lot of heterogeneity" in royalty rates).

Both Rambus and the ALJ highlight a comparison to IBM's patent licensing policy. They state that IBM charged royalties of 1-5% and that Rambus's rates fit well within this range. RB at 73-74; IDF 1548-53; ID at 324-25. The record contains no evidence, however, that IBM's rates reflected royalties for DRAM technologies, or even that the rates stated in IBM's policy ever actually applied. *See* Teece, Tr. 10638-40 (acknowledging that IBM usually cross-licensed without a cash rate). Indeed, even the IBM policy cited by Rambus gave licensees a potentially much less costly option: licensees could choose an 8% royalty based solely on the portion of the selling price attributable to the patented portions of the licensee's product. JX 9 at 24. For a DRAM, in which the four relevant interface technologies are only a small part, the IBM policy might result in only a minimal royalty.

[625] *See* United States v. Microsoft Corp., 253 F.3d 34, 56-58, 76-77 (D.C. Cir.), *cert. denied*, 534 U.S. 952 (2001), quoting Berkey Photo, Inc. v. Eastman Kodak Co., 603 F.2d 263, 274 (2d Cir. 1979), *cert. denied*, 444 U.S. 1093 (1980) ("[I]f monopoly power has been acquired or maintained through improper means, the fact that the power has not been used to extract [a monopoly price] provides no succor to the monopolist."); American Tobacco Co. v. United States, 328 U.S. 781, 809, 811 (1946); *see also* III AREEDA & HOVENKAMP, ANTITRUST LAW, ¶ 651d1 at 80 ("Properly defined monopolizing conduct harms consumers by creating monopoly, increasing its amount, or extending its duration. Thus, an expectation of consumer harm must always be at the logical end of any determination that a particular act 'monopolizes,' and thus satisfies §2's conduct requirement.").

[626] *See supra* Section II.B. (discussing the relevant procedural history).

Many of the basic facts are not in dispute.[627] Rambus began formulating its document retention policy in early 1998 with the assistance of outside counsel,[628] and adopted a document retention policy in July 1998.[629] Rambus then conducted company-wide "shred days" in September 1998 and August 1999 that involved the destruction of significant quantities of documents.[630] Rambus destroyed a similarly large volume of documents in December 2000 when it moved to a new office building.[631] As part of its document destruction efforts, Rambus deleted e-mails,[632] erased computer backup tapes,[633] and instructed its outside patent counsel, Lester Vincent, to clean out his law firm's patent prosecution files so that they mirrored the PTO's file.[634]

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[627] Our discussion draws upon evidence developed in the *Infineon* litigation, pertaining to the nature and extent of Rambus's document destruction effort. This evidence was admitted in this proceeding by a reopening of the record. *See* CX 5000-85; DX 500-07; RX 2500-53; *see also supra* Section II.B.1.d.

[628] *See* CX 5005 at 3; CX 5006 (designated R401111); CX 5007; CX 5069 at 11 (deposition transcript at 376) (Karp 2004 *Infineon* Dep.); CX 5068 at 4-5 (deposition transcript at 26-33) (Savage 2004 *Infineon* Dep.); RX 2502 (March 1998 Rambus memorandum regarding "Document Retention Policy Guidance"; RX 2521 at 11-12 (Johnson *Infineon* Dep.).

[629] *See* RX 2503; CX 2102 at 362 (Karp *Micron* Dep.).

[630] Rambus destroyed 185 burlap bags and 60 boxes full of documents on September 3, 1998. CX 5023 (designated R401307); CX 5050 (designated R400812). Rambus destroyed approximately 150 burlap bags of documents on August 26, 1999. CX 5052 (designated R400819).

[631] *See* CX 5053 (designated R400787) (Rambus destroyed 410 burlap bags) .

[632] *See* CX 1264 at 1 ("EMAIL – THROW IT AWAY"); Diepenbrock, Tr. 6230-32.

[633] *See, e.g.,* CX 5018.

[634] *See* CX 5033; CX 5036; CX 5037 (designated BSTZ 41); CX 5069 at 49 (deposition transcript at 540-41) (Karp 2004 *Infineon* Dep.). (BSTZ refers to Bates stamp numbers that appear on this and other exhibits admitted into this record from the *Infineon* litigation.)

The record shows that key Rambus executives and lawyers – including Richard Crisp,[635] Joel Karp,[636] Billy Garrett,[637] Anthony Diepenbrock,[638] and Lester Vincent[639] – destroyed documents. The record also shows that some of these documents related to subject matter pertinent to this proceeding, such as documents regarding Rambus's participation in JEDEC,[640] and Rambus's patent prosecution files.[641] Indeed, Rambus's document destruction efforts were so thorough and effective that neither Crisp nor Rambus's attorneys were able to find certain JEDEC-related documents when they subsequently searched for them.[642]

In order to establish pre-litigation spoliation, Complaint Counsel must show that Rambus destroyed potentially relevant documents at a time when litigation was reasonably foreseeable.[643] The destruction must have occurred with a culpable state of mind.[644] The appropriate remedy in

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[635] *See* Crisp, Tr. 3425, 3427-30; CX 2082 at 157-59 (deposition transcript at 841-43) (Crisp *Infineon* Dep.) *(in camera)* ("anything that I had on paper, I basically threw away"); CX 5059 (designated GCWF 3456). (GCWF refers to Bates stamp numbers that appear on this and other exhibits admitted into this record from the *Infineon* litigation.)

[636] *See* CX 2059 at 62 (Karp *Infineon* Dep.) (*in camera*); CX 2102 at 115 (deposition transcript at 378) (Karp *Micron* Dep.).

[637] *See* CX 5062 (designated GCWF 3422).

[638] *See* CX 5064 (designated GCWF 3439); Diepenbrock, Tr. 6235-36.

[639] *See* CX 5033; CX 5036; CX 5037 (designated BSTZ 41).

[640] *See* CX 5062 (designated GCWF 3416); CX 5078 at 14 (trial transcript at 124), 20 (trial transcript at 146).

[641] *See* CX 5033; CX 5036; CX 5037 (designated BSTZ 41); CX 5069 at 49 (deposition transcript at 540-41) (Karp 2004 *Infineon* Dep.).

[642] *See* CX 1079 at 1 (Crisp October 1999 email: "I'm looking for a copy (paper or electronic) of one of the original DDR datasheets from the 1996/1997 timeframe. Hopefully someone here has one that hasn't fallen victim to the document retention policy :-)"); CX 5078 at 20 (trial transcript at 146).

[643] *See* Silvestri v. General Motors Corp., 271 F.3d 583, 590 (4th Cir. 2001); Byrnie v. Town of Cromwell, 243 F.3d 93, 107-112 (2nd Cir. 2001). *See also* MARGARET M. KOESEL ET AL., SPOLIATION OF EVIDENCE: SANCTIONS AND REMEDIES FOR DESTRUCTION OF EVIDENCE IN CIVIL LITIGATION 4-5 (Am. Bar Ass'n 2000).

[644] Courts have articulated this requirement in varying terms. *See, e.g.*, *Silvestri*, 271 F.3d at 590 ("some degree of fault"), 593 ("deliberate or negligent"); *Byrnie*, 243 F.3d at 108 ("intentional[]," "in bad faith," or "based on gross negligence"), 109 ("knowingly . . . or negligently").

any particular case typically will vary, depending on the spoliating party's degree of fault as well as the extent to which the other party is prejudiced.[645]

In the present case, we need not resolve whether Rambus engaged in spoliation because the record shows, by a preponderance of the evidence, that Rambus engaged in exclusionary conduct. Our findings stand firmly on the evidence that has survived. No remedy for the alleged spoliation is necessary, and we therefore do not undertake the inquiry required to resolve the spoliation issue.[646]

We stress, however, that Rambus's extensive document destruction campaign had the potential to deny the Commission an opportunity to examine thoroughly Rambus's conduct. In some instances, the Commission has relied on evidence that was preserved only fortuitously.[647] If the record in this case had been marginal, while simultaneously containing evidence that Rambus had destroyed potentially relevant documents, we would have pursued the spoliation inquiry to its conclusion and, if appropriate, imposed a remedy. The Commission has a broad range of remedies available to address spoliation, ranging from drawing adverse inferences to ordering that a proceeding be decided against the spoliating party. If spoliation were proven in a future case, the Commission would not hesitate to impose warranted sanctions, in keeping with its fundamental interest in preserving the integrity of its administrative proceedings.

## VI. CONCLUSION

We find that Rambus engaged in exclusionary conduct that significantly contributed to its acquisition of monopoly power in four related markets. By hiding the potential that Rambus would be able to impose royalty obligations of its own choosing, and by silently using JEDEC to assemble a patent portfolio to cover the SDRAM and DDR SDRAM standards, Rambus's conduct significantly contributed to JEDEC's choice of Rambus's technologies for incorporation in the JEDEC DRAM standards and to JEDEC's failure to secure assurances regarding future

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[645] *See* Residential Funding Corp. v. DeGeorge Financial Corp., 306 F.3d 99, 107 (2d Cir. 2002); Schmid v. Milwaukee Electric Tool Corp., 13 F.3d 76 (3d Cir. 1994).

[646] Accordingly, Complaint Counsel's pending motion for sanctions is denied. Complaint Counsel's Motion for Sanctions Due to Rambus's Spoliation of Documents (Aug. 10, 2005), *available at* http://www.ftc.gov/os/adjpro/d9302/050810ccmosanctions.pdf.

[647] For example, the only sources of Crisp's JEDEC-related e-mails were a hard drive found in Crisp's attic, *see* CX 5075 at 3-5 (deposition transcript at 296-302) (Crisp 2004 *Infineon* Dep.), and an old Rambus server that Crisp had used to transfer e-mails between his Macintosh and PC office computers. *See* Crisp, Tr. 3572-76, 3588-92; CX 5078 at 14 (trial transcript at 124). Likewise, although Rambus's outside patent counsel, Vincent, destroyed most of his Rambus-related files, he retained certain relevant correspondence in his personal files. *See* CX 5066 (designated GCWF 3448). In addition, records that Rambus failed to produce in the normal course of discovery were retrieved from corrupted back-up files in the subsequent *Hynix* litigation, and the Commission was able to add this evidence to this proceeding's record on appeal. *See* CX 5100-16; *see also supra* Section II.B.

royalty rates – which, in turn, significantly contributed to Rambus's acquisition of monopoly power.

Rambus claims that the superiority of its patented technologies was responsible for their inclusion in JEDEC's DRAM standards. These claims are not established by the record. Nor does the record support Rambus's argument that, even after two JEDEC standards were adopted and substantial switching costs had accrued, JEDEC and its participants were not locked into the standards. Rambus now claims that we can and should blind ourselves to the link between its conduct and JEDEC's adoption of the SDRAM and DDR SDRAM standards, as well as to the link between JEDEC's standard-setting process and Rambus's acquisition of monopoly power. These claims fail, both as a matter of fact and as a matter of law. To hold otherwise would be to allow Rambus to exercise monopoly power gained through exclusionary conduct. We cannot abide that result, given the substantial competitive harm that Rambus's course of deceptive conduct has inflicted.

## VII. REMEDY

Complaint Counsel seek an order preventing Rambus from enforcing, against JEDEC-compliant products, (1) any patents that claim priority based on applications filed before Rambus withdrew from JEDEC and (2) any existing licensing agreements.[648] Rambus argues that the Commission lacks authority to impose such a remedy and that the royalty rates set by its existing licenses already satisfy all remedial concerns.[649]

Both parties' arguments regarding remedy have been scant and, for the most part, reflective of opposing extremes.[650] Now that the Commission has found, and determined the scope of, liability, the Commission believes it would exercise its broad remedial powers most responsibly after additional briefing and, if necessary, oral argument devoted specifically to remedial issues.

The accompanying order establishes a briefing schedule. The parties' written presentations directed by the accompanying order will be confined to remedy; re-argument of issues of liability will not be permitted in those presentations. The Commission is most interested in the parties' views regarding possibilities for establishing reasonable royalty rates for JEDEC-compliant products affected by Rambus's exclusionary conduct. The parties should

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[648] CCAB at Attachment 2; CCRB at 95-100.

[649] RB at 128-33.

[650] *See generally* United States v. National Lead Co., 332 U.S. 319 (1947) (rejecting the imposition of compulsory, royalty-free licenses when they were not "necessary in order to enforce effectively the Anti-Trust Act," and finding that "licenses at uniform, reasonable royalties" would be sufficient to accomplish the discontinuance and prevention of the illegal restraints). For discussion of Rambus's existing royalty rates, *see supra* Section IV.C.4.

address, without limitation: (1) means for the Commission to determine, based on the existing record, reasonable royalty rates for licensing all technologies applicable to JEDEC-compliant products and covered by relevant Rambus patents; (2) alternative mechanisms and procedures for determining reasonable royalty rates, such as an independent arbitrator, a special master, or an ALJ; (3) qualitative characteristics descriptive of appropriate relief, against which specific royalty proposals might be evaluated; and (4) appropriate injunctive and other provisions that should be incorporated in the Final Order in this proceeding.