

MEMS microphone electrical implementation

About this document

Scope and purpose

This document covers important information about analog and digital microphone electrical interfaces and signal requirements. It also imparts information about important parameters like Acoustic Overload Point (AOP), Signal to Noise Ratio (SNR), dynamic range, sensitivity and bandwidth.

Intended audience

Infineon XENSIVTM MEMS microphone customers.

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1 Abstract

1 Abstract

Electrical implementation is a critical microphone success factor, alongside acoustical and mechanical implementation. Microphones need a high-performance output signal path and a working environment that enables getting the best possible signal quality out of the system.

Optimizing signal quality includes, for example:

- A high-performance signal path that is able to carry the microphone output signal without degradation in noise level, frequency response, phase performance, dynamic range, or other key parameters
- A clean and steady power source
- A clean, steady, low-impedance ground
- Well protected, clean signal lines
 - Protection from external disturbances, such as conducted and radiated RF signals
 - Separation from other data traces to avoid crosstalk
- Isolation from other noisy electrical systems in the device
- A reasonable electromagnetic radiation environment
- A high-quality clock signal (for digital microphones)

In this application note, we go through key information and guidelines for the electrical implementation of MEMS microphones into systems such as smartphones, smart speakers, IoT devices and laptops. Some of the information is divided into two sections based on the output format of the microphone, analog or digital.

Analog signals are significantly more susceptible to disturbances than digital signals. Therefore, the tasks of implementing analog and digital microphones into a device differ significantly. Typically, it takes more time and effort to achieve a high performance level with analog microphones than with digital microphones. The design of the circuitry, board layout and wiring are much more critical tasks in the analog domain than they are in digital. Achieving a satisfactory result with analog microphones requires experience, careful design work, prototyping and often several design iterations. With digital microphones, the rules are more straightforward.

Due to the easier implementation, the popularity of digital interface microphones has risen, especially in bigger devices and devices in which the electromagnetic environment is especially hostile. For example, laptop microphone traces tend to be long and they run next to disturbance sources so digital microphones are used practically exclusively in that product category.



2

Electrical implementation of analog microphones

2.1 Analog microphone interfaces

There are two commonly used interfaces for analog MEMS microphones: single-ended and differential. Singleended has dominated the market until recent years but differential has recently gained more popularity due to increased performance requirements (for example, dynamic range) and the need for better signal robustness against disturbances.

The **single ended interface** is a simple and low cost solution. The microphone requires only three pins: VDD, signal and ground. Singleended interfaces do not offer significant protection against disturbances, such as radio frequency interference, cross talk from other signal lines, or differences in ground voltages between the sending and receiving ends.

A **differential interface** transmits the microphone output signal divided into two complementary signal lines with opposite polarities. The effective signal V_{out} at the receiving end is the difference between the two signals. Therefore, differential interface offers a 6dB higher dynamic range than single-ended (assuming same interface rail voltage and same sensitivity for both MEMS sensors). In other words, a differential interface doubles the dynamic range of the interface. The key benefit in a differential interface, what comes to interference, is that disturbances in the two complementary signal lines are (ideally) the same and they get canceled from the signal when received with a differential amplifier. The electromagnetic field around an ideal differential line is zero, so a well-designed differential interface also reduces disturbances emitted by the microphone output signals to other traces. Good disturbance rejection performance requires that the two signal traces are well matched (balanced impedance, matched trace layout).

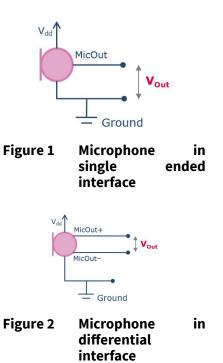


Figure 3 shows two examples of analog microphone interfaces. The single-ended interface on the left is an interface to an audio codec. The differential interface is an interface with a differential amplifier. Both circuits include a 0.1μ F capacitor (a higher capacitance can be used, up to 10μ F) to filter disturbances from the supply voltage line. Additional smaller value capacitors (50 - 100pF) may be needed on the power supply line to filter out RF disturbances. Typically, the power supply filtering capacitors should be placed physically as close to the microphone as possible, the smallest value one closest to the microphone. There are also series capacitors (>1 μ F) in the output lines to filter possible DC component out of the signal.

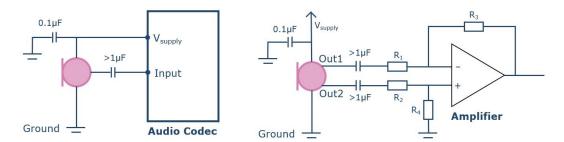


Figure 3 Single ended (left) and differential (right) analog microphone interface examples

See more details on microphone signal protection in section '*RF disturbance mitigation*'.

Note: A differential interface should be chosen instead of a single-ended when high disturbance immunity or high dynamic range is needed.



2.2 Device microphone signal path requirements - dynamic range

A key success factor in high performance analog microphone interfaces is making sure that the dynamic range of the signal path does not limit the performance of the microphone. The maximum signal swing of an analog microphone output can be calculated using the sensitivity (output voltage with a 94dBSPL (1Pa) *rms acoustic reference signal* input) and the acoustic overload point (AOP) of the microphone. The AOP of a microphone can be specified either as a *peak* value or as an *rms* value. For output voltages, we concentrate on *peak* or *peak-to-peak* values when calculating maximum signals levels.

The *rms sensitivity* of an analog microphone can be calculated with the equation below, where $Sensitivity_{mV/Pa(rms)}$ is the output voltage of the microphone with a 94dBSPL_{rms} reference sound input.

$$Sensitivity_{dBV} = 20 \times \log_{10} \left(\frac{Sensitivity_{mV/Pa(rms)}}{1000mV/Pa} \right)$$

The *rms output voltage* measured with the 94dBSPL_{rms} sound input can be derived from the equation above:

 $\Leftrightarrow V_{output(rms)@94dBSPL(rms)} = Sensitivity_{mV/Pa(rms)} = 10^{\left(\frac{Sensitivity_{dBV}}{20}\right)} V$

If the AOP sound pressure level is specified for the microphone as a *peak* value (AOP_{peak}), the *peak* output voltage of the microphone at the AOP can be obtained by calculating the *difference (in decibels) between* AOP_{dBSPL(peak)} and 94dBSPL_{rms} and adding it to V_{output(rms)@94dBSPL(rms)}.

$$V_{output(peak)@AOP(peak)} = 10^{\left(\frac{Sensitivity_{dBV} + (AOP_{dBSPL(peak)} - 94dBSPL_{rms})}{20}\right)}V$$

If the AOPSPL is given as an *rms* value (AOP_{rms}), the *peak* AOP output voltage can be calculated by adding +3dB to $V_{output(peak)@AOP(peak)}$ (see *Figure 4*).

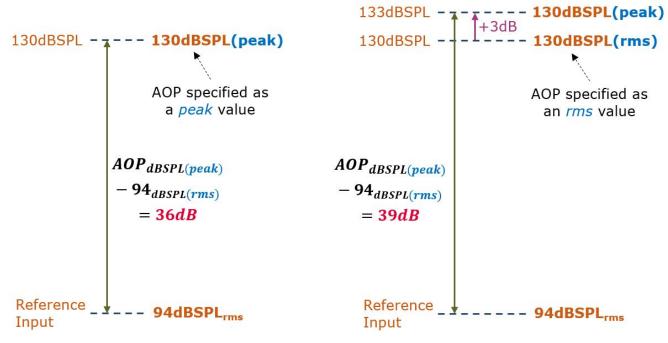


Figure 4 Difference between AOP (peak) and AOP(rms) on the microphone sensitivity

 $V_{output(peak)@AOP(rms)} = 10^{\left(\frac{Sensitivity_{dBV} + (AOP_{dBSPL(peak)} - 94dBSPL_{rms}) + 3dB}{20}\right)}V$

The *peak-to-peak* signal voltage swing can be calculated by doubling the *peak* value. For example, for a microphone with Sensitivity -38dBV and AOP_{peak} 130dBSPL, the maximum *peak-to-peak* output voltage is:



$$V_{output(p-p)@130dBSPL(peak)} = 10^{\left(\frac{-38dB_V + (130dB_{SPL(peak)} - 94dB_{SPL(rms)})}{20}\right)} V \times 2 = 1.6V$$

This peak-to-peak voltage swing might barely be compatible with a single-ended interface that has a 1.8V rail voltage and maximum signal swing of approximately 1.6V (from 0.1V to 1.7V; the practical maximum and minimum signal values are typically about 100mV from the theoretical rail voltages). However, if the sensitivity tolerances for the microphones are ±1dB, the sensitivities of the outlier microphones could be -37dBV. The resulting V_{output(p-p)@AOP(peak)} is 1.8V and the interface runs out of dynamic range.

If the AOP_{dBSPL} is specified as an *rms value*, the *peak* AOP signal level is 3dB higher. For example, if the *rms AOP* is 130dBSPL, the *peak AOP* is 133dBSPL. If the sensitivity of the microphone is -38dBV like in the example above, the maximum peak-to-peak voltage swing increases from 1.6V to over 2.2V. This is no longer compatible with a 1.8V single-ended interface.

In example case (1) (see *Figure 5*) below, the sound pressure coming into the microphone is too high for the microphone and/or the microphone signal chain so the signal gets distorted, clipped. The problem can be mitigated by:

(a) lowering microphone sensitivity

(b) increasing signal path rail voltage or

(c) switching from a single-ended to differential interface

It should be noted that lowering the sensitivity of the microphone may affect important parameters such as SNR and the microphone system's ability to capture low level / distant sounds.

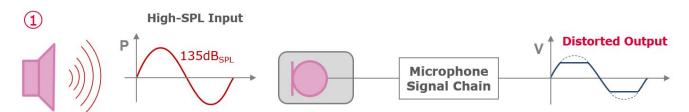


Figure 5 Effect of high SPL input on the microphone output

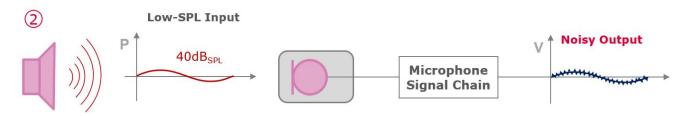
The noise floor of the whole microphone signal chain must be low enough to support the noise performance of the microphone. In some cases, some parts of the microphone signal path, such as an input of a codec, may not support very low signal levels. Signal levels may be low because, for example, the sensitivity of the microphone is low and the incoming sound pressure level is low (for example, if the sound source is relatively quiet and/or far away). The result may be that the microphone signal gets buried in the noise floor of the signal path.

In example case (2) (see *Figure 6*) below, the incoming sound is very quiet (roughly equivalent of a person talking from an 8-meter distance) and the SNR of the output of the microphone system is very low due to the noisiness of the signal path. The problem can be mitigated by:

(a) choosing a microphone with a higher sensitivity (and preferably the same noise floor)

(b) amplifying the microphone output signal before the noisy parts of the signal chain or

(c) reducing the noise floor of the signal chain by choosing lower-noise components and making sure disturbances do not contaminate the lines







In a smartphone, low microphone sensitivity may make it more difficult to pass send distortion tests that are part of the type approval process. On the other hand, increasing the signal level may cause signal headroom problems (see *Figure 5*). As can be seen from the examples here, the sensitivity of the microphones used in a system is often a compromise between high and low SPL capturing capabilities.

2.3 Device microphone signal path requirements - bandwidth

The DC filtering capacitors in the microphone output signal path must be sized so that they don't limit signal bandwidth. ≥1µF components are typically good for this purpose. Also, all the other components in the signal chain must support the microphone output bandwidth. This is especially noteworthy if the intended bandwidth goes beyond 20kHz (ultrasound).

3 Electrical implementation of digital microphones

The same guidelines on protecting and filtering signal connections apply to digital microphones as for analog ones. However, due to the robustness against disturbances of digital signals, there is typically less need for protecting and cleaning the microphone output signal. In many cases, digital microphones enable a reduction in the amount of design work, prototyping, redesigns and filtering components while still achieving a similar or better signal quality as an analog microphone. Digital interfaces are especially beneficial in challenging electromagnetic environments in wirelessly connected devices such as smartphones, tablets, smart speakers and IoT devices. Digital signals also enable using longer trace lengths without problems so they are well suited for large devices, such as laptops, that can have long signal connections.

A drawback of digital interfaces is the higher current consumption of the microphones and the interface as compared to analog interfaces. However, the current consumption for the whole system is not necessarily higher since the analog to digital conversion has to be done at some point in the signal chain also for analog microphones.

Even though implementing digital microphones is in many cases easier than analog microphones, the system designer still has to know what she or he is doing. Analog signals (Vsupply, ground) must be kept stable and clean and digital signal connections must be implemented properly to ensure seamless operation.

3.1 PDM interface

The most common digital interface in MEMS microphones is PDM (Pulse Density Modulation). It is a 1-bit interface. A PDM interface is simpler and cheaper than other digital alternatives. A key simplicity factor is that a PDM interface does not require having a decimator in the microphone. This saves chip area, cost and current consumption in the microphone. The delay caused by the analog to digital conversion is very small in PDM microphones.

A PDM interface consists of two interface signals: Clock and Data. The L/R (left/right) select pins enable using two microphones in the same data line by connecting the pins to either ground or Vsupply. With supply voltage and ground, the total microphone pin count is 5.

3.2 Signal connections

As explained in *Electrical implementation of analog microphones*, signal connection circuit and trace designs are critical for analog microphones. They are equally important for digital microphones, but for different reasons. All traces on a circuit board have impedance. The very high frequencies (up to hundreds of megahertz) caused by sharp digital signal edges in the clock and data signals of digital microphones are affected significantly by those impedance. Also, the outputs and inputs of the components that send and receive signals to and from each other play a big role in maintaining the signal quality. The principles for designing and executing signal connections that do not degrade digital signal quality are relatively straightforward. The key principles are as follows.

The output of the component sending a signal (source) has to match the signal line it drives. A mismatch can cause issues like overshoot, undershoot, reflections and ringing. These can lead to unpredictable signal levels and bit errors as well as emitted disturbances that can affect adjacent systems. Bit errors lower the performance of the microphone system. Ringing, overshoot and undershoot can cause minimum and maximum



signal levels to be significantly lower or higher than anticipated. The resulting levels may violate the absolute maximum ratings specified for the microphone (or other parts of the system).

To avoid problems, the impedance of the clock and data traces should be controlled. The impedance of a trace depends on its dimensions and the materials used in the circuit board. Circuit design tools can be used to design controlled impedance traces, for example between 50 and 100 Ohms.

Source Termination Resistors

- Source termination resistors are used to match the impedance of the source and the trace
 - The resistors are placed in series with the trace, close to the source
 - The component values of the termination resistors depend on the properties of the trace they are on; typical values range from 50 to 100 Ohms
- Clock line source termination resistors (R_{TC}) (1) keep the signal edges clean of overshoot and ringing and help avoid interface timing issues, emitted interference and increased current consumption
- Termination resistors are added also on the data lines (R_{TD}) (2) to avoid timing issues and bit errors Filtering Capacitors
- V_{supply} interference filtering capacitors (C_{PS}) (3); a typical value is 0.1µF but up to 10µF is possible
- RF disturbance filtering capacitors (C_{RF}) (4) for V_{supply}
 - Several may be needed, each to filter out a specific interference frequency
 - The capacitors are typically small value, 10 500pF
- The smallest value filtering capacitor should be placed closest to the microphone
- The trace lengths connecting the capacitors to the power plane should be as short as possible (5); avoiding traces altogether and using vias directly from pads is recommended
- Inductance should be minimized in the capacitor traces (5) to maximize filtering performance
- Some capacitor types (e.g. those based on class 2 dielectrics) can generate acoustic noise
 - They should not be used in close proximity to microphones

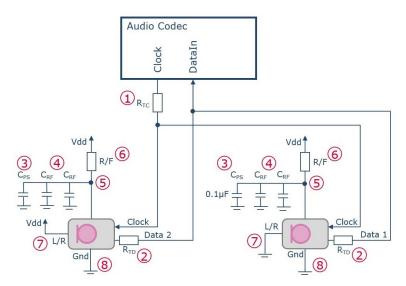


Figure 7 Example of digital microphone and audio codec interface

Other Guidelines

- A series resistor or ferrite (R/F) (6) can be added to the power supply line for each microphone to suppress or filter the amount of high frequency electromagnetic interference (EMI) noise
- Traces from the L/R pins on the microphones to Vdd and Ground (7) should be short
- Microphone grounds (8) should be connected to the circuit board ground plane with vias that are directly on the microphone ground pad; traces should be avoided
- Microphone data and clock lines should be kept separate from high-speed transmission lines

In the configuration shown above, both microphones are powered on or switched to other power modes (e.g. Normal mode <-> Low power mode, controlled by the clock frequency) simultaneously. Switches or AND-gates can be used together with GPIO outputs (general-purpose IO) of the codec to control the power and clock to each microphone individually.

3.3 Digital clock and bandwidth of a PDM interface

Digital microphones need a clock signal from the host device. The clock sets the timing for the binary data output of the microphone. The allowed clock frequencies are specified in component data sheets.

The bandwidth of a PDM interface is limited by its clock frequency because of the increase in quantization noise at higher microphone output signal frequencies. A high clock frequency enables noise shaping, i.e. pushing the noise out of the audio frequencies to higher frequencies that are made available by the higher clock frequency. Oversampling ratio (OSR, decimation factor) is the ratio of the PDM interface clock frequency to the baseband sampling rate. A typical OSR is 64 but there is no defined standard. According to the Nyquist theorem, the sampling rate must be twice the audio bandwidth (BW, the highest used audio frequency). The OSR and the bandwidth determine the required clock frequency:

$$f_{clock} = 2 \times BW \times OSR \iff Bandwidth = \frac{f_{clock}}{2 \times OSR}$$

The minimum clock frequency needed for the full audio band (20Hz – 20kHz) is 2.56MHz (with OSR 64). The commonly used 2.4MHz clock enables an 18.75kHz audio bandwidth (with OSR 64).

Some standard audio sampling rates exist and example can be found in *Table 4*.

Using high ultrasonic frequencies requires the PDM interface clock frequency to be significantly higher than for audible frequencies. A 40kHz bandwidth (with OSR 64) requires a 5.12MHz or higher clock frequency.

3.4 L/R channel multiplexing

Left/right channel multiplexing is done by using the rising and falling clock signal edges to drive two microphones (channels). The multiplexing works so that at on each clock edge one microphone is transmitting and the other is in a high-impedance state. For example, on a rising clock signal, Data_L channel asserts (writes) data onto the data line and Data_R goes into a high-impedance (HiZ) state. Similarly, on a falling clock signal, channel Data_R asserts data and Data_L goes into a high-impedance state.

When in the high-impedance state, the microphone is electrically invisible to the output data line. This allows each microphone to drive the contents of the data line while the other one is waiting quietly for its turn (in HiZ state).

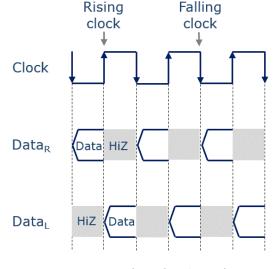


Figure 8 L/R channel multiplexing for using two microphones on a single DATA line

Note: The clock frequency of a PDM interface must be high enough not to limit the frequency band of the microphone. For a system with OSR = 64 the clock frequency must be 128 times the desired microphone output bandwidth.





3.5 Digital timing

When implementing different microphone models or microphones from several suppliers into the same device, it is very important to make sure their interface properties allow them to work together seamlessly. For example, when using two PDM microphones on one data line, their timing parameters must be compatible. Naturally, also the timings of the microphone system and the microphones must match.

Table 1 shows an example set of timing parameters from Infineon's IM69D130 microphone data sheet.

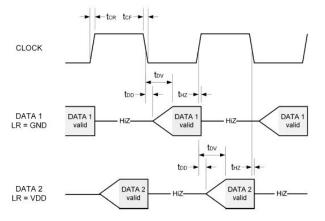


Figure 9

Digital timing for implementing two microphones on the DATA line

Parameter	Symbol	Values		Unit	Note or	Description	
		Min.	Max.		Test Condition		
PDM clock frequency	f _{clock}	0.35	3.3	MHz		Defines the sampling rate and the rate at which bits are transmitted on the data line	
Clock duty cycle		40	60		f _{clock} <2.75 MHz	The ratio of clock high to one clock period, given as a percentage (%).	
		48	52	- %	f _{clock} ≥2.75 MHz	Different duty cycles may be specified for different clock frequencies.	
Clock rise/fall time			13			The maximum time it takes for the clock signal to rise and fall.	
				ns		The exact voltage levels from which the time is measured may be specified together with the rise / fall time.	
Delay time for DATA driven	t _{DD}	40	80	ns	Delay time for CLOCK edge (0.5 x V _{DD}) to DATA driven	Delay time from when the clock edge is at 50% of supply voltage (0.5 x VDD) to when data is driven on the data line.	
Delay time for DATA high-Z ¹⁾	t _{HZ}	5	30	ns	Delay time for CLOCK edge (0.5 x V _{DD}) to DATA high impedance state	Delay time from when the clock edge is at 0.5 x VDD to when the data output of the microphone switches into a high impedance (HiZ) state. In the high-impedance state the microphone allows the other microphone to drive the data line.	

Table 1 Common digital timing parameters



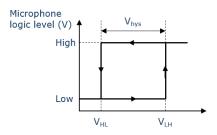
Parameter	Symbol	Values		Unit	Note or	Description
		Min.	Max.	_	Test Condition	
Delay time for DATA valid ²⁾	t _{DV}		100	ns	Delay time for CLOCK edge (0.5 x V _{DD}) to DATA valid (<0.3 x V _{DD} or>0.7 x V _{DD}	Delay time from when the clock edge is at 0.5 x VDD to when the data driven by the microphone on the Data line is valid (accurately readable). The voltage levels for valid 0 and 1 should be specified; e.g. 0 is < 0.30 x VDD and 1 is > 0.70 x VDD.

Table 1 Common digital timing parameters (continued)

3.6 Digital I/O levels

In addition to timing parameters, also the IO (input / output) voltage levels of microphones must be specified to make sure the microphones work as intended within the system together with other microphones. Choosing the correct levels helps minimize the amount of data errors (cases where the output of the microphone is interpreted as a 1 when the microphone is actually giving 0 as an output, or vice versa).

The properties of the Data line affect the functionality of the interface. Therefore, the maximum output load capacitance on the Data line (C_{load}) that the microphone is capable of driving is typically also specified in microphone data sheets. The data line in the device should be compatible with the required max C_{load} .



The Data pin of the microphone is typically specified to be in a high-impedance state when the microphone is in standby mode.

Figure 10 Hysteresis in microphone logic level shift

The hysteresis in microphone logic level shifts from 0 to 1 and back is shown in the illustration on the right. Key IO parameters for PDM microphones are listed in the table below. The table on the next page shows an example set of IO parameters from Infineon's IM69D130 microphone data sheet.

Parameter	Symbol	Symbol Values		Unit	Note or	Description	
		Min.	Max.	_	Test Conditio n		
Input logic level	V _{IL}	-0.3	0.35 x V _{DD}	V		The range of voltages the microphone interprets as a 0 (logic low).	
Input logic high level	V _{IH}	0.65 x V _{DD}	V _{DD} + 0.4	V		The range of voltages the microphone interprets as a 1 (logic high).	
Hysterisis width	V _{hys}	0.1 x V _{DD}	0.29 x V _{DD}	V		The difference between the low->high and high->low thresholds (VLH / VHL) (see drawing).	

Table 2Common IO level parameters



Parameter	Symbol	Values		Unit	Note or	Description	
		Min.	Max.	_	Test Conditio n		
Output logic low level	V _{OL}		0.3 x V _{DD}	V	I _{out} =2mA	The range of microphone output logic voltages that represent a 0 (logic low).	
						The output current lout should also be specified.	
Output logic high level	V _{OH}	0.7 x V _{DD}		V	I _{out} =2mA	The range of microphone output logic voltages that represent a 1 (logic high)	
						The output current I _{out} should also be specified	
Output load capacitance on DATA	C _{load}		200	pF			

Table 2 Common IO level parameters (continued)

3.7 Device microphone signal path requirements - dynamic range

The output of a PDM MEMS microphone is converted into an analog signal for human ears (by low-pass filtering) or a PCM (pulse code modulated) digital signal that is passed on in the device system. For example, DSP systems accept PCM as their input (but cannot handle PDM).

Conversion to PCM is done with a decimator that uses digital filtering downsample the signal according to the oversampling rate. The sample rate reduction increases the word length of the digital signal so the resulting baseband rate PCM signal is no longer a 1-bit signal. Typical resulting word lengths are 16, 20 or 24 bits. The aliasing to audible frequencies of the noise at ultrasonic frequencies in the PDM signal must be prevented by using decimation filters. The decimator system can be included in the microphone for PCM output. PCM/I2S microphones have not gained as much popularity as microphones with PDM outputs.

Two key parameters of a microphone are Signal to Noise Ratio (SNR) and Acoustic Overload Point (AOP). These parameters reflect the quietest sound a microphone can handle (SNR) and the loudest sound a microphone can detect while maintaining a reasonable distortion level (AOP; the sound pressure level at which THD rises above 10%). By combining these two parameters we can determine the entire range of sound levels which a microphone can detect, from the noise floor to the overload point; see illustration on the right.

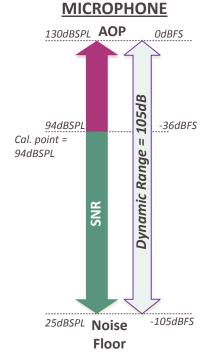


Figure 11 Dynamic range and SNR representation of Infineon digital microphone

For PCM-based audio system components, such as ADCs and codecs, Dynamic Range and SNR are measured in a significantly different way to a microphone SNR. Microphone SNR is defined as the difference (in dB[A]) between the microphone output when the acoustic input is a 1kHz sine wave at 94dBSPL and when there is no acoustic input to the microphone (noise floor). This is because microphone SNR is a measurement of the audibility of the microphone self-noise, so it is referred to a defined acoustic "real world" signal.

ADC or codec SNR is generally defined as the difference (in dB) between the maximum input signal level and the minimum input signal level. This performance is usually reflected in the bit depth of the digital encoding scheme used, typically 16-bit, 20-bit or 24-bit. This means that the SNRs of audio components are actually more closely related to microphone Dynamic Ranges than microphone SNRs.

It is necessary to select audio components and a digital encoding scheme which have equivalent or greater SNR / Dynamic Range than the Dynamic Range of the microphone being used. If not, the noise floor of these audio components will dominate the system and the full microphone performance will not be realized.

The number of bits (N = word length) determines the dynamic range (DR) of PCM-based ADCs and codecs:

$DR = (6.02 \times N + 1.76) dB$

For example, inserting 16 as the N in the equation above for a 16-bit system gives a dynamic range of about 98dB. In practice, dithering reduces the SNR by about 4 dB (dithering is a deliberate addition of noise used to randomize quantization error and thereby linearize the system and eliminate noise modulation). For easy estimation the equation above can be reduced to: DR[dB] = N * 6 (not taking dithering into account).

All digital signals are measured in dBFS (dB relative to full scale). Full scale is the maximum number which can be represented in the digital numbering system. In PDM, this is represented by 100% 1's in the output. In a digital MEMS microphone, the AOP typically coincides approximately with 0dBFS (full scale). All other output levels are specified as –xdBFS, signifying that they are lower than full scale. The Dynamic Range of the codec specifies the lowest dBFS level which it can pass through.

See the illustration on the right for an example of a microphone and some accompanying audio components with different dynamic ranges

As illustrated here, the full-scale levels of the microphone and downstream components will generally align regardless of the signal chain dynamic range. However, the noise floors may not. This is because 0dBFS (full scale) is the same for both systems, but the digital numbering system used by the audio signal chain may not be able to represent levels as low as the microphone noise floor. This means that if a digital microphone is used with a digital encoding scheme which does not use enough bits to represent the noise floor of the microphone, the system noise will not reflect the microphone's true performance.

Note: Select audio components and a digital encoding scheme which have equivalent or greater SNR / Dynamic Range than the Dynamic Range of the microphone being used.

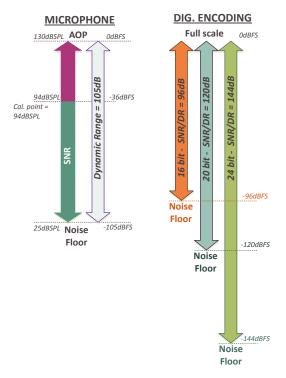


Figure 12 16bit encoding does not have sufficient Dynamic range for this microphone. The system performance will be limited by the audio encoding scheme

If a high SNR microphone is to be used in an audio signal chain with low dynamic range (for example, 16 bits), the system is not able to preserve the SNR performance of the microphone (see illustration above). One option to mitigate this is to use a microphone that has a lower AOP. This can be achieved, for example, by calibrating

fineon



the microphone to an increased sensitivity, for example -26dBFS instead of -36dBFS. This will reduce the AOP from 130 to 120 dBSPL. The dBFS value of the noise floor will increase but since the full-scale value (0 dBFS) was reduced by the same number of decibels (on the SPL scale), the noise floor of the microphone is preserved. This is the difference between Infineon's IM69D130 and IM69D120 microphones (see details in the table below); IM69D130 cannot be used in a 16-bit system without SNR degradation but IM69D120 can. If both high AOP (130dBSPL) and high SNR (69dB) are required, a 20-bit or 24-bit audio signal chain must be used.

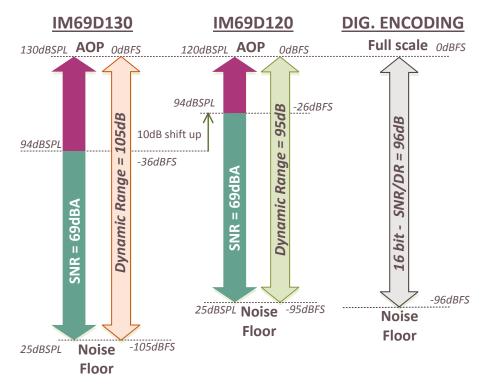


Figure 13 Reduction of the AOP allows high SNR in a 16 bit system

Table 3Important Infineon digital microphone parameters and corresponding system bit
requirement

Microphone Model	Sensitivity	SNR	АОР	DR	Required Bits in System
IM69D130	-36dBFS	69dB	130dBSPL	105dB	20
IM69D120	-26dBFS	69dB	120dBSPL	95dB	16

3.8 Device microphone signal path requirements - bandwidth

The sampling rate (Fs) determines the bandwidth of a PCM system:

$$Bandwidth = \frac{F_s}{2}$$

Common audio bandwidths and the corresponding sampling rate requirements are listed in the table below. To enable an audio system with a 20kHz bandwidth, the sampling rate must be 40kHz or higher. 48kHz and 44.1kHz (used in CDs), are typical rates. In communication systems, full band audio is enabled by, for example, VoIP (Voice over Internet Protocol) and VoLTE (Long-Term Evolution) technologies.



	1 01	
Codec / System	Bandwidth (Hz)	Min. Sample Rate (Hz)
Standard telephone bandwidth (AMR)	300 – 3.4k	8k
"Wideband Audio" / "HD-Voice" / AMR-WB	50 – 7k	16k
"Superwideband Audio"	50–14k	32k
"Fullband Audio" / "Full-HD Voice" / VoIP / VoLTE	20 – 20k *	44.1k / 48k
Ultrasound (excluding frequencies >48kHz)	Up to 48kHz	96k
	1	1

Table 4 Common codecs used and their corresponding parameters

* depends on codec used

Another often available sampling rate is 96kHz. It may be needed in microphone systems used for capturing ultrasound with frequencies up to 48kHz. Using a 96kHz sampling rate is very unlikely to improve audio quality in practice in the audible frequency range.

Even a 32kHz or 16kHz sampling rate can be high enough if the goal is not to cover the whole 20kHz audible sound bandwidth. The lower sampling rates can be considered in order to gain benefits such as lower transmission bit rates, lower system current consumption, simpler system or lower price. Even a 16kHz sampling rate and the corresponding 8kHz audio bandwidth enable "HD Voice" quality and using the AMR-WB (Adaptive Multi-Rate Wideband; ITU-T / 3GPP) codec used in GSM telephony

Note: Design the system to have an audio bandwidth that enables fulfilling the audio quality requirements in all use cases; the sampling rate must be 2x the bandwidth.

3.9 Current consumption

The current consumption of digital microphones is typically higher than the consumption of analog interface microphones with a comparable performance level. The difference is due to the analog to digital conversion done in the microphone instead of doing it later in the signal chain. There are also other factors that affect the current consumption of digital microphone systems. The consumption depends on the supply voltage level, clock frequency and the capacitive load in the system. The higher the clock frequency, the faster the clock and data lines have to be driven back and forth from one state to another. The higher the capacitive load, the more current is consumed to drive those lines.

The current consumption of the microphone system depends also on the power supply arrangement. A microphone with high power supply rejection performance (PSR/PSRR) can be used with a power supply that is readily available in the system that is maybe not absolutely clean of disturbances. A microphone with lower rejection capabilities may have to be used with a very clean power supply that is created with the help of an LDO (low-dropout regulator) from a higher voltage source. The LDO solution is likely to consume significantly more current. This applies also to analog microphones.

3.10 Multi-mode PDM microphones

The current consumption of high-performance digital microphones can be too high for some applications or use cases. There can also be other reasons for wanting to change the characteristics of microphones. Multimode microphones address this need for microphone versatility. The most common available alternative use mode in PDM MEMS microphones is the Low Power Mode, that typically compromises the performance of the microphone to enable reaching a lower current consumption.

In PDM interface microphones, the mode is usually controlled by changing the frequency of the microphone clock. This, of course, means that the device system (/ codec) must have the needed clock frequencies available



4 Electromagnetic compatibility (EMC)

and a way to switch from one frequency to another. For example, Normal Mode can be in use at 2.4 or 3.072 MHz and Low Power Mode at 768kHz.

The system should also take into account that the switching from one mode to another may not be completely glitch-free. To avoid any unwanted pops or clicks in the output of the microphone system, the microphone signal may have to be muted temporarily during mode switching.

Electromagnetic compatibility (EMC)

Electromagnetic compatibility (EMC), describes the ability of a microphone.

- to operate in a device without being disturbed by the electromagnetic environment
- to not disturb other systems in the device

An EMC issue with a microphone can manifest itself in different ways:

- The microphone gets disturbed by the radiated or conducted disturbances in the device
- A poorly designed digital microphone (for example, too fast signal rise/fall speeds, compromised grounding) can emit disturbances that can affect antennas located very close to the microphone
- The microphone effectively a relatively large grounded metal box passively disturbs the functionality of adjacent antennas

- This can be mitigated by moving the microphone further from the antenna or by improving grounding There are many noise sources in connected devices such as smartphones:

- Wireless connectivity antennas (cellular, wi-fi, etc.) output both electrical and magnetic fields
- Other signal lines from which the disturbances couple to the microphone lines
- Indirect coupling: for example, radiated RF disturbances that originate either in the device itself or in external sources get coupled into signal traces and from there to the microphone
- Noisy grounds

4

• Electrically noisy components (such as RF power systems) may add noise into microphone signal traces

Radio frequency interference (RFI) appears when RF disturbances get coupled to the microphone signal lines or directly into the microphone itself. The disturbances can propagate to the microphone output signal and cause an audible disturbance, 'TDMA noise'. GSM cellular devices use time-division multiple access (TDMA) technology at 800 to 900MHz and 1800 to 1900MHz. The transmission pulses at an audible 217Hz frequency and the power levels can be high, causing the 217Hz pulsing to couple into the microphone output signal.

4.1 RF disturbance mitigation

Microphone implementation has to be well executed so that the microphone is well protected from all the radiated and conducted disturbances that are present in wireless connected devices.

Microphone signals should be filtered with, for example, capacitors and inductors

- A capacitor (C) passes high frequencies, depending on its capacitance value, so it can be used for shorting unwanted high frequencies to the ground of the device
- An inductor (L) allows low frequencies to pass and blocks high frequencies so it can be used in series on a signal line to filter out radio frequency disturbances
- Combinations of capacitors and inductors may yield the best filtering results; for example, the so-called pi filter (see illustration on the right)

The optimal filtering circuit design, layout and filtering components depend on

- the design of the microphone and possible filtering systems built into it
- the filtering built into the system that receives the signal (e.g. codec)

Proper circuit design and layout are key enablers for disturbance free microphone signals. The guidelines for sensitive signal wiring are as follows:

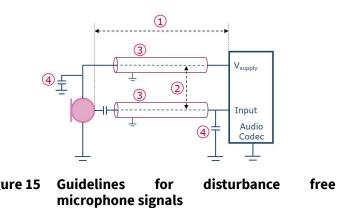


Figure 14 Pi filter



4 Electromagnetic compatibility (EMC)

- Signal trace lengths should be minimized to minimize disturbance pick-up (1)
- Signal lines should be separated to prevents cross talk (2)
- Signals should be shielded properly from electromagnetic radiation and cross talk from other signal lines (3)
 - Often the safest place for the signal lines is inside a circuit board between two ground planes (layers) with protective ground traces running on both sides of the signal trace
- Filtering should be used to remove disturbances from the signals (4)



- Microphones or other audio systems should not be placed close to RF systems
 - It is good practice to separate microphones and antennas onto different planes in the device
- Audio signals or grounding should not be routed parallel to RF traces (RF signals or RF grounding)
 - Signals should be routed perpendicular to each other and the distance between the microphone signals and disturbance sources should be maximized
 - RF traces or other disturbance sources should not be located under the microphones

In addition to the signal cleanliness advice above, the methods listed in the digital microphone implementation section apply also generally (see more details in section 'Signal Connections')

- Use capacitors (CPS, CRF) in V_{supply} to filter low and high frequency interference from the power lines
 - Place the smallest value filtering capacitor closest to the microphone
 - Minimize trace lengths from the filtering capacitors to the power plane
 - Minimize inductance in the capacitor traces
 - Avoid capacitors based on class 2 dielectrics close to microphones (due to risk of audible noise)
- Add a series resistor or ferrite to each power supply line for additional EMI suppression
- Connect microphone grounds to the circuit board ground plane with vias that are directly on the microphone ground pads; avoid traces

A digital (or differential analog) interface is recommended; especially if the lines are long and the environment challenging. See guidelines for digital microphone RF implementation is section '*Electrical Implementation of Digital Microphones*'.

Note: RF disturbances can be mitigated by, for example, using filtering and shielding, minimizing signal trace lengths and preventing disturbance coupling between signal lines and disturbance sources.

The inside of the microphone is protected against radiated disturbances by the metal package, however high quality grounding is also essential for high disturbance immunity.

- A high-quality ground must be provided for the microphone so that disturbances have a low impedance path to bypass the microphone
- To optimize disturbance protection, the ground should be designed to have minimal potential (voltage) variation throughout the ground area ($\Delta V = 0$)
 - A solid board-wide ground plane provides the lowest impedance for RF signals and thereby a steady ground
- Using a flexible circuit board may degrade ground quality; ground stability and disturbance immunity may be compromised
 - Ground traces on flex boards should be made wide to improve ground quality
 - Tying the microphone ground to the ground on the main circuit board (typically the same as e.g. codecs) is recommended



5 Power supply disturbances

5

- Paying attention to ground quality on flex boards is especially important when trace lengths are long and close to disturbance sources

Power supply disturbances

Immunity to disturbances in the power supply line is a key factor in a microphone's electrical robustness and its immunity to electromagnetic and other disturbances in the device. A microphone with good power supply rejection capabilities can save a device designer / manufacturer time and money but it is still also up to the device design to make sure the disturbances in the power line stay at a level at which the microphones can cope with them without degradation in output signal quality. Power Supply Rejection (PSR) and Power Supply Rejection Ratio (PSRR) are the parameters that indicate the rejection capabilities of the microphone.

The power supply line must be kept clean of disturbances

- Filter disturbances (see 'RF Disturbance Mitigation' on the previous page for more details)
- Shield power supply traces
- Avoid the proximity of power supply disturbance sources such as data buses and switching regulators
- Use a regulated low noise power supply if necessary

As mentioned in the '*Current consumption*' section, a microphone with good power supply interference rejection performance can help reduce system current consumption by enabling simpler powering solutions.

6 Electrostatic discharges (ESD)

The way a MEMS microphone is implemented into a device can have a significant effect on the microphone's immunity to electrostatic discharges (ESD). A discharge can harm a MEMS microphone in two different ways: electrically and mechanically (due to high-pressure pulses caused by the sparks).

The electrical damage caused by the high voltage levels associated with ESD can be prevented by preventing the spark from reaching the sensitive semiconductor parts of the microphone

- A low-impedance path to ground that bypasses the microphone must be provided for the discharge
- MEMS microphone packages are typically shielded and grounded but it is preferable not to let the spark get grounded through the package
 - It is important to keep the extremely loud spark as far away as possible from the acoustic sensor
- The key implementation factor is that the quality of the microphone ground must be high, i.e. the impedance to the ground and inside the ground must be low

7 Wind

Wind is a challenging environmental factor for microphones. There are few effective ways to mitigate wind noise. In most types of consumer electronics devices, traditional wind noise mitigation tactics such as foam or fur wind screens are not feasible due to their sizes, appearances and challenging mass manufacturability.

Electrical solutions are relatively ineffective. Wind (noise) is typically arbitrary and uncorrelated from one location to another and therefore difficult to cancel with, for example, multi-microphone software solutions. Wind noise also tends to have a wide frequency band that overlaps with the wanted sounds so electrical signal filtering cannot be used effectively either. Most wind noise energy is at low frequencies so some improvement can be achieved with high pass filtering but this is likely to impact the low frequencies of the wanted audio signal.

Due to the often-turbulent nature of wind, the noise can often sound like bad distortion but this does not necessarily mean that the microphone (system) is actually saturated. However, some types of wind, such as bursts of non-stationary noise can cause the signal level to rise high enough to cause saturation. High acoustic overload point of the microphone and the system may help with this kind of wind noise.

8 Further information

Read more about PDM and PCM here:

http://users.ece.utexas.edu/~bevans/courses/rtdsp/lectures/10_Data_Conversion/ AP_Understanding_PDM_Digital_Audio.pdf

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