Intel® Server System SC5650BCDP

Technical Product Specification

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Revision 1.5

March 2010

Enterprise Platforms and Services Division – Marketing

Revision History

Date	Revision Number	Modifications
August 2009	1.0	Initial Release
March 2010	1.5	Adding support for Intel® Xeon® processors 5600 series

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1. Introduction

This Technical Product Specification (TPS) provides system specific information detailing the features, functionality, and high level architecture of the Intel® Server System SC5650BCDP. You should also reference the *Intel® Server Board S5500BC Technical Product Specification* for more details regarding the functionality and architecture specific to the integrated server board and what is supported in this server system.

The Intel® Server System SC5650BCDP may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Refer to the *Intel® Server Board S5500BC/ Intel® Server System Sr1630BC/Intel® Server System SC5650BCDP Specification Update* for published errata.

1.1 Server Board Use Disclaimer

This document is divided into the following chapters:

Chapter 1 – Introduction
Chapter 2 – Product Overview
Chapter 3 – Power Sub-System
Chapter 4 – Cooling Sub-System
Chapter 5 – Peripheral and Drive Support
Chapter 6 – Front Control Panel
Chapter 7 – PCI Card and Assembly
Chapter 8 – Environmental and Regulatory Specifications
Appendix A – Integration and Usage Tips
Appendix B – POST Code Diagnostic LED Decoder
Appendix C – Post Error Message and Handling
Glossary
Reference Documents

1.2 Server Board Use Disclaimer

Intel® Server Systems support add-in peripherals and contain a number of high-density VLSI and power delivery components that need adequate airflow to cool. Intel ensures through its own chassis development and testing that when Intel server building blocks are used together, the fully integrated system will meet the intended thermal requirements of supported components. It is the responsibility of the system integrator who chooses not to use Intel developed server building blocks to consult vendor datasheets and operating parameters to determine the amount of air flow required for their specific application and environmental conditions. Intel Corporation cannot be held responsible if components fail or the server system does not operate correctly when used outside any of their published operating or non-operating limits.

2. Product Overview

The Intel® Server System SC5650BCDP is a 5U server system which integrates the Intel® Server Board S5500BC into the Intel® Server Chassis SC5650DP. The server system features are designed to support the high-density server market. This chapter provides a high-level overview of the system features. Greater detail for each major system component or feature is provided in the following chapters.

Table 1. System Feature Set

Feature	Description
Dimensions	17.8 inch (45.2 cm) x 9.256 inch (23.5 cm) x 19 inch (48.3 cm)
Server Chassis	Intel® Server Chassis SC5650DP
Server Board	Intel® Server Board S5500BC
Processor	LGA 1366 sockets supporting up to two Intel® Xeon® processor 5500 series and 5600 series with Intel® QuickPath Interconnect (QPI) and Integrated Memory controllers. • Supports up to 95 W Thermal Design Power (TDP) • 4.8 GT/s, 5.86 GT/s, and 6.4 GT/s Intel® QuickPath Interconnect (Intel® QPI) • EVRD11.1 For a complete list of supported processors, see: http://support.intel.com/support/motherboards/server/s5500bc/compat.htm
Memory	Eight DDR3 DIMM slots supporting up to 32 GB of DDR3 800/166/1333 MT/s ECC Registered (RDIMM), or ECC Unbuffered (UDIMM) DDR3 memory • Four memory sockets support CPU_1 and four memory sockets support CPU_2. NOTE: Mixed memory is not tested or supported. Non-ECC memory is not tested and is not recommended for use in a server environment
Chipset	• Intel® I/O Hub (IOH) 5500 chipset • Intel® 82801Jx I/O Controller Hub 10 Raid (ICH10R) • ServerEngines* LLC Pilot II BMC controller (Integrated BMC)
Peripheral Interfaces	**External connections:** • DB-15 video connector (back) • RJ-45 serial Port A connector • Two RJ-45 10/100/1000 Mb network connections • Four USB 2.0 connectors (back) • One USB 2.0 connector (front) **Internal connections:** • Two USB 2x5 pin header, each supports two USB 2.0 ports • One DH-10 Serial Port B header • Six Serial ATA (SATA) II connectors • One SSI-EEB compliant front panel header • One SSI-EEB compliant 24-pin main power connector • One SSI-compliant 8-pin CPU power connector • One SSI-compliant 5-pin auxiliary power connector • One 4-Pin SGPIO connector

Feature	Description
Add-in PCI, PCI Express* Cards	Slot6: One half-length (6.6 inches) PCI Express* Gen2 x8 connector with X8 link width Slot7 : One half-length (6.6 inches) PCI Express* Gen2 x8 connector with x8 link width Slot5 : One half-length (6.6 inches) PCI Express* Gen2 x8 connector with x4 link width Slot3 : One half-length (6.6 inches) PCI Express* x4 connector with x4 link width Slot4 : One half-length (6.6 inches) 5V PCI 32 bit / 33 MHz connector
Video	On-board ServerEngines* LLC Pilot II BMC controller • Integrated 2D video controller • 64 MB DDR2 667 MHz Memory
LAN	Two 10/100/1000 NICs ▪ One 82574LGbE PCI Express* Network Controller connects to the Gen2 x1 interface on the Intel® 5500 IOH chipset. ▪ One 82567 Gigabit Network Connection that connects to the Gigabit LAN Connect Interface / LAN Connect Interface on the Intel® ICH10R ▪ Two 10/100/1000 Base-TX Interfaces through RJ-45 connectors with integrated magnetics. ▪ Link and Speed LEDs on the RJ-45 Connector.
Hard Drive Options	Includes one tool-less fixed drive bay for up to six fixed drives
External front connectors	Two USB ports
Peripherals	Two tool-less, multi-mount 5.25-in peripheral bays. One standard 3.5-in removable media peripheral bay.
Control Panel	LEDs for NIC1, NIC2, HDD activity, power status, and system fault status. Switches for power, NMI, and reset. Integrated temperature sensor for fan speed management.
LEDs and displays	LEDs with standard control panel: ▪ NIC1 Activity ▪ NIC2 Activity ▪ Power / Sleep ▪ System Status ▪ Hard Drive Activity Intel® Light-Guided diagnostic LEDs: ▪ Fan Fault ▪ DIMM Fault ▪ CPU Fault ▪ 5V-STBY ▪ System State ▪ POST Code Diagnostics
Power Supply	600-W PFC Intel validated PSU with integrated cooling fan.
Fans	One tool-less, 120-mm chassis rear fan. One tool-less 120-mm PCI fan. One tool-less 92-mm drive bay fan.

Feature	Description
Server Management	On-board ServerEngines* LLC Pilot II Controller ▪ Integrated Baseboard Management Controller (Integrated BMC), IPMI 2.0 compliant ▪ Integrated Super I/O on LPC interface Support for Intel® Server Management Software
System Management	Intel® System Management Software

2.1 System Views

Figure 1. Intel® Server System SC5650BCDP

2.2 System Dimensions

Table 2. Intel® Server System SC5650BCDP Dimensions

Height	17.8 Inches
Width without rails	9.256 Inches
Depth without CMA	19 inches

2.3 System Components

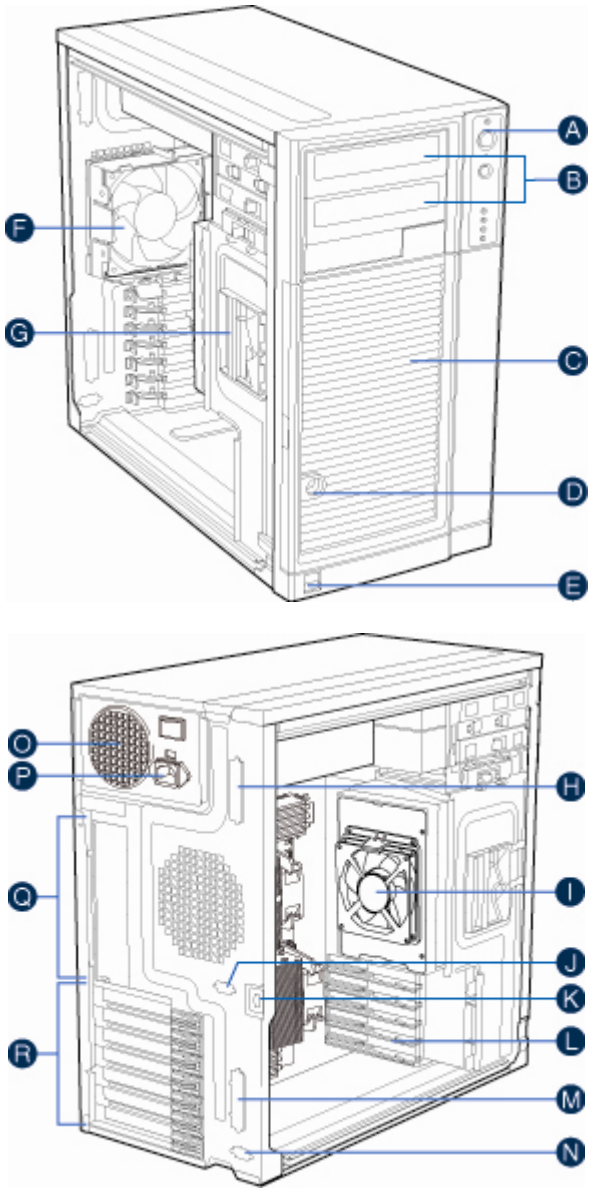


Figure 2. Intel® Server System SC5650BCDP Components

Table 3. Intel® Server System SC5650BCDP Components Reference

	Description		Description
A	Control panel controls and indicators	B	Two half-height 5.25-in peripheral drive bays
C	Internal hard drive bay cage (behind door)	D	Security lock
E	USB ports(two)	F	120-mm system fan

	Description		Description
G	Hard drive cage retention mechanism	H	Alternate external SCSI knockout
I	Fixed Hard drive fan	J	Alternate serial B port knockout
K	Padlock loop	L	PCI card guide (PCI fan behind)
M	External SCSI knockout	N	Serial B port knockout
O	Power supply (fixed power supply shown)	P	AC input power connector
Q	I/O shield	R	PCI Add-in board slots

2.4 I/O Panel

All input/output (I/O) connectors are accessible from the rear of the chassis. The SSI E-bay 3.61-compliant chassis provides an ATX 2.2-compatible cutout for I/O shield installation. Boxed Intel® server boards provide the required I/O shield for installation in the cutout. The I/O cutout dimensions are shown in the following figure for reference.

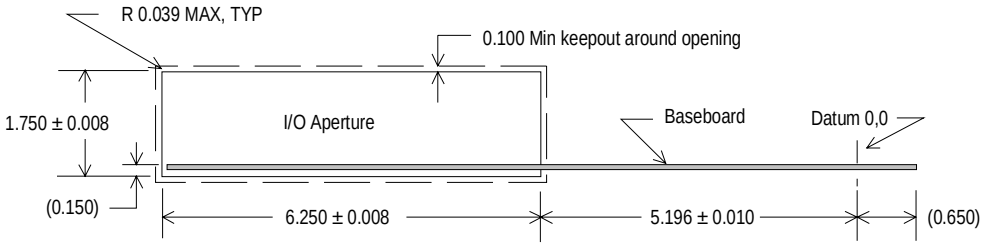


Figure 3. ATX 2.2 I/O Aperture

2.5 Rack and Cabinet Mounting Option

The Intel® Server System SC5650BCDP supports a rack mount configuration. The rack mount kit includes the chassis slide rails, rack handle, rack orientation label, screws, and manual. This rack mount kit is designed to meet the EIA-310-D enclosure specification. General rack compatibility is further described in the *Server Rack Cabinet Compatibility Guide* found at http://support.intel.com.

2.6 Front Bezel Features

The bezel is constructed of molded plastic and attaches to the front of the chassis with three clips on the right side and two snaps on the left. The snaps at the left attach behind the access cover, thereby preventing accidental removal of the bezel. The bezel can only be removed by first removing the server access cover. This provides additional security to the hard drive and peripheral bay area. The bezel also includes a key-locking door that covers the drive cage area permitting access to hot swap drives when a hot swap drive bay is installed.

2.7 Server Board Overview

The system integrates one Intel® Server Board S5500BC.

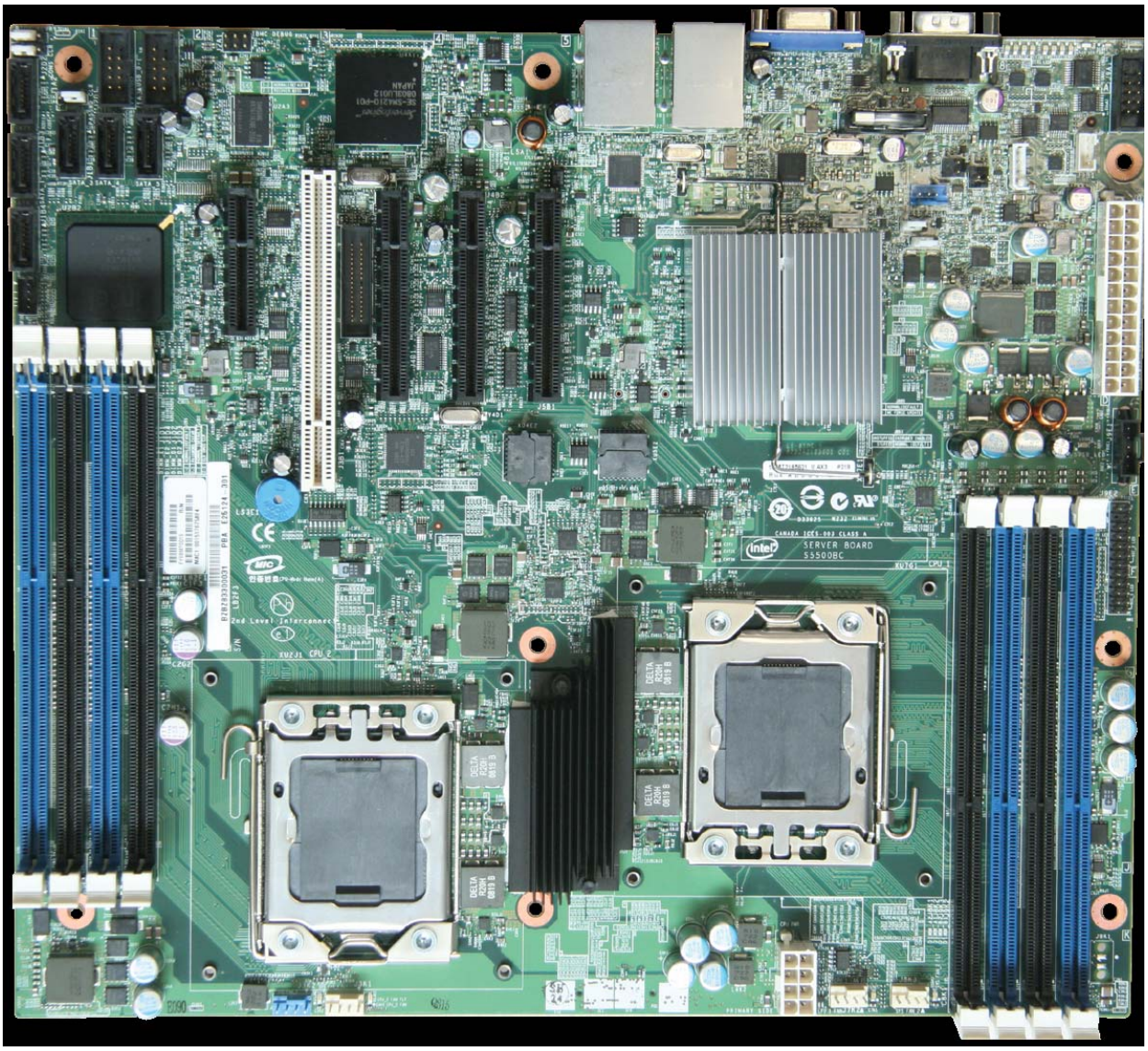


Figure 4. Intel® Server Board S5500BC picture

2.7.1 Server Board Connector and Component Layout

The following figure shows the board layout of the server board. Each connector and major component is identified by a number or letter, and is described in Table 4..

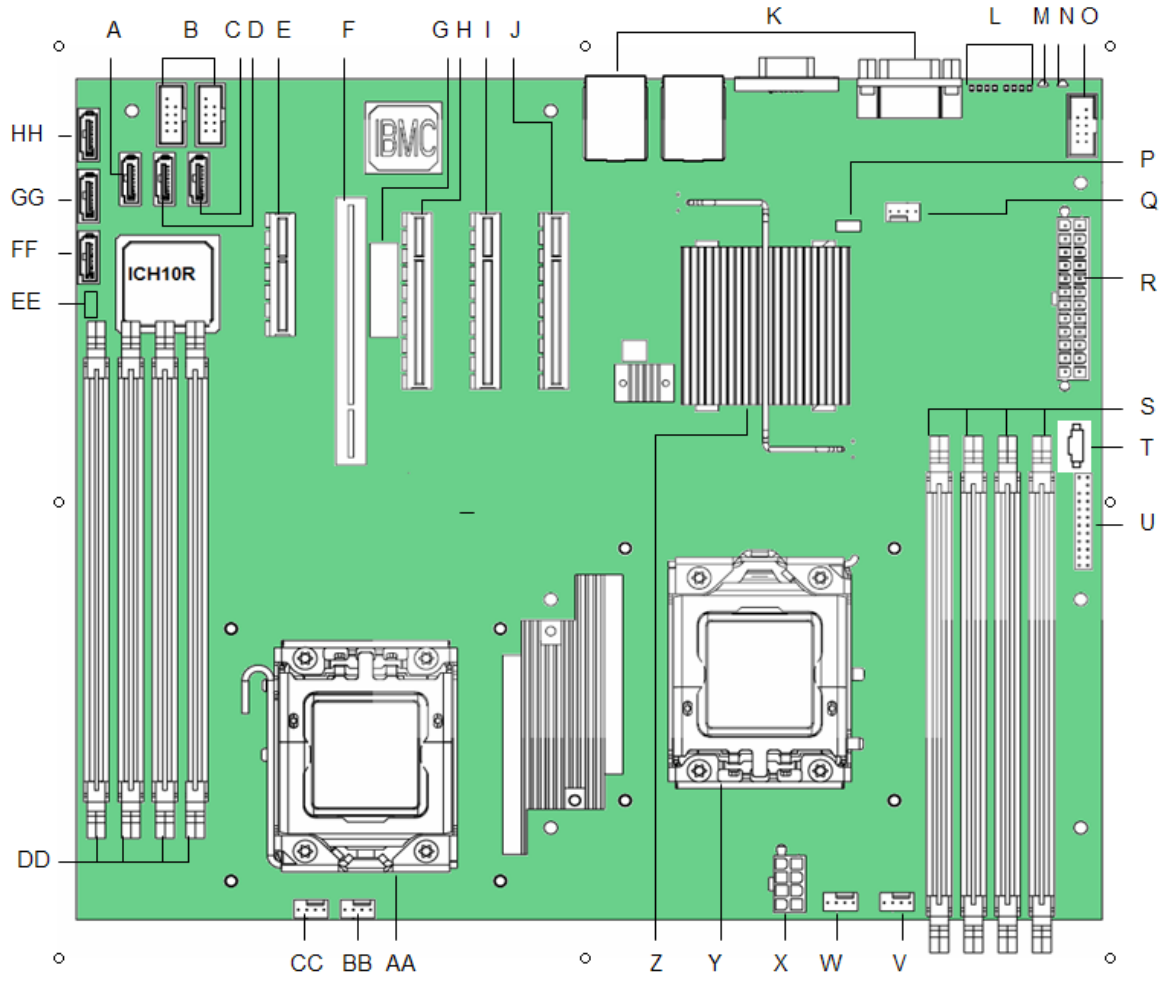


Figure 5. Intel® Server Board S5500BC Layout

Table 4. Board Layout reference

	Description		Description
A	SATA 3	B	Internal dual port USB2.0 header
C	SATA 5	D	SATA 4
E	Slot 3, PCI Express* x4	F	Slot 4, PCI 32-bit/33 MHz
G	Intel® RMM3 slot	H	Slot 5, PCI Express* x8
I	Slot 6, PCI Express* x8 (Riser card)	J	Slot 7, PCI Express* x8
K	Back panel I/O ports	L	Diagnostic LEDs
M	Status LED	N	ID LED
O	External Serial B header	P	SATA Key

	Description		Description
Q	System fan 3 header	R	Main power connector
S	DIMM sockets for Channel A & B (Supports CPU_1)	T	Power Supply Auxiliary Connector
U	SSI 24-pin Front Panel connector	V	System fan 2 header
W	CPU_1 fan header	X	CPU Power Connector
Y	CPU_1 Socket	Z	Intel® IOH 5500 chipset
AA	CPU Socket 2	BB	CPU 2 fan header
CC	System fan 1 header	DD	DIMM sockets for Channels D and E (Supports CPU_2)
EE	SATA SGPIO	FF	SATA 0
GG	SATA 1	HH	SATA 2

2.7.2 Intel® Light-Guided Diagnostic LED Locations

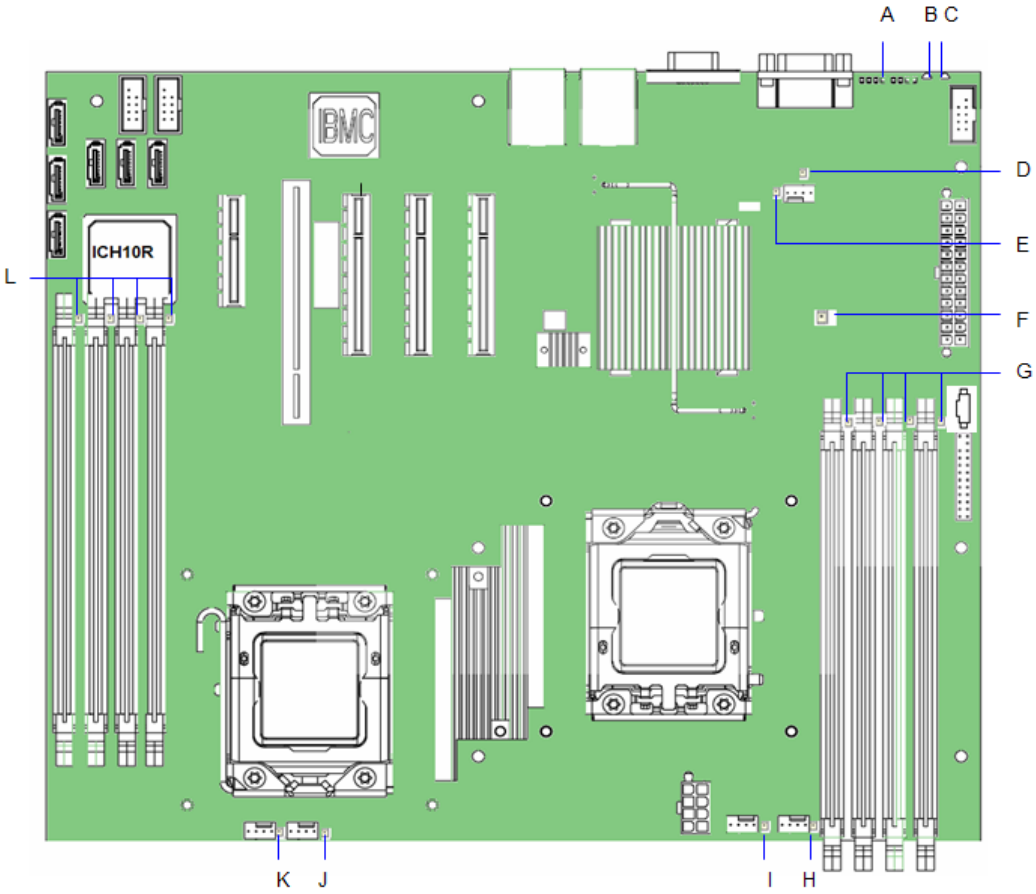


Figure 6. Intel® Light-Guided Diagnostic LED Locations

Table 5. Intel® Light-Guided Diagnostic LED reference

	Description		Description
A	Post-Code Diagnostic LEDs	B	Status LED
C	System ID LED	D	HDD LED
E	System Fan 3 Fault LED	F	5 VSB LED
G	DIMM Fault LED	H	System Fan 2 Fault LED
I	CPU 1 Fan Fault LED	J	CPU 2 Fan Fault LED
K	System Fan 1 Fault LED	L	DIMM Fault LED

3. Power Sub-System

3.1 600-Watt Power Supply

The 600-W power supply specification defines a non-redundant power supply that supports the Intel® server systems SC5650BCDP. The 600-W power supply has eight outputs: 3.3V, 5V, 12V1, 12V2, 12V3, 12V4, -12V and 5VSB. This form factor fits into a pedestal system and provides a wire harness output to the system. An IEC connector is provided on the external face for AC input to the power supply.

The power supply incorporates a Power Factor Correction circuit. The power supply is tested as described in EN 61000-3-2: Electromagnetic Compatibility (EMC) Part 3: Limits-Section 2: Limits for Harmonic Current Emissions, and meets the harmonic current emissions limits specified for ITE equipment.

The power supply is tested as described in JEIDA MITI Guideline for Suppression of High Harmonics in Appliances and General-Use Equipment and meets the harmonic current emissions limits specified for ITE equipment.

3.1.1 Mechanical Overview

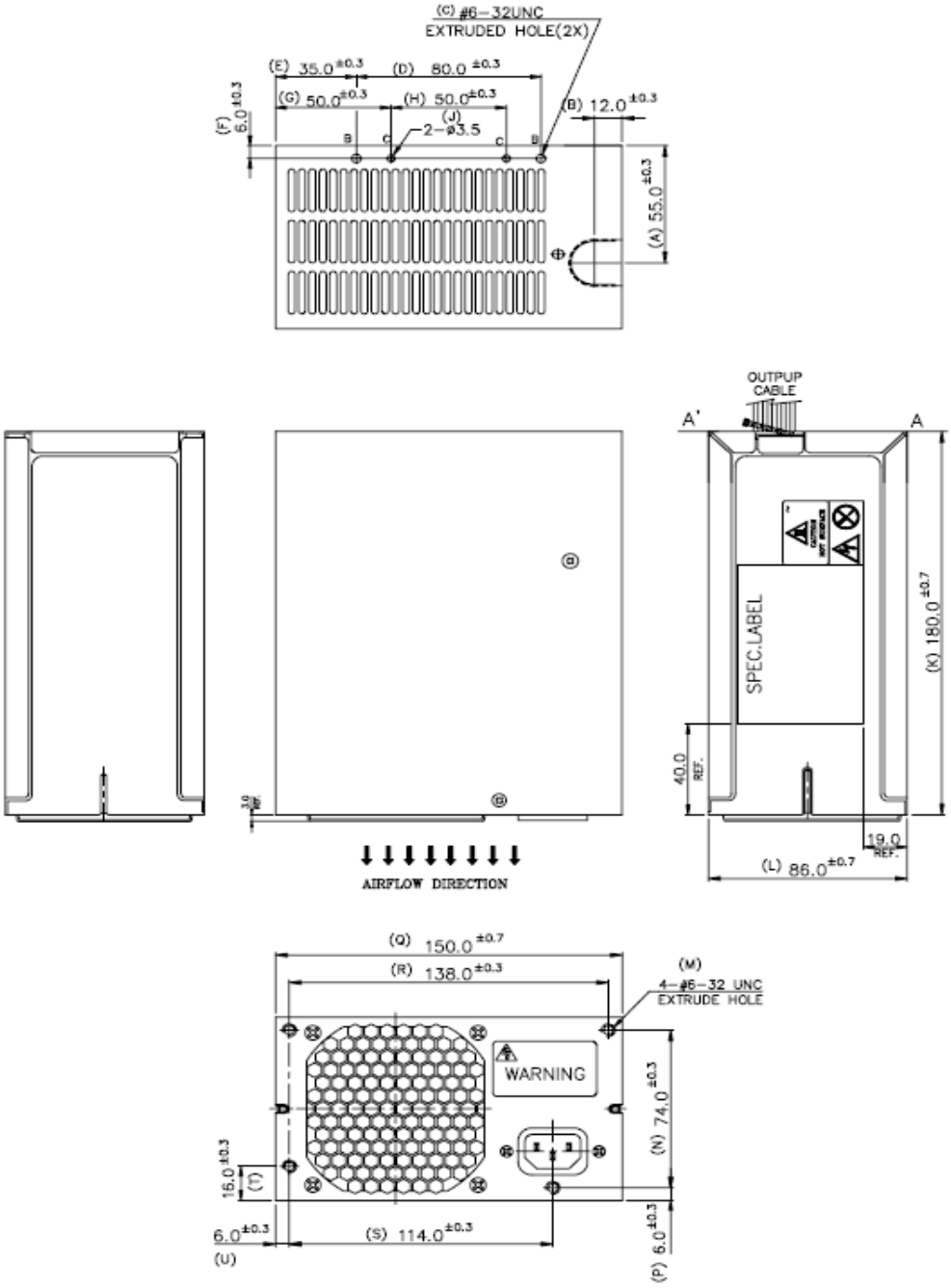


Figure 7. Mechanical Drawing for Power Supply Enclosure

3.1.2 Airflow and Temperature

The power supply incorporates one 80-mm fan for self and system cooling. The fan provides no less than 14 CFM of airflow through the power supply when installed in the system. The cooling air enters the power module from the non-AC side. The power supply operates within all specified limits over the T_{op} temperature range.

Table 6. Thermal Environmental Requirements

ITEM	DESCRIPTION	MIN	Specification	UNITS
T_{op}	Operating temperature range.	0	50	°C
T_{non-op}	Non-operating temperature range.	-40	70	°C
Altitude	Maximum operating altitude		1500	m

The power supply meets UL enclosure requirements for temperature rise limits. All sides of the power supply, with the exception of the air exhaust side, are classified as “Handle, knobs, grips, etc. held for short periods of time only.”

3.1.3 Output Cable Harness

Listed or recognized component appliance wiring material (AVLV2), CN, rated min 105°C, 300Vdc is used for all output wiring.

P1 BASEBOARD POWER CONNECTOR

PIN	SIGNAL	COLOR	PIN	SIGNAL	COLOR
1	+3.3 VDC	ORANGE AWG#18	13	+3.3 VDC	ORANGE
	+3.3V R.S.	ORANGE AWG#24			
2	+3.3 VDC	ORANGE AWG#18	14	−12 VDC	BLUE
3	COM	BLACK AWG#18	15	COM	BLACK
4	+5 VDC	RED AWG#18	16	PS_ON	GREEN
	+5V R.S.	RED AWG#24	17	COM	BLACK
5	COM	BLACK	18	COM	BLACK
	RETURNS	BLACK AWG#24	19	COM	BLACK
6	+5 VDC	RED	20	RESERVED	N.C.
7	COM	BLACK	21	+5 VDC	RED
8	PWR OK	GRAY	22	+5 VDC	RED
9	5VSB	PURPLE	23	+5 VDC	RED
10	+12 V3	YELLOW	24	COM	BLACK
	+12V3 RS	YELLOW AWG#24			
11	+12 V3	YELLOW			
12	+3.3 VDC	ORANGE			

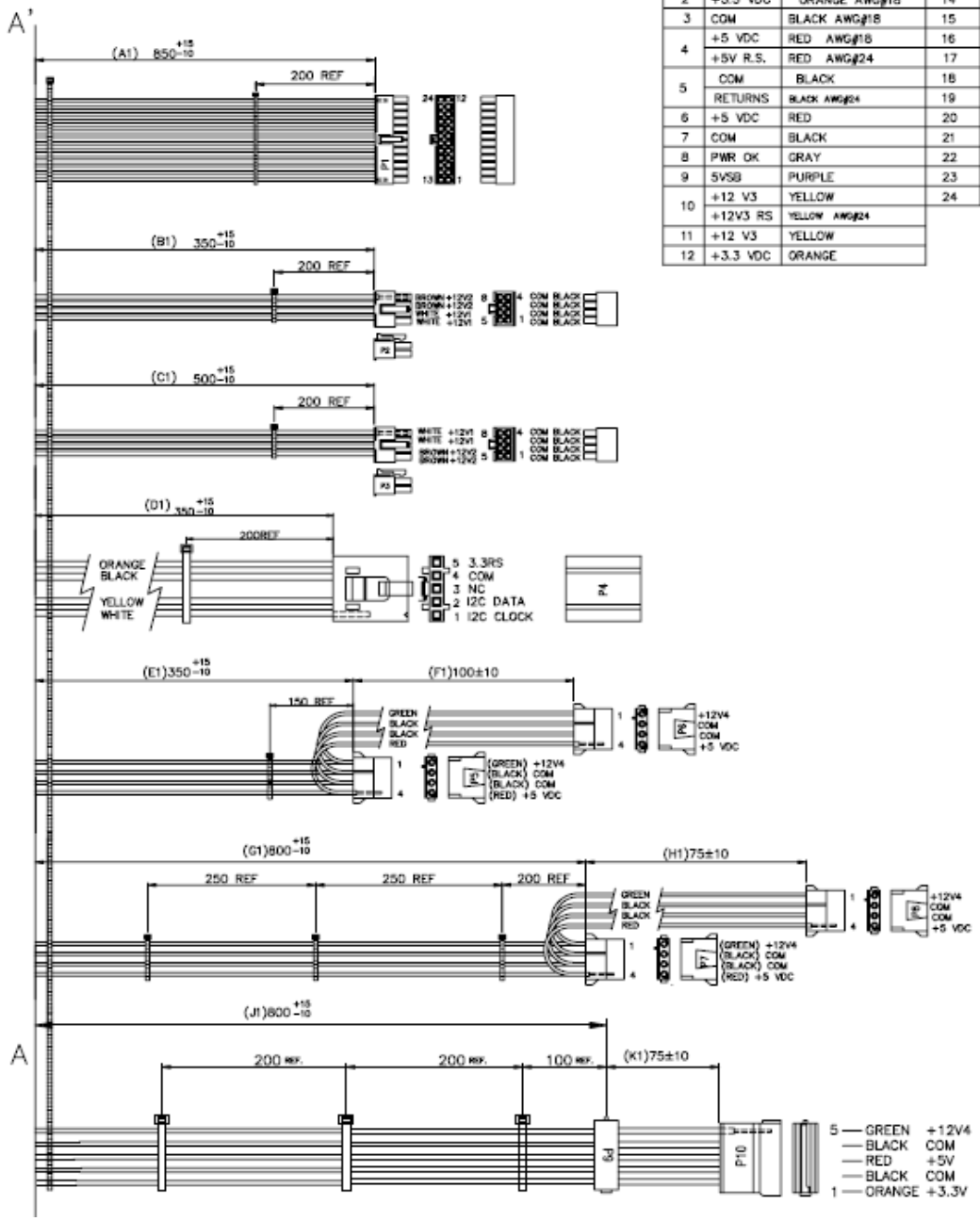


Figure 8. Output Cable Harness for 600-W Power Supply

NOTES:
1. ALL DIMENSIONS ARE IN MM
2. ALL TOLERANCES ARE +10 MM / -0 MM
3. INSTALL 1 TIE WRAP WITHIN 12MM OF THE PSU CAGE
4. MARK REFERENCE DESIGNATOR ON EACH CONNECTOR
5. TIE WRAP EACH HARNESS AT APPROX. MID POINT
6. TIE WRAP P1 WITH 2 TIES AT APPROXIMATELY 15M SPACING.

Table 7. Cable Lengths

From	To Connector #	Length (mm)	Number of Pins	Description
Power Supply cover exit hole	P1	850	24	Baseboard Power Connector
From	**To Connector #**	**Length (mm)**	**Number of Pins**	**Description**
Power Supply cover exit hole	P2	400	8	Processor 0 Power Connector
Power Supply cover exit hole	P3	400	8	Processor 1 Power Connector
Power Supply cover exit hole	P4	350	5	Power PSMI Connector
Power Supply cover exit hole	P5	350	4	Peripheral Power Connector
Extension	P6	100	4	Peripheral Power Connector
Power Supply cover exit hole	P7	800	4	Peripheral Power Connector
Extension	P8	75	4	Peripheral Power Connector
Power Supply cover exit hole	P9	800	5	Right-angle SATA Power Connector
Extension	P10	75	5	SATA Power Connector

3.1.3.1 P1 Baseboard Power Connector

Connector housing: 24- Pin Molex* Mini-Fit Jr. 39-01-2245 or equivalent
Contact: Molex* 39-00-0059, or equivalent; Molex* 44476-1111 for P10 & P11

Table 8. P1 Baseboard Power Connector

Pin	Signal	18 AWG Color	Pin	Signal	18 AWG Color
1	+3.3 VDC	Orange	13	+3.3 VDC	Orange
2	+3.3 VDC	Orange	14	-12 VDC	Blue
3	COM	Black	15	COM	Black
4	+5 VDC	Red	16	PSON#	Green
5	COM	Black	17	COM	Black
6	+5 VDC	Red	18	COM	Black
7	COM	Black	19	COM	Black
8	PWR OK	Gray	20	Reserved	N.C.
9	5VSB	Purple	21	+5 VDC	Red
10	+12V3	Yellow	22	+5 VDC	Red
11	+12V2	Yellow	23	+5 VDC	Red
12	+3.3 VDC	Orange	24	COM	Black

3.1.3.2 P2 Processor 0 Power Connector

Connector housing: 8- Pin Molex* 39-01-2085 or equivalent

Contact: Molex* 39-00-0059 or equivalent

Table 9. P2 Processor 0 Power Connector

Pin	Signal	18 AWG Color	Pin	Signal	18 AWG Color
1	COM	Black	5	+12V1	White
2	COM	Black	6	+12V1	White
3	COM	Black	7	+12V1	Brown
4	COM	Black	8	+12V1	Brown

3.1.3.3 P3 Processor 1 Power Connector

Connector housing: 8- Pin Molex* 39-01-2085 or equivalent
Contact: Molex* 39-00-0059 or equivalent

Table 10. P3 Processor 1 Power Connector

Pin	Signal	18 AWG Color	Pin	Signal	18 AWG Color
1	COM	Black	5	+12V1	Brown
2	COM	Black	6	+12V1	Brown
3	COM	Black	7	+12V1	White
4	COM	Black	8	+12V1	White

3.1.3.4 P4 Power Signal Connectors

Connector housing: 5-pin Molex* 50-57-9405 or equivalent
Contacts: Molex* 16-02-0087 or equivalent

Table 11. P4 Power Signal Connectors

Pin	Signal	24 AWG Color
1	I²C Clock	White
2	I²C Data	Yellow
3	Reserved	N.C.
4	COM	Black
5	3.3RS	Orange

3.1.3.5 P5-P8 Peripheral Power Connector

Connector housing: AMP* 770827-1 or equivalent
Contact: AMP* 61117-4, or equivalent

Table 12. P5-P8 Peripheral Power Connector

Pin	Signal	18 AWG Color

1	+12V4	Blue/White Stripe
2	COM	Black
3	COM	Black
4	+5Vdc	RED

3.1.3.6 P9 Right-angle SATA Power Connector

Connector Housing: JWT* F6002HS0-5P-18 or equivalent
Contact:

Table 13. P9 Right-angle SATA Power Connector

Pin	Signal	18 AWG Color
1	+3.3V	Orange
2	Ground	Black
3	+5V	Red
4	Ground	Black
5	+12V4	Green

3.1.3.7 P10 SATA Power Connector

Connector Housing: 5-pin Molex* 67926-0011 or equivalent
Contact: Molex* 67926-0041 or equivalent

Table 14. P10 SATA Power Connector

Pin	Signal	18 AWG Color
1	+3.3V	Orange
2	COM	Black
3	+5V	Red
4	COM	Black
5	+12V2	Blue/White

3.1.4 AC Input Requirements

The power supply operates within all specified limits over the following input voltage range, shown in the following table. Harmonic distortion of up to 10% of the rated line voltage must not cause the power supply to go out of specified limits. The power supply does power off if the AC input is less than 75VAC +/-5VAC range. The power supply starts up if the AC input is greater than 85VAC +/-4VAC. Application of an input voltage below 85VAC does not cause damage to the power supply, including a fuse blow.

Table 15. AC Input Rating

PARAMETER	MIN	Rated	MAX	Max Input Current	Start up VAC	Power Off VAC
Voltage (110)	90 V_{rms}	100-127 V_{rms}	140 V_{rms}	10 $A_{1,3}$	85Vac +/- 4Vac	75Vac +/- 5Vac
Voltage (220)	180 V_{rms}	200-240 V_{rms}	264 V_{rms}	5 $A_{2,3}$		
Frequency	47 Hz	50/60Hz	63 Hz			

Notes:
Maximum input current at low input voltage range shall be measured at 90VAC, at max load.
Maximum input current at high input voltage range shall be measured at 180VAC, at max load.
This requirement is not to be used for determining agency input current markings.

3.1.4.1 AC Inlet Connector

The AC input connector is an IEC 320 C-14 power inlet. This inlet is rated for 10A / 250VAC.

3.1.4.2 Efficiency

The power supply has a recommended efficiency of 68% at maximum load and over the specified AC voltage.

3.1.4.3 AC Line Dropout / Holdup

An AC line dropout is defined to be when the AC input drops to 0VAC at any phase of the AC line for any length of time. During an AC dropout of one cycle or less the power supply meets dynamic voltage regulation requirements over the rated load. An AC line dropout of one cycle or less (20ms min) does not cause any tripping of control signals or protection circuits. If the AC dropout lasts longer than one cycle, the power will recover and meet all turn-on requirements. The power supply meets the AC dropout requirement over rated AC voltages, frequencies, and output loading conditions. Any dropout of the AC line does not cause damage to the power supply.

3.1.4.3.1 AC Line 5VSB Holdup

The 5VSB output voltage stays in regulation under its full load (static or dynamic) during an AC dropout of 70ms min (=5VSB holdup time) whether the power supply is in the ON or OFF state (PSON asserted or de-asserted).

3.1.4.4 AC Line Fuse

The power supply has a single line fuse on the Line (Hot) wire of the AC input. The line fusing is acceptable for all safety agency requirements. The input fuse is a slow blow type. AC inrush current does not cause the AC line fuse to blow under any conditions. All protection circuits in the power supply do not cause the AC fuse to blow unless a component in the power supply has failed. This includes DC output load short conditions.

3.1.4.5 AC In-rush

AC line in-rush current does not exceed a 50A peak, cold start @ 20 degrees C and no damage @ hot start for up to one-quarter of the AC cycle, after which, the input current is no more than the specified maximum input current at 264Vac input. The peak in-rush current is less than the ratings of its critical components (including input fuse, bulk rectifiers, and surge limiting device).

The power supply meets the in-rush requirements for any rated AC voltage during turn on at any phase of AC voltage, during a single cycle AC dropout condition as well as upon recovery after AC dropout of any duration, and over the specified temperature range (T_{op}).

3.1.4.6 AC Line Surge

The power supply is tested with the system for immunity to AC Ringwave and AC Unidirectional wave, both up to 2kV, per EN 55024:1998, EN 61000-4-5:1995 and ANSI C62.45: 1992.

Pass criteria includes: No unsafe operation allowed under any conditions; all power supply output voltage levels must stay within proper specification levels; no change in operating state or loss of data during and after the test profile; no component damage under any conditions.

3.1.4.7 AC Line Transient Specification

AC line transient conditions are defined as “sag” and “surge” conditions. “Sag” conditions are also commonly referred to as “brownout,” and are defined as AC line voltage drops below nominal voltage conditions. “Surge” is defined as AC line voltage rises above nominal voltage conditions.

The power supply meets requirements under the following AC line sag and surge conditions.

Table 16. AC Line Sag Transient Performance

Duration	Sag	Operating AC Voltage	Line Frequency	Performance Criteria
Continuous	10%	Nominal AC Voltage ranges	50/60Hz	No loss of function or performance
0 to 1 AC cycle	95%	Nominal AC Voltage ranges	50/60Hz	No loss of function or performance
> 1 AC cycle	>30%	Nominal AC Voltage ranges	50/60Hz	Loss of function acceptable, self recoverable

Table 17. AC Line Surge Transient Performance

Duration	Surge	Operating AC Voltage	Line Frequency	Performance Criteria
Continuous	10%	Nominal AC Voltages	50/60Hz	No loss of function or performance
0 to ½ AC cycle	30%	Mid-point of nominal AC Voltages	50/60Hz	No loss of function or performance

3.1.4.8 AC Line Fast Transient (EFT) Specification

The power supply meets the EN 61000-4-5 directive and any additional requirements in IEC1000-4-5:1995 and the Level 3 requirements for surge-withstand capability, with the following conditions and exceptions:

- These input transients do not cause any out-of-regulation conditions, such as overshoot and undershoot, nor do they cause any nuisance trips of any of the power supply protection circuits.
- The surge-withstand test does not produce damage to the power supply.
- The power supply meets surge-withstand test conditions under maximum and minimum DC-output load conditions.

3.1.4.9 AC Line Leakage Current

The maximum leakage current to ground for each power supply is 3.5mA when tested at 240VAC.

3.1.5 DC Output Specifications

3.1.5.1 Grounding

The ground of the pins of the power supply output connector provides the power return path. The output connector ground pins are connected to safety ground (power supply enclosure).

3.1.5.2 Standby Output

The 5VSB output is present when an AC input greater than the power supply turn-on voltage is applied.

3.1.5.3 Fan-less Operation

Fan-less operation is the power supply's ability to work indefinitely in standby mode with power on, power supply off, and the 5VSB at full load (=2A) under environmental conditions (temperature, humidity, altitude). In this mode, the components' maximum temperature should follow the same guidelines.

3.1.5.4 Remote Sense

The power supply has remote sense return (ReturnS) to regulate out ground drops for all output voltages; +3.3V, +5V, +12V1, +12V2, +12V3, +12V4, -12V, and 5VSB. The power supply uses remote sense to regulate out drops in the system for the +3.3V, +5V and +12V1 output. The +5V, +12V1, +12V2, +12V3, +12V4, –12V and 5VSB outputs only use remote sense referenced to the ReturnS signal. The remote sense input impedance to the power supply is greater than 200Ω. This is the value of the resistor connecting the remote sense to the output voltage internal to the power supply. Remote sense is able to regulate out a minimum of 200mV drop.

The remote sense return (ReturnS) is able to regulate out a minimum of 200mV drop in the power ground return. The current in any remote sense line is less than 5mA to prevent voltage sensing errors. The power supply operates within specification over the full range of voltage drops from the power supply's output connector to the remote sense points.

3.1.5.5 Power Module Output Power / Currents

The following table defines power and current ratings for this 600W power supply. The combined output power of all outputs does not exceed the rated output power. Below are load ranges for each of the two power supply power levels. The power supply meets both static and dynamic voltage regulation requirements for the minimum loading conditions.

Table 18. Load Ratings

Load Range 1 (Maximum System Loading)

Voltage	Minimum Continuous Load	Maximum Continuous Load[1, 3]	Peak Load[2, 4, 5]
+3.3V[6]	1.5 A	20 A	
+5V[6]	5.0 A	24 A	
+12V1	1.5 A	15 A	18 A
+12V2	1.5 A	15 A	18 A
+12V3	1.5 A	16 A	18 A
+12V4	1.5 A	16 A	18 A
-12V	0 A	0.5 A	
+5VSB	0.1 A	2.0 A	

Load Range 2 (Light System Loading)

Voltage	Minimum Continuous Load	Maximum Continuous Load	Peak Load[5]
+3.3V[6]	0.5 A	9.0 A	
+5V[6]	2.0 A	7.0 A	
+12V1	0.5 A	5.0 A	7.0 A
+12V2	0.5 A	5.0 A	7.0 A
+12V3	2.0 A	6.0 A	
+12V4	0.5 A	5.0 A	
-12V	0 A	0.5 A	
+5VSB	0.1 A	2.0 A	

Notes:

A. Maximum continuous total DC output power should not exceed 600 W.

B. Peak load on the combined 12-V output shall not exceed 48 A.

C. Maximum continuous load on the combined 12-V output shall not exceed 43 A.

D. Peak total DC output power should not exceed 660 W.

E. Peak power and peak current loading shall be supported for a minimum of 12 seconds.

F. Combined 3.3V/5V power shall not exceed 140 W.

3.1.5.6 Voltage Regulation

The power supply output voltages are within the following voltage limits when operating at steady state and dynamic loading conditions. These limits include the peak-peak ripple/noise. All outputs are measured with reference to the return remote sense signal (ReturnS). The +12V3, +12V4, –12V and 5VSB outputs are measured at the power supply connectors referenced to ReturnS. The +3.3V, +5V, +12V1, and +12V2 are measured at the remote sense signal located at the signal connector.

Table 19. Voltage Regulation Limits

Parameter	Tolerance	MIN	NOM	MAX	Units
+ 3.3V	- 5% / +5%	+3.14	+3.30	+3.46	V_{rms}
+ 5V	- 5% / +5%	+4.75	+5.00	+5.25	V_{rms}
+ 12V1	- 5% / +5%	+11.40	+12.00	+12.60	V_{rms}
+ 12V2	- 5% / +5%	+11.40	+12.00	+12.60	V_{rms}
+12V3	- 5% / +5%	+11.40	+12.00	+12.60	V_{rms}
+12V4	- 5% / +5%	+11.40	+12.00	+12.60	V_{rms}
- 12V	- 5% / +9%	-11.40	-12.00	-13.08	V_{rms}
+ 5VSB	- 5% / +5%	+4.75	+5.00	+5.25	V_{rms}

3.1.5.7 Dynamic Loading

The output voltages are within the limits specified for the step loading and capacitive loading requirements specified in the following table. The load transient repetition rate is tested between 50Hz and 5 kHz at duty cycles ranging from 10%-90%. The load transient repetition rate is only a test specification. The ∆ step load may occur anywhere within the MIN load and MAX load conditions.

Table 20. Transient Load Requirements

Output	∆ Step Load Size 1, 2	Load Slew Rate	Test Capacitive Load
+3.3V	7.0A	0.25 A/μsec	4700 μF
+5V	7.0A	0.25 A/μsec	1000 μF
+12V	25A	0.25 A/μsec	2700 μF
+5VSB	0.5A	0.25 A/μsec	20 μF

3.1.5.8 Capacitive Loading

The power supply is stable and meets all requirements with the following capacitive loading ranges.

Table 21. Capacitive Loading Conditions

Output	MIN	MAX	Units
+3.3V	10	12,000	μF
+5V	10	12,000	μF
+12V(1, 2, 3)	500 each	11,000	μF
+12V4	10	500	μF
-12V	1	350	μF
+5VSB	20	350	μF

3.1.5.9 Closed Loop Stability

The power supply is unconditionally stable under all line/load/transient load conditions, including capacitive load ranges in Section 2.1.5.8. A minimum of a 45-degree phase margin and -10dB-gain margin is required. Closed-loop stability is ensured at the maximum and minimum loads as applicable.

3.1.5.10 Residual Voltage Immunity in Standby Mode

The power supply is immune to any residual voltage placed on its outputs (typically a leakage voltage through the system from standby output) up to 500mV. There is neither additional heat generated, nor stressing of any internal components with this voltage applied to any individual output or all outputs simultaneously. Residual voltage also does not trip the protection circuits during turn on/off.

The residual voltage at the power supply outputs for a no-load condition does not exceed 100mV when AC voltage is applied.

3.1.5.11 Common Mode Noise

The Common Mode noise on any output does not exceed 350mV pk-pk over the frequency band of 10Hz to 30MHz.The measurement is made across a 100Ω resistor between each of the DC outputs, including ground at the DC power connector and chassis ground (power subsystem enclosure). The test set-up uses a FET probe, such as a Tektronix* P6046, or equivalent.

3.1.5.12 Ripple / Noise

The maximum allowed ripple/noise output of the power supply is defined in the following table. This is measured over a bandwidth of 10 Hz to 20 MHz at the power supply output connectors. A 10μF tantalum capacitor in parallel with a 0.1μF ceramic capacitor is placed at the point of measurement.

Table 22. Ripple and Noise

+3.3V	+5V	+12V(1,2,3,4)	-12V	+5VSB
50mVp-p	50mVp-p	120mVp-p	120mVp-p	50mVp-p

3.1.5.13 Timing Requirements

The timing requirements for power supply operation are as follows. The output voltages must rise from 10% to within regulation limits (T_{vout_rise}) within 5 to 70ms, except for 5VSB which is allowed to rise from 1.0 to 25ms. The +3.3V, +5V and +12V output voltages start to rise at approximately the same time**.** All outputs must rise monotonically. The 5V output needs to be greater than the +3.3V output during any point of the voltage rise. The +5V output must never be greater than the +3.3V output by more than 2.25V. Each output voltage reaches regulation within 50ms (T_{vout_on}) of each other during turn on of the power supply. Each output voltage falls out of regulation within 400msec (T_{vout_off}) of each other during turn off. The following table shows the timing requirements for the power supply being turned on and off via the AC input, with PSON held low and the PSON signal, with the AC input applied.

Table 23. Output Voltage Timing

Item	Description	Minimum	Maximum	Units
T_{vout_rise}	Output voltage rise time from each main output.	5.0*	70*	msec
T_{vout_on}	All main outputs must be within regulation of each other within this time.		50	msec
T_{vout_off}	All main outputs must leave regulation within this time.		400	msec

* The 5VSB output voltage rise time shall be from 1.0 ms to 25 ms

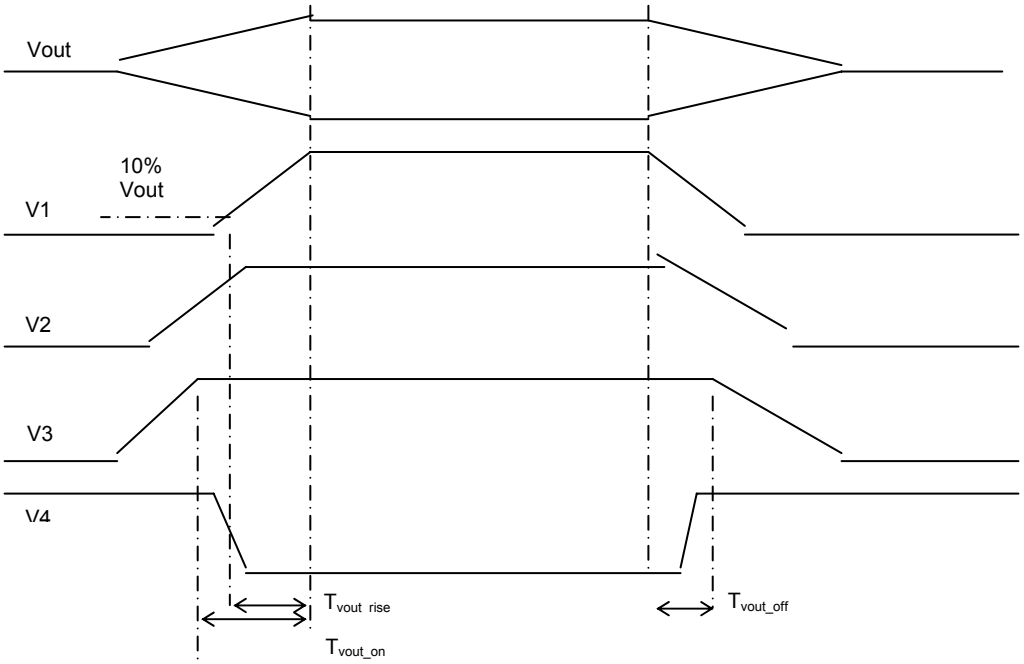


Figure 9. Output Voltage Timing

Table 24. Turn On / Off Timing

Item	Description	Minimum	Maximum	Units
$T_{sb\_on\_delay}$	Delay from AC being applied to 5VSB being within regulation.		1500	msec
$T_{ac\_on\_delay}$	Delay from AC being applied to all output voltages being within regulation.		2500	msec
T_{vout_holdup}	Time all output voltages stay within regulation after loss of AC.	21		msec
T_{pwok_holdup}	Delay from loss of AC to de-assertion of PWOK.	20		msec
$T_{pson\_on\_delay}$	Delay from PSON# active to output voltages within regulation limits.	5	400	msec
T_{pson_pwok}	Delay from PSON# deactive to PWOK being de-asserted.		50	msec
T_{pwok_on}	Delay from output voltages within regulation limits to PWOK asserted at turn on.	100	1000	msec
T_{pwok_off}	Delay from PWOK de-asserted to output voltages (3.3V, 5V, 12V, -12V) dropping out of regulation limits.	1	200	msec
T_{pwok_low}	Duration of PWOK being in the de-asserted state during an off/on cycle using AC or the PSON signal.	100		msec
T_{sb_vout}	Delay from 5VSB being in regulation to O/Ps being in regulation at AC turn on.	50	1000	msec
T_{5VSB_holdup}	Time the 5VSB output voltage stays within regulation after loss of AC.	70		msec

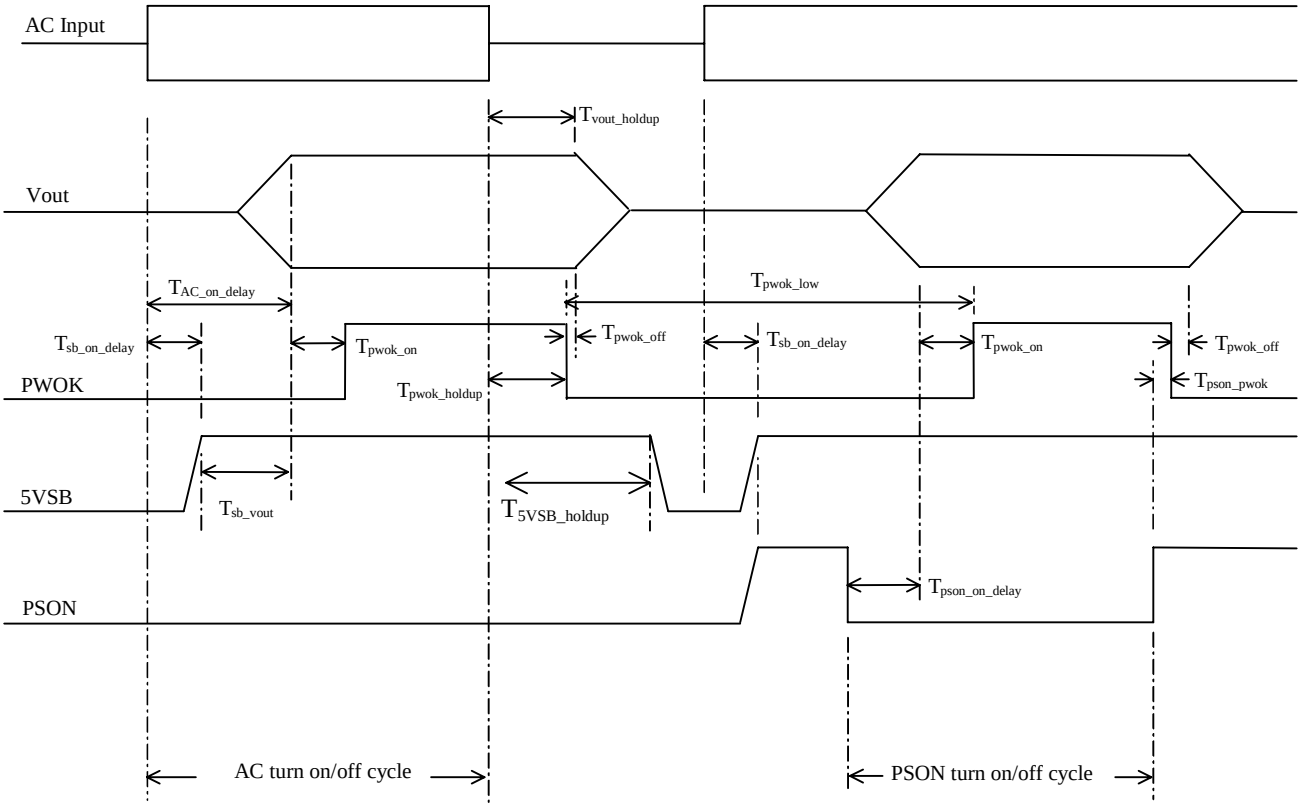


Figure 10. Turn On/Off Timing (Power Supply Signals)

3.1.6 Protection Circuits

Protection circuits inside the power supply cause only the power supply's main outputs to shut down. If the power supply latches off due to a protection circuit tripping, an AC cycle OFF for 15 sec and a PSON# cycle HIGH for 1sec will reset the power supply.

3.1.7 Current Limit (OCP)

The power supply has a current limit to prevent the +3.3V, +5V, and +12V outputs from exceeding the values shown in the following table. If the current limits are exceeded, the power supply will shut down and latch off. The latch will be cleared by either toggling the PSON# signal or by an AC power interruption. The power supply is not damaged from repeated power cycling in this condition. -12V and 5VSB are protected under over current or shorted conditions so that no damage occurs to the power supply. 5VSB will auto-recover after the OCP limit is removed.

Table 25. Over Current Protection (OCP)

VOLTAGE	OVER CURRENT LIMIT	
	Min	Max
+3.3V	26.4A	36A
+5V	26.4A	36A
+12V1	18A	20A
+12V2	18A	20A
+12V3	18A	20A
+12V4	18A	20A
-12V	0.625A	4A
5VSB	N/A	8A

3.1.7.1 Over Voltage Protection (OVP)

The power supply over voltage protection is locally sensed. The power supply will shut down and latch off after an over voltage condition occurs. This latch can be cleared by toggling the PSON# signal or by an AC power interruption. The following table contains the over voltage limits. The values are measured at the output of the power supply's pins. The voltage never exceeds the maximum levels when measured at the power pins of the power supply connector during any single point of fail. The voltage will not trip any lower than the minimum levels when measured at the power pins of the power supply connector. +5VSB will auto-recover after the OVP condition is removed.

Table 26. Over Voltage Protection Limits

Output Voltage	MIN (V)	MAX (V)
+3.3V	3.9	4.5
+5V	5.7	6.5
+12V1,2,3,4	13.3	14.5
-12V	-13.3	-16
+5VSB	5.7	6.5

3.1.7.2 Over Temperature Protection (OTP)

The power supply is protected against over temperature conditions caused by loss of fan cooling or excessive ambient temperature. In an OTP condition, the power supply will shut down. When the power supply temperature drops to within specified limits, the power supply will restore power automatically, while the 5VSB will always remain on. The OTP circuit has a built-in hysteresis such that the power supply will not oscillate on and off due to a temperature recovering condition. The OTP trip level has a minimum of 4°C of ambient temperature hysteresis.

3.1.7.3 PSON# Input Signal

The PSON# signal is required to remotely turn on/off the power supply. PSON# is an active low signal that turns on the +3.3V, +5V, +12V, and -12V power rails. When this signal is not pulled low by the system, or left open, the outputs (except the +5VSB) turn off. This signal is pulled to a standby voltage by a pull-up resistor internal to the power supply. Refer to the following table and figure for PSON# signal characteristics.

Table 27. PSON# Signal Characteristics

Signal Type	Accepts an open collector/drain input from the system. Pull-up to 5V located in power supply.	
PSON# = Low	ON	
PSON# = High or Open	OFF	
	MIN	**MAX**
Logic level low (power supply ON)	0V	1.0V
Logic level high (power supply OFF)	2.1V	5.25V
Source current, Vpson = low		4mA
Power up delay: $T_{pson\_on\_delay}$	5msec	400msec
PWOK delay: T_{pson_pwok}		50msec

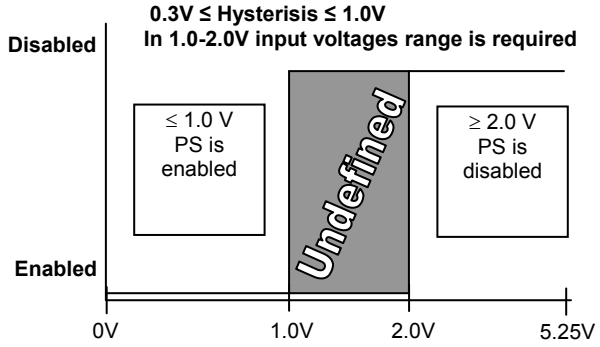


Figure 11. PSON# Required Signal Characteristics

3.1.7.4 PWOK (Power OK) Output Signal

PWOK is a power OK signal and is pulled HIGH by the power supply to indicate that all the outputs are within the regulation limits of the power supply. When any output voltage falls below regulation limits or when AC power has been removed for a time sufficiently long so that the power supply operation is no longer guaranteed, PWOK will be de-asserted to a LOW state. The start of the PWOK delay time is inhibited as long as any power supply output is within current limit.

Table 28. PWOK Signal Characteristics

Signal Type	Open collector/drain output from power supply. Pull-up to VSB located in system.	
PWOK = High	Power OK	
PWOK = Low	Power Not OK	
	MIN	**MAX**
Logic level low voltage, Isink=4mA	0V	0.4V
Logic level high voltage, Isource=200μA	2.4V	5.25V
Sink current, PWOK = low		4mA
Source current, PWOK = high		2mA
PWOK delay: T_{pwok_on}	100ms	1000ms
PWOK rise and fall time		100μsec
Power down delay: T_{pwok_off}	1ms	200msec

3.1.8 FRU Data

The FRU data format is compliant with the IPMI, version 1.0 specification. To find the most current version of these specifications you can go to http:\\developer.intel.com/design/servers/ipmi/spec.htm.

3.1.8.1 Device Address Locations

The power supply device address location is as follows:

Power Supply FRU Device	A0h

4. Cooling Sub-System

4.1 Fan Configuration

The cooling sub-system of the Intel® Server System SC5650BCDP consists of one 120mm chassis fan, one 120mm PCI fan and one 92mm drive bay fan. The 4-wire chassis fan provides cooling at the rear of the chassis by drawing fresh air into the chassis from the front and exhausting warm air out the system. This fan is PWM controlled. The server board S5500BC monitors several temperature sensors and adjusts the duty cycle of the PWM signal to drive the fan at the appropriate speed. The 4-wire PCI fan behind the PCI card guide provides cooling by drawing fresh air from the front of the chassis through PCI fan guide and exhausting it into the PCI bay area. The 4-wire 92-mm drive bay fan provides additional cooling to the drive bay by drawing fresh air from the front of the chassis through drive bay area and exhausting warm air out the bay area.

Removal and insertion of the two 120-mm fans or 92-mm fan can be done without tools. The power supply internal fan assists in drawing air through the peripheral bay area, through the power supply and exhausting it out the rear of the system. The Intel® Server System SC5650BCDP is optimized for the Intel® server board S5500BC that using an active CPU heatsink solution.

If an optional hot-swap drive bay is installed, a 4-wire 92-mm fan is included with the mounting bracket kit for installation onto the drive bay. This fan has a PWM circuit that allows the server board to control the fan speed based on sensor readings of ambient temperature.

The front panel of the Intel® Server System SC5650BCDP provides a TMP75 temperature sensor for BMC control. The Intel® Server Board S5500BC BMC controller may use the TMP75 sensor to adjust fan speeds according to air intake temperatures. Refer to the *Intel® Server Board S5500BC Technical Product Specification* for configuring information.

4.2 Server Board Fan Control

The fans provided in the Intel® Server System SC5650BCDP contain a tachometer signal that can be monitored by the server management subsystem for the Intel® Server Boards S5500BC. See Intel® Server Boards S5500BC Technical Product Specification for details on how this feature works.

4.3 Cooling Solution

Air should flow through the system from front to back, as indicated by the arrows in the following figure.

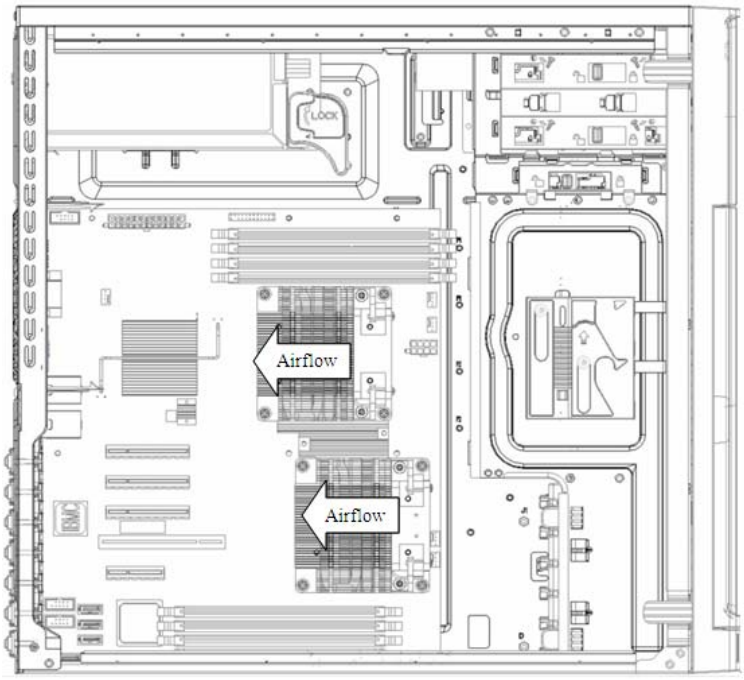


Figure 12. Cooling Fan Configuration for Intel® Server Board S5500BC

The Intel® Server System SC5650BCDP is engineered to provide sufficient cooling for all internal components of the server. The cooling subsystem is dependent upon proper airflow. The designated cooling vents on both the front and back of the chassis must be left open and must not be blocked by improperly installed devices. All internal cables must be routed in a manner that does not impede airflow, and ducting provided for CPU cooling must be installed.

Active heatsinks for CPUs incorporate a fan to provide cooling. The Intel® Server System SC5650BCDP is engineered to work with processors that have an active heatsink solution. Heatsink thermal solutions are sold separately, be sure that you use one that is rated for the wattage of your processor. Proper installation of the processor cooling solution is required for circulating air toward the rear of the chassis (toward I/O connectors).

4.3.1 System Fan Connectors

The Intel® Server System SC5650BCDP supports three system fans. The Intel® Server Board S5500BC supports five SSI compliant 4-pin fan connectors. The two 4-pin fan connectors are for processor cooling fans: CPU_1 fan (J3K1) and CPU_2 fan (J7K2). The three 4-pin fan connectors are for system fans system fan 1(J3K2), system fan 2(J8K3), and system fan 3 (J8B4).

Fan	Connect to fan connector
Rear Chassis Fan	System Fan 3
HDD Bay Fan	System Fan 2
PCI Zone fan	System Fan 1

The pin configuration for each fan connector is identical. The following table provides pin-out information.

Table 29. CPU and System Fan Connector Pin-out

(Location: J3K1, J7K2, J3K2, J8K3, J8B4)

Pin	Signal Name	Type	Description
1	Ground	GND	GROUND is the power supply ground.
2	12V	Power	Power supply 12 V.
3	Fan Tach	Out	FAN_TACH signal is connected to the BMC to monitor the fan speed.
4	Fan PWM	In	FAN_PWM signal to control the fan speed.

5. Peripheral and Hard Drive Support

The following sections describe the components shown in the figure below:

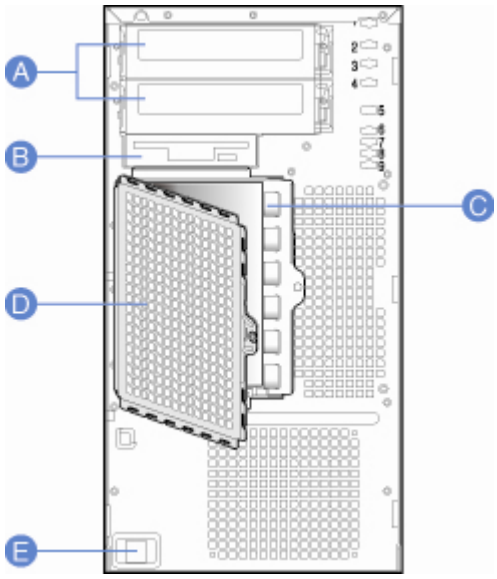


Figure 13: Front View Components (without Front Bezel Assembly)

Table 30: Front View Components Reference

	Description
A	5.25-in Device Drive Bays
B	3.5-in Device Drive Bay
C	Hard Drive Cage
D	Drive Bay EMI Shield (shown open)
E	Front Panel USB Ports

5.1 3.5-in Peripheral Drive Bay

Intel® Server System SC5650BCDP supports one 3.5-in removable media peripheral, such as a tape drive, below the 5.25-in peripheral bays. The bezel must be removed prior to installing a 3.5-in removable media devise. When a drive is not installed, a snap-in EMI shield must be in place to ensure regulatory compliance. Cosmetic plastic filler is provided to snap into the bezel.

The 3.5-in bay is designed for tool-less insertion and removal so that no screws are required. On the right side of the chassis, two protrusions in the sheet metal help locate the drive. On the left side are two levers to lock the drive into place.

5.2 5.25-in Peripheral Drive Bays

Intel® Server System SC5650BCDP supports two half-height 5.25-in removable media peripheral devices, such as a magnetic/optical disk, DVD/CD-ROM drive, or tape drive. These

peripherals can be up to 9 inches (228.6 mm) deep. As a guideline, the maximum recommended power per device is 17W. Thermal performance of specific devices must be verified to ensure compliance to the manufacturer's specifications.

The 5.25-in peripherals can be inserted and removed without tools from the front of the chassis after taking off the access cover and removing the front bezel. The peripheral bay utilizes visual guide holes to correctly line up the position of peripheral drives. Locking slide levers push retaining pins into the drive to hold the drive securely in the bay. EMI shield panels are installed and should be retained in unused 5.25-in bays to ensure proper cooling and EMI conformance.

The peripheral bays are covered with plastic snap-in cosmetic pieces that must be removed to add peripherals to the system. Control panel buttons and lights are located along the right side of the peripheral bays.

Note: Use caution when approaching the maximum level of integration for the 5.25-in drive bays. Power consumption of the devices integrated needs must be carefully considered to ensure that the maximum power levels of the power supply are not exceeded.

5.3 Hot Swap Hard Disk Drive Bays

The system can support either an active SAS/SATA or a passive SAS/SATA backplane. The backplanes provide platform support for hot-swap SAS or SATA hard drives. For more information about SAS/SATA Hot Swap Backplane (HSBP), please refer to the *Intel® Server Chassis SC5650 Technical Product Specification.*

The passive backplane acts as a "pass-through" for the SAS/SATA data from the drives to the SAS/SATA controller on the baseboard or a SAS/SATA controller add-in card. It provides the physical requirements for the hot-swap capabilities. The active backplane has a built-in SAS controller that requires a SAS controller on the baseboard or a SAS add-in card for communication. The active SAS/SATA backplane reduces the number of required cables by using only two SAS/SATA connectors to drive up to six hard drives.

When the hot swap drive bay is installed, a bi-color hard drive LED is located on each drive carrier to indicate specific drive failure or activity. For pedestal systems, these LEDs are visible upon opening the front bezel door.

5.3.1 Fixed Hard Drive Bay

Intel® Server System SC5650BCDP comes with a removable hard drive bay that can accept up to six cabled 3.5-in x 1-in hard drives. Power requirements for each individual hard drive may limit the maximum number of drives that can be integrated into an Intel® Server System SC5650BCDP. The drive bay is designed to allow adequate airflow between drives, and no additional cooling fan is required. Drives must be installed in the order of slot 1, 3, 5 first (skipping slots) to ensure proper cooling. The drive bay is secured with a tool-less retention mechanism.

Note: The hard drive bay must be pushed forward or removed to install the server board.

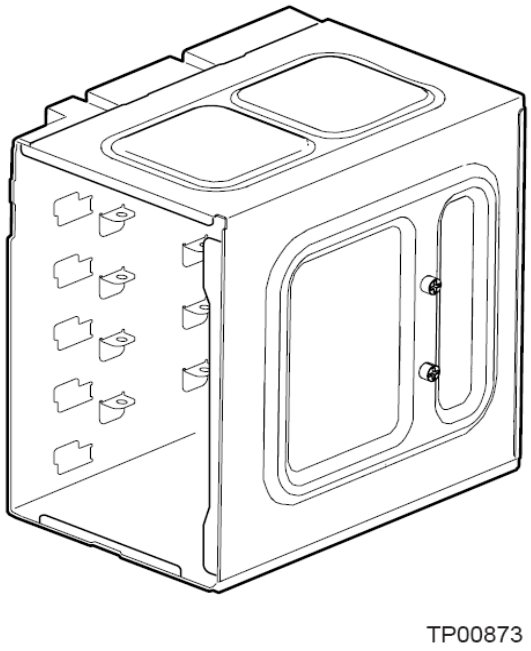


Figure 14: Fixed Hard Drive Bay

Intel® Server System SC5650BCDP is capable of accepting a single SAS/SATA hot swap backplane hard drive enclosure in place of the fixed drive bay. Both backplanes (expanded and non-expanded) have a connector to accommodate a SAF-TE controller on an add-in card. Each backplane type supports up to six 1-in hot swap drives when mounted in the docking drive carrier.

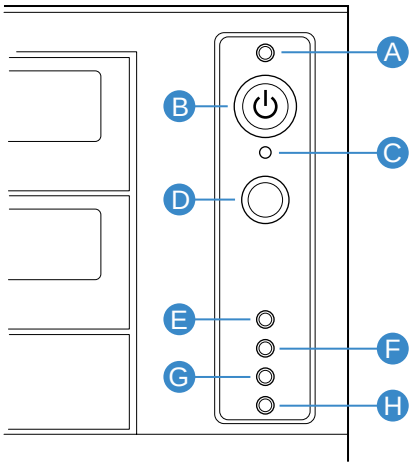
6. Standard Control Panel

The Intel® Server System SC5650BCDP control panel configuration has three buttons and five LEDs.

When the hot-swap drive bay is installed, a bi-color hard drive LED is located on each drive carrier (six totals) to indicate specific drive failure or activity. These LEDs are visible upon opening the front bezel door.

6.1 Control Panel

The control panel buttons and LED indicators are displayed in the following figure. The Entry Ebay SSI (rev 3.61) compliant front panel header for Intel® server boards is located on the back of the front panel. This allows for connection of a 24-pin ribbon cable for use with SSI rev 3.61-compliant server boards. The connector cable is compatible with the 24-pin SSI standard.



A. Power / Sleep LED
B. Power button
C. NMI button
D. Reset Button
E. LAN # 1 Activity LED
F. LAN # 2 Activity LED
G. Hard Drive Activity LED
H. Status LED

Figure 15. Panel Controls and Indicators

Table 31. Control Panel LED Functions

LED Name	Color	Condition	Description
Power/Sleep LED	Green	ON	Power on
		OFF	Power off
LAN # 1- Link/Activity	Green	ON	Linked
		BLINK	LAN activity
		OFF	Disconnected
LAN # 2- Link/Activity	Green	ON	Linked
		BLINK	LAN activity
		OFF	Disconnected
Hard drive activity	Green	BLINK	Hard drive activity
		OFF	No activity
Status LED	Green	ON	System ready (not supported by all server boards)
		BLINK	Processor or memory disabled
	Amber	ON	Critical temperature or voltage fault; CPU/Terminator missing
		BLINK	Power fault; Fan fault; Non-critical temperature or voltage fault
		OFF	Fatal error during POST

7. PCI Cards and Assembly

The Intel® Server Board S5500BC integrated into this system provides five PCI slots:

- Slot3: One half-length (6.6 inches) PCI Express* x4 connector with x4 link width
- Slot4: One half-length (6.6 inches) 5-V PCI 32 bit / 33 MHz connector
- Slot5: One half-length (6.6 inches) PCI Express* Gen2 x8 connector with x4 link width
- Slot6: One half-length (6.6 inches) PCI Express* Gen2 x8 connector with X8 link width
- Slot7: One half-length (6.6 inches) PCI Express* Gen2 x8 connector with x8 link width

The Intel® Server Board S5500BC provides a connector (J3C1) to support a RMM3 card. The RMM3 card provides the Integrated BMC with an additional dedicated network interface. The dedicated interface uses a separate LAN channel. The RMM3 provides additional flash storage for advanced features such as the WS-MAN.

8. Environmental and Regulatory Specifications

8.1 System Level Environmental Limits

The following table defines the system level operating and non-operating environmental limits.

Table 32. System Environmental Limits Summary

Parameter	Limits
Operating Temperature	+10° C to +35° C with the maximum rate of change not to exceed 10° C per hour
Non-Operating Temperature	-40° C to +70° C
Non-Operating Humidity	90%, non-condensing at 35° C
Acoustic noise	Sound power: 7.0 BA in an idle state at typical office ambient temperature. (23 +/- 2 degrees C)
Shock, operating	Half sine, 2 g peak, 11 mSec
Shock, unpackaged	Trapezoidal, 25 g, velocity change 136 inches/sec (≧40 lbs to > 80 lbs)
Shock, packaged	Non-palletized free fall in height of 24 inches (≧40 lbs to > 80 lbs)
Vibration, unpackaged	5 Hz to 500 Hz, 2.20 g RMS random
Shock, operating	Half sine, 2 g peak, 11 mSec
ESD*	+/-15 KV except I/O port +/-8 KV per the Intel Environmental test specification
System Cooling Requirement in BTU/Hr	2550 BTU/hour

* **IMPORTANT NOTES:** ***The host system*** *with the Intel® Server Board S5500BC requires the use of shielded LAN cable to comply with Immunity regulatory requirements. Use of non-shielded cables* ***may result in*** *the product having insufficient immunity electromagnetic effects, which may cause improper operation of the product.*

8.2 Serviceability and Availability

The system is designed to be serviced by qualified technical personnel only.

The recommended Mean Time To Repair (MTTR) of the system is 30 minutes including diagnosis of the system problem. To meet this goal, the system enclosure and hardware were designed to minimize the MTTR.

Following are the maximum times that a trained field service technician should take to perform the listed system maintenance procedures, after diagnosing the system and identifying the failed component.

Table 33. System Maintenance Procedure Times

Activity	Time Estimate
Remove cover	1 min
Remove and replace hard disk drive	5 min
Remove and replace power supply module	1 min
Remove and replace system fan	7 min
Remove and replace control panel module	2 min
Remove and replace baseboard	15 min

8.3 Replacing the CMOS Battery

The lithium battery on the server board powers the real time clock (RTC) for several years in the absence of power. When the battery starts to weaken, it loses voltage, and the server settings stored in CMOS RAM in the RTC (for example, the date and time) may be wrong. Contact your customer service representative or dealer for a list of approved devices.

⚠ WARNING

Danger of explosion if battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the equipment manufacturer. Discard used batteries according to manufacturer's instructions.

⚠ ADVARSEL!

Lithiumbatteri - Eksplosionsfare ved fejlagtig håndtering. Udskiftning må kun ske med batteri af samme fabrikat og type. Levér det brugte batteri tilbage til leverandøren.

⚠ ADVARSEL

Lithiumbatteri - Eksplosjonsfare. Ved utskifting benyttes kun batteri som anbefalt av apparatfabrikanten. Brukt batteri returneres apparatleverandøren.

⚠ VARNING

Explosionsfara vid felaktigt batteribyte. Använd samma batterityp eller en ekvivalent typ som rekommenderas av apparattillverkaren. Kassera använt batteri enligt fabrikantens instruktion.

⚠ VAROITUS

Paristo voi räjähtää, jos se on virheellisesti asennettu. Vaihda paristo ainoastaan laitevalmistajan suosittelemaan tyyppiin. Hävitä käytetty paristo valmistajan ohjeiden mukaisesti.

8.4 Product Regulatory Compliance

The server chassis product, when correctly integrated per this guide, complies with the following safety and electromagnetic compatibility (EMC) regulations.

Intended Application – This product was evaluated as Information Technology Equipment (ITE), which may be installed in offices, schools, computer rooms, and similar commercial type locations. The suitability of this product for other product categories and environments (such as: medical, industrial, telecommunications, NEBS, residential, alarm systems, test equipment, etc.), other than an ITE application, may require further evaluation.

Notifications to Users on Product Regulatory Compliance and Maintaining Compliance

To ensure regulatory compliance, you must adhere to the assembly instructions in this guide to ensure and maintain compliance with existing product certifications and approvals. Use only the described, regulated components specified in this guide. Use of other products / components will void the UL listing and other regulatory approvals of the product and will most likely result in noncompliance with product regulations in the region(s) in which the product is sold.

To help ensure EMC compliance with your local regional rules and regulations, before computer integration, make sure that the chassis, power supply, and other modules have passed EMC testing using a server board with a microprocessor from the same family (or higher) and operating at the same (or higher) speed as the microprocessor used on this server board. The final configuration of your end system product may require additional EMC compliance testing. For more information please contact your local Intel Representative. This is an FCC Class A device and its use is intended for a commercial type market place.

8.5 Use of Specified Regulated Components

To maintain the UL listing and compliance to other regulatory certifications and/or declarations, the following regulated components must be used and conditions adhered to. Interchanging or use of other component will void the UL listing and other product certifications and approvals. Updated product information for configurations can be found on the Intel Server Builder Web site at http://www.intel.com/go/serverbuilder.
If you do not have access to Intel's Web address, please contact your local Intel representative.

- **Server chassis** (base chassis is provided with power supply and fans)—UL listed.
- **Server board**—you must use an Intel server board—UL recognized.
- **Add-in boards**—must have a printed wiring board flammability rating of minimum UL94V-1. Add-in boards containing external power connectors and/or lithium batteries must be UL recognized or UL listed. Any add-in board containing modem telecommunication circuitry must be UL listed. In addition, the modem must have the appropriate telecommunications, safety, and EMC approvals for the region in which it is sold.
- **Peripheral Storage Devices** - must be UL recognized or UL listed accessory and TUV or VDE licensed. Maximum power rating of any one device or combination of devices can not exceed manufacturer's specifications. Total server configuration is not to exceed the maximum loading conditions of the power supply.

The following table references Server Chassis Compliance and markings that may appear on the product. Markings below are typical markings however, may vary or be different based on how certification is obtained.

Table 34. Product Safety & Electromagnetic (EMC) Compliance

Compliance Regional Description	Compliance Reference	Compliance Reference Marking Example
Australia / New Zealand	AS/NZS 3548 (Emissions)	 N232
Argentina	IRAM Certification (Safety)	
Belarus	Belarus Certification	None Required
Canada / USA	CSA 60950 – UL 60950 (Safety)	
	Industry Canada ICES-003 (Emissions)	CANADA ICES-003 CLASS A CANADA NMB-003 CLASSE A
	FCC CFR 47, Part 15 (Emissions)	This device complies with Part 15 of the FCC Rules. Operation of this device is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) This device must accept interference receive, including interference that may cause undesired operation.
China	CNCA – CB4943 (Safety) GB 9254 (Emissions) GB17625 (Harmonics)	
CENELEC Europe	Low Voltage Directive 93/68/EEC; EMC Directive 89/336/EEC EN55022 (Emissions) EN55024 (Immunity) EN61000-3-2 (Harmonics) EN61000-3-3 (Voltage Flicker) CE Declaration of Conformity	
Germany	GS Certification – EN60950	
International	CB Certification – IEC60950 CISPR 22 / CISPR 24	None Required

Compliance Regional Description	Compliance Reference	Compliance Reference Marking Example
Japan	VCCI Certification	この装置は、クラス A 情報技術装置です。この装置を家庭環境で使用すると電波妨害を引き起こすことがあります。この場合には使用者が適切な対策を講ずるよう要求されることがあります。VCCI-A
Korea	RRL Certification MIC Notice No. 1997-41 (EMC) & 1997-42 (EMI)	MIC 인증번호: CPU-Model Name (A)
Russia	GOST-R Certification GOST R 29216-91 (Emissions) GOST R 50628-95 (Immunity)	PCT
Ukraine	Ukraine Certification	None Required
Taiwan	BSMI CNS13438	R33025 警告使用者： 這是甲類的資訊產品，在居住的環境中使用時，可能會造成射頻干擾，在這種情況下，使用者會被要求採取某些適當的對策

8.6 Electromagnetic Compatibility Notices

8.6.1 USA

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

For questions related to the EMC performance of this product, contact:

Intel Corporation
5200 N.E. Elam Young Parkway
Hillsboro, OR 97124
1-800-628-8686

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and the receiver.
- Connect the equipment to an outlet on a circuit other than the one to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Any changes or modifications not expressly approved by the grantee of this device could void the user's authority to operate the equipment. The customer is responsible for ensuring compliance of the modified product.

Only peripherals (computer input/output devices, terminals, printers, etc.) that comply with FCC Class B limits may be attached to this computer product. Operation with noncompliant peripherals is likely to result in interference to radio and TV reception.

All cables used to connect to peripherals must be shielded and grounded. Operation with cables, connected to peripherals that are not shielded and grounded may result in interference to radio and TV reception.

8.6.2 FCC Verification Statement

Product Type: SR1630; S5500BC

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

For questions related to the EMC performance of this product, contact:

Intel Corporation
5200 N.E. Elam Young Parkway
Hillsboro, OR 97124-6497

Phone: 1 (800)-INTEL4U or 1 (800) 628-8686

8.6.3 ICES-003 (Canada)

Cet appareil numérique respecte les limites bruits radioélectriques applicables aux appareils numériques de Classe A prescrites dans la norme sur le matériel brouilleur: “Appareils Numériques”, NMB-003 édictée par le Ministre Canadian des Communications.

(English translation of the notice above) This digital apparatus does not exceed the Class A limits for radio noise emissions from digital apparatus set out in the interference-causing equipment standard entitled “Digital Apparatus,” ICES-003 of the Canadian Department of Communications.

8.6.4 Europe (CE Declaration of Conformity)

This product has been tested in accordance too, and complies with the Low Voltage Directive (73/23/EEC) and EMC Directive (89/336/EEC). The product has been marked with the CE Mark to illustrate its compliance.

8.6.5 Japan EMC Compatibility

Electromagnetic Compatibility Notices (International)

この装置は、情報処理装置等電波障害自主規制協議会（ＶＣＣＩ）の基準に基づくクラスＡ情報技術装置です。この装置を家庭環境で使用すると電波妨害を引き起こすことがあります。この場合には使用者が適切な対策を講ずるよう要求されることがあります。

English translation of the notice above:

This is a Class A product based on the standard of the Voluntary Control Council For Interference (VCCI) from Information Technology Equipment. If this is used near a radio or television receiver in a domestic environment, it may cause radio interference. Install and use the equipment according to the instruction manual.

8.6.6 BSMI (Taiwan)

The BSMI Certification number and the following warning is located on the product safety label which is located on the bottom side (pedestal orientation) or side (rack mount configuration).

警告使用者：

這是甲類的資訊產品，在居住的環境中使用時，可能會造成射頻干擾，在這種情況下，使用者會被要求採取某些適當的對策。

8.6.7 RRL (Korea)

Following is the RRL certification information for Korea.

English translation of the notice above:

1. Type of Equipment (Model Name): On License and Product
2. Certification No.: On RRL certificate. Obtain certificate from local Intel representative
3. Name of Certification Recipient: Intel Corporation
4. Date of Manufacturer: Refer to date code on product
5. Manufacturer/Nation: Intel Corporation/Refer to country of origin marked on product

8.6.8 CNCA (CCC-China)

The CCC Certification Marking and EMC warning is located on the outside rear area of the product.

声明

此为A级产品，在生活环境中，该产品可能会造成无线电干扰。在这种情况下，可能需要用户对其干扰采取可行的措施。

8.7 Product Ecology Compliance

Intel has a system in place to restrict the use of banned substances in accordance with world wide product ecology regulatory requirements. The following is Intel's product ecology compliance criteria.

Table 35. Product Ecology Compliance Reference Table

Compliance Regional Description	Compliance Reference	Compliance Reference Marking Example
California	California Code of Regulations, Title 22, Division 4.5; Chapter 33: Best Management Practices for Perchlorate Materials.	Special handling may apply. See www.dtsc.ca.gov/hazardouswaste/perchlorate This notice is required by California Code of Regulations, Title 22, Division 4.5; Chapter 33: Best Management Practices for Perchlorate Materials. This product / part includes a battery which contains Perchlorate material.
China	**China RoHS** Administrative Measures on the Control of Pollution Caused by Electronic Information Products" (EIP) #39. Referred to as China RoHS. Mark requires to be applied to retail products only. Mark used is the Environmental Friendly Use Period (EFUP). Number represents years. **China Recycling (GB18455-2001)** Mark requires to be applied to be retail product only. Marking applied to bulk packaging and single packages. Not applied to internal packaging such as plastics, foams, etc.	 
Intel Internal Specification	All materials, parts and subassemblies must not contain restricted materials as defined in Intel's ***Environmental Product Content Specification*** of Suppliers and Outsourced Manufacturers – http://supplier.intel.com/ehs/environmental.htm	None Required
Europe	**Waste Electrical and Electronic Equipment (WEEE) Directive 2002/96/EC** – Mark applied to system level products only.	

Compliance Regional Description	Compliance Reference	Compliance Reference Marking Example
	European Directive 2002/95/EC - Restriction of Hazardous Substances (RoHS) Threshold limits and banned substances are noted below. Quantity limit of 0.1% by mass (1000 PPM) for: Lead, Mercury, Hexavalent Chromium, Polybrominated Biphenyls Diphenyl Ethers (PBB/PBDE) Quantity limit of 0.01% by mass (100 PPM) for: Cadmium	None Required
Germany	**German Green Dot** Applied to Retail Packaging Only for Boxed Boards	
Intel Internal Specification	All materials, parts and subassemblies must not contain restricted materials as defined in Intel's ***Environmental Product Content Specification*** of Suppliers and Outsourced Manufacturers – http://supplier.intel.com/ehs/environmental.htm	None Required
International	**ISO11469** - Plastic parts weighing >25gm are intended to be marked with per ISO11469.	>PC/ABS<
	Recycling Markings – Fiberboard (FB) and Cardboard (CB) are marked with international recycling marks. Applied to outer bulk packaging and single package.	 
Japan	**Japan Recycling** Applied to Retail Packaging Only for Boxed Boards	 

8.8 Other Markings

Compliance Description	Compliance Reference	Compliance Reference Marking Example
Stand-by Power	60950 Safety Requirement Applied to product is stand-by power switch is used.	
Multiple Power Cords	60950 Safety Requirement Applied to product if more than one power cord is used.	English: This unit has more than one power supply cord. To reduce the risk of electrical shock, disconnect (2) two power supply cords before servicing.
		Simplified Chinese: 注意： 本设备包括多条电源系统电缆。为避免遭受电击，在进行维修之前应断开两（2）条电源系统电缆。
		Traditional Chinese: 注意： 本設備包括多條電源系統電纜。爲避免遭受電擊，在進行維修之前應斷開兩（2）條電源系統電纜。
		German: Dieses Geräte hat mehr als ein Stromkabel. Um eine Gefahr des elektrischen Schlages zu verringern trennen sie beide (2) Stromkabeln bevor Instandhaltung.
Ground Connection	60950 Deviation for Nordic Countries	Line1 : "WARNING:" Swedish on line2: "Apparaten skall anslutas till jordat uttag, när den ansluts till ett nätverk." Finnish on line 3: "Laite on liitettävä suojamaadoituskoskettimilla varustettuun pistorasiaan." English on line 4: "Connect only to a properly earth grounded outlet."
Country of Origin	Logistic Requirements Applied to products to indicate where product was made.	Made in XXXX

Appendix A: Integration and Usage Tips

This section provides a list of useful information unique to the Intel® Server System SC5650BCDP that you should keep in mind while integrating the server system.

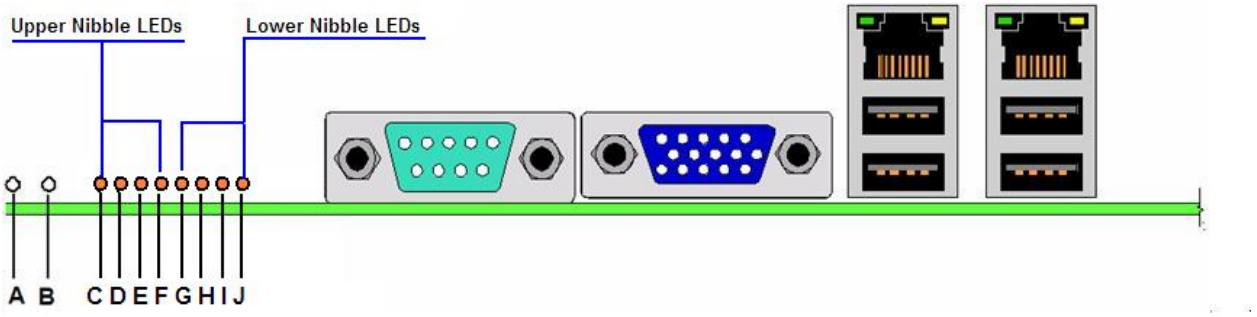
- The Intel® Server System SC5650BCDP requires the use of a shielded LAN cable to comply with Immunity regulatory requirements.
- You must use the system air duct to maintain system thermals.
- System fans are not hot-swappable.
- The FRUSDR utility must be run to load the proper sensor data records for the server chassis onto the server board.
- Make sure the latest system software is loaded. This includes the system BMC firmware, FRUSDR, and BIOS. You can download the latest system software from: http://support.intel.com/support/motherboards/server/S5500BC/

Appendix B: POST Code Diagnostic LED Decoder

The BIOS executes platform configuration processes during the system boot. Each process is assigned a specific hex POST code number. As each configuration routine is started, the BIOS displays the POST code on the POST Code Diagnostic LEDs on the back edge of the server board. The Diagnostic LEDs identify the last POST process to be executed.

Each POST code is represented by the eight amber Diagnostic LEDs. The POST codes are divided into two nibbles: an upper nibble and a lower nibble. The upper nibble bits are represented by Diagnostic LEDs #4, #5, #6, and #7. The lower nibble bits are represented by Diagnostics LEDs #0, #1, #2, and #3. Given the bit is set in the upper and lower nibbles, and then the corresponding LED is lit. If the bit is clear, corresponding LED is off.

Diagnostic LED #7 is labeled as “MSB” and the Diagnostic LED #0 is labeled as “LSB”.



A. ID LED	F. Diagnostic LED #4
B. Status LED	G. Diagnostic LED #3
C. Diagnostic LED #7 (MSB LED)	H. Diagnostic LED #2
D. Diagnostic LED #6	I. Diagnostic LED #1
E. Diagnostic LED #5	J. Diagnostic LED #0 (LSB LED)

Figure 16. Diagnostic LED Placement Diagram

In the following example, the BIOS sends a value of ACh to the diagnostic LED decoder. The LEDs are decoded as follows:

Table 36. POST Progress Code LED Example

	Upper Nibble LEDs				Lower Nibble LEDs			
	MSB							LSB
	LED #7	LED #6	LED #5	LED #4	LED #3	LED #2	LED #1	LED #0
	8h	4h	2h	1h	8h	4h	2h	1h
Status	ON	OFF	ON	OFF	ON	ON	OFF	OFF
	1	0	1	0	1	1	0	0
	Ah				Ch			

Upper nibble bits = 1010b = Ah; Lower nibble bits = 1100b = Ch; the two are concatenated as ACh.

Table 37. Diagnostic LED POST Code Decoder

Checkpoint	Diagnostic LED Decoder O = On, X=Off								Description
	Upper Nibble				Lower Nibble				
	MSB							LSB	
	8h	4h	2h	1h	8h	4h	2h	1h	
LED	#7	#6	#5	#4	#3	#2	#1	#0	
Multi-use code – This POST Code is used in different contexts.									
0xF2h	O	O	O	O	X	X	O	X	Seen at the start of Memory Reference Code (MRC)
									Start of the very early platform initialization code
									Very late in POST, it is the signal that the operating system has switched to virtual memory mode
Memory Error Codes (Accompanied by a beep code) **Note that these are codes used in early POST by Memory Reference Code. Later in POST these same codes are used for other Progress Codes. (These progress codes are not controlled by BIOS and are subject to change at the discretion of the Memory Reference Code team.)**									
0xE8h	O	O	O	X	O	X	X	X	No Usable Memory Error: No memory in the system, or SPD bad so no memory could be detected
0xEAh	O	O	O	X	O	X	O	X	Channel Training Error: DQ/DQS training failed on a channel during memory channel initialization. If no usable memory remains, system is halted.
0xEBh	O	O	O	X	O	X	O	O	Memory Test Error: memory failed Hardware BIST.
0xEDh	O	O	O	X	O	O	X	O	Population Error: RDIMMs and UDIMMs cannot be mixed in the system
0xEEh	O	O	O	X	O	O	O	X	Mismatch Error: more than 2 Quad Ranked DIMMS in a channel.
Memory Reference Code Progress Codes (Not accompanied by a beep code)									
0xB0h	O	X	O	O	X	X	X	X	Chipset Initialization Phase
0xB1h	O	X	O	O	X	X	X	O	Reset Phase
0xB2h	O	X	O	O	X	X	O	X	DIMM Detection Phase
0xB3h	O	X	O	O	X	X	O	O	Clock Initialization Phase
0Xb4h	O	X	O	O	X	O	X	X	SPD Data Collection Phase
0Xb6h	O	X	O	O	X	O	O	X	Rank Formation Phase
0xB8h	O	X	O	O	O	X	X	X	Channel Training Phase
0xB9h	O	X	O	O	O	X	X	O	Memory Test Phase
0xBAh	O	X	O	O	O	X	O	X	Memory Map Creation Phase
0xBBh	O	X	O	O	O	X	O	O	RAS Initialization Phase
0xBCh	O	X	O	O	O	O	X	X	MRC Complete
Host Processor									
0x04h	X	X	X	O	X	O	X	X	Early processor initialization (flat32.asm) where system BSP is selected
0x10h	X	X	X	O	X	X	X	X	Power-on initialization of the host processor (bootstrap processor)
0x11h	X	X	X	O	X	X	X	O	Host processor cache initialization (including AP)
0x12h	X	X	X	O	X	X	O	X	Starting application processor initialization
0x13h	X	X	X	O	X	X	O	O	SMM initialization
Chipset									
0x21h	X	X	O	X	X	X	X	O	Initializing a chipset component
Memory									
0x22h	X	X	O	X	X	X	O	X	Reading configuration data from memory (SPD on DIMM)
0x23h	X	X	O	X	X	X	O	O	Detecting presence of memory
0x24h	X	X	O	X	X	O	X	X	Programming timing parameters in the memory controller
0x25h	X	X	O	X	X	O	X	O	Configuring memory parameters in the memory controller
0x26h	X	X	O	X	X	O	O	X	Optimizing memory controller settings
0x27h	X	X	O	X	X	O	O	O	Initializing memory, such as ECC init
0x28h	X	X	O	X	O	X	X	X	Testing memory
PCI Bus									
0x50h	X	O	X	O	X	X	X	X	Enumerating PCI buses

Checkpoint	Diagnostic LED Decoder O = On, X=Off								Description
	Upper Nibble				Lower Nibble				
	MSB							LSB	
	8h	4h	2h	1h	8h	4h	2h	1h	
LED	#7	#6	#5	#4	#3	#2	#1	#0	
0x51h	X	O	X	O	X	X	X	O	Allocating resources to PCI buses
0x52h	X	O	X	O	X	X	O	X	Hot Plug PCI controller initialization
0x53h	X	O	X	O	X	X	O	O	Reserved for PCI bus
0x54h	X	O	X	O	X	O	X	X	Reserved for PCI bus
0x55h	X	O	X	O	X	O	X	O	Reserved for PCI bus
0X56h	X	O	X	O	X	O	O	X	Reserved for PCI bus
0x57h	X	O	X	O	X	O	O	O	Reserved for PCI bus
USB									
0x58h	X	O	X	O	O	X	X	X	Resetting USB bus
0x59h	X	O	X	O	O	X	X	O	Reserved for USB devices
ATA/ATAPI/SATA									
0x5Ah	X	O	X	O	O	X	O	X	Resetting SATA bus and all devices
0x5Bh	X	O	X	O	O	X	O	O	Reserved for ATA
SMBUS									
0x5Ch	X	O	X	O	O	O	X	X	Resetting SMBUS
0x5Dh	X	O	X	O	O	O	X	O	Reserved for SMBUS
Local Console									
0x70h	X	O	O	O	X	X	X	X	Resetting the video controller (VGA)
0x71h	X	O	O	O	X	X	X	O	Disabling the video controller (VGA)
0x72h	X	O	O	O	X	X	O	X	Enabling the video controller (VGA)
Remote Console									
0x78h	X	O	O	O	O	X	X	X	Resetting the console controller
0x79h	X	O	O	O	O	X	X	O	Disabling the console controller
0x7Ah	X	O	O	O	O	X	O	X	Enabling the console controller
Keyboard (only USB)									
0x90h	O	X	X	O	X	X	X	X	Resetting the keyboard
0x91h	O	X	X	O	X	X	X	O	Disabling the keyboard
0x92h	O	X	X	O	X	X	O	X	Detecting the presence of the keyboard
0x93h	O	X	X	O	X	X	O	O	Enabling the keyboard
0x94h	O	X	X	O	X	O	X	X	Clearing keyboard input buffer
0x95h	O	X	X	O	X	O	X	O	Instructing keyboard controller to run Self Test(PS/2 only)
Mouse (only USB)									
0x98h	O	X	X	O	O	X	X	X	Resetting the mouse
0x99h	O	X	X	O	O	X	X	O	Detecting the mouse
0x9Ah	O	X	X	O	O	X	O	X	Detecting the presence of mouse
0x9Bh	O	X	X	O	O	X	O	O	Enabling the mouse
Fixed Media									
0xB0h	O	X	O	O	X	X	X	X	Resetting fixed media device
0xB1h	O	X	O	O	X	X	X	O	Disabling fixed media device
0xB2h	O	X	O	O	X	X	O	X	Detecting presence of a fixed media device (hard drive detection, and so forth.)
0xB3h	O	X	O	O	X	X	O	O	Enabling / configuring a fixed media device
Removable Media									
0xB8h	O	X	O	O	O	X	X	X	Resetting removable media device
0xB9h	O	X	O	O	O	X	X	O	Disabling removable media device
0xBAh	O	X	O	O	O	X	O	X	Detecting presence of a removable media device (CD-ROM detection, and so forth.)
0xBCh	O	X	O	O	O	O	X	X	Enabling / configuring a removable media device
Boot Device Selection (BDS)									
0xD0	O	O	X	O	X	X	X	X	Trying to boot device selection 0
0xD1	O	O	X	O	X	X	X	O	Trying to boot device selection 1
0xD2	O	O	X	O	X	X	O	X	Trying to boot device selection 2

Checkpoint	Diagnostic LED Decoder O = On, X=Off								Description
	Upper Nibble				Lower Nibble				
	MSB							LSB	
	8h	4h	2h	1h	8h	4h	2h	1h	
LED	#7	#6	#5	#4	#3	#2	#1	#0	
0xD3	O	O	X	O	X	X	O	O	Trying to boot device selection 3
0xD4	O	O	X	O	X	O	X	X	Trying to boot device selection 4
0xD5	O	O	X	O	X	O	X	O	Trying to boot device selection 5
0xD6	O	O	X	O	X	O	O	X	Trying to boot device selection 6
0Xd7	O	O	X	O	X	O	O	O	Trying to boot device selection 7
0xD8	O	O	X	O	O	X	X	X	Trying to boot device selection 8
0xD9	O	O	X	O	O	X	X	O	Trying to boot device selection 9
0xDA	O	O	X	O	O	X	O	X	Trying to boot device selection A
0xDB	O	O	X	O	O	X	O	O	Trying to boot device selection B
0xDC	O	O	X	O	O	O	X	X	Trying to boot device selection C
0xDD	O	O	X	O	O	O	X	O	Trying to boot device selection D
0xDE	O	O	X	O	O	O	O	X	Trying to boot device selection E
0xDF	O	O	X	O	O	O	O	O	Trying to boot device selection F
Pre-EFI Initialization (PEI) Core									
0xE0h	O	O	O	X	X	X	X	X	Started dispatching early initialization modules (PEIM)
0xE1h	O	O	O	X	X	X	X	O	Reserved for Initializaiton module use (PEIM)
0xE2h	O	O	O	X	X	X	O	X	Initial memory found, configured, and installed correctly
0xE3h	O	O	O	X	X	X	O	O	Reserved for Initializaiton module use (PEIM)
Driver eXecution Environment (DXE) Core (not accompanied by a beep code)									
0xE4h	O	O	O	X	X	O	X	X	Entered EFI driver execution phase (DXE)
0xE5h	O	O	O	X	X	O	X	O	Started dispatching drivers
0xE6h	O	O	O	X	X	O	O	X	Started connecting drivers
DXE Drivers									
0xE7h	O	O	O	X	O	O	X	O	Waiting for user input
0xE8h	O	O	O	X	O	X	X	X	Checking password
0xE9h	O	O	O	X	O	X	X	O	Entering BIOS setup
0xEAh	O	O	O	X	O	X	O	X	Flash Update
0xEEh	O	O	O	X	O	O	O	X	Calling Int 19. One beep unless silent boot is enabled.
0xEFh	O	O	O	X	O	O	O	O	Unrecoverable boot failure
Runtime Phase / EFI Operating System Boot									
0xF4h	O	O	O	O	X	O	X	X	Entering Sleep state
0xF5h	O	O	O	O	X	O	X	O	Exiting Sleep state
0xF8h	O	O	O	O	O	X	X	X	Operating system has requested EFI to close boot services (ExitBootServices ( ) Has been called)
0xF9h	O	O	O	O	O	X	X	O	Operating system has switched to virtual address mode (SetVirtualAddressMap ( ) Has been called)
0xFAh	O	O	O	O	O	X	O	X	Operating system has requested the system to reset (ResetSystem ( ) has been called)
Pre-EFI Initialization Module (PEIM) / Recovery									
0x30h	X	X	O	O	X	X	X	X	Crisis recovery has been initiated because of a user request
0x31h	X	X	O	O	X	X	X	O	Crisis recovery has been initiated by software (corrupt flash)
0x34h	X	X	O	O	X	O	X	X	Loading crisis recovery capsule
0x35h	X	X	O	O	X	O	X	O	Handing off control to the crisis recovery capsule
0x3Fh	X	X	O	O	O	O	O	O	Unable to complete crisis recovery capsule

Appendix C: POST Error Messages and Handling

Whenever possible, the BIOS outputs the current boot progress codes on the video screen. Progress codes are 32-bit quantities plus optional data. The 32-bit numbers include class, subclass, and operation information. The class and subclass fields point to the type of hardware being initialized. The operation field represents the specific initialization activity. Based on the data bit availability to display progress codes, a progress code can be customized to fit the data width. The higher the data bit, the higher the granularity of information that can be sent on the progress port. The progress codes may be reported by the system BIOS or option ROMs.

The Response section in the following table is divided into three types:

- **Minor:** The message displays on the screen or in the Error Manager screen. The system continues booting with a degraded state. The user may want to replace the erroneous unit. The setup POST error Pause setting does not have any effect with this error.
- **Major:** The message is displayed in the Error Manager screen and an error is logged to the SEL. The setup POST error Pause setting determines whether the system pauses to the Error Manager for this type of error where the user can take immediate corrective action or choose to continue booting.
- **Fatal:** The message displays in the Error Manager screen, an error is logged to the SEL, and the system cannot boot unless the error is resolved. The user must replace the faulty part and restart the system. The setup POST error Pause setting does not have any effect with this error.

Table 38. SEL Format for POST Error Messages

Generator ID	Sensor Type Code	Sensor number	Type code	Event Data1	Event Data2	Event Data3
33h (BIOS POST)	**0Fh** (System Firmware Progress)	**06h** (BIOS POST Error)	**6Fh** (Sensor Specific Offset)	**A0h** (OEM Codes in Data2 & Data3)	**xxh** (Low Byte of POST Error Code)	**xxh** (High Byte of POST Error Code)

Table 39. POST Error Messages and Handling

Error Code	Error Message	Response
0012	CMOS date / time not set	Major
0048	Password check failed	Major
0108	Keyboard component encountered a locked error.	Minor
0109	Keyboard component encountered a stuck key error.	Minor
0113	Fixed Media: The SAS RAID firmware can not run properly. The user should attempt to reflash the firmware.	Major
0140	PCI component encountered a PERR error.	Major
0141	PCI resource conflict	Major
0146	PCI out of resources error	Major
0192	Processor 0x cache size mismatch detected.	Fatal
0193	Processor 0x stepping mismatch.	Minor
0194	Processor 0x family mismatch detected.	Fatal

Error Code	Error Message	Response
0195	Processor 0x Intel(R) QPI speed mismatch.	Major
0196	Processor 0x model mismatch.	Fatal
0197	Processor 0x speeds mismatched.	Fatal
0198	Processor 0x family is not supported.	Fatal
019F	Processor and chipset stepping configuration is unsupported.	Major
5220	CMOS/NVRAM Configuration Cleared	Major
5221	Passwords cleared by jumper	Major
5224	Password clear Jumper is Set.	Major
8160	Processor 01 unable to apply microcode update	Major
8161	Processor 02 unable to apply microcode update	Major
8180	Processor 0x microcode update not found.	Minor
8190	Watchdog timer failed on last boot	Major
8198	OS boot watchdog timer failure.	Major
8300	Baseboard management controller failed self-test	Major
84F2	Baseboard management controller failed to respond	Major
84F3	Baseboard management controller in update mode	Major
84F4	Sensor data record empty	Major
84FF	System event log full	Minor
8500	Memory component could not be configured in the selected RAS mode.	Major
8501	DIMM Population Error.	Major
8502	CLTT Configuration Failure Error.	Major
8520	DIMM_A1 failed Self Test (BIST).	Major
8521	DIMM_A2 failed Self Test (BIST).	Major
8522	DIMM_B1 failed Self Test (BIST).	Major
8523	DIMM_B2 failed Self Test (BIST).	Major
8524	DIMM_C1 failed Self Test (BIST).	Major
8525	DIMM_C2 failed Self Test (BIST).	Major
8526	DIMM_D1 failed Self Test (BIST).	Major
8527	DIMM_D2 failed Self Test (BIST).	Major
8528	DIMM_E1 failed Self Test (BIST).	Major
8529	DIMM_E2 failed Self Test (BIST).	Major
852A	DIMM_F1 failed Self Test (BIST).	Major
852B	DIMM_F2 failed Self Test (BIST).	Major
8540	DIMM_A1 Disabled.	Major
8541	DIMM_A2 Disabled.	Major
8542	DIMM_B1 Disabled.	Major
8543	DIMM_B2 Disabled.	Major
8544	DIMM_C1 Disabled.	Major
8545	DIMM_C2 Disabled.	Major
8546	DIMM_D1 Disabled.	Major
8547	DIMM_D2 Disabled.	Major
8548	DIMM_E1 Disabled.	Major
8549	DIMM_E2 Disabled.	Major
854A	DIMM_F1 Disabled.	Major

Error Code	Error Message	Response
854B	DIMM_F2 Disabled.	Major
8560	DIMM_A1 Component encountered a Serial Presence Detection (SPD) fail error.	Major
8561	DIMM_A2 Component encountered a Serial Presence Detection (SPD) fail error.	Major
8562	DIMM_B1 Component encountered a Serial Presence Detection (SPD) fail error.	Major
8563	DIMM_B2 Component encountered a Serial Presence Detection (SPD) fail error.	Major
8564	DIMM_C1 Component encountered a Serial Presence Detection (SPD) fail error.	Major
8565	DIMM_C2 Component encountered a Serial Presence Detection (SPD) fail error.	Major
8566	DIMM_D1 Component encountered a Serial Presence Detection (SPD) fail error.	Major
8567	DIMM_D2 Component encountered a Serial Presence Detection (SPD) fail error.	Major
8568	DIMM_E1 Component encountered a Serial Presence Detection (SPD) fail error.	Major
8569	DIMM_E2 Component encountered a Serial Presence Detection (SPD) fail error.	Major
856A	DIMM_F1 Component encountered a Serial Presence Detection (SPD) fail error.	Major
856B	DIMM_F2 Component encountered a Serial Presence Detection (SPD) fail error.	Major
85A0	DIMM_A1 Uncorrectable ECC error encountered.	Major
85A1	DIMM_A2 Uncorrectable ECC error encountered.	Major
85A2	DIMM_B1 Uncorrectable ECC error encountered.	Major
85A3	DIMM_B2 Uncorrectable ECC error encountered.	Major
85A4	DIMM_C1 Uncorrectable ECC error encountered.	Major
85A5	DIMM_C2 Uncorrectable ECC error encountered.	Major
85A6	DIMM_D1 Uncorrectable ECC error encountered.	Major
85A7	DIMM_D2 Uncorrectable ECC error encountered.	Major
85A8	DIMM_E1 Uncorrectable ECC error encountered.	Major
85A9	DIMM_E2 Uncorrectable ECC error encountered.	Major
85AA	DIMM_F1 Uncorrectable ECC error encountered.	Major
85AB	DIMM_F2 Uncorrectable ECC error encountered.	Major
8604	Chipset Reclaim of non critical variables complete.	Minor
9000	Unspecified processor component has encountered a non specific error.	Major
9223	Keyboard component was not detected.	Minor
9226	Keyboard component encountered a controller error.	Minor
9243	Mouse component was not detected.	Minor
9246	Mouse component encountered a controller error.	Minor
9266	Local Console component encountered a controller error.	Minor
9268	Local Console component encountered an output error.	Minor
9269	Local Console component encountered a resource conflict error.	Minor
9286	Remote Console component encountered a controller error.	Minor
9287	Remote Console component encountered an input error.	Minor
9288	Remote Console component encountered an output error.	Minor
92A3	Serial port component was not detected	Major
92A9	Serial port component encountered a resource conflict error	Major
92C6	Serial Port controller error	Minor
92C7	Serial Port component encountered an input error.	Minor
92C8	Serial Port component encountered an output error.	Minor
94C6	LPC component encountered a controller error.	Minor
94C9	LPC component encountered a resource conflict error.	Major

Error Code	Error Message	Response
9506	ATA/ATPI component encountered a controller error.	Minor
95A6	PCI component encountered a controller error.	Minor
95A7	PCI component encountered a read error.	Minor
95A8	PCI component encountered a write error.	Minor
9609	Unspecified software component encountered a start error.	Minor
9641	PEI Core component encountered a load error.	Minor
9667	PEI module component encountered a illegal software state error.	Fatal
9687	DXE core component encountered a illegal software state error.	Fatal
96A7	DXE boot services driver component encountered a illegal software state error.	Fatal
96AB	DXE boot services driver component encountered invalid configuration.	Minor
96E7	SMM driver component encountered a illegal software state error.	Fatal
0xA022	Processor component encountered a mismatch error.	Major
0xA027	Processor component encountered a low voltage error.	Minor
0xA028	Processor component encountered a high voltage error.	Minor
0xA421	PCI component encountered a SERR error.	Fatal
0xA500	ATA/ATPI ATA bus SMART not supported.	Minor
0xA501	ATA/ATPI ATA SMART is disabled.	Minor
0xA5A0	PCI Express component encountered a PERR error.	Minor
0xA5A1	PCI Express component encountered a SERR error.	Fatal
0xA5A4	PCI Express IBIST error.	Major
0xA6A0	DXE boot services driver Not enough memory available to shadow a legacy option ROM.	Minor
0xB6A3	DXE boot services driver Unrecognized.	Major

The following table lists POST error beep codes. Prior to system video initialization, the BIOS uses these beep codes to inform users of error conditions. The beep code is followed by a user-visible code on POST Progress LEDs.

Table 40. POST Error Beep Codes

Beeps	Error Message	POST Progress Code	Description
3	Memory error	Multiple	System halted because a fatal error related to the memory was detected.
The following Beep Codes are from the BMC, and are controlled by the Firmware team. They are listed here for convenience.			
1-5-2-1	CPU: Empty slot / population error.	N/A	CPU sockets are populated incorrectly – CPU1 must be populated before CPU2.
1-5-4-2	Power fault: DC power unexpectedly lost (power good dropout)	N/A	Power unit sensors – power unit failure offset.
1-5-4-4	Power control fault (Power good assertion timeout)	N/A	Power unit sensors – soft power control failure offset.

In case of POST error(s) listed as Major, the BIOS enters the error manager and waits for the user to press an appropriate key before booting the operating system or entering the BIOS Setup.

The user can override this option by setting the POST Error Pause option as disabled on the BIOS setup Main screen. If this option is disabled, the system boots the operating system without user intervention. The default is disabled.

Glossary

Word / Acronym	Definition
ACA	Australian Communication Authority
ANSI	American National Standards Institute
BMC	Baseboard Management Controller
CMOS	Complementary Metal Oxide Silicon
D2D	DC-to-DC
EMP	Emergency Management Port
FP	Front Panel
FRB	Fault Resilient Boot
FRU	Field Replaceable Unit
LCD	Liquid Crystal Display
LPC	Low-Pin Count
MTBF	Mean Time Between Failure
MTTR	Mean Time to Repair
OTP	Over-temperature Protection
OVP	Over-voltage Protection
PFC	Power Factor Correction
PSU	Power Supply Unit
RI	Ring Indicate
SCA	Single Connector Attachment
SDR	Sensor Data Record
SE	Single-Ended
UART	Universal Asynchronous Receiver Transmitter
USB	Universal Serial Bus
VCCI	Voluntary Control Council for Interference

Reference Documents

- *Intel® Server Board S5500BC Technical Product Specification*
- *Intel® Server Chassis SC5650 Technical Product Specification*
- *Intel® Server Board S5500BC / Intel® Server Chassis SC5650 / Intel® Server System SR1630BC Spares/Parts List and Configuration Guide*
- *Intel® S5500 Chipsets Server Board BIOS External Product Specification*