Advance Program

ICEP2013

International Conference on Electronics Packaging

April 10-12, 2013

Osaka International Convention Center
Osaka, Japan

Sponsored by JIEP, IEEE CPMT Society Japan Chapter and IMAPS

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With great honor and pleasure, we, the conference committee, welcome you to the 13th **International Symposium on Electronics Packaging (ICEP2013)** held in Osaka. ICEP is the premier international conference covering wide ranges of "Jisso", such as advanced semiconductor/electronics packaging, new materials, fabrication process, modeling/simulation, and applications. Both academic and industry professionals come together annually from all over the world. Since 1980, started as IMC, the impact of this conference has significantly grown up on electronics packaging field.

Following the successful meetings in Sapporo(2010), Nara(2011), and Tokyo(2012), the ICEP is proudly held in Osaka for the first time of its history from April 10 to 12, 2013, the best season of cherry blossoms. Osaka is not just only the second largest city in Japan, but also has successful history as the center for international trade and cultural interactions. In the 7th century, the oldest palace, Naniwa-no-miya" was built. During the 17th century, Osaka became the center for trade, thanks to the city's resourceful and enterprising merchants. In the Edo period of the 19th century, Osaka drastically developed as the gourmet city, "Kitchen of the Nation". Besides these, Osaka features the beautiful Osaka Castle, many traditional Buddhist temples, convenient access to Kyoto, Nara, and Kobe, and of course, friendly people with the best sense of humor in Japan.

Last year, ICEP2012 was jointly held with IMAPS All Asia Conference (IAAC) for the first time, and had many discussions for three and half days, including the Global Business Council, and IAAC special session. This year, ICEP2013 will return to the usual program schedule as three days with keynote speeches, technical sessions and reception. It is great pleasures for us, the conference committee, to invite three keynote speakers, Dr. Subramanian S. Iyer, IBM, Dr. Takeshi Uenoyama, Panasonic, and Dr. Urmi Ray, Qualcomm. Each technology session may also invite a special speaker, and more than 180 papers and over 20 posters will be presented. Major topics are: Advanced Packaging, Substrate & Interposer, 2.5D and 3DIC Packaging, Design/Modeling/Reliability, Thermal Management, Materials and Process, Printed Electronics, N-MEMS, Optoelectronics, Power Devices, RF, and Biomimetic. In addition, ASET session, Taiwan session, and Korean session will specially be held for intensive discussions. Also, Medical Device session will be organized for the first time with panel discussion.

We also plan to have welcome events to enjoy Osaka's friendly atmosphere and hospitality. We believe ICEP2013 will provide excellent opportunities for fruitful discussions on advanced technologies, and for developing global networks.

Finally, it is truly a great pleasure for me to serve as the general chairperson of ICEP2013, and I would like to express my special thanks to all the ICEP2013 Organizing Committee members for their enthusiastic work and collaboration, to Japan Institute of Electronics Packaging(JIEP) staff members for their continuous supports, and to many international friends for supporting special sessions, in order to make this conference successful.

I sincerely look forward to seeing you in April, and wish you all a pleasant stay in Osaka.

Shintaro Yamamichi
General Chairperson ICEP 2013

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	Room A (1003)	Room B (1002)	Room C (1001)	Room D (1004-5)
9:40	**WA1: 3DIC Packaging-1** **WA1-1** Identification of Through Silicon Via (TSV) Failure Point using Time Domain Reflectometry (TDR) Method Keiji Matsumoto[1], Hiroaki Otsuka[2], Osamu Horiuchi[3], Young Gun Han[3], Woon Choi[2], Hajime Tomokage[2,3], [1]Kitakyushu National College of Technology, [2]Fukuoka University, [3]Center of System Integration Platform Organization Standards / Japan **WA1-2** Advanced TSV Inspection for 3D Integration Takashi Tsuto[1], Yoshihiko Fujimori[1], Hiroyuki Tsukamoto[1], Kyoichi Suwa[1], Kazuya Okamoto[2], [1]Nikon, [3]Osaka University / Japan **WA1-3** Electrical Test Method of Open Defects at Bi-directional Interconnects in 3D ICs Masaki Hashizume[1], Shyue-Kung Lu[1,2], Hiroyuki Yotsuyanagi[1], [1]The University of Tokushima / Japan, [2]National Taiwan University of Science and Technology / Taiwan	**WB1: Interconnection-1** **WB1-1** <Session Invited> *(50min.)* iNEMI 2013 Technology Roadmap: Key Issues, Paradigm Shifts and Emerging Technology Trends Bill Bader, International Electronics Manufacturing Initiative (iNEMI) / USA **WB1-2** Development of Advanced Interconnection Technology for High Density Mounting Using Solder Sheet with Flux Adhesive Film Kei Kawasaki, Sumitomo Bakelite / Japan	**WC1: N-MEMS-1** **WC1-1** <Session Invited> VUV-Assisted Hybrid Bonding of Organic/Inorganic Substrates at Atmospheric Pressure Akitsu Shigetou[1], Mano Ajayan[1], Jun Mizuno[2], [1]National Institute for Materials Science (NIMS), [2]Waseda University / Japan **WC1-2** A Study of the Effect of Indium Filler Metal on the Bonding Strength of Copper and Tin Seng Keat Ting, Shinji Koyama, Yukinari Aoki, Naoki Hagiwara, Ikuo Shohji, Gunma University / Japan **WC1-3** Surface Activated Bonding of Laser Diode Chips Using N_2 Atmospheric-Pressure Plasma Michitaka Yamamoto[1], Eiji Higurashi[1], Tadatomo Suga[1], Renshi Sawada[2], [1]The University of Tokyo, [2]Kyushu University / Japan	**WD1: Thermal Management-1** **WD1-1** New Method for Evaluating Heat Transfer Material Yasuhiro Saito, Yuki Tsuji, Hiroyuki Emoto, Takanori Komuro, Kanagawa Institute of Technology / Japan **WD1-2** Establishment of Design Methods for High Thermal Conductive UF for FCPKG Toshiaki Enomoto, NAMICS / Japan **WD1-3** A Possible Method to Assess the Accuracy of a TIM Testing Solution Andras Vass-Varnai, Zoltan Sarkany, Csaba Barna, Sandor Laky, Marta Rencz, Mentor Graphics / Hungary
10:55				
	Break			
11:05	**WA2: 3DIC Packaging-2** **WA2-1** <Session Invited> Advanced TSV Fabrication Processes for Future Packaging Koukou Suu, Yasuhiro Morikawa, Takahide Murayama, Toshiyuki Sakuishi, Toshiyuki Nakamura, Yuu Nakamuta, ULVAC / Japan **WA2-2** Nonlinear FEA for a 3D SIC Package Improved by the Digital Image Correlation with SEM Toru Ikeda[1], Masatoshi Oka[2], Noriyuki Miyazaki[2], Keiji Matsumoto[3], Sayuri Kohara[3], Yasumitsu Orii[3], Fumiaki Yamada[3], Morihiro Kada[3], [1]Kagoshima University, [2]Kyoto University, [3]ASET / Japan **WA2-3** Finite Element Analysis for 3D IC Packaging Structural Design During Thermal Cycling You-Cheng Luo, Mei-Ling Wu, National Sun Yat-Sen University / Taiwan	**WB2: Interconnection-2** **WB2-1** Flip-chip Bonding with Variable Direction of Ultrasonic Vibration on a Pad Mutsumi Masumoto[1], Yoshiyuki Arai[1,2], Hajime Tomokage[1], [1]Fukuoka University, [2]Toray Engineering / Japan **WB2-2** Power Cycling Simulation of Flip Chip BGA Package during Stress Relaxation Yu-Sheng Lai, Mei-Ling Wu, National Sun Yat-Sen University / Taiwan **WB2-3** Microstructural Design in Ultrafine Interconnects under Current Stressing Hua Xiong[1], Zhiheng Huang[1], Paul Conway[2], Yong Zhang[1], Qingfeng Zeng[3], [1]Sun Yat-sen University / China, [2]Loughborough University / UK, [3]Northwestern Polytechnical University / China	**WC2: Materials and Processes-1** **WC2-1** <Session Invited> Chip Thinning Technologies for Chip Stacking Packages Shinya Takyu, Tetsuya Kurosawa, Toshiba / Japan **WC2-2** Development of the Au(Ag) Les Process Method in Solder Mounting of Si Device Yuu Nakamuta, ULVAC / Japan **WC2-3** Polymer/Glass and Polymer/Polymer Bonding at Room Temperature using a Modified Surface Activated Bonding Method Takashi Matsumae[1], Akitsu Shigetou[2], Masahisa Fujino[1], Yoshiei Matsumoto[3], Tadatomo Suga[1], [1]The University of Tokyo, [2]NIMS, [3]LANTECHNICAL SERVICE / Japan	**WD2: Thermal Management-2** **WD2-1** Analysis of Heat Generation from Power Si MOSFET Risako Kibushi, Tomoyuki Hatakeyama, Masaru Ishizuka, Toyama Prefectural University / Japan **WD2-2** Transient Heat Transfer of The Microprocessor System - Invenstigation regarding Natural Convection with Slate Style Chassis Koji Nishi[1], Tomoyuki Hatakeyama[2], Masaru Ishizuka[1], [1]AMD Japan, [2]Toyama Prefectural University / Japan **WD2-3** Experimental Evaluation of the Cooling Performance of Compact Heat Sink for LSI Packages Masaru Ishizuka, Tomoyuki Hatakeyama, Risako Kibushi, Toyama Prefectural University / Japan
12:20				
	Lunch			
13:10	**Award Ceremony**			
13:35				
	Poster Session / Break			
14:00	**Keynote Speeches** (Room A) **Keynote Speech 1** From Deep Trends to Skyscrapers −Orthogonal Scaling Subramanian S. Iyer, International Business Machines			
15:00	**Keynote Speech 2** R&D Strategy to Become No.1 Green Innovation Company. Takeshi Uenoyama, Panasonic			
16:00	**Keynote Speech 3** Architecture Trends in Mobile Industry and Impact on Packaging and Integration Urmi Ray, Qualcomm			
17:00				
	Welcome Reception			

*The content of the program may be subject to change without any prior notice.
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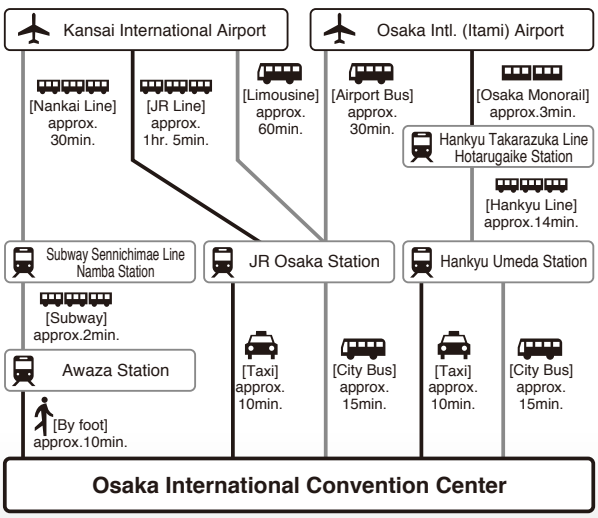

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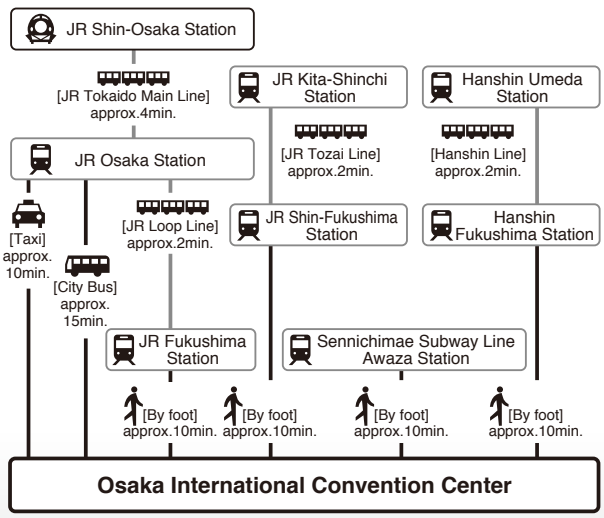

	Room A (1003)	Room B (1002)	Room C (1001)	Room D (1004)	Room E (1005)
9:10	**TA1: ASET-1** **TA1-1** High Precision Bonding for Fine-pitch Interconnection Kuniaki Sueoka, Fumiaki Yamada, Hidekazu Kikuchi, Kenichi Takeda, Yasumitsu Orii. Association of Super-Advanced Electronics Technologies (ASET) / Japan **TA1-2** 3D Package Assembly Development with the Use of the Dicing Tape Having NCF Layer Kosuke Kitaichi[1], Haruo Shimamoto[1], FumiakiYamada[2], Kuniaki Sueoka[2], [1]ASET, Renesas Electronics, [2]ASET, IBM Japan / Japan **TA1-3** 3D Integration Technology Using Hybrid Wafer Bonding and Its Electrical Characteristics Kazuyuki Hozawa, Kenichi Takeda, Mayu Aoki, Futoshi Furuta, Azusa Yanagisawa, Hidekazu Kikuchi, Toshio Mitsuhashi, Harufumi Kobayashi, ASET / Japan **TA1-4** RF MEMS Devices and 3D Heterogeneous Integration Fumihiko Nakazawa, Hiroaki Inoue, Takashi Katsuki, Tadashi Nakatani, Takashi Yamagajo, Xiaoyu Mi, ASET, FUJITSU LABORATORIES / Japan	**TB1: Printed Electronics-1** **TB1-1** <Session Invited> *(50min.)* Trend and development of Advanced Printed Electronics Technologies for New Flexible Electronics Fields Toshihide Kamata, National Institute of Advanced Industrial Science and Technology(AIST) / Japan **TB1-2** <Session Invited> Pattern Formation Technology of NnanoPaste for Printed Electronics Makoto Nakatani, HARIMA CHEMICALS / Japan **TB1-3** <Session Invited> Development of Low Temperature Sintered Clustered Nano Silver Pastes for Die Attach Application Using Resin Reinforcing Technology Koji Sasaki, NAMICS / Japan	**TC1: Advanced Packaging-1** **TC1-1** <Session Invited> Meterials, Structures, and Processes Eliminate Lead in Electronic Manufacturing Charles E. Bauer, Herbert J. Neuhaus, TechLead / USA **TC1-2** Novel GPS SiP Module with Miniaturized Substrate by Using RF Sub-Circuit Embedding Technology Yasuhiko Katsuhara[1], Masaya Tanaka[1], Desmond Wong[2], [1]Dai Nippon Printing, [2]Telit Wireless Solutions / Japan **TC1-3** High Performance 3D Package for Wide IO Memory Ilyas Mohammed, Hiroaki Sato, Yukio Hashimoto, Invensas / USA **TC1-4** DIMM-in-a-PACKAGE Memory Module Devices for Ultra-Thin Client Computing Richard D. Crisp, Kevin Chen, Wael Zohni, Invensas / USA	**TD1: N-MEMS-2** **TD1-1** <Session Invited> iNEMI MEMS Collaborative Projects and Opportunities Bill Bader, International Electronics Manufacturing Initiative (iNEMI) / USA **TD1-2** Development of Reel to Reel Chip Mounting System for LED Lighting Seiichi Takamatsu[1], Takahiro Yamashita[2], Takahiko Imai[2], Toshihiro Itoh[1], [1]AIST, [2]BEANS Laboratory / Japan **TD1-3** A 0.18-μm Standard CMOS Process Utilizing CMOS MEMS Switches in RF Power Amplifier Exchanges Dual-Band (2.4-GHz / 5.2-GHz) Jung-Tang Huang, Chia-Jung YEH, National Taipei University of Technology / Taiwan **TD1-4** SU-8 Microfluidic Chip Integrated with Indium Tin Oxide (ITO) Electrodes for Organic Light Emitting Device Applications Takashi Kasahara[1], Shigeyuki Matsunami[2], Tomohiko Edura[2], Miho Tsuwaki[1], Juro Oshima[2,3], Chihaya Adachi[2], Shuichi Shoji[1], Jun Mizuno[1], [1]Waseda University, [2]Kyushu University, [3]Nissan Chemical Industries / Japan	**TE1: DMR-Electrical-1** **TE1-1** Cool System - An Energy-Efficient and Scalable 3D Heterogeneous Multi-Chip System Consists of Cool Interconnect, Cool Chip, and Cool Software Yukoh Matsumoto, TOPS Systems / Japan **TE1-2** Power Supply Noise Minimization by Designing Variable On-die Resistance and Capacitance Sho Kiyoshige, Wataru Ichikawa, Ryota Kobayashi, Genki Kubo, Hiroki Otsuka, Toshio Sudo, Shibaura Institute of Technology / Japan **TE1-3** A Multi-Stage Broadband Impedance Matching Circuit Built into FC-BGA Substrate Package for Over 12Gbps SerDes Application Shuichi Kariyazaki, Ryuichi Oikawa, Yasuhiko Suzuki, Renesas Electronics / Japan **TE1-4** Electrical Study of Differential Clock in Multi-Chip Packages Die-to-Die Interconnection Min Keen Tang, Wei Jern Tan, Intel / Malaysia
10:50					
	Break				
11:00	**TA2: ASET-2** **TA2-1** Cooling Strategy and Structure of 3D Integrated Image Sensor for Auto Mobile Application Fumiaki Yamada[1], Keiji Matsumoto[1], Tomoyuki Hatakeyama[2], Masaru Ishizuka[2], Koji. Kondo[3], Kanji Otsuka[4], Harufumi Kobayashi[1], Kuniaki Sueoka[1], Akihiro Horibe[1], Sayuri Kohara[1], Hiroyuki Mori[1], Yasumitsu Orii[1], [1]ASET, [2]Toyama Prefectural University, [3]Denso, [4]Meisei University / Japan **TA2-2** DRAM & CMOS Device Characteristics Affected by Ultra Thin Wafer Thinning Haruo Shimamoto[1], Shigeaki Saito[1], Koske Kitaichi[1], Shoji Yasunaga[2], Kang Wook Lee[3], Tetsu Tanaka[3], Mitsumasa Koyanagi[3], [1]ASET, Renesas Electronics, [2]ASET, Rohm, [3]ASET, Tohoku University / Japan **TA2-3** Scalable IO Circuits for 3D TSV Stacked Layers Futoshi Furuta, Kenichi Osada, Kenichi Takeda, ASET / Japan **TA2-4** Measurement and Simulation of SSO Noise Reduction of 3D-SiP with 4K-IO Widebus Structure Masaomi Sato[1], Yosuke Tanaka[1], Hiroki Takatani[1], Haruya Fujita[1], Toshio Sudo[1], Atsushi Sakai[2], Shiro Uchiyama[2], Hiroaki Ikeda[2], [1]Shibaura Institute of Technology, [2]ASET / Japan	**TB2: Printed Electronics-2** **TB2-1** <Session Invited> Transparent Conductive Oxide Patterning on GaN Substrate by Screen Printing with Nanoparticle Pastes Yukiyasu Kashiwagi[1], Atsushi Koizumi[2], Yasutaka Takemura[3], Mari Yamamoto[1], Masashi Saitoh[1], Masanari Takahashi[1], Toshinobu Ohno[1], Yasufumi Fujiwara[2], Koichiro Murahashi[3], Kuniaki Ohtsuka[3], Masami Nakamoto[1], [1]Osaka Municipal Technical Research Institute, [2]Osaka University, [3]OKUNO CHEMICAL INDUSTRIES / Japan **TB2-2** <Session Invited> Latest Printing Materials for Printed Electronics Kaori Eguchi, JNC Petrochemical / Japan **TB2-3** Processing Thick-Film Conductive Inks with Photonic Curing Stan Farnsworth, Kurt Schroder, Dave Pope, Ian Rawson, Andrew Edd, NovaCentrix / USA **TB2-4** <Session Invited> Theoretical Consideration of Micro Droplet Formation in a Piezo Inkjet Shinri Sakai, The University of Tokyo / Japan	**TC2: Advanced Packaging-2** **TC2-1** Memory On Reversed Package-A Novel Packaging Solution Howe Yin Loo, Intel Microelectronics (M) / Malaysia **TC2-2** Fabrication and Evaluation of Thin Embedded LSI Chip Package for the Package-on-Package Structure by Using LSI and Package Co-Design Methodology Daisuke Ohshima[1], Kentaro Mori[1], Yoshiki Nakashima[1], Katsumi Kikuchi[1], Hideki Sasaki[2], Shintaro Yamamichi[1], [1]NEC, [2]NEC Electronics / Japan **TC2-3** The Predictions of Wire Sag for Semiconductor Packaging of 3-Dimensional and Multi-Chip Modules Huang-Kuang Kung[1], J.C. Hsiung[1], J.N. Lee[1], H.S. Chen[1], Jan-Yee Kung[2], [1]Cheng Shiu University, [2]National Kaohsiun University of Applied Sciences / Taiwan **TC2-4** Implementation of a Silicon-Based LED Packaging Module with Temperature Sensor Chingfu Tsou, Shengwei Chang, Chenghan Huang, Feng Chia University / Taiwan	**TD2: Optoelectronics-1** **TD2-1** Simultaneous Optical and Electrical Connection for Optical Interconnect Yoichi Taira, Hidetoshi Numata, IBM Research - Tokyo / Japan **TD2-2** High Bandwidth Density and Low Power Optical MCM Masao Tokunari, Yutaka Tsukada, Kazushige Toriyama, Hirokazu Noma, Shigeru Nakagawa, IBM Research - Tokyo / Japan **TD2-3** Fabrication of Cavity-Resonator-Integrated Guided-Mode Resonance Filter with Channel Waveguide Junichi Inoue[1], Tomonori Ogura[1], Koji Hatanaka[1], Kenji Kintaka[2], Kenzo Nishio[1], Yasuhiro Awatsuji[1], Shogo Ura[1], [1]Kyoto Institute of Technology, [2]National Institute of Advanced Industrial Science and Technology / Japan **TD2-4** Development of Subassemblies for Active Optical Cable using 14Gbps VCSELs Takuya Oda, Takayuki Tanaka, Teijiro Ori, Fujikura / Japan	**TE2: DMR-Electrical-2** **TE2-1** Electrical Design Optimization for High-Bandwidth Die-to-Die Interconnection in a MCP Package Jackson Kong, Bok Eng Cheah, Thim Khuen Wong, Intel Microelectronics (M) / Malaysia **TE2-2** Impact of Package Power Referencing to Multi-Gbps Serial I/O Channel Margin Jackson Kong, Jiun Kai Beh, Darren Tan, Intel Microelectronics (M) / Malaysia **TE2-3** High Speed DDR3 System Level On-Die Power Grid Design for System-On-Chip (SoC) Power Integrity Heng Chuan Shu, Li Chuang Quek, Intel Microelectronics Malaysia / Malaysia **TE2-4** PDN Impedance Estimation Techniques Based on Transmission Matrix Method for Design Optimization of Wire Bonding BGA Packages Masahiro Toyama, Hidenari Nakashima, Kazuyuki Sakata, Mikiko Sode Tanaka, Motoo Suwa, Atsushi Nakamura, Renesas Electronics / Japan
12:40					
	Lunch				
13:30	**TA3: Taiwan Session-1** **TA3-1** Systemic Integration of Interconnections - from OSAT perspective Mike Ma, Siliconware Precision Industries (SPIL) / Taiwan **TA3-2** IC Substrate Challenges D.C. Hu, Unimicron / Taiwan **TA3-3** Advanced IC Substrate and Package Material T.M. Lee, ITRI / Taiwan **TA3-4** Advanced 3D SiP/3D Integration W.C. Lo, ITRI / Taiwan	**TB3: Printed Electronics-3** **TB3-1** <Session Invited> CAD to BMP Conversion Software for Inkjet Printing on Flexible Substates Masaaki Oda[1], Kenya Uwaya[2], [1]ULVAC, [2]Zuken / Japan **TB3-2** Pico-liter Dispenser with Needle and Tube for Repair Systems Yoshiyuki Kato, Ei Ka, Sadayuki Takahashi, Applied Micro Systems / Japan **TB3-3** <Session Invited> Development of the Super Precision Gravure Offset / Flexo Printing Kotaro Baba, Takafumi kuwano, Micro Engineering / Japan **TB3-4** <Session Invited> Joint Strength of Cu-to-Cu Joint Using Cu Nanoparticle Paste Hiroshi Nishikawa, Osaka University / Japan	**TC3: Interconnection-3** **TC3-1** Transferring Carbon Nanotube Bumps on Polyimide as Flexible Multilayer Substrate Masahisa Fujino[1], Hidenori Terasaka[1], Tadatomo Suga[1], Ikuo Soga[2], Daiyu Kondo[2], Yoshikatsu Ishizuki[2], Taisuke Iwai[2], [1]The University of Tokyo, [2]Fujitsu, Fujitsu Laboratories / Japan **TC3-2** Carbon Nanostructures Interconnects Dedicated to RF Nanopackaging Christophe Brun[1,2], Chin Chong Yap[1,3], Dominique Baillargeat[1], Beng Kang Tay[1,3], [1]Research Techno Plaza / Singapore, [2]Universite de Limoges / France, [3]Nanyang Technological University / Singapore **TC3-3** A new High Temperature Packaging for SiC Power Devices by Using Ni Electroplating interconnection Kohei Tatsumi, Noriyuki Katou, Waseda University / Japan **TC3-4** Study of Low Temperature Cu Electrodes Bonding Based on Different Formic Acid In-Situ Treatment Processes Wenhua Yang, Masatake Akaike, Masahisa Fujino, Tadatomo Suga, The University of Tokyo / Japan	**TD3: Optoelectronics-2** **TD3-1** Optimum Core Structure and Size of Polymer Optical Waveguide for On-Board and Board-to-board Interconnects Ryota Kinoshita, Keishiro Shitanda, Takaaki Ishigure, Keio University / Japan **TD3-2** Reliability and Polarization Characteristics of Optical Devices by using Silane Modified Highly Moisture-Resistant Optical Adhesives Seiko Mitachi[1], Kazushi Kimura[2], [1]Tokyo University of Technology, [2]The Yokohama Rubber / Japan **TD3-3** Development of a 200 kHz Swept Light Source Using a KTN Deflector and High-Speed Optical Coherence Tomography System Yuichi Okabe[1,2], Masahiro Ueno[1], Yuzo Sasaki[1], Takashi Sakamoto[1], Seiji Toyoda[1], Junya Kobayashi[1], Yoshihiko Sugawa[2], Akihiro Fukuda[2], Masato Ohmi[2], [1]NTT, [2]Osaka University / Japan **TD3-4** Room-Temperature Direct Bonding of GaAs and SiC Wafers for Improved Heat Dissipation in High-Power Semiconductor Lasers Eiji Higurashi, Kaori Nakasuji, Tadatomo Suga, The University of Tokyo / Japan	**TE3: DMR-Mechanical-1** **TE3-1** Reliability of Electroless Nickel Immersion Gold Finishes John Roller, Bhanu Sood, Michael Pecht, University of Maryland / USA **TE3-2** Unique Adhesion Testing and MSL Modeling Masazumi Amagai, Texas Instruments, Japan / Japan **TE3-3** Study of Surface Treatment on Flip Chip Underfill Adhesion by Using Canti-Lever Beam Test Keishi Okamoto, K. Toriyama, A. Horibe, IBM Japan / Japan **TE3-4** Multiscale Multiphysics Electromigration Simulator Based on Ultra-Accelerated Quantum Chemical Molecular Dynamics Method Akira Miyamoto[1], Ryuji Miura[1], Ai Suzuki[1], Nozomu Hatakeyama[1], Kunio Shiokawa[2], Mitsuo Yamashita[2], [1]Tohoku University, [2]Fuji Electric / Japan
15:10					
	Poster Session / Break				
15:40	**TA4: Korea Session-1** **TA4-1** Simulation and Measurement of the Warpage for the Package-on-Package with Variations of Epoxy Molding Compounds and Process Variables Dong-Myung Jung[1], Min-Young Kim[1], Hyouk Lee[2], Carlos Moraes[3], Guilherme Vaccaro[3], Tae-Sung Oh[1], [1]Hongik University, [2]Hana Micron / Korea, [3]Unisinos University / Brazil **TA4-2** Design and Fabrication of an Organic High Density Interconnection Substrate with Ultra Fine Pattern Christian Romero, Dongwhan Lee, Seungwook Park, Mijin Park, Youngdo Kweon, Samsung Electromechanics / Korea **TA4-3** Effects of Bath Conditions and Operating Parameters on Electroless Nickel-Iron Alloy Plating for UBM Applications Myung-Won Jung[1], Jae-Ho Lee[1], Sung K. Kang[2], [1]Hongik University / Korea, [2]IBM / USA **TA4-4** The Effect of Low Temp Soldering Using Sn-In Solder Addition in Sn-Ag-Cu Solder on the Board Level Package Ji Won Jeong, SK Hynix / Korea **TA4-5** Analysis of Electrical and Mechanical Characteristics of Screen-Printed Cu Circuit with Its Fracture Structure Kwang-Seok Kim[1], Wataru Takahara[2], Seung-Boo Jung[1], [1]Sungkyunkwan University / Korea, [2]Osaka University / Japan	**TB4: Printed Electronics-4** **TB4-1** Influence of Semi-Additive Respective Subtractive Process on Etch Factor and Characteristic Impedance of PWB Trace Arash Risseh, Rikard Qvarnstrom, Jerker Delsing, Lulea University of Technology / Sweden **TB4-2** Development of Solution Processed Inorganic Flexible Thin-Film Transistor Takashi Matsumoto, Shingo Komatsu, Takashi Ichiryu, Tetsuyoshi Ogura, Koichi Hirano, Takeshi Suzuki, Panasonic / Japan **TB4-3** Low Temperature Co-Fired High Current Multilayer Ferrite Inductor Mean Jue Tung, W. S. Ko, Y. T. Haung, S. Y. Tong, M. D. Yang, ITRI / Taiwan (16:55)	**TC4: Interconnection-4** **TC4-1** iNEMI Cu Wire Bonding Project Update on Technology Investigation Reliability Test with Concerns Masahiro Tsuriya, International Electronics Manufacturing Initiative (iNEMI) / Japan **TC4-2** Cu Wire-Bonding for 28 nm Wafer Technology Andy Tseng[1], Shoji Uegaki[2], Bryan Lin[3], Louie Huang[3], [1]ASEUS / USA, [2]ASEJP / Japan, [3]ASEKH / Taiwan **TC4-3** A Comparison Study on Interconnection with Using Cooper and Silver Wires in Wedge Bonding for High Temperature Power Devices Zhou Yu, Kohei Tastumi, Waseda University / Japan **TC4-4** VUV/O_3 Treatment for Reduction of Au-Au Bonding Temperature Akiko Okada[1], Masatsugu Nimura[1], Akitsu Shigetou[2], Katsuyuki Sakuma[3], Jun Mizuno[1], Shuichi Shoji[1], [1]Waseda University, [2]NIMS / Japan, [3]IBM / USA **TC4-5** An Investigation on Nanoscale Tensile Mechanical Properties for Pd-coated Copper Wire Hsiang-Chen Hsu[1], Jih-Hsin Chien[1], Li-Ming Chu[1], Shin-Pon Ju[2], Yu-Ting Feng[2], Shen-Li Fu[1], [1]I-Shou University, [2]National Sun Yat-Sen University / Taiwan	**TD4: Optoelectronics-3** **TD4-1** <Session Invited> LED & SSL Packaging Trends View by x-ray Imaging Tetsuya Onishi, Grand Joint Technology / Hong Kong **TD4-2** LED Wafer Level Packaging with a Waffle Pack Remote Phosphor Layer Huihua LIU, S. W. Ricky LEE, Hong Kong University of Science & Technology / Hong Kong **TD4-3** High Bright White LED COB Packaging Technology and It's Applications Atsushi Okuno, SANYU REC / Japan **TD4-4** Shape and Structure of Conductive Polymeric Electrospinning Nanofiber Chih-Hao Hsu, Jheng-Jhih Pan, Cho-Liang Chung, Sheng-Min Hung, Sheng-Li Fu, I-Shou University / Taiwan **TD4-5** Routine Thermal Erasing Procedure (RTEP) and Annealing Effect on the Photoelectronic Properties of Semi-conductive Polymers Yu-hsuanLin, Yi-ShiangChen, Cho-Liang Chung, Yi-Jiun Huang, Sheng-Li Fu, I-Shou University / Taiwan	**TE4: DMR-Electrical-3** **TE4-1** Multi Chip Package Power Integrity Design for High Speed High Power Density SoC Design Li Chuang Quek, Intel / Malaysia **TE4-2** Open Defect Detection in Assembled PCBs by Supply Current Testing with Electrodes Embedded inside ICs Akira Ono[1], Masao Takagi[1], Hiroyuki Yotsuyanagi[2], Masaki Hashizume[2], [1]Kagawa National College of Technology, [2]Tokushima University / Japan **TE4-3** Fine Pitch Multilayer Board with CPW Structure Including Mesh Plane Ki-Jae Song, Samsung Electronics / Korea **TE4-4** EMC Mitigation Impacts on USB 3.0 Signaling Florence Phun[1], Dong-Ho Han[2], Ho Kah Wai[1], Jon Schenk[2], Howard Heck[2], [1]Intel Microelectronics (M) / Malaysia, [2]Intel / U.S.A **TE4-5** Electromagnetic Band Gap Structure in 3-D Stacked Printed Circuit Board Tadahiro Sasaki, Hiroshi Yamada, Tooru Kijima, Mitsuru Otani, Kazuhisa Imura, Toshiba / Japan
17:45					

*DMR: Design, Modeling and Reliability

Room A (1003)

FA1: 3DIC Packaging-3

FA1-1 <Session Invited>
3DIC Architectures for Next Generation High-Performance/Low-Power Computing
Koji Inoue, Kyusyu University / Japan

FA1-2
Investigation of Program-Voltage Generator Integration for ReRAM and NAND Flash Memory Hybrid Three-Dimensional Solid-State Drive
Teruyoshi Hatanaka[1,2], Koh Johguchi[1], Ken Takeuchi[1], [1]Chuo University, [2]The University of Tokyo / Japan

FA1-3
System Design Method of 3D System LSI from System Definition Model with Automatic SDSI-Cubic
Yoshiharu Iwata, Hidenori Murata, Ryouhei Satoh, Koichiro Atsumi, Kazuya Okamoto, Osaka University / Japan

FA1-4
Testing Method of Wide Bus Chip-to-Chip Interconnection for 3D LSI Chip Stacking System
Masahiro Aoyagi[1], F. Imura[1], S. Nemoto[1], N. Watanabe[1], F. Kato[1], K. Kikuchi[1], H. Nakagawa[1], M. Hagimoto[2], H. Uchida[2], Y. Matsumoto[2], [1]AIST, [2]TOPS Systems / Japan

Break

FA2: 3DIC Packaging-4

FA2-1
Study of Low Load and Temperature Solid-Phase Sn-Ag Bonding with Formation of High Heat-Resistant Ag_3Sn Intermetallic Compound Via Nanoscale Thin Film Control for Wafer-Level 3D-Stacking for 3D LSI
Kiyoto Yoneta, Ryohei Satoh, Yoshiharu Iwata, Koichiro Atsumi, Kazuya Okamoto, Yukihiro Sato, Osaka University / Japan

FA2-2
Optimization of High Thermal Conductive ICF for 3D-IC through Pre-applied Process
Yasuhiro Kawase[1], Makoto Ikemoto[1], Masanori Yamazaki[2], Hideki Kiritani[1], Fumikazu Mizutani[1], Keiji Matsumoto[3], Akihiro Horibe[3], Hiroyuki Mori[3], Yasumitsu Orii[3], [1]Mitsubishi Chemical, [2]Mitsubishi Chemical Group Science and Technology Research Center, [3]IBM Japan / Japan

FA2-3
Assembly of 3D-Stacked Chip Architecture with 30μm Pitch Micro Bump Interconnections Using Paste-type and Sheet-type Adhesive Materials
Yu-Wei Huang, Jing-Ye Juang, Chau-Jie Zhan, Yu-Min Lin, Shin-Yi Huang, Chia-Wen Fan, Su-Ching Chung, Jon-Shiou Peng, Su-Mei Chen, Yu-Lan Lu, Tao-Chih Chang, ITRI / Taiwan

FA2-4
Chip-to-Wafer 3D Stacking Using Self-Assembly and Electrostatic Temporary Bonding/Debonding
Hideto Hashiguchi, Takafumi Fukushima, Jicheol Bea, Hisashi Kino, Kangwook Lee, Tetsu Tanaka, Mitsumasa Koyanagi, Tohoku University / Japan

Lunch

FA3: Korea Session-2

FA3-1
Development of SDRAM Package Module for Satellite
Hyouk Lee[1], Jinwook Jeong[1], Jangsoo Chae[2], Miyoung Park[2], [1]HanaMicron, [2]SaTRec(Satellite Technology Research Center) / Korea

FA3-2
Epoxy Copper Paste as an Isotropic Conductive Adhesive
Yong-Sung EOM, Hyun-Cheol Bae, Kwang-Seong CHOI, Electronics and Telecommunications Research Institute / Korea

FA3-3
Low-Temperature Flip Chip Process for Stretchable Electronic Packaging
Jung-Yeol Choi[1], Jae-Hwan Kim[1], Kwan-Jae Shin[1], Yong-Ki Sohn[2], Tae-Sung Oh[1], [1]Hongik University, [2]Electronics and Telecommunications Research Institute / Korea

FA3-4
Study of Mechanical Properties in Organic Embedded Package Substrate According to Base Materials
Lee Han Sung, LeeYong Bin, Kwan Sun Yun, Daeduck Electronics / Korea

FA3-5
Electrical Properties of Organic Solar Cells with LiF Buffer Layers
Kun Ho Kim[1], Seung Ho Kim[1], Young Chul Chang[2], Ho Jung Chang[1], [1]Dankook University, [2]Korea University of Technology and Education / Korea

Break

FA4: Taiwan Session-2

FA4-1
Board Level Drop Impact Assessment of 3D Chip-on-Chip Packages
Hsien-Chie Cheng[1], Hsin-Kai Cheng[2], Wen-Hwa Chen[2], Tzu-Hsuan Cheng[2], Su-Tsai Lu[3], Jing-Ye Jung[3], [1]Feng Chia University, [2]National Tsing Hua University, [3]ITRI / Taiwan

FA4-2
Nanoscale Interfacial Frictional Behavior on Copper-Aluminum Intermetallic Compound
Hsiang-Chen Hsu, Li-Ming Chu, Jih-Hsin Chien, Chen-Yi Wang, Shen-Li Fu, Miin-Shyan Bair, I-Shou University / Taiwan

FA4-3
Characterization of Hot-spot Effect on a Chip Embedded with TSVs
Ra-Min Tain, Ming-Ji Dai, Li-Ling Liao, Chih-Sheng Lin, Shyh-Shyuan Sheu, Wei-Chung Lo, ITRI / Taiwan

FA4-4
Thermal Management for 3D-WLCSP Package
Jia-Shen Lan, Mei-Ling Wu, National Sun Yat-Sen University / Taiwan

Room B (1002)

FB1: Substrates and Interposers

FB1-1 <Session Invited>
Si Interposers with Integrated Passives for Power Integrity Application
Koichi Takemura, NEC / Japan

FB1-2
TSV Interposer Fabrication with 300 mm Wafer for 3D Packaging
Seiichi Yoshimi[1,2], Koji Fujimoto[1,2], Miyuki Akazawa[1,2], Hiroshi Mawatari[1], Hidenobu Matsumoto[1], Kousuke Suzuki[1], Toshihiro Itoh[2,3], Ryutaro Maeda[2,3], [1]Dai Nippon Printing, [2]NMEMS Technology Research Organization, [3]AIST / Japan

FB1-3
Integrated Meander Resistor in Printed Circuit Board Manufacturing
Rikard Qvarnstrom, Lulea University of Technology / Sweden

FB1-4
Via Formation Process to Form the Smooth Copper Wiring Using Adhesion Layer
Shinya Sasaki, Motoaki Tani, Fujitsu Laboratories / Japan

FB2: Biomimetics

FB2-1
Mechanisms and Models for Bio-Mimicry Design of Grip-and-Release Devices
Kunio Takahashi, Shigeki Saito, Pasomphone Hemthavy, Yu Sekiguchi, Tokyo Institute of Technology / Japan

FB2-2
Reversible Interconnection Leaning from Beetles
Naoe Hosoda, NIMS / Japan

FB2-3
Continuous Roll Imprinting of Moth-Eye Antireflection Surface Using Anodic Porous Alumina
Yoshihiro Uozu, Mitsubishi Rayon / Japan

FB2-4
Development of the Sirocco Fan Featuring the Dragonfly Wing Characteristics
Yui Kumon, Masaki Otsuka, SHARP / Japan

FB3: Medical Devices <Panel Session>

FB3-1
A Characteristic Evaluation of a Conductive Ink Wire Suited for Measuring the Biological Signal
Yasunori Tada[1], Masahiro Inoue[1], Tomohiro Tokumaru[2], [1]Gunma University, [2]Biosignal / Japan

FB3-2
Soft Contact-Lens Type Sensing Device for Tear Glucose Monitoring
Kohji Mitsubayashi, Tokyo Medical and Dental University / Japan

FB3-3
Implantable CMOS Devices for Biomedical Applications
Jun Ohta, Nara Institue of Science and Technology / Japan

FB3-4
Development of Medical Devices for Minimally Invasive Diagnosis and Therapy Using Micro/Nano Fabrication Technology
Yoichi Haga, Tohoku University / Japan

FB3-5
2D-realtime Analysis of Neuro-functions and Degenerations by an Ion Image Sensor-based Chemical Microscopy
Takashi Sakurai, Kazuaki Sawada, Toyohashi University of Technology / Japan

FB3-6
Wireless Body Area Communication Using Electromagnetic Resonance Coupling
Fukuro Koshiji[1,2], Nanako Yuyama[1], Kohji Koshiji[2], [1]Kokushikan University, [2]Tokyo University of Science / Japan

FB3-7
Development and Study of Electrical Property on Phantom for Human Body Communication Considering Tissue Structure of Human Arm
Dairoku Muramatsu[1], Fukuro Koshiji[2], Kohji Koshiji[3], Ken Sasaki[1], [1]The University of Tokyo, [2]Kokushikan University, [3]Tokyo University of Science / Japan

Panel discussion (approx. 50 min.)
There will be a break during the panel session.

Room C (1001)

FC1: Materials and Processes-2

(9：35)

FC1-1
Maskless Electroplating of Copper on Diamond-Like Carbon Films Modified by Scanning Probe Method
Shigehiro Hayashi, Woon Choi, Hajime Tomokage, Fukuoka University / Japan

FC1-2
High-Speed Bump Height Measurement System MB-3000 Based on Precise Stereoscopy
Kazuyoshi Suzuki, Toray Engineering / Japan

FC1-3
Warpage Behavior of Multi-tier Stacking in 2.5D/3D Package under Different Joining Process Conditions
Takashi Hisada, Kazushige Toriyama, Toyohiro Aoki, Yasuharu Yamada, IBM Japan / Japan

Break

FC2: Materials and Processes-3

FC2-1
Direct EP/EPAG - A Revolutionary Surface Finish for Electronic Packaging
Mustafa Oezkoek, Atotech Deutschland GmbH / Germany

FC2-2
Ag Nanoparticle Catalyst for Electroless Plating-Its Adsorption and Activation at Polymer Substrates
Yutaka Fujiwara, Yasuyuki Kobayashi, Shingo Ikeda, Osaka Municipal Technical Research Institute / Japan

FC2-3
Latest Additive of Acid Copper Plating for PWB, Designed for Higher Current Density
Toshimitsu Nagao, Yuuhei Kitahara, Shingo Nishiki, Okuno Chemical Industries / Japan

FC2-4
Adsorption Kinetic Study of Poly (ethylene glycol) During Copper Electrodeposition by a Microfluidic Device and an Electrochemical Quartz Crystal Microbalance
Yuichi Tsujimoto, Takeyasu Saito, Yutaka Miyamoto, Naoki Okamoto, Kazuo Kondo, Osaka Prefecture University / Japan

Lunch

FC3: Materials and Processes-3

FC3-1
Development of Epoxy/Mica Nanocomposites Formed Through Exfoliation of Mica Layer Treated by Different Types of Long-Chain Alkylamine.
Nobutake Tsuyuno[1,2], Shogo Nakai[1], Akira Irifune[1], Mitsukazu Ochi[1], [1]Kansai University, [2]Hitachi / Japan

FC3-2
Development of Encapsulated Resin Materials for Power Semiconductor Devices
Yuki Ishikawa, Kazuhiro Dohi, Kenichi Ueno, Tomoya Takao, Sanyu Rec / Japan

FC3-3
Adhesion Improvement of Epoxy Underfill to Polyimide Passivation Layers
Toshiyuki Sato, NAMICS / Japan

FC3-4
A Novel Halogen-Free and Reworkable Capillary Flow Underfill for Lead-Free Fine Pitch Area Array Package Applications
Hongbin Shi[1], Cuihua Tian[1], Michael Petch[2], Toshitsugu Ueda[1], [1]Waseda University / Japan, [2]University of Maryland / USA

FC3-5
Alkaline Developable Film Type Photoresist Material for Solder Paste Printing and Reflow Process
Daisuke Kanamori[1], Takuro Oda[1], Michiko Yamaguchi[1], Kazuyuki Matsumura[1], Toshihisa Nonaka[1], Yoshinori Miyamoto[2], Hajime Hirata[2], [1]Toray Industries, [2]Toray Engineering / Japan

Break

FC4: Interconnection-5

FC4-1
IMC Growth of Solder Capped Cu Pillar Bump Interconnection during Electromigration Test
Hirokazu Noma, Kazushige Toriyama, Sayuri Kohara, Keishi Okamoto, Yasumitsu Orii, IBM Japan / Japan

FC4-2
Interfacial Reaction Between Solder Filled TSV and Ti/Cu UBM
Young-Ki Ko[1,3], Myong-Suk Kang[1,2], Hiroyuki Kokawa[3], Yutaka S. Sato[3], Sehoon Yoo[1], Chang-Woo Lee[1], [1]Korea Institute of Industrial Technology, [2]University of Science and Technology / Korea, [3]Tohoku University / Japan

FC4-3
Crack Formation and Propagation Mechanisms in Interfacial Cu_6Sn_5
Kazuhiro Nogita[1], Dekui Mu[1], Stuart D. McDonald[1], Jonathan Read[1], Keith Sweatman[1,2], [1]The University of Queensland / Australia, [2]Nihon Superior / Japan

FC4-4
Effects of the Morphology of Ni-P Films on Black Pad Formation After the ENIG (Electroless Nickel Immersion Gold) Process
Kyoungdoc Kim, Jin Yu, Korea Advanced Institute of Science and Technology / Korea

Room D (1004)

FD1: RF-1

FD1-1
A 36 W 240 kHz Wireless Power Transfer System with a 82% Efficiency for LED Lighting Applications
Wei-Ting Chen[1], Raul A. Chinga[2], Shuhei Yoshida[3], Jenshan Lin[2], Chao-Kai Hsu[1], [1]ITRI / Taiwan, [2]University of Florida / USA, [3]NEC / Japan

FD1-2
Novel System Design for Both Wireless Power Supply and Communication Through Two-Dimensional Wave-Guiding Sheet
Keishi Kosaka, Hiroshi Fukuda, Koichiro Nakase, Naoki Kobayashi, Akira Miyata, Toshinobu Ogatsu, NEC / Japan

FD1-3
Radiation Noise Reduction Technique from Power Supply Layers in PCB using Resistors
Hitoshi Takakura, Shinichi Sasaki, Saga university / Japan

FD1-4
Reduction Technique for Power Supply Noise of Analog-Digital Mixed Circuit Boards -Adjustment of Attached Resistor Method-
Shunsuke Baba, Saga University / Japan

FD2: RF-2

FD2-1
A UWB Antenna Built into 3G Smart Phone
Yusuke Akiyama[1], Fukuro Koshiji[1,2], Kohji Koshiji[1,2], [1]Kokushikan University, [2]Tokyo University of Science / Japan

FD2-2
A Study on EM Radiation from Shielded-Flexible Flat Cable for Interconnection
Yoshiki Kayano, Ryo Uesugi, Hiroshi Inoue, Akita University / Japan

FD2-3
Electromagnetic Simulation of Printed Circuit Board inside Chassis Using Equivalent Model Focusing on Common-mode
Yuli Wakaduki[1], Yoshitaka Toyota[1], Kengo Iokibe[1], Ryuji Koga[1], Tetsushi Watanabe[2], [1]Okayama University, [2]Industrial Technology Center of Okayama Prefecture / Japan

FD2-4
Mold-based Compartment Shielding Investigation for SiP Modules
Kuo-Hsien Liao, ASE / Taiwan

FD3: Thermal Management-3

FD3-1
Direct Liquid Immersion Cooling of Power LEDs by an Injection Molded Substrate with Fluidic Features
Thomas Leneke, S. Hirsch, B. Schmidt, Otto-von-Guericke-University / Germany

FD3-2
Heat Management Solutions for Advanced Packaging
Randeep Singh, Masataka Mochizuki, Mohammad Shahed Ahamed, Yuji Saito, Koichi Mashiko, Fujikura / Japan

FD3-3
Single-Phase and Two-Phase Flow Heat Transfer Performances of Minichannel Finned Heat Sinks
Kazuhisa Yuki, Koichi Suzuki, Tokyo University of Science, Yamaguchi / Japan

FD3-4
Thermal Management of Dust-Proof ICT Systems
Hitoshi Sakamoto, Akira Shojiguchi, Masaki Chiba, Minoru Yoshikawa, NEC / Japan

FD3-5
Energy-Efficient Technology for Data Centers Using Phase Change Cooling Units
Arihiro Matsunaga, NEC / Japan

Break

FD4: Thermal Management-4

FD4-1
Thermal Conductivity and Evaluation of Various Types of Polymer Composites with filler
Yasuyuki Agari, Hiroshi Hirano, Joji Kadota, Akinori Okada, Osaka Municipal Technical Research Institute / Japan

FD4-2
Experimental Verification of the Relationship Between Isothermal Surface and Structure Function
Yafei Luo[1], Masaru Ishizuka[2], Tomoyuki Hatakeyama[2], [1]Mentor Graphics, [2]Toyama Prefectural University / Japan

FD4-3
Flow and Thermal Resistance Network Analysis of Fan Cooled Thin Enclosure
Takashi Fukue[1], Tomoyuki Hatakeyama[2], Masaru Ishizuka[2], Koichi Horose[1], Katsuhiro Koizumi[3], [1]Iwate University, [2]Toyama Prefectural University, [3]Cosel / Japan
(17:00)

Room E (1005)

FE1: DMR-Mechanical-2

(9：35)

FE1-1
Evolution of Microstructure of SAC305 and SN100C Solders on ENIG/Cu Pads under Isothermal Aging
Mei-Ling Wu[1], Preeti Chauhan[2], Michael Osterman[2], Michael Pecht[2], [1]National Sun Yat-Sen University / Taiwan, [2]University of Maryland, / USA

FE1-2
Ultra-Accelerated Quantum Chemical Molecular Dynamics Simulation of Atomic Level Stability of Solder Materials
Nozomu Hatakeyama[1], Ryuji Miura[1], Ai Suzuki[1], Kunio Shiokawa[2], Mitsuo Yamashita[2], Akira Miyamoto[1], [1]Tohoku University, [2]Fuji Electric / Japan

FE1-3
A New Reference Area for Indentation Creep Tests to Obtain Real Steady Creep Strain of Solder Alloy
Atsuko Takita[1], Katsuhiko Sasaki[1], Ken-ichi Ohguchi[2], [1]Hokkaido University, [2]Akita University / Japan

FE2: DMR-Mechanical-3

FE2-1
Multiscale Modeling of Anisotropic Creep Response of Heterogeneous Single Crystal SnAgCu Solder
S.Mukherjee[1], B. Zhou[2], T. Bieler[2], A.Dasgupta[1], [1]University of Maryland, [2]Michigan State University / USA

FE2-2
Board Level Reliability and Assembly Process of Advanced Fine Pitch QFN Packages
Li Li[1], Brian Smith[2], Joe Smetana[3], David Geiger[4], Chris Katzko[5], Jeffrey ChangBing Lee[6], Richard Coyle[3], Alex Chan[3], [1]Cisco Systems, [2]HDP User Group International, [3]Alcatel-Lucent, [4]Flextronics / USA, [5]TTM Technologies / China, [6]IST-Integrated Service Technology / Taiwan

FE2-3
Bonding Properties between Cu Wire and Al Pad in Microelectronics Packaging after Stress Test
Yuji Ishida, Akihiro Shinomiya, Takayuki Akaboshi, Nobuhiko Ota, Shinji Yamashita, Yaskawa Electric / Japan

FE2-4
Accelerated Failure of Microjoints Caused by the Thermal Expansion of Underfill Material within a Chip Stacking Architecture
Jing-Yao Chang[1,2], Shin-Yi Huang[1], Tao-Chih Chang[1], Tung-Han Chuang[2], [1]ITRI, [2]National Taiwan University / Taiwan

FE3: Power Devices

FE3-1
Electrical Characteristics and Reliability Performance of IGBT Power Module by Chip Embedding Technology
Yin-Po Hung, Sheng-Che Hung, Ren-Shin Cheng, Fang-Jun Leu, Jing-Ye Juang, Shang-Wei Chen, Chao-Kai Hsu, and Tao-Chih Chang, ITRI / Taiwan

FE3-2
Interfacial Properties of IGBT Module with IBP Bonding in Electronic Vehicles
A Young Kim[1], Won Sik Hong[1], Sung Min Park[2], Young Pyong Kim[2], Dong-Keun Jang[2], Yong-Mo Kim[3], [1]Korea Electronics Technology Institute, [2]LS Industrial Systems, [3]Korea Instrument / Korea

FE3-3
The Solder Creep Behavior of Power Module subject to Temperature Cycling Test with Different Temperature Profiles
Hsiang-Chun Huang[1,2], Tuan- Yu Hunga[1,2], Chin-Chun Wang[4], Keng-Cheng Lu[4], Kuo-Ning Chiang[1,2,3], [1]Advanced Microsystem Packaging and Nano-Mechanics Research Lab, [2]National Tsing Hua University, [3]National Applied Research Laboratories, [4]DELTA Electronics / Taiwan

FE3-4
Transfer Molding Compounds for Power Electronic Applications -A Qualification Methodology for HT Capable Materials-
T. Braun[1], K.-F. Becker[1], M. Koch[1], T. Thomas[2], T. Schreier-Alt[1], V. Bader[1], J. Bauer[1], T. Nowak[1], O. Bochow-Ness[2], R. Aschenbrenner[1], M. Schneider-Ramelow[1], K.-D. Lang[2], [1]Fraunhofer Institute for Reliability and Microintegration, [2]Technical University Berlin / Germany

FE3-5
Failure Mode Analysis of Electrical Double Layer Capacitors
Masaki Moriyama[1,2], Michael H. Azarian[1], Michael Pecht[1], [1]University of Maryland / USA, [2]Kyoto University / Japan

*DMR: Design, Modeling and Reliability

■Keynote Speeches

From Deep Trenches to Skyscrapers – Orthogonal Scaling

Subramanian S. Iyer, PhD
IBM Fellow
International Business Machines Corp.

The absence of cost effective lithography and patterning schemes is predicted to make the historical expectations of the cost –performance benefits of scaling (popularly known as Moore's Law) difficult to sustain. In this talk we introduce the concept of orthogonal scaling. Orthogonal scaling refers to features that can be added to the technology which significantly enhance the technology and which are sustainable over several generations of technology. We will examine three such orthogonal features that have either been implemented or being actively worked on. The first is embedded memory, where the integration of logic based embedded DRAMs can effectively yield up to a generational jump in effective density. The second case we consider is the use of deep trench decoupling that can reduce mid-frequency power supply noise in processor and general purpose ASICs effectively adding up to10% in chip performance above the scaling entitlement and finally, three dimensional integration which depending on its implementation can address die size, performance, process simplicity and cost beyond the expectation of semiconductor scaling. We summarize this talk with where the fundamental limits are and what our long-term options are for the evolution of a systems' based scaling methodology.

■Biography

Subramanian S. Iyer is an IBM Fellow at the Systems & Technology Group, and is responsible for technology strategy and competitiveness, embedded memory and Three-Dimensional Integration.He obtained his B.Tech in Electrical Engineering at the Indian Institute of Technology, Bombay, and his M.S. and Ph.D. in Electrical Engineering at the University of California at Los Angeles. He joined the IBM T. J. Watson Research Center in 1981 and was manager of the Exploratory Structures and Devices Group till 1994, when he co-founded SiBond LLC to develop and manufacture Silicon-on-insulator materials. He has been with the IBM Microelectronics Division since 1997. Dr. Iyer has received two Corporate awards and four Outstanding Technical Achievement awards at IBM for the development of the Titanium Salicide process, the fabrication of the first SiGe Heterojunction Bipolar Transistor, the development of embedded DRAM technology and the development of eFUSE technology. His current technical interests and work lie in the area of 3-dimensional integration for memory sub-systems and the semiconductor roadmap. He is a Master Inventor. He received the Distingushed Aluminus award from the Indian Institute of Technology, Bombay in 2004. Dr. Iyer has authored over 175 articles in technical journals and several book chapters and co-edited a book on bonded SOI. He has served as an Adjunct Professor of Electrical Engineering at Columbia University, NY. He was honored as the Asian Engineer of the Year in 2011. He is the recepient of the 2012 IEEE Daniel Nobel award for emerging techologies In his spare time, he studies Sanskrit and role of Indic languages, traditions and culture in different parts of the world.

R&D Strategy to Become No.1 Green Innovation Company

Takeshi Uenoyama, PhD
Executive Officer
Panasonic Corp.

Looking towards 2018, the 100th anniversary of our founding, Panasonic is working under a grand vision of becoming No.1 Green Innovation Company with the concept of "Eco & Smart" solutions; aiming to integrate our business growth into environmental contribution . We are considering 4 categories to serve our customer needs: "residential space," "non-residential space," including offices, factories, and stores/facilities, "mobility space," including cars and airplanes, and "personal space." In order to achieve our goal, we established 4 companies deeply linked to 4 categories above on April 1st 2013: "Appliances Company", "Eco Solutions Company", "AVC Networks Company" and "Automotive & Industrial Company". Today I would like to describe briefly about our new mid-term business plan and our R&D strategy. I would like to explain our Cloud/ Energy/ Device solutions, the 3 important fields we consider in our R&D.

■Biography

Takeshi Uenoyama was born in Wakayama, Japan in 1956. He received the MS degree from Osaka University in 1981, the PhD from University of California, San Diego in 1990, respectively. He joined Matsushita Electric in 1981 and started his careers in the fields of semiconductors, display devices and environmental technologies. Subsequently he has held several management positions: as from 2004: director of Advanced Technology Research Laboratories, Nanotechnology Research Laboratory, and Image Devices Development Center; as from 2006: executive senior councilor of Corporate R&D Center. In April 2008, he promoted to Executive Officer of Panasonic Corporation.

Since March 2012, he has assumed the position of vice president of The Electrochemical Society of Japan.

Architecture Trends in Mobile Industry and Impact on Packaging and Integration

Urmi Ray, PhD
Program Manager
Qualcomm Inc.

The last decade has seen an exponential growth in the mobile phone and computing industry. The emergence of smartphones and the ever growing demand of packing more and more features and functionality by the consumers has rapidly driven innovations in advanced packaging and integration. Smart integration at reasonable cost is a key to driving advanced functionality to mass market quickly.

This talk will provide an overview of the latest trends in the mobile and wireless industries, with examples of architectural platforms, several disruptive technology platforms as well as evolutionary trends towards integration and miniaturization. Key focus of this presentation will be on emerging technologies, such as 2.5D TSV interposers and 3D IC integration. The applications of 3D IC integration include CMOS image sensor, MEMS, LED, memory + logic, logic + logic, memory + microproces¬sor. For 2.5D, active and passive interposers using Si and glass will be covered.

Technology development challenges include tools, materials, infrastructure, reliability and many more. Several key challenges must be overcome before these integrations can be realized. In addition to lowering cost, increasingly complex tradeoffs, such as architectural partitioning, cost-performance-thermal, Chip-Package Interaction (CPI) must be managed. Electrical noise coupling, thermal interaction, and mechanical stress effects require multiphysics simulation and an infrastructure to support design for X across multiple domains. Tools, models, methodologies, materials, structural constructs, and experimental results are needed to ensure quality, yield and reliability.

Current R&D and industry status will be presented, including technical, cost, business, standards and other factors important for rapid technology adoption.

■Biography

Urmi Ray is currently the technical program manager for Qualcomm's Through Silicon Stacking (TSS) program and is also leading a program on low cost interposer technology. She joined Qualcomm in 2006, after spending 10+ years at Lucent Technologies Bell Laboratories in NJ working on advanced materials and reliability for a diverse set of product portfolios, including consumer products to high reliability telecommunications projects. She is currently active in the 3D technology area. She has a PhD from Columbia University (New York City).

■Poster Session

P01 Through Silicon Vias Design Using the Scattering Matrix
You-Yi Chen, Mei-Ling Wu, National Sun Yat-Sen University / Taiwan

P02 Thermo-Mechanical Stress of Underfilled 3D IC Packaging
Ming-Han Wang, Mei-Ling Wu, National Sun Yat-Sen University / Taiwan

P03 Study of Microstructure Evolution in Nanoscale-Thickness Cu/Sn/Cu and Cu-Sn/Zn-Cu Sandwich Structure for 3D Packaging
Qingqian Li, Y. C. Chan, City University of Hong Kong, / Hong Kong

P04 Cu/Ni/SnAg Microbump Bonding Processes for 30μm Pitch Thin-Chip-on-Chip Package Using a Wafer-Level Underfill Film
Chang-Chun Lee, Tzai-Liang Tzeng, Chung Yuan Christian University / Taiwan

P05 Using Electromagnetic Band-gap Structure to Eliminate Frequency Multiplication Noise and Implement 3D Band-pass Filter on Testing Load Board
Yu-Chi Kuo, Sung-Mao Wu, National University of Kaohsiung / Taiwan

P06 Halogen-Free Substrate Materials with High Thermal-Resistant and High Thermal Conductivity
Kuo-Chan Chiou, Feng-Po Tseng, Lu-Shih Liao, Kuei-yi Chuang, ITRI / Taiwan

P07 Analysis of the Temperature Effect on the Liquid Bridge Behavior between Fixed Plates for the Heat Switch System
Su-Heon Jeong[1], Wataru Nakayama[2], Sung-Ki Nam[1], Sun-Kyu Lee[1], [1]Gwangju Institute of Science and Technology, [2]ThermTech International / Korea

P08 Surface Modification of Polyimide Films by the Remote Plasma for Enhance the Adhesion Strength with Epoxy Molding Compounds
Chih-Feng Wang[1], Jian-Yi Wu[1], Yi-Shao Lai[2], Ping-Feng Yang[2], [1]I-Shou University, [2]ASE / Taiwan

P09 Developing a Lignin-based Resin for FCCL
Wei-Ta Yang, Li-Ming Chang, ITRI / Taiwan

P10 The Study of Angular Color Uniformity in Various Package Structure and Lens Geometry of White LED Package
Syue-Fong Hu, Chien-Lin Chang Chien, Chang-Wen Sun, Chung-Min Chang, Chih-Peng Hsu, Advanced Optoelectronic Technology / Taiwan

P11 Development of Space Free LED Module for the Improvement of Brightness and the Light Uniformity of Light Guide Element
Ming-Ta Tsai[1,2], Syue-Fong Hu[1], Chien-Lin Chang Chien[1], Chung-Min Chang[1], Chih-Peng Hsu[1], Wei-I Lee[2], [1]Advanced Optoelectronic Technology, [2]National Chiao Tung University / Taiwan

P12 A CMOS Inverter Detector for Package High-Speed Characteristics Testing
Yuan-Ming Wu, Ping-Lin Chang, Jain-Kai Fang, Sung-Mao Wu, National University of Kaohsiung / Taiwan

P13 Simplified VRM Modeling Proposal for Signal and Power Integrity Analysis
Mitsuharu Umekawa, Agilent Technologies Japan / Japan

P14 A Fault Detection Methodology for a Multipoint-Differential Cabling System
Takashi Kuwahara[1], Tsuyoshi Kobayashi[1], Hiroyuki Joba[1], Yoshihiro Akeboshi[1], Seiichi Saito[2], [1]Mitsubishi Electric, [2]Salesian Polytechnic / Japan

P15 Using for Three-dimensional Broadband Double-side Direct Thru Kit with Non-exchange Layer Design and Analysis
Wen-Yi Ruan, Ting-Han Chien, Lung-Shu Huang, Sung-Mao Wu, National University of Kaohsiung / Taiwan

P16 A Proposal of New Electrode Structure for Intra-Body Communication
Takaaki Fujisawa[1], Fukuro Koshiji[1,2], Kohji Koshiji[2], [1]Kokushikan University, [2]Tokyo University of Science / Japan

P17 Fabrication of PTFE Micro Fluidic Chip for Amino Acid Derivatization Process
Hideki Kido[1], Ikuo Okada[2], Yuichi Utsumi[1], Hajime Mita[3], [1]University of Hyogo, [2]Nagoya University, [3]Fukuoka Institute of Technology / Japan

P18 Microfluidic Devices with SERS Active Three-dimensional Gold Nanostructure
Ryo Takahashi, T.Fukuoka, Y.Utsumi, University of Hyogo / Japan

P19 Three-dimensional Silver Nanostructure for Surface Enhanced Raman Scattering
Ryohei Hara, R.Takahashi, T.Fukuoka, Y.Utsumi, University of Hyogo / Japan

P20 Proposal of a Novel Internally-Triggered Automatic Flow Sequencing on Centrifugal Microfluidics
Masaki Ishizawa[1], H. Nose[1], Y. Ukita[2], and Y. Utsumi[1], [1]University of Hyogo, [2]Japan Advanced Institute of Science and Technology / Japan

■Registration

The online registration system on the ICEP web site (http://www.jiep.or.jp/icep/) will be available through March 31.
Please come to the on-site registration desk after April 1.

Registration Fees

Member of JIEP / IEEE / IMAPS (Including Company Member of JIEP)	¥40,000	[¥47,000]	Including Reception and Proceedings
Member of Partner Organization	¥40,000	[¥47,000]	Including Reception and Proceedings
Non-Member	¥50,000	[¥57,000]	Including Reception and Proceedings
Student	¥7,000	[¥7,000]	Including Proceedings
Speaker	¥40,000		Including Reception and Proceedings
Student speaker	¥7,000		Including Proceedings
Welcome Reception Only	¥10,000		[ ] At door

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