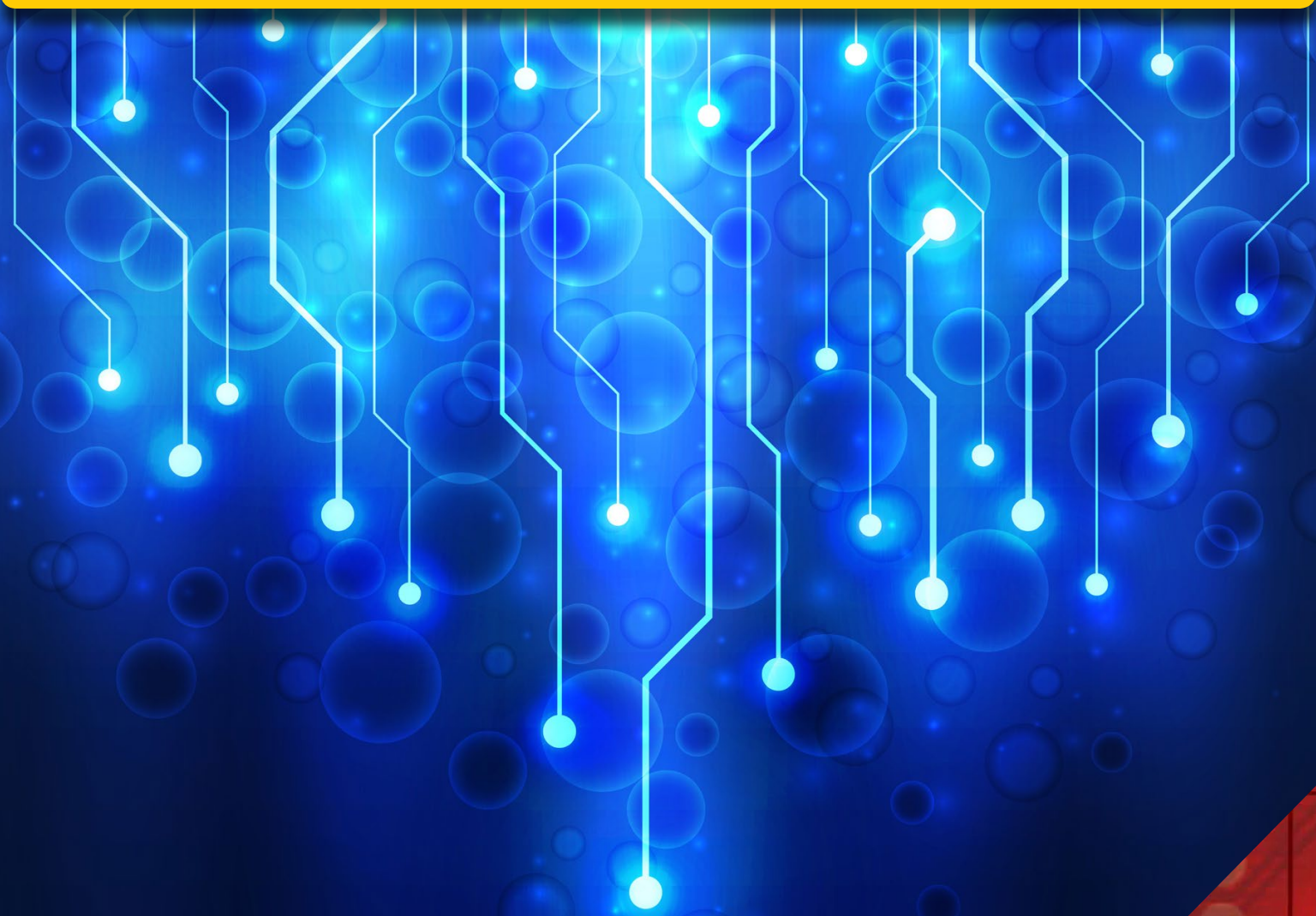
THE pcb design MAGAZINE

March 2015

an I-Connect007 publication

DESIGN FOR MANUFACTURING



Understanding DFM and Its Role in PCB Layout

by Rick Almeida, page 10

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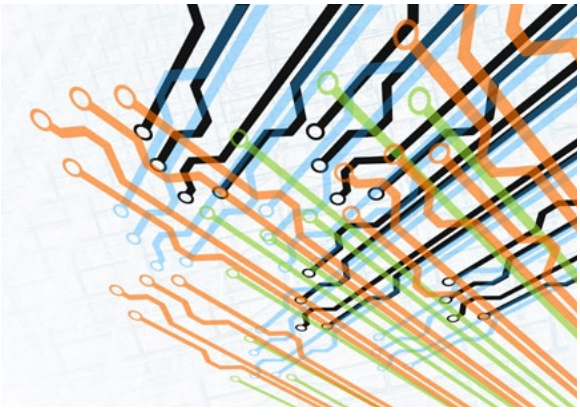
THE pcb design MAGAZINE
March 2015

This Issue: DESIGN FOR MANUFACTURING

FEATURED CONTENT

As the speed of electronic devices continues to increase, so does the cost of re-spins, making good DFM practices more important than ever. Catching problems at the design stage can save weeks of wasted time, not to mention thousands of dollars. This month, we focus on design for manufacturability techniques and processes, with articles from our contributors Rick Almeida, Tim Haag, and Martin Cotton.



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* Dk & Df are dependent on resin content NOTE: Dk/Df is at one resin %. Please refer to the Isola website for a complete list of Dk/Df values. The data, while believed to be accurate & based on analytical methods considered to be reliable, is for information purposes only. Any sales of these products will be governed by the terms & conditions of the agreement under which they are sold.

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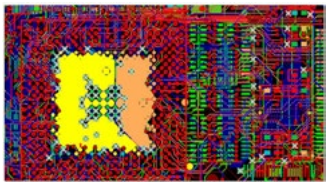

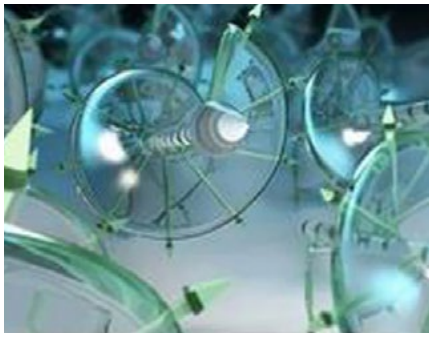

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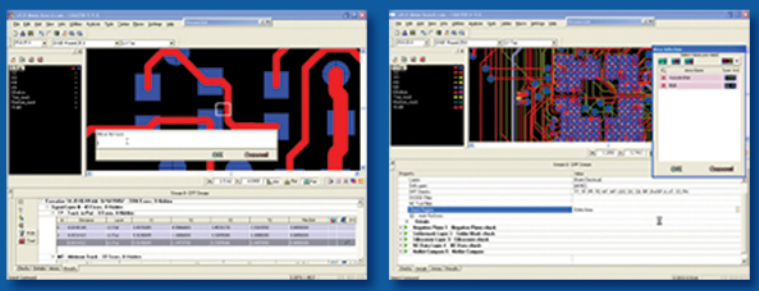

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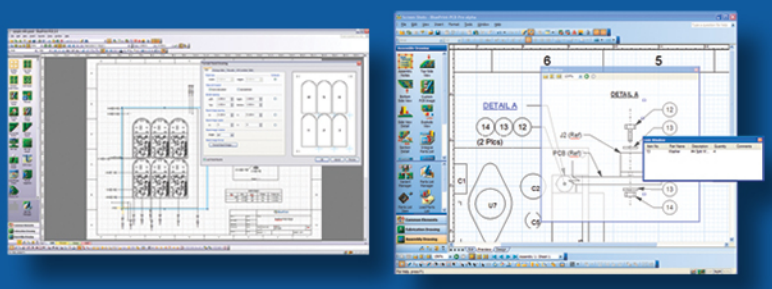

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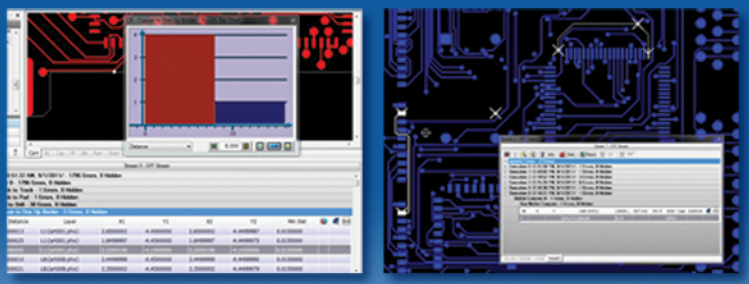

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Good Vibes at IPC APEX EXPO 2015

by Andy Shaughnessy
I-CONNECT007

IPC APEX EXPO has come and gone, and I'm still exhausted. Of course, I caught the creeping crud and lost my voice at the show. I'm used to being one of the louder people in the room, but for almost a week, all I could do was whisper.

I wonder if I caught a bug from someone on the plane. Half the passengers on the plane were coughing and sneezing for the whole four-and-a-half-hour flight. I think that flight attendants should force you to wear a mask if you cough or sneeze more than one time on a flight. I'm surprised we don't get sick every time we fly.

Still, if you're going to be under the weather, there are a lot worse places to be than San Diego. It's just tough to have a bad time there.

Before the show kicked off, Guest Editor Kelly Dack and I went in search of sushi in the Gaslamp District. I love the way restaurants in the Gaslamp post their menus outside; some sushi restaurants were asking $25 per roll. But we found the perfect sushi place, and it was in the middle of happy hour, so we got an ocean full of sushi for not very much money.

Kelly is not just a PCB designer and guest editor; he recently branched out and became an IPC Certified Interconnect Designer (CID) instructor with EPTAC. He spent days teaching the CID curriculum, and almost everyone in the class passed the certification exam, so I guess Kelly knows what he's talking about. Soon we'll see him hanging out in the teachers' lounge in a blazer with elbow patches!

On Monday, the Design Forum crowd nearly filled the room. Carl Schattke, a PCB design engineer with Tesla Motors, gave the keynote speech. He was followed by Rainer Taube of Taube Electronic GmbH and FED discussing IPC-7070 component mounting issues, and

Tom Hausherr of PCB Libraries focusing on IPC-7351C requirements for surface mount design and land pattern standard. After lunch, Stephen V. Chavez of UTC Aerospace Systems discussed communication with cross-cultural teams, and Rick Hartley covered succeeding through controlling cost and quality.

But conspicuous in his absence was Dieter Bergman. This marks the first Design Forum since Dieter's death last year, and he always kicked off the event. A tribute to Dieter was held on Wednesday night, with attendees swapping their favorite stories about Dieter.

IPC announced the recipients of the First Annual Dieter Bergman IPC Fellowship Award: Don Dupriest of Lockheed Martin, Denny Fritz of SAIC, Dave Hillman of Rockwell Collins, Bernie Kessler of Bernard Kessler & Associates, Bob Neves of Microtek Laboratories, Ray Prasad of Ray Prasad Consultancy Group, Randy Reed of Viasystems, and Doug Sober of Shengyi Technology. All recipients are longtime IPC members who have shown ongoing leadership.

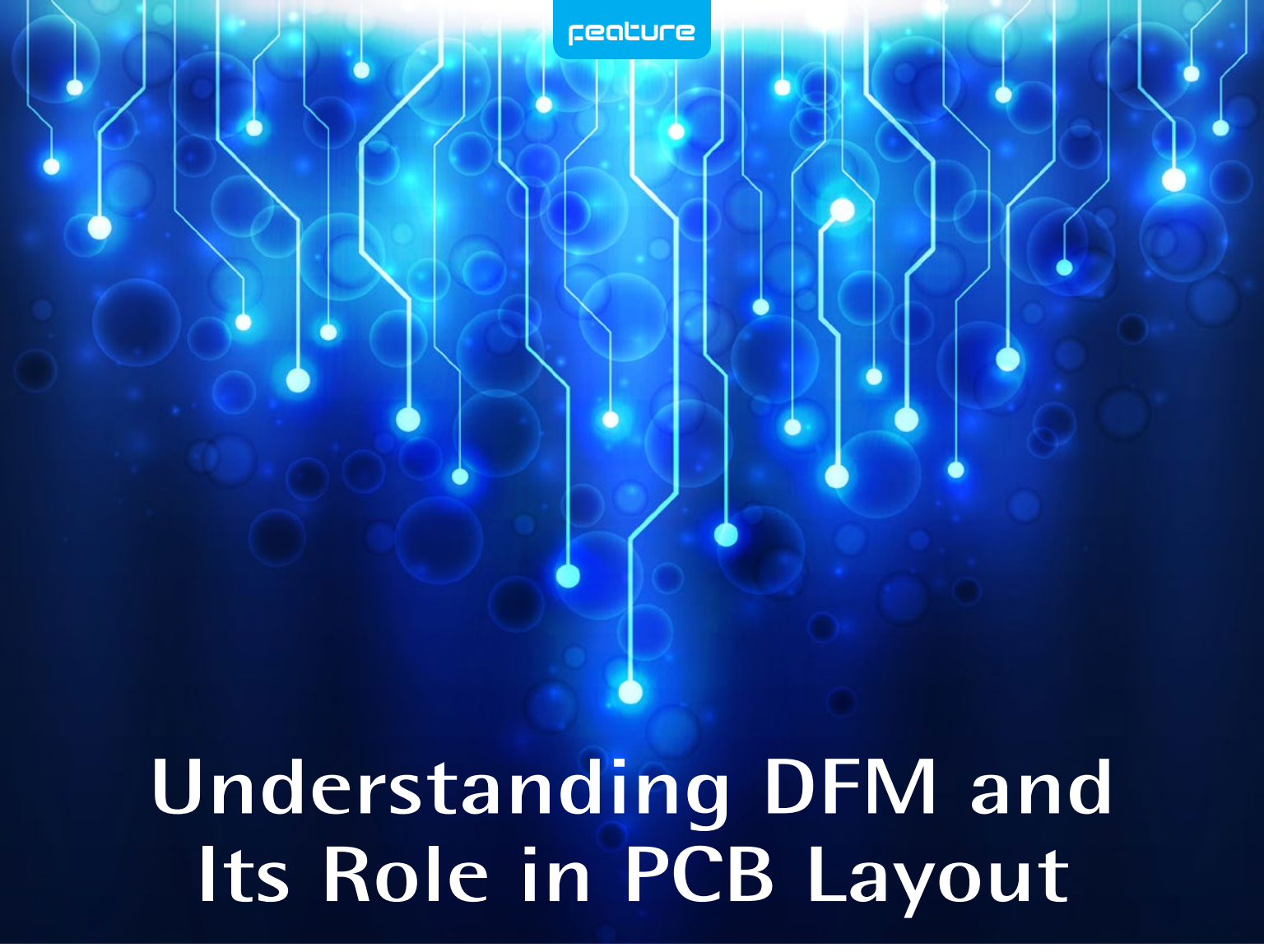
I also have to mention Gary Ferrari of FTG Corporation and Nilesh Naik, president of Eagle Circuits, for taking home the Raymond E. Pritchard Hall of Fame Award. Gary is the co-founder of the IPC Designers Council, creator of the CID courses, and a veteran PCB design instructor, just to name a few highlights. Nilesh Naik was active in the Designers Council nationally and regionally, and he has served as chairman of the PCB/IMS Presidents Management Council. He is a member of the Government Relations Steering Committee and was re-elected to the IPC Board of Directors. Let's give these guys a round of applause for being awarded the highest level of recognition that IPC can grant to an individual.

On the show floor, I found the mood to be more upbeat than last year; some companies are hiring right now, and there was no undercurrent of negativity that I've sensed at previous shows (for instance, at APEX two years ago, during the sequestration battle on Capitol Hill). Nearly every company seems to be growing steadily, if not in leaps and bounds. It's just a gut feeling, and not very scientific, but it feels like this is a good time to be in this industry.

Next year, IPC APEX EXPO returns to Las Vegas, but this time it's in the Las Vegas Convention Center, away from the Strip. That sounds like a good plan to me. I've had enough of Mandalay Bay for a while.

As the show season rolls along, look for our complete coverage of the CPCA Show in Shanghai in March 17-19. If you can't make it, don't worry. We'll be there. **PCBDESIGN**

Andy Shaughnessy is managing editor of *The PCB Design Magazine.* He has been covering PCB design for 15 years. He can be reached by clicking here.



Understanding DFM and Its Role in PCB Layout

by Rick Almeida
DOWNSTREAM TECHNOLOGIES

DFM, DRC, DFF, DFA, DFwhat? These are all terms used daily in the PCB design world regarding manufacturing analysis, and they are often used interchangeably. But what exactly is DFM and why is it such an important, but often ignored aspect of the PCB design process?

Let's start by clarifying some terms. DFM is short for "design for manufacturability." It is the process of arranging a PCB layout topology to mitigate problems that could be encountered during the PCB fabrication and assembly processes required to manufacture an electronic system. Addressing fabrication issues is what's known as design for fabrication (DFF), and addressing assembly issues during design is known as design for assembly (DFA). The two together mostly make up DFM analysis—mostly.

In many cases, the term DRC, which stands for design rule checking, is also used interchangeably with DFM and creates further confusion. That's understandable, because DRC issues detected in manufacturing can indeed have a direct impact on the manufacturability of a PCB. However, DRC is markedly different from DFF and DFA. Think of DRC as a hard pass/fail detection of a problem in a PCB. Either a problem exists or it doesn't. In engineering, DRC is used to ensure that PCB layout connectivity accurately reflects the connectivity defined in a board's associated schematic diagram. But connectivity is only one aspect of DRC. The "R" stands for rules. The rules are used largely to define the minimum spacing allowed between various PCB objects for the entire PCB or for individual layers, nets or areas on the PCB. In engineering, the spacing may have direct impact on circuit performance. In manufacturing, spacing may play a pivotal role in the ability to fabricate or assemble a PCB.

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As a result, DRC becomes a subset of DFM, but only if the rules used reflect a manufacturer's requirements for spacing. Otherwise, DRC is used solely for electrical verification.

DFM's two primary components, DFF and DFA, are more nuanced than DRC. While DRC detects very specific discrepancies from the intended interconnect, DFM identifies issues in the PCB topology that have the potential to create manufacturing problems. What's more, a DRC defect will be present in every copy of the PCB built, so if there is a short missed in DRC, every PCB will contain the short, no matter how many PCBs are produced. By contrast, if the same PCB quantities contain DFM issues, problems may only manifest in some of the PCBs while others perform correctly as expected. For example, a PCB layout containing very thin pieces of copper created in the design tool by rule would be correct per the schematic. And if spaced properly it would pass DRC. However, that same sliver, being so thin, could potentially detach on the physical PCB and inadvertently connect itself to other copper elements during assembly, thus creating shorts on some PCBs but not on others. So, the sliver would pass DRC verification, but in real-world manufacturing the sliver could cause some PCBs to fail. Without DFM, this problem would go on undetected and would result in scrap or rework.

Until recently, DFM analysis was either left to the PCB fabricator or assembly engineer to manage, or it was performed by companies that had the financial resources to purchase high-end DFM analysis software and support a dedicated staff to run DFM analysis. Most PCB designers would perform only a DRC analysis and visual inspection of the design before submitting the design to be manufactured. Manufacturers know that DFM issues such as acid traps, slivers and starved thermal pad connections can decrease manufacturing yields and increase costs, and they take it upon themselves to analyze the design, often making modifications to ensure that the design can be built with maximum yields and lowest costs. So long as the finished PCB functioned properly, the design engineer was content.

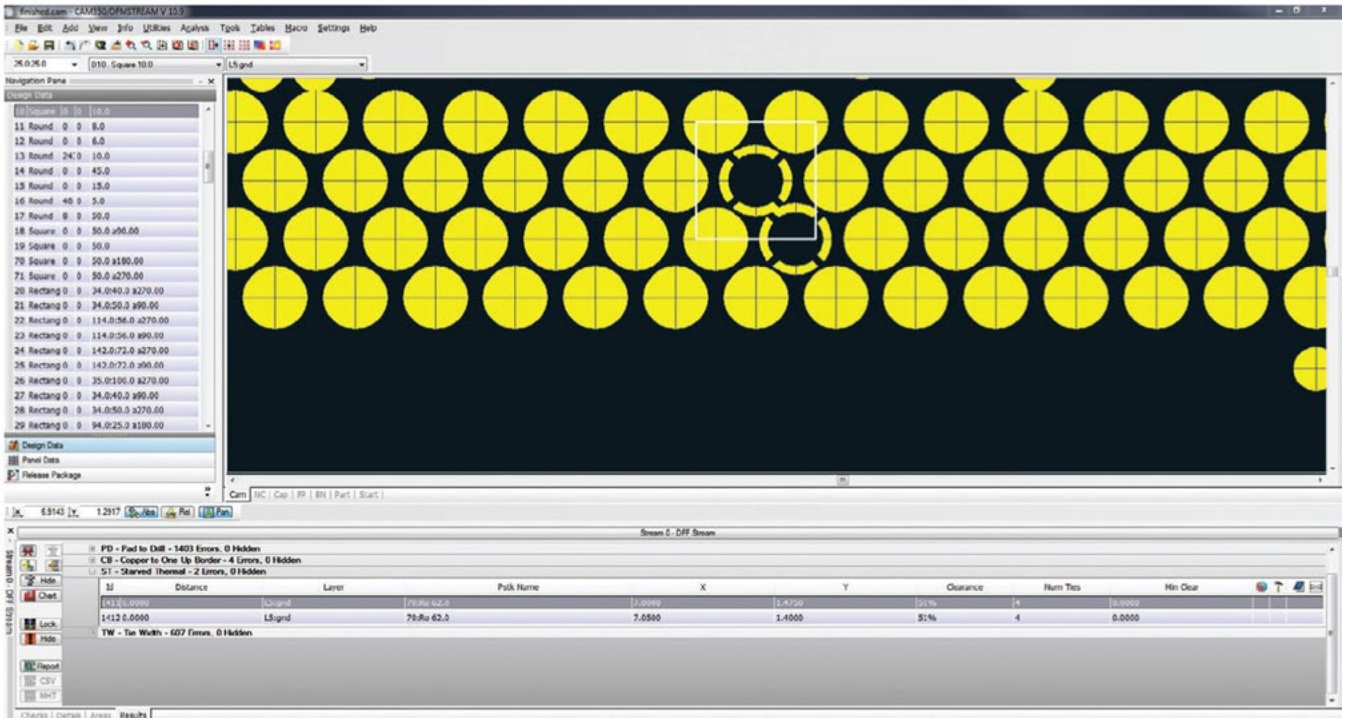
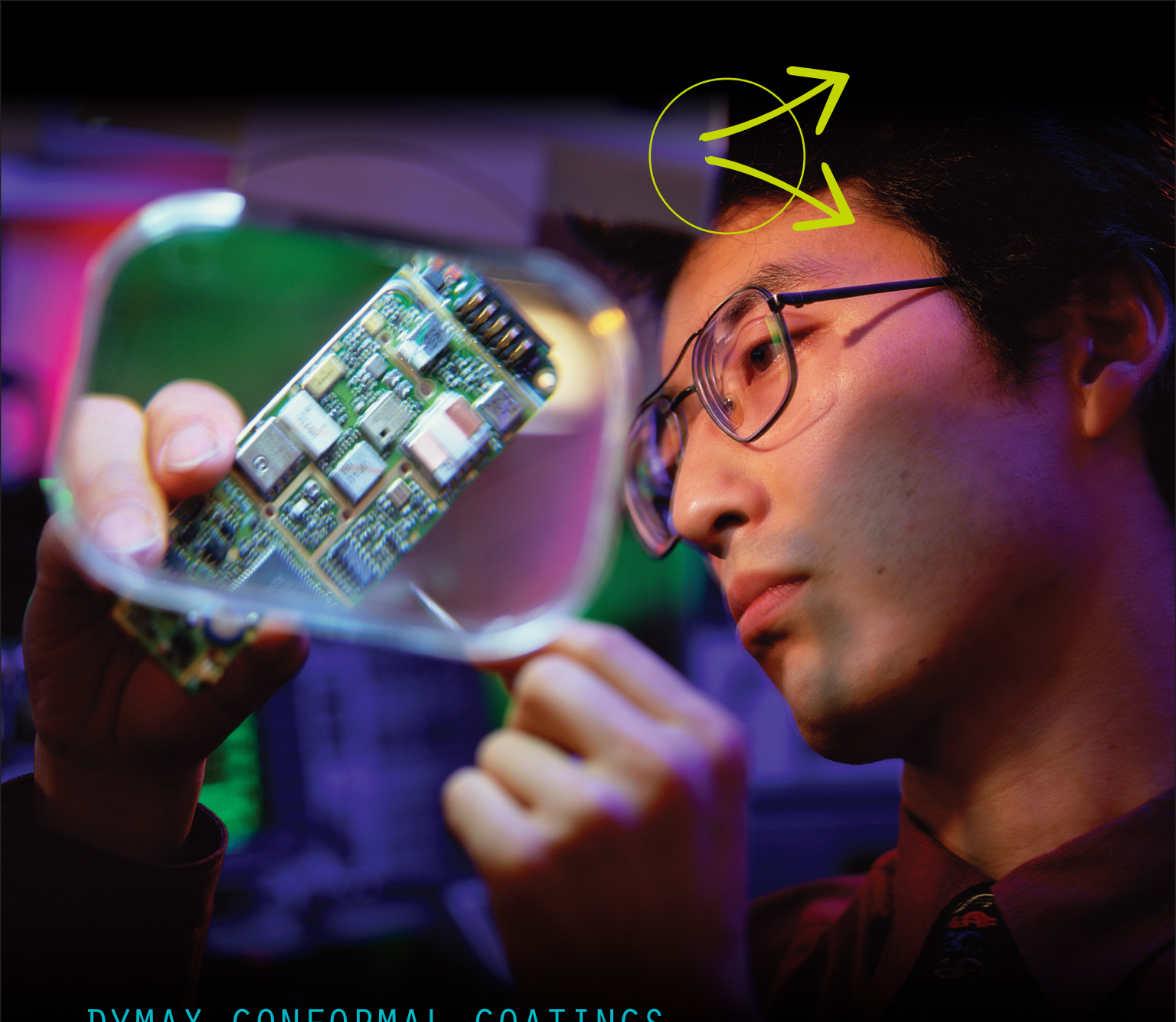


Figure 1: These starved thermals pass electrical DRC, but in reality the connection to the actual source is insufficient for a good connection.



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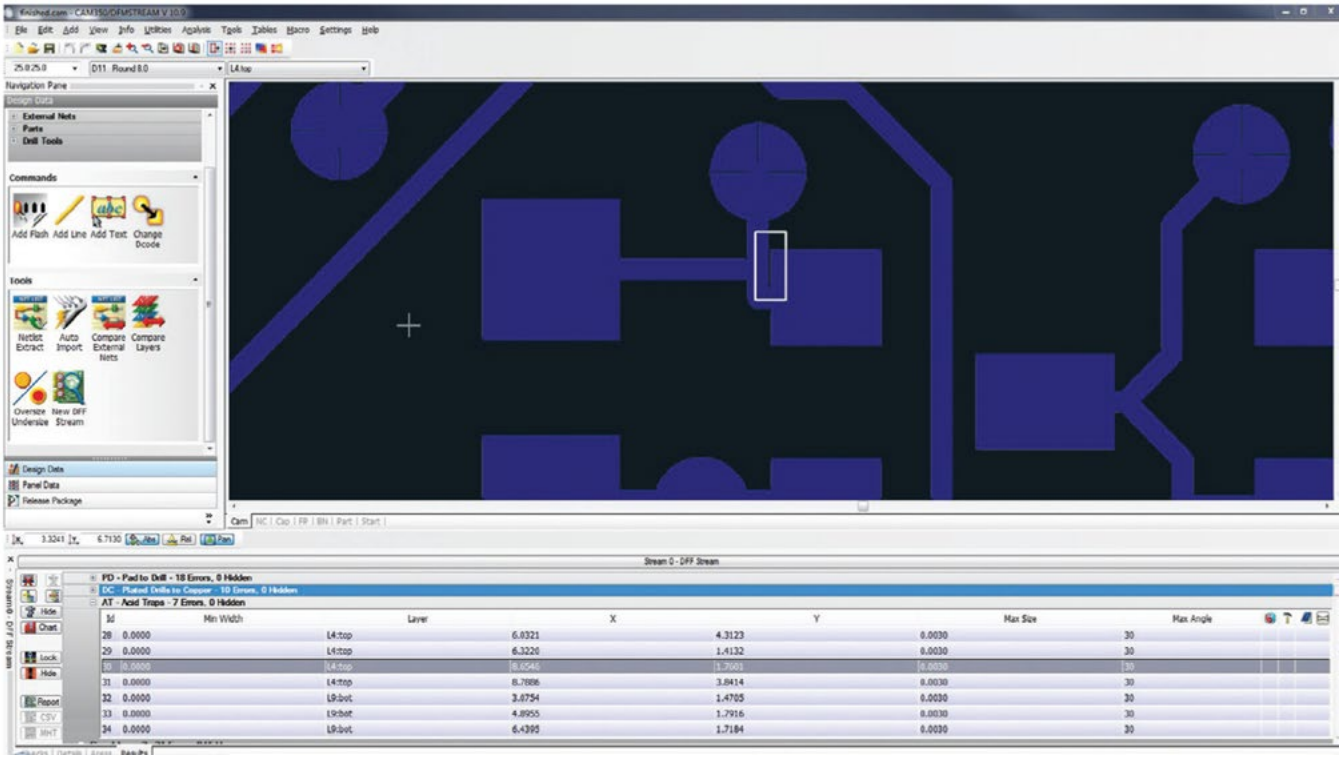

Figure 2: Acid traps have the potential of trapping acid during the PCB etching process longer than intended and can eat away a connection, making the circuit defective.

So why move DFM into the PCB design flow? There are several reasons: cost of finished PCBs, maintaining design intent, and the potential for future design failure. It can cost a PCB manufacturer as much as 20% of the cost of the PCBs for CAM engineering, which is the processing and tooling of design data to prepare it for manufacture. This additional cost is built into the end price that users pay to have physical PCBs fabricated. So, theoretically, designs submitted without DFM defects are less expensive to manufacture than ones with DFM defects. One could deduce that it's better to pay a little more to have a manufacturer ensure the design can be built. However, this creates other issues that are not so desirable.

To take a design that has DFM issues and make it comply with the manufacturing process, a CAM engineer may need to modify the design data. What this means is that the layout provided to manufacturing may not be 100% consistent with the finished PCB. Issues with electromagnetic interference, signal integrity, cross talk, etc., which are commonplace in today's high-tech electronics and are addressed in design engineering, may be unknowingly reintroduced into the design as it's reworked for manufacturing. There is also no guarantee that a CAM engineer will communicate the design changes back to engineering to be incorporated into the original PCB design database. So not only is the design layout different between engineering and manufacturing, but what happens when a second manufacturing build is required or the design is released to a different manufacturer for volume production?

Consider this real-life scenario: a design engineer designs a PCB, runs DRC analysis and determines that the design is correct. He creates PCB manufacturing files and sends the files off to a manufacturer to have prototypes made. The manufacturing engineer runs his analysis on the PCB files to ensure the design can be fabricated and identifies defects in the design that could result in scrap or low yields. Wanting to deliver a good product, the manufacturer fixes

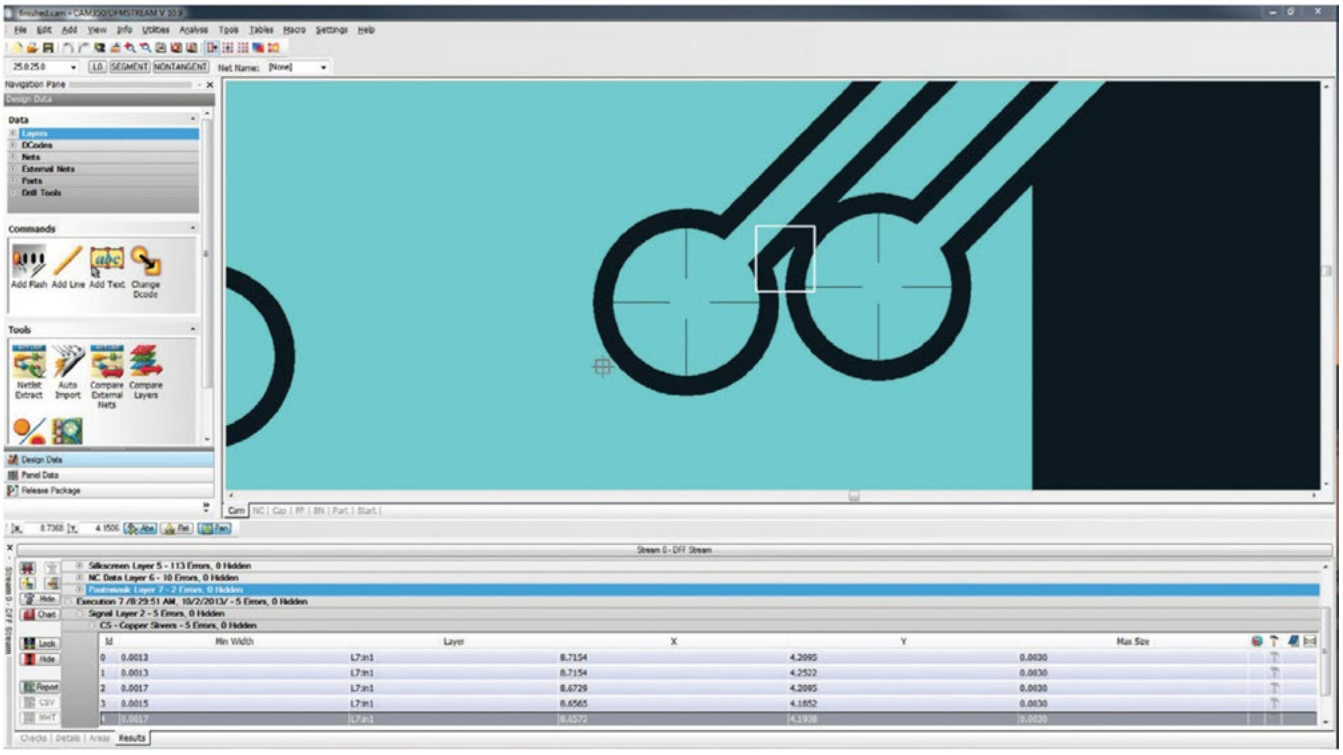

Figure 3: Small copper slivers can detach themselves during assembly, float around during soldering and inadvertently reconnect themselves anywhere on the PCB, potentially tying multiple nets together.

the issues, builds the PCBs and ships back the finished prototypes without communicating what changes were made. Back in the lab, the design engineer tests the prototypes and finds that they work successfully. That's great; however, unbeknownst to the design engineer, his prototypes are different from his PCB manufacturing files. Now the design engineer releases the manufacturing files for high-volume production from a different manufacturer who specializes in production PCBs. This manufacturer, for one reason or another, chooses not to run an analysis prior to manufacturing and therefore doesn't detect the same issues as the prototype manufacturer. They build and ship the finished PCBs back to the customer.

The boards are assembled and tested and, oddly enough, some, most, or all of the PCBs fail. Why? Because the design data still contained the manufacturing file's original DFM errors that were corrected in prototype, but never incorporated for production. The result was thousands of dollars in material being scrapped but—even worse and more costly—lost time-to-market. Had the design engineer had the ability to perform his own DFM analysis prior to prototype, the same issues could have been detected and addressed in engineering and incorporated in the PCB design where they belong, lowering the cost, maintaining design intent, and ensuring that follow-on builds also work correctly.

Just a few more minutes with the design in engineering would have prevented a whole design and manufacturing iteration, and the costs associated with it. So what are DFM issues? Mostly these are issues in the PCB topology that create adverse effects in manufacturing and are typically not detected in the CAD software that creates the design. Table 1 provides a short list of typical DFM issues that pass detection in the CAD system but can result in PCB failures in the real world. This is just a short list of DFM issues. Good DFM tools will analyze for not only these issues, but also many more that most PCB design systems are not architecturally designed to detect.

DFM Defect	Description
Starved Thermals	Plane connections that are tied correctly to a plane layer in a CAD system but inadvertently isolated from the rest of the plane.
Acid Traps	Acute angles that allow acid to build up in the fabrication process and over-etch a trace, potentially creating an open in the circuit.
Slivers	Narrow wedges of copper or soldermask that can peel off and either reconnect to other pieces of copper or expose copper that should be covered with soldermask.
Insufficient Annular Ring	A drill size is specified that exceeds the size of the pad being drilled and can result in a disconnect of the pin or short in a voltage plane.
Missing Clearance Pads on Planes	Pins that are missing a clearance pad will be connected to a plane layer. If clearance pads are missing from all plane layers for the pin, it will tie together all of the voltage planes as well.
Copper too close to board edge	When there is insufficient clearance of plane layers from board edges it's very likely that the voltage planes will be connected together when the PCB form factor is routed. The copper on each voltage layer is inadvertently "mashed" together.
Missing Soldermask Pads	End user failed to define a soldermask pad for a pin or component. This exposes more copper and creates the potential for bridging pins together during assembly.

Table 1: A short list of common DFM issues.

Until recently, having DFM analysis in-house has been very costly, creating an obstacle for many companies to adopt a pre-manufacturing DFM process. Previous DFM analysis software tools came with a very high price point, ran on expensive hardware, and required dedicated users to run the analysis, making it very difficult for adoption in the majority of the electronics market. The good news is that more mainstream DFM tools are now available in the market and can provide the same in-depth analysis, but instead have a very low cost of ownership to procure and, more importantly, maintain.

These tools are also much easier for the everyday design engineer to use and deploy in the PCB layout process, without really having to be a manufacturing expert. Several of these new offerings allow users to model the rules that their intended manufacturer uses, to ensure that PCBs can be built by a particular manufacturer, and then rule sets can be switched to model different manufacturers when the design moves from prototype to production. Because these tools are designed as DFM tools and are free from the constraints of PCB CAD, they can detect problems in a design that are not supported by core PCB CAD tools. Good DFM ensures that a design not only performs electrically as expected, but can be manufactured successfully in high volume quantities without increasing cost or risk, or adding unnecessary time to the design process. **PCBDESIGN**

Rick Almeida is one of the founders of DownStream Technologies.

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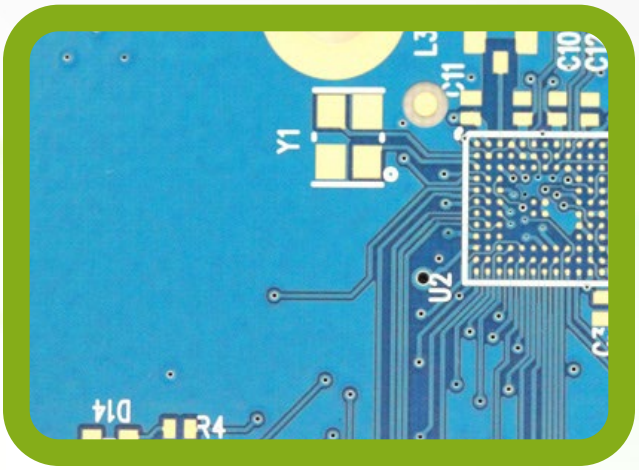

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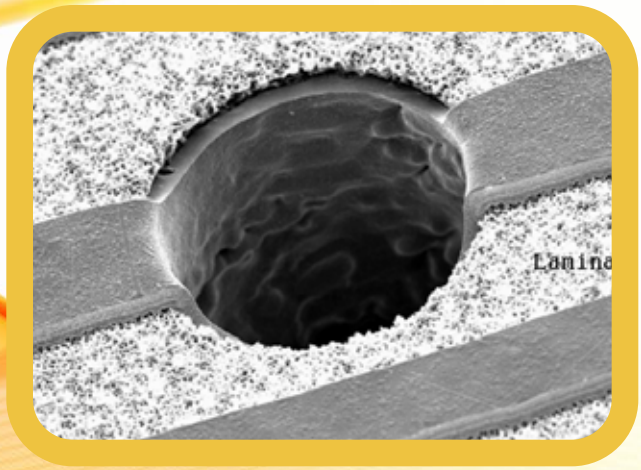

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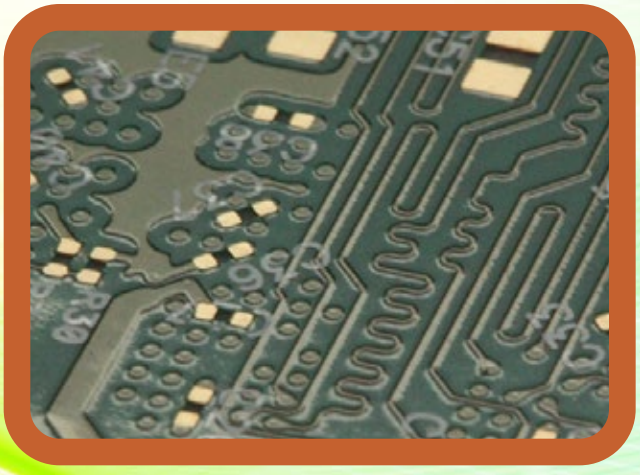

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DFM:
The PCB Designer as Arbitrator

by Tim Haag
INTERCEPT TECHNOLOGY

You abruptly snap awake. With a shock, you realize that you've fallen back asleep and now you're going to be late to work.

Quick! Get cleaned up and hope that no one notices that big tuft of hair on the back of your head that won't lie down as it should. You throw your clothes on and tiptoe across the bedroom in the dark, only to be rewarded by a squeal of pain as you step on the dog's tail. Sleepily, your spouse asks, "What's going on?" You growl a response that sounds similar to the dog's..

There's no time for breakfast, so on the way to work you pull into the nearest fast-food drive-through where the cheery mood of the perky young lady behind the window doesn't help your half-asleep dourness.You try to act like a human, grumbling a half-hearted "thanks" as you drive away, only to realize after you get on the freeway that your order is wrong. It's too late to turn around, so you throw the breakfast slider down your throat just to get something in your stomach, which now feels like it is lined with cement.

As you walk into the office, you get some puzzled looks and a few stifled giggles. All of which you ignore, until the guy in the cubicle next to you says, "Hey, did you know that your shirt is inside out?" The day hasn't started out very well and the last thing you want to deal with this early is a conflict. But when you see your design engineer approaching from one side and your manufacturing engineer from the other, you know that there is no escape. Welcome to the battlefield.

The Role of the PCB Designer: Appeasing Two Superpowers

We've all had mornings like this (to my embarrassment, I actually was told one morning that my shirt was on inside out), and then to get stuck between design and manufacturing requirements while the project is demanding results can really jump-start a migraine. But that's the job. Our role as a circuit board de-

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signer is, at least officially, to produce the best possible board design that we can. But realistically we have a lot of hats to wear, and one of the most difficult is to serve as arbitrator. We are the no man's land between two superpowers at war with each other: design requirements and manufacturing requirements. It is our job to come up with an amazing board design that satisfies both sides of this struggle. So let's look at how we can best serve that purpose.

Design engineering is usually a combination of electrical and mechanical engineers. Although these two groups can have their own dramatic conflicts between each other, they will usually end up working together because they ultimately serve each other's needs. But the manufacturing engineering requirements usually come from a completely different department or from an outside manufacturing vendor. To put it simply: The design team will probably be much more concerned that their design is functioning as intended as opposed to how it gets built. On the other hand, the manufacturing team's concerns aren't the function of a design; it's making sure that the design fits their criteria so that they can build it. This doesn't mean that either one of these groups are the bad guys. But they each have important needs that we circuit board designers have to meet.

“The design team will probably be much more concerned that their design is functioning as intended as opposed to how it gets built. On the other hand, the manufacturing team's concerns aren't the function of a design; it's making sure that the design fits their criteria so that they can build it.”

In my career, I have spoken with a lot of people at many different companies, and I have found that the adherence to manufacturing requirements in board design is vastly different from company to company. On one end of the spectrum are those companies who don't pay much attention to manufacturing requirements. These designs are usually generated in low numbers, so yields aren't the primary concern. Whether the boards are simple or very critical, their applications are typically limited and therefore unique. Because of this, there often is little in the way of manufacturing requirements as a lot of this work ends up being done manually instead of with automation.

Then, on the other end of the spectrum are those companies whose designs will be produced in high volumes. The manufacturing requirements here are usually very high, as the key to cutting cost is to automate the process as much as possible in order to reduce overhead and increase yields. And then there are all the other companies that are in between these two extremes. Many of these "in-between" companies will even use different levels of manufacturing requirements depending on which customer that they are working for, and/or which vendor will be used for which project.

So, the first thing that we can do to help out the relationship between design and manufacturing engineering is to improve communications. Often the board designer is the focal point between these two superpowers, which gives us the perfect opportunity to facilitate a productive environment where both sides can work together. I know that it is tempting to want to avoid conflict altogether and bury our head in the sand and just route traces. But ultimately our goal should be one in the same: To produce the best design possible that will generate the most success for our company so that we can all move on to the next project in a continual pattern of growth. So let's get these two sides communicating instead of fighting against each other.

And let me state the obvious here, just because we get them talking doesn't mean that there still won't be some conflict. No, there will still be issues that have to be worked out, and sometimes with a lot of debate. But getting the two sides working together on these issues is a much better solution than allowing problems to fester until upper management is forced to

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step in and find a resolution. So, how can we do this?

One way to help intra-departmental communications is to encourage participation. I have seen what happens in companies where communication is poor; instead of working together, they foster an "Us vs. Them" mentality. This can happen when people don't know each other, or are unsure of who has what responsibilities, or are blocked by departmental divisions or antiquated corporate policies.

So, engage these people. Ask for their opinions about your project and make sure that regular design reviews are scheduled. If anyone who should be part of the design review isn't, get them on board. One of the worst experiences you can have is to find out that a design failed due to a detail that was missed because a key person's input was absent during the design process. On the other hand, I've experienced the success that you can have by soliciting input from all team members during the design. Getting everyone working together usually leads to a result that exceeds the sum of the individual team members (synergy) which is good for the design, and ultimately good for the company.

Another thing that really helps is having your company's DFM process documented so that everyone has a clear understanding of the objectives. I have found that there is a vast difference between levels of documentation from company to company. For those companies who are already following established DFM practices, there is usually a high level of documentation. Typically it is formatted according to the standards used at that company and is available on the company's Intranet or at least in some sort of printed format. In some of these companies, the design is actually gated to this documentation and won't be released until official reviews are completed and signed off by specific design team members. Then on the flip side are those companies who have little, if anything, in the way of documented DFM practices. If DFM practices are followed at all it is usually in the form of "tribal knowledge" based on previous manufacturing experiences. And as before, there is a vast amount of companies whose DFM documentation is in between these two extremes.

So how can we help in this documentation process? First of all, make sure that you are fluent with your company's DFM documentation and that it is well ingrained with your design process. On the other hand, if you are working at a company where the DFM processes are not well documented, you can start by getting some of these processes written down. Ask "Is that really my job?" Depending on the size and structure of your company, it just might be!

"Another thing that really helps is having your company's DFM process documented so that everyone has a clear understanding of the objectives. I have found that there is a vast difference between levels of documentation from company to company."

Your next question might be, "How can I start?" A good place to start is by working with your company's manufacturing engineers, if available, or your manufacturing vendors, and finding out what your current standards are. Researching industry established manufacturing specifications is also a good way to gather information. The important thing is to start capturing some of these standards and get them documented. Even if all you do is to just create some simple bullet points, it's a good place to begin. You don't have to start out by trying to write a novel, just get the basics down in one place. Once you gather some of these ideas you will probably find that they will start flowing into what will eventually become a good working document.

The last area to mention in helping to build a successful union between design and manufacturing requirements is to incorporate automated DFM checking into the design process. Once again, there is a big difference in how this is being done from company to company. Some companies doing design don't have any

DFM checking in place and rely solely on their manufacturer. Other companies use only a visual check of their designs while others employ a very sophisticated automated checking process. Traditionally, automated DFM checking has been left to the manufacturing vendors to handle, and then those results are reported back to the designers. Any problems that are found would require design changes, and sometimes board spins are used to get the manufacturing bugs worked out. Since these same types of DFM checking tools used by manufacturers are available to us on the design side, we should use them.

There are a lot of applications out there that will assist you in DFM checking. Some PCB design systems have DFM checking functionality built right into them. Recently I was able to help one of our customers use our built-in manufacturing rules checking in order to expose a problem that would have resulted in his design being rejected by the manufacturer. There are also a lot of third-party tools out there that will perform these checks as well. The point is that you can perform the same level of checking that your manufacturing vendor does before the design ever leaves your department. This will save you the time and expense of waiting for someone else's checking results to be reported back to you.

Trust me; after years of working with designers from a support perspective, I am a big believer in automated checking. It can save your company time and money, it can save your design from being a mess, it can help prevent bad boards from being built, and it may even help you look like a hero when you save the day.

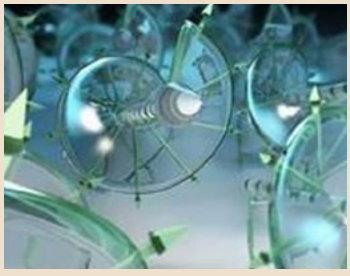
We have a big job ahead of us trying to satisfy the requirements of both design and manufacturing. But fortunately there's a lot of help out there for us to successfully negotiate a win for both sides of this epic conflict. Now, hold your head up high; your contribution as a board designer goes much further than simply pounding traces in. You have the higher calling of ushering in a new era of peace and increased productivity to this age-old struggle. **PCBDESIGN**

Tim Haag is customer support and training manager for Intercept Technology.

The Taming of Magnetic Vortices

Magnetic vortex structures, so-called skyrmions, in the future could store and process information very efficiently. They could also be the basis for high-frequency components.

More than six years ago, physicists at the Technische Universität München discovered extremely stable magnetic vortex structures in a metallic alloy of manganese and silicon. Since then, they have driven this technology further together with theoretical physicists from the University of Cologne.



The production of computer chips requires insulating, semiconducting and conducting materials. Today, magnetic vortex structures are available for all three classes of materials. Now a team of physicists at the TU München, the University of Cologne and the École Polytechnique Fédérale de Lausanne (Switzerland) has examined the dynamic behavior of the three materials.

With the results of their measurements, the team developed a theoretical description of behavior valid for all three material classes. The typical resonance frequencies of the skyrmions are in the microwave range – the frequency range of mobile phones, Wi-Fi and many types of microelectronic remote controls. Thanks to the robustness of the magnetic vortices and their ease of excitability, skyrmion materials could be the basis for highly efficient microwave transmitters and receivers.

Make the Right Decisions at the Right Time in the PCB Design Process

by Martin Cotton
VENTEC INTERNATIONAL GROUP

The right decisions are not always the easiest decisions, but making them well and as early as possible often avoids errors and addition costs. This is certainly the case in PCB design and a key decision influencing the design process and the eventual outcome is the selection of material and of the materials vendor. This is even more important when the PCB requires significant performance parameters to be met, such as high speeds.

What I am not trying to do is teach hardware or PCB design. What I am seeking to do is to consider the processes that lead to successful design and the errors that lead to risk, potential problems and compromises.

Let's take an example of a back plane design that has been specified at 10Gbs with 100 ohm impedance with a design target of 36 layers.

First, we need to ensure that we fully understand what the specification means. Are we sure we mean 10Gbs, which is a data rate in gigabits per second, and not 10Ghz, which is a frequency? Are we seeking that data rate for a single channel, or do we need that rate for a buss? The buss speed is the total of all the channels in that buss.

The next task would be to consider the design rules we'd like to apply based on the need for 100 ohms of differential impedance using two tracks that are in harmony so that losses

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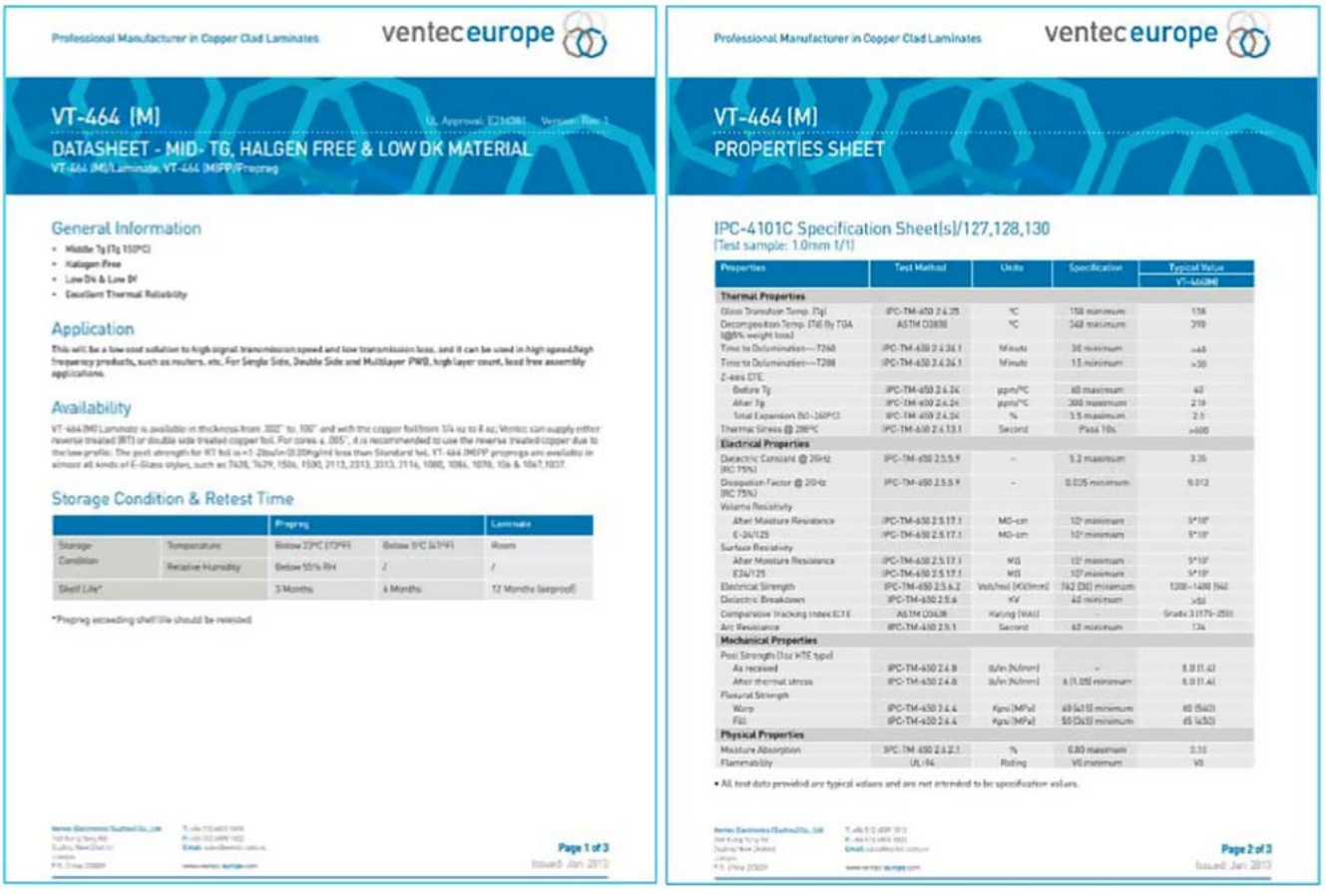

Figure 1: Typical supplier specification.

are minimized. The geometry of those tracks and their positioning with the PCB structure are critical to realizing a good design that can be manufactured with a good yield.

The design is only good when the specifications are met and the PCB can be manufactured with a good yield.

Now is the time to consider materials, because setting up differential pairs in the X, Y & Z axis requires we know and understand the Dk (dielectric constant) and Df (dissipation factor) of the material. Materials specifications are a good starting point. After all the suppliers will have designed the material with a purpose, so they will have a particular data rate in mind. But not all material suppliers are the same. Some will have design experience and some will not. Some are distributors, whilst others will have direct access to the staff at the laminator who designed the materials to meet a particular need in the market. Choose the vendor carefully and work closely with them to get the right material designed in, and agree design rules appropriate to that material and to your needs. They'll need to have experience of the fabrication process as well as design and be able to support you in working with the PCB manufacturer throughout the prototype and volume manufacturing process.

You're now ready to create the specification of the 'cells'—the traces, trace separation, pair separation, and the layer-to-layer separation. Again, the materials team should be able to support this and you should certainly be sharing it with them before starting the design. Impedance modeling can be performed at this stage using modeling software, such as that offered by Polar Instruments and other companies. The material Dk will have a substantial effect at this point impacting upon layer separation

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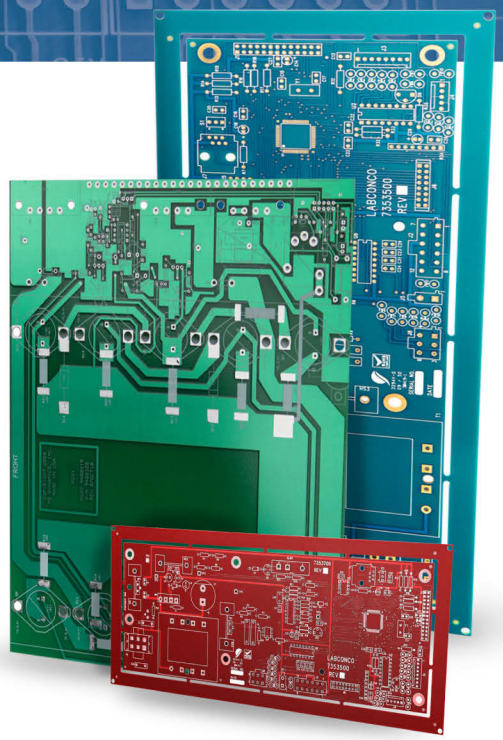

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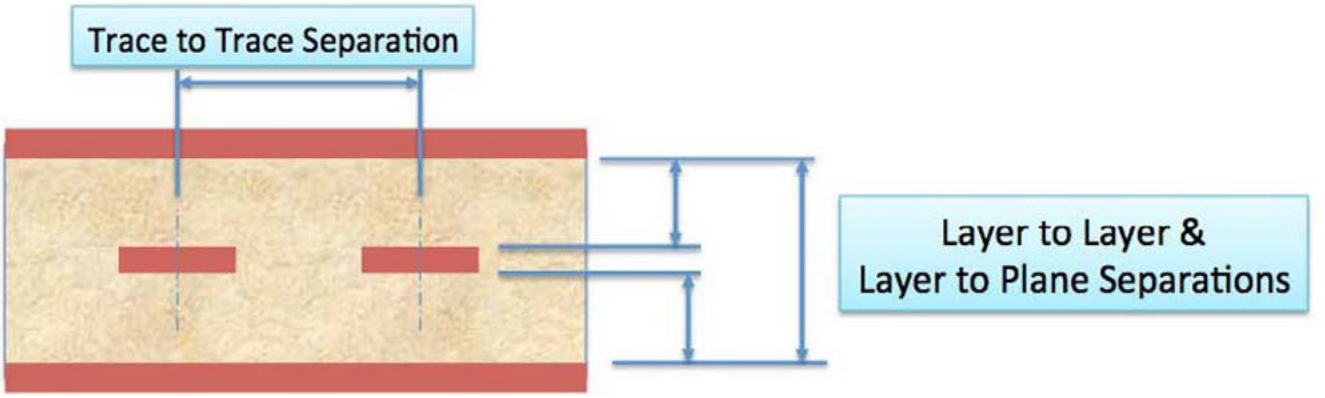

Figure 2: The completed cell.

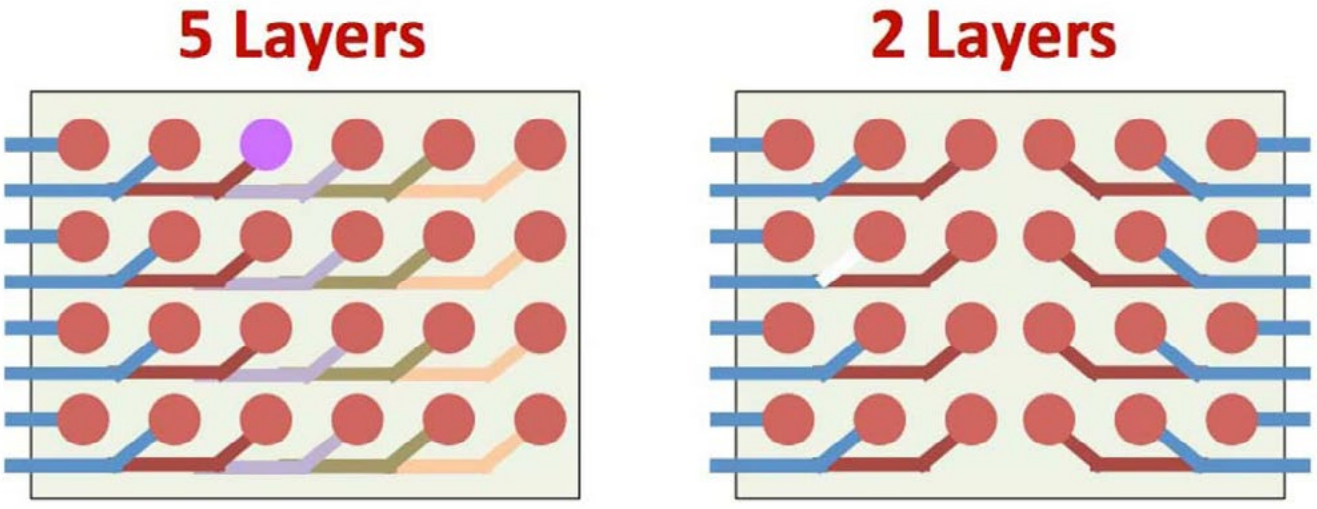

Figure 3: Trace mapping and depth of complexity (DoC).

and trace width. Df considerations are also critical in designing a successful cell that has the appropriate trace, pair and layer separation. It is worth spending time at this stage to get the right cell design and the right material, as it will impact everything moving forward.

With the cell as the heart of the design and the right material selected the stack up can be created, again with the support of the laminate manufacturer and the PCB fabricator. Key to understanding the impact of density on layer count and stack up is mapping the densest devices on the PCB, such as BGAs and connectors. Depth of Complexity (DoC) is a methodology for measuring and calculating initial layer requirements. Mapping power distribution and layers is essential at this stage in establishing how many layers are required to realize a successful design. And remember by successful we mean within specification and with a high level of manufacturability.

Having created the cell structure, the design rule, the orthogonal design and having selected the material and build we can estimate the cost and start the design. Again a good time to make sure everything is synchronized with the laminate supplier and the fabricator. Throughout layout additional checks and simulations are made to ensure we are meeting our specifications for good signal integrity (SI).

Having done it right so far, this is no time to lose your nerve.

The first pass of the design layout may not produce the perfect result. Let's imagine the post layout simulation reveals we have SI issues with 90 differential pairs of the 2,000 that we have used. This leaves us two choices. The hard way—fix them by individual review or the easy way—add four more layers dedicated to the 90 pairs. Clearly the hard way is the better way, but that takes time and that time requires skills, not just machines. This is where good designers stand out and can really earn their money. All too often the easy way is chosen, more layers are added, a materials upgrade is chosen with better performance and higher costs, often in the order of 15–25% are added.

In the case of our example, the hard way resulted in a board meeting the 36-layer target that fits mechanically and is easily manufacturable at the target cost of $1,200. The easy way delivered a 42-layer board, with a less readily available materials, which is harder to manufacture, costs $1,550 and impacts on other parts of the mechanical design, having impacted on board thickness.

The right way is undoubtedly the harder way, and the results will be savings enjoyed throughout the life of the product, greater reliability, more manufacturing flexibility and a real sense of satisfaction in getting it right.

Choosing a laminate is important, choosing a laminate supplier is even more important. A supplier or distributor can provide you with what you ask for, but a laminate partner will provide you with design and fabrication support throughout, helping you get it right first time. **PCBDESIGN**

Martin Cotton is director of OEM technology for Ventec International Group.

PCB007
News Highlights

California Congressman Mike Honda Discusses American Manufacturing

Barry Matties, publisher of I-Connect007, sat down with Congressman Honda, who represents District 17 in the Silicon Valley, to talk about American manufacturing, infrastructure, education and some of the current thinking in America. According to Honda, "The policies we pass and the things we do in D.C. that negatively impact our economy...a lot of those guys who don't support some of the positive things we want to see happen don't really understand that it impacts their districts, their social services, health and business."

MacDermid's Cullen Reflects on 20 Years in China

Recently, while in Shenzhen, China, Barry Matties had the chance to catch up with Don Cullen, the global marketing director at MacDermid Electronics Solutions. They sat down to discuss the many changes he's seen in China since his first visit there nearly 20 years ago, and the country's future.

Viasystems Reports Solid Q4 2014 Results

The settlement of our business interruption insurance claim certainly helped our reported profit for the period," noted David M. Sindelar, chief executive officer of Viasystems, "but even without that favorable impact, we had a solid quarter, growing net sales both sequentially and year-over-year."

N.A. PCB Business Growth Flat in 2014

"PCB business in North America was virtually flat in 2014 compared to the previous year," said IPC's Sharon Starr. "Sales ended the year less than one percentage point below 2013, while orders finished the year just 0.6% above 2013. Strong orders in the fourth quarter have kept the book-to-bill ratio solidly in positive territory, which bodes well for sales growth in 2015."

China Outlook: An Interview with Hamed El-Abd, Lionel Fullwood, and Gene Weiner of WKK

Barry Matties spoke with WKK's Hamed El-Abd, Lionel Fullwood, and Gene Weiner on their outlook on PCB manufacturing in China, as well as on what it takes to stay competitive in this market.

Exception PCB Names Martin Managing Director

Frederick Martin has been appointed as managing director for Exception PCB Solutions and brings a wealth of experience. Frederick will join Clive Wall and Rob Buswell in the Senior Management Team. The senior management are a highly experienced and results driven team that has the proven capability to implement Fastprints' European strategy and leverage the business's undoubted potential.

2015 EIPC Winter Conference, Munich: Day 1 Review

Ninety delegates, eleven countries represented and a thought-provoking two-day programme on themes of reliability in PCB fabrication and assembly, copper cleaning and advanced material solutions, advanced imaging and soldermask, and how to make PCBs smart and ready for Industry 4.0. Add the further attractions of a keynote by Walt Custer and the chance to visit a military aircraft assembly plant: the formula for another highly successful EIPC Conference—this time close to Munich Airport.

Schweizer Electronic Concludes FY2014 with Sales Growth

Dr. Maren Schweizer, CEO of Schweizer Electronic AG comments: "We proceeded very well in 2014 on operational as well as strategic levels. We increased turnover and earnings, and our order book is well stocked. Thanks to the continuously high demand our order backlog increased again in 2014, amounting to 119.2 million euro against 114.2 million euro the year before.

PCi Upgrades Imaging Department with New Equipment

Rigid-flex circuit board manufacturer, Printed Circuits Inc. has recently installed a Maskless Lithography printer and an Orbotech Paragon 9800 laser-direct imager at their facility based in Minneapolis, Minnesota.

DSG Invests in the Future

Mauro Dallora, COO of Dongguan Somacis Graphic PCB Co. Ltd (DSG), shares how they have increased revenue and their plans to double it.

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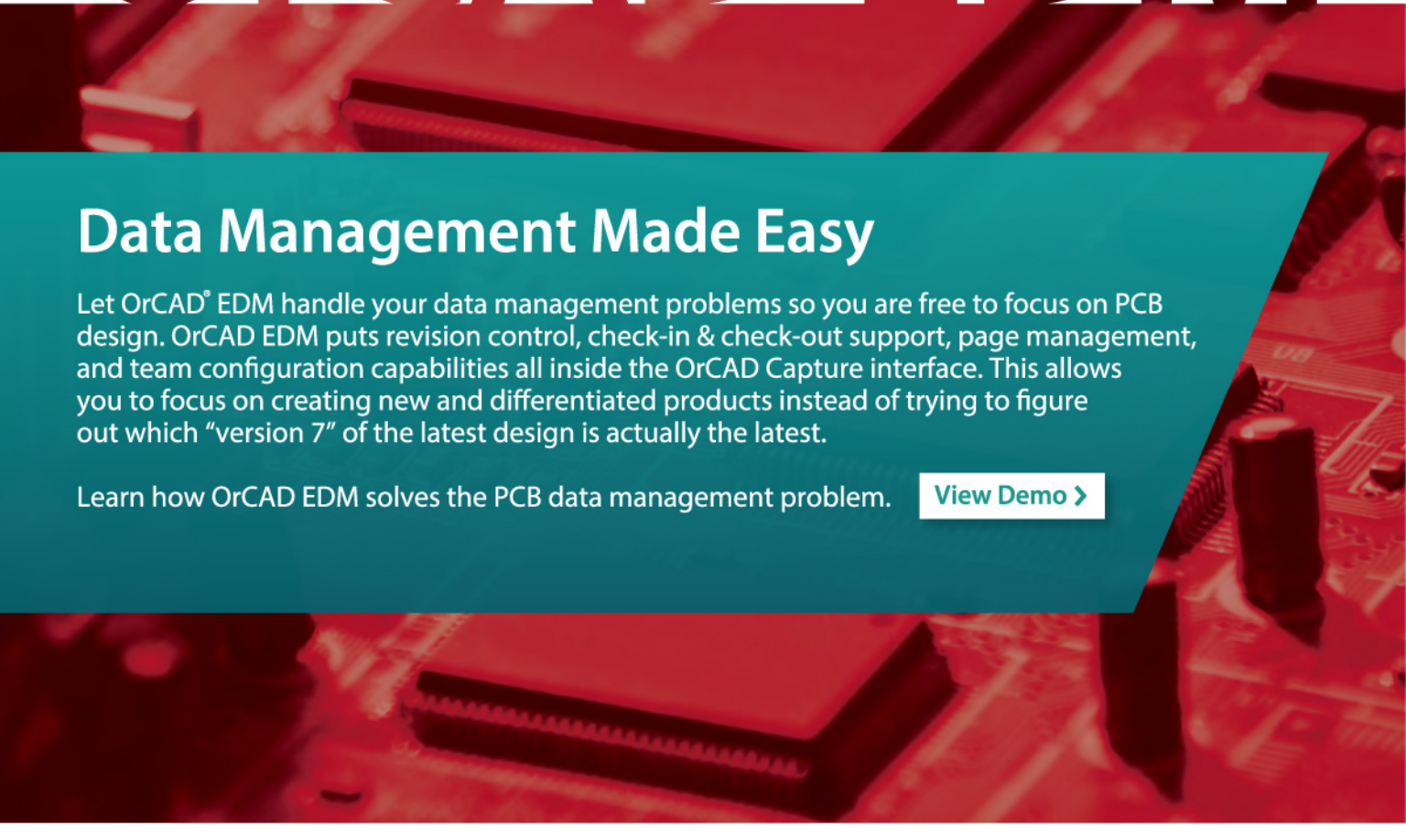

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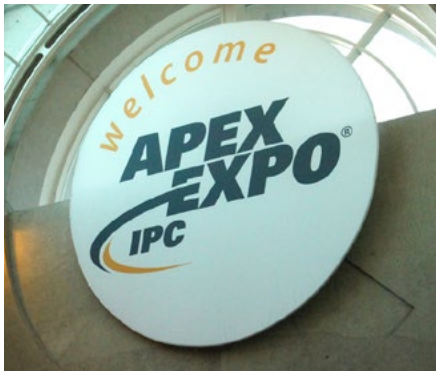
IPC APEX EXPO 2015: Tough Act to Follow

by Joe Fjelstad
SPECIAL TO I-CONNECT007

Based on personal impressions and conversations with folks met on the show floor and technical meetings, this year's IPC APEX EXPO trade show and conference was an unqualified success. The various trade show, conference and standards committees, in concert with the IPC staff, continue to raise the bar, improving the event to the benefit of members and industry participants from around the globe.

However, this year also marked, with sorrow, the first IPC APEX EXPO at which much beloved IPC staff member and industry icon, Dieter Bergman, was absent. It was tough not seeing him at the event—a feeling that was shared by everyone I met. Yet somehow, I sensed that many might have felt, as I did, that Dieter's spirit was still with us, urging us on.



In that regard, one of the highlights of APEX for me this year was an event held on Wednesday evening. It was a special tribute honoring Dieter with shared remembrances of a man, the likes of which we are unlikely to see again in our lifetimes. The well attended event was also the inauguration of the Dieter Bergman IPC Fellowship award. This new award in Dieter's memory was bestowed upon on a group of highly respected veteran IPC volunteers, each with decades of service to IPC and the industry. The inaugural award recipients included: Doug Sober, Shengyi Technology; Bernie Kessler, Bernard Kessler Associates; Denny Fritz, SAIC; Dave Hillman, Rockwell Collins; Don Du Priest, Lockheed Martin; Bob Neves, Microtech; Ray Prasad, Ray Prasad Associates; and Randy Reed, Via Systems. Each recipient was allowed to bestow a Dieter Bergman memorial scholarship upon the college or university of their choice. It

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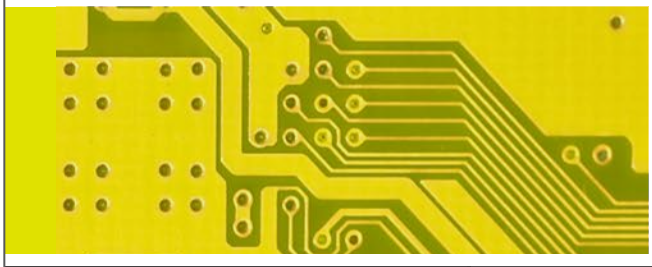

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2015 IPC APEX EXPO Show Review

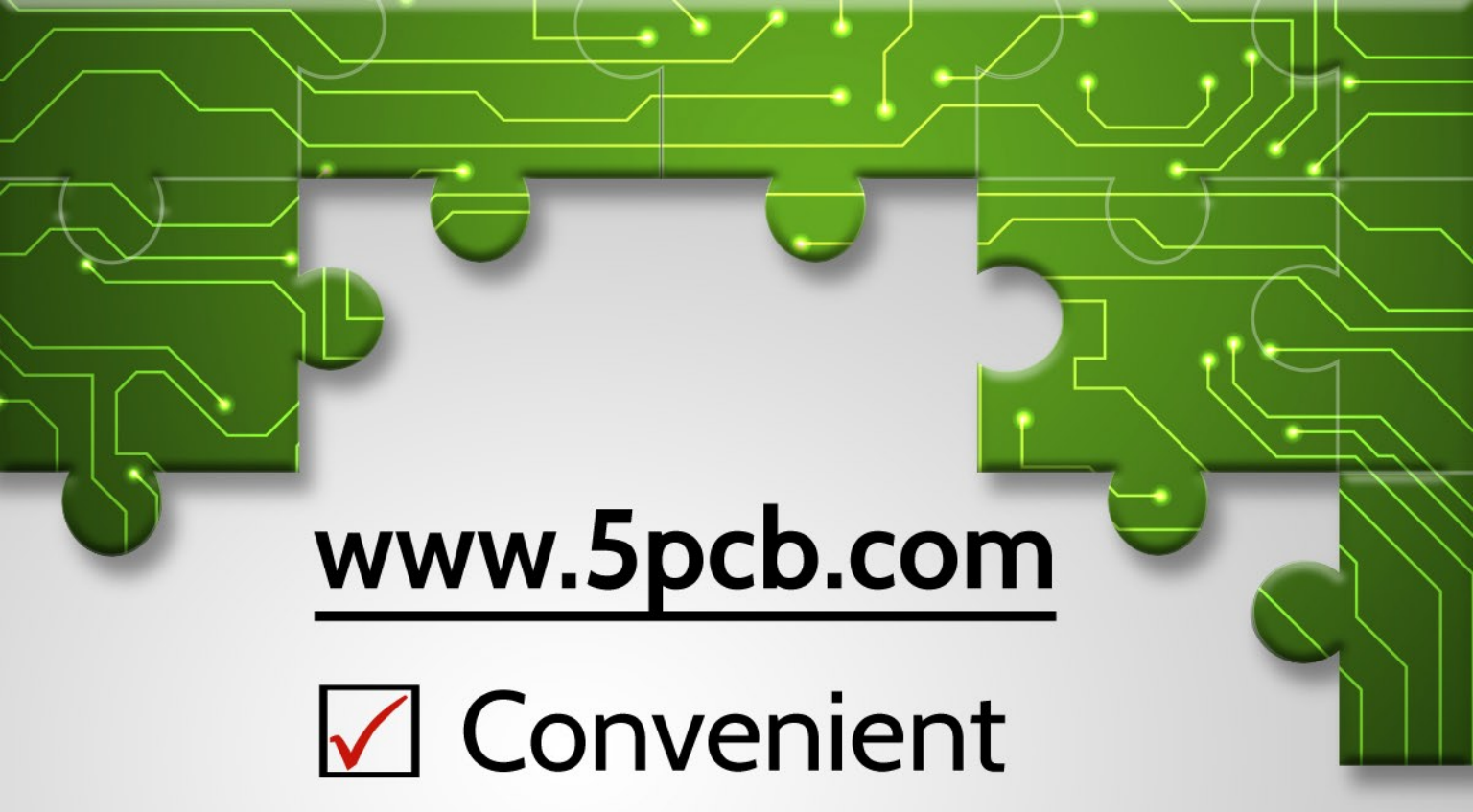
was a fitting tribute for a man who spent most of his life in service of and teaching industry colleagues around the globe.

Another highlight of the week was the induction of Gary Ferrari to the IPC Raymond Pritchard Hall of Fame. Ferrari was the first executive director of the IPC Designers Council and was instrumental in organizing and structuring the training courses that have been the backbone of design instruction for entry level PCB designers as well as the certification of seasoned ones.

A couple of other items of note caught my interest and attention. The first was a significant departure of tradition. This year's keynote session had a sponsor, eSurface. The company presented an impressively produced video which provided a visually captivating overview of their novel circuit manufacturing technology. Doubtless, it caught most everyone off guard. It was a foray into new territory for IPC and a significant break from tradition; frankly, I like such experimentation and the breaking of traditions. It could presage a future when, like the Super Bowl, such commercial productions, if done to a similar high level as this first one, could prove of as much interest to attendees as the subject of the keynote.

Finally, on the morning of the last day, there was the inauguration of IPC Town Hall, an open event, the purpose of which was to engage senior staff members, including president and CEO John Mitchell, directly with members in attendance with the intent of creating a dialog relative to what might be missing and or improved on with IPC programs and services. Discussions were lively and the challenges discussed were both real and important. I look forward to attending future such events. I think it could prove a great way for frontline members of IPC to express their desires and needs and hopefully help guide the association to improve its services to both members and the electronics industry.

In many ways new and old, the 2015 IPC APEX EXPO is going to be a tough act to follow. **PCBDESIGN**



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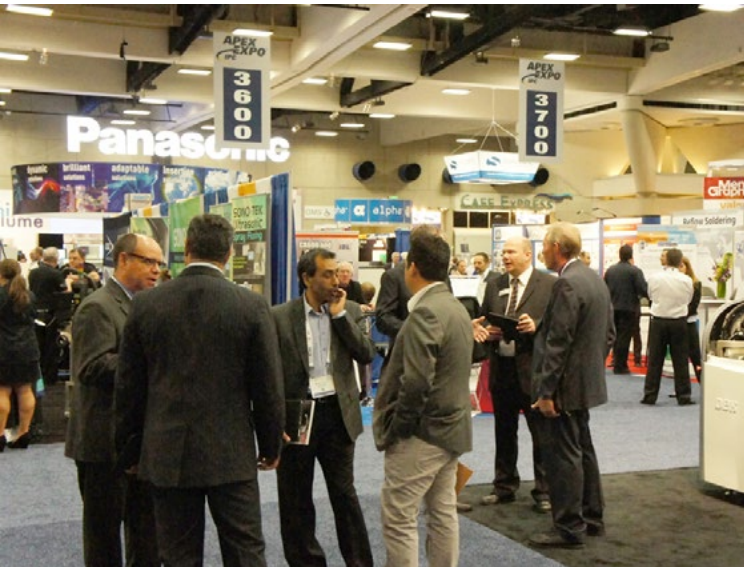
This Ice Cream's for You, Dieter

by Patty Goldman
I-CONNECT007

Another year has come and gone and so has another IPC conference and show. Doesn't seem that long since the last one, but a year is a year (well, actually 11 months but who's counting).

I'm one of those cross-over people, involved in committee meetings, the technical program and also an exhibitor at the show. San Diego is such a great venue for this, with everything right there and accessible. How pleasant to be able to quickly transfer from one area to the other. Plus, you were just a few steps from the door and could step out into the sunshine and perfect weather at any time; there were even tables set up outside (in the back) that we could use. We sure missed that in Las Vegas!

A number of people mentioned that everything seemed so…organized. The technical conference ran smooth as silk (at least that's what we saw—I know IPC staff works hard at that). Same comment for the show and show floor. It's always amazing to see the transformation from Monday night to Tuesday's opening bell. But it was really all very organized. The technical conference session I moderated was pretty much packed. The show floor was very busy on Tuesday, a little less so on Wednesday, and Thursday was exhibitors' day—where the exhibitors have a chance to conduct business with each other. I am sure much was accomplished all around.



A most notable exception to the regular programs was the tribute to Dieter Bergman on Wednesday evening. Dieter was without question the most recognized and best known person at IPC, truly the face of IPC. While most knew of him, recognized him, perhaps had met him or heard him speak, some of us were better acquainted with Dieter. We worked with him on standards activities, argued with him, had dinner and ice cream with him, laughed and argued some more, and counted him as a true friend. Many people spoke on Wednesday evening, recounting funny stories and jokes. But all had another common thread—friendship.

After this event a group of us decided on another IPC meeting tradition: ice cream! We headed out with IPC patriarch Bernie Kessler to a tiny shop in the Gaslamp District. Some of us had gone on many an ice cream outing at IPC meetings; we dragged along some newbies this time. The only rule was "no business to be discussed." And so a pleasant hour was spent and new friendships were formed, complete with the required group photo (thanks, Kelly Dack). And that's what it's all about. **PCBDESIGN**

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Real Time with…IPC APEX EXPO 2015

An Interview with Keynote Speaker Dr. Stanton Friedman and Publisher Barry Matties

After Wednesday's keynote, publisher Barry Matties invited Dr. Stanton Friedman, a nuclear physicist, lecturer and UFO researcher to the *Real Time with…* booth for a lengthy interview on Friedman's long career with companies such as GE, Westinghouse, and McDonnell Douglas, among others. Friedman has worked extensively on highly advanced and classified programs focused on nuclear aircraft, fission and fusion rockets and compact nuclear power plants for space and terrestrial applications. Friedman has presented at more than 600 colleges and universities and 100 organizations spanning the United States and Canada, and more than a dozen countries abroad. The following is excerpted from the complete interview conducted on February 25, 2015 on the show floor.

On ENERGY RESEARCH:

Barry Matties: I'm interested in how your career and our industry eventually intersected. Let's start by telling us about your early career, and the scope of your work in energy programs.

Stanton Friedman: From 1956 to 1959, I worked on the General Electric aircraft nuclear propulsion program at Cincinnati General Electric. In '58, we spent somewhere around $100 million. We employed 3,500 people, of whom 1,100 were engineers and scientists. In other words, it wasn't six professors and 12 grad students; it was a major effort to develop a nuclear airplane that could fly farther, longer. It wouldn't have to stop for fuel. All the programs that I worked on spent tons of money. It was all based on the premise that we were going to beat the Russians.

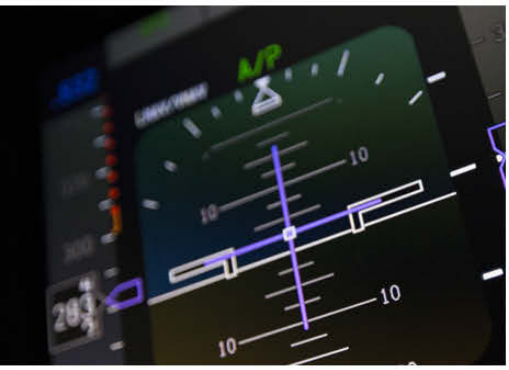
When I worked for Westinghouse, we tested a nuclear rocket engine that was less than eight feet in diameter. The power level was 4,400 megawatts, twice the power of Hoover Dam, which is a little bit larger than that. It was all government funding. Then they cancelled the program. It takes guts to pursue new technology.

Barry: There is such a fear of nuclear energy as a power source, which I don't understand.

Stanton: I don't understand it either. Nobody said, "We should get rid of all our cars because we killed over 30,000 people last year with automobiles." That's the price you pay.

Barry: I understand the catastrophe we saw in Japan, but now my understanding is, and maybe you can clear my thinking up here, that years ago the French approach was not to use rods, but balls, it seems. They turned off all the cooling. There was no melt-down.

Stanton: The nuclear industry is frankly one of the safest industries. I'm not an apologist for the industry at all. I belong to the American Nuclear Society who use double, triple, quadruple backups for things because they realize how important it is. If you're in a submarine, often in the middle of nowhere and down 1,000 feet, the alarm system better be reliable. It isn't



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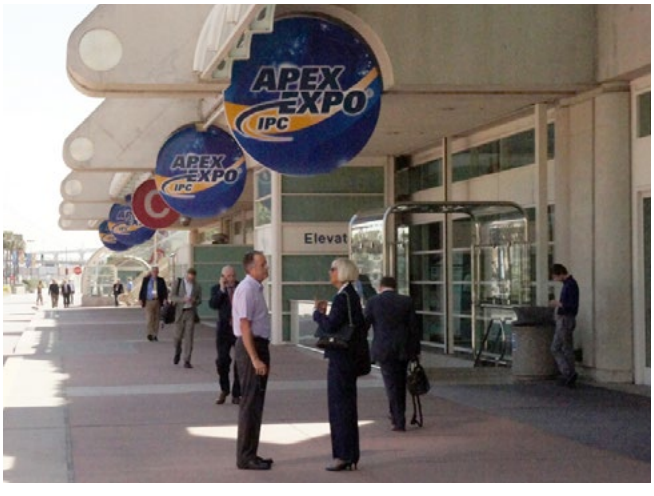
enough to say, 'It works but if something goes wrong, we'll just stop in a port and fix it.' It's not like you're driving on the highway and you need a new tire or a new battery. You're shit out of luck if these things don't work reliably.

They're designed for long life but people are shocked when I tell them, 'We have nuclear power to aircraft carriers that can operate for 18 years without refueling,' which means everything in there has to be ultra-reliable. What good is it if things break down all the time?

On TECHNOLOGY:

Barry: What is your opinion on the direction of technological progress?

Stanton: My motto, mantra, is that technological progress comes from doing things differently in an unpredictable way. The future is not an extrapolation of the past. You have to change how you do things. Some people don't realize that. I lecture at a lot of universities. I run into opposition from the nasty, noisy, negativists as I call them. You can't get here from there. It's impossible. An outstanding astronomer of the 19th century, Simon Newcomb said, 'Man will never fly in an airplane.' Two months later, the Wright Brothers made their first flight. The year before Sputnik, Astronomer Royal Sir Richard van der Riet Woolley was quoted in *Time Magazine* as saying that 'space flight is utter bilge' and that 'nobody would every pay for it. What we need is better instruments for astronomy.' Mankind has a long history of underestimating change.



On the ELECTRONICS MANUFACTURING INDUSTRY and UFO RESEARCH:

Barry: Tell me about your experience here, at our industry event.

Stanton: This industry, well, I'm intrigued to be here for two reasons. First, it's proof that technological progress comes from doing things differently in an unpredictable way because whatever they're doing today is altogether different than the way it would have been done 20 years ago. Second, this is an international meeting. At least 49 countries are represented here. I am very worried about how we look to the aliens as a primitive society when our major activity is tribal warfare. We only killed 50 million people during WWII. That's pretty sad commentary, but here I see people from all over the world. They're exchanging ideas, talking to each other, being friendly, if you will, with each other instead of each one sticking to his own thing.

We all realize there's benefit from interchange. You may lose some sales, but in the bigger picture you're better off. I'm very pleased about it. I've got an eight-year-old great-grandson. I try to envision what the world is going to be like when he grows up.

Barry: It's a real treat to talk to you today. I really appreciate your time.

Stanton: My pleasure. I've enjoyed this conference. **PCBDESIGN**

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IPC APEX EXPO 2015: Allow for Serendipity

by Kelly Dack
I-CONNECT007 GUEST EDITOR

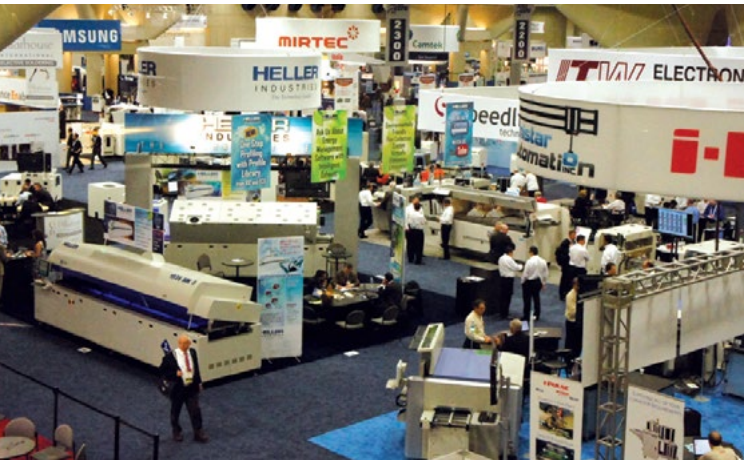
"If *Plan A* doesn't work, stay cool! The alphabet has twenty-five more letters…"

—Claire Cook, best-selling author and reinvention expert

Andy Down!

At the start of the IPC APEX EXPO, Andy Shaughnessy, managing editor of The PCB Design Magazine and my trade show coverage mentor, was horribly under the weather. But while he arrived in San Diego eager to begin reporting and interviews, he was able to cover only a few events before being quarantined by his I-Connect007 team out of fear of being the first media organization to accidently record a lung being coughed up on-cam during an interview.

Now, while Andy looked and sounded really sick, I don't think he was at all contagious. I spent a good deal of time before the show with him strategizing for some interviews and I even dined with him at a local sushi joint. And even as I write this, days later, I still feel great. Disclaimer: I do tend to spend a lot of time with Andy at the shows so I've built up plenty of immunity points. Andy asked if I'd submit my show perspective since his was shrouded in a haze of cough remedies. (I hope you are better, my friend!)



Kelly the Trainer

I arrived in San Diego early to join Gary Ferrari, IPC Master Instructor and co-founder of the Certified Interconnect Designer program, to conduct basic CID training prior to the start of APEX. As the official instructor for the course, Gary was there to not only facilitate review and learning for the students, but to mentor, observe and evaluate me as a candidate for Certified Interconnect Trainer (CIT.) In the months of preparation for this week, I learned a lot about the origins of the subject matter covered in both the CID and CID+ programs. I learned that the material is actively reviewed, updated and taught by a team of highly skilled, highly connected and highly respected IPC certified PCB instructors who double as industry design professionals. I learned that they put in countless hours of their own time improving the program and I learned that these folks aren't willing to settle for good enough when it comes to course materials and training.

The logistics behind the CID & CID+ programs are effectively administered by EPTAC, an IPC-licensed training center. It was easy for me to see that everyone involved in the CID, CID+, and CIT programs plans for success that is very much based upon the success of others. It is up to the students how much time beforehand they put into individual study. The job of the class instructor is to review, discuss and teach the materials and proctor the exam. I was very proud of this basic CID class. My excite-

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ment for their success grew as I got to know them a bit throughout the three day program. Their questions, challenges, dialogue and extra efforts in study resulted in an exceptionally high pass rate overall. Well done. Go on to design great things!

IPC Designers Council Executive Board Meeting

Enter serendipity. I was pleased to accept an invite to attend the IPC Designers Council Executive Board meeting scheduled for the evening after our testing concluded. Within moments of entering the meeting room I was shaking hands with Master Instructors and executive board members from Australia, Germany and Malaysia…even as far away as Texas! They are a friendly and lively bunch. And while it is not my place to report on any details of the meeting, I will declare to all Designers Council members and anyone thinking about joining the IPC Designers Council that you are well represented by this executive board! They work passionately within the council and effectively with IPC directors to plan, evaluate and improve IPC supported programs which involve and educate PCB designers.

Design Forum

Once again, I was glad to have the opportunity to attend the Monday Design Forum event. This year's list of speakers included Carl Schattke, a PCB design engineer from Tesla Motors, who spoke on the subject of design for success.

PCB library expert Tom Hausherr, president of PCB Libraries Inc. discussed the IPC-7531C land pattern standard and generated quite a bit of audience engagement by presenting some new ideas for PCB component identification and marking.

IPC Master Trainer Rainer Taube, from Taube Electronic GmgH and FED Germany, spoke on component mounting issues and offered some

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recommendations in context of IPC-7070, for which he serves as committee co-chair.

Now, my usual plans for attending any designer event are clear: hear what industry icon Rick Hartley has to say. Rick speaks out of love and experience on every topic he discusses. At previous Designer Forum events, I've heard him give kudos, and I've heard him be blunt. I've watched him yell at the top of his lungs while pounding on the lectern to make a point, and I've heard him explain the need to invest in yourself and your design education, while the audience sat so mesmerized that you could hear a pin drop. So I could only imagine that his talk this year on "success through control of cost and quality" would bring the house down. But as serendipity would have it, I got called out early for a previously arranged plant tour of Hallmark.

Plant Tour

San Diego County is home to quite a few reputable PCB manufacturers. Whenever I travel, to PCB industry events, I make a point of visiting and getting to know the processes and capabilities of PCB manufacturers in the area. This year, I wanted to follow up on a 2013 interview I did with the Italian PCB manufacturer Somacis and check out their progress since their acquisition of Hallmark Circuits in nearby Poway.

Hosting my visit to Hallmark was Somacis Sales Manager Bryan Fish, who was happy to pick me up for the tour. While the Hallmark facility was much as I remembered it when I lived in the area 14 years ago, the equipment and capabilities have surely changed! Bryan was able to show me most of the new equipment. I met some staff members in the CAM area who worked there over 14 years ago. I try to include lots of photos in my reports to reinforce what I've learned, but my photo snapping was limited due to Hallmark's certification as an ITAR facility, so I have nothing visual from my tour to share. But while pictures may be worth a thousand words, taking time to tour a PCB manufacturing facility like Hallmark can be worth a thousand pictures! Designers, immerse yourselves in on-site understanding. Make what you've heard and read about tangible; it will make you a better designer.

Andy Kowalewski talks with Gary Ferrari at the Hall of Fame Award ceremony.

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Awards

IPC is very active in acknowledging unique individuals in the electronics industry. Tuesday's award luncheon granted IPC's highest honor—the IPC Raymond E. Pritchard Hall of Fame Award—to two recipients, Gary Ferrari and Eagle Circuits President Nilesh Naik. I caught up with Gary talking to IPC Master Instructor Andy Kowalewski. Andy asked Gary a few questions about winning this prestigious award. Andy asked Gary, "What's next?" Without flinching, Gary replied, "Keep going!"

Dieter Bergman Memorial Tribute

As planned, Wednesday evening I attended the memorial tribute to Dieter Bergman. I knew what to expect. I knew there would be food, drink, photos and good stories about the man Dieter. I expected tears of sadness at this gathering but felt joy for all of Dieter's friends and family when many of those who stepped up to tell a personal story about Dieter parlayed their experiences into tears of laughter from the audience. Many stories stood out about Dieter's bizarre foods affinity. As told, when travelling, Dieter made a point of sampling new foods. Some of these foods did a good job of upsetting his constitution. To soothe his stomach, he and his meal-mates began enjoying a bit of ice cream after their meetings, which seem to help. Closing out an evening with ice cream quickly went from panacea to tradition for Dieter and many of his frequent companions.

After the tribute ended, PCB designer Jack Olson and I ran into a group of IPC members who were celebrating Dieter's ice cream tradition, and they invited us to join them. And so it was that some of Dieter's good friends who wanted to soothe the events of the past few months, the week and the evening, did just that—and the ice cream tradition continued.

Hope to see you next year. **PCBDESIGN**

Dieter's last ice cream stand: From left: Bernard Kessler, Jo Ann Sotelo, Patty Goldman, Midge Ferrari, Gary Ferrari, (unidentified IPC member), Vern Solberg and Jack Olson.

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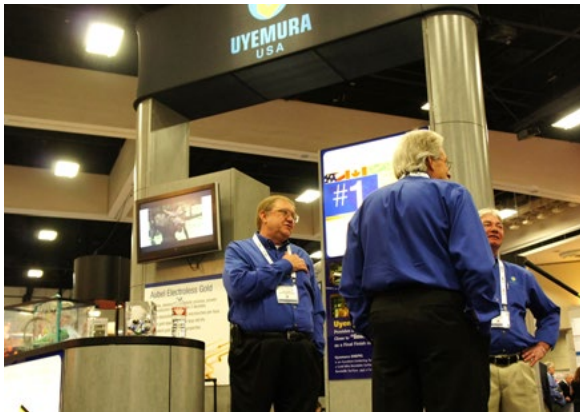

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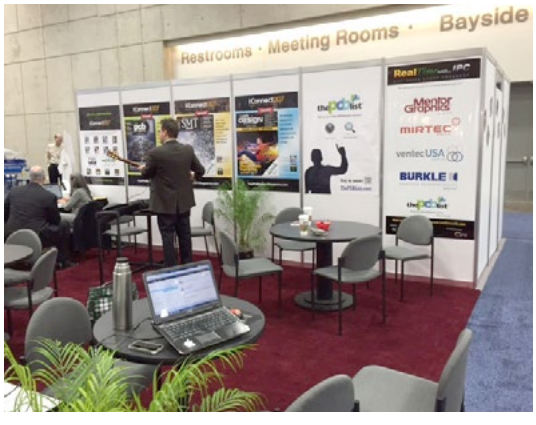

Cadence's Brad Griffin Digs Deep Into DDR

Guest Editor Kelly Dack stopped by the Cadence Design Systems booth at DesignCon 2015, where he sat down with Product Marketing Manager Brad Griffin to discuss Cadence's advanced PCB design and signal integrity tools, and the company's focus on DDR.

Kelly Dack: Brad, since you're the product marketing director for Cadence Design Systems, I'd like to ask a few questions about your DDR products. But first, please give us a brief overview of DDR.

Brad Griffin: I'd be happy to. One of the main points about a computer is that it has memory and you can store data in that memory—that's kind of what makes it a computing device. So they've been finding ways over the life of electronics to store and retrieve data faster out of memory. Somewhere around 2002, we came up with this idea of doubling the data rate in DDR memory, or double data rate memory. That was unique because basically, we clocked the data into the memory, both on the rising edge and on the falling edge of the clock. It was a clever way with the same sort of signaling to basically double the data rate speeds.

KD: Was there an organization involved? Was it standardized?

BG: That's really good question. As of right now, there's a standard committee called JEDEC, and I'm going to assume they were in place back in the 2002 timeframe, but I'd have to go back and check. But obviously there's memory companies and they have to be able to plug-and-play with different controllers as they're driving the memory, so there's probably always been a standard they've been marching toward. That process used to be a lot simpler. You'd be transferring data at maybe 100 megabits per second. You would send the data, clock it in, and it wasn't nearly as complicated as it is now.

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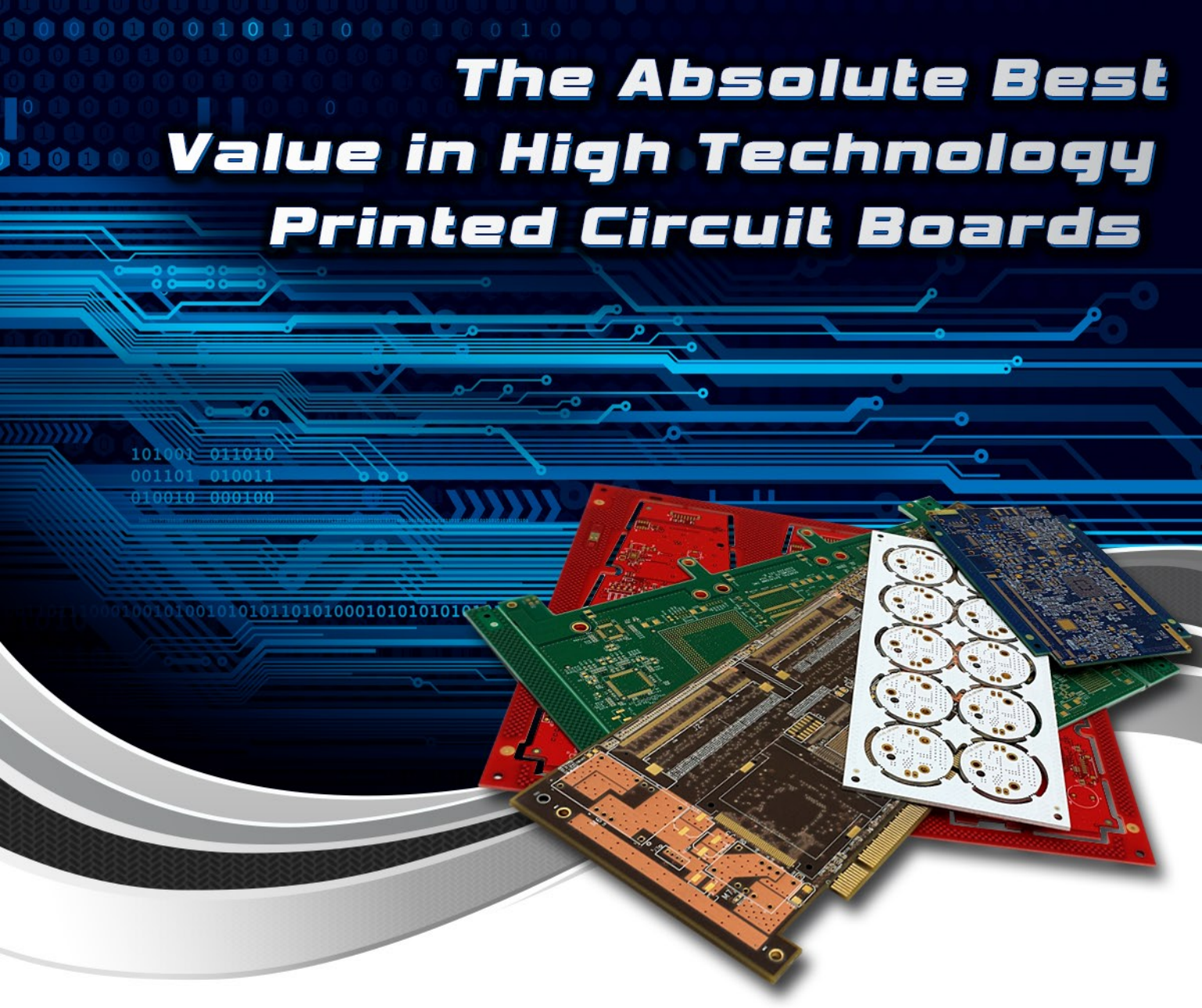

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KD: So where has DDR come from, and where is it now?

BG: There was DDR2 and then DDR3, and probably 2015 is going to be the transition where most DDR3 designs go over to DDR4. Typically, this happens because the DDR4 memory will actually become less expensive than some of the DDR3 memory.

KD: What does that mean as far as the technology from a power standpoint as well as a data standpoint?

BG: The main difference from a technology standpoint from DDR3 to DDR4 is the speed. It basically just gets faster. So any application you have in the computer that's run with DDR4 memory will make for a faster computer than one running with DDR3. One of the exciting things that has migrated probably over the last five to seven years is this new version of DDR called LPDDR, which stands for low power. That's been something primarily used in mobile devices because you certainly don't want your cell phone to run out of power in the middle of the day.

KD: With this reference to power, if I understand correctly, DDR came from a 2.5 V system and shrunk to 1.8 V and 1.5 V, and DDR4 is down at a little over 1 V. That seems really low already, so where will the LPDDR take us?

BG: If you can believe it, the LPDDR4 specification only has a 300 mV swing, so it's really low. That means that for signal integrity and power integrity engineers, there's really very little margin left. We said there was very little margin left when it was 1.5 V, and now we're down to 300 mV; this very small swing of data means that your signals have to clean and your power planes have to basically be stable. Because then you have to have a power/ground bounce associated with simultaneous switching signals. It's going to basically make it so that you're not going to meet the signal quality requirements that JEDEC puts in place for LPDDR4. So designs are getting really interesting and what we're excited about this year at DesignCon are the things we've been putting into our tools to enable designers to be able to validate that they've done everything they need to do to meet those LPDDR4 requirements.

KD: Let's talk about your tools. Would you give us an overview of some of the advanced tools at Cadence and how you're helping designers to solve some of these higher-speed, lower-power issues?

BG: Thank you for giving me the opportunity to talk about that because we're really excited about our products. Really, the foundation for the PCB and IC package design technology at Cadence is Allegro. Allegro has been around a long time; it was called Valid a long time ago before Cadence acquired it. So that's been the place where all the actual physical implementation takes place. What we did is layer signal integrity and power integrity analysis tools on top of Allegro, which have been in place since the mid-1990s. They've been serving the market fairly well but a very exciting thing happened in 2012. Cadence acquired a company called Sigrity. Sigrity is well-known for power integrity technology and their tools called PowerDC and PowerSI, which enable both AC and DC power integrity analysis

When you merge that together with their signal integrity analysis technology, what we've been able to do is take state-of-the-art, world-class signal integrity and power integrity technology in 2012 and spent the last two and half years not only improving that technology but tightly integrating it with Allegro. Now the Allegro user base has grown accustomed to having tools where they can have signal integrity analysis on-the-fly right from the board. We're giving them advanced technology that allows them to run more advanced field solvers, more advanced analysis engines and it might not sound like that much but when we go back to the idea that we only have that 300 mV swing in LPDDR4 an integrated solution is key to converging on a working solution.

We've got this advanced analysis technology tightly integrated with the implementation environment because what will typically happen is you'll run an analysis and it doesn't work—it failed the JEDEC requirements. So, what do I have to do? I have to start working with my power plane, working with the signaling, cleaning up everything, maybe there are too many vias on the signal, etc. But once you do all this you rerun the analysis and see that you're getting closer and you start to see yourself improving. Because it's so tightly integrated, our customers can accelerate the process of finding the problem, fixing the problem and verifying you fixed the problem. It's been an exciting ride the last two and half years with Sigrity and Cadence, and the Sigrity 2015 release coming out during DesignCon is really the culmination of bringing the latest and greatest technology to the market and has addressed these very difficult design and analysis challenges around LPDDR4.

KD: We have engineers and layout people—people that specifically do SI work. Are these tools used in a team application?

BG: The challenge has been that historically, data has just been thrown over the wall: I'm the designer and I throw it over the wall; the SI guy says "fix this" and throws it back over the wall, and it's a typical back-and-forth. It's very difficult to converge. On the other hand, the work that the signal integrity and power integrity engineer performs comes from a level of expertise in his area that you can't really expect a PCB designer to have. On the other hand, the person doing integrity analysis doesn't really have the level of expertise to make the changes to the physical design that the PCB designer has. We recognize that, yet we try to provide an environment which allows the gap to be bridged as much as possible. So our Allegro PCB analysis tools, as I mentioned, have the signal integrity tools residing right on top, so we have an environment where the layout person with some level of knowledge—maybe he knows how to get IBIS model on the web and can attach that to one of his components and can make sure that all of his resistors and capacitors have proper values associated with the design database—can actually say let me analyze the signal and see what it looks like. He may not have the expertise to know exactly how to fix it, but at least he can identify there's a problem and then just needs to determine how to resolve it.

Our approach here is that we try to let the layout person with some level of electrical background go as far as he can and then bring the expert into the same environment. It's how we've sort of structured our technology—we've got the base signal integrity technology that probably both expert and non-expert can use, and then we have advanced analysis technology that sits on top of that. The expert can go in and run the DDR simultaneous switching noise analysis. It can figure out that he's going to have 64 bits simultaneously switching and the signal is not going to work. He'll have to make some changes to the power plane to make sure it's more stable, perhaps by adding some more decoupling. He could actually with some level of expertise or knowledge of how to place things around the board put down his own capacitors, try out how it'll work and improve the overall process.

KD: Is what you're describing a radical change to front-end design with these new speeds, where it's not your classic front-end design anymore with a simple schematic passed down to a layout designer?

BG: It's an excellent question because for quite a long time Cadence has pushed what we've called a constraint-driven flow, where you do a lot of analysis upfront, create constraints, drive those constraints into design and push that forward to layout and verify it at the end. That's basically our methodology that Cadence has put in place for signal integrity, but one of the things we're showing in our booth is that we're moving this constraint-driven flow so it's not just signal integrity, but also power integrity. Because we believe that if the hardware engineer that is doing the schematic knows this

component needs a certain amount of decoupling associated with it, instead of just putting all the decoupling capacitors on a page at the end, he basically associates his decoupling capacitors with that component in the schematic. Then when it gets to the point that you're doing actual placement of the decoupling capacitors you're going to get violations that tell you that you haven't placed the right capacitors within the right radius of this component. So we're bringing this constraint-driven flow to power integrity that's always been there for signal integrity.

KD: Excellent. Let's talk about serial interfaces. Tell us where they've come from and where we're going with them.

BG: One of the most interesting things in signal integrity is around the serial interfaces and it also sort of mixes with memory interface design as well, which is a parallel bus. With serial interfaces, the way that we typically check compliance on them is by running many signals which we call high-capacity simulation, and by many I mean like millions and tens of millions of bits. We're looking to see how many of those bits actually get transferred correctly. So when you go to the PCI-SIG, the special-interest group, they have a bit error rate test that they do with hardware. Well we can do the same sort of bit error rate testing with software. Our signal integrity software supports a high-capacity simulation and then lets you look at the eye diagram and just like with PCI-SIG we have that compliance test built into our software.

There are a couple of really interesting things about what's happening in this space. One is the most popular serial interface by far, which is PCI express. We've been at PCIe 3.0 for a few years now, and that's an 8 Gb/s interface. Most people here at DesignCon are talking about up to 28 or 56 Gb/s, so 8 is a little bit behind the bleeding edge at this point. But what's going to be happening this year is PCI-SIG is going to approve the 4.0 spec, which is moving it to 16. Still maybe not on the bleeding edge, but doubling the data rate is very significant. One of the cool things we're showing in our booth is if someone who is using 8 Gb/s today wants to see if their same hardware will support a 16 Gb/s data transfer, we can help them check that feasibility. It's really quite interesting because you can see by default the answer is probably no, the eye is going to be closed and you're not going to meet your bit error rate testing. But because these transceivers and receivers have such advanced equalization in them we have what's called algorithmic models that sit on both sides, transmitter and receiver, and this is the same type of stuff we're going to see in devices that come out and support PCIe 4.0. We can turn on a level of equalization and see if when we boost that signal if we can open up that eye and see if it's going to meet those compliance requirements that are going to be associated with doubling the date rate from 8 to 16.

That's a pretty interesting thing that's going to be happening in 2015. But one other thing I just wanted to throw in is when we talked about LPDDR4, that data rate is actually going to go up to as high as 4266, so that's going to be working in a similar way that serial links were working about two or three years ago. The same equalization that you needed in serial links a few years ago are going to be needed in memory interfaces this year. We will support that with our algorithmic modeling interface. We can actually show today AMI modeling associated with DDR4 and LPDDR4 as well as, of course, serial links. It's just tremendously interesting and exciting with all this different technology that we get data passed across the ether into the cloud as fast as possible. All this stuff is really exciting, and the fact that we're able to analyze this and help customers get to market right the first time is what we're really excited about at Cadence, and the Allegro technology is providing that link to getting the product done right the first time.

KD: Thanks for taking the time to talk with me today, Brad.

BG: Thank you, Kelly. **PCBDESIGN**

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News Highlights

Over a Dozen RoHS Exemptions Requested

IPC, in conjunction with an international industry stakeholder group, applied for more than a dozen exemption extension requests under the European Union (EU) RoHS Directive. The RoHS2 Directive dictates expiration dates for all exemptions granted and several critical to the electronics manufacturing industry are set to expire in 2016.

A Cautionary Tale: Counterfeit Materials

John Ling of EIPC writes, "Risk from counterfeits wears many hats. There is reputational risk, which can be damaging; there is inherent safety risk, which could be fatal; and there is financial risk to the OEM, the PCB manufacturer, and the PCB broker. One way of minimising risk is by dealing direct."

FTG Secures New Agreement with Rockwell Collins

The agreement incorporates a variety of technologies for use on major airframe platforms across business regional, air transport and government systems market applications.

It's Only Common Sense: Saving the Military PCB Market

The DoD has to come to its senses and start working with the sub-$20 million well-qualified board shops. These shops have been the backbone of the American PCB industry since its inception. It must work with them and support them, making sure they pay prices that are fair enough for them to stay in business.

New Defense PCB Regulations Take Effect December 30

Changes to the U.S. Munitions List, which is regulated through the International Traffic in Arms Regulations, states that PCBs "specially designed" for defense-related purposes will be controlled under USML Category XI. Additionally, any designs or digital data related to "specially designed" PCBs will be controlled as technical data.

2015 Global Aerospace and Defense Industry to Rise

"The commercial aerospace sector is expected to set new records for aircraft production in 2015. The accelerated replacement cycle of obsolete aircraft with next generation fuel-efficient aircraft, and growing passenger travel demand, especially in the Middle East and the Asia-Pacific region are key drivers behind this trend," said Tom Captain, Deloitte Global Aerospace and Defense Sector Leader.

IDTechEx Sees Rapidly Changing $7.5B Market for Drones

Dr. Harrop, Chairman of IDTechEx says, "The biggest market sub-sector will be small UAVs that are not toys or personal, with $2 billion in sales in 2025 generating over $20 billion in benefits to agriculture, border protection, parcel delivery, logistics such as warehousing, coastguard, customs, search and rescue, medical emergency, malaria research, mine detection, protection of rare species, movie production and so on."

DARPA Boosts Investment in LRASM Program

Initiated in 2009 in collaboration with the U.S. Navy and U.S. Air Force, DARPA's Long Range Anti-Ship Missile (LRASM) program has been investing in advanced technologies to provide a leap ahead in U.S. surface warfare capability.

DARPA to Put Fab Lab at Navy Ship Maintenance Center

High-tech fabrication facility aims to enhance ship maintenance and repair by enabling more cost-effective training and rapid onsite production of parts and components.

Camtek Secures First Conditional Order for Gryphon

Camtek Ltd. announced that it has received a conditional purchase order from Bay Area Circuits Inc. for a Gryphon system. The purchase order will become firm upon successful completion of an evaluation process.

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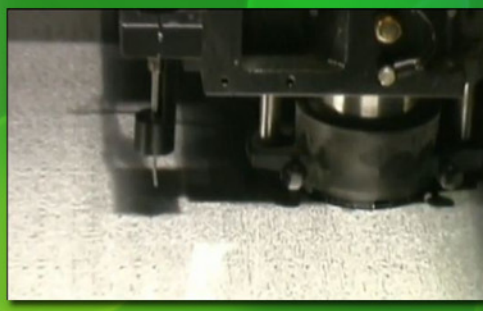

Multilayer Technology
3835 Conflans Rd
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ITAR

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Split Planes in Multilayer PCBs

by Barry Olney
IN-CIRCUIT DESIGN PTY LTD

Creating split planes or isolated islands in the copper planes of multilayer PCBs at first seems like a good idea. Today's high-speed processors and FPGAs require more than six or seven different high-current power sources. And keeping sensitive analog circuitry isolated from those nasty, fast, digital switching signals seems like a priority in designing a noise-free environment for your product. Or is it?

Many analog-to-digital converter (ADC) manufacturers recommend the use of split ground planes. "The analog ground (AGND) and digital ground (DGND) pins must be connected together externally to the same low impedance ground plane with minimum lead length." This has been the age-old method for audio design. However, this approach has the potential of creating a number of additional problems in high-speed digital circuits. A much better way to connect AGND and DGND together, through a low impedance path, is to use only one ground plane to begin with.

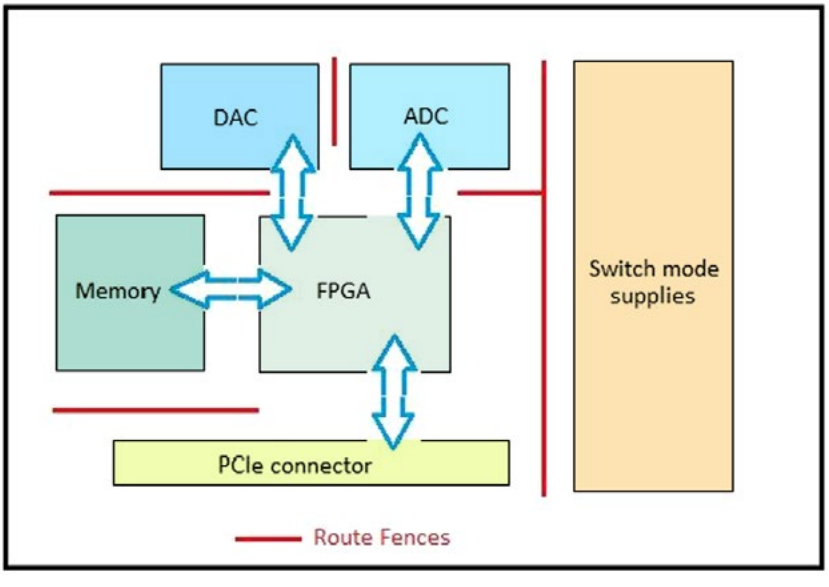

Figure 1: Route fences used to control routing and isolation.

When both analog and digital devices are used on the same PCB, it is usually necessary to partition (not split) the ground plane. The components should be grouped by functionality and positioned so that no digital signals will cross over the analog ground, and no analog signals will cross over the digital ground. Precise partitioning will minimize the trace lengths, improve signal quality, minimize the coupling and reduce radiated emissions and susceptibility. This is traditionally done by using keep-out zones whereby no trace can cross through the keep-out area. But this also creates issues in that control signals need to go into and out of these sensitive areas.

Particular care needs to be taken with oscillators and switch mode power supplies that may generate high frequency electromagnetic fields. If space permits, keep these circuits 10mm from any critical signals to avoid parasitic coupling.

Route fences, rather than route keep-outs, are useful to control the routing. Controlled routing is the key to a successful mixed signal design. The planes should not be split, but rather a pass-through gap is left in the plane so that control signals can enter and leave that area as seen in Figure 1. Route fences are also very effective is controlling an autorouter. They can be set up for each router pass and then moved to a different location. This is best done with interactive cross-probing from schematic to PCB, controlling functional sections of the design one-by-one, building up the route to completion.

At low frequencies, current follows the path of least resistance. But at high frequencies, return current follows the path of least inductance—which happens to be directly under the signal trace on a plane (power or ground) that is closest to

2015 Programs

April 29–30
IMPACT 2015: IPC ON CAPITOL HILL
Washington, DC, USA

May 13–14
IPC Technical Education
Fort Worth, TX, USA

Professional development courses for engineering staff and managers:
- DFX-Design For Excellence (DFM, DFA, DFT and more)
- Best Practices in Fabrication
- Advanced Troubleshooting

June 9
ITI & IPC Conference on Emerging & Critical Environmental Product Requirements
Fort Lee, NJ, USA

June 9–10
IPC Technical Education
Chicago, IL, USA

Professional development courses for engineering staff and managers:
- DFX-Design For Excellence (DFM, DFA, DFT and more)
- Best Practices in Fabrication
- Advanced Troubleshooting

June 10
ITI & IPC Conference on Emerging & Critical Environmental Product Requirements
Des Plaines, IL, USA

June 12
ITI & IPC Conference on Emerging & Critical Environmental Product Requirements
Milpitas, CA, USA (San Jose area)

September 27–October 1
IPC Fall Standards Development Committee Meetings
Rosemont, IL, USA

Co-located with SMTA International

September 28
IPC EMS Management Meeting
Rosemont, IL, USA

October 13
IPC Conference on Government Regulation
Essen, Germany

Discussion with international experts on regulatory issues

October 13–15
IPC Europe Forum: Innovation for Reliability
Essen, Germany

Practical applications for meeting reliability challenges like tin whiskers, with special focus on military-aerospace and automotive sectors

October 26–27
IPC Technical Education
Minneapolis, MN, USA

Professional development courses for engineering staff and managers:
- DFX-Design For Excellence (DFM, DFA, DFT and more)
- Best Practices in Fabrication
- Advanced Troubleshooting

October 28–29
IPC Flexible Circuits-HDI Conference
Minneapolis, MN, USA

Presentations will address Flex and HDI challenges in methodology, materials, and technology.

November 2–6
IPC EMS Program Management Training and Certification
Chicago, IL, USA

November 4
PCB Carolina 2015
Raleigh, NC, USA

December 2–3
IPC Technical Education
Raleigh, NC, USA

Professional development courses for engineering staff and managers:
- DFX-Design For Excellence (DFM, DFA, DFT and more)
- Best Practices in Fabrication
- Advanced Troubleshooting

December 2–4
International Printed Circuit and APEX South China Fair (HKPCA & IPC Show)
Shenzhen, China

Questions? Contact IPC registration staff at registration@ipc.org or +1 847-597-2861

SPLIT PLANES IN MULTILAYER PCBS *continues*

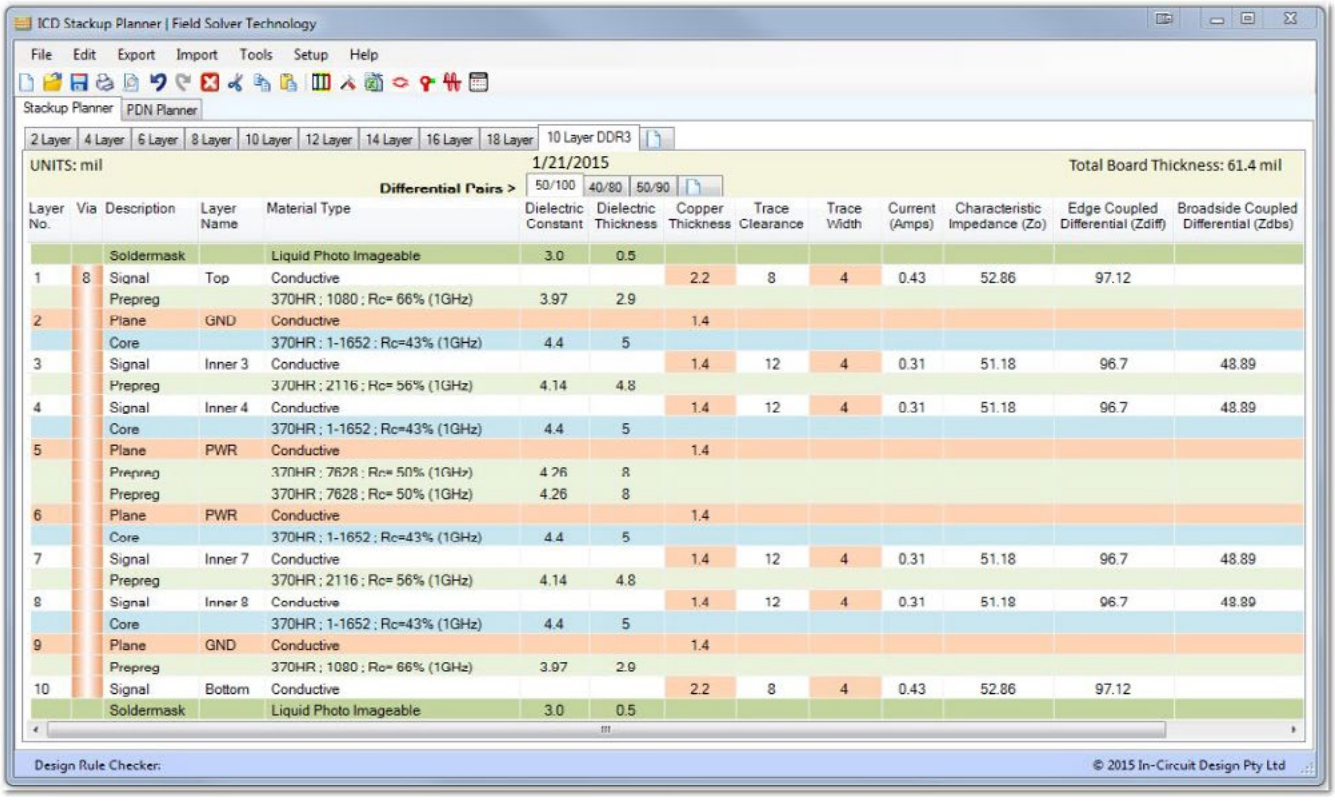

Figure 2: A 10-layer DDR3 stackup.

the trace. This also provides the smallest loop area.

When a trace crosses a gap in the adjacent plane, the return current is diverted from underneath the trace in order to go around the gap. This causes the current to flow through a much larger loop area which changes the characteristic impedance of the trace, increases the crosstalk between adjacent traces, and thus increases the radiation from the board. In some instances, the return current may have to go all the way back to the power supply. A major EMC problem occurs when there are discontinuities in the current return path. Routing traces via the pass-through gap alleviates these problems and still allows vital signals to enter and leave the sensitive area. The return current will always follow the signal traces and will not go through other areas.

Also, there is the issue of what to do with all the different power supplies for the major chips without splitting the planes. These days, it is typical to have six or more different supplies. In fact, a DDR3 motherboard that I just completed had a count of 30 different supplies plus an analog and a digital ground. On a complex multilayer board, it is typical to use eight or more layers, four of these being planes.

Figure 2 shows how the ICD Stackup Planner was used to calculate the impedance of the traces and to plan the stackup of the PCB substrate using multiple supplies. This may at first look unusual for DDR3 design, but the addition of copper pours on the dual stripline layers changes everything. Power planes are on layers 5 and 6 and are also placed as pours under the chips on the top and bottom layers. However, pouring copper over the entire outer layers is not recommended. With this particular design, ground pours were added to layers 4 and 7 under the DDR3 devices, to drop the impedance in these areas to 40/80 ohm single-ended/differential. Figure 3 shows layer 4 as GND and the impedance has been altered to 40/80 ohms with the addition of this plane under the DDR3 devices. This also provides good planar capacitance and stability for the 1.5V power distribution network (PDN).

UNITS: mil | 1/21/2015 | Total Board Thickness: 62.8 mil

Differential Pairs > 50/100 | 40/80 | 50/90

Layer No.	Via	Description	Layer Name	Material Type	Dielectric Constant	Dielectric Thickness	Copper Thickness	Trace Clearance	Trace Width	Current (Amps)	Characteristic Impedance (Zo)	Edge Coupled Differential (Zdiff)	Broadside Coupled Differential (Zdbs)
		Soldermask		Liquid Photo Imageable	3.0	0.5							
1	8	Signal	Top	Conductive			2.2	8	4	0.43	52.86	97.12	
		Prepreg		370HR ; 1080 ; Rc= 66% (1GHz)	3.97	2.9							
2		Plane	GND	Conductive			1.4						
		Core		370HR ; 1-1652 ; Rc=43% (1GHz)	4.4	5							
3		Signal	Inner 3	Conductive			1.4	12	4	0.31	40.76	80.75	
		Prepreg		370HR ; 2116 ; Rc= 56% (1GHz)	4.14	4.8							
4		Plane	GND	Conductive			1.4						
		Core		370HR ; 1-1652 ; Rc=43% (1GHz)	4.4	5							
5		Plane	PWR	Conductive			1.4						

Figure 3: Impedance altered to 40/80 ohms by pours under the DDR3 devices.

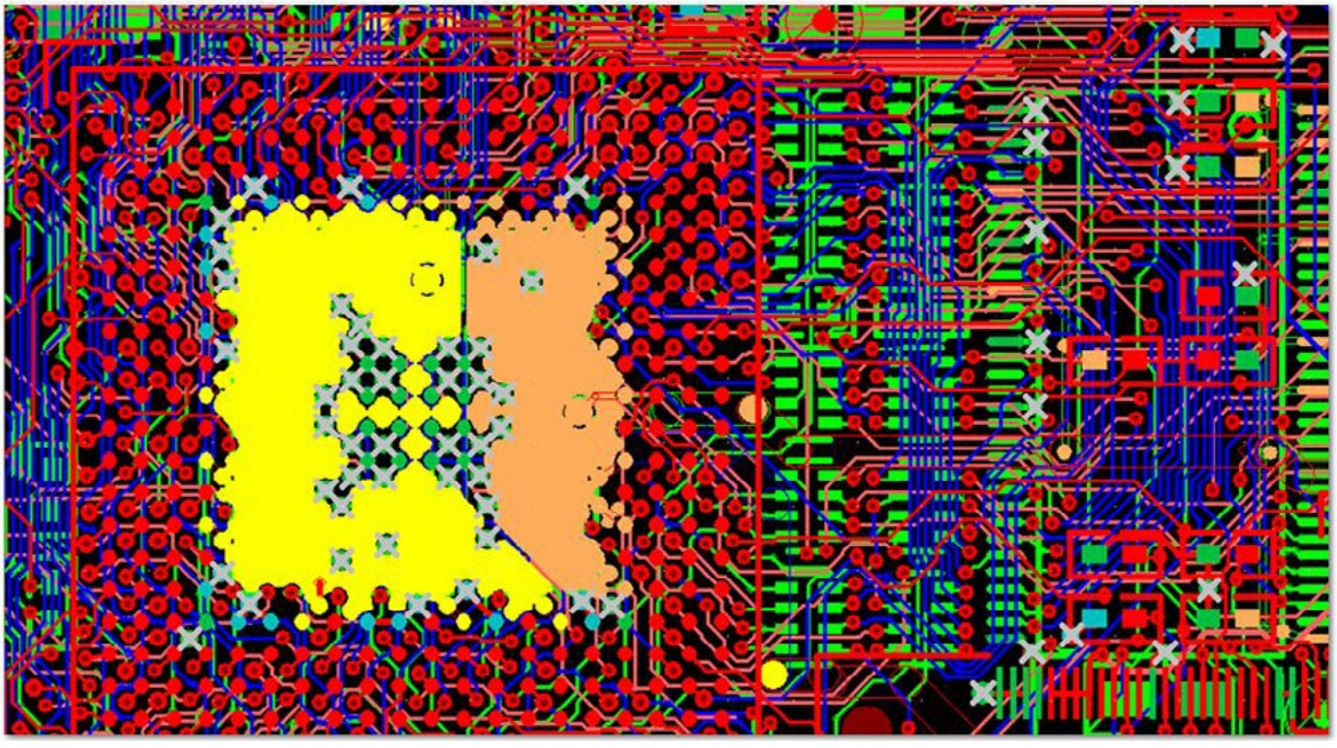

Figure 4: Supplies routed directly under the IC on the top layer.

One of the keys to determining the optimal PCB stackup is to understand how and where the return signals actually flow. The schematic only shows the signal path whereas the return path is implicit. The ICD Stackup Planner allows the designer to determine any number of single-ended and differential impedance technologies on the same substrate. In Figure 3, I have simulated 50/100 (digital), 40/80 (DDR3) and 50/90 ohm (USB) on the same substrate.

It is recommended to use as many GND planes as possible in the stackup. The decoupling capacitor and IC GNDs naturally provide stitching vias to connect the GND planes in most cases. However, any plane, not just ground, can act as the return path of a signal. Care must be taken to ensure there is a provision for enough decoupling between the power and ground planes, in this case. But still, even after putting as many supplies as possible on the power planes, without doubling up, we soon run out of planes. So what do we do with the other supplies?

In the above screenshot of Figure 3, 1V8

(yellow) and 2V5 (orange), supplies are routed on the top layer and the core fills (copper pours) are placed directly under the processor chip. Since there is little room for routing on the top (or bottom) layer anyway, this does not affect the routability of the design but rather has the added advantage of a low inductance power supply close to the chip.

In conclusion, split ground planes are a great way to create discontinuities of impedance, crosstalk and EMI—so, don't use them! Controlled routing is the key to a successful mixed signal design. The ground planes should not be split, but rather partitioned and a pass-through gap left in the plane so that vital signals can enter and leave the sensitive area.

Points to Remember

- The best way, to connect AGND and DGND together through a low impedance path, is to use only one ground plane to begin with.
- When both analog and digital devices are used on the same PCB, it is usually necessary to partition (not split) the ground plane.
- Keep-outs create issues in that control signals need to go into and out of these sensitive areas.
- If space permits, keep these circuits 10 mm from any critical signals to avoid parasitic coupling.
- Route fences, rather than route keep-outs, are useful to control the routing.
- The planes are not split but rather a pass-through gap is left in the plane so that control signals can enter and leave that area. Route fences are also very effective is controlling an autorouter.
- At low frequencies, current follows the path of least resistance. But at high frequencies, return current flows the path of least inductance—which happens to be directly under the signal trace on a plane (power or ground) that is closest to the trace.
- When a trace crosses a gap in the adjacent plane, the return current is diverted from underneath the trace in order to go around the gap. This causes the current to flow through a much larger loop area.
- A major EMC problem occurs when there are discontinuities in the current return path. Routing traces via the pass-through gap alleviates these problems and still allows vital signals to enter and leave the sensitive area.
- Pouring copper over the entire outer layers is not recommended.
- One of the keys to determining the optimal PCB stackup is to understand how and where the return signals actually flow. The schematic only shows the signal path, whereas the return path is implicit.
- The ICD Stackup Planner allows the designer to determine any number of single-ended and differential impedance technologies on the same substrate.
- Use as many GND planes as possible in the stackup. The decoupling capacitor and IC GNDs naturally provide stitching vias to connect the GND planes in most cases.
- Supplies may be routed on the top layer and the core fills (copper pours) are placed directly under the processor chip.
- Split ground planes are a great way to create discontinuities of impedance, crosstalk and EMI—so, don't use them! **PCBDESIGN**

References

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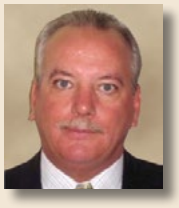
2. Howard Johnson: High-Speed Digital Design—A Handbook of Black Magic.

3. Henry Ott: Electromagnetic Compatibility Engineering.

4. The ICD Stackup and PDN Planner: www.icd.com.au.



Barry Olney is managing director of In-Circuit Design Pty Ltd (ICD), Australia. This PCB design service bureau specializes in board-level simulation, and has developed the ICD Stackup Planner and ICD PDN Planner software. To read past columns, or to contact Olney, click here.

TOP TEN

Highlights from PCBDesign007 this Month

1 Gary Ferrari Wins IPC Hall of Fame Award

Gary Ferrari, director of technical support for FTG Corporation, has been awarded the highest level of recognition that IPC can give to an individual, the Raymond E. Pritchard Hall of Fame Award. The award is given to an individual in recognition of the highest level of achievement, extraordinary contributions and distinguished service to IPC and the advancement of the electronics industry.

2 Mentor Graphics Acquires Tanner EDA

Mentor Graphics Corp. has acquired the business assets of Tanner EDA, a leading tool provider for the design, layout and verification of analog/mixed-signal (AMS) and MEMS integrated circuits. With this acquisition, more designers will now have access to Tanner's AMS products based on the strength and reach of the Mentor Graphics global sales organization.

3 Sunstone Circuits Chooses InSight Software

Sunstone Circuits has purchased Orbotech's InSight PCB pre-sales and pre-engineering software. InSight PCB is a web-based tool for managing and assessing incoming customer PCB data for salespeople and engineers who are not CAM experts. The result is faster and more accurate quoting and product engineering, and increased throughput.

4 Complete Coverage of IPC APEX EXPO 2015

I-Connect007's complete coverage of this year's IPC APEX EXPO is now online. For those of you who weren't able to visit this year's event, tune in to RealTime with... IPC to watch I-Connect007's interviews with many of the industry's movers and shakers.

5 Zuken, SiSoft Collaborate on Multi-gigabit Design and Analysis Solutions

Zuken and SiSoftTM have united to deliver solutions for complex high-speed designs and multi-gigabit applications. By integrating SiSoft's advanced signal integrity solutions for state-of-the-art, high-speed digital system design with Zuken's 3D multi-board, system-level platform, the two companies will provide a combined design and verification flow.

6 Mentor Graphics Joins CPES

Mentor Graphics Corporation has joined the Center for Power Electronics Systems (CPES) at Virginia Tech, the industry consortium dedicated to improving electrical power processing and distribution across various systems.

7 Altium Updates its Flagship PCB Design Tool

The next update to Altium's flagship PCB design tool, Altium Designer 15.1, will introduce several new features for improved design productivity, documentation outputs, and high-speed design efficiency. Altium Designer 15.1 also enhances the core philosophy of the software, with a continued focus on improved design productivity and efficiency.

8 Zuken Schedules Innovation World 2015 Customer Events

Zuken has announced the locations and dates for its popular Zuken Innovation World conferences. The conferences launch in Germany in May, moving around Europe and North America, before landing in Japan in October. Registration is now open for most events.

9 Mentor Posts Record Q4, FY15 Results

Mentor Graphics Corporation today announced financial results for the company's fiscal fourth quarter ended January 31, 2015. The company reported revenues of $439.1 million, non-GAAP earnings per share of $1.09, and GAAP earnings per share of $0.96. For the full fiscal year, revenues were $1.244 billion, non-GAAP earnings per share were $1.77, and GAAP earnings per share were $1.26.

10 IPC APEX EXPO Selects Best Tech Paper

Taking top honors, the winning paper is "High-Frequency Loss Test Methods for Laminate Materials Comparison (a High-Density Packaging User Group/HDPUG Project)," by Karl Sauter, Oracle Corporation USA. His co-author was Joseph Smetana, Alcatel-Lucent. The paper was presented at APEX on February 26.

events

For the IPC Calendar of Events, click here.

For the SMTA Calendar of Events, click here.

For a complete listing, check out *The PCB Design Magazine's* event calendar.

Puget Sound Advanced SMT Chapter Tutorial Program
March 17, 2015
Puget Sound, WA

CPCA 2015
March 17-19, 2015
Shanghai, China

Process Optimization and Defect Elimination for PCB Assembly
Webinar: March 18 & 25, 2015

Shining a Light on LED Technology
Webinar: March 19, 2015

Dallas Expo & Tech Forum
March 24, 2015
Plano, Texas, USA

Houston Expo & Tech Forum
March 26, 2015
Stafford, Texas, USA

PUBLISHER: **BARRY MATTIES**
barry@iconnect007.com

PUBLISHER: **RAY RASMUSSEN**
(916) 337-4402; ray@iconnect007.com

SALES MANAGER: **BARB HOCKADAY**
(916) 608-0660; barb@iconnect007.com

MARKETING SERVICES: **TOBEY MARSICOVETERE**
(916) 266-9160; tobey@iconnect007.com

EDITORIAL:
GROUP EDITORIAL DIRECTOR: **RAY RASMUSSEN**
(916) 337-4402; ray@iconnect007.com

MANAGING EDITOR: **ANDY SHAUGHNESSY**
(404) 806-0508; andy@iconnect007.com

TECHNICAL EDITOR: **PETE STARKEY**
+44 (0) 1455 293333; pete@iconnect007.com

MAGAZINE PRODUCTION CREW:
PRODUCTION MANAGER: **MIKE RADOGNA**
mike@iconnect007.com

MAGAZINE LAYOUT: **RON MEOGROSSI**

AD DESIGN: **SHELLY STEIN, MIKE RADOGNA**

INNOVATIVE TECHNOLOGY: **BRYSON MATTIES**

COVER: **RON MEOGROSSI**

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April:
Surface Finishes

May:
Controlled Impedance

June:
IPC Standards Update