

THE **pcb** **design** MAGAZINE

March 2013

AN  I-CONNECT  PUBLICATION

Design for Profitability:
Avoiding Fabrication
Issues and Minimizing
Costly Revisions p.10

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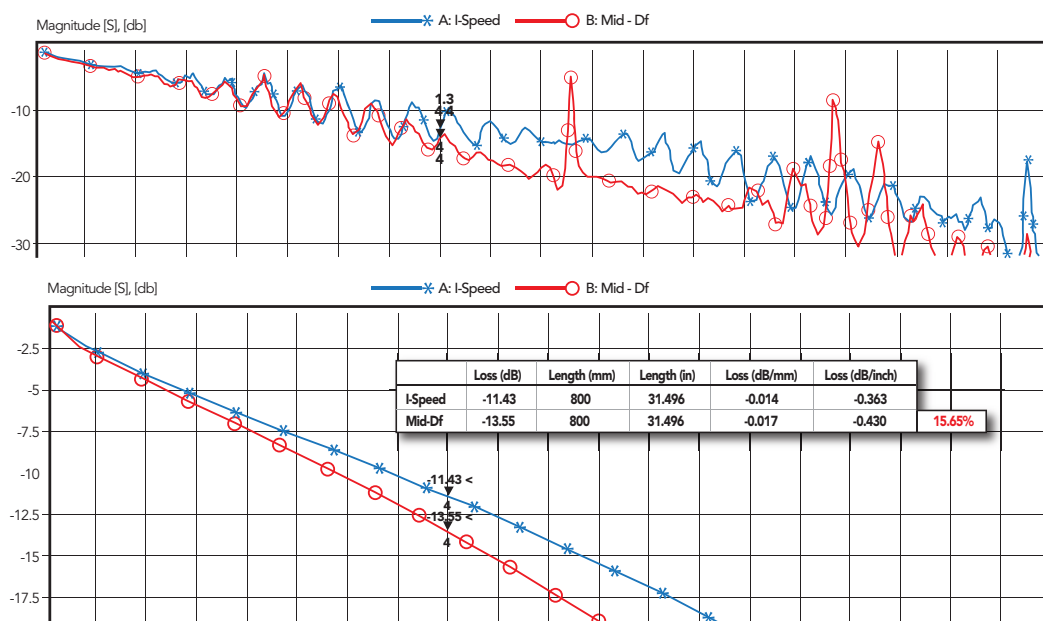
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THIS ISSUE: DFM

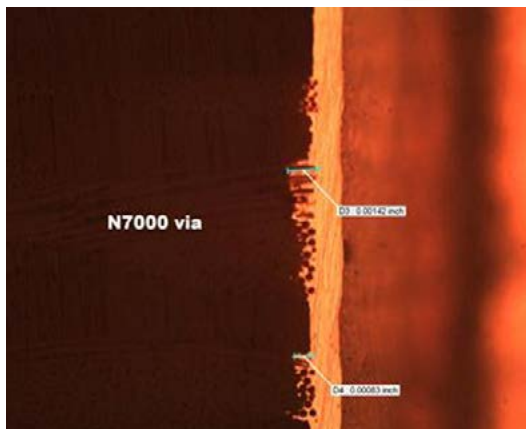
FEATURED CONTENT

Most PCB designers claim to be designing for manufacturability, but CAM engineers tell a different story. This month, our expert contributors discuss many of the DFM challenges they see with incoming PCB designs, and present a variety of options for ensuring manufacturability. Hint: Communication can prevent many DFM snafus.

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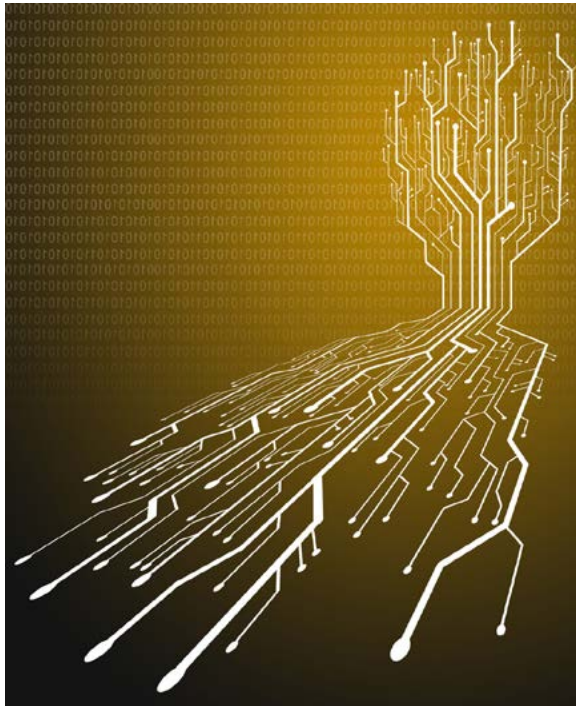
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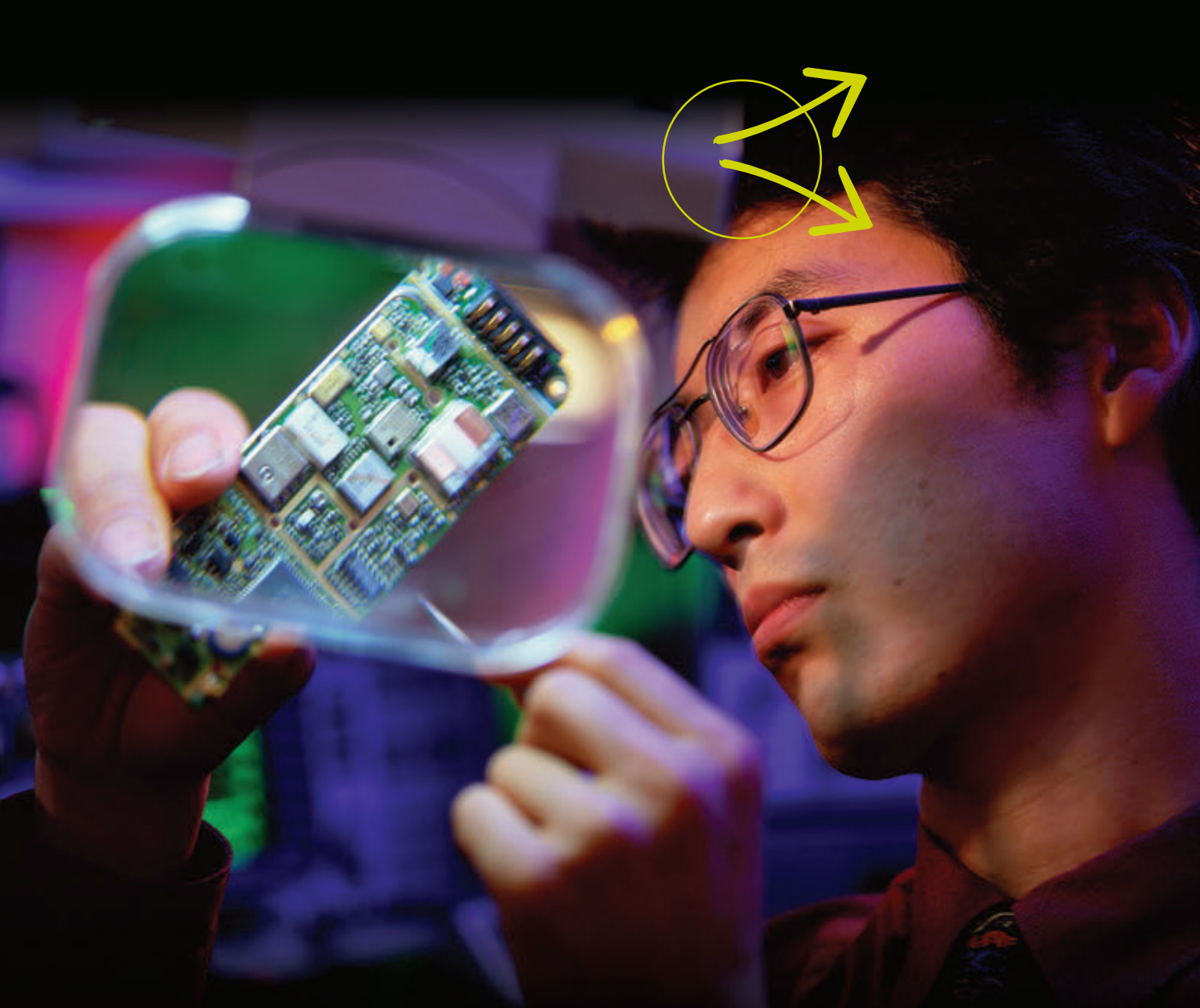
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The State of PCB Design

by Andy Shaughnessy
I-CONNECT007

Once again, it's the season for trade shows and conferences. After attending events like DesignCon and the Designers Forum at IPC APEX EXPO, I can safely say that the state of PCB design is sound...for now. The "graybearding" of the design community continues unabated, but the designers I met with at both shows are as enthusiastic as ever about their careers and electronics in general.

The Designers Forum kicked off the week-long activities at IPC APEX EXPO 2013, much in the way that designers kick off the development of the PCB. And this year, the designers showed up early and stayed late.

IPC Director of Technology Transfer Dieter Bergman got the show under way with a look at IPC's roadmap for design. For the rest of the day, attendees heard presentations from Rick Hartley, L-3 Communications; Ed Acheson, Cadence Design Systems; Daniel TiTuro, TiTuro Consulting; Happy Holden, Gentex; Vern Solberg, Solberg Technical Consulting; Mark Finstad, Flexible Circuit Technologies; and Mark Verbrugge, Pica Manufacturing Solutions.

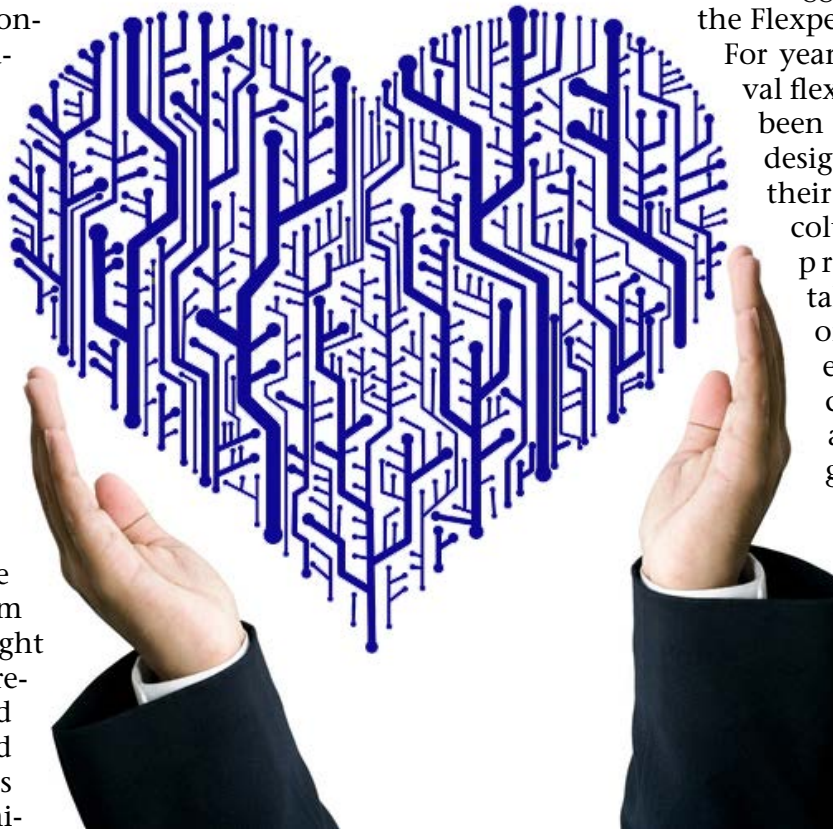
For most of the day, Guest Editor Kelly Dack and I were busy conducting video interviews for our Real Time with...Designers Forum program, but I caught Hartley's lunchtime presentation to a packed room. His talk focused on the risks designers face by accepting semi-

conductor companies' app notes at face value, and he detailed a slew of horror stories to back his premise. Whoa! One particularly bad example wound up costing over \$200 per board, but after a proper redesign, the cost per board dropped by about \$200—scary stuff!

For years, Hartley has been on a campaign to make designers aware of the power they can, and should, wield during the product development process. This year was no different. Hartley urged designers to take the initiative, run all the numbers, and refuse to settle for anything less than perfect. And in a Real Time with...Designers Forum interview, Hartley urged designers and EEs to continue their design education, even if it means shelling out their own money for classes and textbooks that can keep them ahead of the game.

Attendees also gave rave reviews to Finstad and Verbrugge for their "Ask the Flexexperts" discussion.

For years, these two rival flex designers have been answering flex design questions in their "Flexexperts" column, and their presentations take on the air of standup comedy. At a technical conference, a little levity goes a long way. Holden focused on the ever-increasing complexity of designs. What is the limit to the amount of technology



we can squeeze into shrinking amounts of real estate? Solberg discussed the advances and challenges to embedding circuits, including embedded actives. Most PCB fabricators have little experience embedding bare die inside circuit boards, but that's the way technology is heading.

DiTuro, formerly with Honeywell and now a consultant, detailed new approaches to designing for high-reliability PCBs. Ed Acheson offered an update on the vendor-neutral IPC-2581 standard. Now that the first PCB has been fabricated with IPC-2581 data, the members of the IPC-2581 Consortium are focusing on ironing out the final bugs.

Monday evening, the Designers Council's San Diego Chapter held a meeting that drew a crowd that was about as big as the daytime crowd. San Diego PCB's Mike Creeden gave a great presentation on the next generation of PCB designers, or lack thereof. Creeden asked if anyone knew any PCB designers under 30. I think one hand went up.

He made a great point: It's up to us to identify and bring in the "new blood" that will become the senior designers of tomorrow. The best and brightest young people are not likely to find their way into this profession on their own. They'll need to be steered in the right direction.

I like to ask my nephew's friends, fairly intelligent guys in their 20s, what they know about PCB design. Usually, all I get are blank stares. They want to be Web designers or IT guys, or they're considering law school. They get interested when I explain that some designers make good money with little or no college. But as a career, PCB design is not on their radar screen.

So, do you know any designers under 30? How about anyone in fabrication or assembly? If you do, I'd love to hear from you.

Sequestration Trepidation

Almost everyone I spoke with at the Designers Forum and IPC APEx EXPO was optimistic about 2013 and beyond. The only exceptions were the military contractors, who were concerned about the effects of sequestration. For those not paying attention at home, the Budget

Control Act of 2011 stipulated that defense and non-defense discretionary spending would be cut by sequestration if Congress couldn't agree on a better way.

But if you cut to the chase (or go to this [fantastic entry](#) in Wikipedia designed for laymen like me), you'll see that the end-result is that there are no cuts in military spending. What we have is just a reduction in the rate of the increase in spending; military spending will only rise 1.5% per year for the next 10 years. The big worry is that spending increases of 1.5% won't keep up with inflation, which is a pretty accurate worry.

So, we wind up with a cut of about \$55 billion in defense spending per year for 10 years. That's about two aircraft carriers per year. Already, the Pentagon has announced that it can't afford to send a carrier to the Mideast because of financial concerns.

Part of me can't help thinking, "Hey, DoD, just be glad you're getting a budget increase in the first place." But I'd also like for our military to have all the funds necessary to keep our warfighters supplied with the best equipment in the world.

Is there a solution to the DoD's funding blues? We don't want to set up all of our warships with tourist-friendly railings and handicap-accessible bathrooms and start charging \$10 a head for tours, do we? But it might come down to that!

The gridlock in Washington is not likely to dissipate any time soon and the budget fight will probably carry over into the 2014 midterm elections. We can expect to see a drop in military spending on PCBs, but the brunt of it will probably not take effect until next year.

So, the Pentagon is in panic mode, and officials are watching every penny. Welcome to the party, DoD. **PCBDESIGN**



Andy Shaughnessy is managing editor of *The PCB Design Magazine*. He has been covering PCB design for 13 years. He can be reached by clicking [here](#).



Design for Profitability: Avoiding Fabrication Issues and Minimizing Costly Revisions

by Mark Thompson, CID+
PROTOTRON

SUMMARY: *At last, PCB designers are finally realizing the power they wield: They have the power to design profit into the board, or, conversely, increase costs and remove profit from the PCB. In this article I am going to go over a few of the challenges that fabricators routinely face, and present some typical DFP solutions that can affect your bottom line.*

Note that I use the term “design for profitability,” or DFP, as opposed to any of the other acronyms such as DFM (design for manufacturability), DFT (design for test), or DFA (design for assembly). I’m taking this approach because it really all comes down to profit, doesn’t it?

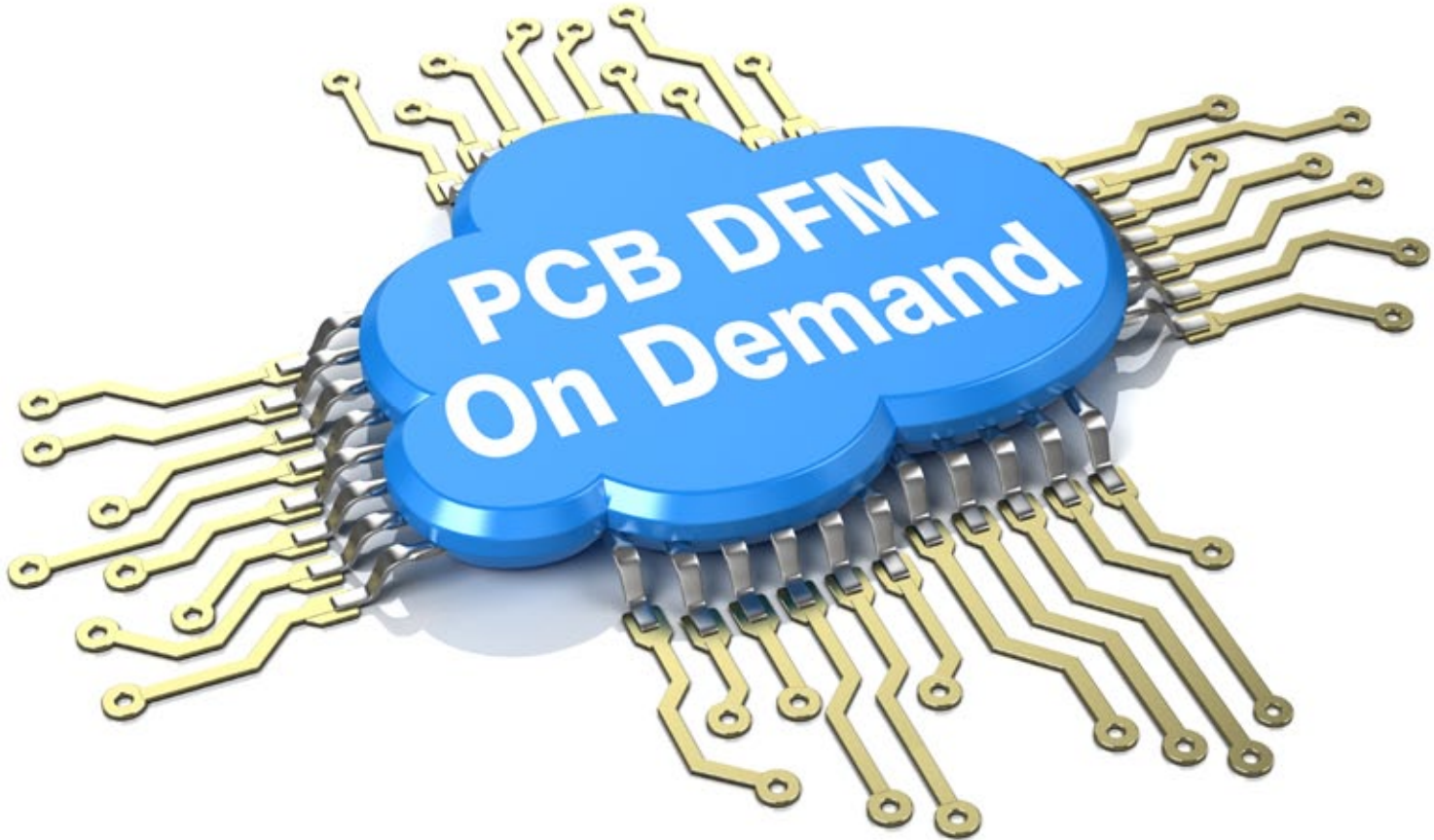
Designers have the power to design profit into the board, or, conversely, inadvertently increase costs and remove profit from the PCB.

In this article I am going to go over just a few of the challenges that fabricators routinely face and some typical solutions, especially solutions that can affect your bottom line.

I will start with DFM. Generally, this is the first stage for prototyping and DFM depends greatly on the capabilities of your chosen fab shop. Some designs are finished with autorouters after the critical traces have been hand-placed. It is at this point that unintended issues can arise between design and fab.

An example of this is same net-spacing violations where a track may “double back” near a surface mounted component, creating same-net spacing violations (Figure 1). Whereas the software does not see these as legit violations because they are same net, a fabricator knows that any features creating spaces below .003” can easily flake off at the image stage and create havoc elsewhere in the form of shorts. Edit time must be taken at the fab stage when these same-net spacing violations occur and the sliv-

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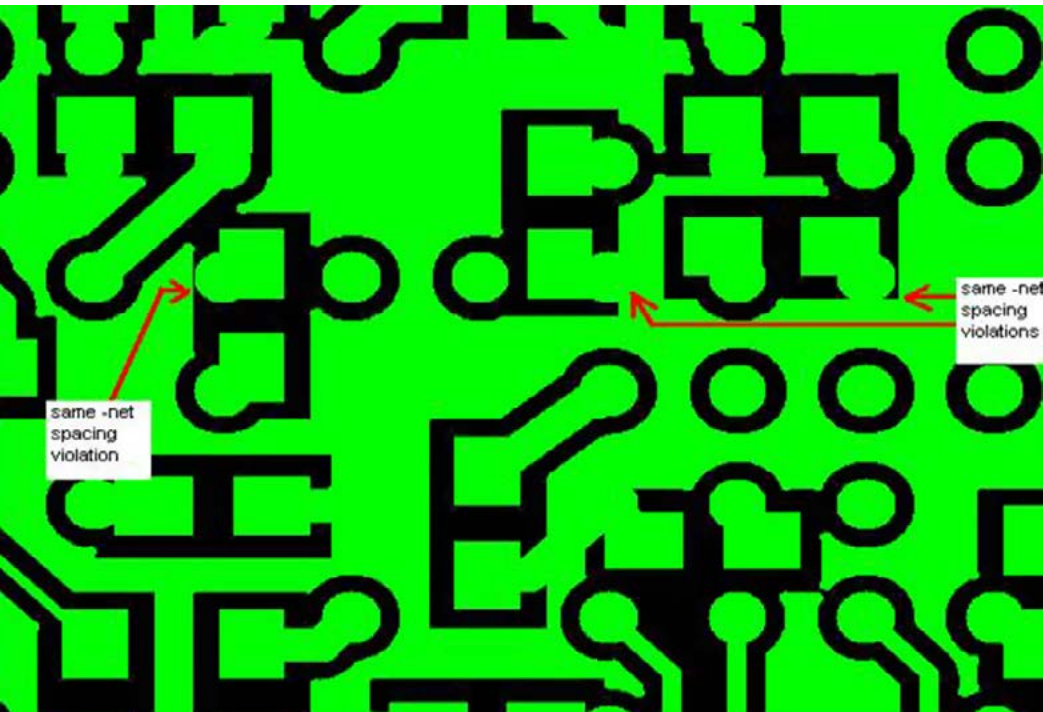


Figure 1: Examples of same-net spacing violations.

ers eliminated. Some CAM software packages have a sliver fill option, but again this requires additional edit time at CAM.

Other high-edit-time potentials are jobs that have been outsourced for design/layout to contractors who use an autorouter for routing non-critical traces. These autorouters are notorious for making silly decisions, such as not centering the trace between pins and creating potential gap violations.

An example of issues that can slow down time-critical jobs: A drawing with a specific call-out for impedances based on metric sizes. Gerber files are typically output in imperial units, in inches. Many times these slight rounding errors mean a phone call is necessary to make sure we are dealing with the correct impedance line sizes.

This brings me to my next point. Many times in my workday, an end-user asks for panelized data from the fabricator and sends this data to other fabricators. The thought process is that with this approach, borders with rails, tooling and fiducial placement have already been established. This is a huge risk and is not at all advised by the fabrication community for the following reasons:

1. The panelized data has been etch-compensated for the known loss at the given fabricator's shop. One fab shop's etch comp may be different from another. Worse yet, fabricators may not be aware they are receiving panel data from another shop, and they may perform an additional etch compensation.


2. Drill compensations: Same problem, as the panelized data may contain the actual working NC drill file with the drill compensations for plating already performed. Fabricators use different compensations and what works for one may not work

for another. In addition, as with image data, if the fab shop is unaware that the panelized data has had drill compensations already performed, they may attempt to add an additional comp, which could result in annular ring or other feature proximity violations.

One way of ensuring that the data is what the customer expects is to send check plots. But again, even check plots can be misunderstood, as typically they are sent after any fabrication mods have been done for both drill and image compensations. From the fabrication standpoint, the purpose of the check plots is to verify things like locations and sizes of additional frame fiducials or tooling holes.

So, how can a designer ensure that the broadest range of fabricators can reliably build their products? Simply design for maximum producibility, allowing for process variances in the design.

Let me give you an example of this philosophy. I get phone calls all the time from customers asking for a minimum annular ring size for a given hole size. From my viewpoint, when maximizing the producibility for the part, my answer is always the same: For signal layers (in-



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DESIGN FOR PROFITABILITY *continues*

ternal and external) make the pad size .010" larger than your desired finished hole size. This allows for .004"-.005" drill compensation (to plate back down to the intended finished hole size) and .002" per side annular ring prior to process to deal with any slight misregistration.

For inner plane layers, obviously a fabricator would like to see more distance between the edge of a plated hole and the adjacent copper pour for plane so they can allow for their machine tolerance and any drill misregistration that may occur. (With today's drill machines, this is less and less of an issue.)

The area of RF circuit design offers plenty of opportunity to design profit into, or out of, the PCB. Let's talk a little bit about creating RF features at a conventional fabricator and go over some common issues we find with artwork provided for RF jobs. First off, the very nature of RF is that the features must be tightly controlled. Typically RF features are done as "constructs" or "islands," because using standard "drawn" features leaves undesirable radii. This means a fabricator must be very careful when attempting an "etch compensation" for the known loss at an etcher based on starting copper weight. All features must be selected on the constructs or they will not perform as expected. Net lists are helpful, but can also cause delays on RF jobs.

Let's look at an example:

If the net list definition assumes a later connection to a surface feature – say, through a metal screw head or plated half-hole (castellation), you can get false open nets that can cause delays.

A good fabricator sees an RF device for what it is and understands certain CAM rules apply. Rules include things like clipping back the metal running to a part edge (assuming no Z-axis connection is to be made). Normally, a shop

may clip metal back anywhere from .004" to .010" so burring does not occur at final rout. Not so on RF type jobs. Trimming the RF leads more than .005" can sometimes result in performance issues, and this is generally not done unless the customer is aware and has approved.

Many RF features themselves can look very much like "stubs" or unterminated traces and some CAM systems may flag them as such. Even on predominantly digital boards, RF features such as antennas can look like stubs or unterminated traces.

Clear solder mask seems to be a favorite of RF engineers who like to verify that their feature geometries are as designed, or WYSIWYG (what you see is what you get). Unlike conventional designs, RF designs have characteristics that require an understanding of the intended performance of the product.

Communication with the customer is key when any modification is being considered. Even the slightest variation in the end product from the design can yield performance issues.

All of these challenges, left unchecked, can lead to costly revisions, missed deadlines, and failure in the field. And all of them could potentially lead to higher product costs. It's up to you, the PCB designer, to design profits in and keep unnecessary costs out.

As always, feel free to contact me with any questions. **PCBDESIGN**

“
For inner plane layers, obviously a fabricator would like to see more distance between the edge of a plated hole and the adjacent copper pour for plane so they can allow for their machine tolerance and any drill misregistration that may occur.
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Mark Thompson is in engineering support at Prototron Circuits. To contact Mark, click [here](#), or call 425-823-7000.

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Electromagnetic Fields: Part 1

by Barry Olney

IN-CIRCUIT DESIGN

SUMMARY: *Our whole world literally revolves around electromagnetic fields. Much insight into high-speed PCB design can be gained by understanding the behavior of transmission lines and the influence of their associated electromagnetic fields.*

Migrating birds, turtles, whales, etc., all use the earth's magnetic field to navigate vast distances. Whales, for instance, can negotiate a 9,000 mile stretch of open, ocean without varying from their course by more than 1 degree. However, one theory for their occasional mass beaching cites the highly magnetic materials on the ocean floor that apparently mislead the whales, pointing them in the wrong direction. According to an [article](#) by environmental writer Larry West, "Mass strandings of dolphins are far less common than mass strandings of whales. And among whales, deep-water species such as pilot whales and sperm whales are more likely to strand themselves on land than whale species such as orcas (killer whales) that live closer to shore."

This phenomenon obviously does not affect birds insulated from the ocean floor by miles of water (and air). And as for turtles, they are also surface dwellers that lay their eggs on the beach, so this may be an advantage for them.

We can glean more information from a [Web presentation](#) by Georgia State University's Department of Physics and Astronomy:

The earth's magnetic field is similar to that of a bar magnet tilted 11 degrees from the spin axis of the earth. The problem with that picture is that the Curie temperature of iron is about 770°C. The earth's core is hotter than that and therefore not magnetic. So how did the Earth get its magnetic field? Magnetic fields surround electric currents, so we surmise that circulating electric currents in the earth's molten metallic core are the origin of the magnetic field... The earth's magnetic field is attributed to a dynamo effect of circulating electric current, but it is not constant in direction. Rock specimens of different age in similar locations have different directions of permanent magnetization. Evidence for 171 magnetic field reversals during the past 71 million years has been reported.

Danish physicist Hans Christian Oersted made great strides in electromagnetic research. During a lecture in 1820, he discovered that electric currents create magnetic fields. He later found that a current-carrying wire created a circular magnetic field around that wire, and that this circular field was strongest closer to the wire.

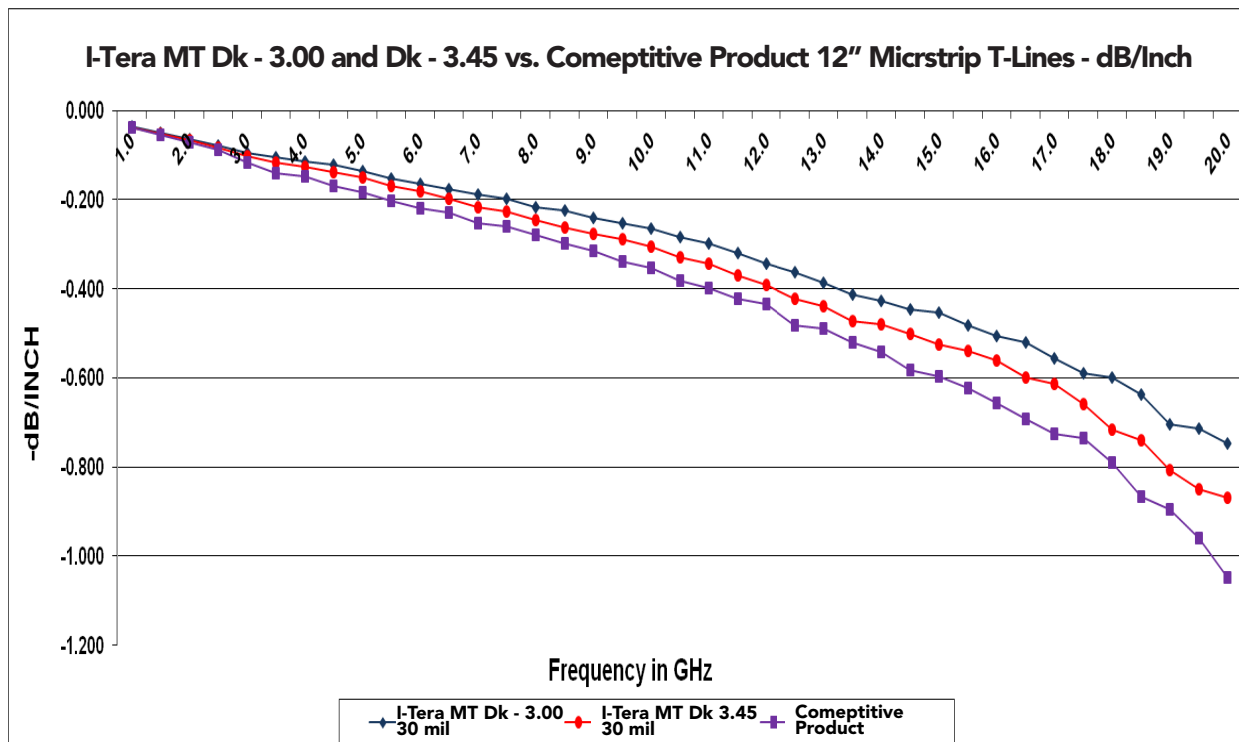
Traces in a multilayer PCB act in much the same way. A current loop produces a field similar to that of Earth, although much smaller of



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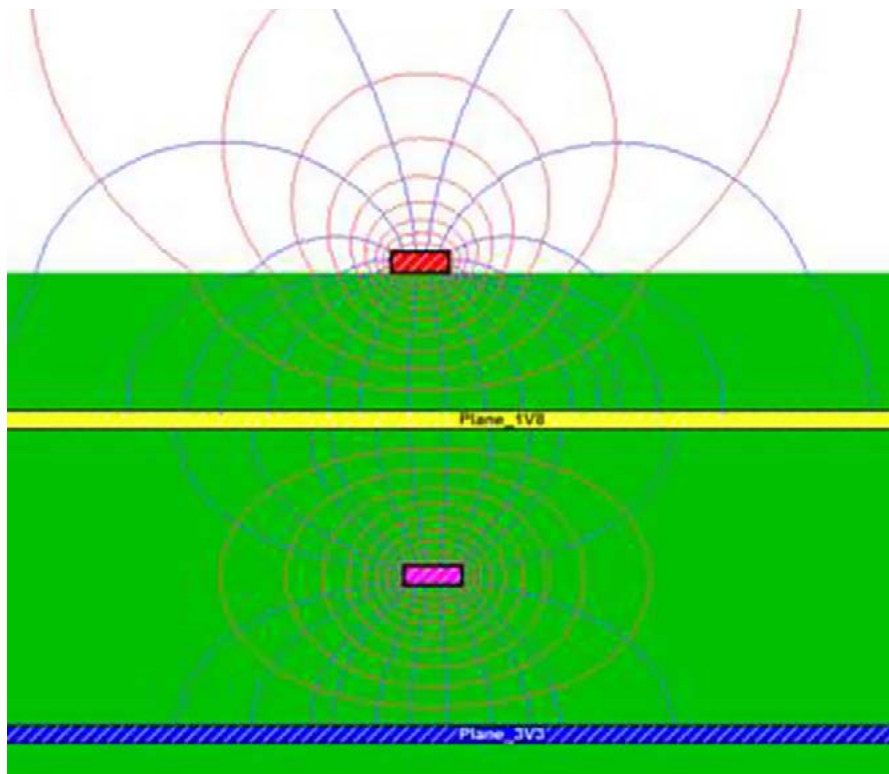
ELECTROMAGNETIC FIELDS: PART 1 *continues*

Figure 1: Electromagnetic fields of traces on a multilayer PCB displayed in HyperLynx.

course. Electromagnetic fields are produced when a logic driver delivers a high-speed, fast rise time pulse into a trace. The electromagnetic wave propagates down the length of the trace radiating into the surrounding dielectric material and coupling energy to nearby trace segments. These electromagnetic fields are not restricted to the multilayer substrate and if proper care is not taken, they may emit radiation causing electromagnetic interference.

A stripline configuration (traces embedded between planes) contains this radiation very well, but microstrip (outer layer traces) tend to emit high levels of radiation. This can be seen in Figure 1. Notice how the fields do not cross the plane layers. So, each microstrip and each stripline configuration is totally isolated from the layers above or below.

That is why high-speed, critical signals should always be routed between two planes in a stripline configuration. I discussed this in detail in a past column, [Beyond Design: Embedded Signal Routing](#). I wrote: “Routing high-speed signals embedded between the planes re-

duces the radiated emissions by as much as 10 dB. Adding a series terminator may help reduce this even further, but this should be determined by simulation and there has to be a trade-off with other factors as in any design.”

In Figure 1, electric field lines are plotted in blue. These can be thought of as the “lines of force.” Note that they begin and end on conductor surfaces (where physical charges reside). They refract (i.e., change direction) at boundaries between different dielectrics. Electric fields, which capacitively couple current into a nearby trace, are somewhat absorbed by the plane but still tend to radiate noise outward.

Magnetic fields are plotted in red. These existed in circular form around the trace

along which the electric potential (i.e., voltage) is a constant. They form closed contours around one or more conductors, and refract at dissimilar dielectric boundaries and couple voltage inductively into a nearby trace. The inductance of the trace depends on the geometry of the circuit and the magnetic properties of the media containing the field.

The differential pair in Figure 2 illustrates the electromagnetic field coupling between the two trace segments. Magnetic fields tend to radiate into air, which is actually just another dielectric with a dielectric constant of one.

Crosstalk is caused by capacitive and inductive coupling:

- Capacitive coupling causes signal voltages to couple current into nearby nets. This is also referred to as forward or far-end crosstalk (FEXT).
- Inductive coupling causes signal currents to couple voltage into nearby nets. This is also referred to as backward or near-end crosstalk (NEXT).

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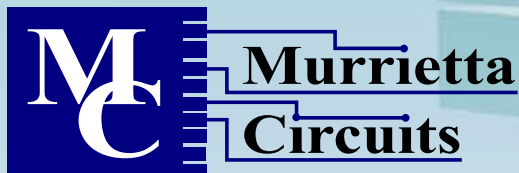
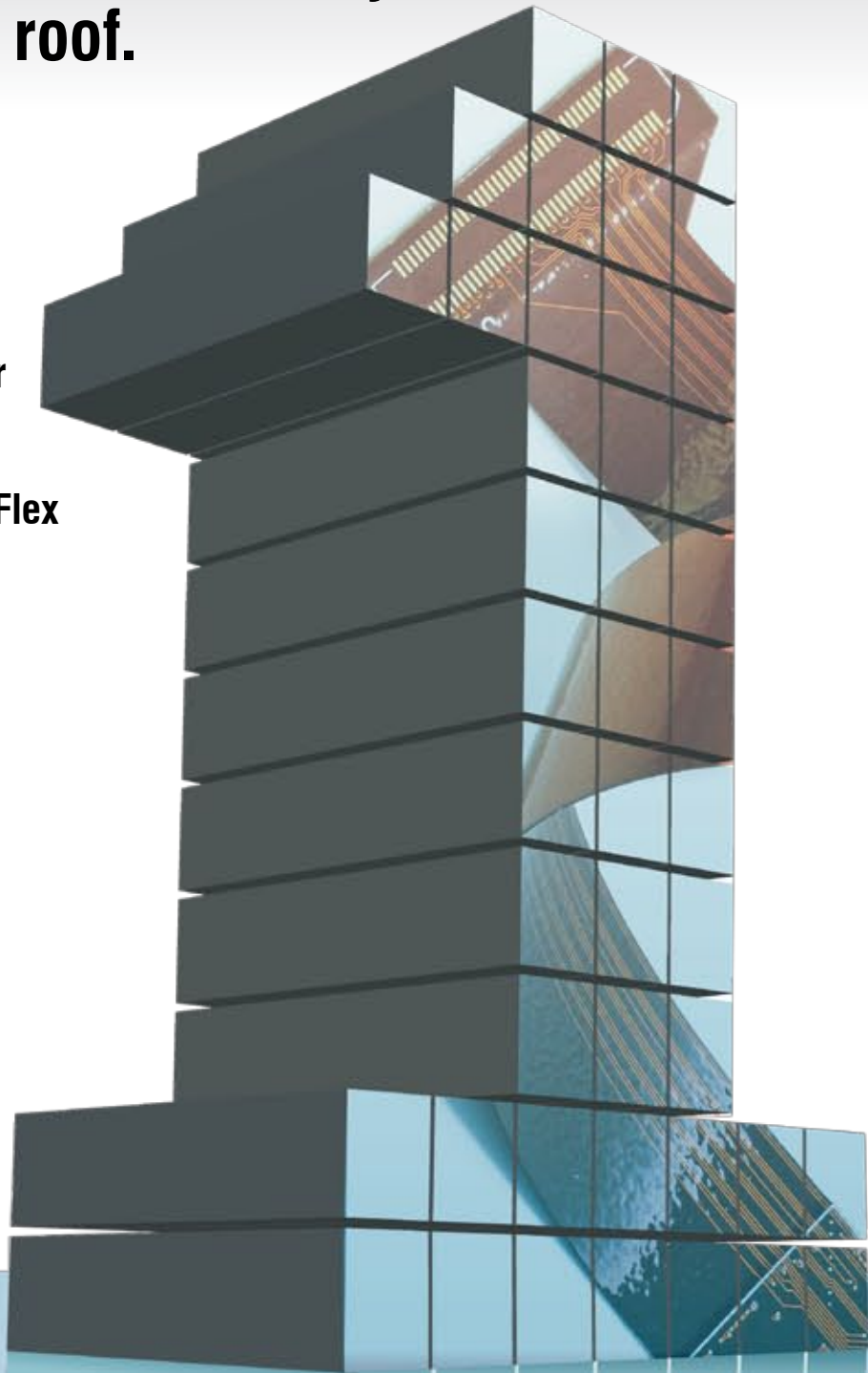
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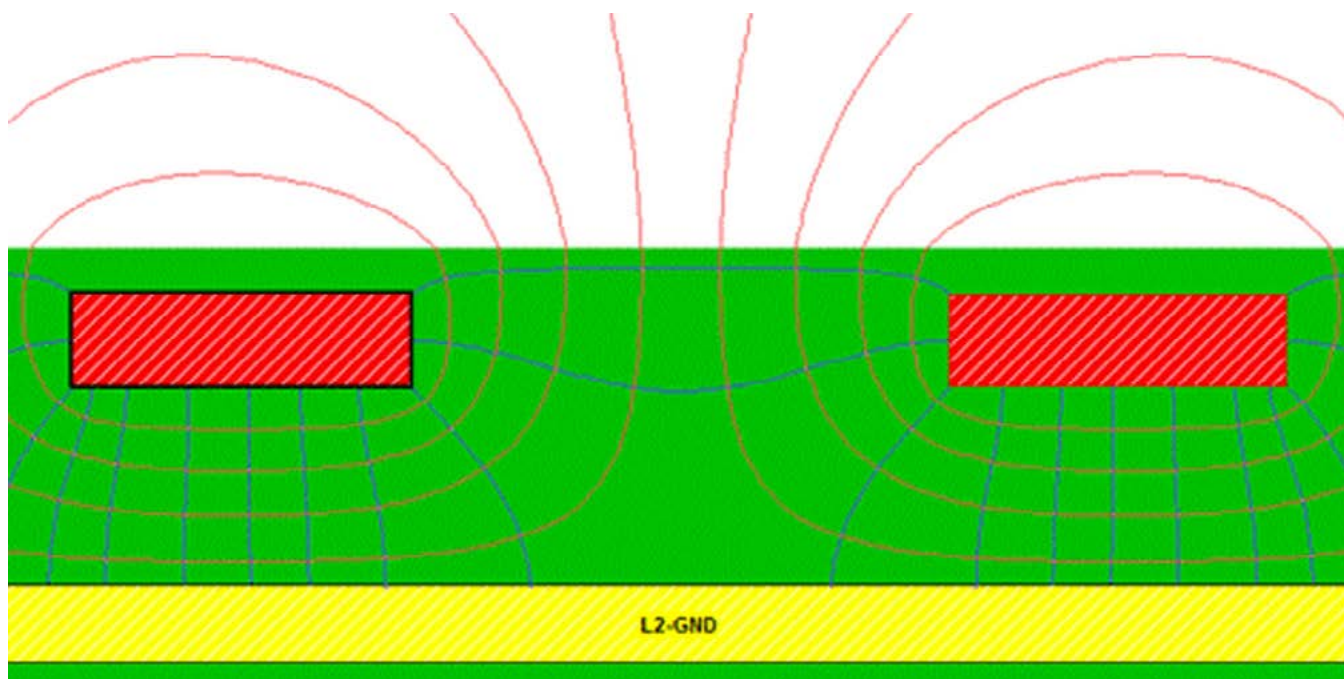
ELECTROMAGNETIC FIELDS: PART 1 *continues*

Figure 2: Microstrip differential pair coupling.

Points to remember:

- Our whole world literally revolves around electromagnetic fields. Migrating birds, turtles, and whales all use Earth's magnetic field to navigate vast distances.

- The earth's magnetic field is attributed to a dynamo effect of circulating electric current in the core.

- Electromagnetic fields are produced when a logic driver delivers a high-speed, fast rise time pulse into a trace. The electromagnetic wave propagates down the length of the trace radiating in to the surrounding dielectric material and coupling energy to nearby trace segments.

- In a multilayer board, each microstrip and each stripline configuration is totally isolated from the layers above or below.

- Electric fields, which capacitively couple current into a nearby trace, are somewhat absorbed by the plane but still tend to radiate noise outward.

- Magnetic fields refract at dissimilar dielectric boundaries and couple voltage inductively into a nearby trace.

Part 2 of "Beyond Design: Electromagnetic Fields" continues next month and in it, we will

look at how electromagnetic fields influence transmission lines and how they can be applied to a BEM field solver. **PCBDESIGN**

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2. [Beyond Design: Embedded Signal Routing](#) – Barry Olney
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6. National Geographic Jan-Feb 2013
7. The ICD Stackup and PDN Planner can be downloaded from www.icd.com.au



Barry Olney is managing director of In-Circuit Design Pty Ltd (ICD), Australia. The company is a PCB design service bureau that specializes in board-level simulation, and is the developer of the ICD Stackup Planner and ICD PDN Planner software.

To contact Barry [click here](#).



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[Apple Gets Down to It, Targets China's PCB Fabs](#)

The report mentions how Apple, after a long period of reluctance and resistance, finally overcame their original state of denial and began to communicate with the environmental NGOs, as well as comprehensively follow-up on the questions raised by the NGOs about their supply chain pollution problems.

[TTM Technologies Inks LOI for SYE, DMC Plants](#)

TTM Technologies, Inc., a major global PCB manufacturer, has signed a letter of intent with its minority partner, Shengyi Technology Co. Ltd. (Sytech), to dispose of TTM's 70.2% equity interest in the SYE plant and to acquire Sytech's 20% equity interest in the DMC plant. Both the SYE and DMC plants manufacture conventional PCBs and are located in Dongguan, China.

[ACE Manufactures First 3D PCB](#)

Accurate Circuit Engineering has just successfully manufactured its first 3D circuit board. This PCB is not a flat, two-dimensional PCB like most. Extensive use of angle and contours make this board as much a machined work of art as a PCB.

[Viasystems' PCB Segment Expects Sales Drop in Q4](#)

"Typical year-end seasonal decline in demand was exaggerated in our fourth quarter by a couple of factors," stated David M. Sindelar, chief executive officer. "First, while we have made progress in restoring full operations following a fire in one of our Printed Circuit Boards segment factories in China in September, our recovery was not completed until January 2013. Second, unrelated to the fire and as we anticipated, demand for our wind energy products dropped steeply in our assembly segment."

[PCB Industry Results for December 2012 Released by IPC](#)

"North American PCB book-to-bill ratios appear to have begun recovering after a downward trend that began in the second quarter of 2012," according to Sharon Starr, IPC director of market research. "The industry's sales ended 2012 at 5.2% below 2011."

[ACI Achieves ISO9001 Certification](#)

"When we received the ISO certification in October, our auditor was very surprised with our initial quality metrics, which are excellent for any company, let alone a newly certified one," said ACI Vice President Matt Osborne. "We were not surprised. Quality begins as a mindset, and our commitment to quality is evident across our service and our products. By reaching this milestone, we demonstrate the commitment to continually improve our process."

[Advanced Circuits Expands Aurora, Colorado Facility](#)

"At a time when many manufacturers have turned to outsourcing to offshore locations, Advanced Circuits is proud to feature 100% U.S.-based manufacturing and continues to provide stable job opportunities not only in Colorado, but in many states across America," said John Yacoub, president and CEO.

[Epec Adds Heavy Copper; Acquires UPE Inc.](#)

"Extreme copper technology is a growing part of the PCB industry and UPE is at the leading edge of that technology," said Ed McMahon, CEO of Epec. "With Epec's considerable high-tech manufacturing investment in both the U.S. and Asia, we are well positioned to improve on the technology that UPE has pioneered."

[AT&S Expands Portfolio; Adds IC Substrates](#)

AT&S is now taking the next logical step by expanding its portfolio with the production of integrated circuit (IC) substrates and entering into a further high-tech business segment. IC substrates serve as a connection between semiconductors and PCBs.

[Multilayer Technology adds 12 IPC-Certified Specialists](#)

Multilayer President Viny Mulani said, "This is a continuation of our ongoing commitment to the education of our staff. This year we added the IPC 6010 certification in an effort to better support our internal auditing and enhanced specification reviews."



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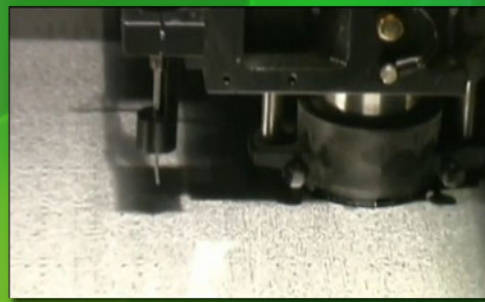
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Data Sheets Are Incomplete Guides

by **Amit Bahl**
SIERRA CIRCUITS

Call me a broken record, but I'll say it again: Consult a manufacturer before beginning any complex board design, and by complex I mean at the very least any project involving controlled impedance, unusual operating environments, high voltage, high current, or tolerances tighter than IPC Class 2. The best precaution you can take to help you achieve a board design for high manufacturing yield, greatest reliability, and the lowest possible cost is to dialogue with your manufacturer to help determine the optimum material set and stackup.

Laminates and prepregs may seem well characterized in data sheets, and they conform by category to the requirements spelled out in the various IPC specification ("slash") sheets, but that information is merely a starting point for predicting how they will behave during and after fabrication. On paper, a dozen or more materials from competing suppliers may appear to have nearly identical characteristics, but the only way to distinguish which is best for a particular application is through experience.

Consider the following example. Polyimides are candidates when performance at high temperature is a concern and they also offer low dielectric loss. Military and aerospace custom-

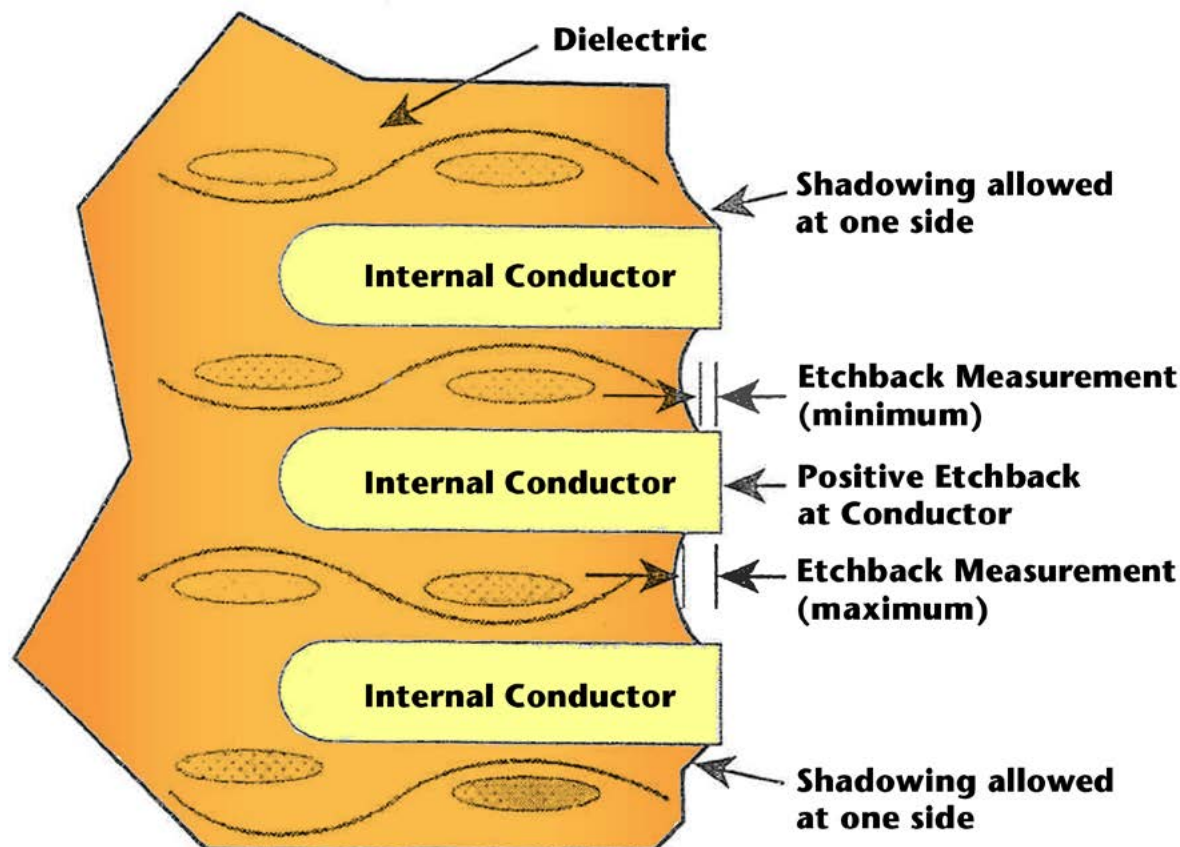


Figure 1: Positive etchback removes a slight amount of dielectric between internal copper planes, to expose more area of the planes for connection with the via barrels. (Illustration courtesy of IPC)

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Figure 2: Wicking in test boards with this particular polyimide following etchback and electroless copper deposit could not meet the IPC Class 3A limit despite strict adherence to the recommendations from the material supplier and several process adjustments.

ers frequently specify them; sometimes they request a material from a particular supplier, but often they simply call out one of the three IPC slash sheet numbers that pertain to those materials, such as IPC-4101/41. There are many comparable materials from several suppliers that all conform to that same standard.

Mil/aero customers typically require fabrication to satisfy Class 3A requirements, the most stringent IPC tolerances. And it is routine for those customers to also specify positive etchback for through-hole vias, though there is some debate whether the etchback does or doesn't provide the intended strength improvement to the unions between the plated via barrels and inner copper planes. Etchback results in a three-

point connection between a via barrel and inner planes, something like a mortise-and-tenon joint in carpentry.

The etchback processes used to bolster the connections are well established, but somewhat complicated, requiring precise control of various chemistries and exposure times. After the board layers have been laminated and drilled, the panels are sent to a plasma etching machine. Within the machine, an RF field is applied to a combination of gases, which then eats away at the resin that binds the dielectric between the copper inner planes. The copper is not attacked nor at this stage are the glass fibers of the dielectric, but a small area at the upper and lower surfaces of each inner copper plane is



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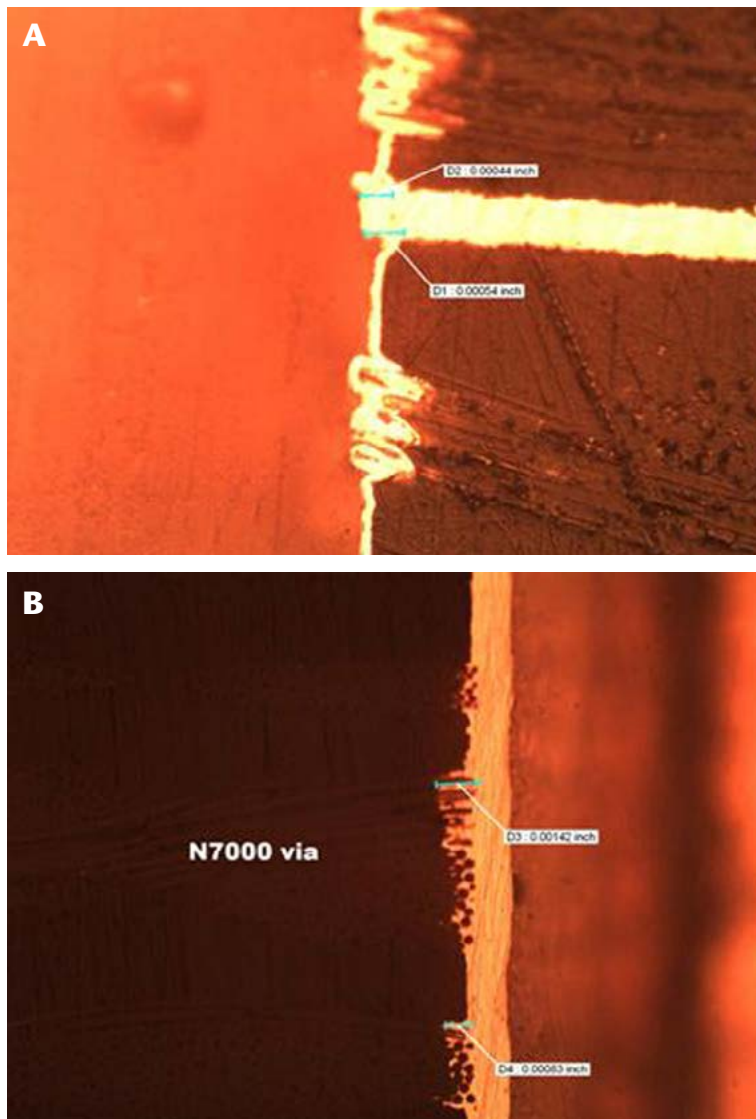
DATA SHEETS ARE INCOMPLETE GUIDES *continues*

Figure 3: Worst-case wicking in test boards built from an alternative polyimide is well within Class 3A tolerance after electroless copper deposition (a) and via plating (b).

uncovered by the removal of up to 3 mils of resin between them. The etchback also desmears the hole bores from drilling debris.

Next, the panels are sent to a chemical bath that removes the glass fibers that were bared where the resin was etched back, which would otherwise interfere with depositing and plating copper in the bores. The panels are rinsed, and then immersed in an alkaline solution to further treat the bores so electroless copper will adhere. There are upwards of 30 subsequent baths and rinses leading to the electroless deposition

of copper as a seed to bind copper plating to the hole bores and to the areas of the inner layers that were exposed by etching back the dielectric.

How do those minute details about etchback relate to seeking design advice from a board manufacturer at the outset of a project? Remember, I mentioned there are many alternative polyimide materials whose published specifications are very similar to one another. But if you were to pick one independently based on those specs, architect a stackup, and devote months to perfecting a design that works fine in simulation, you would likely wind up with an unmanufacturable product, if etchback and Class 3A tolerances are key requirements.

Why? Because IPC Class 3A stipulates that wicking cannot exceed 50 microns (just under 2 mils). Wicking refers to the migration of copper into the dielectric. The plasma etchback, alkaline bath, and the chemicals that remove the glass fibers must be very carefully controlled to minimize wicking. Compared to the Class 3 limit for wicking, which is very demanding, the Class 3A tolerance is 40 percent tighter.

If you want through-hole etchback and fabrication to meet 3A requirements, only certain of the polyimides that conform to IPC-4101/41 can meet the wicking tolerance. It takes an experienced manufacturer to know which ones.

You may never need to meet such objectives, but anytime you deviate from your routine requirements, check with your PCB manufacturer before you establish a stackup. **PCBDESIGN**



Amit Bahl directs sales and marketing at Sierra Circuits, a PCB manufacturer in Sunnyvale, CA. He can be reached via amit@protoexpress.com.

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Trace Currents and Temperature, Part 4: Via Heating

by Douglas Brooks, PhD
ULTRACAD DESIGN

SUMMARY: This is the final installment of the four-part series titled *Trace Currents and Temperature*. This column suggests a new method for dealing with vias. In Part 1, we hypothesized that trace heating was a function of the i^2R power dissipated in the trace, and trace cooling was a function of surface area. Can these same fundamental principles be applied to vias when looking at their current-carrying capacities?



ing its width ($W1$) by its thickness ($T1$). A via placed somewhere along the trace has a cylindrical geometry, with a finished diameter $D2$ and a wall thickness $T2$. Therefore, the outer diameter of the cylinder is $D2+2*T2$. The cross-sectional area of the via's cylindrical structure is π times the average diameter ($D2+T2$) multiplied by its thickness, $T2$, or $\pi*(D2+T2)*T2$.

The [first part](#) in this series discusses the role of resistance and then formulates a basic model for analysis. The [second part](#) explores various results that have been empirically obtained. The [third part](#) explores how we may be able to use the melting temperature of a trace to our advantage. In this fourth and final part, we examine a way to deal with vias.

Recall the model we developed in Part 1. We hypothesized that trace heating was a function of the i^2R power dissipated in the trace, and trace cooling was a function of surface area. Perhaps these same fundamental principles can be applied to vias when looking at their current-carrying capacities.

Consider Figure 1. As before, the cross-sectional area of the trace is found by multiply-

Equality

It seems reasonable that the current-carrying capacity of the via is determined by the same thing that determines the current-carrying capacity of the trace – cross-sectional area and environment. Looking first at the cross-sectional areas, they are equal for both the via and the trace when:

$$W1*T1 = \pi*(D2+T2)*T2$$

Using a little algebra, it can be shown that the cross-sectional area of the trace and the cross-sectional area of the via are equal when:

$$D2 = \frac{W1}{\pi} * \frac{T1}{T2} - T2 \quad (\text{Equation 1})$$

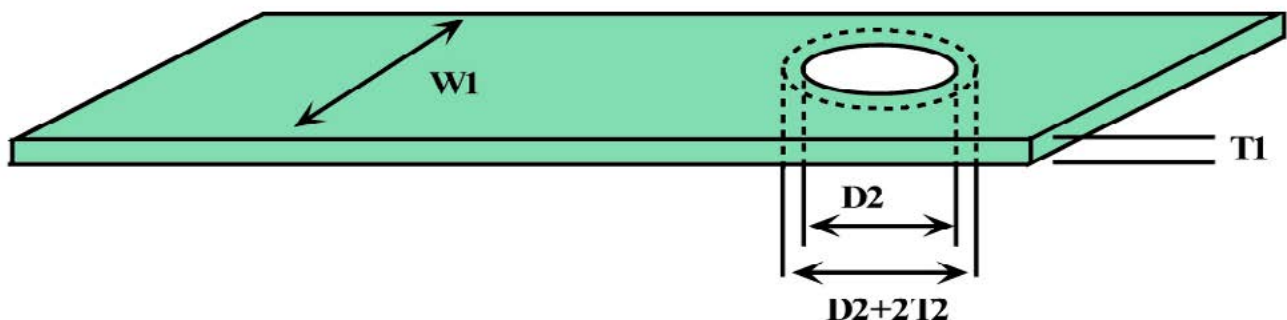


Figure 1: Relationship of a via to the trace it is placed in.

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TRACE CURRENTS AND TEMPERATURE, PART 4: VIA HEATING *continues*

If we make the simplifying assumption that via wall thickness (T2) and trace thickness (T1) are the same (T), then equation 1 reduces to:

$$D2 = \frac{W1}{\pi} - T \approx \frac{W1}{\pi} \quad \text{(Equation 2)}$$

If we further recognize that T is usually small with respect to W1, then the approximate result is that the finished diameter of the via must be at least as large as the trace width divided by π , or approximately one-third the trace width! At that via size, trace heating and via heating will be approximately equal. Larger vias will presumably heat proportionally less.

Solder-Filled Via

Solder coating has negligible impact on the current-carrying capability of a trace. This is because the resistivity of solder is usually at least ten times (or more) that of copper. Therefore, even with a solder coat whose thickness is equal to the thickness of the underlying trace, over 90% of the current still flows through the copper. Similarly, a solder-filled via will not increase the effective cross sectional area of the current path of the via, nor reduce via heating.

Multiple Vias

Are multiple vias better than a single via? An interesting question! For example, would five 8-mil vias be better than a single, 40-mil via? Figure 2 helps us see the (perhaps surprising) result. Vias contact traces or planes with a surface area defined by the outer circumference of the via cylinder and the thickness of the plane or trace (denoted as a in Figure 2). This contact area is calculated as $\pi*d*T$. The transfer of heat between the via and the trace or plane would be directly proportional to this area.

Consider two vias, one with diameter d1 and the other with diameter d2. We can compare their contact areas as follows (Equation 3):

$$\frac{A1}{A2} = \frac{\pi * d1 * T}{\pi * d2 * T} = \frac{d1}{d2} \quad \text{(Equation 3)}$$

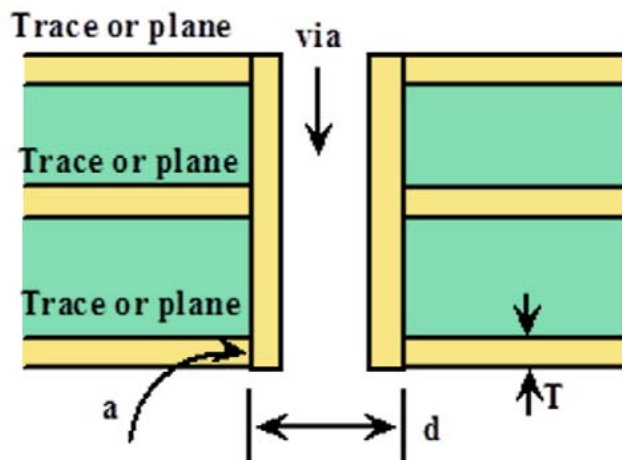


Figure 2: Are multiple vias better than a single via?

That is, the ratio of the contact areas is directly proportional to the ratio of the via outside diameters. The result is that n vias, of outside diameter d1, are equally effective as a single via whose outside diameter is n times d1, no more and no less.

Note: There are other cases where multiple vias are clearly better. For example, multiple vias can be effective in reducing overall via inductance and therefore increasing bandwidth. But these are different issues than the thermal issues being discussed in this article. **PCBDESIGN**



Douglas Brooks has an MS/EE from Stanford University and a Ph.D. from the University of Washington. He has spent most of his career in the electronics industry in positions of engineering, marketing, general management, and as CEO of several companies. He has owned UltraCAD Design Inc. since 1992. He is the author of numerous articles in several disciplines, and has written articles and given seminars all over the world on signal integrity issues since founding UltraCAD. His book, *Printed Circuit Board Design and Signal Integrity Issues* was published by Prentice Hall in 2003. Visit his website at www.ultracadm.com.

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IPC APEX EXPO Ends on a High Note

by Ray Rasmussen, Publisher

I'd say the mood of the show was pretty optimistic. All of the fabricators and assemblers I ran into were at the show prospecting for technology, additional capacity, or both. Most exhibitors felt that the show had done its job. They were selling equipment and materials.

One of the last interviews I conducted as part of our Real Time with...IPC program was with Walt Custer, who offered an upbeat 2013 market forecast and even extended industry growth into 2014. Although he was reluctant to look beyond 2014, he basically stated that all market segments, along with most geographical regions are trending up, which bodes well the industry. Great news! [Watch Walt's interview here.](#)

Lisa Lucke, managing editor of The PCB Magazine, managed our panel sessions this year with 13 in-depth discussions covering the market, onshoring, and some hot technical topics. To view, click the "Panel Discussions" tab at [Real Time with...IPC.](#)

We're off to Las Vegas in 2014. Not everyone I spoke with was excited about the prospect of moving the show next year. Some felt Vegas distracts the attendees. I agree that it does, but it also attracts a more international crowd. Personally, I like Vegas, although after a long day on the show floor, the mile walk back to the hotel room can be a bit taxing. In talking to Dave

Torp, VP of Standards and Technology at IPC, he didn't expect the conference attendance to suffer in Vegas. It's more a condition of the market than of the location. If people can afford it, and if the conference is relevant to them, they'll come.

APEX EXPO and beyond! I'm hearing that the IPC will be developing additional, major, APEX-like shows in hotspots around the globe, along with a substantial increase in the number of technical conferences as well, to service existing and emerging markets. Looks like the staff is going to have their hands full over the next couple of years.

IPC President John Mitchell has been busy getting all the right people on his IPC bus and placing them in the right seats. It's an interesting transition to watch as the old guard "roadblocks," some might say, make way for those who'll transform the IPC into an organization for the future. I'm optimistic. [Watch John's interview here.](#)

Whether you made it to the show or not, you might want to take a look at a few of the more than [150 video discussions](#) we produced, featuring the industry's leading personalities to help keep you up to speed.

A big THANK YOU to the crew at I-Connect007 and to our hard-working guest editors who helped make it all possible.



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A Panel Wonders.... What Will it Take to Bring Manufacturing Back to N.A.?

By **Steve Williams**, guest editor

During the 2013 IPCAPEX EXPO in San Diego recently, I had the pleasure of moderating a very distinguished panel of industry luminaries for I-Connect007's new panel discussion program, Real Time with...IPC APEX EXPO to discuss the hot topic of bringing back manufacturing to North America. Members of the panel included Eric Miscoll, managing partner, Charlie Barnhart & Associates; Shane Whiteside, COO, TTM Technologies; and Yash Sutariya, president, Saturn Flex Systems.

The discussion started with a review of some alarming facts: In 1950, 60% of Americans employed were in the manufacturing sector, contrasted with only 20% in 2010; less than 20% of America's GDP currently comes from manufacturing, which means that over 80% of our revenue as a country comes from service-related industries. This is great news if you sell insurance, but catastrophic if you manufacture anything. Over the last two decades, the number of North American printed circuit shops has declined 75%, from 1500 in 1985, to 336 as of February 2013. The panel noted that the 336 is also misleading, as many of these remaining shops are technically listed as being in North America, but have a majority of their revenue coming from Asian factories.

We next discussed whether "reshoring/regionalization" are merely buzzwords, or are we truly seeing a manufacturing renaissance here in the U.S.? The panel was mixed on this question, depending on the definition of "what" work is coming back to North America. The recent an-

nouncement by Apple that they would be bringing back \$100 million of manufacturing to the states generated more than a few rolled eyes on the panel; not only is that a drop in the bucket for Apple, you have to look at the content of what is coming back. Certainly not the high-level assembly of the Mac, iPod, iPhone or iPad.

Global Competitiveness

The panel discussed the fact that North America cannot compete with China on labor rates, with the average U.S. manufacturing wage in 2011 being north of \$25/hour, while China is at \$2.18. However, we can compete on productivity/efficiency; a recent IHS Global Insight survey reported that China required 110 million workers to produce the same amount of goods that 11.5 million American workers could produce—a factor of 10x!

The topic of TCO (total cost of ownership) was discussed in great depth, and that customer education is sorely needed in order to move away from "unit cost" mentality to one of "total cost." Some things clearly belong in China; however, TCO factors such as the long supply chain, high inventory levels, language/misinterpretation, duties/taxes, logistics and intellectual property concerns must be weighed into any America vs. Asia sourcing decision.

The panel closed with a discussion on the ongoing Boeing case, the impact of the proposed \$9 minimum wage in the U.S., and the politics surrounding small business operation and needed legislation.



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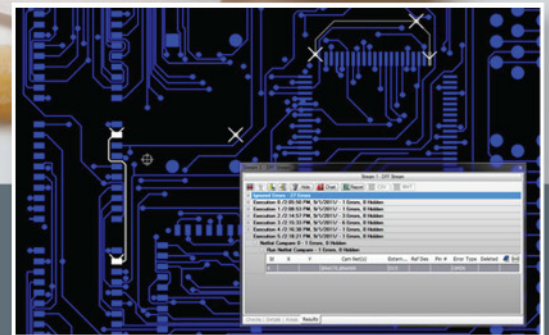
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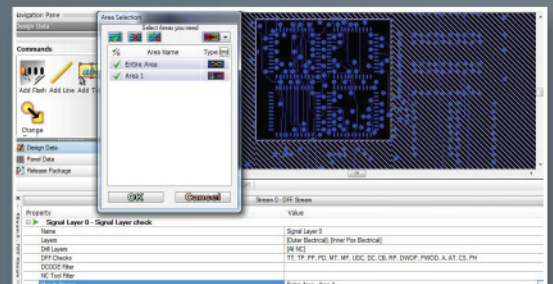
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IPC APEX EXPO Keynote from Michio Kaku *The future is closer than you think!*

by Pete Starkey, I-Connect007 technical editor



“Eternity is an awful long time, especially towards the end...Prediction is awfully hard to do, especially if it’s about the future...” Dr. Michio Kaku, author of *Physics of the Impossible* and *Physics of the Future*, quoted Woody

Allen and philosopher Yogi Berra in his preamble to the fascinating, entertaining and, in many respects, disturbing, keynote address that opened IPC’s 2013 APEX EXPO in San Diego on February 19.

Dr. Kaku, famous as a theoretical physicist, futurist and populariser of science, held the attention of a packed San Diego Convention Center audience with his views on the way technology could dramatically reshape how people would live and play 20 years into the future.

Let alone predict the future, in many respects, physicists could not even predict the past! Or could they? Dr. Kaku began his talk of the future by looking back at the history of technology and deducing that wealth originates from science.

The steam age, the industrial revolution, created enormous wealth. And what happened to the wealth? “Wealth is restless,” Kaku declared. “It went to the stock exchange, the bubble

burst, and there was a great crash in 1850.” The second wave, electricity and the automobile, created enormous wealth, which went into the stock exchange. The bubble burst and there was another great crash in 1929. The third wave, according to Kaku, was “high technology.” Again, it generated the wealth that indirectly resulted in the crash of 2008. And history appeared to repeat itself every 80 years or so.

Against this background of a physicist’s analysis of boom and bust cycles, Dr. Kaku asked, “What would be the basis of the fourth wave?” That was his topic for the day, and he predicted that biotechnology, artificial intelligence and nanotechnology would be the basis of the home of the future.

Considering computing power and Moore’s Law, and commenting that a throw-away musical birthday card had more computing power than the Allied forces had during the second World War, and that a modern mobile phone had more computing power than NASA when it put the first men on the moon, Dr. Kaku extrapolated that by 2020, a basic computer chip would cost about a penny and everything would just get smarter: Internet “everywhere and nowhere” (in terms of being conscious of it), with everyone connected all the time, whether by their “Google Glasses,” their Internet contact lenses, or even their electronic wallpaper. And





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CERTIFICATIONS



Michio Kaku *continues*

children would be the driving force, not the Pentagon any more. There would be exponential growth in the digitalisation of information, with industry after industry following the precedents of electronic financial transactions and digital music.

He envisaged a world of “augmented reality,” which Kaku described as a virtual reality imposed on real reality. He listed a long catalogue of potential applications. Intelligent wallpaper gave the scope for services like “RoboDoc,” where a robotic doctor could answer all of the most common medical questions, and “RoboLawyer,” could answer common legal questions, at very low cost. Just ask the wallpaper! And 3D TV without glasses was already feasible. The car of the future would be driverless—Dr. Kaku had already ridden in an early prototype, and the term traffic accident would eventually disappear from the language.

The areas of medical diagnosis and treat-

ment were where the outcomes could be truly beneficial: smart pills with TV cameras and transmitters to carry out internal examinations; MRI scanners the size of cell phones; DNA analysers to detect the earliest signs of cancer; nanotechnology providing medicines to attack individual cancer cells at the molecular level; personal genomics offering individual “body owner’s manuals” at low cost; grow-your-own replacement organs. His list went on and on.

What would be the next frontier? The brain—synthetic telepathy, Dr. Kaku suggested. Why do we have to grow old? Ageing is the build-up of errors—there was no reason why the ageing process could not be halted and the human lifespan extended. Reversible death, suspended animation—getting deep into the realms of science fiction here, but if we followed the logic of Dr. Kaku’s extrapolations, there was no reason why fantasy could not become reality.

The future is closer than you think!

showcase video interview

IPC APEX EXPO 2013: That’s a Wrap!

by Real Time with...
IPC APEX EXPO 2013



Editors Andy Shaughnessy, Kelly Dack and Mark Thompson provide a final wrap-up of IPC APEX EXPO 2013. Find out what piqued each editor’s interest during this weeklong event. Next year, the show moves to Mandalay Bay in Las Vegas. We’ll see you in Vegas!



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Good Show or Bad Show, it's up to You: Comments on IPC APEX EXPO 2013

by **Dan Beaulieu**, guest editor

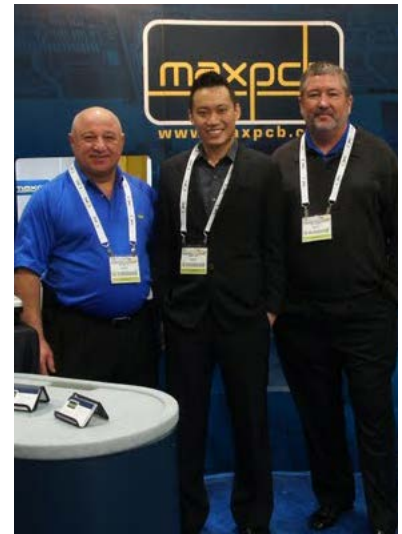
While talking to people at IPC APEX EXPO 2013, I came to realize that there are two kinds of people at the show: those who come and set up their booth and expect things to happen and then blame the show organizers when nothing does, and those who make things happen. It is the latter who now think it was a great show.

A trade show is yet another opportunity to make something happen; and just like advertising, social media or other forms of marketing, you get out of it what you put into it. If you want more traffic at your booth, then send a series of e-mails in advance, telling people not only that you are going to be there, but why they should come by to speak with you. If you want to meet the right people, don't walk around hoping to bump into them and then get mad when that

doesn't happen; preschedule the meetings with those people you would like to meet.

Do you want to make a splash at the show? If you want to get noticed, and leave a lasting impression, then arrange to be interviewed. It's not difficult; there are camera crews running around all over the place, looking for interesting people to talk about their companies and products. All you have to do is be willing to do it...and make sure you know what you want to say because when all is said and done, you are creating a seven-minute re-usable commercial about your company. Make it good.

This was a great show for those who put themselves into it; for those who expected something to happen by just being there...well, maybe not so much.





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Real Time with and Panel Discussions Make Waves in San Diego!

By **Andy Shaughnessy and Lisa Lucke**, I-Connect007 editors

It was a busy week in San Diego. IPC APEX EXPO and the Designers Forum drew attendees from around the globe. I-Connect007 covered the week's events from start to finish, shooting Real Time with video interviews and panel discussions with the industry's top technologists and managers.

We interviewed some of the PCB design community's preeminent designers and design engineers for the Real Time with...Designers Forum program. Rick Hartley of L-3 Avionics, Ruth Conner of RADServices, and Mike Creeden of San Diego PCB shared their thoughts on the challenges designers face every day, as well as the need for continued design education. And Mentor Graphics' Julian Coates detailed some

of the updates to the newest release of ODB++, as the ODB++ Solutions Alliance celebrated its first anniversary.

On the show floor, the Real Time with... IPC APEX EXPO stage and I-Connect007 booth stayed packed. Most of the time, it was impossible to find a seat, as some of the leading PCB fabrication and assembly experts mingled with one another while waiting their turn in front of the camera. At one point, the authors of the top PCB manufacturing books could be found chatting with the Real Time guest editors.

Speaking of guest editors, we don't think we've ever seen such a talented group of industry professionals all working for a common cause — in this case, that cause was approxi-

showcase video interview

Take Charge of Your Design Education

by *Real Time with...
Designers Forum*



Rick Hartley, senior principal engineer with L-3 Avionics, discusses several classes he's teaching at IPC APEX EXPO 2013 and The Designers Forum. He explains why designers and engineers should continue their design education throughout their lives and how colleges so often drop the ball when it comes to teaching design.



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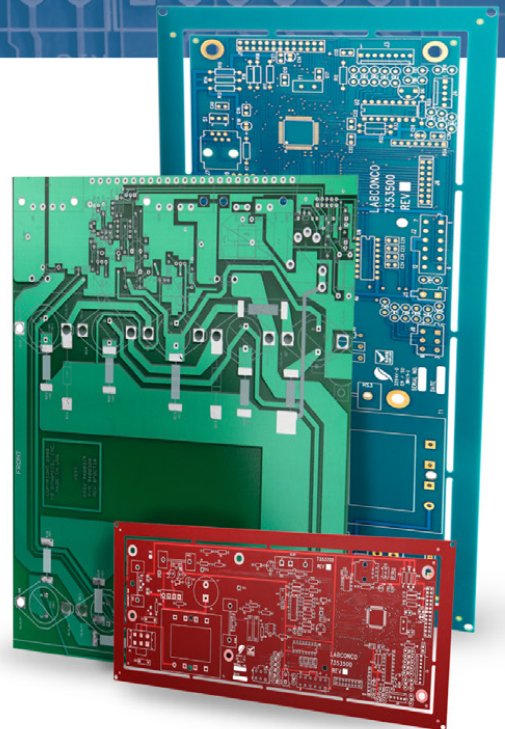


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Real Time With and Panel Discussions *continues*

mately 150 interviews, produced during the four-day run of IPC APEX EXPO. These professionals work in the design, fab and assembly segments, taking time away from their day jobs to work with I-Connect007 to bring the quality of our technical interviews to the next level. Guys (and gals) like Joe Fjelsstad, Steve Williams, Stuart Hayton, Mark Thompson, Dick Crowe, Mike Carano, Kelly Dack, Dan Feinberg, Happy Holden, Michael Weinhold, Judy Warner, Jack Fisher, Greg Thomas, Bob Neves, Mike Konrad, Susan Mucha, Dan Beaulieu, Dr. Ron Lasky, and Jennie Hwang. Let's not forget Osvaldo Targon, who shot a handful of interviews in Spanish. These people help set I-Connect007 content apart from the pack, period.

Back with a little more punch this year was our Panel Discussion program, which debuted



at last year's show. We took it to the next level this year, and in all, 13 panels were produced, each comprised of a moderator and three panelists. These panels delve a little deeper, and run a little longer (about 20 minutes) than the one-on-one RTW interviews, and we definitely hit our goal of lively, informative debate—our guest panelists did not disappoint (Yash, are you listening?) Topics ranged from technical issues to marketing, onshoring, roadmapping, and beyond. It really seemed like a good time was had by all who participated and we think our viewers will have as much fun watching as we did producing. Look for these content-rich interviews again at IPC APEX EXPO 2014 in Las Vegas. Check them out by clicking [here](#), or catch them as they appear in upcoming issues of our magazines and newsletters.

showcase video interview

Happy Birthday to the ODB++ Solutions Alliance

*by Real Time with...
Designers Forum*



The ODB++ Solutions Alliance celebrated its first anniversary with a banquet at IPC APEX EXPO. Julian Coates, director of the ODB++ Solutions Alliance, discusses the newest version of ODB++. He also talks about the testimonials presented by ODB++ users at the party, some of whom say that they no longer even think about ODB++ anymore--it's become a part of their workday.



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The PCB List Demos a Hit!

The PCB List demos on the show floor attracted the attention of just about everyone possible — from fabricators to OEMs to EMS companies, according to I-Connect007’s Project Manager Patty Goldman. EIPC Director Michael Weinhold even stopped by the booth for a Real Time with... interview to discuss *The PCB List* with Goldman and Dan Beaulieu. Watch it [here](#). Goldman sits down with editor Lisa Lucke and answers a few quick questions after the show.

How would you describe the response to The PCB List at the show?

Really good! We expected plenty of interest in the demos and we weren’t disappointed.

We had quite a few people register to use *The PCB List*, and a number of PCB manufacturers claimed their companies. We had many EMS companies commenting on how valuable *The PCB List* has been to them. They are using it all

the time to find fabricators for their specific needs.

How was the traffic at the I-Connect007 booth?

It was literally busy all the time. We did dozens of demos—lots of people sitting right down, claiming their companies. All I really did was show them the GO button and they were off!

Did I hear a rumor about a sister list for EMS?

Yes, we also started letting people know about the sister “list”—*The EMS List*—a directory of EMS companies worldwide. People seemed very interested in knowing more about that. We’ll be letting people know about the launch as it gets closer.



showcase video interview

A New Generation of PCB Designers

by Real Time with...
 Designers Forum



Mike Creeden, CEO of San Diego PCB, discusses the San Diego Designers Council and the topic of his presentation, “Where are the Next Generation of Designers?” He identifies several industry events that have had a devastating effect on the PCB designer population and warns of dire consequences unless current designers can find ways to pass on their unique knowledge to a new generation.



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The Flex (and APEX) Future is so Bright, I've Got to Wear Shades

by Joe Fjelstad, guest editor

The 2013 edition of the IPC APEX conference and exposition, held in San Diego, once again cleared the bar of attendee expectations as the electronics industry continues its rebound from the last few years of globally grim economic conditions. In that regard, this year appears to have sparked some renewed enthusiasm for the future.

A good deal of innovation was in evidence as materials and equipment suppliers have been preparing to meet the needs of evolving electronic interconnection solutions both rigid and flexible. While there is not space to mention all of the deserving technologies on display, a few notable manufacturing solutions in imaging and lamination really popped for this visitor.

On the imaging side, there was the desktop coater and exposure table unit from Rainbow Technology. It is ideally suited to small prototyping needs and is capable of resolving sub-20 micrometer feature sizes. There was as well a new

(for this reviewer) lamination registration aid for rigid/flex manufactures from Chemplate, in Barcelona, Spain, called Indubond (short for inductive bonding), which employs inductive heating to spot-weld pin-registered circuits before lamination to mitigate circuit feature movement.

In the realm of test and reliability assurance, there was the miniaturized HATS test system on display and being demonstrated by Integrated Reliability Test Systems, Inc. This appears an ideal, low-cost alternative to the much more massive multipurpose test systems commonly used for PCB assembly coupon testing and should readily find new customers seeking to better understand the true quality of their products, all to the greater comfort their customers.

To summarize, this year's APEX was an all around excellent show and if past in any way predicts the future, next year's EXPO in Las Vegas will be even better.



Increased Performance with Cost-Effective HDI Technology

by **Bill CuvIELLO**

VISHAY

SUMMARY: *With enhanced signal routing and response conditioning, HDI technology enables greater wiring density and closer component spacing. All these improvements are possible thanks to the use of thin film, high-density multilayer substrates.*

Electronic systems across the board are decreasing in size while increasing in performance. In compact and portable products ranging from cell phones to smart weapons, high-density integration (HDI) technology is enabling the design of smaller end products that meet higher standards for electrical performance and efficiency.

HDI boards themselves are low-noise products that integrate conductor patterns and other passive components in custom resistor solutions. With enhanced signal routing and response conditioning, HDI technology enables greater wiring density and closer component spacing. All these improvements are possible thanks to the use of thin film, high-density multilayer substrates.

Because these devices can be tremendously complex and their design tied tightly to the end-product performance, most HDI boards are custom-designed to meet the specific requirements of a given application and to deliver the best ratio of price to performance. The design process involves a series of critical decisions that will shape the performance of the HDI and its aptitude for the target application.

The Circuit Foundation: the Substrate

At the foundation of the circuit is the substrate, or base material. Selection of the base material is the first step in creating an HDI scheme. Every choice offers a unique set of behaviors and characteristics that will influence overall operation. Key considerations include power dissipation capability, a primary factor in DC applications, and the dielectric constant, which is of the utmost importance in higher-frequency applications.

Vishay and its clients develop HDI products that incorporate quartz (SiO_2), alumina (Al_2O_3), silicon, ferrites, titanates, aluminum nitride (AlN), or beryllia (BeO). In terms of its performance, quartz makes a good match for high-density patterns. It features a low loss tangent and a CTE of just 0.55 ppm/°C and typically is

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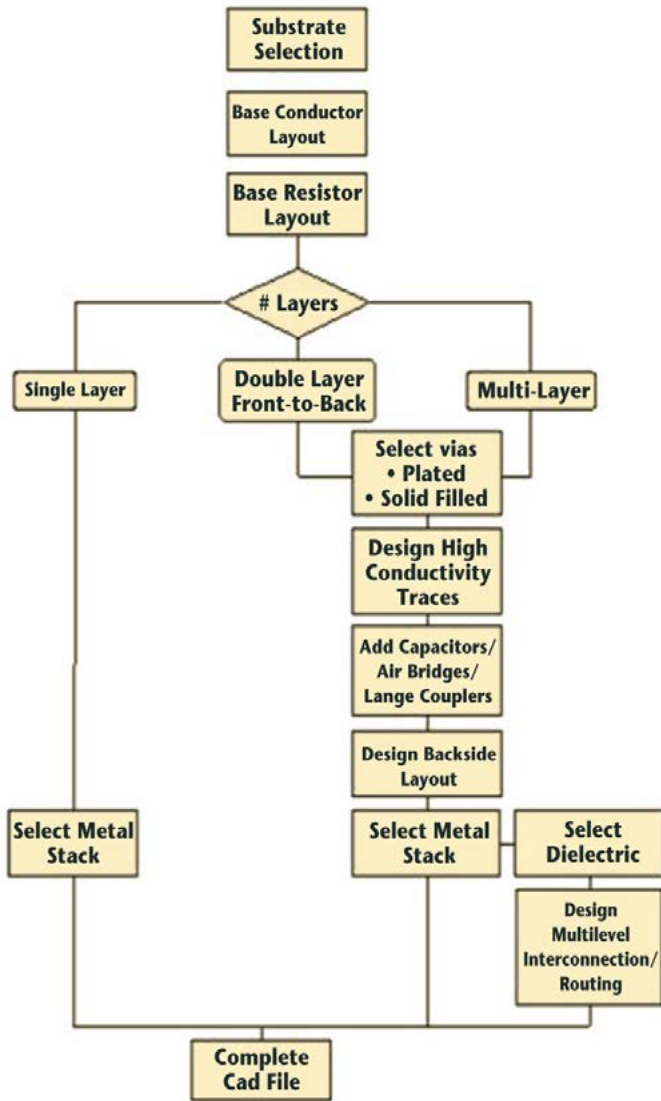


Figure 1: Roadmap to the design of an HDI circuit board.

chosen for microwave or millimeter-wave low-power/low shunt capacitance. The main drawback to selecting from quartz substrates is their very high cost. At a friendlier price point, alumina offers a cost-effective alternative suitable for standard hybrid or medium-power microwave applications. Both options have a minimum thickness of 5 mils, which makes them twice as thin as the remaining three substrate choices.

Silicon, aluminum nitride, and beryllia feature much higher thermal conductivity than do quartz and alumina. From among these three

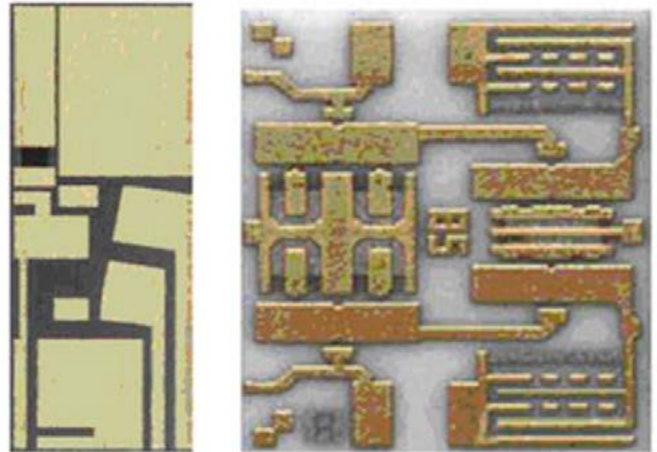


Figure 2: Examples of conductor patterns with special routing for externally mounting components.

substrates, silicon is the best fit for medium- and high-power DC applications, as well as for high-density, fine-line interconnections. A common choice for high-power microwaves, aluminum nitride makes an ideal CTE match to silicon devices. Finally, with ratings of 300 W/M at 25°C and 240 W/M at 100°C, beryllia features thermal conductivity nearly twice that of the nearest comparable base material.

The Base Conductor and Routing Scheme

Once the designer and user establish the appropriate substrate for HDI, it's time to select the conductor material and routing schemes for the circuit. The conductor material is the first metal layer that makes all the major routing connections, and conductor lines must be designed not only to withstand the current they will carry, but also to provide resistance low enough not to interfere with device performance.

Current density and conductor impedance have a direct effect on circuit performance, so the choice of metal used as the base conductor [aluminum (Al) and gold (Au)] can have significant ramifications. For widths up to 20 mils, gold is capable of conducting five times the maximum amperage handled by aluminum. The advantage persists to a lesser extent in wire bonds over 40 mils long. Because gold is limited to a 2-mil diameter, aluminum has the advantage in achieving much higher amperages.

Though vias (through-hole or filled) are added to the HDI at a later stage, their placement must be decided at this stage. Like substrate and base conductor, the type of via selected will differ according to the application. Either plated through-hole conductors or simple holes for pin alignment help to identify via placement.

The Base Resistor

Knowledge of the resistor material, power, temperature coefficient of resistance (TCR), tolerance, and application is required for effective circuit design because again, the choice of material dictates performance of the circuit.

Nichrome and tantalum nitride are two of the most common resistor materials, with nichrome able to handle much lower TCR values and much higher sheet resistivity than tantalum nitride, but with less resistance to environmental degradation. Sheet resistivity and current density are inversely related, and different line widths are required by different substrate materials to achieve a target sheet resistance.

Quartz has the lowest line-width requirements, needing a width of only 0.5 mA/mil to reach 25 ohms/sq. Alumina, too, requires only thin lines, requiring 4 mA/mil for the same resistance value. Silicon and aluminum nitride demand lines of 20 mA/mil and 19 mA/mil, respectively, for 25 ohms/sq, while Beryllia demands 32 mA/mil to achieve 25 ohms/sq and 4 mA/mil for 200 ohms/sq.

Resistor Ratings and Design

Typical ratings for standard resistors include a resistance range of 5 ohms to 2 megohms, absolute tolerance of 5% to 0.1%, and ratio tolerance of 1% to 0.01% depending on the range. These figures change when microwave resistors are taken into consideration. Such devices offer resistance parameters ranging from between 10 ohms and 1,000 ohms, with an absolute tolerance and ratio tolerance both of 0.5% and absolute TCR of less than or equal to 200 ppm/°C.

With their narrower specifications, microwave applications tend to require lower-value resistors designed in a stripline format. In this manufacturing model, the resistor layout is a simple rectangle without any cuts that could cause reflection and affect VSWR characteristics.

Trimming enables the tight resistance values required while maximizing yield, and a method called edge-sense trimming around a center line can limit the ill effects of trimming and maintain frequency response. Finally, the use of a high-temperature stabilization procedure produces very stable resistors and minimizes drift over time or temperature.

The Fit: The HDI Shape

The substrate material can be cut into virtually any shape to meet the space, shape and size requirements of the end product. Using CO₂ cutting, Vishay can create the necessary form, complete with in-hole drilling to enable inclusion of the necessary through holes, vias and filled vias, as well as two-sided-substrate patterning and edge-wrap metallization.

The smaller the end system, the more likely a multilayer solution will be needed. This more complex approach often demands design on a CAD system, as the many factors that must be taken into account include conductor routing, vias, resistor cells, added active devices, special features such as capacitors, Lange couples, and any associated interconnects. The selection and interaction of different layer applications also play a role in determining the effectiveness of an HDI for a particular application. As much as is possible, all of these elements must be optimized to contribute to performance of the end device.

As far as positioning the substrate, placement parameters require a position tolerance of 0.003", placement a minimum of 0.002" from the substrate edge to the circuit, an inside corner radius of 0.005" minimum, and 25% removal of the substrate.

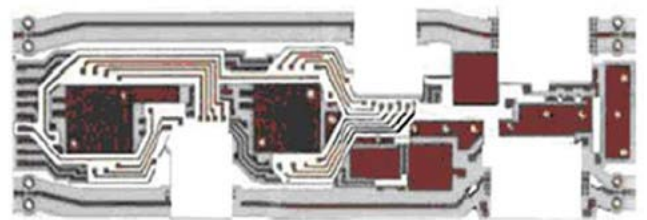


Figure 3: With CO₂ cutting, almost any shape of HDI board with multiple holes can be achieved.

INCREASED PERFORMANCE WITH COST-EFFECTIVE HDI TECHNOLOGY *continues*

Layer	Material	Std Sputter Thickness	Std Plated Thickness	Comments
Adhesion	Titanium-Tungsten (TiW)	500Å min	~	
	Titanium (Ti)	500Å min	~	
	Nichrome (NiCr)	500Å min.	~	
	Chrome (Cr)	500Å min	~	
Barrier	Tantalum Nitride (Ta ₂ N)	300Å min	~	High temp barrier
	Palladium (Pd)	3kÅ- 5kÅ	~	High temp barrier
	Tiw	500Å-1kÅ	~	High temp barrier
Conductor	Nickel (Ni)	1.5kÅ- 5kÅ	5kÅ-15kÅ	
	Aluminum (Al)	10kÅ min	~	
	Gold (Au)	1kÅ-3kÅ	25.4kÅ min	
	Copper (Cu)	4-12u (1kÅ-3kÅ)	15-45u inches (3.8kÅ-11.4kÅ)	
High Current Conductor	Gold (Au)	~	300u inches (76.2kÅ)	Min
	Copper (Cu)	~	1000u inches (254kÅ)	
Dielectric	Silicon Nitride (Si ₃ N ₄)	2kÅ-5kÅ	~	Diel. Constant= 6-9
	Polyimide	48kÅ +/-1kÅ		Diel. Constant= 3.4

Figure 4: Film materials available for particular layer applications, and the thickness of each type.

The Electrical Path: Vias and Crossover Solutions

Plated through-hole and filled vias are suited to differing applications. While the formed represents the least expensive solution, it is functional only in HDIs requiring a simple front-to-back electrical path. Through-hole patterns require a minimum 0.005" ring around each hole to compensate for the tolerance build-up caused by hole placement, manufacturing alignment, diameter tolerances, slight laser entrance hole rounding, and other factors. Plated through-hole designs require a minimum thickness of 0.8 times the substrate thickness with a typical impedance of less than 20 milliohms.

When improved thermal conductivity to the back side of the circuit is required, filled vias offer a better solution. They offer the designer as many heat channels as the area allows, and additional thermal conductivity is enabled by the

placement of components directly over the via for maximum heat transfer from those components. To improve signal transmission, the designer can use filled vias to provide additional low thermal conductivity paths to ground plate heat sinks. Gold or copper filled vias require a diameter of 7 mils to 20 mils with typical impedance of less than 3 milliohms.

When crossovers are necessary, air bridges are configured on the conductor pattern through the depositing and patterning of a layer, placement of a second layer in place over it, and subsequent removal of the first layer. Air

bridges require a minimum gap of 0.5 mils between lines, a tolerance of 0.1 mils, minimum line width of 0.5 mils, and bridge height of 300 to 500 microinches.

In the case of a supported air bridge, polyamide is used as the first layer, which remains intact, supporting the bridge in a more stable and durable structure. If epoxy or solder is used to attach components to the substrate, addi-

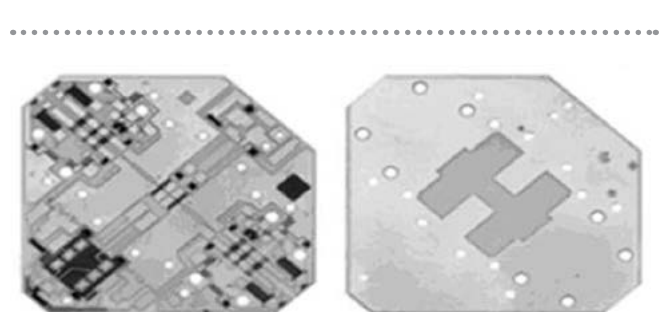


Figure 5: An example of an array patterned on both the front and back sides.

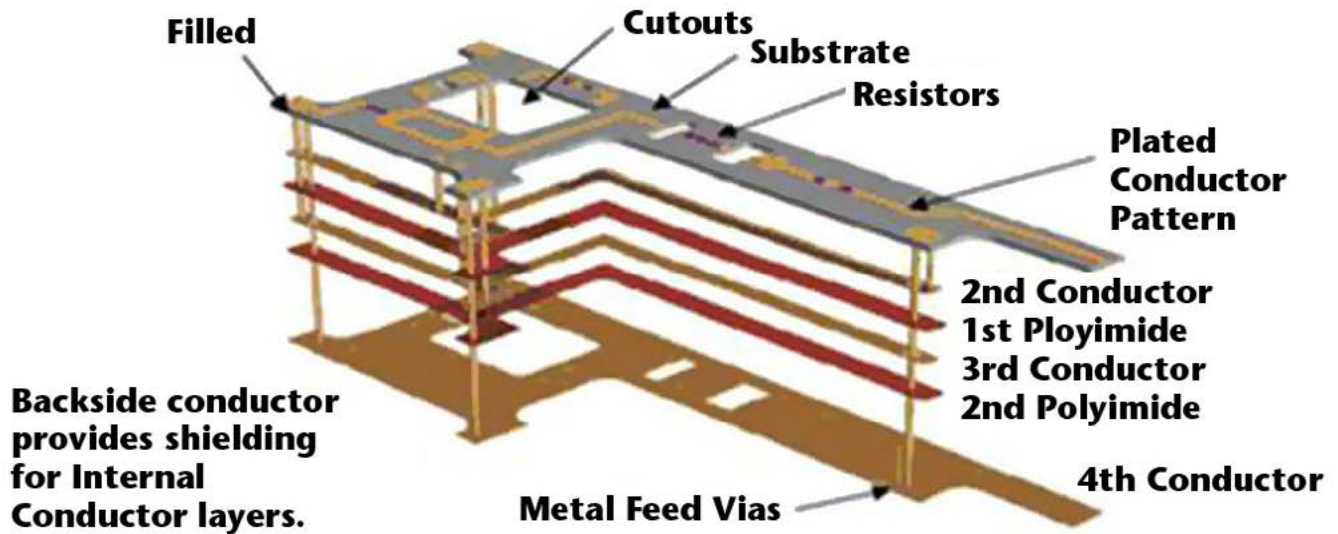


Figure 6: Expanded view of a thin film multilayer HDI circuit designed for a military helicopter. The design used almost all of the design and process options available, and after significant R&D effort was manufactured with reasonable yields.

tional stability can be provided by solder dams in either polyimide or a lower-temperature thermal-set plastic.

The Backside and Multilayer HDI

Backside and multilayer HDI circuits are necessary to provide the necessary performance within a space-constrained design. Although board space savings are influenced by many factors, one additional layer can reduce the area by a factor of approximately 1.33, two layers by 1.77, three by 2.37, and four by 3.16.

In backside designs, the bottom surface of the substrate can also be used for conductor interconnect patterns or ground plane definitions, and front-to-back alignment can be held to 0.002". Back-side metallization can offer shielding for interconductor layers in multilayer designs, and options in thin film techniques include metallized through-holes for grounding, large-area metal for impedance, and custom shapes. Furthermore, back-side patterning provides a cost-effective alternative to top-surface multilayer designs.

If a single-layer front-and-back combination can't provide the necessary layers, then layers

can be stacked on either side of the circuit in a multilayer arrangement.

A dielectric material such as polyamide, or sometimes silicon nitride, serves as insulation between metal layers. While polyimide offers better patterning properties and processing temperatures, in general no stacking restrictions apply for either material.

Again, it should be noted that process compatibility issues between layers should be explored with design engineers, as these issues can restrict the use of multiple metal stacks on multiple dielectric layers. **PCBDESIGN**



William Cuvillo is a senior product marketing manager at Vishay Intertechnology with 24 years of experience in general sales and application engineering management for specialty film products. Cuvillo has published and presented papers at technical symposiums in Europe and the United States on thin film HDI, design guidelines, and frequency response of thin film chip resistors.

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"FTG continued to improve key aspects of the business in 2012 while making key strategic investments in new facilities for our Aerospace business for the future," stated Brad Bourne, president and chief executive officer. He added, "The addition of facilities in China and the U.S., the two largest aerospace markets, are already resulting in new revenue streams for FTG."

[Proposed Revisions to USML Category XI: IPC Comments](#)

For the past year, IPC has conducted an educational campaign, "Follow the Law, Protect the Board," to highlight the importance to national security of clear, unambiguous controls for PCBs because of the important information they contain about the workings of defense electronics for which they are uniquely designed.

[U.S. DoD Spending on Renewable Energy to Hit \\$1.8B by 2025](#)

"U.S. military spending on renewable energy programs, including conservation measures, will reach almost \$1.8 billion in 2025," says research analyst Dexter Gauntlett. "This effort has the potential to not only transform the production, consumption, and transport of fuel and energy within the military; it will likely make the DoD one of the most important drivers of cleantech in the United States."

[DARPA, Semi and Defense Industries to Set Up STARnet](#)

The Semiconductor Technology Advanced Research Network (STARnet) will support large university communities to look beyond the current evolutionary directions and make the discoveries that will drive technology innovation beyond what can be imagined for electronics today.

[FlexTech Alliance Forms New Nano-Bio Consortium](#)

The Alliance has been selected to launch a new manufacturing consortium which will operate at the junction of nanotechnology, biotechnology, additive manufacturing, and flexible electronics. Bringing together world-class researchers and building prototype monitoring devices are the new nano-bio manufacturing consortium's primary goals.

[McConnell and Woody Earn IPC Presidents Award](#)

Karen McConnell, Northrop Grumman, and Linda Woody, Lockheed Martin, earned IPC Presidents Awards at IPC APEX EXPO. "IPC and the entire industry are fortunate to have Karen and Linda contributing their time and expertise to IPC standards and program development. Their work has enriched both IPC and the industry," said John Mitchell, IPC president and CEO.

[AIA Reports on Contraction of the U.S. Economy](#)

The contraction of the U.S. economy in the fourth quarter underscores AIA's warning for the past 18 months that severe cuts across the board budget cuts—both to defense and non-defense discretionary spending—threaten to throw the economy into a tailspin.

[DARPA Seeks Tech for Transient Electronics](#)

The sophisticated electronics used by warfighters in everything from radios, remote sensors and even phones can now be made at such a low cost that they are pervasive throughout the battlefield. These electronics have become necessary for operations, but it is almost impossible to track and recover every device.

[IHS: India to be 4th Biggest Defence Spender in 2020](#)

IHS forecasts that India will become the fourth biggest defence spender in the world by 2020, behind the U.S., China and Russia—surpassing France, Japan and the U.K. over the next eight years. IHS Jane's Defence Budgets projects that India's defence spend will reach USD65.4 billion in 2020 despite cuts announced by India's defence minister in January 2013 caused by the challenging economic and fiscal climate.

[High Value in Security Drives Global Border Security Market Growth](#)

The Global Border Security Market 2013-2023: UAVs, UGVs and Perimeter Surveillance Systems, Visiongain's latest defence and security report, values the global market for border security at \$19.34bn in 2013, due to the high value placed on the security and effectiveness of border security systems in order to protect citizens against various external threats.

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Packaging and Patterns

by Jack Olson, CID+

SUMMARY: In previous episodes, we've learned what a circuit board is, we've learned that we use a schematic to begin the design process, and that the end result will be a whole bunch of data and a couple of drawings. Now it's time to start "connecting the dots" to get from here to there.

Packaging

Once the schematic diagram is complete, the next step is to convert it into the type of data needed to start a circuit board design. This process of "packaging" a schematic creates a part list and a net list.

Let's imagine that our schematic features two identical circuits, and each one of these cir-



cuits contains a pair of op-amp symbols, for a total of four op-amps. We need to assign these op-amps to a specific component type, and we have found two different components that would be acceptable. One is a "dual" package and the other is a "quad."

Without going into the details of why we would choose one over the other, we need to notice that depending on which one we select, the part list and net list will change. If we use two dual packages, we will have a U1 and a U2 with pins numbered 1-8. If we use a quad package we will only have a U1, but the pins will be numbered 1-14. Both the net list and the part list will be affected by our choice.

In a similar way, all of the symbols on a schematic will be assigned to physical components, and then a part list can be created. All of the lines connecting the symbols together on the schematic will be mapped to the pin numbers of those parts and this data will be organized into a net list. Both the part list and the net list are required to begin the circuit board design. Before computer-aided design was available, the part list and net list information was created manually, but now most CAD systems can generate them automatically as a result of the schematic packaging process. After packaging the design, the schematic is back-annotated with the pin numbers and reference designator

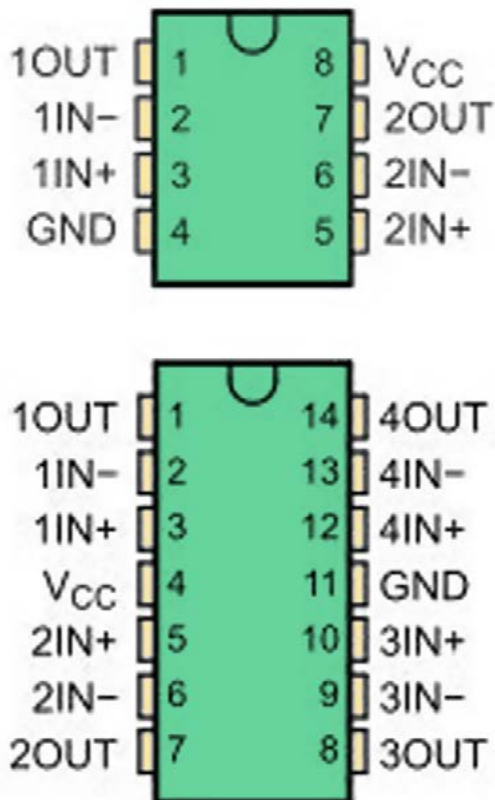
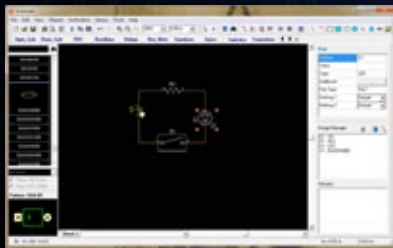


Figure 1: Component choices.

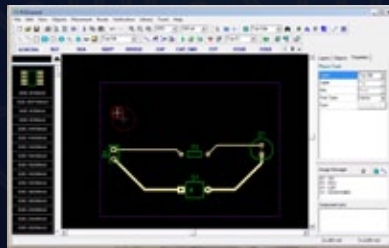
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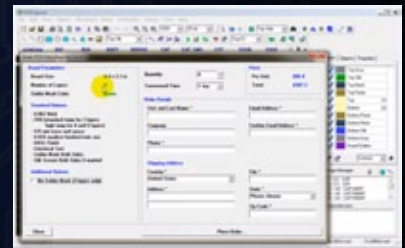
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PACKAGING AND PATTERNS *continues*

Figure 2: Blast from the past: The esteemed X-Acto knife.

assignments. At this point the schematic database and the design database are “in sync” (synchronized).

You should scan through the BOM before forwarding it to other departments. One improvement you should try to make is the combination of similar parts. For example, you may see two different groups of parts that are calling for 0.1uF capacitors, but they are similar enough that they can both be combined into the same part number. This reduces cost by allowing purchasing to buy common components in higher quantities, and it improves efficiency by leaving you with one less reel of components to stock, transport, and load onto the assembly equipment. Also, look for inconsistencies. If the design is primarily surface mount technology but you see a through-hole component in the BOM, it might be worth asking if it is correct. Sometimes a single component change can affect the assembly process significantly.

Patterns

Early circuit board design was done by hand, first by drawing the circuit pattern and then either:

1. Using some form of painting, spraying, dusting, depositing or stamping conductive material onto a substrate, or
2. Applying the pattern to a copper-clad substrate as an etch resist, and then removing all the extra material except the desired copper pattern.

Both of these methods describe the fabrication of the board, but we are interested in the patterns. Where do they come from?

One improvement over hand drawing was the method of using colored tape to create the pattern on clear sheets of Mylar film at 2X or



Figure 3: Tools of the trade in the days before design software.

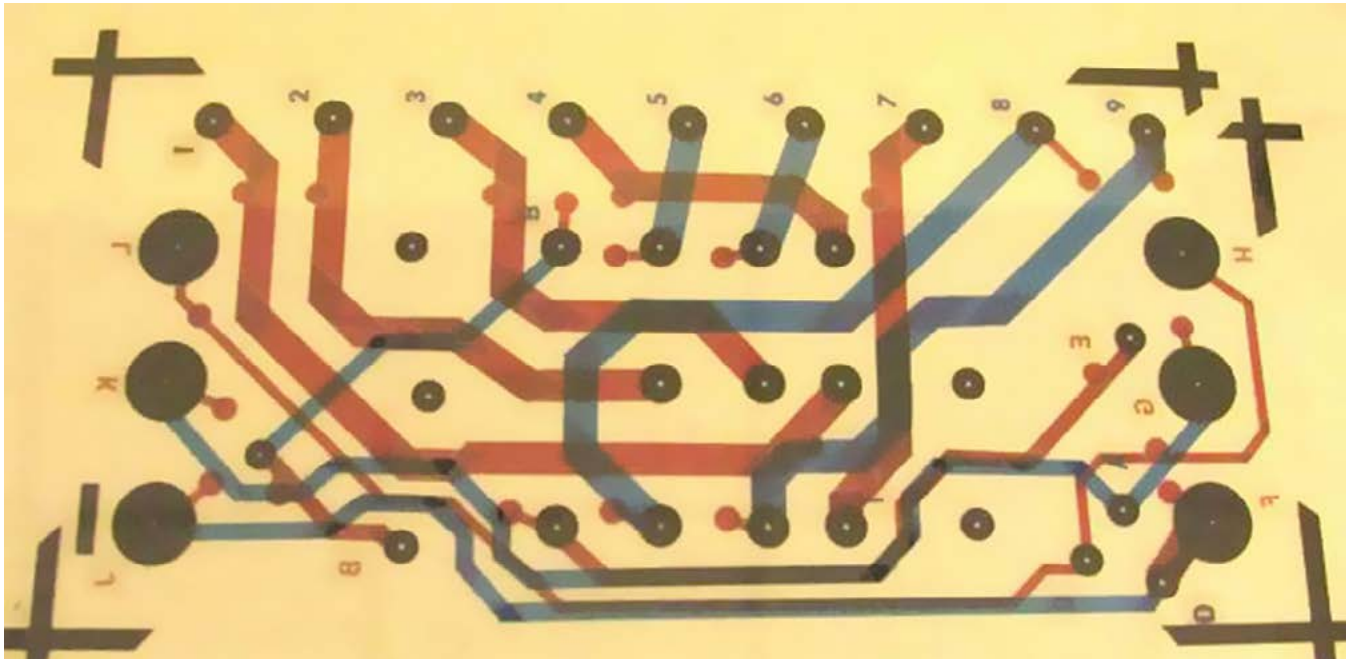


Figure 4: A simple two-layer design layout.

4X or 10X the desired size, then reducing the pattern down to 1:1 scale for the master film, which would be used repeatedly to image the etch resist patterns onto copper-clad laminates. To be successful at taping PCB layouts, you had to plan ahead and be pretty good at using an X-Acto knife.

Some of you old-timers might recognize the classic book shown in Figure 3. The Bishop Graphics publication of “The Design and Drafting of Printed Circuits” introduced the basic principles of board design, and included instructions for “taping up” a layout. Also shown in the picture are several widths and styles of tape, and some of the “ChartPak” decals that were available to place footprints, graphic shapes and targets quickly.

Figure 4 shows a very simple layout of a two-layer design. The top side of the board pattern was created using blue tape, the bottom was created with red, and the common features like board edge crops and pads were black. (I was told that the red side signified the “hot” soldering side of the board.) This was a common method until computers and CAD software became available. Interestingly, many designers I know still set their surface copper colors for red and blue, even

though the color preferences mean nothing anymore. Do old habits die hard?

You can imagine that the only way to check a layout created with tape is to manually verify each net point-to-point. This is a tedious process that only gets worse as the complexity of designs increase. Modern circuit board design is similar in that the goal is to create images for each copper layer (and for solder mask, solder paste and silkscreen layers, too), but the synchronization between schematic and board can be verified automatically.

I’m revealing my age here, but my first circuit board design task after college was to learn PCAD version 1.31 for DOS, which was one of the only circuit board layout software packages available for personal computers in 1987. A company hired me because none of their tape-up guys wanted to learn it! Now, with the exception of a few hobbyists making circuit boards the old-fashioned way, virtually all circuit board design today is accomplished using computers. There are many different software packages available, some inexpensive or free but with limited capabilities, and others that provide quite sophisticated integrated toolsets offering many extra features

PACKAGING AND PATTERNS *continues*

such as circuit simulation, 3D visualization, multiple data format exports, constraint editing, autorouting, interactive design rule checking, etc.

These columns will not focus on any particular brand of CAD software. What you learn here will be the most basic concepts of good circuit board design, which should be applicable to any software package you use. **PCBDESIGN**



Jack Olson, CID+, has been designing circuit boards full-time for over 20 years. He would like to thank Richard Nedbal for creating affordable and reliable PC-based software tools. His work with companies like Personal CAD Systems opened doors for many of us.

IPC Technology Roadmap Takes New Directions

By Terry Costlow

Industry roadmaps predict the future in many ways, beginning with an in-depth analysis of the technologies used in their industry. They can also herald shifts in the way an industry is meeting its challenges.

The 2013 IPC International Technology Roadmap for Electronic Interconnections marks a shift that's occurring throughout the electronics industry: There's more cooperation and information sharing. As technologies get more complex, it's critical to have information on all aspects that impact a technology, from initial design to manufacturing processes and products.

IPC is meeting this challenge by working closely with iNEMI, among others, helping in some research projects and gleaning data from areas that are at the core of iNEMI's roadmapping efforts. The IPC roadmap also utilizes information from the International Technology Roadmap for Semiconductors, as well as from the Japan Printed Circuit Association (JPCA).

"This roadmap has a lot more shared in-

formation. There's more exchange between a number of electronics industry groups; we're focused on providing the best information for our respective constituencies with less concern on where the facts originate," said Jack Fisher, president of Interconnect Technology Analysis, Inc. and chairman of the IPC Roadmap Executive Committee. "There's also less company-based research, the knowledge is more spread out."

A major shift in technology comes in the environmental section. It's been transformed and renamed the stewardship section. Consumers in many fields have embraced the green movement, which prompted some changes in the way companies view related environmental issues.

"We're no longer looking at environmental issues as a burden; we're looking at them as an opportunity," Fisher said.

That shift will force many companies to alter some of their programs and processes. One challenge for development teams will be to come up with solutions that meet all the varied regulations, which have not been completely harmonized. That's one of the reasons that Fisher suggests that developers focus on sustainability at the start of the design cycle.

"To be successful, you need to look at it early in the process instead of waiting until it's the equivalent of a fiscal cliff," Fisher said.





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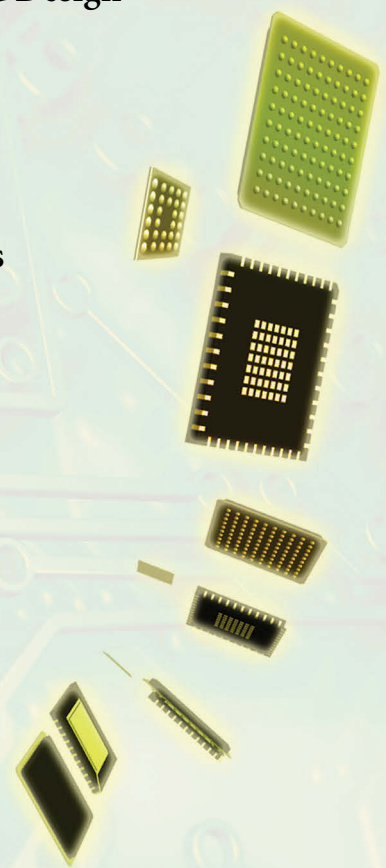
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TOP TEN

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News

Most-Read News Highlights from PCBDesign007 this Month

① Complete IPC Designers Forum Coverage From San Diego

The Designers Forum is over, but we have interviews with the movers and shakers of the PCB design world. If you couldn't make it to IPC APEX EXPO in San Diego, you missed a great event, with presentations by Rick Hartley, Happy Holden, the "Ask the Flexperts" guys, and more!

② Industry Icons Star in Panel Discussions

During IPC APEX EXPO 2013 in San Diego, I-Connect007 shot a dozen hard-hitting, long-form panel discussions with a who's who of the PCB and EMS communities, discussing industry issues that matter most.

③ ODB++ Solutions Alliance Launches Next-Gen Data Format

The newly improved format offers increased time savings, further reduction of manual errors, and even higher levels of automation for enhanced user productivity. New features and enhancements help PCB designers and manufacturers minimize the manual entry of data into NPI, DFM, and CAM software tools.

④ Zuken's CADSTAR 14 Drives Out Design Errors

Designers using Zuken's expert desktop design solution will benefit from improved productivity and reduced design times through key enhancements. These include improved error report management, an updated BGA wizard and automatic net rerouting.

5 Intercept Enhances Pantheon PCB Layout Software

"With Pantheon's new user interface reaching maturity, the engineering team is now making great strides in core functionality, Engineering Manager said John Towers. "Our focus this year is to increase usability for all technology areas while continuing to forge new ground for RF and hybrid designers."

6 EMA Releases TimingDesigner 9.3 Analysis Tool

"With a fresh, redesigned user interface and improved controls, TimingDesigner 9.3 is the most intuitive timing analysis tool on the market," said Manny Marcano, president and CEO of EMA. "We've made several useful additions to diagram and spreadsheet styling, as well as enhancements to the image exporting capabilities."

7 Ucamco Offers Latest Gerber Format Specification

Following months of intensive work, Ucamco has released the latest Gerber Format Specification. While the format itself remains unchanged, the specification has been thoroughly revised for clarity and ease of use.

8 Altium Designer 2013 Creates New Opportunities

Altium Designer 2013 not only delivers new and enhanced features, it also opens up Altium's design platform to key partners. This creates a range of new opportunities for users, partners and system integrators and represents a quantum leap for the industry.

9 McConnell and Woody Earn IPC Presidents Award

Karen McConnell, PCB designer with Northrop Grumman, and Linda Woody, engineering manager with Lockheed Martin, took home IPC Presidents Awards at IPC APEX EXPO. "IPC and the entire industry are fortunate to have Karen and Linda contributing their time and expertise to IPC standards and program development. Their work has enriched both IPC and the industry," said John Mitchell, IPC president and CEO.

10 Mentor's Flowmaster Thermal Tool Boosts Capabilities

Mentor Graphics Corporation has announced several new capabilities for its Flowmaster simulation software solution for thermo-fluid systems. From concept through design, optimization, and validation, the Flowmaster products are used at every stage of development.



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Application of Printed, Organic & Flexible Electronics

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Eastin Hotel, Penang, Malaysia

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San Jose, California, USA

2013 Defense, Security, and Sensing Exhibition

April 29-May 3, 2013
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Next Month in *The PCB Design Magazine*

Unintentional radiated emissions can cause a variety of problems on high-speed PCBs. But simple changes in your layout can prevent EMI. Next month we tackle the challenges of achieving EMC, and discuss some proven methods for minimizing EMI transmissions.

See you in April!