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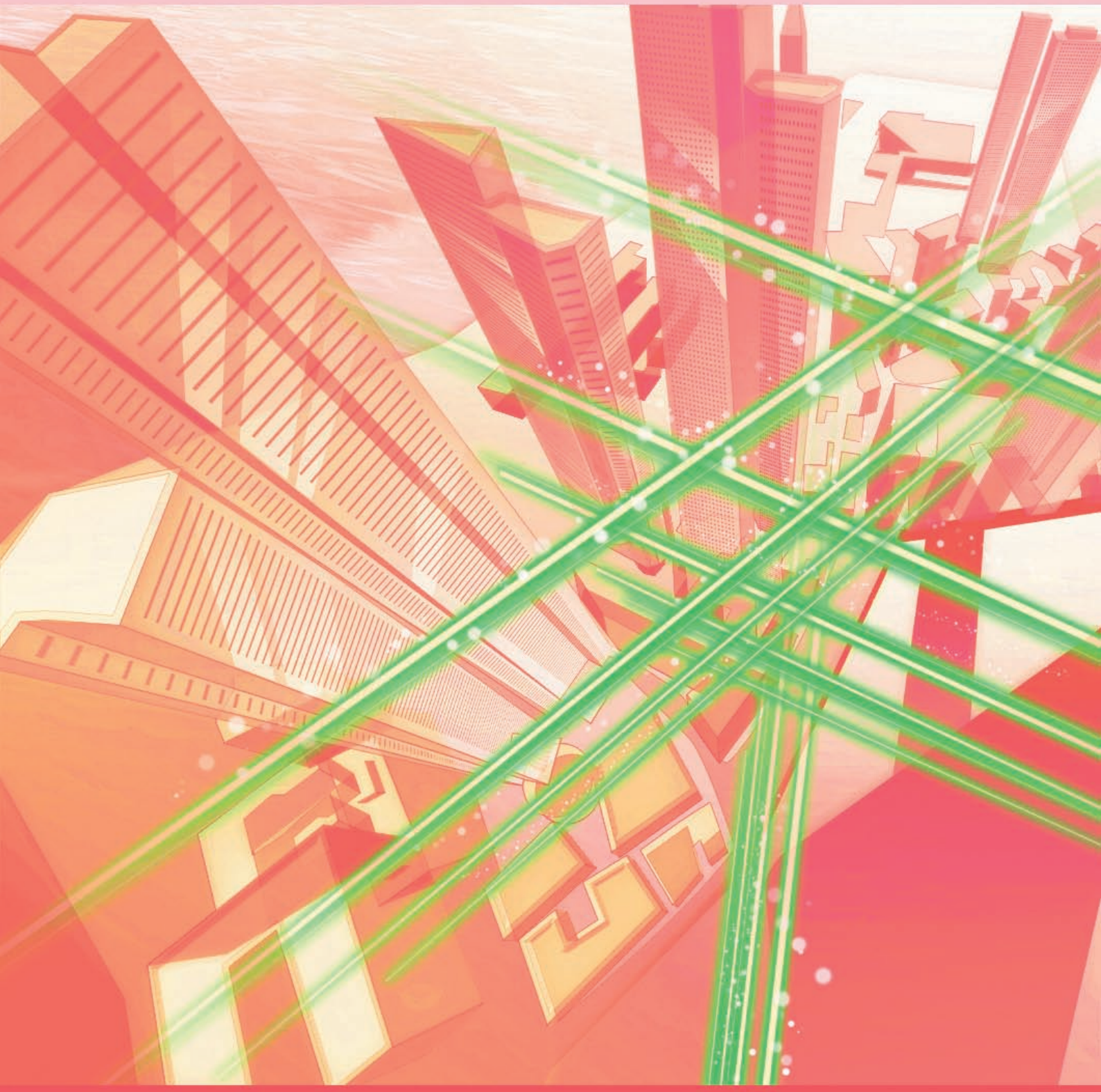

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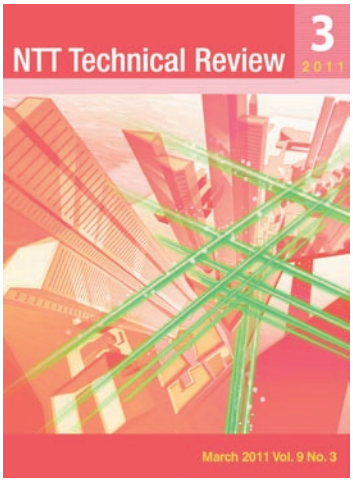

Toward Life-enriching Technologies

Makio Kashino
Senior Distinguished Researcher
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Makio Kashino, an NTT Senior Distinguished Researcher, has enjoyed Japanese and Chinese classical literature since childhood. He has been particularly influenced by the *Zhuangzi* (classical Taoist book) by the Chinese author of the same name and the *Hojoki* (An Account of My Hut) by the Japanese author and poet Kamo no Chomei. Both of these philosophize about the impermanence of worldly things. We asked Dr. Kashino, a unique researcher who attempts to explain *hearing* and *communication* from the viewpoints of psychology, neuroscience, and information science, to tell us about the manner, significance, and future of his type of research.

Probing the human mind via an integrated approach

—Dr. Kashino, could you first give us some background to your research?

Since entering NTT, I have been exclusively researching human perception with a focus on human auditory mechanisms. While hearing a sound may appear to be easy, it is actually a very complex process. If you visit the Illusion Forum website [1] that we have created, it's plain to see, or rather, it's plain to hear, that this is so. In hearing, a variety of peculiar things can occur; for example, you might hear nonexistent sounds or hear the same sound in different ways. Such phenomena are manifestations of brain functions that enable humans to adapt to their surroundings. In my research, I have been working to elucidate these clever neural mechanisms.

In this kind of research, I have found it essential to integrate three approaches. The first is to quantify the features of human perception, as in the case of illusions such as those that I just mentioned. The second is to study the workings of the human brain and nervous system that serve as the hardware for achieving those features. And the third is to comprehend the principles of information processing that make those features possible in the first place. In other words, we can begin to explain the mechanisms of *hearing* through the three fields of psychology, neuroscience, and information science. Let me make an analogy here. If I were to research the flight of birds, I could not simply analyze wing strokes and the structures of wings and muscles: I would also need to understand the principles of flight, that is, of aerodynamics. Only then would I be able to apply the knowledge gained to aircraft.

—What is your current research theme?

Well, my research is still centered on hearing, but I am currently working to broaden the scope of my studies. It occurred to me that this integrated approach that I've developed could perhaps be used to scientifically explain heretofore elusive problems like preferences and feelings. Let me give you three specific examples of this expanded research in our group.

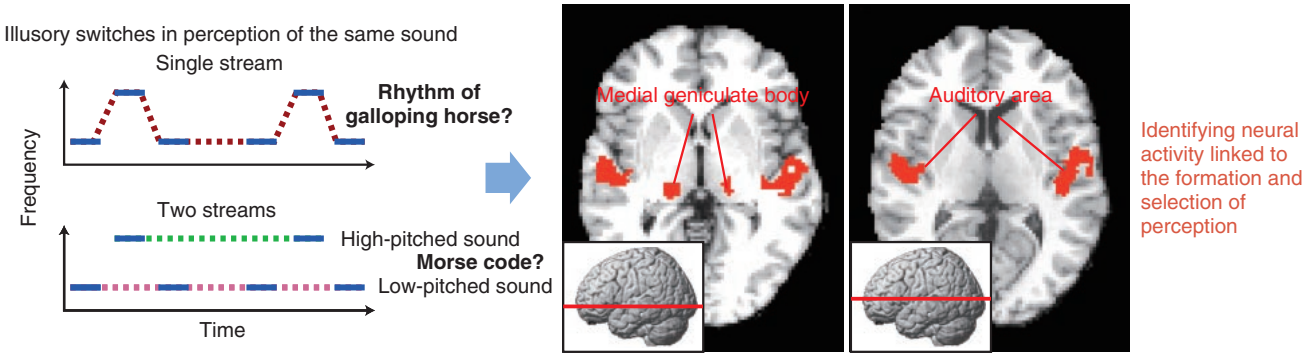

Fig. 1. Uncovering neural information-processing principles from an illusion.

First, in relation to hearing, we're researching the neural mechanism that enables one to selectively listen to only what one intends to hear in a mixture of many sounds. (**Fig. 1**). This *cocktail party effect* is often said to be an outstanding feature of human hearing, but it tends to be deficient in some groups of people such as the elderly and hearing impaired. A hearing aid often just amplifies noise as well, resulting in no substantial improvement in hearing. In our research on testing hearing ability, we have found that some people who show no apparent abnormalities in an ordinary otological test may sometimes have difficulty hearing a sound in the presence of competing sounds. We have been investigating a new hearing test that can identify such people and we are close to finding the cause of this phenomenon.

Cases in which a hearing problem can hinder an individual's full participation in society despite ample skills or motivation are expected to multiply as we enter the aging society. The creation of a barrier-free society is a key objective of information and communications technology (ICT), and I think that we can help give many people a greater sense of purpose in their lives if we can develop a hearing aid that lets them hear only what they prefer to hear.

Second, we're researching ways of quantitatively predicting preferences in relation to music, design, etc. For example, a person may respond favorably to certain kinds of music saying something like "that's good" or "I like that music." In such a case, the music is probably somewhat familiar and not completely new to the user. In other words, music that is all too common for the listener can be boring while something that is too novel or original may turn the listener off. So how new should something be to be the most attractive?

The ability to derive this in theoretical terms would no doubt bring big changes to the way that products are designed and advertised. Traditionally, design and advertising have depended on the experiences and hunches of those in charge, but a systematic approach could make the process more efficient. All this might sound too good to be true, but I believe that such predictions should be possible to some extent by applying the principles of neural information processing. What we need here is some kind of proof, and to this end, we are conducting various types of experiments.

Third, we're researching subliminal signals and body language (**Fig. 2**). In interpersonal communication, information that cannot be directly conveyed by words plays an important role. In particular, the atmosphere between two people is often created by slight changes in facial expression or tone of voice that are usually unnoticeable to either party. This type of unconscious exchange of implicit information between two people helps to establish smooth communication. We are now working to explain the actual mechanisms of nonverbal communication through experiments that measure slight body movements, physiological changes, and neural activity during interpersonal communication.

Such implicit information was probably discarded as unnecessary in past technologies because, in conventional communication systems, it was sufficient to assess whether a phrase like "thank you" was actually heard as "thank you". As a consequence, information that could convey whether this "thank you" was actually an expression of gratitude or a sarcastic remark was simply ignored. However, if such elements of communication can be clarified, it should be possible to achieve a form of communication with a high level

- Implicit interpersonal information (IIPI) is unconscious (implicit) body movements or physiological responses made by one or both parties while they are communicating with each other.
- Basic hypothesis: IIPI is the foundation of subliminal signals.
- IIPI and its underlying neural and nervous-system activities can be used to clarify and appropriately control emotions and the state of communication.

Supported by JST CREST (research representative: Makio Kashino (NTT); coworkers: Shinsuke Shimojo (California Institute of Technology) and Katsumi Watanabe (The University of Tokyo))

Fig. 2. Clarifying subliminal signals based on IIPI.

of presence such as in a videoconference system connecting remote locations via the network.

Toward a career in hearing research from an attraction to temporal flow

—What moved you to become a researcher in the field of hearing?

Most of my instructors and seniors in my university research laboratory were researching topics related to vision. For example, they were studying the response of goldfish retina cells to light, the neural activity of monkeys, and human visual illusions. Moreover, my advisor was researching mathematical models of visual pattern recognition. I learned a lot about methodology from my involvement in these studies. However, I had developed an interest in sounds through listening to a wide variety of music and building electronic gadgets from discarded parts starting in my elementary school days, and what I really wanted to research was the perception of sound, or in other words, hearing. In Japan, there were not many researchers in this area. I could therefore pursue this interest to my heart's desire, which suited me perfectly.

In addition, since my childhood, I've been interested in how one captures things that change and the nature of impermanence. Living things move and change, and this change occurs continuously together with a *temporal flow*. I found this flow to be very appealing.

At the same time, I thought that sound, which cannot exist without incessant change, is closer in essence to flow than vision. This is also one factor that led me to specialize in hearing.

—What kind of researcher do you think you are?

I believe that my motivating force is a philosophical awareness of problems, but in my case, pure speculation by itself has its limits. Come to think of it, I've enjoyed doing experiments since my childhood. What I like about experiments is that they do not always turn out as expected. Of course, if we establish a certain hypothesis, perform an experiment to test it, and obtain a result that meets our expectations, then it's time to celebrate! But this could also be boring in the sense of a pre-established harmony as discussed in philosophy. An unexpected result, on the other hand, can broaden our scope of thought and be much more interesting. If we give lots of thought to an unexpected result, we may find it to be the most natural outcome after all.

At the same time, I also enjoy theory, and it gives me great pleasure to be able to provide a uniform explanation for perplexing things or unrelated things through simple principles. In short, a continuous cycle of theory and experiment is essential to my integrated approach.

Baseball and work: *unconditioned nature*

—I've heard that pitching—as in baseball—is a hobby for you.

Yes, that's right, but not in the sense of playing sandlot baseball just for fun. What I pursue is simply the act of throwing with great devotion. I do this every day if possible. But please don't ask me why I do it. Perhaps I find the act of throwing one ball after another interesting like the cycle of hypothesis and experiment. At any rate, one throw out of maybe 30 or 40 surprises even me. But if I get all excited and try to do it again, I end up making a throw that's not nearly as good. This is very strange.

A ball is thrown not by the power of one's arm but rather by accelerating the tips of one's fingers to the utmost through power generated by the movement of one's weight and the twisting of one's lower body. An arm that is simply shaking looks exactly like a flexible whip. However, when you consciously attempt to throw a fast ball, excessive power will enter your arm and shoulders, and at that instant, the power that would normally be conveyed by the lower part of your body and by your trunk will fall behind. It so happens that when I fall into some kind of rhythm and stop worrying about my next pitch, I get this sensation of being driven only by gravity and inertia and I end up making some incredible pitches while feeling quite relaxed.

Perhaps this is an example of *unconditioned nature* as described in the *Zhuangzi*. In some way, you can perform your best when you lose the self and do not fight the providence of nature (when you go with the flow). If, by plain luck, you were to throw a great ball, it could then be said that you already had it in you to do so, but the problem now is whether you can invoke that ability at will. In other words, the problem is how to coordinate with good timing the roughly 400 skeletal muscles in the human body without mutually cancelling out the flow of power through them. It is said that the great baseball player Ichiro, though having a thin figure, can outperform other major-league players far superior in strength by optimizing muscle coordination.

For this reason, I do not go out of my way to build up my muscles, but look for ways of improving my coordination. I feel as if I'm advancing little by little, and I don't think it's altogether unrealistic to aim for a pitching speed of 130 km/h at 50 years old.

The importance of natural coordination should also hold true in work. The more one thinks about having to go all out, the more one's natural pace will fall apart without any gain in performance. This also applies to management in an organization. If superiors in their excitement to excel assign useless work, subordinates are bound to become exhausted. Whether it be an individual or an organization, I don't think that intrinsic potential can be tapped in this way. It must be said, however, that working in a natural way is really difficult.

Future outlook for ICT

—What do you think is the future of ICT?

The research that I conduct aims to elucidate this providence of nature. In other words, I am involved in scientific research, but at the same time, I am deeply concerned with the future of ICT. As a basic belief, I feel that ICT is not simply a means of making life more convenient—it must also serve to enrich the lives of human beings. And to this end, ICT must help people achieve their intrinsic, natural state of being. Accordingly, basic research on clarifying the providence of nature in relation to human beings should, in the end, lead to a form of ICT that works to enrich people's lives.

It would be natural to think that ICT could be used to good effect by establishing a barrier-free society and to assist the sensory and motor functions of the elderly. But on a long-term basis, what if such measures turned out to actually weaken brain functions? My answer to this is to make use of nature and

isolate and enhance intrinsic neural and physical functions. Ideally, there would be a set of tools that can do just that.

While it is easy to measure the efficiency and physical performance of just about any product, it is difficult to measure the extent to which such a product actually enriches a person's life. It is exactly this point that should become a matter of importance in the years to come. The provision of top specifications and high quality is a matter of conscience for certain types of enterprises, but as a natural precondition for this, I believe that products should be designed taking into account feelings and perception so that possessing a product brings some delight into a person's life. For this reason, feelings and perception should be subjects of discussion in scientific and engineering fields.

Today, Japan provides the fastest and most inexpensive broadband environment in the world. The optical-fiber service area covers 90% of all households, but no more than 30% are actually making use of these services. Why are the remaining 60% not using broadband? No doubt price is one factor, but could another factor be not actually being able to feel the value of broadband? Do these households perhaps feel that their current way of using the web, email, and weblogs (blogs) is more than sufficient? If a household were to upgrade to broadband or introduce ICT, to what extent would the lives of its family members be enriched? Customers don't think in these terms, and neither, I suspect, do service providers. Here, remote medicine, to give one example, could be used not simply as a means of transmitting digital medical records but also to encourage interest in broadband and ICT. So there's still hope. I feel strongly that disseminating such a concrete image of broadband services should be the responsibility of us basic researchers.

To young researchers

—Dr. Kashino, please leave us with a message for young researchers.

It is often said that originality is essential for researchers, but I feel that the meaning of this is sometimes misinterpreted. In particular, in today's competitive society, we are made to feel like a failure if we don't do something different from other people, and we start out by thinking "How can I do something unique?" However, great baseball players like Nomo and Ichiro were not great just because they had different forms of play. Each worked ceaselessly to optimize his individual performance and simply came to adopt that form as a result. While appearing to be unique at first glance, their forms of play owe a lot to the providence of nature.

I think this also holds true in research. The etymology of the word original is origin, and the origin of ICT is to find out what is needed to enrich people's lives. If we return to this origin and listen carefully to the voice of nature, I think that we should be able to perform great work.

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He received the B.A., M.A, and Ph.D. degrees in experimental psychology from the University of Tokyo in 1987, 1989, and 2000, respectively. He joined NTT in 1989. He has also held various posts outside NTT including those of visiting scientist at the University of Wisconsin (1992–93), visiting professor at Tokyo Institute of Technology (2006–current), invited professor at l'Université Paris Descartes (2008), and project leader of a CREST (Core Research of Evolutional Science & Technology) project of the Japan Science and Technology Agency (JST) (2009–current). His research field is cognitive neuroscience of human perception and communication.

System LSI Design Technology for Communications Networks

Tsugumichi Shibata†, *Mamoru Nakanishi, and Mamoru Kitamura*

Abstract

The first set of Feature Articles in this issue describes research and development of system large-scale integration (LSI) technology (also known as system-on-a-chip (SoC) technology) and high-speed front-end electronics for optical access systems being conducted at NTT Microsystem Integration Laboratories. This article provides an overview and the other articles discuss their roles and characteristics well as related design technology and issues.

1. Introduction

Opportunities to use a variety of applications on the Internet in daily life are increasing, and Internet access is becoming indispensable. It is desirable for high-quality, convenient, and safe application services to become even more common. This is backed up by the existence of a secure, broadband network services infrastructure utilizing the low losses of optical fiber and the broad bandwidth of light, so networking advances should contribute to a more vibrant, rich, and plentiful society. Optical networks have various components, each playing an important role, including (1) optical devices such as light sources, modulators, transmitters, splitters, and multiplexers; (2) electrical devices that reproduce and process signals and communications protocol controllers; and (3) software that operates them and the communications systems they are part of. At NTT Microsystem Integration Laboratories, one focus of our work is research and development (R&D) of electronics for these communications systems of these types.

Among electronic device technologies used in telecommunications systems, ones that we view as particularly important include system large-scale integration (system LSI), which is also known as system-on-a-chip (SoC) technology, which provides sophisticated communications functions, and optical front-end integrated circuits (ICs), which perform high-speed signal processing. SoC technology generally refers to implementations that include a central processing unit (CPU), memory, and large-scale dedicated logic, along with the software to operate it (**Fig. 1**). SoC technology is used widely, including in general-purpose and household products, but we focus on applications for communications systems using SoC devices (SoCs) that incorporate our experience and knowledge as a communications carrier and contribute to the advancement of communications

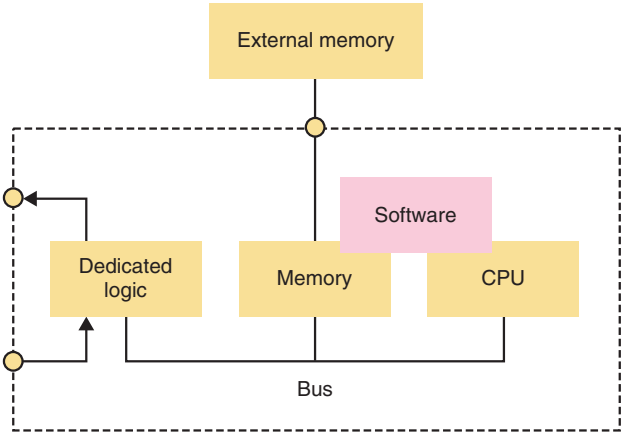

Fig. 1. Elemental SoC architecture.

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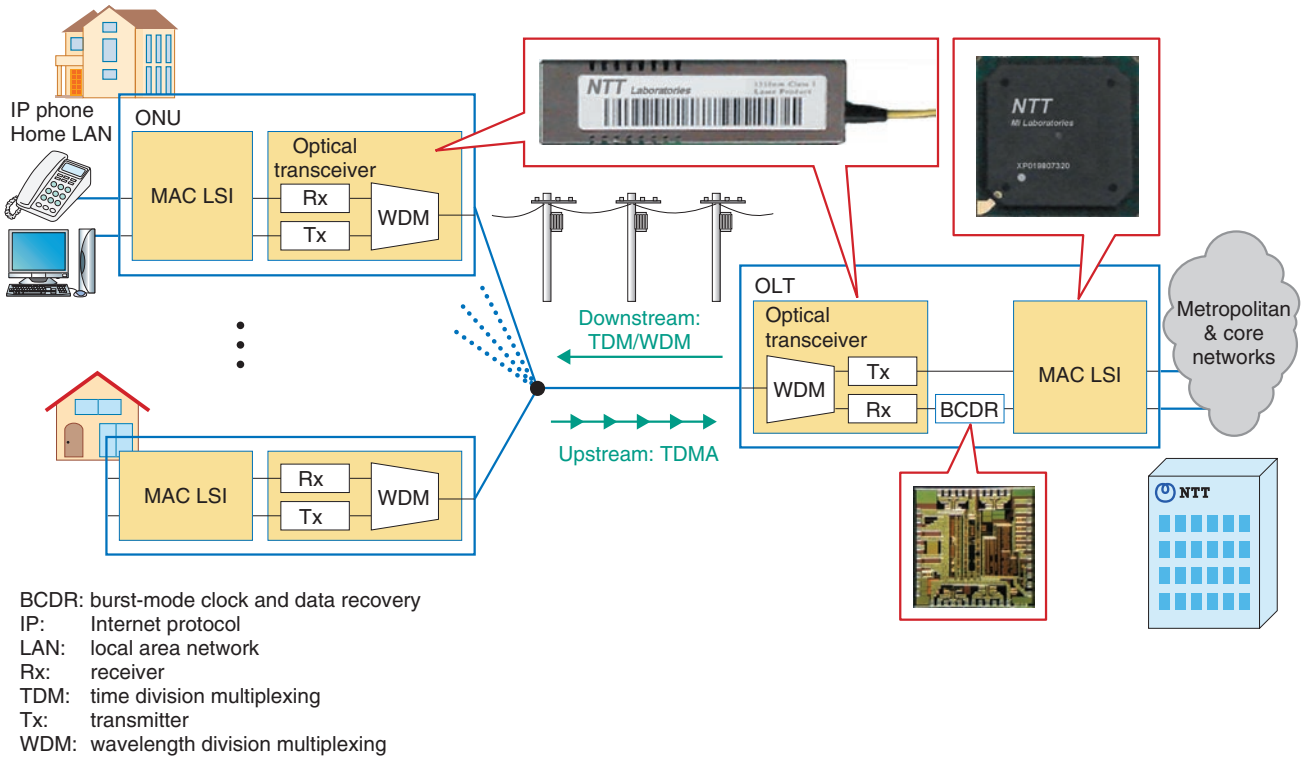


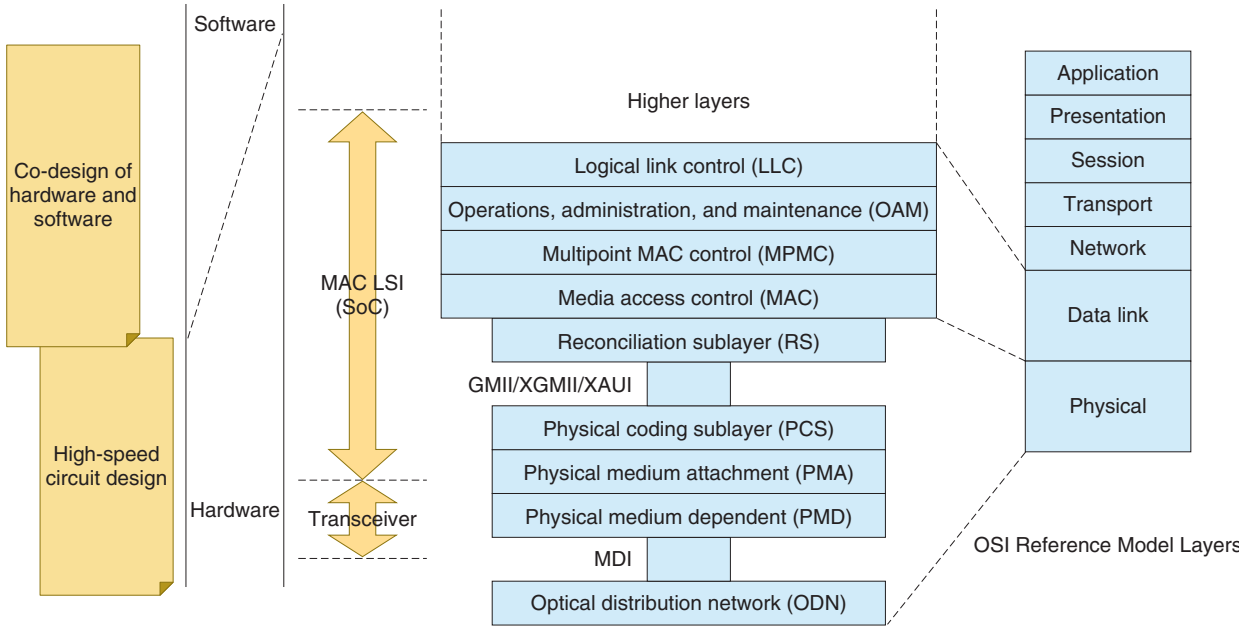
Fig. 2. Electronic devices used in an Ethernet PON system.

systems. We are conducting R&D of SoC design technology, including hardware and some of the software, in cooperation with other research laboratories working in the field of communications systems.

2. SoC design for optical access networks

In Japan, most broadband access services are currently provided by fiber-to-the-home (FTTH) access, and they mostly use the GE-PON (Gigabit Ethernet passive optical network) system [1], [2]. A block diagram of an Ethernet PON system is shown in **Fig. 2**. A PON allows services to be provided to multiple customers economically by branching a single fiber. It requires the formation of a secure and efficient point-to-multipoint (P2MP) connection between the optical line terminal (OLT) on the network side and the optical network units (ONUs) at the customers' locations. This is done by sending upstream signals from ONUs to the OLT by using time-division multiple access (TDMA), which is controlled using the multipoint control protocol (MPCP). The main functional components of the OLT and ONU are media access control (MAC) LSIs, which are SoCs, and optical transceivers. The MPCP processing function is implemented in the MAC LSI. Furthermore, the optical transceiver must be able to amplify and regenerate burst frames sent from multiple ONUs when frames have different timings and optical intensities. The electrical components in this optical transceiver are called the optical front-end ICs. At the beginning of system development, functions that could not be included in the SoC were implemented using external components, but as the technology advanced, more of the functions could be integrated into the SoC, reducing the number of parts and overall cost.

Standardization of 10G-EPON (10-Gbit/s Ethernet PON), the successor to GE-PON, has recently made progress [2]–[4]. We have responded to this by establishing technology for implementing the standard functions of 10G-EPON in SoCs and optical front-end ICs. We have also conducted feasibility studies on achieving more-sophisticated and higher-performance devices. Below, we discuss the characteristics and technical directions for SoCs and optical front-end ICs in the context of Ethernet PON systems.



GMII: Gigabit media independent interface
MDI: media dependant interface
OSI : open systems interconnection
XAUI: 10 Gigabit attachment unit interface
XGMII: 10 Gigabit media independent interface

Fig. 3. Architectural positioning of P2MP topologies in the IEEE 802.3ah "Ethernet in the First Mile" and their implementation by the transceiver and the MAC LSI.

3. Cooperative design of hardware and software

When one is implementing the required functions in an SoC, a major issue is to develop design methods that optimize the partitioning of functionality between functions implemented in hardware with dedicated logic and functions handled by the CPU using software and to generate interfaces between them.

For communications operators like NTT, a major concern is whether the systems being developed are flexible enough to accommodate extensions for future services, maintenance, and monitoring functions. Up until now, the general approach to implementing these types of flexible functionality in SoCs has been to use software, but if cooperative design of hardware and software were easier, then circuit configuration and control could be done in more detail, allowing one to pursue both extensibility and flexibility.

Moreover, a basic performance requirement for OLTs, ONUs, and, in general, network switches is the capability to process signals at *wire speed*. To handle the requirements of increased traffic, transmission capacity must be expanded and data must be processed without any frame loss, which places a demand for increased performance on SoCs. To achieve this high performance, hardware techniques for increasing speed play an important role, such as using faster algorithms for logic circuits, parallelization, and pipelining, but we believe that we should also be able to make breakthroughs in power saving for the overall system through better cooperation between hardware and software and by controlling hardware according to actual traffic conditions.

4. MAC LSI functionality

The P2MP architecture [5] specified in IEEE 802.3ah, the standard for Ethernet PON systems, and the way in which the architecture is implemented using MAC LSIs, transceivers, and other components are shown in **Fig. 3**. Most of the functions required by the system are implemented in the MAC LSI. Most of the functions required by the system are integrated on a single chip, focusing on the various Layer 2 switch (data-link layer) functions from higher-ranking

functions such as encryption to physical-layer functions such as encoding and serial/parallel conversion.

5. Research on optical front-end ICs

NTT Microsystem Integration Laboratories, together with the NTT Photonics Laboratories, is continually advancing R&D of optical front-end technology. Optical front-end ICs, include amplifiers that reshape in the receiver the weak signals attenuated by transmission through the fiber, digital-data retiming and regeneration circuits, and laser-driver circuits required to produce good quality signals in the transmitter. In the system, these are sections with strict analog requirements, such as sensitivity, feedback or feedforward control, and dynamic range; moreover, they require broadband operation. Furthermore, there is the additional difficulty, mentioned earlier, that data frames arrive at the OLT in burst mode in the PON system. Research issues for these circuits are more physical compared with large-scale SoCs, involving transistor-level circuit design, as well as the physical layout of the circuit and packaging. The selection of semiconductor technology is also an important factor in satisfying performance requirements. We consider (1) compound semiconductors such as InP for heterojunction bipolar transistors (HBTs) and high electron mobility transistors (HEMTs) and GaAs for metal semiconductor field effect transistors (MESFETs), (2) silicon bipolar-junction transistors integrated with complementary metal-oxide semiconductor (CMOS) transistors on a single substrate (Si BiCMOS) including silicon-germanium BiCMOS (SiGe BiCMOS), which integrates SiGe HBTs with conventional CMOS processing, and (3) silicon CMOS (Si CMOS) from cost and performance perspectives and select the optimal technology for a given application.

In R&D of optical front-end ICs, there are two key points to consider. First, as with other long-term basic research, it is important to ascertain the feasibility of the technology. When planning and developing innovative services or systems, one must verify in advance whether they are achievable. For example, in order to progress from GE-PON to 10G-EPON, which is a ten-fold increase in transmission capacity, it is necessary to make front-end ICs that are ten times as fast at handling received frames. In particular, the frame header synchronization speed has a great effect on system design with respect to transmission efficiency. Moreover, sensitivity can have an effect on transmission distance or the number of customers that can be accommodated in a single optical distribution network. In this way, the performance levels achievable in the front end have a large effect on overall system specifications, so basic research in this area is done as a precursor to standardization. By conducting R&D in the area that is the physical bottleneck for performance, we will be able to contribute to higher system performance and lead the industry.

The second point is that there is synergy in having both SoC technology and front-end technology. Having experience with both makes it easier to study overall optimizations such as controlling the front end from the SoC or optimizing the chip partitioning and interface implementations. We want to use this synergy as one of our strengths in proceeding with R&D.

6. Organization of the Feature Articles

This topic has five Feature Articles, including this one which discussed our initiatives related to SoC technology for optical access communications systems and optical front-end IC technology. Next, “Cooperative Hardware/software Design Technology” [6] describes a high-level design technology using virtual hardware effectively for the initial stages of design, including cooperative design. “MAC LSI Design Technology for Optical Access Communications” [7] explains the LSI design process flow and discusses the architecture of an Ethernet PON SoC in detail. “Design Verification Using Field-programmable Gate Arrays for Optical Access Communications SoC” [8] introduces a technology for verifying large-scale SoC functions using field programmable gate arrays before chip prototypes are created. Finally, “10-Gbit/s Burst-mode Receiver Integrated Circuits for Broadband Optical Access Networks” [9] introduces the state of development of optical front-end IC technology for 10G-EPON systems.

7. Future trends

At NTT Laboratories, we will continue to expand our R&D efforts toward improving the value provided to customers and resolving business issues. To do so, we will continue development of SoC technology in order to further increase system performance, pursue “Green of ICT” much further, and contribute to making systems more flexible by improving customizability and other aspects (ICT: information and communications technology).

Until now, the integration level of LSIs has increased according to Moore's Law* year after year, and this has been the force behind progress in the functionality and performance of semiconductor products. At the beginning of this century, there was some serious discussion about reaching practical limits for reductions in the size of semiconductor processes, but now it appears that some of the fabrication process problems will be solved, and the International Technology Roadmap for Semiconductors (ITRS) [10] has continued to issue roadmaps for still finer technologies. Accordingly, there is hope for continued progress in SoCs and communications systems through R&D driven by leading-edge processes.

On the other hand, in addition to active R&D on further miniaturization (*more Moore*), new functional materials and devices are being developed, in synergy with miniaturization (*more than Moore*), and research on utilizing more-than-Moore technology for communications systems in the medium-to-long term will also be important.

* Moore's Law: A law that states that the density of semiconductor integration will double every 18 to 24 months.

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Cooperative Hardware/software Design Technology

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Abstract

In this article, we introduce a hardware/software co-design simulation method for testing the cooperative design of hardware and software for system-on-a-chip (SoC) devices. For SoCs, which incorporate dedicated processing circuits and a processor, combined testing of the software running on the processor and the operations of the dedicated circuits must be done from the initial design stages in order to reduce the amount of redesign and the turnaround time, i.e., the number of person-hours of work required. Our cooperative simulation method uses virtual hardware. We discuss its effectiveness by referring to real examples.

1. Introduction

In the design of system-on-a-chip (SoC) devices, it is extremely important to design so that the hardware, which handles specialized processing, and the software running on the microprocessor, operate cooperatively. In other words, the design process must also be cooperative. How can this be tested?

The microprocessor operates according to what is written in its program (software). On the other hand, the dedicated processing circuits process data continuously according to how the hardware has been designed and a clock signal. Thus, the operation of the two must be checked to ensure that they do not cause a conflict, mismatch, deadlock, or other type of performance drop. This is cooperative design evaluation.

The evaluation results can affect the system architecture greatly, so such an evaluation must be done from the initial stages and from the top level of design. However, at the top-level design stage, there is no actual hardware. It would be nice to build an overall prototype including both the microprocessor and dedicated circuits, put them together and test them, but development usually cannot wait for this. Systems being implemented as SoCs have recently become extremely complex, so that even building or rebuilding a single prototype can take several weeks or months. For this reason, it has become necessary to simulate the hardware together with the system software before prototyping it; in other words, one must perform a hardware/software co-design simulation.

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2. Virtual hardware

To implement co-design simulation, we need a simulator for virtual hardware. Physical hardware operates with a clock signal for input and output to the dedicated circuits so the processor can read from and write to it, but virtual hardware does not have a physical clock. Instead, attention must be paid to the sequencing and dependencies of reading and writing and to the input and output between the processor and dedicated circuits, and the simulator must be built to maintain these relationships.

Before the design of the dedicated circuits is complete, one does not know how many clock cycles will be required for these circuits to complete their operation. However, the correct sequencing and dependencies for reading and writing are correctly coded in the virtual hardware, so the virtual hardware can respond to the software behavior without conflict. This makes co-design simulation possible from the top-level design stages.

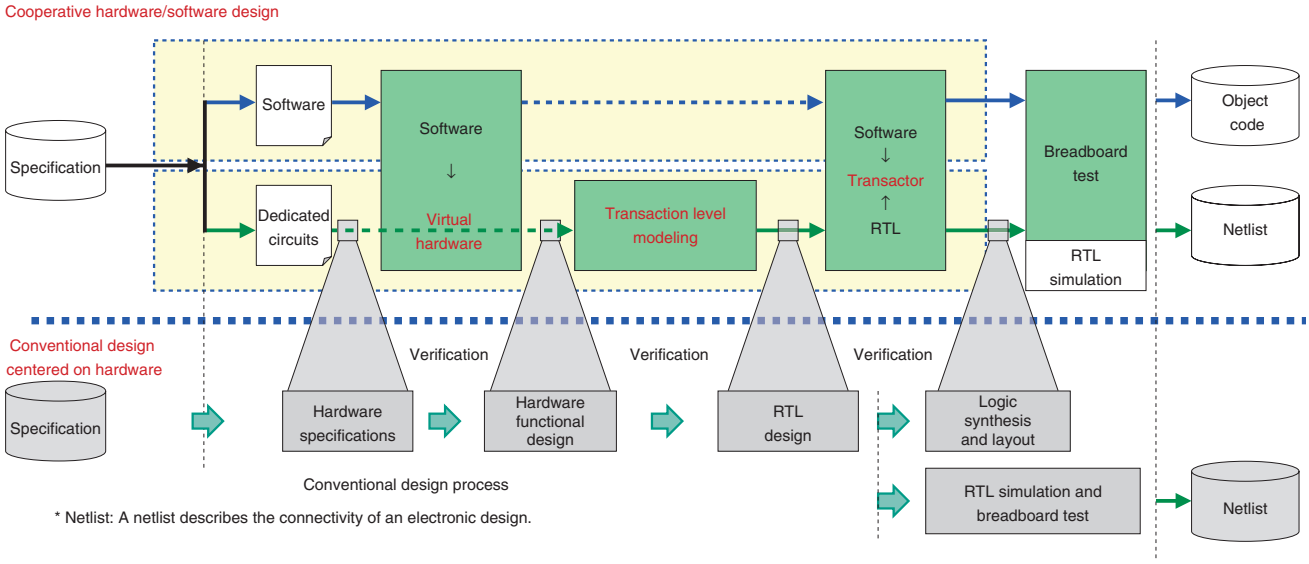


Fig. 1. New design process that allows cooperative testing with software.

3. Issues being addressed

We have applied this type of co-design simulation using virtual hardware to the evaluation of SoC designs for optical access systems. As a result, we have confirmed the usefulness of the method. The new process is shown in **Fig. 1** together with the conventional design process. The lower half of the figure shows the conventional design process centered on hardware. Here, the hardware was the only specification to achieve. However, in hardware/software co-design, which allows cooperative testing with the software, part of the specification is achieved with software. The hardware/software co-design process can handle a wider specification range than the conventional design process. Moreover, whereas the conventional design process creates a hardware netlist, the cooperative design process creates two netlists—one for the dedicated circuits and another that connects the processor and dedicated circuits—and software object code that controls the processor's behavior. Therefore, Specification and Netlist are grayed out in the lower half of Fig. 1 because they cover different ranges to those in the upper half.

The dedicated circuits are designed according to the conventional hardware design process: they become more detailed in three stages from specifications to functional design and register transfer level (RTL) design. Software cooperative testing (verification) can be done at each of these three stages by using co-design simulation with virtual hardware.

We started by building the virtual hardware (leftmost green box in Fig. 1.) for the initial stage (specification design). This allowed early verification of the SoC software.

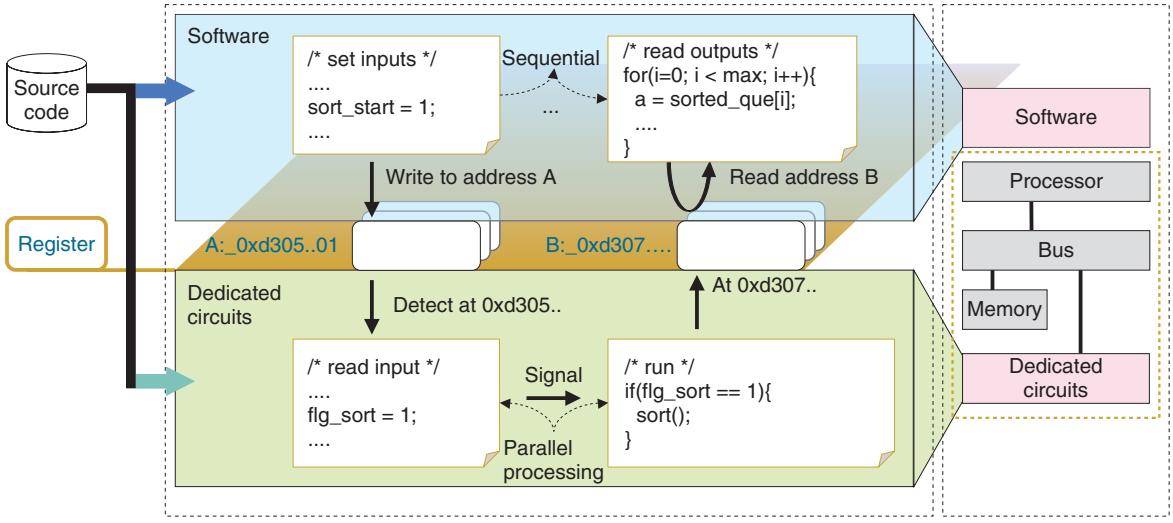
Then, at the intermediate stage (functional design), we addressed the hardware transaction-level design (second green box). This can be simulated several times faster than when designing in detail to the RTL level.

Finally, at the RTL design stage, we built a mechanism called a transactor (third green box) into the system for sections connecting the dedicated circuits with the processor. This enables precise final verification of the interfaces between hardware and software in the SoC.

4. Construction of virtual hardware

We verify the software at the specification design stage with the goal of determining aspects such as whether adequate performance is achieved and whether performance will drop owing to interference with the dedicated circuits. The software is not executed independently, but loaded on the original SoC architecture, which includes both the processor and dedicated circuits. Thus, we have built virtual hardware that simulates the entire SoC, as shown in **Fig. 2**.

The key to building virtual hardware is the separate



* http: //www.synopsys. com/Community/Interoperability/SystemLevelCatalyst/Pages/MVaST.aspx

Fig. 2. Virtual hardware.

parts for software and dedicated circuits, which are where the processing that defines the functional characteristics of the SoC takes place. For our optical-access SoC, these characteristics were the ability to interface with sophisticated, high-speed communication lines. The specifications for these components are complex, so they were expressed not only in documents, but also as source code in the C programming language. To ensure that the implementation was faithful to the specifications, we built the dedicated circuit part of the virtual hardware by directly using this C source code as far as possible.

The source code includes both the software that will be loaded by the processor in the SoC and the software representing the dedicated circuits. Communication between them uses registers, which create the correspondence between variables in the software and variables for the dedicated circuits, so the address-mappings for these registers must be managed. The mechanism of communication between software and a dedicated circuit conducted via a register is shown in Fig. 2. When the software side writes to address A, the dedicated circuit side detects it as being written at address 0xd305… (in hexadecimal). Because the dedicated circuit is always processing, the influence of the write will sooner or later be written at address 0xd307…, which is equivalent to Address B on the software side. The software side reads values from Address B according to the execution order and conditional judgment. The dedicated circuit reads the value that was written earlier to Address B, and, as a result of the dedicated circuit procedure, its behavior when it reads Address B reflects the software side.

The number of these registers is generally very large. Most of the specification is related to these registers, so any updates to the specifications can involve a significant amount of rewriting in the virtual hardware. This results in additional design work, so we used data structures, which allow us to manage all of the registers at once and make it easy to apply updates to the specification.

This approach can be generalized, decreasing the amount of time required from confirmation of the specifications to system-level operation. For the current project, we were able to detect routines that were performing inadequately several months before beginning verification of the physical hardware.

5. Transaction-level design

In the same way that software performance can be checked using virtual hardware, the dedicated circuits can be simulated at the functional design stage. This simulation is faster than RTL-stage simulation, but it must be done using transaction level modeling (TLM) to describe the transaction-level design.

In the past, for functional design simulations, each of the lines between modules would be simulated individually and in complete detail, down to individual

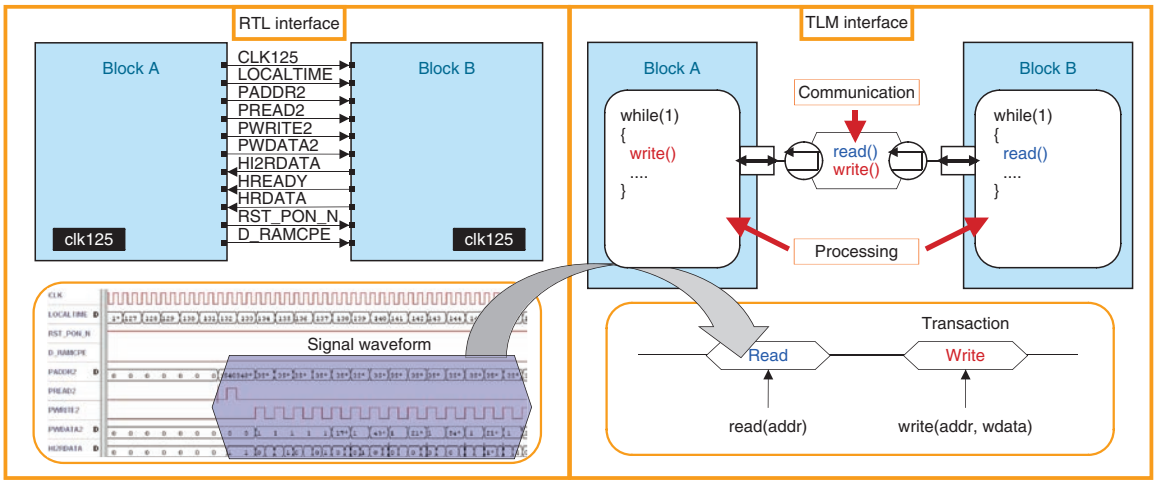


Fig. 3. TLM interface.

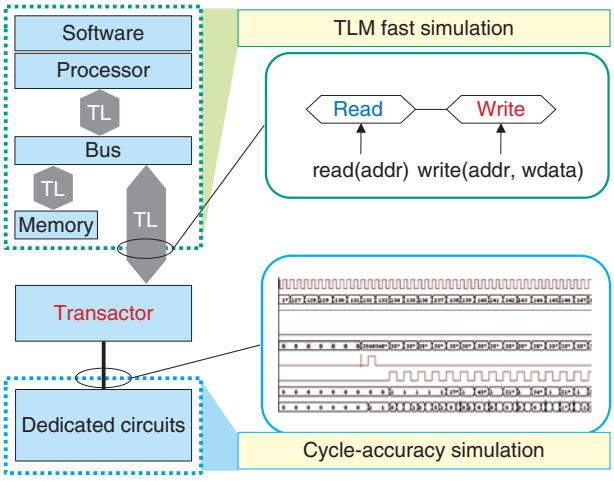
clock cycles. This resulted in a number of problems. First, a lot of work was required to complete the detailed design before simulation could begin; moreover, component redesign because of interference with other blocks could have a major effect on the design schedule [1]. Second, a detailed simulation could not be executed quickly and consumed much time. Third, the test coverage was difficult to manage [2].

To resolve these difficulties, we used SystemC [3] TLM to structure the design file for the dedicated circuit section. At the functional design stage, testing must verify points where data is exchanged between blocks. The TLM interface between blocks A and B is compared with the RTL interface in **Fig. 3**. When a block passes the results of its processing to another block, the procedure can be very long, as in the RTL case on the left. However, this procedure can become very simple, as shown on the right side, if the exchange is rewritten as a transaction. A transaction is the core action, such as the start or confirmation of a transmission or reception. The events handled in a simulation using TLM are arranged beforehand, so simulation can be done at high speed. When TLM is used, descriptors for the lines connecting blocks are much shorter, and this effectively reduces the amount of preparation work for simulation. Overall, the amount of descriptor code was about one-tenth of that for RTL, and the simulation executed about 100 times as fast as the RTL simulation.

6. Built-in transactors

Completing an RTL design of the dedicated-circuit section enables precise simulations to be done in block units, but problems arise when cooperative simulation is performed. The processor in the virtual hardware does not have actual signal lines, so the RTL for the dedicated circuit section cannot be connected to the virtual hardware as it is.

Thus, we built transactors into the virtual hardware, as shown in **Fig. 4**. Transactors are composed of libraries provided by the existing simulation infrastructure [4]. We used library functions to code the transactor to monitor accesses to the bus by the RTL of the dedicated circuits. When an access is detected, a function updates the register value at the appropriate address. Figure 4 shows a transactor connecting two simulators: the lower one simulates the dedicated circuits with cycle accuracy and the upper one simulates the software-equipped processor with fast TLM. The grey areas labeled TL (transaction level) mean that a TL connection is used when these areas are simulated. In the processor and bus in this area, when each part performs communications with the other part, the performance is set using a TL write. The TL connection enables communications to be performed with transaction between connected parts (models) and leads to high-speed simulation. On the other hand, the area of dedicated circuits is written to enable simulation with more detailed cycle accuracy. There is no way to connect directly between an area that uses TL connection when simulated and another



TL: transaction level

Fig. 4. Built-in transactors.

area simulated with cycle accuracy because the input/output signal formats are completely different. That is why a transactor plays the role of a mutual conversion function for the two communication methods.

With the earlier approach, we built a prototype board, reproduced the RTL on a field-programmable gate array (FPGA), and loaded the software onto the processor to evaluate the whole system. The data for writing the FPGA was created using computer-aided design, and this also required several weeks of preparatory work. In comparison, using the new method, the design for this project required only five person-days of preparation before evaluation was started. The method cannot replace all of the testing done with a prototype board, such as realtime signal processing, but final testing can be started several weeks earlier; the saved time is the time that would have been required to prepare the data for rewriting the board.

7. Cooperative design technology in the future

In this article, we introduced an example of applying cooperative design methods to the design of an SoC for optical access. Through this example, we showed that system-level cooperative simulation, at a level of precision appropriate and relevant for design stages as they progress, is possible for the dedicated circuit components, from top-level design to the final processes.

In the future, it will become more important to do multistage cooperative simulation, from the beginning and in accordance with the design stages, when designing SoCs. The future possibilities enabled by this sort of design methodology are not limited to SoCs. Large-scale systems of even more complexity will fall into the scope of this research and we are taking on this new challenge.

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MAC LSI Design Technology for Optical Access Communications

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Abstract

In this article, we explain the development process and architecture of a media access control (MAC) large-scale integrated circuit (LSI). The MAC LSI is a very important component that provides most of the functions of an optical line terminal and optical network unit, which are the main devices in an optical access system. The required functions include the passive optical network interface, buffers, bridges, and maintenance & authentication.

1. Introduction

The development of a large-scale integrated circuit (LSI) begins with the definition of requirements. For this, the specifications of the systems in which the LSI will be used must first be decided appropriately. A media access control (MAC) LSI is a very important component in an optical access system because these LSIs provide most of the functions of the optical line terminals (OLTs) and optical network units (ONUs), which are the main devices. The MAC LSI is classified as a system on a chip (SoC) because it contains a central processing unit (CPU), memory, and large-scale dedicated logic circuits. When MAC LSI development begins, many details of the service and system specifications are still undecided, so while the specifications are being decided, close communication must be kept with internal departments studying the next-generation systems. For each system function, one must decide whether it will be implemented in the LSI or by using external components. As many functions as possible should be placed in the LSI to reduce the number of external parts and hence the equipment cost. However, as the number of functions in the LSI increases, the cost of the LSI itself also increases, so a good balance must be found.

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Requirements other than functionality must also be decided appropriately, including power consumption targets or performance parameters such as frame processing speed and processing time.

2. LSI design

After the LSI requirements have been decided, one must decide which of the functions are to be implemented in hardware and which in software. Generally, functions that require high performance are implemented in hardware, and ones that require a flexible configuration are done in software. For a MAC LSI, functionality must be allocated to satisfy the requirement that all input frames can be processed, without the speed dropping below the wire speed.

Once the hardware/software assignments have been decided, their designs can proceed. We try to keep the hardware design as small as possible while meeting the performance requirements, but we must also consider the following points:

(1) Each function should be able to be modified flexibly through configuration. This is so that, for example, if standards have not been finalized at the development stage, they can be accommodated even if they do change without the hardware needing to be rebuilt.

(2) At the beginning of development, in particular, in addition to the functions required for services, testing and debugging functions needed during

development should also be provided. Examples of functions of this sort are a loopback for the main signal, various counters, and internal signal monitoring functions.

The software can be categorized into components that access the hardware and those that do not, and the software design can proceed more smoothly if the hardware-accessing components are designed as application programming interfaces.

3. Coding and verification

The next part of the design is coding. For the hardware, we use a register transfer level (RTL) description with a hardware description language such as Verilog-HDL. For the software, we mainly use the C language.

Coding is followed by verification testing. Once the hardware has been built, making further changes is extremely expensive and time consuming, so testing must be done before production to eliminate as many problems as possible.

For the hardware, in addition to using logical simulation to check operations, we check some of the functions by actually running them using field programmable gate arrays (FPGAs) to emulate the hardware. Verification using FPGAs is discussed in detail in the fourth Feature Article in this issue, "Design Verification Using Field-programmable Gate Arrays for Optical Access Communications SoC" [1].

The operation of the software must ultimately be checked on the actual hardware, but as hardware and software development proceeds in parallel, the software must be tested as far as possible before the hardware is complete. For this purpose, a software model simulating the hardware is created. This is discussed in detail in the second Feature Article in this issue, "Cooperative Hardware/software Design Technology" [2].

When testing is complete, a logic-synthesis tool is used to create a netlist* from the RTL description. Once the RTL description has passed all testing, it is called the *clean file*, and a netlist created from this clean RTL description is passed to an LSI manufacturer for outsourced production.

4. MAC LSI architecture

Having given a step-by-step explanation of the LSI development process above, we now describe the architecture of the optical access communications MAC LSI.

There are several optical access methods, but as an example, we describe EPON (Ethernet passive optical network) here. There are two types of EPON [4], [5]: GE-PON (Gigabit Ethernet passive optical network) with a frame rate of 1 Gbit/s and 10G-EPON at 10 Gbit/s, but most of the following description applies to both equally. An overview of the EPON system is shown in **Fig. 1**. It is composed of an OLT, ONUs, optical fibers, and splitters. The OLT, which is usually in the provider's central office, is connected to the service network through the service node interface (SNI), and an ONU, which is usually on the user's premises, is connected to the user network through the user network interface (UNI).

The functions required by the OLT and ONU, with explanations, are given in **Table 1**. Each of these functions must be implemented either in the LSI or by using external components. For LSI implementation, each function is designed in a cluster called a functional block. The correspondence between functional blocks and these functions is shown in Table 1. The functional blocks are divided into two types: (1) functional blocks that receive, process, and transmit frames and (2) other functional blocks.

In Table 1, the dynamic bandwidth allocation (DBA) and CPU sections are of type (2) and the rest are of type (1). The MAC LSI architecture can be formed by arranging the type (1) functional blocks in the order of frame flow, and connecting type (2) blocks to the blocks that they control. Examples of OLT and ONU implementations using an LSI with this architecture are shown in **Fig. 2**. As shown clearly in Table 1 and Fig. 2, most of the functions of both OLT and ONU are implemented in the MAC LSI.

The MAC LSIs for the OLT and ONU in Fig. 2 have similar structures, but although they may share the same name for a functional block, there are differences in the functional blocks of the OLT and ONU, as described below.

(1) Within the EPON system, multiple ONUs connect to a single OLT, so all blocks except the SERDES (serializer/deserializer), SNI, and CPU in the OLT MAC LSI must be able to handle multiple ONUs.

(2) To implement the PON control function, the PON components of the MAC LSI for OLT and ONU must each transmit and receive control frames according to the well-defined sequence for each. The PON control function is described

* Netlist: A netlist describes the connectivity of an electronic design [3].

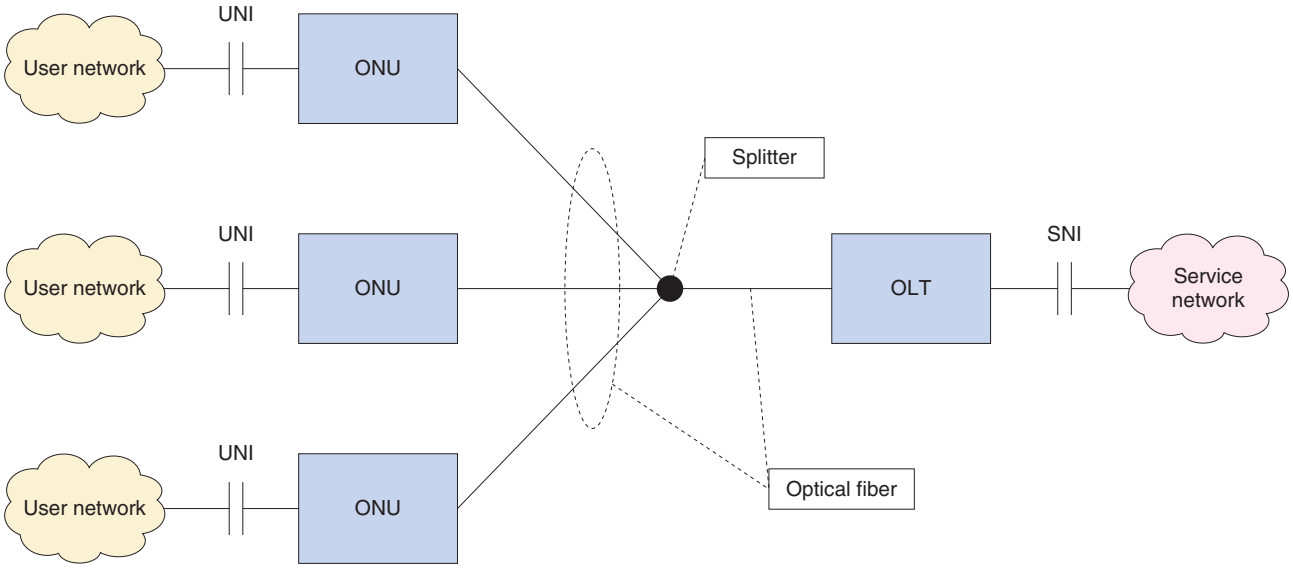

Fig. 1. Outline of EPON system.

Table 1. Functions of OLT and ONU and functional blocks in MAC LSI.

Function		Description	Functional block implementing the function	
			OLT	ONU
PON interface*	Optical transceiver	Converts optical signal to electric signal and vice versa.	(external component)	(external component)
	SERDES	Converts serial signal to parallel signal and vice versa.	SERDES	SERDES
	PCS	Channel coding and error correction	FEC	FEC
	PON control	Transmits and receives MPCP frames, maintains logical link, and adjusts local time for synchronization.	PON, CPU (software)	PON
DBA		Allocates bandwidth for upstream transmission.	DBA	(not applicable)
Encryption/decryption		Performs encryption and decryption.	ENC	ENC
Buffer		Temporarily buffers frames and counts accumulated frames (only in ONU).	BUF, external RAM	BUF
Bridge		Bridges between service network and PON (in OLT). Bridges between user network and PON (in ONU).	BRG	BRG
VLAN		Frame processing based on VLAN tags		
Priority control		Priority queuing of the frames		
SNI		Interface between service network and OLT	SNI	(not applicable)
UNI		Interface between user network and ONU	(not applicable)	UNI
Maintenance*		Transmits and receives OAM frames.	CPU (software)	CPU (software)
Authentication		Authenticates ONUs.	CPU (software)	CPU (software)

* IEEE802.3/IEEE802.3av compliant

BRG: bridge
ENC: encryption
FEC: forward error correction
OAM: operations, administration, and maintenance
PCS: physical coding sublayer
RAM: random access memory
VLAN: virtual local area network

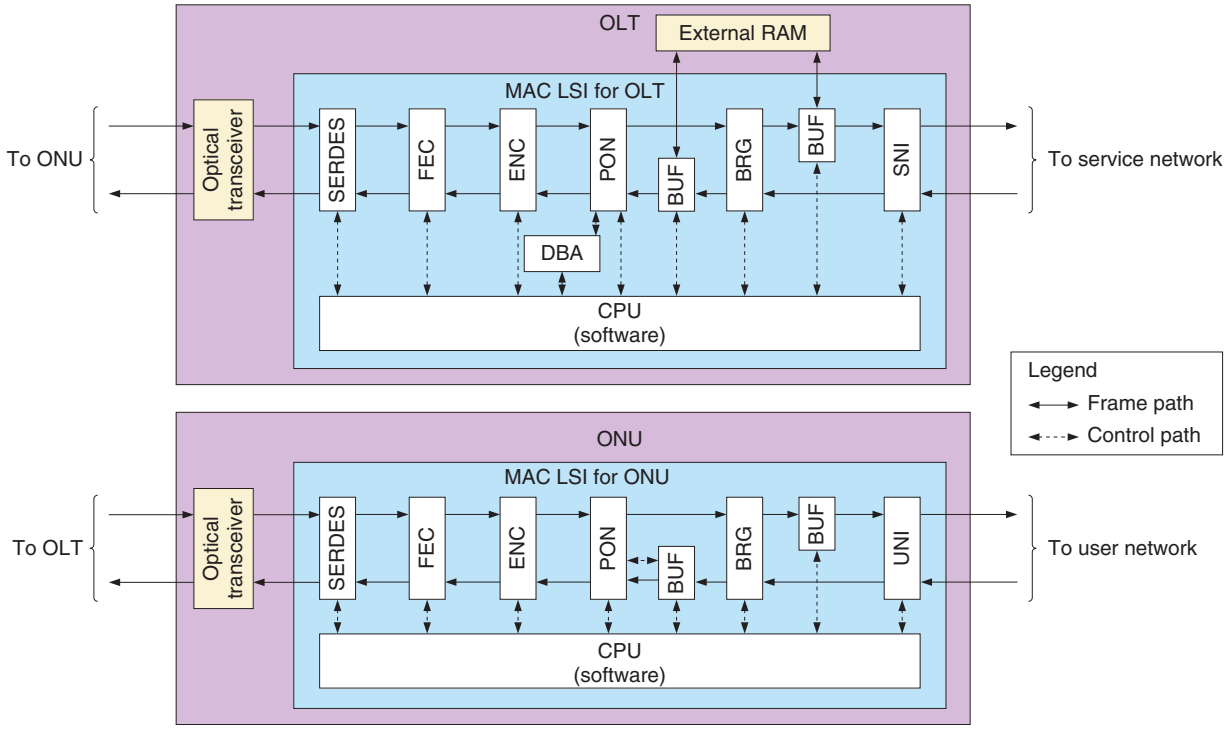

Fig. 2. Examples of MAC LSI block diagrams (top: OLT, bottom: ONU).

later.

(3) Uplink bandwidth allocation is required only in the OLT, so only the OLT has the DBA block. Conversely, the ONU must notify the OLT of accumulated frames, so the accumulated frame calculation function is present only in the buffer (BUF) section of the ONU.

(4) In the PON section for EPON, the downlink is a continuous signal, but the uplink is a burst-mode signal, so the ONU transmitter and the OLT receiver must support burst-mode communication. Burst-mode communication is described in detail in the fifth Feature Article "10-Gbit/s Burst-mode Receiver Integrated Circuits for Broadband Optical Access Networks" [5].

5. PON control function

The PON control function is an important function that administers the OLT-ONU links. When a new ONU connects to the PON, the PON control functions of the OLT and ONU establish a link by exchanging multipoint control protocol (MPCP) control frames in the sequence shown in **Fig. 3**. The process by which a newly connected ONU establishes a link is called *discovery*. Once discovery has been completed, MPCP control frames are exchanged periodically for link maintenance.

EPON uses time-division multiple access on the uplink, so the OLT and ONU must be synchronized, and this is also done by the PON control function. With EPON, the OLT internal clock acts as master, and ONUs are notified of the time by the transmit timestamp set in MPCP control frames. ONUs receiving this notification adjust their clocks to match. This can produce some jitter in the ONU clocks, so the ONU's PON control function must be designed not to malfunction owing to clock jitter.

6. Example of MAC LSI prototype

We have built a prototype LSI for a GE-PON ONU as described here. Details of the prototype are given in **Table 2**, and a photograph of the LSI mounted on an evaluation board is shown in **Fig. 4**.

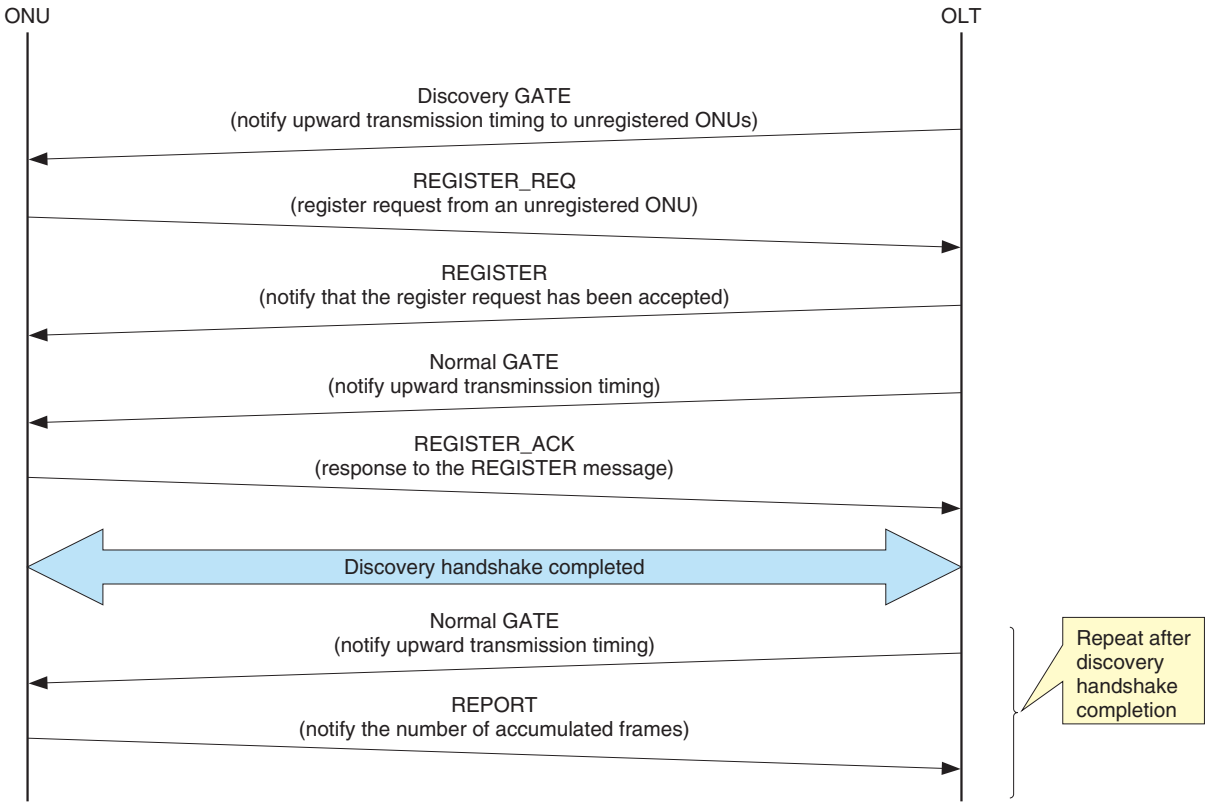

Fig. 3. Discovery handshake message exchange.

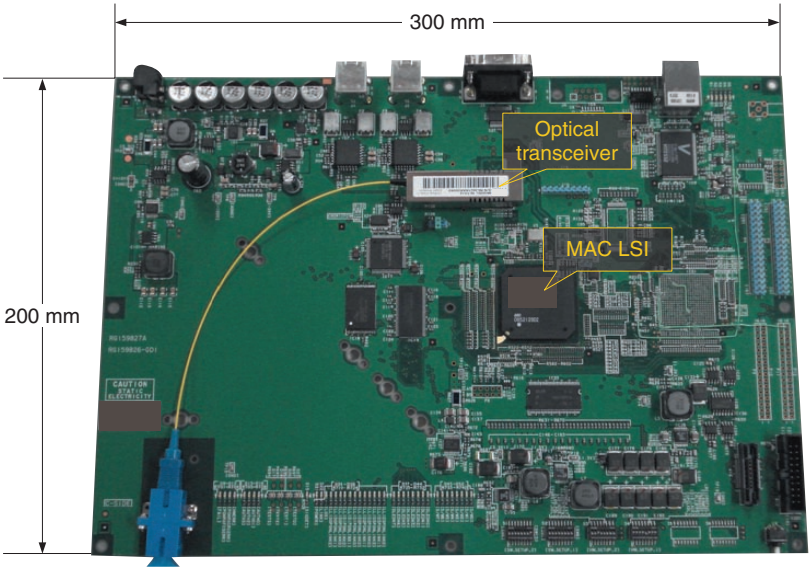

Fig. 4. Evaluation board with MAC LSI.

Table 2. Details of the prototype.

Logic	4.5 M gates	Total: 90 M transistors
Memory	12.4 Mbit/s	
Die size	9.25 mm × 9.25 mm	
Power consumption	2.2 W	

M: million

7. Conclusions and future developments

We described the development process and architecture for a MAC LSI for optical access communications and introduced a prototype of the LSI. 1-Gbit/s services using the GE-PON optical access system have been commercialized. However, the 10-Gbit/s rate for 10G-EPON has already been standardized, and even faster systems are expected in the future. LSI operation speeds are expected to increase slowly in comparison with these data transmission rates, so new architectures may be needed to handle the rising network speeds. Equipment cost reduction and power consumption control will also continue to increase in importance, so technical development be needed for their achievement. Finally, as functionality becomes more complex, the scale of LSIs needed for networking will continue to increase, so design technology and tools to handle larger-scale LSIs will also need to be developed.

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Design Verification Using Field-programmable Gate Arrays for Optical Access Communications SoC

Ritsku Kusaba†, Sadayuki Yasuda, Kenji Kawai, Tomoaki Kawamura, and Shoko Oteru

Abstract

We describe evaluation technology that uses field-programmable gate arrays (FPGAs) to test a system on a chip (SoC). This should reduce the time taken for testing SoCs used in optical access communications by letting us conduct tests using FPGAs in parallel with conventional testing to reduce the testing time and improve the design quality.

1. Introduction

The process of evaluating a system on a chip (SoC) involves verifying a register transfer level (RTL) description. The RTL description is written in a hardware description language and created through specification design, functional design, and RTL design, as shown in the SoC design flow in **Fig. 1**. The result is a verified RTL description, called a *clean file*, which is used next in the large-scale integrated circuit (LSI) production process.

SoC evaluation usually takes several times longer than SoC design, so as the scale of designs increases, the evaluation time is becoming a problem. Moreover, if a problem is discovered during the evaluation, the evaluation process can take even longer because additional checking is needed after the problem has been fixed to ensure that revisions have not affected other aspects of the design. Furthermore, the repair time and cost for fixing problems found after production has begun can be very high, so as much testing as possible must be done to eliminate these problems beforehand.

To date, SoC testing has generally been done using a logic simulator, which is a computer program ((a) in Fig. 1). However, simulating the functions of a large-scale device such as an SoC takes a long time, which makes it difficult to test all of the functionality adequately.

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2. Benefits of FPGA testing

To overcome this problem with logic simulation, it has recently become more common to conduct testing using field-programmable gate arrays (FPGAs) ((b) in Fig. 1) in parallel with logic simulation. An FPGA is an LSI [1] that can be programmed any number of times for the desired logic. In FPGA testing, hardware with the same functionality as the SoC is implemented by writing FPGA design data to an FPGA mounted on an evaluation board. This data is created from the hardware description of the SoC design. The functionality is then checked using measuring instruments to input data and evaluate whether the intended output data is obtained. FPGAs can operate several hundred times faster than a logic simulator, so they make possible long-term, continuous testing that is difficult with simulation.

Functionality can also be evaluated under conditions closer to real ones by connecting the evaluation board to other equipment and communicating at real speeds. FPGA evaluation allows functionality to be tested under more conditions than logic simulation

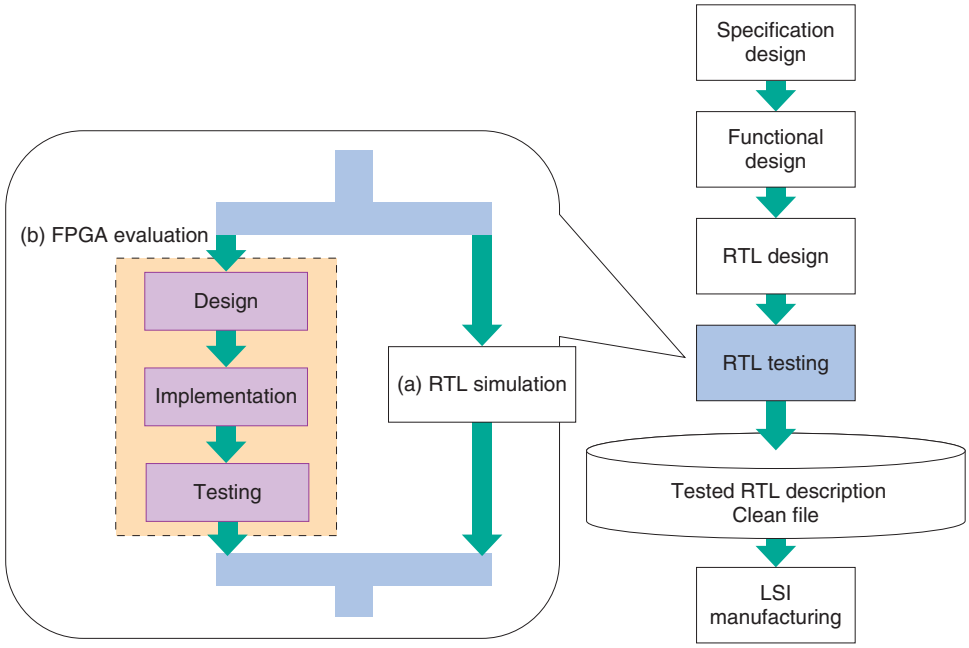

Fig. 1. SoC design flow.

and thereby allows for more improvements in design quality.

Another major benefit is that in combination with software, overall system operation can be tested. In this article, we focus on RTL evaluation using FPGAs.

3. Features of FPGA testing for optical access communications SoCs

This type of FPGA testing has many benefits, but when used to test SoCs for optical access communications, it must support large-scale systems and high-speed communications and make the test shorter and easier to perform. Below, we describe how these issues are handled.

3.1 Large-scale systems

An optical-access communications SoC requires a variety of functions, from communications using the prescribed protocol, to encryption for maintaining security and quality-of-service control to maintain service quality, so the design data may be large-scale.

For testing, the design data must be written to FPGAs, but a large-scale design may not fit onto a single FPGA device. In such cases, the design data can be divided and written to multiple FPGAs, but this presents the additional issues of how to divide the design data appropriately and how to transmit high-speed signals among the devices.

Communications SoCs are usually organized to perform the prescribed processing in order according to the signal flow for upstream and downstream signals. Thus, the design can be divided according to the major functions to enable this sort of processing, and each function can be implemented in a separate FPGA (**Fig. 2**).

3.2 High-speed communications

The next-generation of optical access communications SoCs will send and receive data at a high wire-speed of 10 Gbit/s. FPGA testing allows the design to be evaluated at these speeds, so this technology has the advantage of evaluating the design under nearly real conditions.

When data is transmitted among multiple FPGAs, it can be difficult to transmit or receive data between devices in some cases owing to delay in the lines among FPGAs or to phase differences among the FPGA clocks. For this reason, in 10-Gbit/s processing, a 64-bit-wide data frame and control signals are sent together with the clock from the sending FPGA to the receiving FPGA (**Fig. 3**). The data is written to

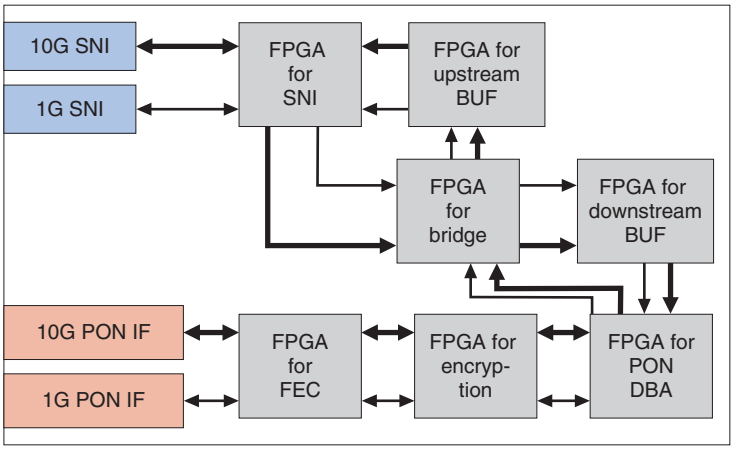

Fig. 2. Example of FPGA implementation.

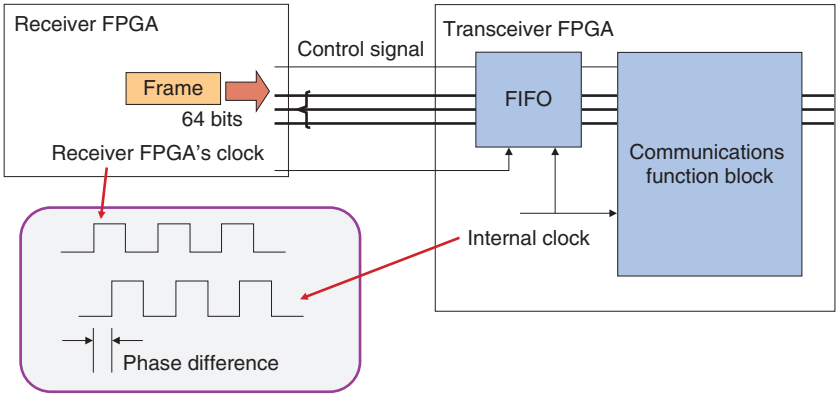

Fig. 3. Clock phase differences.

a first-in first-out (FIFO) buffer in sync with the sending FPGA's clock. It is then read out of the buffer in sync with the receiving FPGA's clock to compensate for any phase differences and to maintain high-speed communications [2].

The wiring, connectors, and other aspects of the FPGA evaluation board are also selected to handle high-speed communications.

3.3 Reduced testing time

For large-scale SoCs, all the functional blocks are designed and tested in parallel. With conventional FPGA testing, frame continuity is not achieved, and it is impossible to test all functional blocks or the LSI as a whole until the design data for all functional blocks has been implemented in FPGAs. Because of this, if the design and testing of a particular block is delayed and the block has not yet been implemented in the FPGA, testing cannot begin, which creates a bottleneck for the entire test schedule.

To deal with this issue, various approaches are used to replace the FPGA that is behind schedule until it is ready in order to prevent major delays in the overall test schedule. These include using an FPGA that implements only the minimum functionality (a substitute circuit), one that simply takes a frame from the previous block and outputs it in a format acceptable to the following block (through circuit), and one that

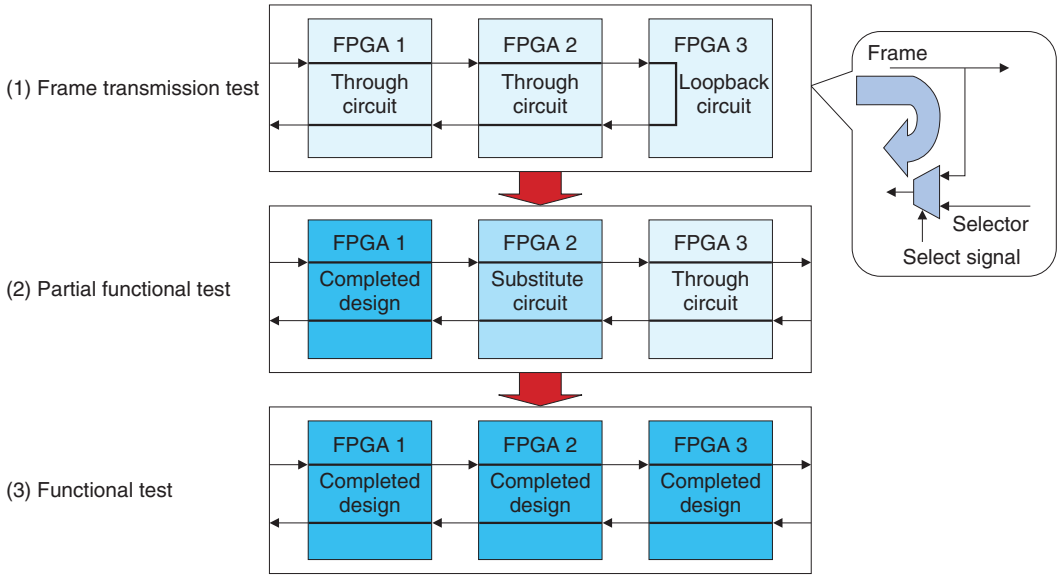

Fig. 4. Gradual FPGA testing method.

takes the output from the previous block and sends it back as input to the previous block (loop-back circuit).

Examples of applying these types of circuit at various stages of testing (gradual FPGA testing method) are shown in **Fig. 4**. In the early stages of testing, none of the block designs are complete, so a through circuit is implemented for each one and a loop-back circuit is used to perform a frame continuity test (1). When the designs of some of the blocks are complete, either through or substitute circuits can be used for blocks that are still incomplete so that FPGA testing of the completed circuits can proceed (2). In this way, evaluation can proceed, starting with the blocks completed first, and at the end, when the designs and FPGA implementations for all blocks are complete, the overall LSI functionality is tested (3). Before the designs for all of the blocks are complete, testing of individual functional blocks can proceed (1)–(2), and when the design data for all of the blocks is ready, testing of the overall LSI is done. This allows testing to be completed earlier than with previous approaches.

3.4 Easier testing

An SoC for communications processes frames from the communications path, performing forward error correction (FEC) to correct errors, encryption to provide high security, etc. Testing instruments similar to local area network (LAN) analyzers are used in FPGA testing for communications SoCs, but they generally cannot create or receive these types of frames, so it is impossible to check functionality without performing testing by actually connecting together devices of the same type. To resolve this issue, we built the test system shown in **Fig. 5**.

This system consists of a LAN analyzer that embeds test data generated on a personal computer (PC) in frames and sends them to the FPGA port, and an optical line terminal (OLT) FPGA board (see "MAC LSI Design Technology for Optical Access Communications" [3]) with the circuit being tested as well as circuits that encapsulate and decapsulate the test data from the frames and send them to the test circuit.

Test frames are encrypted and FEC-encoded using a program running on the PC, stored in the data segments of Ethernet frames by the LAN analyzer, and input to the OLT FPGA board. On the FPGA board, the decapsulation circuit retrieves the encrypted and FEC-encoded frames from the Ethernet frames and removes the FEC encoding and encryption. Correct operation can be checked by comparing the test frame with the output frame. This method makes tests simulating communication conditions easy to do using an ordinary LAN analyzer.

4. FPGA evaluation boards

An example of an FPGA evaluation board developed

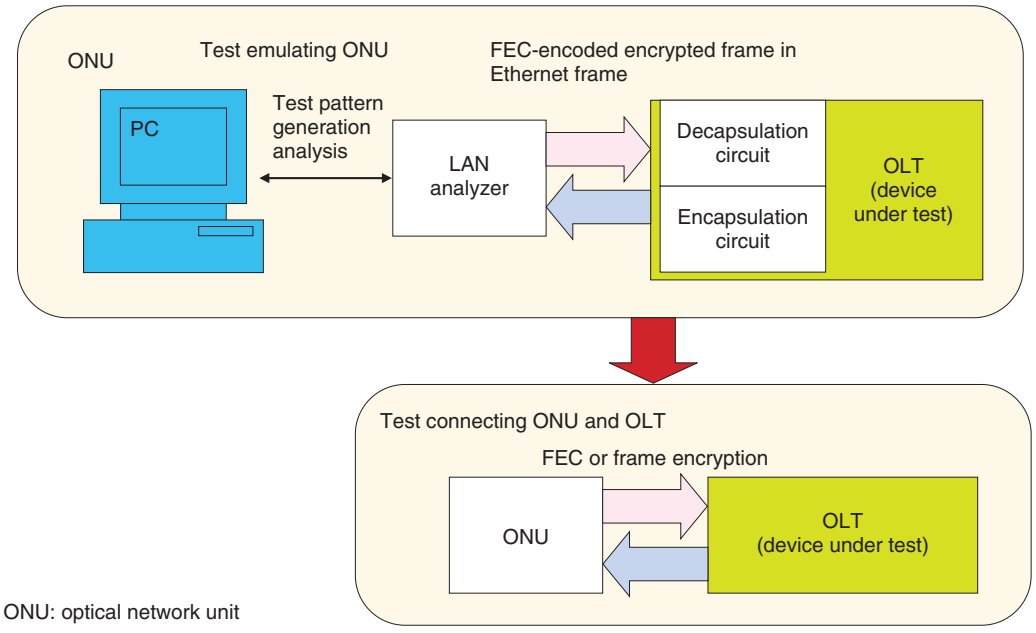

Fig. 5. Test environment for connection test between ONU and OLT.

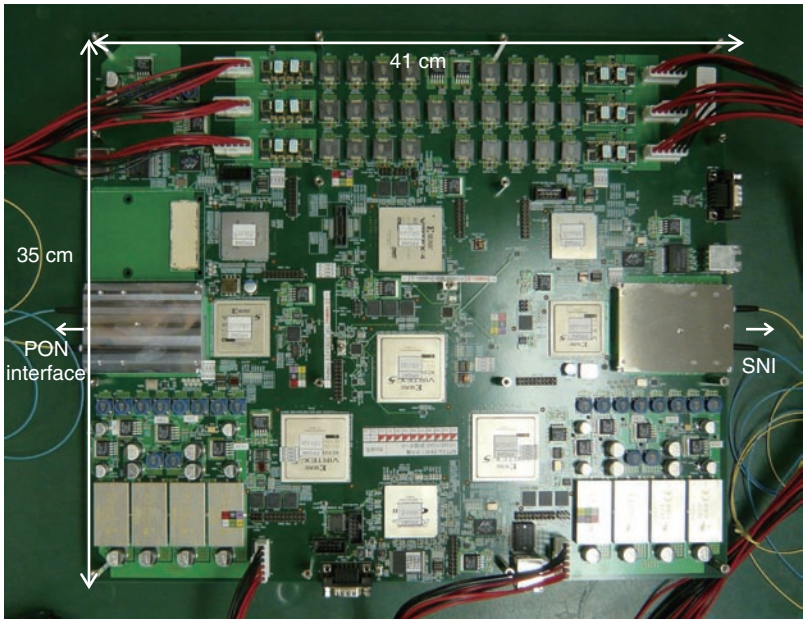

Fig. 6. PGA board for optical access network SOC.

for an optical access communications SoC is shown in **Fig. 6**. This evaluation board implements OLT circuits in multiple FPGAs for FPGA testing.

5. Future developments

After an LSI has been produced, an LSI evaluation board is constructed and the LSI's system operation

is tested. FPGA testing know-how can also be useful for this. We plan to study new functionality by using the fact that functions on the FPGA board itself can also be modified.

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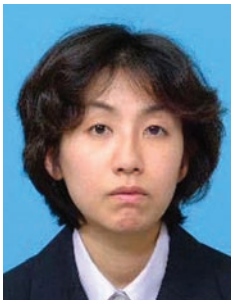

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10-Gbit/s Burst-mode Receiver Integrated Circuits for Broadband Optical Access Networks

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Abstract

We introduce burst-mode receiver integrated circuits that can respond instantaneously to a suddenly arriving optical signal and receive it correctly. They are suitable for the next-generation optical access system (10G-EPON: 10-Gbit/s Ethernet passive optical network), which requires a receiver that can receive high-speed (10-Gbit/s) optical burst signals, unlike typical receivers which receive continuous signals.

1. Introduction

NTT's FLET'S Hikari service, which is a passive optical network (PON) system, is currently spreading in Japan. In this service, the signal sent from a customer's terminal (optical network unit (ONU)) to the optical line terminal (OLT) in the central office is a burst signal. Unlike the continuous signals widely used with Ethernet and other technologies, burst signals have no signal at all between data segments. Moreover, the distances from customers to the central office vary, which affects the signal strength accordingly. This is shown in **Fig. 1**, where the signal from ONU 1 is strong, while that from ONU 2 is weak. For the central office to be able to handle such customer data, these optical burst signals with differing strengths and timings must be converted into electrical signals of fixed intensity and timing. For the next generation of optical access communications, this functionality must be achieved for data being transmitted at ten times the current speeds.

2. Receiver architecture

As shown in **Fig. 2**, the burst-mode receiver [1], [2] for an OLT consists of an avalanche photodiode, which converts the optical signal into an electrical current signal; a transimpedance amplifier (TIA), which amplifies and converts the current signal into a voltage signal; a limiting amplifier (LA), which converts weak and strong voltages into fixed-amplitude voltage signals; and a clock and data recovery (CDR), which extracts the timing clock from this signal and

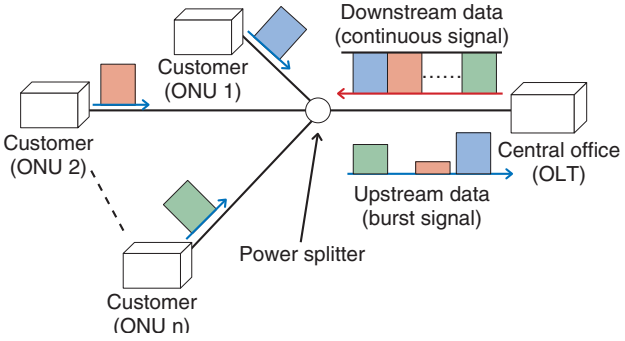

Fig. 1. PON system.

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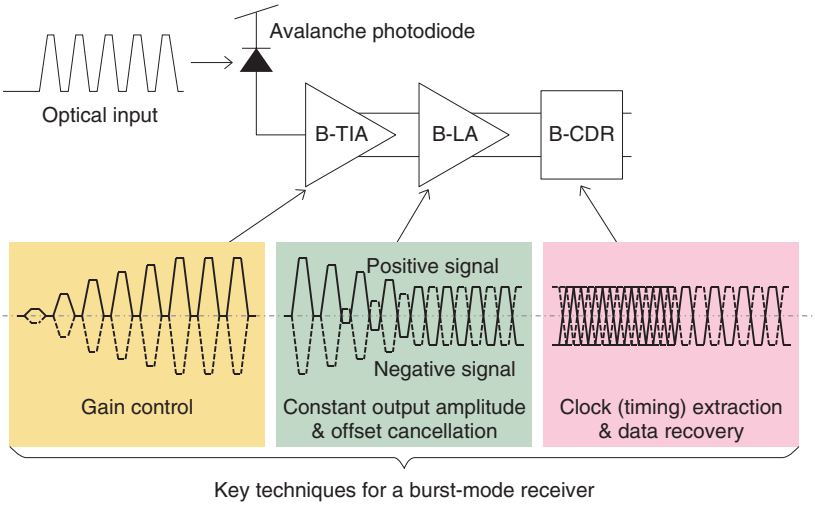

Fig. 2. Burst-mode receiver.

Table 1. Specifications of burst-mode receivers in PON systems.

	GE-PON IEEE 802.3ah	10G-EPON IEEE 802.3av	
	1000BASE-PX20-D	10GBASE-PR-D3	10/1GBASE-PRX-D3
Data rate	1.25 Gb/s	10.3125 Gb/s	1.25 Gb/s
Response time for TIA + LA	< 400 ns	< 800 ns	< 400 ns
Response time for CDR	< 400 ns	< 400 ns	< 400 ns
Sensitivity	–27 dBm	–28 dBm	–29.78 dBm
Overload	–6 dBm	–6 dBm	–9.38 dBm
Bit error ratio	$< 10^{-12}$	$< 10^{-3}$ (with FEC)	$< 10^{-12}$
Maximum length of consecutive identical digits*	5 bits	66 bits	5 bits

FEC: forward error correction

*Counted using the encoding method used in the standard.

reshapes the signal waveform using the extracted clock signal. For a burst-mode receiver, the TIA, LA, and CDR need to be burst-mode devices, which are denoted B-TIA, B-LA, and B-CDR, respectively.

Below, we discuss the international standard specifications and characteristics of burst-mode receivers.

3. International standard specifications

The specifications for 10-Gbit/s PON-system (10G-EPON (10-Gbit/s Ethernet PON), IEEE 802.3av) [3] burst-mode receivers, as defined by IEEE, are shown in **Table 1**. For comparison, the table also shows the specifications for the 1-Gbit/s PON system (GE-PON (Gigabit Ethernet PON), IEEE 802.3ah) [4] currently in common use. For the 10G-EPON system, both 10- and 1-Gbit/s burst signal rates are stipulated. For signals at each rate, burst-mode receivers must satisfy the values in the table for optical input sensitivity and overload (tolerance to strong signals) just like continuous-mode receivers. Characteristics particular to burst-mode receivers are the response times. For 10-Gbit/s receivers, the response times of the TIA and LA are twice those in

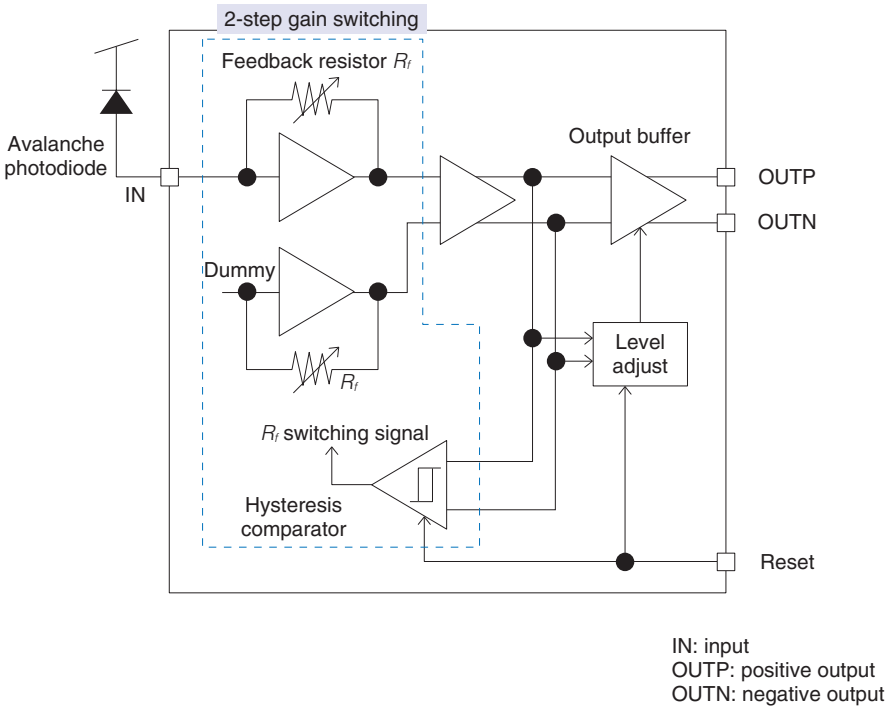

Fig. 3. Block diagram of B-TIA.

1-Gbit/s receivers, and the time allowed for the CDR to extract signal timing has not changed. However, the maximum number of consecutive identical digits (CIDs) (zero or one) has been increased to 66 bits. This means that when a signal begins suddenly after a period of no signal, the TIA and LA must adjust the amplification, and the CDR must match the signal timing within a short time (although it is 1.5 times the previous time). On the other hand, each integrated circuit (IC) must not change state within a CID period (the same as when there is no signal) that is over 13 times longer than that specified for 1 Gbit/s. These requirements appear to conflict: they require a fast response while also requiring that the state does not change.

4. Burst-mode receiver circuits

Below, we introduce receiver circuits that satisfy the particular requirements of burst signals.

4.1 Burst-mode transimpedance amplifier (B-TIA)

A block diagram of a B-TIA [5] is shown in **Fig. 3**. In order to respond to a sudden input signal and instantly set the gain optimally, the circuit switches between two feedback resistor values R_f. When the input signal is weak, a high feedback resistance is used for high gain, and when the input signal strength exceeds a set value, the TIA switches to a low feedback resistance for lower gain. Existing circuits either do not switch feedback resistance or vary it continuously. In the former case, when the sensitivity is set to handle weak signals, strong signals produce signal distortion, while when it is set to handle strong signals, the sensitivity is not enough for weak signals. In the latter case, when the response time controlling the feedback resistance is fast, sensitivity changes during a CID period. If the response is made slower to prevent this, the burst response is somewhat slower, which is a drawback. Switching between two values allows for a fast response, and a comparator that has hysteresis is used to preserve the post-switching state, which enables good CID reception.

4.2 Burst-mode limiting amplifier (B-LA)

A block diagram of a B-LA [6] is shown in **Fig. 4**. The basic function of the LA is to receive an input voltage signal with a varying amplitude (ranging from small to large) and to output a fixed-amplitude signal. For burst signals, another function is also important: the B-LA adjusts the voltage levels of

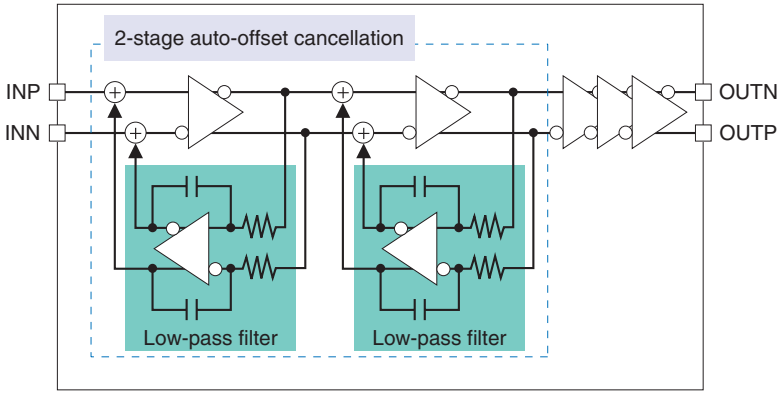

Fig. 4. Block diagram of B-LA.

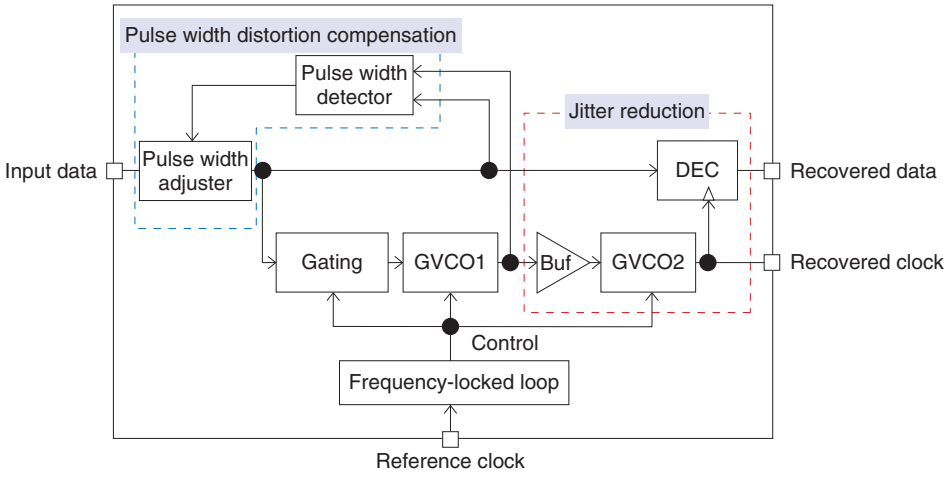

Fig. 5. Block diagram of B-CDR.

positive and negative signals quickly (see Fig. 2), which is called offset cancellation. When a burst signal arrives after a period of no signal, the positive input (INP) of the LA goes to *high* with respect to a fixed center level and the negative input (INN) goes to *low*. The LA output signal first appears when the positive and negative signals cross, so to reduce the amount of time until a signal is output, a means of ensuring fast offset cancellation is needed. In the first offset cancellation stage in Fig. 4, the average level of the negative output of the first stage is fed back to the positive input and vice versa. This causes both signals to approach the same potential. We get a second-order filter effect by connecting two such circuits in series. With a second-order filter, the first state change is slow and the subsequent change is fast. Therefore, while reducing the level variation due to CID, the second-order filter can cancel the offset quickly for both positive and negative signals at the beginning of a burst and can reduce the time until the burst signal is output.

4.3 Burst-mode clock and data recovery (B-CDR)

A block diagram of a B-CDR circuit [7] is shown in **Fig. 5**. This CDR is based on a gated voltage-controlled oscillator (GVCO) that has the fastest synchronization time to the input signal. When the input signal rises from low to high, a pulse is output from the gating circuit. When this pulse is input to a NAND gate, which is one of the ring gates in GVCO1, the clock timing of GVCO1 adjusts to the data in that single pulse. Since the matching of the timing is so

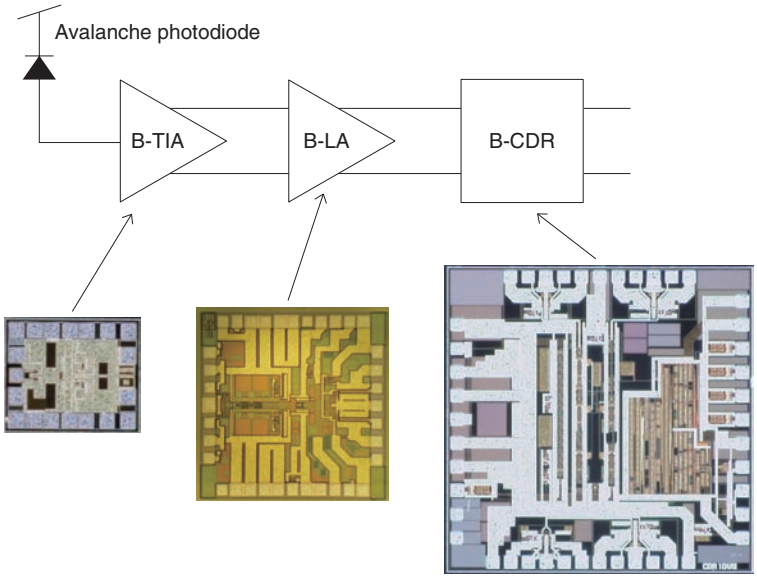

Fig. 6. Micrographs of the receiver ICs.

fast, any jitter in the input signal appears as-is in the output clock of GVCO1, so synchronization loss problems may occur in later-stage circuits. Moreover, when the *high* width of an input signal is much shorter than the *low* width, the decision circuit (DEC) produces a false detection. For this design, a second oscillator (GVCO2) is placed in series with the first. By inputting the output clock from GVCO1 attenuated in the buffer (Buf), we were able to obtain a stable output clock that was less affected by the jitter in the input signal. Moreover, by adding a feedback loop that monitors the input signal pulse width and compensates for its distortion, we were able to make the pulse widths for high and low symbols close to one another.

5. Burst-mode receiver characteristics

Micrographs of IC prototypes of the B-TIA, B-LA, and B-CDR for the burst-mode receiver are shown in **Fig. 6**. We selected a silicon process to fabricate these ICs, putting priority on high-volume production and low cost considering that they are for access network services. Taking into consideration their high-frequency characteristics, we housed each IC in a package for high-speed IC applications, mounted each package on an evaluation board, and evaluated their characteristics as a burst-mode receiver.

The evaluation results are shown in **Fig. 7**. We varied the power of the input optical burst signal and measured the bit error ratio (BER) in the output signal payload. To ensure that measurements reflected the receiver's longest (worst-case) possible response time, we input a signal of the maximum strength indicated in the specifications directly before inputting a signal of the strength being measured. Points labeled 2R are the BERs for the TIA + LA output, while 3R is the BER that also includes the CDR. For both 10 Gbit/s and 1 Gbit/s, the receive sensitivity and overload values met those in the standards specifications shown in Table 1. The receiver can set the gain and adjust the timing within a preamble time of 200 ns. This indicates that the receiver achieves a very fast burst-response time of less than one sixth of the 1200 ns specified in the 10G-EPON standard.

6. Future developments

In the future, we plan to use this technology in our research and development of higher-layer LSIs to promote the use of 10G-EPON in Japan and around the world and to develop circuit techniques with even better energy-saving characteristics, as this becomes more and more important.

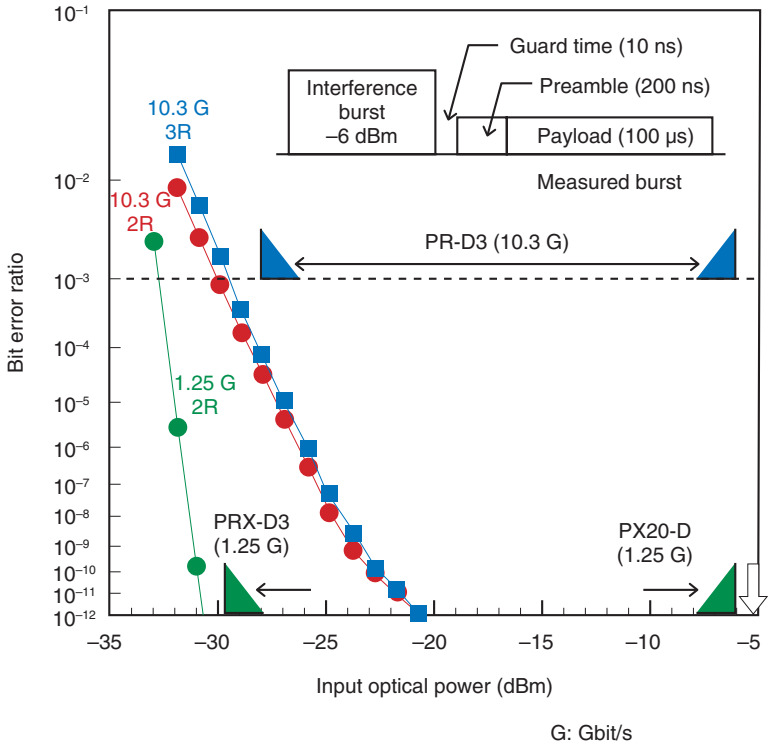

Fig. 7. Measured bit error ratio of the burst-mode receiver.

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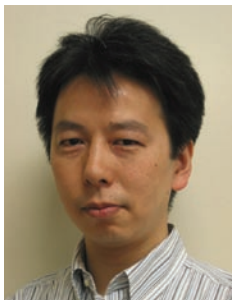

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Optical Device Technologies for Future Network Evolution

Koichi Murata† *and Takashi Saida*

Abstract

This article outlines progress in optical device technologies for photonic networks, focusing on integrated optical device technologies for digital coherent optical transmission technologies. With the rapid spread of fiber to the home (FTTH), broadband video services and mobile Internet devices now require a highly functional optical network infrastructure with a large capacity.

1. Introduction

Communication traffic has grown owing to the rapid growth of the Internet and broadband services. The technological progress in high-speed and large-capacity optical transmission and the optical devices for optical transmission systems have supported the evolution of information and communications technology. Trends in the transmission capacity of the core network are shown in **Fig. 1**. From 1980 to the beginning of the 1990s, electrical time domain multiplexing (ETDM) based on on-off keying was the major technology in optical transmission systems. In ETDM systems, high-speed optical and electrical devices as well as optical fiber amplifiers were the keys to achieving high-speed long-haul transmission systems. The total transmission capacity reached 10 Gbit/s. In the 1990s, wavelength division multiplexing (WDM) led to rapid progress in transmission capacity owing to the appearance of optical filters providing optical multiplexing and/or demultiplexing functions. Arrayed-waveguide grating (AWG) technology based on silica-based planar lightwave circuits (PLCs) [1] played an important role in achieving those functions with excellent stability, robustness, and reliability. Since silica-based glass waveguides are formed on the Si substrate in PLC technology, this technology can provide various functions with a very small die area, such as optical multiplexing/demultiplexing, optical switching, and optical attenuation [2]. Here, the optical switching and attenuation is achieved by Mach-Zehnder interferometers with thermo-optic heaters. These PLC technologies are applied to key optical components for not only core networks but also metro-area networks. For example, reconfigurable optical add/drop multiplexers (ROADMs), which feature low latency, flexibility, and upgradability, have been developed using PLC technology. In an ROADM switching module, highly integrated PLC technology containing the AWG and optical switches and hybrid integration technology have been used to achieve a compact and highly functional OADM [3].

The latest 40-Gbit/s × 40 wavelengths WDM system has been deployed in the core network, and total transmission capacity has reached 1.6 Tbit/s. To keep up with the demand for rapid growth of communication traffic, new technologies supporting 10-Tbit/s optical transmission systems based on 100 Gbit/s per channel (ch) are expected. One attractive candidate technology for 100-Gbit/s-based WDM systems is digital coherent transmission, which combines coherent detection and digital signal processing [4]. In the next section, we review the transmitter/receiver configurations for various optical modulation formats and describe the integrated optical device techniques for digital coherent technology.

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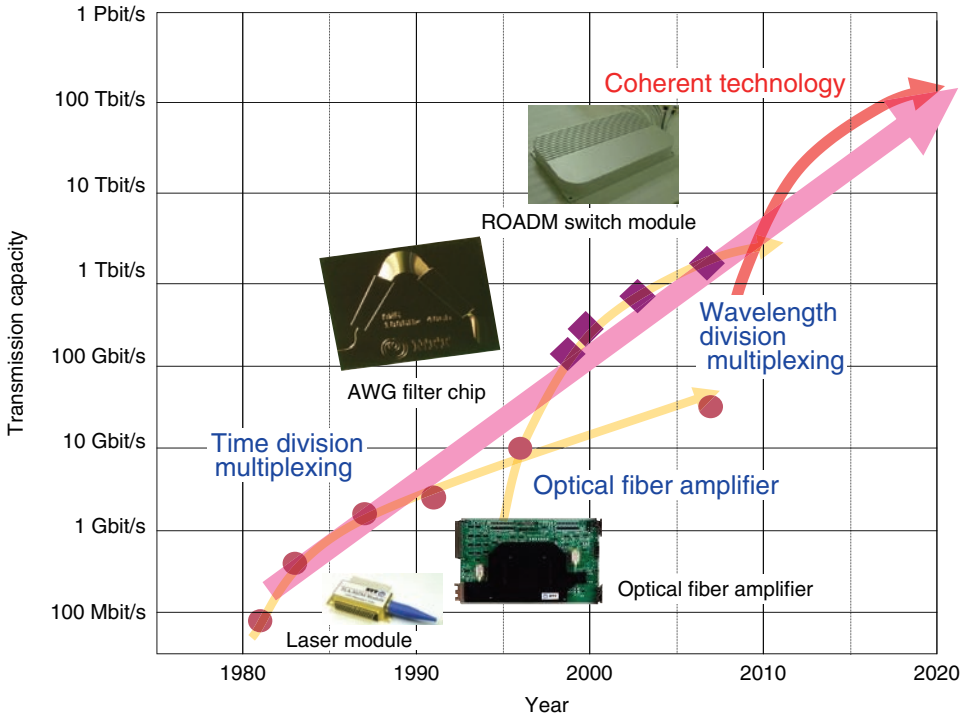


Fig. 1. Trends in optical transmission system capacity.

2. Optical modulation formats and optical transmitter/receiver configurations

The configurations of optical modulators and receivers for various optical modulation formats as well as the relationship between symbol and data transmission rates are summarized in **Fig. 2**. The on and off optical signals were generated in the optical modulator according to the signal information of "1" and "0" in on-off keying (OOK) direct detection modulation. OOK was widely applied to systems with data transmission rates up to 10 Gbit/s because it lets us make a simple optical modulator and receiver configuration. To achieve even greater capacity and long-distance transmission, the important technical issue is how to increase the spectral efficiency while maintaining the tolerance of the optical signal-to-noise ratio. In order to achieve this, optical phase shift keying schemes such as differential phase shift keying (DPSK) and differential quadrature phase shift keying (DQPSK) have been investigated. For example, DQPSK has been applied to the abovementioned 40-Gbit/s/ch WDM systems. In the case of DQPSK, 2-bit signals are modulated and assigned to four optical phases, which results in a two-fold improvement in spectral efficiency compared with OOK. DQPSK is thus able to relax the limitations on both optical bandwidth and transmission distance due to chromatic dispersion. Polarization division multiplexed quadrature phase shift keying (PDM-QPSK) with coherent detection is being investigated for the next-generation 100-Gbit/s/ch systems. PDM-QPSK multiplexes two QPSK signals in the polarization domain. It has the great advantage of mitigating the problems of increasing both the electrical analog amplification bandwidth and the digital signal processing speed because it can reduce the symbol rate to 1/4 of the data transmission rate. As shown in Fig. 2, the configurations of modulators and receivers become complicated when phase shift keying and polarization multiplexing are used. This indicates that highly functional and integrated optical device technology, which provides a small size and low cost, will be important to support future large-capacity optical transmission systems.

3. Digital coherent technology and optical front-end configurations

Digital coherent technology combines coherent

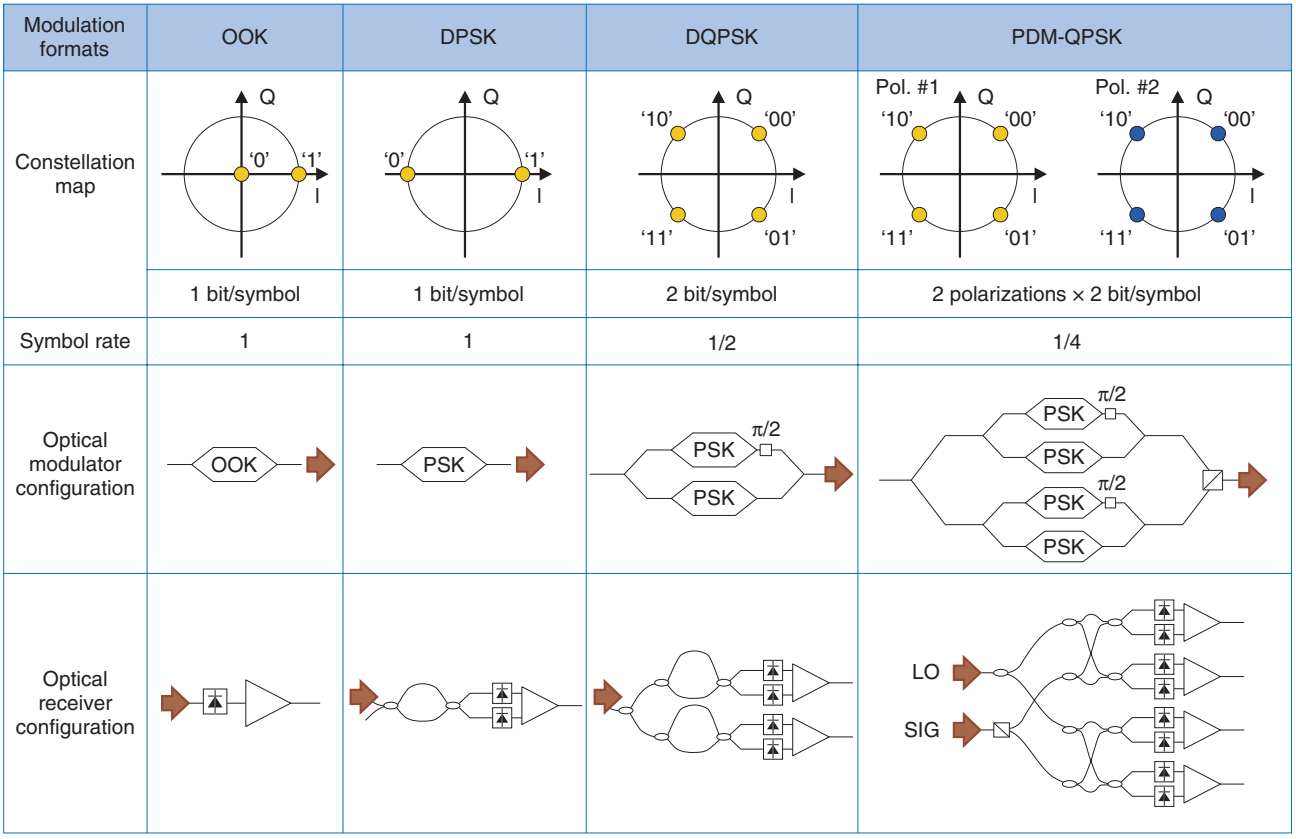
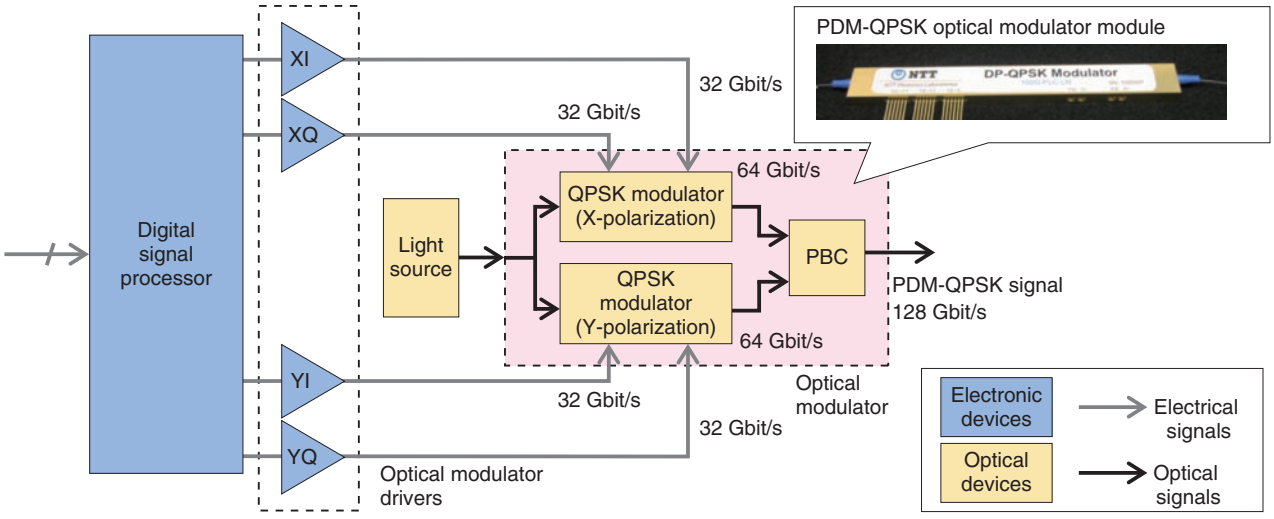


Fig. 2. Optical modulation formats and their optical modulator and receiver configurations.

detection and digital signal processing at the receiver side and enables us to use various modulation formats. The transmitter and receiver for a digital coherent system using PDM-QPSK modulation format are shown in **Figs. 3** and **4**, respectively. Here, the signal data transmission rate is 128 Gbit/s when a forward error correction code that allows a 20% increase in the data rate is used. The transmitter consists of a digital signal processor, a light source, an optical modulator, and modulator drivers, as shown in Fig. 3. Here, the optical modulator comprises two QPSK modulators and a polarization beam combiner (PBC). On the other hand, the receiver consists of a local oscillator (LO) light source, optical receiver front-end, analog/digital convertors (ADCs), and a digital signal processor, as shown in Fig. 4. First, the optical phase information is recovered by mixing the input optical signal with the LO light, and then the signals are converted into electrical signals and linearly amplified in the front-end. After that, the electrical signals are sampled by the ADCs, and the original data signals are then recovered in the digital signal processor by using a phase and amplitude estimation algorithm. Here, the use of the digital signal processing has three important features, which is quite different from the previous technologies: 1) stable phase synchronization between the received optical signal and the local light as well as stable polarization demultiplexing, 2) both adaptive polarization dispersion compensation and chromatic dispersion compensation through the use of sophisticated digital filter technology, and 3) flexible selection of various modulation formats with minimum modification of the hardware.



XI, XQ, YI, YQ: in-phase and quadrature components on the X and Y axes, respectively.

Fig. 3. Digital coherent transmitter for PDM-QPSK. (DP (dual polarization), shown in the photograph, is equivalent to PDM)).

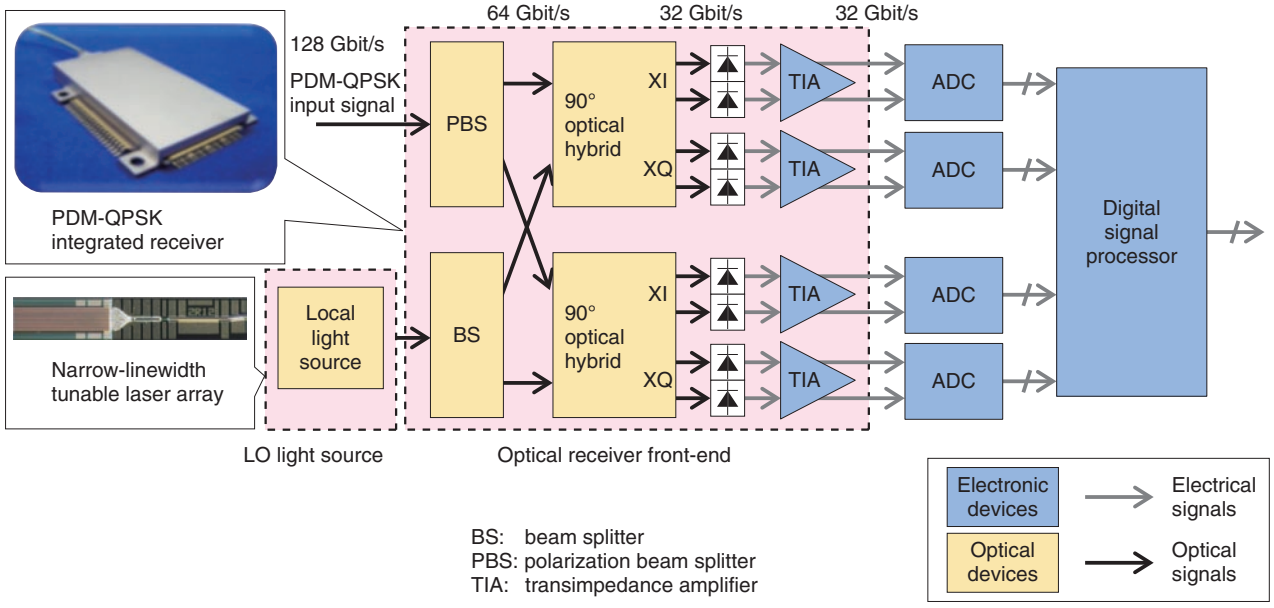


Fig. 4. Digital coherent receiver for the PDM-QPSK.

4. Optical modulator for 100-Gbit/s digital coherent technology

Mach-Zehnder interferometers have been widely used as optical amplitude modulators for conventional OOK systems. In this case, the optical phase difference of the interferometer is controlled by external data signals. When the phase difference is 0°, the output optical signal is on, while when the phase difference is 180°, the output optical signal amplitude is off. On the other hand, in QPSK modulation, the phase of the interferometer must be controlled in the range from 0° to 360°, which means that QPSK optical modulators require twice the driving voltage that

conventional amplitude modulators do. In addition, a polarization multiplexing function, which combines two QPSK signals in the X and Y polarizations, is indispensable for PDM-QPSK signal generation. Therefore, the PDM-QPSK optical modulator must satisfy two requirements: a low driving voltage and the integration of two QPSK modulators and a PBC. As the material for conventional optical modulators, $LiNbO_3$ has been widely used. It features low chirp and low insertion-loss characteristics. However, there are technical issues in the monolithic integration of a complicated low-loss waveguide and PBC in order to construct a complicated optical modulator for PDM-QPSK. NTT Photonics Laboratories has been investigating PLC-$LiNbO_3$ hybrid technology for those complicated multilevel optical formats [5], [6]. In this technology, various kinds of optical components like optical couplers, PBCs, and splitters are monolithically integrated on the PLC, while $LiNbO_3$ is just used for optical phase modulation. Since a PLC can provide various functions in a small size with high reliability, hybrid technology is advantageous in terms of flexibility for various modulation formats, like PSK and QAM (quadrature amplitude modulation), and scalability to advanced modulation formats [5], [6].

5. Optical receiver devices for 100-bit/s digital coherent technology

Key optical devices for the digital coherent receiver are the optical receiver front-end and LO light source, as shown in Fig. 4. The receiver front-end consists of optical polarization splitters, 90° optical hybrids, photodiodes, and transimpedance amplifiers (TIAs) [7]. To make small low-cost receivers, technology for integrating these optical and electrical devices is of great importance. The passive optical circuits, for demultiplexing polarization components and mixers for mixing an optical signal with an LO light, are required to have a high polarization extinction ratio at the polarization demultiplexers and a low phase error at the mixers. They have conventionally been implemented using optical fiber or free-space optics technologies. However, those technologies cannot easily provide stable operation with a small size. One promising approach is the application of PLC technology to the monolithic integration of these two functions because a PLC can monolithically integrate 90° hybrids, couplers, and a polarization beam splitter (PBS) on a single Si-substrate [8]. As for the conversion of optical signals to electrical ones in the front-end receiver, the following three performances are required: 1) broadband characteristics able to handle a data rate of 32 Gbit/s, 2) a wide dynamic range for the optical signal input intensity, and 3) linear amplification with low variation in output voltage swing, phase, and skew in each output channel. The TIA is required to provide not only the functions of auto-gain control and output voltage swing adjustment, but also high-gain, broad-bandwidth, low waveform distortion, and low dynamic skew at the same time. To cope with these requirements, several TIAs that use high-speed and high-breakdown voltage device technologies such as SiGe BiCMOS (bipolar complementary metal oxide semiconductor) and InP HBTs (heterojunction bipolar transistors) are being investigated.

As for the LO light source, both low phase noise, i.e., narrow spectral line width and high output power, are required because the optical frequency stability affects the phase extraction stability, especially in intradyne coherent detection, and high LO light power is useful for obtaining higher signal input sensitivity. NTT Photonics Laboratories has already demonstrated an L-band tunable laser diode array module that provides a narrow linewidth of less than 580 kHz and high fiber output power of 20 mW [9]. An integrable tunable laser assembly, which integrates light wavelength control with a tunable laser source in one module, will be important for achieving a small transmitter and receiver board. Standardization for the abovementioned optical components for 100-Gbit/s/channel digital coherent transmission, such as optical modulators, integrated optical front-ends, and LO light sources, is currently under way in the Optical Internetworking Forum (OIF) [10]. We will continue to improve our optical device and integration technologies to obtain much higher performance and to contribute to future network evolution by providing new optical device technologies.

6. Conclusions

A 100-Gbit/s/channel system based on digital coherent technology is considered to be a promising candidate for next-generation large-capacity long-distance optical communication systems. The optical components required for such systems, such as a PDM-QPSK optical modulator, integrated receiver, and local light source, are under development. Opto-electrical integration technologies, which enable us to construct small, low-cost, and highly functional optical components, will play an important role in

providing cost-effective transmission equipment for future 100-Gbit/s/ch and post-100-Gbit/s/ch optical communications.

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Wavelength-tunable Lasers for Next-generation Optical Networks

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Abstract

Wavelength-tunable lasers are key components as light sources in large-capacity optical core networks that use dense wavelength-division-multiplexing techniques. In next-generation optical networks, an advanced modulation/detection technique will be used, and low phase-noise characteristics will be essential for tunable laser sources. This article reviews techniques for reducing the phase noise of tunable lasers and describes a narrow-linewidth tunable distributed feedback laser array that we have developed.

1. Introduction

The rapid increase in Internet traffic has accelerated the growing demand for greater traffic capacity in recent years. Dense wavelength-division-multiplexing (DWDM) techniques have been developed to increase the transmission capacity by increasing the number of wavelength channels. In commercial photonic network systems, 80–100 wavelength channels are multiplexed on one optical fiber. Early DWDM systems used fixed-wavelength lasers as light sources, which meant that many kinds of optical transceivers were needed for the wavelength channels. The use of tunable lasers, which can operate at any channel wavelength, means that only one kind of transceiver is needed, so the inventory cost can be reduced. Various kinds of tunable laser have already been developed for this purpose [1]. Tunable lasers are now widely used as light sources in DWDM systems.

However, it is difficult to increase the number of wavelength channels and thus further expand the transmission capacity owing to the wavelength range limitation of the optical fiber amplifier. Therefore, a lot of research has concentrated on increasing the signal data rate per wavelength channel. In commercial systems, the fastest data rate per channel is 40 Gbit/s. In next-generation systems, it will be 100 Gbit/s, and an advanced modulation/detection technique, namely a digital coherent system, is expected to be used. In such systems, the tunable lasers are used both as a light source in the transmitter and as a local oscillator in the receiver. In digital coherent systems, the light sources must have low phase-noise characteristics because the phase of the lightwave is used as information.

This article reviews techniques for reducing the phase noise of tunable lasers. The required performance of the light source in digital coherent systems is described, and the development status of an applicable tunable laser is reported. Moreover, narrow-linewidth operation is demonstrated in a widely tunable laser array with stable lasing characteristics.

2. Light sources in digital coherent systems

An intensity modulation/direct detection (IM/DD) technique called on-off keying (OOK) is used in optical networks with a data rate of 10 Gbit/s or less. As shown in **Fig. 1(a)**, in OOK a data bit [1, 0] is allocated to the intensity of the light. The IM/DD method is widely used because it has the simplest optical component configuration and the most cost-effective method. However, it is difficult to use IM/DD for long-haul transmission with a data rate over 10 Gbit/s because of various limitations such as fiber dispersion, limited wavelength channel spacing, and the speed limitations of electrical circuits. To avoid these

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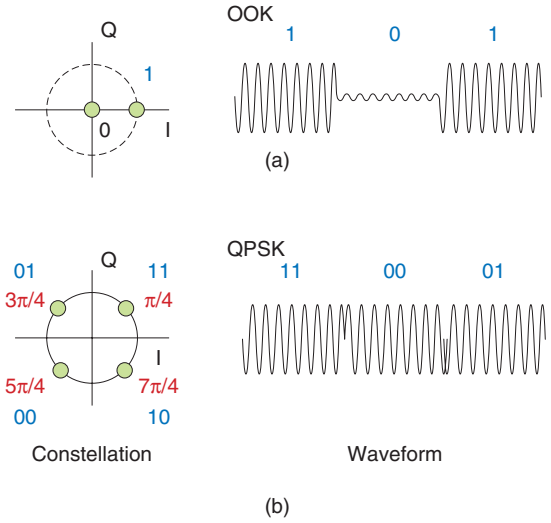

Fig. 1. Modulation format for (a) OOK and (b) QPSK. (Q axis: quadrature component, I axis: in-phase component).

limitations, a phase-shift-keying/differential detection method is used in 40 Gbit/s systems, and a phase-shift-keying/digital coherent detection method will be used in next-generation 100-Gbit/s systems. To make best use of the limited wavelength resource, a multilevel modulation format is used in 100-Gbit/s systems. Quadrature phase shift keying (QPSK) is a four-level modulation format. As shown in **Fig. 1(b)**, four phase states [$\pi/4$, $3\pi/4$, $5\pi/4$, $7\pi/4$] of the lightwave are allocated to two data bits [11, 01, 00, 10]. As a result, the data rate is twice that of a binary modulation signal for the same baud rate. Polarization multiplexing is also used, so the data rate is doubled. Thus, the four-level modulation format and polarization multiplexing enable four 25-Gbaud signals to generate a 100-Gbit/s data signal. Since the baud rate is suppressed to only 25 Gbaud, the modulation spectrum bandwidth is also suppressed to less than 50 GHz. Therefore, this method can be introduced into a DWDM system with a 50-GHz grid spacing. On the receiver side, the phase state of the signal is detected with a coherent detection scheme, where the relative phase of the signal is compared with the phase of a local light source. And a polarization diversity technique is used for the signal polarization state. In digital coherent systems, a tunable laser is also used on the receiver side.

In IM/DD systems, the phase noise of the laser is not an issue because the phase is not used as information. On the other hand, it is a critical issue in digital coherent systems, as described below. In a digital coherent receiver, the frequencies of the local and signal lights should not be exactly the same. The frequency offset is compensated for in a digital signal processor. Although this can compensate for low-speed variations in the phase or frequency, it cannot compensate for high-speed variations due to the intrinsic phase noise of the light sources. Therefore, the phase noise characteristics of the light sources have a great influence on system performance. The spectral linewidth is often used as an index of the amount of phase noise. As shown in **Fig. 2**, when the linewidth is sufficiently narrow, the phase state can be clearly detected in the constellation map. As the linewidth increases, the phase angle variation increases and the phase state can no longer be identified. In a 100-Gbit/s system, a linewidth of 1 MHz or less is required for both the transmitter light source and the local light source [2].

3. Widely wavelength tunable lasers

In the last ten years, various kinds of tunable lasers have been developed, and their performance has been greatly improved. A tunable laser consists of a semiconductor gain region and a wavelength-tunable optical filter. The wavelength is tuned by changing the filter wavelength. Tunable lasers are classified into three structural types: an external cavity laser [3], a distributed feedback (DFB) laser array [4], and a

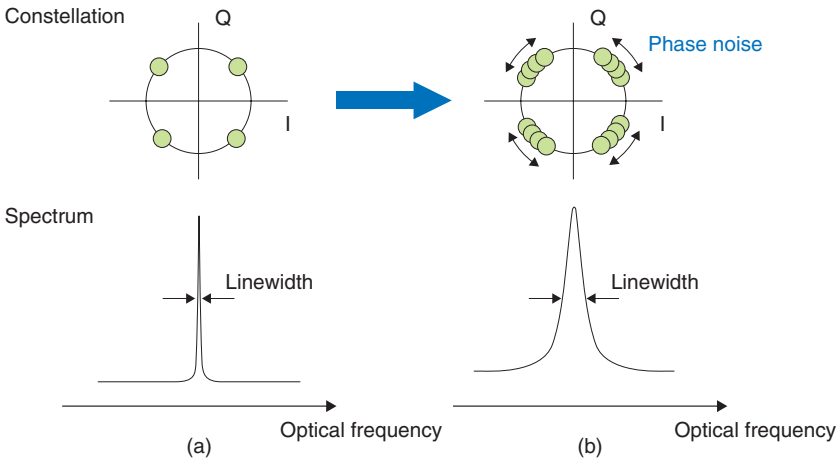

Fig. 2. Influence of laser linewidth in coherent systems.

Table 1. Wavelength-tunable lasers.

Laser structure	Linewidth	Features
External cavity laser	Excellent	Hybrid integration
DFB laser array	Good	Mode-hop free, stable
DBR laser	Fair	Current tuning, high-speed switching

distributed Bragg reflector (DBR) laser [5]–[7]. All of these laser structures provide a tuning range of more than 35 nm, which is required for DWDM systems. The features of the three lasers are summarized in **Table 1**.

The external cavity laser consists of a gain chip and spatially separated external optical filters, which are packaged into a compact optical module by using a hybrid integration technique. This type can easily provide a wide tuning range because optimum optical filters can be selected. For example, external cavity lasers with thermally tunable silicon etalon filters have been commercialized for use in tunable transceivers [8]. Generally, the cavity length is long, and a narrow linewidth of less than 100 kHz can be easily achieved. This laser is a strong candidate for a light source for digital coherent systems. Its drawbacks are that complex tuning control is needed to suppress mode hopping and that it has many optical parts.

The DFB laser array is based on the DFB laser, which has been widely used in commercial optical networks for a long time. The tuning range is expanded by integrating DFB lasers of different wavelengths. An excellent feature of this laser is its mode stability and reliability owing to its mode-hop-free tuning characteristics. Moreover, it is suited to mass production because it is a monolithic chip. Its drawback is its slow wavelength tuning, which is achieved through temperature control. DFB array lasers are widely used in current 10-Gbit/s systems. The linewidth of the conventional DFB laser is several megahertz. However, a narrower linewidth can be obtained by optimizing the cavity structure. Linewidth reduction of a DFB laser array is described in detail in the next section.

A DBR laser is also a monolithic chip. The wavelength can be tuned by controlling the refractive index of the semiconductor-based DBR. Generally, the refractive index is changed by a carrier plasma effect induced by current injection. Therefore, the tuning time is a short as a few nanoseconds. Its drawback is that the linewidth is increased when the tuning current is injected. However, it has been reported that a DBR-type laser with heaters for temperature-based wavelength tuning has a narrow linewidth even during wavelength tuning [9].

As described above, all three laser types have both advantages and disadvantages, and they will be used according to the required application.

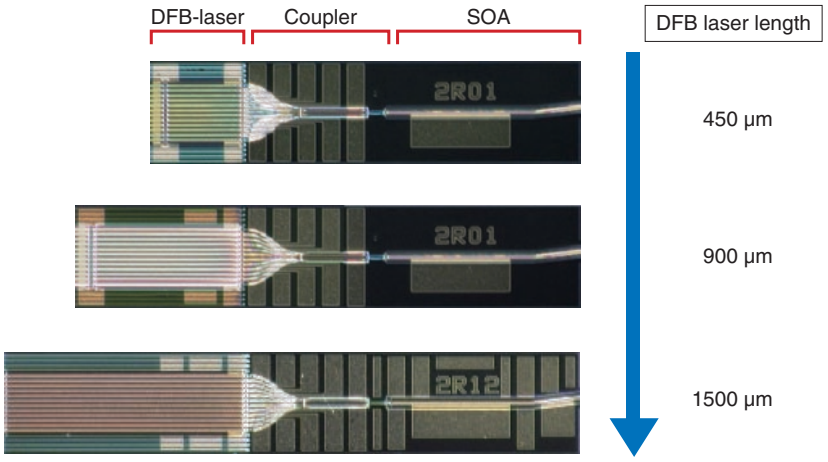

Fig. 3. Photographs of TLA chips with different laser lengths.

4. Narrow-linewidth tunable DFB laser array

We have developed a tunable DFB laser array (TLA) [10], [11] because stable mode characteristics are a great advantage in photonic networks. We have reduced its spectral linewidth, as described below, to make it applicable to 100-Gbit/s systems.

The linewidth in semiconductor lasers is proportional to the ratio of the spontaneous emission noise to the total photon number in the laser cavity [12]. In general, the linewidth can be reduced because the total photon number increases if the laser cavity is lengthened. We fabricated TLAs having longer-cavity DFB lasers and confirmed the linewidth characteristics. Photographs of the TLA chips are shown in **Fig. 3**. The TLA consists of an array of 12 DFB lasers, a 12 × 1 multimode interference (MMI) optical coupler, and a semiconductor optical amplifier (SOA). The output light from each DFB laser is introduced into the MMI coupler through an S-bend waveguide, and the light from the MMI coupler is amplified by the SOA. The length of the SOA region is 1200 µm. We fabricated three types of TLA with DFB laser lengths of 450, 900, and 1500 µm. The three types have the same structure except for the DFB laser length. The DFB lasers and SOA have an active layer composed of compressively strained multiple quantum wells, which is designed to achieve low threshold operation over a wide DFB laser temperature range. The passive waveguide regions consist of an InGaAsP bulk layer with a bandgap wavelength of 1.3 µm. The waveguide was formed with a buried heterostructure of p-n current blocking layers. A λ/4-shifted grating was formed on the DFB laser region by electron beam lithography and wet etching to determine the lasing wavelength precisely. The wavelengths of the lasers were initially set to roughly those specified in the ITU-T grid [13] with a spacing of 400 GHz by designing the grating pitch, which corresponds to wavelength tuning with a temperature change of 35°C (ITU-T: International Telecommunication Union, Telecommunication Standardization Sector). Therefore, the TLA can be operated at an arbitrary optical frequency within a range of 4.8 THz (= 12 × 400 GHz).

The TLA chip was packaged in a butterfly-type pigtail module together with a wavelength locker. The chip contained two thermoelectric coolers: one for the laser and the other for the wavelength locker. It also had two lenses for optical coupling and an optical isolator. The optical coupling efficiency from the chip output to the fiber was about -2 dB. The spectral linewidth on the 97 frequency grids with a 50-GHz spacing is shown in **Fig. 4**. To adjust the frequency on the ITU-T grid, we controlled the laser temperature in the 15–50°C range. The current to the SOA was controlled to maintain fiber output power of 20 mW (13 dBm). The three TLAs covered a frequency range of 4.8 THz. A side-mode suppression ratio of more than 45 dB was obtained for all the frequency grids. We measured the spectral linewidth with a delayed self-heterodyne method using a 5-km single-mode fiber and a 150-MHz acoustic-optic modulator. The linewidths of the TLAs with DFB laser lengths of 450, 900, and 1500 µm were 1–3 MHz, 300–600 kHz, and 90–160 kHz, respectively.

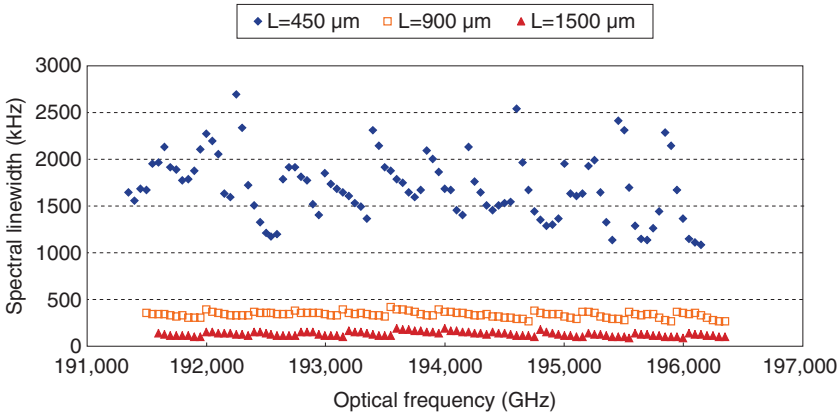

Fig. 4. Spectral linewidth characteristics.

Thus, the linewidths improved with increasing cavity length. The linewidth of a TLA with a DFB laser length of 900 or 1500 μm is less than 1 MHz, which meets the requirement for a 100-Gbit/s system.

5. Conclusions

For the 100-Gbit/s system now being developed as a next-generation optical communication system, we have developed a high-performance tunable laser array with low phase-noise characteristics. Narrow linewidth operation of 90–160 kHz was demonstrated using a TLA with 1500-μm-long DFB lasers. In addition to the linewidth characteristics described here, the tunable laser requires higher power, a wider tuning range, and lower power consumption. Research and development will continue with the aim of obtaining tunable lasers with even better performance.

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Multilevel Optical Modulator Utilizing PLC-$LiNbO_3$ Hybrid-integration Technology

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Abstract

Multilevel optical modulators are key devices for optical transmission systems with transmission rates of 100 Gbit/s and beyond. For such modulators, NTT Photonics Laboratories has developed hybrid-integration technology for silica planar lightwave circuits (PLCs) and $LiNbO_3$ phase modulator arrays. This makes possible various kinds of multilevel modulator featuring a compact size, low loss, and high scalability. We review our recent progress in PLC-$LiNbO_3$ technology and describe some integrated multilevel modulators: 100-Gbit/s PDM-QPSK and post-100G OFDM-QPSK and 64QAM modulators (PDM: polarization-division multiplexing, QPSK: quadrature phase-shift keying, 100G: 100-Gbit/s, OFDM: orthogonal frequency-division multiplexing, QAM: quadrature amplitude modulation).

1. Introduction

Future large-capacity wavelength-division-multiplexing (WDM) transmission systems will require advanced spectrally efficient multilevel modulation formats, such as N-level phase-shift keying (N-PSK), N-level quadrature amplitude modulation (N-QAM), and orthogonal frequency-division multiplexing (OFDM), combined with polarization-division multiplexing (PDM) [1]. High-level QAMs have been used in the latest record-setting experiments: transmission of 69.1 Tbit/s using PDM-16QAM [2], the highest spectral efficiency (SE) for 100-Gbit/s/ch-class transmission of 9.0 bit/s/Hz with PDM-64QAM [3], and the highest potential SE of 12.4 bit/s/Hz with PDM-512QAM [4] (ch: channel). OFDM is promising not only for achieving a high SE [5], but also for enabling a bandwidth-variable optical network for efficient use of the spectral resource [6].

To accomplish those advanced modulations, multilevel electronics, such as arbitrary waveform generators or digital-to-analog converters, have been used in many transmission experiments [3], [4], [7]. They let us cover various modulation formats with a simple optical setup. On the other hand, optical multilevel-signal syntheses, in which only binary electronics are used, have also been studied extensively [2], [5], [8]–[22]. Those schemes are promising for high-speed multilevel modulations because binary electronics pose fewer challenges for high-speed operation than multilevel electronics do [13], [15], [16].

In this article, we briefly review technologies for optical multilevel-signal syntheses and describe our recent work on integrated multilevel optical modulators using a hybrid configuration of silica planar lightwave circuits (PLCs) and $LiNbO_3$ (LN) phase modulators.

2. Optical multilevel-signal syntheses and integrated optical modulators

There have been many studies in which multilevel optical modulations are achieved with combinations of simple commercially available modulators, such as Mach-Zehnder modulators (MZMs), straight phase

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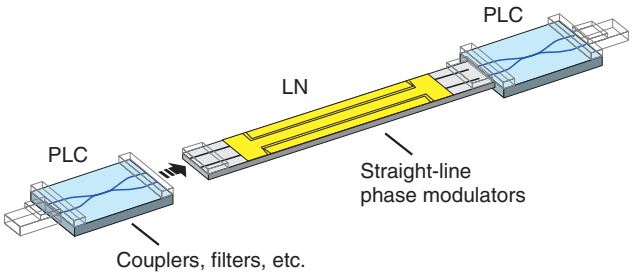

Fig. 1. PLC-LN structure.

modulators, and I/Q modulators with a dual-parallel MZM configuration (I: in-phase component, Q: quadrature component). By connecting those modulators in tandem and adjusting the amplitude of each binary driving signal to an appropriate value, researchers have achieved multilevel modulations, such as 8PSK [8], 16APSK [9], [10], 8QAM [11], and 16QAM [11], with high baud rates (ASPK: amplitude and phase key shifting).

Integrated multilevel modulators have also attracted much attention [12]–[22]. The integration provides two major advantages. First, the transmitter setup is significantly smaller. Second, we can connect modulator components in parallel much more easily than in the case of discrete modulators because integration eliminates fiber connection, which causes optical-phase fluctuation. A parallel configuration enables us to use *superposed modulation*, which was originally demonstrated with high-speed microwave transmission [23]. Integrated modulators for 16QAM have been demonstrated with several configurations, such as a quad-parallel MZM configuration fabricated with LN and PLCs [12], a five-arm configuration with quad-parallel electro-absorption modulators fabricated with InP [13], and a dual-parallel dual-tandem MZM configuration fabricated with LN [14].

In multilevel modulator design, it is worth exploiting a particular characteristic of MZMs. When the MZM is driven in a push-pull condition with a signal amplitude of 2Vπ (binary PSK mode), the output optical signal has smaller distortions in symbol levels than the driving electrical signal. This is because the output optical field of the MZM varies sinusoidally with the driving voltage [15]. For various modulation formats, transmitter configurations with only 2Vπ MZMs have also been investigated [15], [16]. The key to implementing those all-2Vπ-MZM configurations is the integration of MZMs and high-quality passive optics because accurate control of the relative optical amplitude and phase in each optical path is required.

To achieve such integrations with high performance levels, we have been developing hybrid integration technology for PLCs and LN phase modulators.

3. PLC-LN modulators

3.1 Basic structure and concept

The basic structure of a hybrid-integrated PLC-LN modulator is shown in **Fig. 1**. We use an LN chip containing an array of simple straight phase modulators and PLCs containing all the other circuit components, such as couplers and filters. This structure combines the large electro-optic bandwidth of LN and the excellent transparency and design flexibility of PLCs. Another advantage is that this configuration is highly scalable because we can increase the integration level by increasing the number of phase modulator arrays in the LN chip and devising PLCs with corresponding complexity. As shown in **Fig. 2**, we have developed various modulators with increasing integration levels [17]–[22]. Each modulator circuit consists only of 2Vπ MZMs and passive components. Below, we describe PLC-LN modulators based on PDM-QPSK for 100 Gbit/s and based on OFDM-QPSK and 64QAM for post-100G applications. We also briefly describe a modulator with a selectable modulation level for post-100G applications.

3.2 100-Gbit/s PDM-QPSK modulator

The configuration of the PDM-QPSK modulator [19] utilizing PLC-LN integration technology is shown in **Fig. 3(a)**. Eight straight phase modulators with four high-speed signal electrodes in a Z-cut LN chip and thirteen couplers in PLCs make up two QPSK modulator circuits connected in parallel. In addition, a polarization multiplexing circuit, consisting of a polarization rotator with a half-wavelength

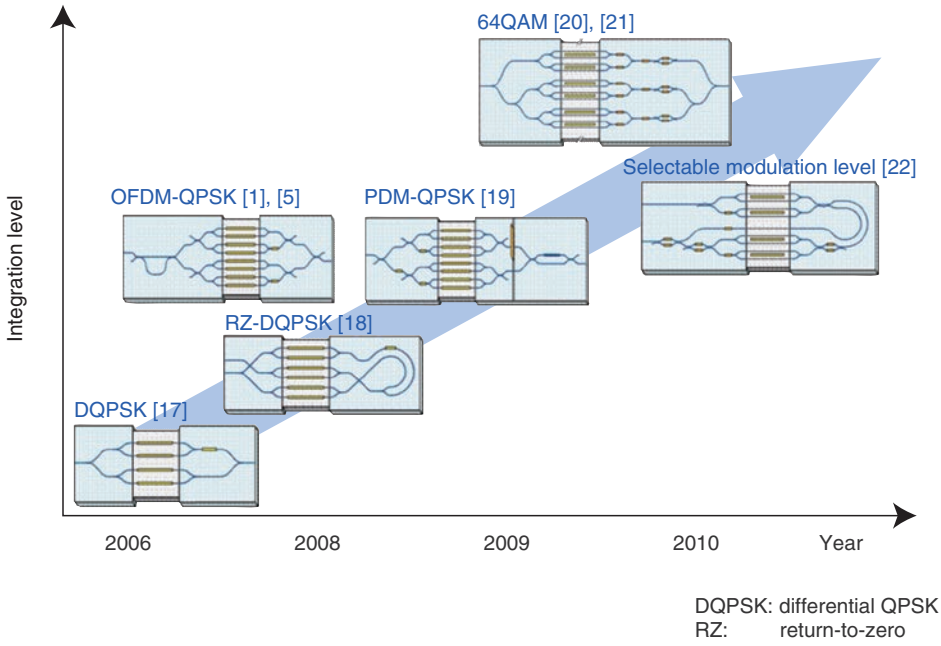

Fig. 2. PLC-LN hybrid modulators.

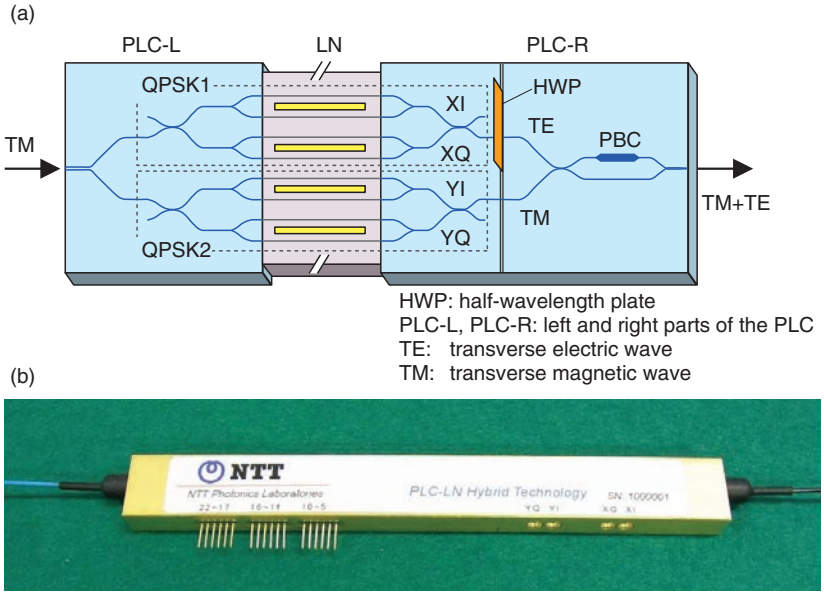

Fig. 3. (a) Configuration and (b) photograph of 100-Gbit/s PDM-QPSK utilizing PLC-LN integration technology. 100G denotes 100 Gbit/s. (package size: 118 mm x 13.5 mm x 7 mm)

plate, and a waveguide polarization beam combiner (PBC) are connected to their output. A PLC-type PBC is a compact Mach-Zehnder interferometer (MZI) about 10 mm in length and has an excellent polarization extinction ratio of greater than 25 dB over the whole C-band wavelength range [24]. A photograph of this module is shown in **Fig. 3(b)**. The module package size is 118 mm × 13.5 mm × 7 mm. Including the fiber boots on both sides, it is 131 mm long, which approaches the smallest size ever reported.

Typical characteristics of a 100-Gbit/s PDM-QPSK

modulator are listed in **Table 1**. The overall optical insertion loss of our PDM-QPSK modulator is 8.7 dB at a wavelength of 1.55 μm including a polarization division intrinsic loss of 3 dB. The modulator's frequency response is shown in **Fig. 4**. XI, XQ, YI, and YQ correspond to the four MZMs shown in Fig. 3(a).

The modulator has an electro-optic 3-dB bandwidth of more than 27 GHz. The driving voltage was less than 3.5 V at 32 Gbit/s. The measured eye pattern for a driving voltage of 3.0 V when the modulator was driven with 32-Gbit/s non-return-to-zero 2^{31}-1 pseudorandom bit sequences in a back-to-back setup is shown in **Fig. 5**. Clear eye opening was obtained in this experiment. The Optical Internetworking Forum (OIF) standardized a 100-Gbit/s integrated modulator in April 2010 [25]. Our 100-Gbit/s PDM-QPSK modulator complies with the target specifications.

3.3 OFDM-QPSK modulator

The configuration of the OFDM-QPSK modulator [1], [5] is shown in **Fig. 6**. The modulator integrates a PLC interleave filter, two QPSK modulation circuits, each with a dual-parallel MZM configuration, and an output coupler. The input light for this modulator consists of two subcarriers, which can be generated by using another MZM driven with a clock signal. The subcarriers are separated by the interleave filter and modulated by different QPSK modulation circuits. The two QPSK signals are finally coupled and the modulator outputs a two-subcarrier OFDM-QPSK signal. The baud rate of the modulation, which is equal to the frequency spacing between the subcarriers, is 13.9 Gbaud.

The spectrum of a 111-Gbit/s PDM-OFDM-QPSK signal generated with the modulator and an external PDM circuit is shown in **Fig. 7**. The signal bandwidth is 42 GHz, which is 1.5 times the baud rate and narrow enough for 50-GHz-grid WDM transmission. Using this modulator, we achieved 13.5-Tbit/s (135 × 111-Gbit/s/ch) WDM transmission over a distance of 7209 km [1], [5].

3.4 64QAM modulator

The configuration of the 64QAM modulator [20], [21] is shown in **Fig. 8**. Three QPSK modulation circuits, each consisting of dual-parallel MZMs, are connected in parallel by a pair of PLC asymmetric 1×3/3×1 splitter/combiners, each with a power splitting/combining ratio of 4:2:1. These asymmetric circuits were designed using the wavefront-matching method, which lets us optimize the waveguide pattern on the basis of the desired splitting/combining ratio. PLC variable optical attenuators enable fine tuning of the power ratio. The 64QAM signal is synthesized by coupling the three QPSK signals with a field-amplitude ratio of 4:2:1 (power ratio of 16:4:1). The module has a small overall optical insertion loss of 5.5 dB,

Table 1. Typical characteristics and target specifications of a 100-Gbit/s PDM-QPSK modulator.

Parameter	Achieved value	Target value
Insertion loss	8.7 dB	< 14 dB
Polarization division loss	0.1 dB	< 1.5 dB
Optical return loss	> 35 dB	> 30 dB
Extinction ratio: parent MZI	> 46 dB	> 22 dB
child MZI	> 25 dB	> 20 dB
Polarization extinction ratio	31 dB	> 20 dB
Electro-optical bandwidth	> 27 GHz	> 23 GHz
RF port Vπ @ 32 Gbaud	< 3.5 V	< 3.5 V

RF: radio frequency

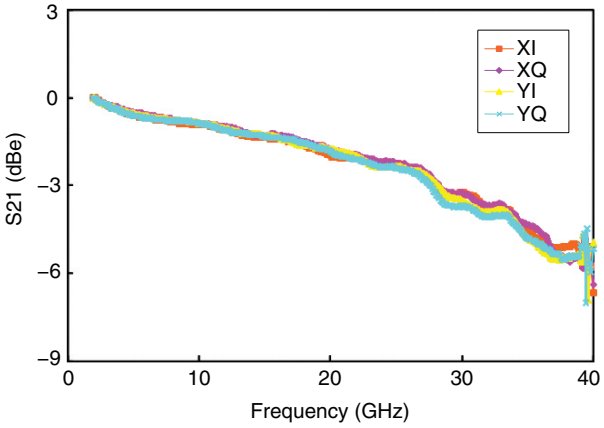

Fig. 4. Frequency response.

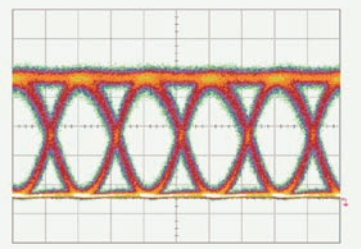

Fig. 5. Measured eye pattern.

as well as a broad electro-optic bandwidth of >25 GHz.

By driving the modulator with six 20-Gbaud binary data signals and using an external PDM circuit, we generated a 240-Gbit/s PDM-64QAM signal [20]. The signal was received with a coherent receiver using a pilotless demodulation algorithm in an offline digital signal processor. The constellations obtained with a back-to-back intradyne setup are shown in **Fig. 9**. The 64 signal points are clearly distinguished. The bit-error rate was better than 1.3×10^{-2}. Thus, we successfully demonstrated the record bit rate of 240 Gbit/s for PDM-64QAM using the modulator.

3.5 Selectable-modulation-level modulator

We also developed a selectable-modulation-level modulator that lets us select QPSK, 8PSK, 8QAM, or 16QAM [22], [26]. This modulator was devised for use in optical networks with a flexible modulation format, which have become the focus of attention in recent years [6]. In this modulator, we can flexibly and adaptively select a suitable multilevel modulation scheme taking account of the transmission condition.

4. Conclusion

We have developed PLC-LN hybrid integration technology for advanced multilevel modulators. Utilizing this technology, we have demonstrated various advanced multilevel modulators, such as a PDM-QPSK modulator for 100 Gbit/s and an OFDM-QPSK modulator, a 64QAM modulator, and a selectable-modulation-level modulator for post-100G applications. Each modulator shows excellent characteristics in terms of compact size and low insertion optical loss and a practical level of optical loss and electro-optic bandwidth. This technology is promising for optical transmission systems with channel rates of 100 Gbit/s/ch and beyond and a transfer rate well above 10 Tbit/s and for future optical networks.

Acknowledgments

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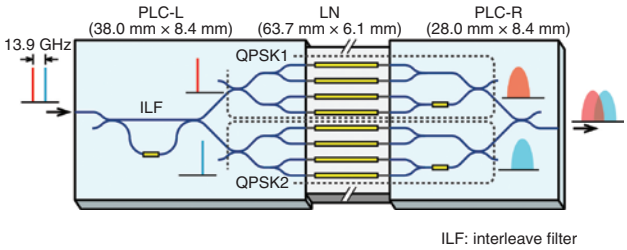

Fig. 6. Configuration of the OFDM-QPSK modulator.

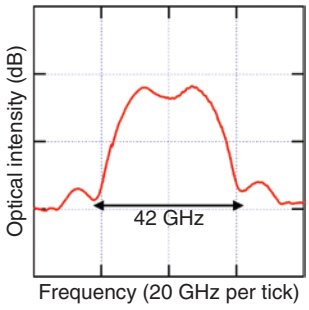

Fig. 7. Optical signal spectrum of 111-Gbit/s PDM-OFDM-QPSK signals.

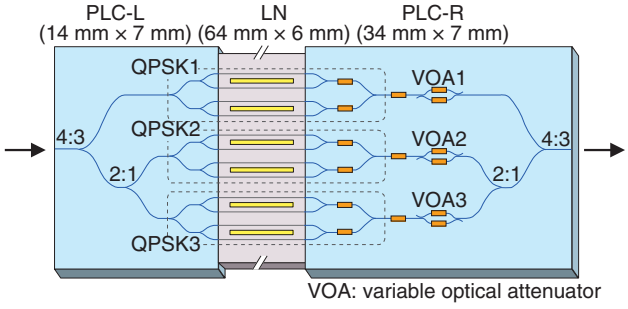

Fig. 8. Configuration of the 64QAM modulator.

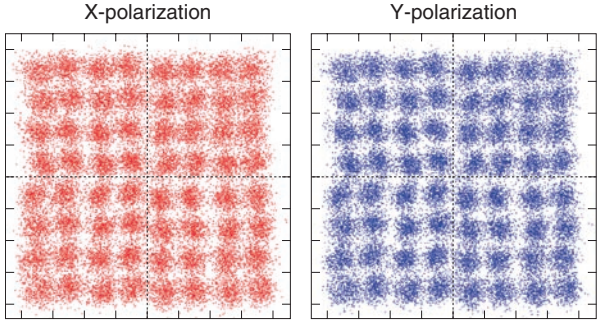

Fig. 9. Constellations of 240-Gbit/s PDM-64QAM signal.

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100-Gbit/s Optical Receiver Front-end Module Technology

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Abstract

We have been developing a 100-Gbit/s-class optical receiver front-end module with a hybrid integration structure using silica-based planar lightwave circuit technology to perform demultiplexing and demodulation in digital coherent photonic network systems. In this article, we describe the module structure and the integration technology that we have developed at NTT Photonics Laboratories.

1. Configuration of digital coherent receiver

Digital coherent communication technology, which is based on techniques for multilevel phase modulation and digital coherent reception, is being studied as a way to achieve ultrahigh-speed photonic networks with a bit rate of 100 Gbit/s or more per channel. Among several reported modulation formats and multiplexing techniques, polarization division multiplexed quadrature phase shift keying (PDM-QPSK)*1 is promising for spectral efficiency and resistance to various types of dispersion, and it is being developed intensively.

The basic configuration of the PDM-QPSK digital coherent receiver is shown in **Fig. 1** [1]. The receiver is composed of an optical front-end (FE), which includes components from the optical input section to the transimpedance amplifiers (TIAs), analog-to-digital converters (ADCs), and a digital signal processor (DSP).

The optical receiver FE consists of an optical signal processing section with a polarization beam splitter (PBS), a beam splitter (BS), and two 90° optical hybrid mixers and an optical-to-electrical (OE) conversion section with eight photodiodes (PDs) and four TIAs. With this receiver FE, the input PDM-QPSK-modulated signal light is separated into orthogonal polarization components (X/Y polarized waves) and orthogonal phase components (I/Q channels; I: in-phase component, Q: quadrature component), which are converted into four high-speed differential electrical signals and output.

The optical receiver FE has functions for optical-domain signal processing and OE conversion and is composed of many optical/electrical components. This creates a need for high-density and well-controlled fabrication techniques for optoelectronic integration.

2. Fabrication issues and approaches for optical receiver FE

Compared with conventional intensity modulation direct detection methods, the digital coherent optical receiver FE requires more-sophisticated functionality. This is because precise and stable optical signal processing is required to separate the X/Y and I/Q components, and the phase and amplitude of the separated signals must be preserved in the connection from the optical stage to the electrical stage in order to achieve the required receiver performance. However,

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*1 PDM-QPSK: A type of phase modulation for digital signals. Two bits of data are allocated using four phase modulations on each of the TE- and TM-polarized lights.

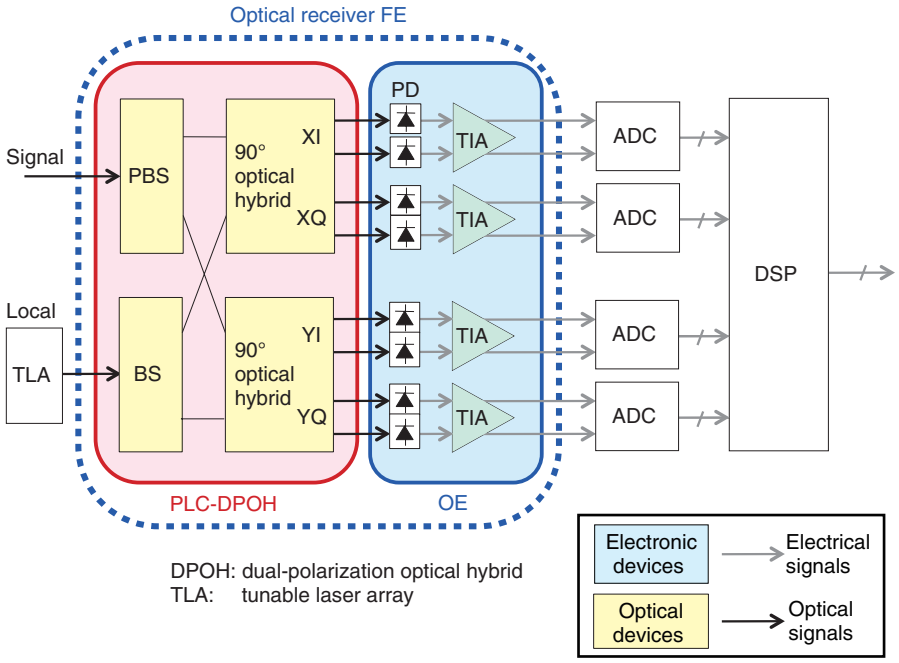


Fig. 1. Configuration of digital coherent receiver.

in conventional technologies using multiple optical fibers interconnecting individual devices, it is difficult to consistently control the optical phase and differential delay between fibers. In other words, implementation of the signal processing from the optical stage through to the electrical stage in a stable integrated circuit has been a critical issue for achieving a practical, digital coherent optical receiver FE and obtaining the required receiver performance.

At NTT Photonics Laboratories, we are developing basic techniques for hybrid integration using silica-based planar lightwave circuits (PLCs). We have successfully fabricated an integrated optical receiver FE module incorporating all the required functions, including a PBS, in a single package [2].

3. Module structure of integrated optical receiver FE and developed techniques

A photograph of the integrated optical receiver FE module with the upper cover removed is shown in **Fig. 2**. The FE is composed of optical signal processing circuits and the OE sub-assembly. We integrated the optical signal processing section including PBS, BS, and two 90° optical hybrid mixers in a single-chip PLC. The OE sub-assembly contains PD and TIA arrays in a compact, hermetically sealed package. A cross-section of the structure near the optical connection between the PLC and OE subassembly is illustrated in **Fig. 3**. The multiport optical connection between the PLC output ends and the PD array mounted in the OE subassembly is implemented with a micro optic system using a micro-lens array and 90° folding mirror. The power supply and electrical control and signal-output lines are all connected to an external board by flexible printed circuit boards. The module size is 27 × 50 × 6 mm^3. The hybrid integration structure lets us use appropriate devices with optimal materials and structures for both the optical signal processing and OE conversion sections, enabling us to achieve compact integration while maintaining maximal performance and reliability for the module as a whole.

Below, we give an overview of the elemental technologies developed for this integration.

3.1 Digital coherent optical receiver circuit integrated on a single silica PLC chip

The optical signal processing required on the optical receiver FE needs stable and highly accurate control of optical phase and interference. To achieve this, we designed a single-chip PLC integrating two PBSs and two 90° optical hybrids [3]. We call this circuit a dual-polarization optical hybrid (DPOH). The circuit

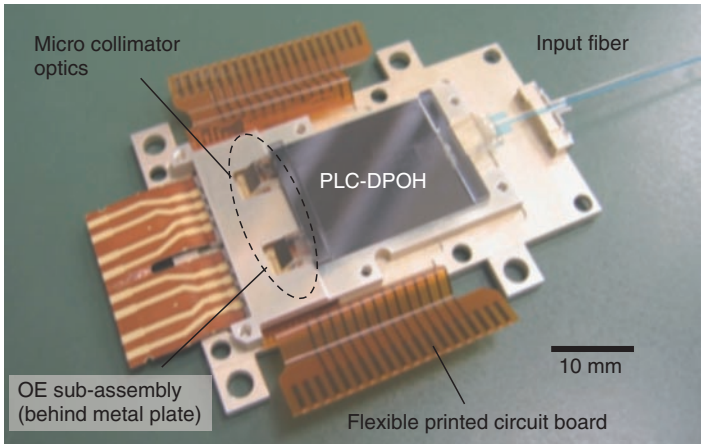


Fig. 2. Integrated optical receiver front-end module.

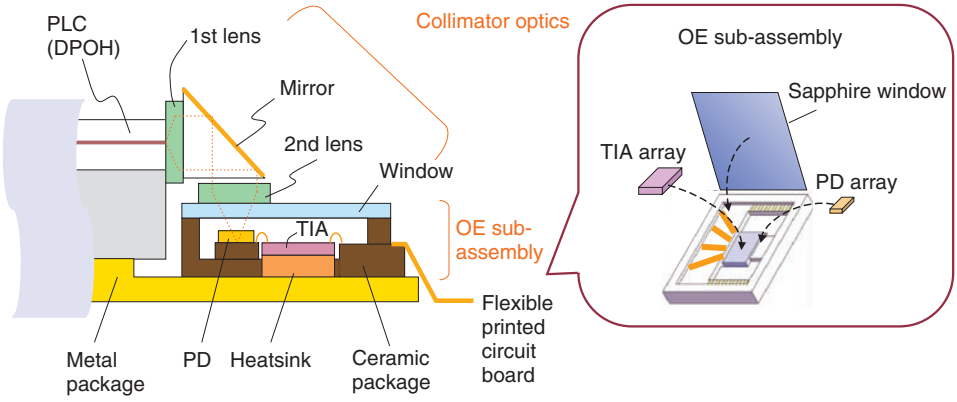


Fig. 3. Integration structure.

configuration is shown in **Fig. 4**. The PBS consists of a Mach-Zehnder interferometer[*2] with grooves formed near one waveguide arm, giving a phase difference of π to the orthogonal polarized waves [4]. This configuration yields a PBS that outputs TE-polarized light from the cross port and TM-polarized light from the through port (TE: transverse electric, TM: transverse magnetic).

The 90° hybrid is structured with optical waveguides arranged to interlace with optical couplers, and 2 × 2 multi-mode interference (MMI) couplers are used. There are various kinds of waveguide-type optical hybrids, such as a slab coupler [5] and a 4 × 4 MMI coupler [6], but this circuit with the interlaced optical-coupler has the benefits of achieving both low loss and orthogonality (phase difference of 90°).

For the DPOH, important performance indexes are the polarization extinction ratio in the PBS, orthogonality in the optical hybrid, and losses and deviations. The fabricated DPOH exhibited excellent results for these: we measured excess loss of less than 2.5 dB, loss deviations of less than 0.2 dB, and a polarization extinction ratio greater than 25 dB. As shown in **Fig. 5**, good values for orthogonality were also obtained: less than ±1° over the wide wavelength range from 1520 nm to 1620 nm.

*2 Mach–Zehnder interferometer: An optical circuit configuration that uses interference between two optical paths to change the light intensity.

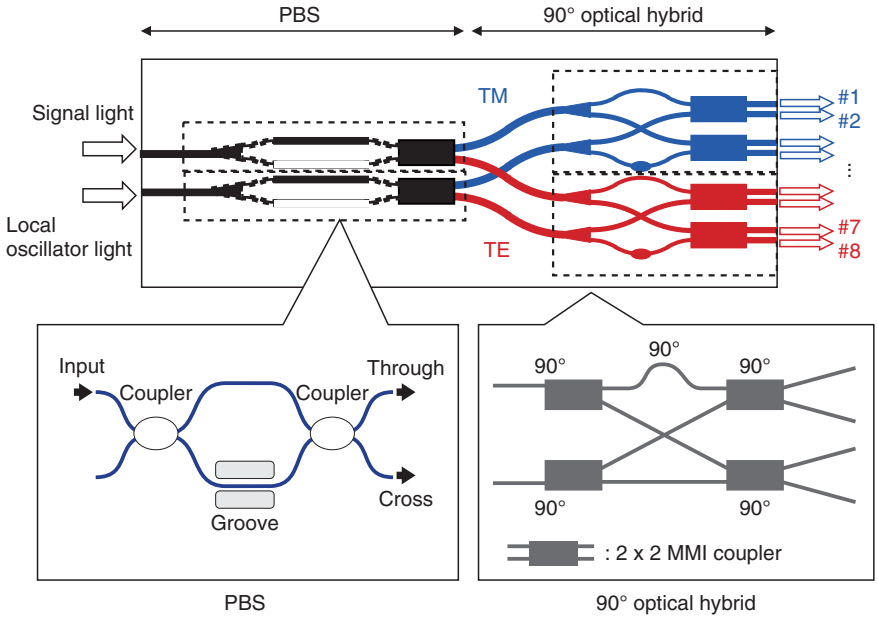


Fig. 4. Circuit configuration of dual polarization optical hybrid (DPOH).

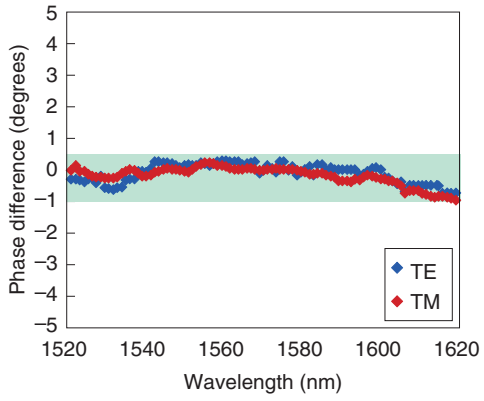


Fig. 5. Phase difference of fabricated DPOH.

3.2 Compact, hermetically sealed OE subassembly

The optical-receiver-FE's OE-conversion section requires high reliability and high-speed operation for receiving 100-Gbit/s-class PDM-QPSK signals. Moreover, for hybrid integration, an optical interface for multi-port optical connection to the optical waveguides is required. We have developed a compact, hermetically sealed OE sub-assembly that meets these requirements.

The OE sub-assembly consists of a layered alumina-ceramic cavity in which the two-channel dual-PD and two-channel TIA arrays are assembled (Fig. 3). The high-frequency signal lines and power/control electrical wiring are also formed on the ceramic layer. The upper surface of the cavity is hermetically sealed by a sapphire window and AuSn solder. The size of the fabricated OE subassembly is $8.2 \times 9.2 \times 1.4$ mm^3. We confirmed that the high-frequency signal lines on this package have a 3-dB transmission bandwidth of more than 40 GHz. The sapphire window provides the hermetic seal required to ensure reliability of the InP semiconductor device while also functioning as the optical interface: it provides an optical window and a fixed surface for the optical connection to external devices. This structure allows us to obtain efficient multi-port optical connections between incident lights and the PD array by using a micro-lens array.

3.3 Multi-port optical connection using micro-lens array

The optical connection between the DPOH and PD must be small in size and have low losses and stability with respect to fluctuations in ambient temperature. To achieve this, we chose to use a micro collimated optical system using a micro-lens array. The first lens is at the PLC's output facet and the second lens is on the surface of the sapphire window of the OE sub-assembly; these lenses were fixed with

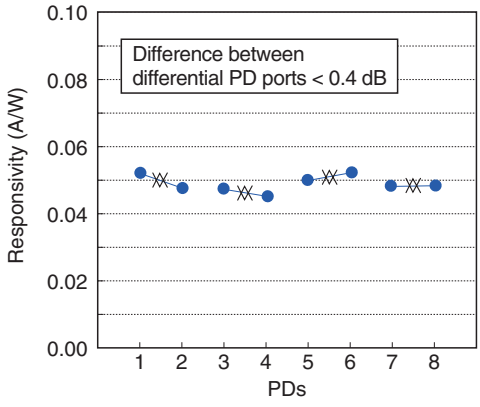


Fig. 6. Responsivity of fabricated optical receiver FE module.

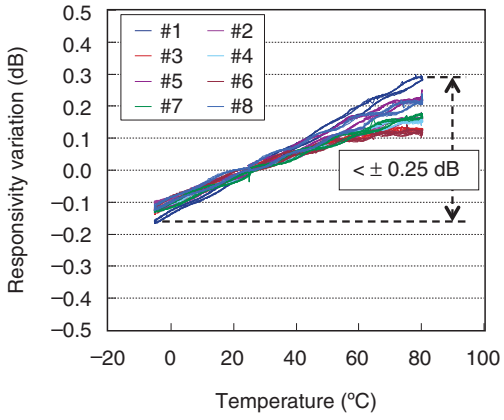
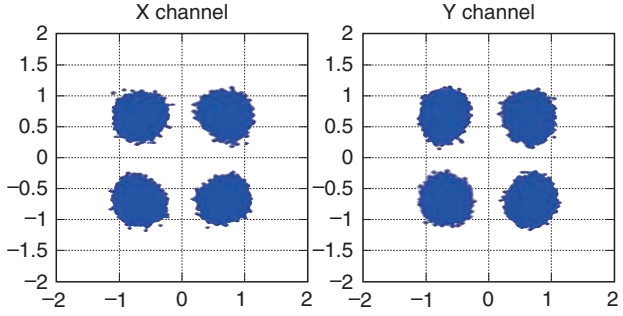
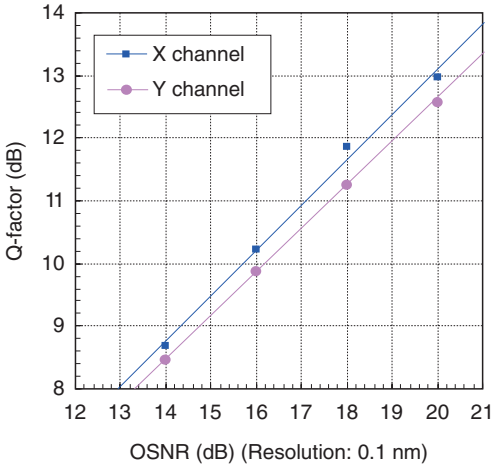


Fig. 7. Relationship between responsivity and temperature.



(a) Constellation



(b) Relationship between Q-factor and OSNR

Fig. 8. Receiver characteristics for 112-Gbit/s PDM-QPSK signal.

ultraviolet-curable adhesive. We used a mirror between the two lenses to change the optical axis of the light emitted from the PLC by 90° and inject it into the PD. With this structure, we achieved an extremely compact optical connection with an optical path length of only about 2.5 mm.

In designing the optical system, it is important to ensure a wide tolerance so as to avoid PD responsivity degradation and port-to-port deviation, even when the positions of the PLC output ends and PDs shift owing to ambient temperature variation. For the fabricated receiver FE module, the maximum optical misalignment caused by differences in thermal expansion coefficients across the operating temperature range of -5 to 80°C was estimated to be ±5 μm, so the module was designed to handle this. The measured tolerance of the designed micro collimator optics system was more than ±10 μm for a 0.2-dB-down width, ensuring sufficient tolerance for the operating temperature range.

4. Characteristics of fabricated PDM-QPSK coherent receiver FE module

The measured responsivity for all ports on the fabricated receiver FE module is shown in **Fig. 6**. It includes the sensitivity characteristics of the PDs themselves as well as an intrinsic loss of 9 dB from

the DPOH. Besides these, excess losses caused by the optical system were estimated to be 0.4 dB, and the responsivity deviation between adjacent PDs was less than 0.4 dB, so we achieved good optical connection performance in terms of both losses and deviation. The relationship between ambient temperature and responsivity is shown in **Fig. 7**. The responsivity variation was less than ±0.25 dB in the operating temperature range of -5 to 80°C.

Next, we tested the receiver operation for a 112-Gbit/s PDM-QPSK signal. The constellation plot and relationship between optical signal-to-noise ratio (OSNR) and Q-factor are shown in **Fig. 8**. These results confirm stable operation as a 100-Gbit/s-class optical receiver FE.

5. Future plans

We plan to make further improvements to the key device technology such as PLC, PD, and TIA, and their integration technology. We will also expand their applications in next-generation optical integration modules needed for 100-Gbit/s-class-and-higher multilevel-modulation optical transmission systems.

Acknowledgments

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Photodiodes and Transimpedance Amplifiers for 100-Gbit/s Digital Coherent Optical Communications

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Abstract

To increase transmission capacity and extend transmission distance, 100-Gbit/s digital coherent optical communications systems have been researched. NTT Photonics Laboratories has developed photodiodes that exhibit a good high-frequency response even under high optical input power and transimpedance amplifiers that have both broadband characteristics and a wide input dynamic range.

1. Introduction

To markedly increase transmission capacity and extend transmission distance, 100-Gbit/s digital coherent optical communications systems have recently been researched and developed. The architecture of optical receivers for such systems is shown in **Fig. 1**. A signal light transmitted through optical fibers (bit rate: 125.6 Gbit/s) and a local light (continuous wave) are input to the optical receiver simultaneously. The local light is necessary in order to decode the signal light, whose signal format is dual polarization quadrature phase shift keying (DP-QPSK). Both the signal light and local light have two optical polarization components (X pol. and Y pol.). Each light is split into beams with different polarizations by polarization beam splitters. Then, the polarization-split lights are fed into 90° optical hybrids. There the signal and local lights are mixed, and two optical-phase-multiplexed components (I and Q, which denote in-phase and quadrature, respectively) in the signal light are separated. The outputs of the 90° optical hybrids are of the differential style, so each hybrid has four outputs (I-pos., I-neg, Q-pos., and Q-neg. (pos.: positive, neg.: negative)). With the polarization beam splitters and the 90° optical hybrids, the signal light, which is both optical polarization multiplexed and optical phase multiplexed, is separated into four independent differential signals. Therefore, the baud rate of each of the four separated differential signals is 31.4 Gbaud, i.e., one-fourth that of the signal light.

Photodiodes (PDs) convert the high-speed (31.4-Gbaud) optical signals into electrical current ones. To convert four differential optical signals, eight PDs are installed in the optical receiver.

Transimpedance amplifiers (TIAs) transform the high-speed electrical current signals into electrical voltage ones, and they linearly amplify the signals to output a constant voltage amplitude that the following analog-to-digital converters can handle. To transform and amplify four differential electrical signals independently, four TIAs are used in the optical receiver.

2. PDs for 100-Gbit/s digital coherent optical communications systems

In 100-Gbit/s digital coherent optical communication systems, high-power local light is used as one of the inputs for the optical receiver. Therefore, PDs that exhibit a good high-frequency response even under high optical input power are required. To meet this

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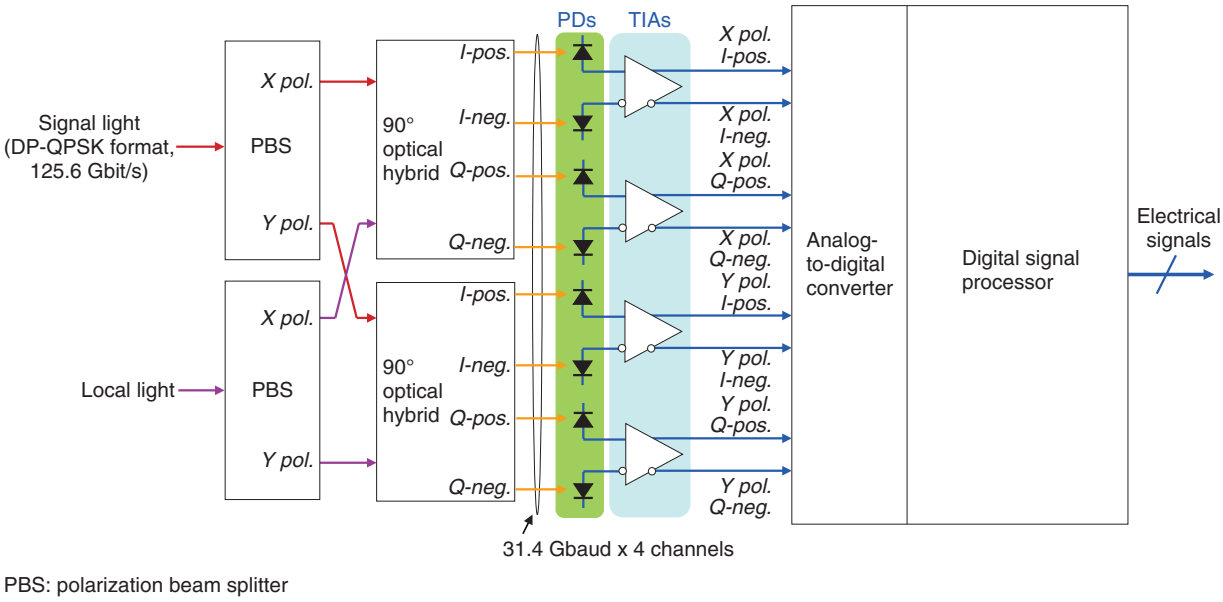


Fig. 1. Architecture of optical receiver for 100-Gbit/s digital coherent optical communications.

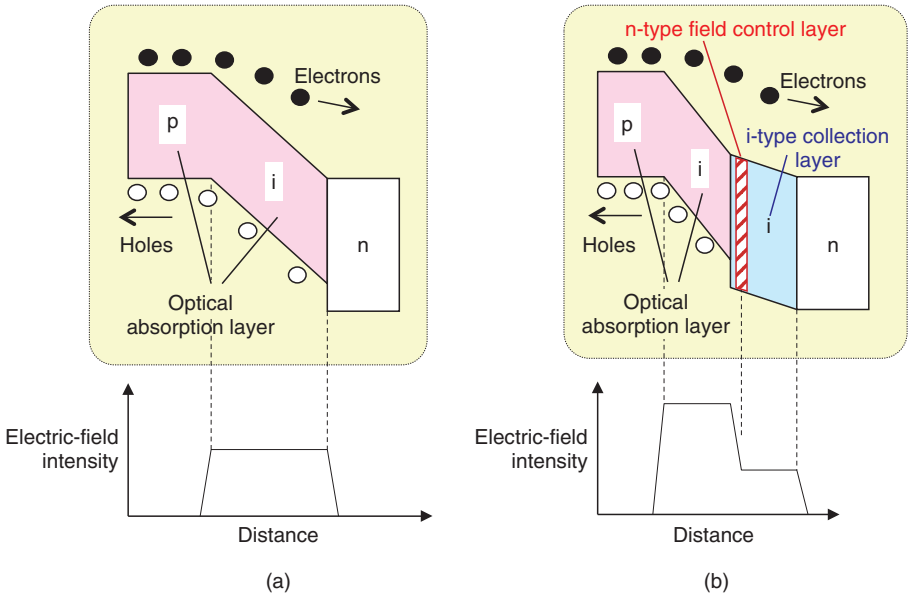


Fig. 2. Energy band diagrams for (a) conventional MIC-PD and (b) composite-field MIC-PD.

requirement, we have developed a new type of PD called a composite-field maximized-induced-current PD (composite-field MIC-PD) [1]. The energy band diagrams for the conventional MIC-PD and the composite-field MIC-PD are compared in **Fig. 2**. In the case of the conventional MIC-PD, under high optical input power, the many holes that accumulate in the intrinsic (i-type) optical absorption layer weaken the electrical field and degrade the high-frequency responses of holes and electrons. This effect is known as the space charge effect. In the composite-field MIC-PD, to mitigate the space charge effect, a

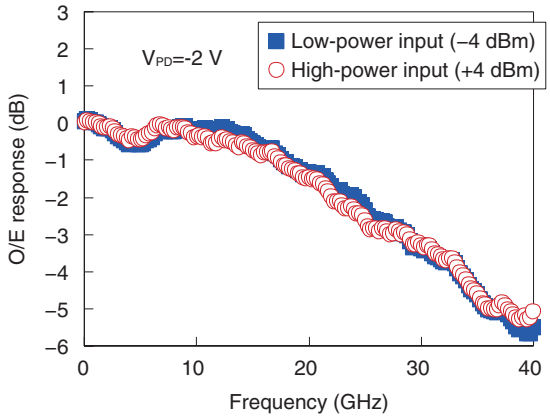


Fig. 3. Frequency optical-to-electrical (O/E) responses for a fabricated composite-field MIC-PD under optical input power of -4 dBm (low-power input) and +4 dBm (high-power input).

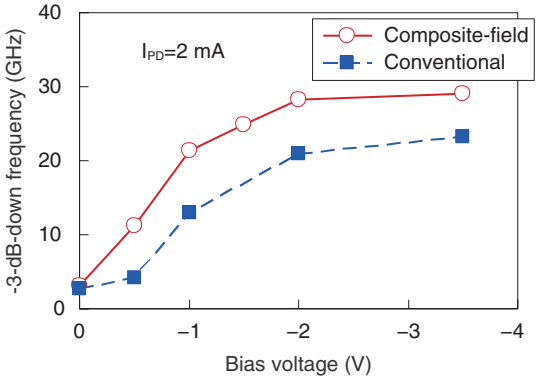


Fig. 4. Bias voltage dependencies of -3-dB-down frequencies for the composite-field MIC-PD and conventional MIC-PD.

negative (n-type) field control layer and an i-type wide bandgap collection layer are newly introduced. These layers strengthen the electrical field of the i-type optical absorption layer and lead to improved high-frequency responses of holes and electrons under high optical input power.

Measured frequency responses for a fabricated composite-field MIC-PD under optical input power of -4 dBm (low-power input) and +4 dBm (high-power input) are shown in **Fig. 3**. For both inputs, the frequency responses are almost the same. The -3-dB-down frequencies for both inputs are 29 GHz. This result demonstrates that the composite-field MIC-PD relaxes the space charge effect and exhibits good high-frequency responses even under high optical input power.

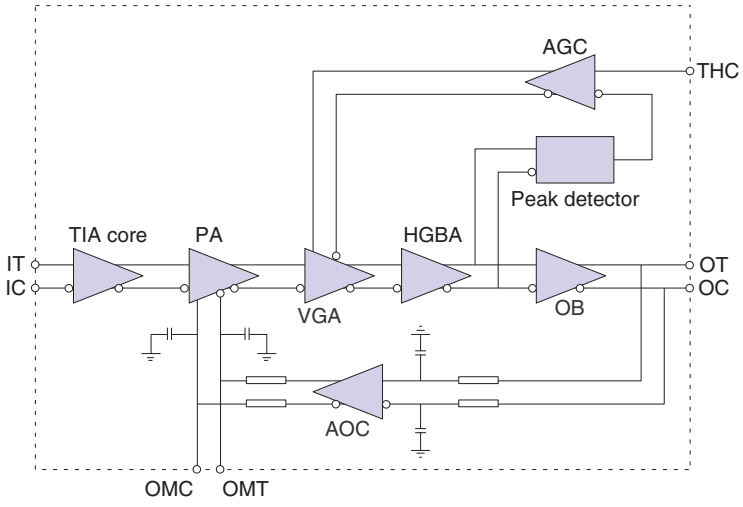
The measured bias voltage dependences of the -3-dB-down frequencies of the composite-field and conventional MIC-PDs are compared in **Fig. 4**. In the measurement, the photocurrent value was set to 2 mA, which is close to real photocurrent values in 100-Gbit/s systems. While the conventional MIC-PD requires a bias voltage of -3.5 V for a 24-GHz -3-dB-down frequency, the composite-field MIC-PD achieves a 29-GHz -3-dB-down frequency with only a -2-V bias voltage. This shows that the electrical field of the i-type optical absorption layer is sufficiently strengthened with a bias voltage as low as -2 V. The responsivity of the composite-field MIC-PD is around 0.8 A/W, which is also high enough for 100-Gbit/s systems.

3. TIAs for 100-Gbit/s digital coherent optical communications systems

In 100-Gbit/s digital coherent optical communications systems, TIAs need to amplify high-speed electrical signals of 31.4 Gbaud. It is empirically known that amplification of a B-baud signal needs bandwidth of 0.7B Hz, where B denotes the baud value. Therefore, TIAs require a broad bandwidth of 31.4 Gbaud × 0.7 = 22 GHz. In addition to the broad bandwidth, TIAs must maintain a constant voltage amplitude in a wide input current range of ~100 μA to ~1 mA

In designing a TIA that could satisfy the above requirements, we used InP heterojunction bipolar transistors (HBTs) with a 1-μm-wide emitter. Since these InP HBTs exhibit high-frequency characteristics represented by a high current cut-off frequency (fT) of 170 GHz, they are suitable for designing a TIA with a broad bandwidth of over 22 GHz.

The circuit diagram of the TIA that we designed is shown in **Fig. 5**. Photocurrent from the PDs is fed into the TIA's input differential terminals IT and IC. Then, the signal is amplified by the following circuit blocks: TIA core, post amplifier, variable gain amplifier (VGA), high-gain broadband amplifier (HGBA), and output buffer. Finally, differential output with a constant voltage amplitude is launched from output terminals OT and OC. To make the output voltage amplitude constant in the whole range of input current, a peak detector and an auto gain control (AGC) circuit are monolithically integrated in the TIA. The peak detector and the AGC circuit compare the real output voltage amplitude of the HGBA with a target



OB: output buffer
OMC & OMT: terminals for connection to external capacitance
PA: post amplifier

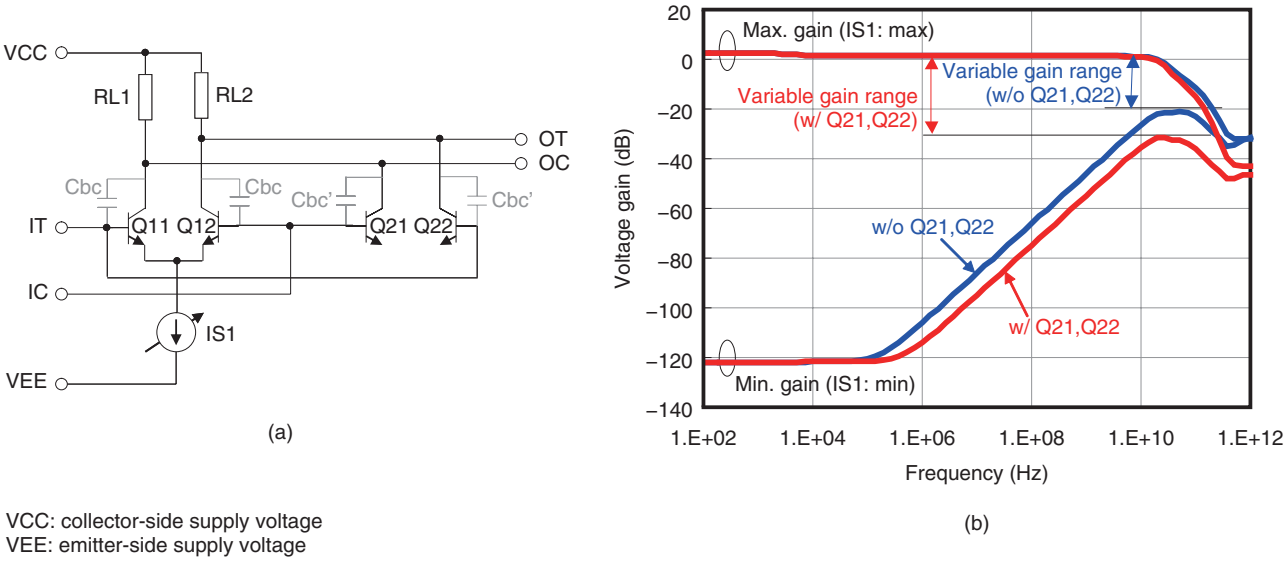
Fig. 5. Circuit diagram of the TIA.

amplitude provided through terminal THC, and they control the gain of the VGA so that the output voltage amplitude of the HGBA is equal to the target one. In this way, a function for achieving constant output voltage amplitude is implemented in the TIA. The TIA also contains an automatic offset canceling (AOC) circuit. The AOC circuit excludes DC voltage offset inside the TIA and ensures that high-speed signals are sufficiently amplified. The power supply voltage for the TIA is -5.2 V, and power consumption of one TIA is 660 mW (2.64 W for all four).

To make the output voltage amplitude constant over the whole range of input current, the VGA gain is controlled by the AGC circuit. Therefore, a variable range of VGA gain is also a key specification for keeping the output voltage amplitude constant, and it should be large enough to correspond to a wide input current range. The circuit configuration of the VGA is shown in **Fig. 6(a)**. The VGA gain is varied by changing current IS1: the gain increases (decreases) with increasing (decreasing) IS1. The simulated frequency-gain characteristics of the VGA for minimum and maximum current IS1 are shown in **Fig 6(b)**. While a large variable range of the gain is achieved at low frequencies, the range is reduced in the high-frequency region because of the increase in minimum gain. This is mainly due to the base-collector capacitances (Cbc) of transistors Q11 and Q12 (Fig. 6(a)), which bypass the high-frequency signal from input to output. To suppress the increase in minimum gain due to Cbc, we added transistors Q21 and Q22 to the VGA. In the circuit configuration in Fig. 6(a), the base-collector capacitances (Cbc') of Q21 and Q22 cancel Cbc and suppress the increase in minimum gain. As a result, the variable range of the gain is widened by about 10 dB in the high-frequency region.

The frequency response of transimpedance gain for a fabricated TIA is shown in **Fig. 7**. Transimpedance gain at low frequency is 68 dBΩ (2510 Ω), and the -3-dB-down frequency is 23 GHz, which exceeds the value required for 100-Gbit/s systems (22 GHz).

The input current dependence of the differential output voltage amplitude for the fabricated TIA is shown in **Fig. 8**. Constant output voltage amplitude of 540 mVppd (ppd: peak-to-peak, differential) was confirmed for a wide input current range from 160 μApp to 2.6 mApp. This result shows that the integrated peak detector and AGC circuit successfully controlled the output amplitude to keep it constant. Furthermore, the variable range of the VGA gain was sufficient to keep a constant output amplitude. The inset of Fig. 8 shows a 32-Gbaud output eye-pattern for 260-μApp input. A clear output eye-pattern was observed for the 32-Gbaud input, which is close to the baud rate for practical 100-Gbit/s systems (31.4 Gbaud).



VCC: collector-side supply voltage
VEE: emitter-side supply voltage

Fig. 6. (a) Circuit configuration of VGA and (b) frequency-gain characteristics of VGA (simulated).

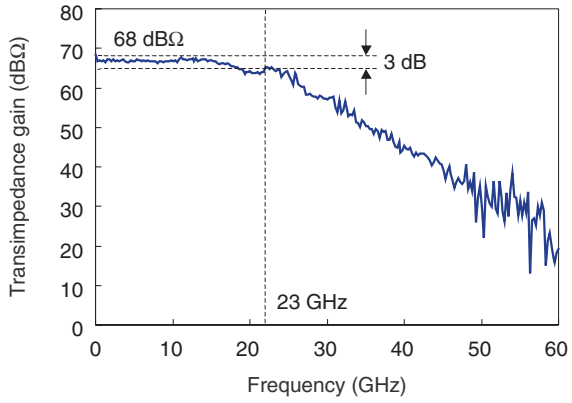


Fig. 7. Frequency response of transimpedance gain for the fabricated TIA.

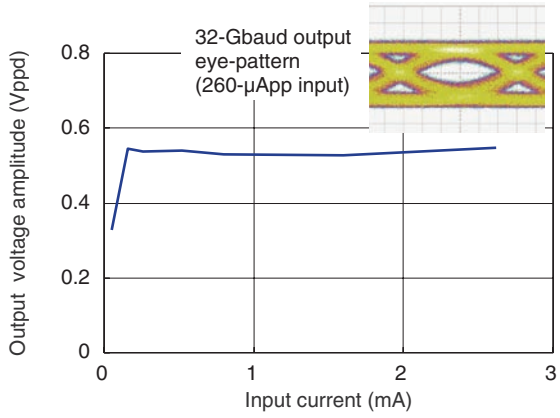


Fig. 8. Input current dependence of differential output voltage amplitude for the fabricated TIA.

4. Conclusion

We described high-speed photodiodes and transimpedance amplifiers for 100-Gbit/s digital coherent optical communications systems. For the photodiodes, we have newly devised composite-field maximized-induced-current photodiodes and confirmed their good high-frequency responses under high optical input power conditions, which are the characteristics required for 100-Gbit/s systems. We designed and fabricated the transimpedance amplifiers using InP HBTs with a 1-μm-wide emitter and confirmed a broad bandwidth of over 22 GHz and constant output amplitude in a wide input current range. These characteristics are indispensable for 100-Gbit/s systems.

In the future, we will research and develop photodiodes that can handle much higher optical input power and transimpedance amplifiers that can keep a constant output amplitude in wider input current ranges.

Acknowledgment

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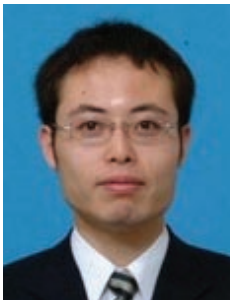

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Antenna Model and Its Application to System Design in the Millimeter-wave Wireless Personal Area Networks Standard

Ichihiko Toyoda† *and Tomohiro Seki*

Abstract

This article describes an antenna model developed for the system design and standardization of millimeter-wave wireless personal area networks (WPANs). It also discusses why a new antenna model is required for standardization activities. The developed antenna model is a simple mathematical analog. It provides a main-lobe pattern and averaged side-lobe level by setting the antenna's half-power beamwidth. This model was adopted as a reference antenna model in the channel model document of the IEEE 802.15.3c millimeter-wave WPAN task group.

1. Introduction

Wireless systems, such as cell phones, wireless local area networks, and wireless personal area networks (WPANs), have come to be widely used in our lives. These systems will also play an important role in future home networks. On the other hand, with the rapid progress of information and communications technologies, including high-performance personal computers (PCs) and high-speed Internet access lines like fiber to the home, the data sets being handled by consumers, such as video and music files, are drastically increasing in size year by year. Therefore, wireless systems are being pressured to support high-speed data transmission with gigabit-per-second-class data rates. One practical way to achieve such high-speed wireless systems is to allocate and use the huge bandwidth available in the millimeter-wave band. When these systems are used in home networks, technology standards are required because home networks consist of devices provided by many vendors.

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This article focuses on an antenna model developed for the standardization of millimeter-wave WPANs and discusses why a new antenna model had to be developed. The antenna model is a simple mathematical analog and provides a main-lobe pattern and averaged side-lobe level by setting the antenna's half-power beamwidth. It enables comprehensive system design by considering signals arriving from all directions including behind the antenna.

2. WPANs

WPANs are consumer-oriented short-range wireless communication systems linking personal devices. They were originally developed as low-rate communication systems for connecting a mouse and/or keyboard to a personal computer, a car navigation system to a cell phone, and a music player to a set of headphones. They were found to be a very cost effective way of linking devices. Two widely used WPAN technologies are Bluetooth and ZigBee.

A very wide frequency band near 60 GHz has been or will be allocated as an unlicensed band in many countries. Examples are 59–66 GHz in Japan, 57–64 GHz in the USA, Canada, and Korea, and 57–66 GHz

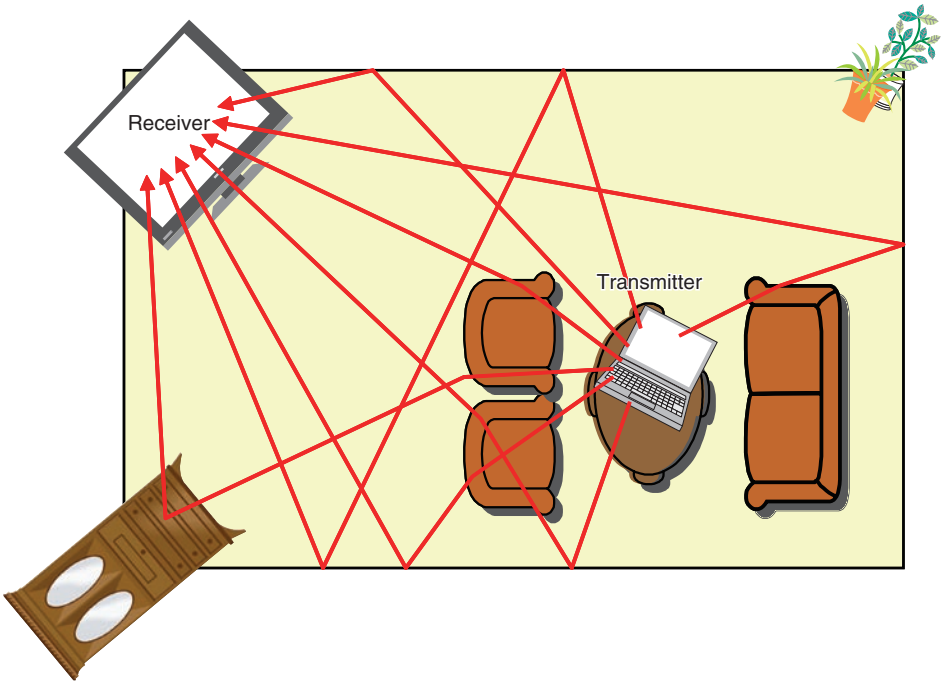


Fig. 1. Typical WPAN usage.

in European countries and Australia. This band is a good candidate for achieving ultrafast WPAN systems suitable for future home networks. To take advantage of the broad unlicensed bandwidth in the 60-GHz band, several standardization activities are focusing on developing standards for this band [1]. The 60-GHz-band WPAN system is promising for supporting uncompressed high-definition video streaming and ultrafast downloading of huge files from a server, namely *kiosk file downloading*.

3. Propagation channels of millimeter-wave WPANs

All wireless systems use radio waves that propagate through the air. The radio waves are reflected by walls and diffracted by obstacles. As a result, the receiver captures scattered signals that arrive from many directions with different time offsets. This propagation environment yields the *propagation channel* or simply *channel*. The propagation channel strongly affects system performance. Hence, accurate modeling of it is important in designing new wireless systems.

A typical example of WPAN usage is schematically shown in **Fig. 1**. A transmitter and receiver are located in a small room. The sofa, chairs, table, and cabinet act as obstacles. Signals from the transmitter are reflected and diffracted by the walls and obstacles. They arrive at the receiver from different directions with different time offsets. In this multipath environment, the delayed signals can improve the system performance as well as degrading it. In a typical standardization process, several systems are proposed, and their performances are evaluated and compared in order to narrow down the proposals to only one. In this process, each proposer must use the same channel model so that comparisons are correct and fair. Therefore, standardization task groups for wireless systems must define the channel model before calling for proposals.

For millimeter-wave WPAN system construction, one must use a directional antenna because of the high propagation loss of millimeter-wave signals and their low transmission power, which is strictly limited by law. The signal power received by the directional antenna is strongly influenced by its antenna pattern and is a significant determiner of system performance. Thus, WPAN system design requires antenna pattern evaluation as well as a channel model.

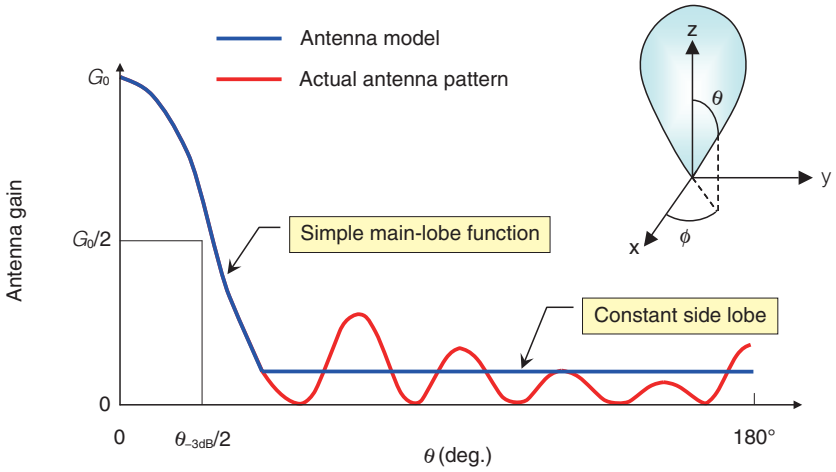


Fig. 2. Basic concept of the antenna model.

4. Antenna model for millimeter-wave WPAN system design

Beside the regulatory constraints, design goals such as low power consumption also dictate low transmission power for WPAN systems. Since millimeter-wave signals have high propagation loss, the use of a directional antenna is essential. As described in section 3, WPAN systems are usually used in multipath environments, so a system design must consider signals arriving from outside the antenna's main lobe. The requirements of the antenna model used for WPAN system design are summarized as follows:

(1) Model antennas with half-power beamwidths of 15–60°, which are common in WPAN systems.
(2) Include side-lobe effects.
(3) Cover antenna patterns defined over 360°.
(4) Provide a simple mathematical model that simplifies system simulation.

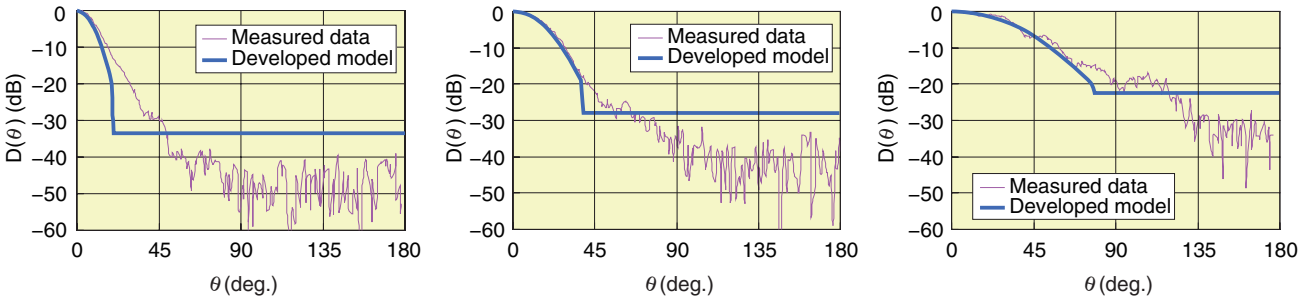
Among these requirements, (2) and (3) are unique to WPAN systems because of their use in multipath environments.

Many antenna models have been developed and used for the design and evaluation of various wireless systems [2], [3]. Here, we introduce a new antenna model suitable for WPAN system design. The basic concept is shown in **Fig. 2**. The red line shows the antenna pattern of a typical directional antenna. The blue line shows the antenna pattern of the design model. The horizontal axis plots the angular offset from the direction of antenna peak gain and the vertical axis plots antenna gain. As shown in this figure, the design model has a constant side-lobe level. Actual performance of a designed wireless system depends on room size, room shape, locations and number of obstacles, and transmitter and receiver locations. Hence, system design is performed for several typical cases using statistical channel models [4]. The channel model is created from measured data in some environments and is used to statistically generate signals arriving at the receiver. That is, the generated signals are not exactly identical to real signals. This means that exact side-lobe patterns are unimportant and the averaged side-lobe level is more practical for this application even though the actual antennas do not have constant side lobes.

There are two ways to determine the side-lobe level. One way is to consider practical applications. For example, in the case of interference assessments, the design side-lobe level is set a little bit higher than the actual side-lobe level. This provides conservative results for interference analyses. However, the antenna model described in this article is intended for new systems that include PHY/MAC (physical layer, medium access control) specifications. Thus, using this conservative approach may cause significant error because the side-lobe effects depend on the specifications. The other way of determining the side-lobe level is to derive it from physical requirements, i.e., the conservation of energy law.

We averaged the power outside the main lobe to obtain a side-lobe level that satisfies the physical requirements. The averaged side-lobe level G_{sl} can be expressed as

$$G_{sl} = \frac{4\pi - G_0 \int_0^{\theta_{ml}/2} \int_0^{2\pi} D(\theta, \phi) \bullet \sin\theta d\phi d\theta}{\int_{\theta_{ml}/2}^{\pi} \int_0^{2\pi} \sin\theta d\phi d\theta}, \quad (1)$$



(a) $\theta_{-3dB} = 15°$ (b) $\theta_{-3dB} = 30°$ (c) $\theta_{-3dB} = 60°$

Fig. 3. Comparison of calculated and measured antenna patterns.

where G_0, $D(\theta, \phi)$, and θ_{ml} are the peak gain, directivity function normalized by the peak gain, and main-lobe angular width, respectively, and θ and ϕ are polar coordinates. The second term of the numerator is the total power included in the main lobe. The denominator is the integration over the solid angle outside the main lobe. This expression ensures that the total radiated power i.e., the integration of the antenna pattern, is kept at 4π.

To calculate this equation, we must determine G_0, $D(\theta, \phi)$, and θ_{ml}. Our approach uses, as the directivity function of the main lobe, a Gaussian function of only θ owing to its simplicity. This means that the modeled antenna has a rotationally symmetric beam. G_0 is calculated from the theoretical response of the circular aperture antenna, which has a similar main-lobe pattern to the Gaussian beam antenna. θ_{ml} is determined by the angle at which the main-lobe function decreases by -20 dB from its peak.

Equation (1) is not easy to calculate in a system simulation because its integration is difficult to solve analytically. Our solution is to derive an approximate expression using the results of a numerical integration.

The developed antenna model is formulated in terms of directivity gain $G(\theta, \phi)$ as follows: [5]

$$G(\theta,\phi)[\text{dBi}]=G_0 -3.01\bullet\left(\frac{2\theta}{\theta_{3dB}}\right)^2 \quad 0 \le\theta\le\theta_{ml}/2 \qquad (2)$$

$$G(\theta,\phi)[\text{dBi}]=-0.411\bullet\ln(\theta_{3dB})-10.6 \quad \theta_{ml}/2<\theta\le 180^{\circ} \qquad (3)$$

$$\theta_{ml} = 2.58 \bullet \theta_{3dB} \qquad (4)$$

$$G_0=20 \bullet \log\left(\frac{1.62}{\sin(\theta_{3dB}/2)}\right), \qquad (5)$$

where θ_{3dB} is the antenna's half-power beamwidth and θ_{3dB} is in units of degrees. Equations (2) and (3) give the directivity gains of the main and side lobes, respectively. Here, the directivity gain is not a function of ϕ, which means that the antenna has a rotationally symmetric beam.

Antenna patterns calculated using the design model and measured patterns for rectangular horn antennas are shown in **Fig. 3**. As shown in this figure, the main-lobe patterns of the design model agree well with the measured ones. The side-lobe levels of the model are constant and well approximate the average values of the measured patterns. Thus, the antenna model is effective in millimeter-wave WPAN system design.

5. Conclusion

This article elucidated the role of antenna models in millimeter-wave WPAN standardization. Antenna patterns along with channel models must be considered in order to achieve fair and correct assessment of new wireless systems that use directional antennas because WPAN systems are commonly used in multipath environments where signals come from many directions. The antenna model described in this article is a simple mathematical analog with constant side-lobe level that reflects the average value. This feature is suitable for designing millimeter-wave WPAN systems. The antenna model has been adopted as a reference antenna model in the channel model document of the IEEE 802.15.3c millimeter-wave WPAN task group [6].

Acknowledgment

This work was conducted as part of the discussions

in the antenna working group of the Consortium for Millimeter Wave Practical Applications (CoMPA). We thank all of the CoMPA members for their comments.

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Compressed Sensing Technology for Flexible Wireless System

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Abstract

We are developing a flexible wireless system (FWS) in response to the rapid development of and changes to wireless radio environments. FWS is a unified wireless platform that simultaneously receives various types of wireless signals at distributed remote stations and performs signal processing at the central station by transferring the received radio wave data via the wired access line. As a partial fulfillment of our system, we have applied compressed sensing technology as a radio wave data compression technology for FWS. Compressed sensing is a new framework for solving an ill-posed inverse problem of a sparse signal. Direct translation of compressed sensing in the sense of wireless technology is as follows: radio wave data can be received, transmitted, and reconstructed using sub-Nyquist rate information without aliasing if the original radio wave is sparse. To provide a full understanding of our approach, this article first reviews basic knowledge about compressed sensing and then describes the application scenario of compressed sensing in FWS.

1. Introduction

The rapid development of and changes to wireless radio environments require a unified platform that can flexibly deal with various wireless radio systems [1]. To satisfy this requirement, we are developing a flexible wireless system (FWS), which is composed of flexible access points and a flexible signal processing unit [2].

The concept of FWS is illustrated in **Fig. 1**. Multiple wireless signals are simultaneously received by flexible access points, which can receive a wide variety of wireless signals with frequencies ranging from several hundred megahertz to several gigahertz. The received radio wave data is transferred to the flexible signal processing unit through a broadband wired access line. The flexible signal processing unit performs multiple types of signal analysis by software exploiting software defined radio and cognitive radio technologies [3]. If necessary, previously stored data at servers can also be used.

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The huge bandwidth necessity for transferring the received radio wave data motivated us to develop a highly flexible and efficient radio wave data compression technology. To accomplish this goal, we applied recently developed compressed sensing technology.

Compressed sensing is a new framework for solving an ill-posed inverse problem of a sparse signal [4]. Direct translation of compressed sensing in the sense of wireless technology is as follows: radio wave data can be received, transmitted, and reconstructed using sub-Nyquist rate information without aliasing if the original radio wave is sparse.

In relation to FWS, compressed sensing has two advantages. First, it provides universality in wireless signal reception regardless of system types. This provides flexible signal reception because all types of signals can be received by a unified signal reception method. Furthermore, no modifications are necessary even when new wireless systems are introduced. Second, it enables signal reception and reconstruction at a lower rate than the Nyquist rate. This reduces the burden of data transfer between flexible access points and the flexible signal processing unit.

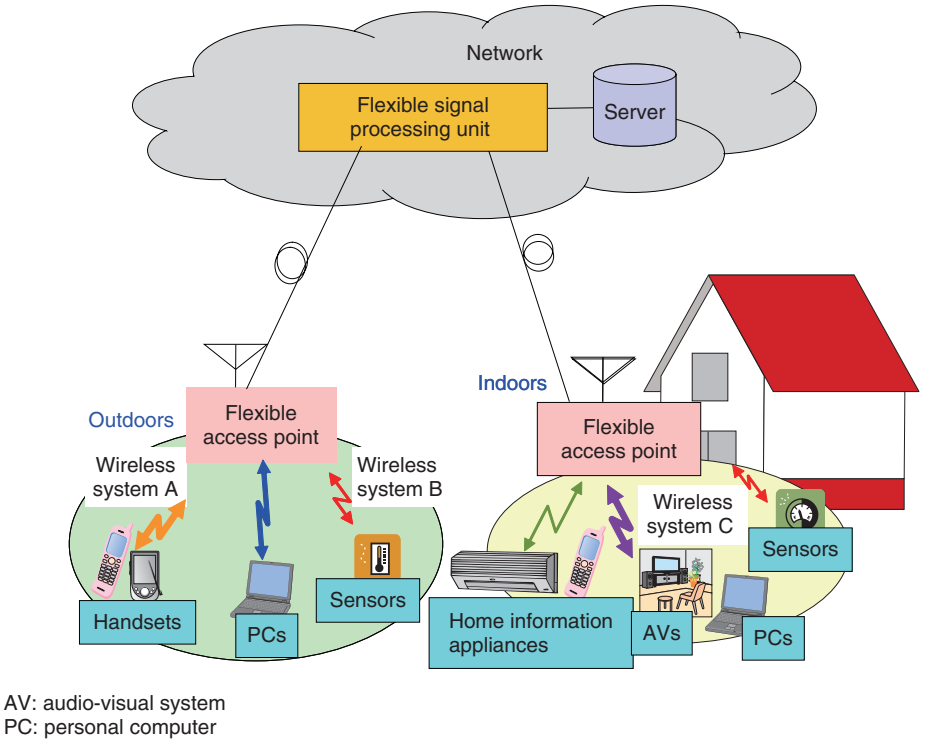

Fig. 1. Concept of a flexible wireless system.

The remainder of this article is organized as follows: Section 2 reviews basic knowledge about compressed sensing, section 3 describes our compression method, and section 4 concludes with a brief summary of the main points and a mention of future work.

2. Compressed sensing

2.1 Basic concept

A simplified explanation of compressed sensing is as follows: A signal projected linearly onto a lower-dimensional space can be used to reconstruct the original higher-dimensional signal with high probability if the signal is sparse (explained in section 2.2) and the projection matrix satisfies the restricted isometry property (RIP, explained in section 2.4).

In a mathematical sense, compressed sensing can be stated as an ill-posed inverse problem. Normally, the solution of an ill-posed inverse problem is not uniquely determined because the number of equations is smaller than the number of variables. However, the solution of an ill-posed inverse problem can be uniquely determined by investigating all possible cases provided that the signal is sparse. Moreover, if an ill-posed inverse problem satisfies RIP and the signal is sparse, the unique solution can be found with a practical degree of complexity.

For an intuitive understanding of compressed sensing, consider the following simple ill-posed inverse problem.

Find m, n, and k such that
$m + 3n - 2k = 1$
$-m - n + k = -1$

Normally, the solution is not uniquely determined because the number of equations is smaller than the number of variables. However, if vector $[m\ k\ n]$ has only one nonzero element, the unique solution can be obtained by investigating all possible cases, as below.

case 1) $m \neq 0,\ n=k=0$ -> $m=1$ (unique solution)
case 2) $n \neq 0,\ m=k=0$ -> impossible
case 3) $k \neq 0,\ m=n=0$ -> impossible

Although the unique solution is available, this is an NP-hard problem for which all possible cases must be investigated. Consequently, it becomes impractical as

the number of dimensions of the signal increases.

This impracticality is overcome if the equation vector [1 3 -2; -1 -1 1] satisfies RIP. The core achievement of compressed sensing is that the above NP-hard problem can be cast into an l1-norm minimization problem (explained in section 2.5) if the signal is sparse and RIP is satisfied. L1-norm minimization problems can be solved by linear programming, which is a well established convex optimization method, with practical complexity $O(n^3)$ [5], [6].

Considering the above example, the following two statements can be made: First the sparsity of the signal assures the unique solution for compressed sensing. Second, RIP assures a practical degree of complexity for finding the unique solution for compressed sensing.

2.2 Sparse signal

A signal is called sparse when it is represented by a small number of nonzero coefficients in any convenient domain. More specifically, $N\times1$ signal $\mathbf{X}$ is called S-sparse if $\mathbf{X}$ is represented by the multiplication of any $N\times N$ transform matrix $\mathbf{\Psi}$ and $N\times1$ coefficient vector $\mathbf{s}$, and $\mathbf{s}$ has only S nonzero coefficients. The definition of sparsity is not limited to the orthogonal transform domain (i.e., Fourier transform or wavelet transform). If a signal is represented in a non-orthogonal domain, including any user-defined domain, the signal is also called sparse [7].

2.3 Measurement

For a given $N\times1$ signal $\mathbf{X}$, measurement is defined as the linear projection of $\mathbf{X}$ onto $M\times1$ signal $\mathbf{Y}$. The $M\times N$ matrix $\mathbf{\Phi}$ that casts $\mathbf{X}$ onto $\mathbf{Y}$ is called the measurement matrix. Matrix description is given by $\mathbf{Y}=\mathbf{\Phi X}$. If $\mathbf{X}$ is represented by $N\times1$ coefficient vector $\mathbf{s}$ in the $N\times N$ transform domain Ψ , it is expressed as $\mathbf{Y}=\mathbf{\Phi\Psi s}$.

The number of measurements is the number of rows in the measurement matrix (M), which is also equivalent to the number of dimensions of the output signal. Therefore, the compression rate increases as the number of measurements increases. Numerous studies have been performed to investigate the minimum bound of the necessary number of measurements for a given signal sparsity [8 and references therein]. It has been shown that $S\bullet\log(N/S)$ measurements are enough for the reconstruction of an S-sparse signal when measurement matrix $\mathbf{\Phi}$ consists of random ensembles [9].

2.4 RIP

The most outstanding achievement of compressed sensing is the fact that RIP casts an NP-hard problem onto an l1-norm minimization method [10], [11].

When an $M\times N$ measurement matrix $\mathbf{\Phi}$ and a $N\times N$ transform domain matrix $\mathbf{\Psi}$ satisfy the following inequality for all S-sparse vectors, matrix $\mathbf{\Theta}(=\mathbf{\Phi\Psi})$ is said to obey RIP of order S with δ.

$$(1-\delta)\|\mathbf{s}\|_2^2\le\|\mathbf{\Phi\Psi s}\|\le(1+\delta)\|\mathbf{s}\|_2^2$$

where $\|\boldsymbol{s}\|_2=\Sigma_i s_i^2$ and $\delta(0\le\delta<1)$ is the smallest constant that satisfies the above inequality.

An intuitive explanation of RIP is as follows: the Euclidian distance between any two $N\times1$ S-sparse vectors is approximately preserved after the measurement as long as $\mathbf{\Theta}$ obeys RIP.

It has been proven that RIP is satisfied if measurement matrix $\mathbf{\Phi}$ consists of random ensembles, which yields the following surprising result: any unknown sparse signals can be reconstructed by random measurement [10]. This property provides flexibility for the compression of an unknown signal because signal-independent measurement is possible by the random measurement as long as the signal is sparse.

2.5 Reconstruction

Reconstruction of the compressed sensing refers to finding $N\times1$ S-sparse vector $\mathbf{s}$ from known $M\times1$ measurement output matrix $\mathbf{Y}$, $M\times N$ measurement matrix $\mathbf{\Phi}$, and $N\times N$ transform matrix $\mathbf{\Psi}$ when $\mathbf{Y}=\mathbf{\Phi\Psi s}$ (S<M<<N). Reconstruction of the original signal $\mathbf{s}$ can be found via the l1-norm minimization problem, as described below, as long as RIP is satisfied.

$$\min\|\hat{\mathbf{s}}\|_1 \text{ subject to } \mathrm{Y}=\mathbf{\Phi\Psi}\hat{\mathbf{s}},\ \hat{\mathbf{s}}\in\mathbf{R}^{\mathrm{N}},$$

$$\text{if RIP satisfies } \hat{\mathbf{s}}=\mathbf{s},$$

where $\|\hat{\mathbf{s}}\|_1=|s_1|+|s_2|+\cdots|s_N|$ and $\mathbf{R}^{\mathrm{N}}$ is the set of $N\times1$ vector.

The l1-norm minimization problem finds $\hat{\mathbf{s}}$ that minimizes the l1-norm subject to $\mathbf{Y}=\mathbf{\Phi\Psi}\hat{\mathbf{s}}$ among all possible S-sparse vectors. This seems to be an NP-hard problem, but it can be cast into a convex optimization problem and solved by the linear programming method. Furthermore, if RIP is satisfied, $\hat{\mathbf{s}}$ is identical to the original vector $\mathbf{s}$ with high probability [10], [11].

If the measurement matrix consists of random ensembles, flexible reconstruction is possible. In the case that signal $\mathbf{X}$ is proved to be more sparsely

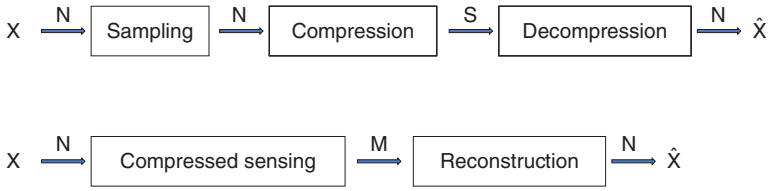

Fig. 2. Comparison between conventional compression and compressed sensing.

represented in another basis matrix Ψ', surprisingly, one does not need to conduct the measurement again since the l1-norm minimization problem can be solved with $\mathbf{Y}$ and a new Θ'(=$\Phi\Psi$'). This indicates that once the projection has been performed, the reconstruction can be performed with any convenient basis matrix.

There are other approaches to the reconstruction of compressed sensing such as an orthogonal matching pursuit algorithm, which uses a greedy iterative algorithm [12].

2.6 Comparison between conventional compression and compressed sensing

The difference between the conventional compression and compressed sensing is shown in **Fig. 2**. The conventional sample-then-compress method compresses the signal by the signal-specific compression method, which yields the optimal compression (S dimensions). On the other hand, compressed sensing conducts a signal-independent linear projection of the original signal onto a lower-dimensional space (M-dimensional, S<M<<N), which yields poor compression performance. Therefore, it can be stated that the conventional compression method is superior to compressed sensing for the known signals in terms of compression performance.

However, compressed sensing has the following advantages compared with the conventional compression method. First, it is suitable for dealing with an unknown sparse signal. Second, it is robust to the introduction of new types of wireless systems. When new types of wireless systems are introduced, receivers (flexible access points in Fig. 1) do not need to be modified because the signal-specific processing burden is moved from the receivers to the server (flexible signal processing unit in Fig. 1). Third, it reduces the burden on receivers. For example, consider a sparse signal of unknown frequency. In the case of the conventional sampling method, receivers must conduct both a fast Fourier transform and a search for nonzero coefficients. On the other hand, in the case of compressed sensing, receivers only need to conduct a linear projection.

3. Application of compressed sensing for FWS

This section describes two radio wave data compression methods that utilize compressed sensing. Both methods try to exploit the flexibility of compressed sensing by utilizing prior information. One method uses a random sparse measurement matrix based on random sampling [13] (or equivalently, random discard from all of the sampled data). The other uses a random dense measurement matrix that conducts a full linear projection of sampled data [14].

3.1 Combined Nyquist and compressed sampling

The goal of this sampling method is to achieve Nyquist-rate sampling of the known signal (hereinafter called the decoding signal) and compressed-rate sampling of the unknown signal (hereinafter called the sensing signal) in a single analog-to-digital converter. To achieve this goal, the following processes are carried out.

At each flexible access point, multiple signals are simultaneously received, filtered, and down-converted to the intermediate frequency (IF) band. In particular, decoding signals are converted to a lower center frequency band than sensing signals, as shown in **Fig. 3**. Signal down-conversion is done by tunable local oscillators and mixers. All down-converted signals are sampled by our method and transferred to the flexible signal processing unit.

Details of the combined Nyquist and compressed sampling method are as follows. Suppose that L decoding signals and M sensing signals are aligned in the IF band, and the total bandwidths of these signals are represented by B_{dec} and B_{sens}, respectively. For the convenience of the explanation, B_{grid} and B_{Nyq} are defined as $(4B_{dec}+2B_{sens})$ and $(2B_{dec}+B_{sens})$, respectively. The purpose of the above setting is to achieve

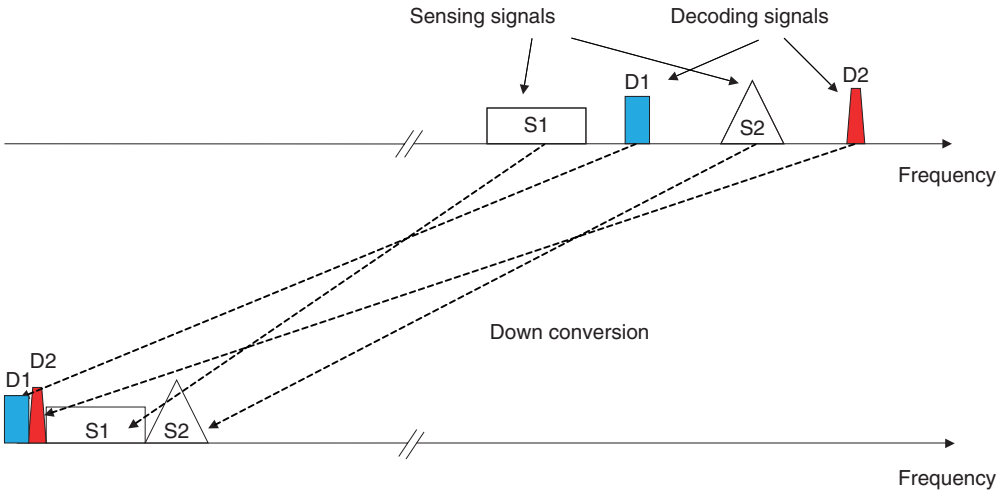

Fig. 3. Example of frequency alignment of multiple signals.

(1) Nyquist-rate sampling of the decoding signals without aliasing from the sensing signals and (2) compressed-rate sampling of the sensing signals in a single analog-to-digital converter simultaneously.

The detailed procedure of our method is as follows. First, B_{grid}-rate sampling is conducted. Second, only some of the even (odd) samples are randomly discarded while all of odd (even) samples are preserved. The locations of randomly discarded samples, which are determined by the random sequences generator, can be known to the flexible signal processing unit if the initial seed of the random sequence generator is shared. Hereinafter, all the odd samples and the remaining even samples are called fixed samples and random samples, respectively. They are transferred to the flexible signal processing unit via the wired access line.

The mathematical description of our method is as follows. For simplicity, we consider multiple sparse signals in the frequency domain. The IF band signal $\mathbf{X}=(\Psi\mathbf{s})$ is sparsely represented in the frequency domain. The basis matrix Ψ is an $N\times N$ inverse Fourier transform, and $\mathbf{s}$ is the $N\times 1$ coefficient vector of $\mathbf{X}$ in the frequency domain. Note that $\mathbf{s}$ has sequential nonzero values in the lower frequency region and randomly sparse nonzero values in the higher frequency region (e.g., s=[1111100100010001]). The $K\times N$ projection matrix Φ has the following sparse representation.

$$\Phi=\begin{bmatrix} 1&0&0&0&0&0&0&\cdots&0\\ 0&0&1&0&0&0&0&\cdots&0\\ 0&0&0&1&0&0&0&\cdots&0\\ 0&0&0&0&1&0&0&\cdots&0\\ 0&0&0&0&0&0&1&\cdots&0\\ \vdots&\vdots&\vdots&\vdots&\vdots&\vdots&\vdots&\ddots&\vdots\\ 0&0&0&0&0&0&0&\cdots&1 \end{bmatrix} \quad (3)$$

Note that each column indicates a sample point of the signal. Every odd sample is preserved while some of the even samples are randomly discarded.

Then, the compressed sensing matrix $\Theta(=\Phi\Psi)$ becomes a $K\times N$ matrix consisting of every odd row and randomly selected even rows of the inverse Fourier transform matrix. Projection vector $\mathbf{Y}$ is represented by $\Theta\mathbf{s}$ and signal reconstruction becomes the inverse problem of $\mathbf{s}=\Theta^{-1}\mathbf{Y}$. This inverse problem is solvable as an l1-norm minimization problem because $\mathbf{s}$ is sparse and Θ consists of randomly selected rows of the inverse Fourier transform matrix*.

Using transferred fixed and random samples from flexible access points, the flexible signal processing unit conducts the decoding and sensing process as follows.

First, the decoding signals are decoded using only fixed samples, which is equivalent to B_{Nyq}-rate sampling. Note that aliasing of the sensing signals occurs

* Compressed sensing theory has proved that randomly permutated Fourier ensembles satisfy RIP. Therefore, we can use randomly selected rows of an inverse Fourier transform matrix as a sensing matrix because Fourier ensembles and inverse Fourier ensembles have identical statistical characteristics.

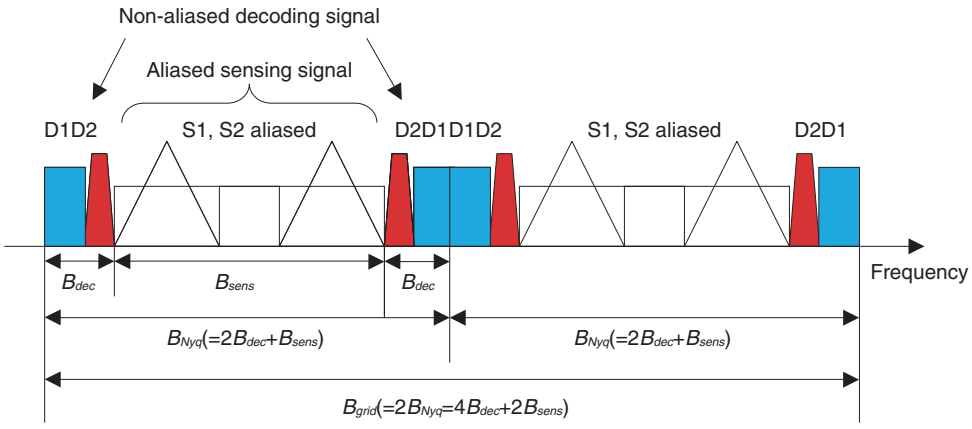

Fig. 4. Frequency domain representation of fixed samples.

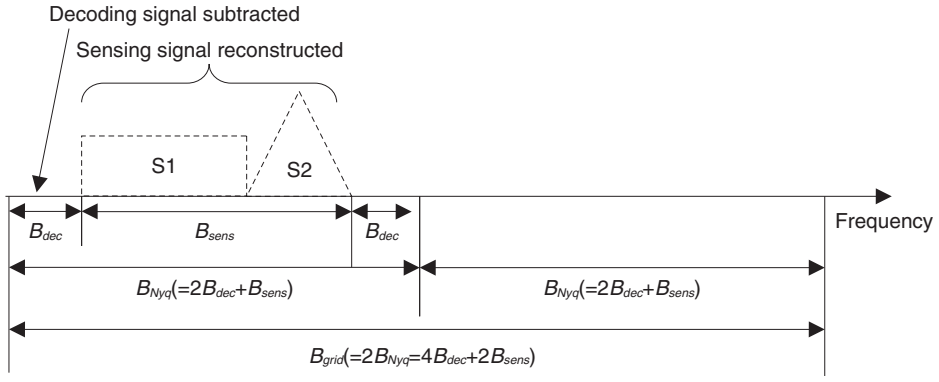

Fig. 5. Frequency domain representation of sensing signals reconstructed from fixed and random samples after subtraction of the decoding signal.

because the sampling rate is insufficient. However, it does not cause interference with the decoding signals. Therefore, the decoding signals can be decoded by using conventional decoding algorithms without aliasing. An example of fixed samples in the frequency domain is shown in **Fig. 4**. Although the aliasing of the sensing signals occurred owing to the insufficient sampling rate, the decoding signal parts are intact. Consequently, Nyquist-rate decoding performance is achieved for the decoding signals. Second, the decoding signal is subtracted from both the fixed and random samples. Third, the sensing signals are reconstructed using both fixed and random samples, whose decoding signals have been subtracted. The reconstruction is done by solving the l1-norm minimization problem. An example of the reconstructed signal in the frequency domain is shown in **Fig. 5**. Note that only sensing signals are reconstructed because the decoding signals have been removed. Fourth, the sensing signals are identified in the reconstructed signal by a conventional spectrum sensing algorithm such as energy detection.

Some experimental results are shown in **Figs. 6** and **7**. Experiments were performed on 310-MHz-band frequency shift keying (FSK) signals transmitted by radio frequency identification (RFID) tags. The RFID tag bandwidth and the total bandwidths of decoding signals and sensing signals were 0.3, 1.73, and 6.54 MHz, respectively. The channel between the RFID tags and a flexible access point was a non-fading additive white Gaussian noise channel.

Figure 6 compares the theoretical and experimental symbol error rates for the decoding signal in terms of Es/No (energy per symbol per noise power spectral

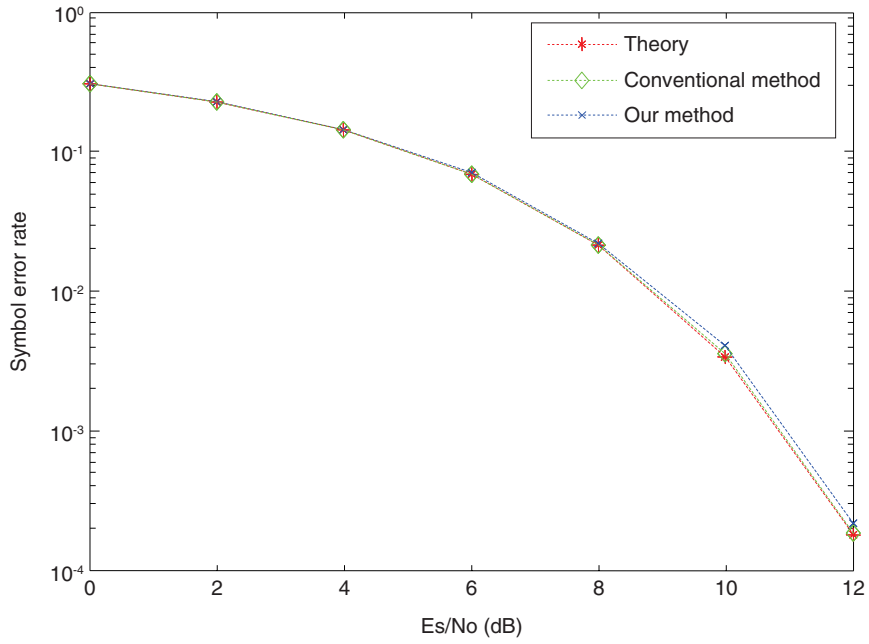

Fig. 6. Symbol error rate comparison.

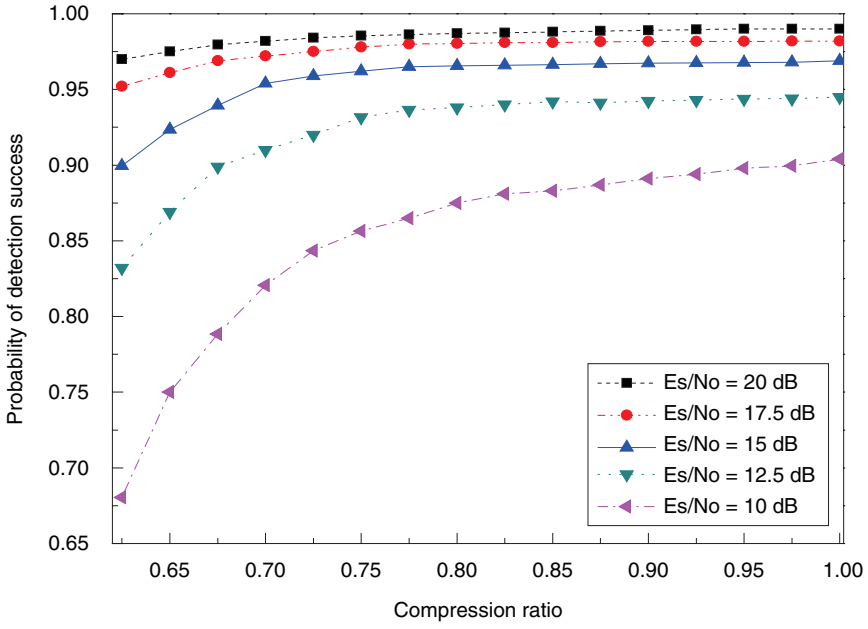

Fig. 7. Probability of detection success.

density). In the experiment using the conventional method, only the down-converted decoding signal was sampled at the Nyquist rate. In the experiment using our method, the decoding signal and the sensing signals were combined in the IF band and sampled by using our method. The performance curve for our method matches those for the theoretical and conventional methods well, which shows that our sampling

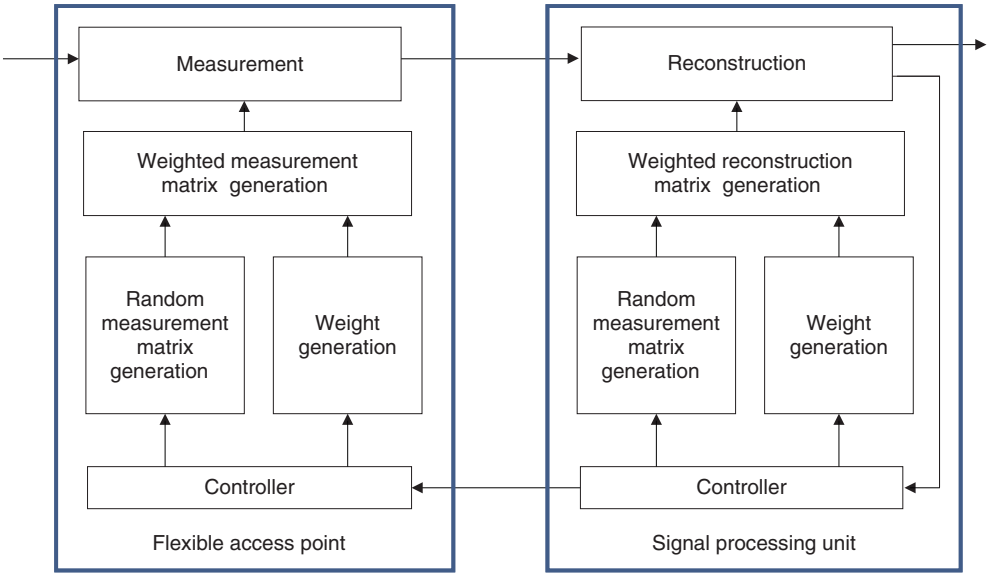

Fig. 8. Block diagram of compressed sensing with weighted measurement matrix generation.

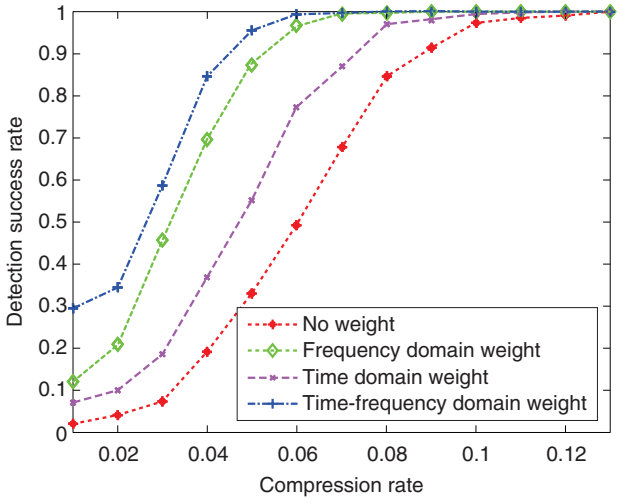

Fig. 9. Probability of detection success.

method guarantees Nyquist-rate decoding performance for the decoding signal.

The detection success rate is shown in Fig. 7. All curves show relatively poor performance at a low compression ratio. This is because reconstruction fails if the number of samples is insufficient. However, P_d (detection success rate) increases with the compression ratio. Approximately, 70% of the compression ratio can be achieved when E_s/N_o is higher than 17.5 dB.

3.2 Compressed sensing with weighted measurement matrix

Our goal for the weighted measurement matrix generation is to reduce the required number of measurements by using prior knowledge of the signal.

A block diagram of compressed sensing with weighted measurement matrix generation is shown in **Fig. 8**. The weighted measurement matrix is generated by multiplying the random measurement matrix and weight matrix, where the weight matrix is generated taking into consideration prior knowledge such as the signal's history. Note that identical weighted and random measurement matrices are generated by both the flexible access points and the signal processing unit for the reconstruction. If the weight needs to be updated, necessary parameters are transmitted from the signal processing unit to the flexible access points.

To verify the efficiency of this method, we conducted an experiment using an RFID signal consisting of a periodically transmitted FSK signal. The total bandwidth and the received signal bandwidth were 5 and 0.6 MHz, respectively. The time occupancy rate of the received signal was 0.25. Therefore, the time-frequency domain signal sparsity was 0.03. The time and frequency domain weights were set to 2.0 and 1.5 using the signal reception history. The detection success rates for the conventional method and our method are compared in **Fig. 9**. The compression rates needed for perfect signal detection were 0.13,

0.12, 0.09, and 0.08, respectively, when the applied weights were no weight, time domain weight, frequency domain weight, and time-frequency domain weight. These results confirm that enhanced compression is achieved by our method.

4. Conclusion

To satisfy the requirement for a unified wireless platform, we are developing a flexible wireless system. As a partial fulfillment of such as system, this article described a highly efficient radio wave data compression method based on currently developed compressed sensing technology. It also described two radio wave data compression methods utilizing compressed sensing technology. Experiments results verified that a compression rate that is slightly higher than the Nyquist rate of the original sparse signal can be achieved. Our future research will include developing further enhanced data compression methods in terms of realtime operation and practical processing burden using compressed sensing technology.

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Electromagnetic Compatibility Standardization Activities in the Telecommunication Field at the 2010 IEC/CISPR Seattle Meeting

Kimihiro Tajima†, *Yoshiharu Akiyama, Norihito Hirasawa, and Fujio Amemiya*

Abstract

This article summarizes recent electromagnetic compatibility (EMC) standardization activities in the telecommunication field at the 2010 IEC/CISPR Plenary Meeting held in Seattle, Washington, USA, from October 6 to October 14 and reports on the state of deliberations relevant to NTT's telecommunication business. As EMC standards are an important issue for the NTT Group, it defines EMC requirements for the provision of safe and secure telecommunication services.

1. Introduction

The NTT Group maintains in-house technical requirements (NTT-TRs) that set out the electromagnetic compatibility (EMC) quality levels to be adhered to when developing or procuring telecommunication equipment and devices. NTT-TRs stipulate EMC requirements (acceptable limits and measurement methods) to ensure safe and secure telecommunication services in terms of emissions (of electromagnetic disturbances), immunity (to electromagnetic disturbances), and overvoltage tolerance capability.

The acceptable EMC limits and measurement methods specified in NTT-TRs conform to international standards on information technology equipment (ITE) or telecommunication equipment set out by organizations such as IEC/CISPR (explained below) and ITU-T SG5 (International Telecommunication Union, Telecommunication Standardization Sector, Study Group 5) so that enterprises in related industrial sectors either in Japan or abroad can abide by the NTT-TRs.

This article summarizes events at the 2010 IEC/CISPR Plenary Meeting held in Seattle, Washington, USA, from October 6 to October 14, 2010. It provides an update to last year's article about the 2009 meeting [1].

2. Meeting overview

The Comité International Spécial des Perturbations Radioélectriques (CISPR)—also known as the International Special Committee on Radio Interference—is a special committee of the International Electrotechnical Commission (IEC). To ensure that there are consistent global standards, it issues international standards for the emission levels of unwanted electromagnetic disturbances from various devices (radio interference sources) as well as for the apparatus and methods used to measure such disturbances. The secretariat is located in Geneva, Switzerland.

CISPR membership includes 42 national committees and a number of related international organizations (International Council on Large Electric Systems (CIGRE), European Broadcasting Union (EBU), European Telecommunications Standards Institute

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(ETSI), International Amateur Radio Union (IARU), and International Telecommunication Union, Radiocommunication Sector (ITU-R)). CISPR standards function as Horizontal Standards within the IEC. They are used across all Technical Committees (TCs) and, as such, impact a wide range of industries.

CISPR comprises a Steering Committee and six subcommittees (A, B, D, F, H, and I) under the CISPR Plenary Assembly (**Fig. 1**). Each subcommittee is responsible for setting standards in its respective industrial field. Working Groups (WGs), set up to handle specific themes, meet throughout the year.

The 2010 IEC/CISPR Plenary Meeting was held at the Washington State Convention & Trade Center in Seattle and lasted for eight days. The Steering Committee, the six subcommittees, 14 WGs, and four joint task forces (JTFs) met in parallel with the Plenary Meeting. Japan sent 38 delegates representing the Ministry of Internal Affairs and Communications, the National Institute of Information and Communications Technology, universities, corporations, and industry groups. NTT sent four delegates. This year's IEC/CISPR Plenary Meeting was held alongside the 74th IEC General Meeting, creating a very large conference that attracted 2800 delegates to some 90 TC meetings over its two-week run (**Photos 1–4**).

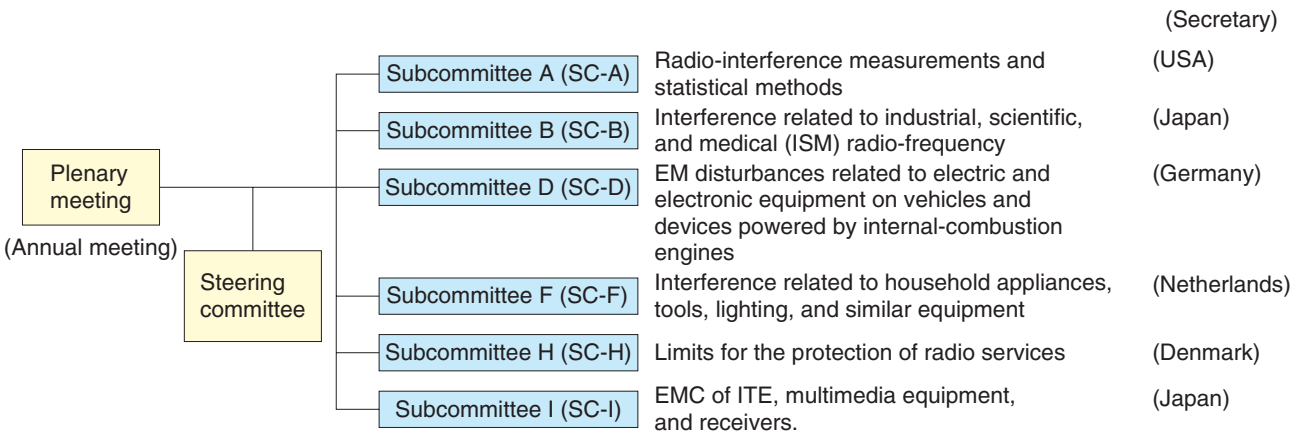

Fig. 1. IEC/CISPR organization.

Photo 1. Meeting place: Seattle Convention Center.

Photo 2. Meeting.

Photo 3. Opening ceremony party in IEC General Meeting.

Photo 4. Seattle Tower.

3. Impact of IEC/CISPR standardization on NTT's business

NTT Group's in-house EMC regulations include EMC standards for telecommunication equipment (in-house standards), which specify the minimum EMC requirements and operational methods for telecommunication equipment that NTT uses to provide telecommunication services as well as for telecommunication equipment provided to customers. NTT-TRs consist of technical requirements taken from the in-house standards (**Fig. 2**) [2]. Currently, there are three TR documents: "Technical requirements for electromagnetic disturbance emitted from telecommunications equipment (TR550004)", "Technical requirements for electromagnetic immunity of telecommunications equipment (TR549001)", and "Technical requirements for resistibility of telecommunications equipment to overvoltage and overcurrent (TR189001)". TR550004 covers electromagnetic disturbances generated by telecommunication equipment, TR549001 covers the capability of telecommunication equipment to tolerate electromagnetic disturbances, and TR189001 covers the capability of telecommunication equipment to tolerate overvoltage. Telecommunication equipment specifications cite these TRs as EMC requirements. The requirements in TR550004 are mandatory, while those in TR549001 and TR189001 are currently recommendations.

TR549001 [3] complies with CISPR 22 and, domestically, with the voluntary technical standards defined by the VCCI Council (VCCI). It also incorporates

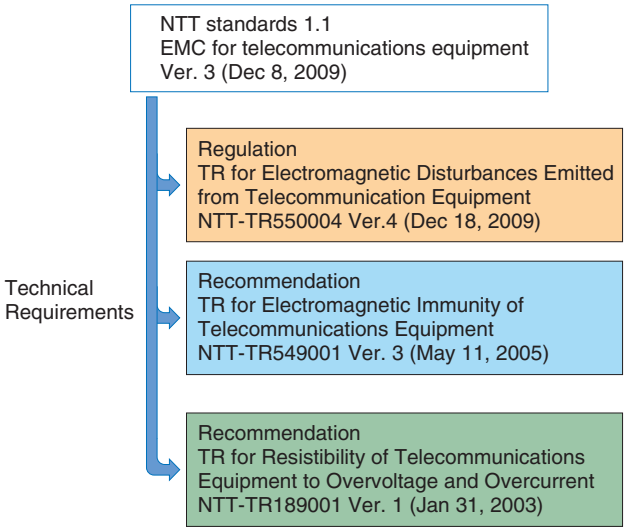

Fig. 2. NTT-TRs for EMC standards.

international standards from ITU-T and other bodies as requirements that apply to telecommunication equipment.

Since December 2009, we have been adding emission regulations for electromagnetic disturbances in the 1–6 GHz band in conjunction with amendments to international standards and domestic rulings (CISPR 22 edition 5.2) and have been adopting rules for conducted disturbances at telecommunication ports as related VCCI technical standards come into effect.

TR549001 [4] complies with CISPR 24 and domes-

tic rulings (the current CISPR committee of the Information and Communications Council). In Japan, CISPR 24 formerly operated as a guideline for each industry, but the Telecommunication Technology Committee (TTC) standardized it as JS-CISPR 24 Version 1 in August 2010 as a domestic standard for the telecommunication industry. We expect that, with the increasing prevalence of broadband services, more international standards and TRs associated with TTC standards will be established to cope with EMC failures in IP (Internet protocol) telecommunication equipment.

NTT TRs are publicly available from NTT's International Procurement web page [3], [4].

4. Main issues and discussion at the meeting

4.1 Subcommittee A

CISPR Subcommittee A is engaged in forming base international standards for radio disturbance measurement apparatus and methods. The subcommittee's main mission is preparing and revising the CISPR 16 series of standards that specify radio disturbance and immunity measurement apparatus and methods and are designated as *base* standards cited by all other CISPR standards.

At the Seattle meeting, NTT proposed a new impedance stabilization network (ISN) for measuring conducted disturbances at telecommunication ports to coincide with maintenance to CISPR 16-1-2 (Radio disturbance and immunity measuring apparatus—Ancillary equipment—Conducted disturbances). As a result of NTT's proposal, the inclusion of the ISN in CISPR 16 will be studied after discussions of its necessity in Subcommittee I, as described below.

4.2 Subcommittee I

Subcommittee I is involved in creating international standards regarding EMC of ITE, multimedia equipment, and receivers. This subcommittee prepares and revises emissions standards (CISPR 22 and CISPR 32) and immunity standards (CISPR 24 and CISPR 35) for telecommunication equipment. It is working on three issues that have a direct bearing on NTT's business.

(1) Emission and immunity standards for multimedia equipment
(2) Measurement methods of and limits on disturbances from high-speed power line telecommunication (PLT) equipment
(3) New ISN for measuring conducted disturbances at telecommunication ports

Issue (1) concerns the establishment of emission standards (CISPR 32) and immunity standards (CISPR 35) that target ITE and broadcast receivers. Since the functional barrier between them has disappeared, new standards that cover both categories are being drawn up. TR550004 (for emissions) and TR549001 (for immunity) are based on the existing CISPR 22 and CISPR 24 standards, but these TRs are expected to be replaced once CISPR 32 and CISPR 35 come into effect. The establishment of new standards that will govern NTT's required EMC performance in the future is therefore a highly relevant issue for NTT's business. At the present time, CISPR 32 and CISPR 35 inherit most of the existing provisions without modification, but CISPR 35 is set to add provisions for testing impulse noise effects on xDSL (various types of digital subscriber line) services. We envision CISPR 32 being issued at the earliest in one to two years and CISPR 35 being issued in two to three years.

Issue (2) concerns the addition to the existing CISPR 22 standard of measurement methods of and limits on disturbances from PLT equipment. This issue has been debated for more than ten years since 1999 but no agreement has been reached yet within CISPR. The Seattle meeting decided to shelve further official standardization investigation in this area. Disturbances from PLT equipment are already regulated in Japan under the Radio Act; therefore, the decision to stop standardization at CISPR has no direct effect on NTT's business. Nevertheless, the European Committee for Electrotechnical Standardization (CENELEC) is still pushing ahead with standardization: once a European EN standard has been established, we presume that it will be incorporated as a CISPR standard. The original goal of creating a CISPR standard for PLT equipment was to unify in an international standard the many PLT equipment disturbance standards operating in different countries and regions. Should an EN standard become a CISPR standard, it may prompt revisions to Japan's Radio Act. For this reason, we should continue to monitor developments in this area.

Issue (3) involves the inclusion in CISPR standards of NTT's newly developed ISN for measuring conducted disturbances at telecommunication ports. Conventional ISNs perform well with well-balanced*

* Balance in this context refers to the electrical balance in the ground plane. A poorly balanced ground plane can lead to communication signals being radiated as radio disturbance.

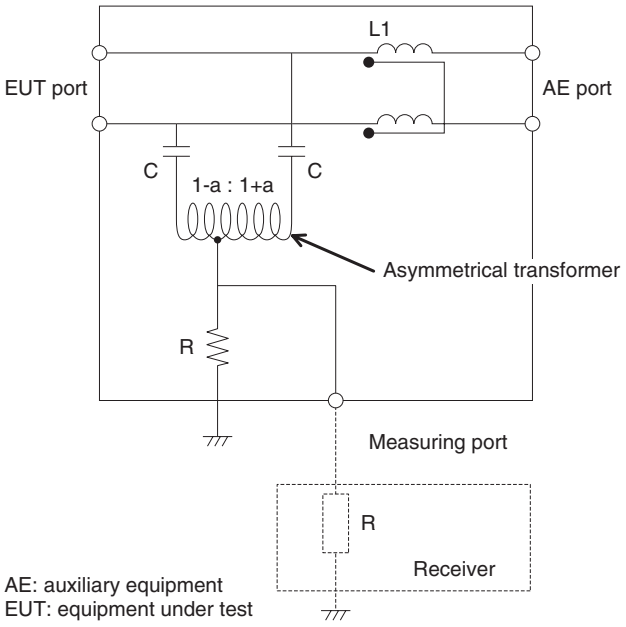

Fig. 3. Diagram of the asymmetric artificial network using an asymmetrical transformer.

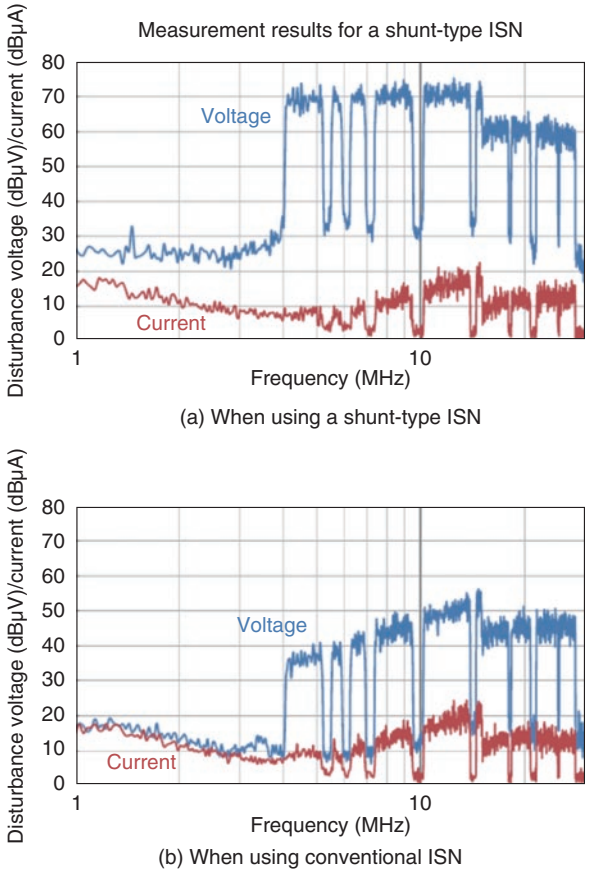

Fig. 4. Measurement results at the telecommunication ports.

telecommunication lines, such as Ethernet lines. The problem with conventional ISNs is that they produce measurement errors when measuring poorly balanced telecommunication lines. Now that NTT Energy and Environment Systems Laboratory has developed a new ISN that resolves this problem, NTT is pressing for its inclusion in CISPR standards. Because the new ISN can be used for more accurate assessments of and correspondence to disturbances from ordinary telecommunication lines and xDSL lines, this issue will impact NTT's business.

A schematic diagram of the proposed ISN, which uses an asymmetrical transformer, is shown in **Fig. 3**. The way the voltage-characteristic measurements of a transmission port are improved when a telecommunication device's electromagnetic disturbance is measured with the proposed measurement apparatus is shown in **Fig. 4** [5]. This example demonstrates that the proposed measurement apparatus, using an asymmetrical transformer circuit, can measure very poorly balanced transmission ports (20 dB or less) and that the voltage measurements obtained concur with the current characteristics.

4.3 State of discussions at JTFs and other venues

The JTF between CISPR subcommittees A and F (A&F JTF) is examining a simple alternative (CDNE method) for measuring radio-frequency disturbances from lighting equipment in the frequency range from 30 MHz to 300 MHz by a conducted disturbance measurement method that uses coupling decoupling networks (CDNs) for conducted immunity tests. Although this examination does not directly involve the measurement of electromagnetic disturbances in telecommunication equipment or systems, NTT Group experts are active in the discussions, as their direction needs to be monitored because any new standards will require lower transient noise and steady-state noise and lower energy consumption from lighting equipment used in machine rooms and datacenters. The committee draft on the CDNE method submitted just prior to the Seattle meeting was withdrawn because of too many technical deficiencies, according to a comment put forth by the NTT Group. Instead, the identified issues were discussed point by point. The CDNE method will be debated again in the A&F JTF after the committee draft has been revised in the light of the Seattle dis-

cussions. We feel that it is necessary to continue to watch the correlation between the CDNE method and conventional measurement methods performed in anechoic chambers.

5. Concluding remarks

This article described the relationship between NTT's EMC regulations and IEC/CISPR international standards, the main issues being debated within CISPR, and the direction of discussions at the Seattle Plenary Meeting. CISPR will continue to establish new standards and update existing standards to keep abreast of the various transformations in the electromagnetic environment, such as the convergence of telecommunication equipment and broadcasting equipment driven by broadband-service proliferation and the adoption of PLT and other new transmission methods caused by the move to intelligent power control.

Through participation in international EMC standardization processes and active promotion of in-house regulations, the NTT Group is committed to maintaining a good electromagnetic environment and providing high-quality, highly reliable telecommunication services.

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[5] N. Hirasawa, Y. Akiyama, and F. Amemiya, "Impedance Stabilization Networks by Using Asymmetrical Transformer for More Accurate Conducted Disturbances Measurement on Power Line," Proc. of EMC Europe 2010 Wroclaw, Poland.

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Papers Published in Technical Journals and Conference Proceedings

Escaped-Huffman and Adaptive Recursive Rice Coding for Lossless Compression of the Mapped Domain Linear Prediction Residual

N. Harada, Y. Kamamoto, and T. Moriya

Proc. of ICASSP 2010, IEEE, pp. 4646–4649, Dallas, Texas, USA.

ITU-T Recommendation G.711.0 has just been established. It defines a lossless and stateless compression for G.711 packet payloads (for both A-law and μ-law). This paper introduces some coding technologies proposed and applied to the G.711.0 codec, such as Plus-Minus zero mapping for the mapped domain linear predictive coding and escaped-Huffman coding combined with adaptive recursive Rice coding for lossless compression of the prediction residual. Performance test results for those coding tools are shown in comparison with the results for the conventional technology. The performance is measured on the basis of the figure of merit (FoM), which is a function of the trade-off between compression performance and computational complexity. The proposed tools improve the compression performance by 0.16% in total while keeping the computational complexity of the encoder/decoder pair low (about 1.0 WMOPS on average and 1.667 WMOPS in the worst case).

Emerging ITU-T Standard G.711.0—Lossless Compression of G.711 Pulse Code Modulation

N. Harada, Y. Kamamoto, T. Moriya, Y. Hiwasaki, M. A. Ramalho, L. Netsch, J. Stachurski, L. Miao, H. Taddei, and F. Qi

Proc. of ICASSP 2010, IEEE, pp. 4658–4661, Dallas, Texas, USA.

ITU-T Recommendation G.711 is the benchmark standard for narrowband telephony. It has been successful for many decades because of its proven voice quality, ubiquity, and utility. A new ITU-T recommendation, denoted G.711.0, has recently been established defining lossless compression for G.711 packet payloads typically found in IP networks. This paper presents a brief overview of technologies employed within the G.711.0 standard and summarizes the compression and complexity results. It is shown that G.711.0 provides greater than 50% average compression in typical service provider environments while keeping low computational complexity for the encoder/decoder pair (1.0 WMOPS average, <1.7 WMOPS worst case) and low memory footprint (about 5 k octets of RAM, 5.7 k octets of ROM, and 3.6 k of program memory measured in the number of basic operators).

Voice Activity Detection Using Frame-wise Model Re-estimation Method Based on Gaussian Pruning with Weight Normalization

M. Fujimoto, S. Watanabe, and T. Nakatani

Proc. of INTERSPEECH 2010, Makuhari, Chiba, Japan.

This paper proposes a frame-wise model re-estimation method based on Gaussian pruning with weight normalization for noise robust voice activity detection (VAD). Our previous work, switching-Kalman-filter-based VAD, sequentially estimates a non-stationary-noise Gaussian mixture model (GMM) and constructs GMMs of observed noisy speech signals by composing pre-trained silence and clean GMMs and sequentially estimated noise GMMs. However, the composed models are not optimal because they do not fully reflect the characteristics of the observed signal. Thus, to ensure the optimality of the composed models, we investigate a method for re-estimating the composed model. Since our VAD method works under frame-wise sequential processing, there are insufficient re-training data for re-estimation of all the model parameters. To solve this problem, we propose a model re-estimation method that involves the extraction of reliable information using Gaussian pruning with weight normalization. Namely, the proposed method re-estimates the model by pruning non-dominant Gaussian distributions in expressing the local characteristics of each frame and by normalizing the Gaussian weights of the remaining distributions.

Increase of Fundamental Oscillation Frequency in Resonant Tunneling Diode with Thin Barrier and Graded Emitter Structure

S. Suzuki, A. Teranishi, M. Asada, H. Sugiyama, and H. Yokoyama

Proc. of Infrared Millimeter and Terahertz Waves (IRMMW-THz), Rome, Italy, 2010.

We obtained an increase in the oscillation frequency of resonant tunneling diodes (RTDs) using a graded emitter and thin barriers for reduced transit and tunneling times. The fundamental oscillation frequency of 1.04 THz was achieved with this structure. The dependence of output power on oscillation frequency is also shown. The output power was around 10 μW in the 0.9–1 THz region.

Wide-range and Fast-tracking Frequency Offset Estimator for Optical Coherent Receivers

T. Nakagawa, K. Ishihara, T. Kobayashi, R. Kudo, M. Matsui, Y. Takatori, and M. Mizoguchi

Proc. of ECOC 2010, Torino, Italy.

A blind spectrum-based frequency offset estimator with fast tracking time is presented. A receiver using the proposed estimator to eliminate the frequency ambiguity of the m^{th} power algorithm can achieve precise estimation over a wide frequency range.

Efficient Secure Auction Protocols Based on the Boneh-Goh-Nissim Encryption

T. Mitsunaga, Y. Manabe, and T. Okamoto

Proc. of SCIS 2010, IEICE, Takamatsu, Japan.

This paper presents efficient secure auction protocols for first price auction and second price auction. Previous auction protocols are based on a generally secure multi-party protocol called the mix-and-match protocol. However, the time complexity of the mix-and-match protocol is large, although it can securely calculate any logical circuits. The proposed protocols reduce the number of times the mix-and-match protocol is used by replacing them with Boneh-Goh-Nissim encryption, which enables calculation of 2-DNF (disjunctive normal form) of encrypted data.

Spatial Pooling of One-dimensional Second-order Motion Signals

K. Maruya and S. Nishida

Journal of Vision, Vol. 10, No. 13:24, pp. 1–18, 2010.

We can detect visual movements not only from luminance motion signals (first-order motion) but also from non-luminance motion signals (second-order motion). It has been established for first-order motion that the visual system pools local one-dimensional motion signals across space and orientation to solve the aperture problem and to estimate two-dimensional object motion. In this study, we investigated (i) whether local one-dimensional second-order motion signals are also pooled across space and orientation into a global 2D motion and, if so, (ii) whether the second-order motion signals are pooled independently of, or in cooperation with, first-order motion signals. We measured the direction-discrimination performance and the rating of a global circular translation of four oscillating bars, each defined either by luminance or by a non-luminance attribute, such as flicker or binocular depth. The results showed evidence of motion pooling both when the stimulus consisted only of second-order bars and when it consisted of first-order and second-order bars. We observed global motion pooling across first- and second-order motions even when the first-order motion was not accompanied by trackable position changes. These results suggest the presence of a universal pooling system for first- and second-order one-dimensional motion signals.

Creation and Analysis of a Japanese Speaking Style Parallel Database for Expressive Speech Synthesis

H. Nakajima, N. Miyazaki, A. Yoshida, T. Nakamura, and H. Mizuno

Proc. of Oriental COCOSDA 2010, COCOSDA Asia Section, Kathmandu, Nepal.

This paper describes a newly developed database for expressive speech synthesis. This speech database is characterized by two features: i) the sentences are taken from real domains such as sales talk, storytelling, and telephone conversations, where speech is uttered in expressive (or conversational) style, so sentences are domain-dependent and ii) each sentence is uttered in both reading style and expressive style, so this database stores parallel speaking style speech. This database is designed to capture the acoustic and prosodic differences between parallel styles and to elucidate the domain-dependent linguistic characteristics that cause those differences. This paper describes both the concept of this speech database and the issues raised by its implementation. We detail the basic characteristics and preliminary results of two style comparisons to elucidate the linguistic characteristics that contribute to the establishment of expressive speech synthesis.

Effect of Speech Sound Naturalness on the Neural Basis of Format Frequency Discrimination

S. Hiroya and F. H. Guenther

Proc. of Neuroscience 2010, the Society for Neuroscience, San Diego, 2010.

Few previous imaging studies of speech perception have investigated the neural mechanisms underlying discriminability of format frequencies for less natural vowel sounds. First, we developed a novel method for controlling vowel naturalness on the basis of band-limited finite impulse response filters related to the first four formats. The results showed that naturalness was significantly reduced for sounds with decreasing filter bandwidths. Next, we performed a functional magnetic resonance imaging study that investigated the neural basis of formant frequency discrimination in less natural vowel sounds. The result showed that the left-lateralized premotor cortex was more activated for less natural sounds, and the area overlapped that of vowel production. This suggests that the involvement of the premotor cortex varies depending on speech sound naturalness.

Fast Template Matching Based on Normalized Cross Correlation Using Adaptive Block Partitioning and Initial Threshold Estimation

M. Mori and K. Kashino

Proc. of 2010 IEEE International Symposium on Multimedia, pp. 196–203, Taichung, Taiwan.

This paper proposes a fast template matching method based on normalized cross correlation (NCC). NCC is more robust against image variations such as illumination changes than the widely used sum of absolute difference (SAD). A problem with NCC has been its high computation cost. To deal with this problem, we use adaptive block partitioning and initial threshold estimation to extend the multilevel successive elimination algorithm. Adaptive block partitioning provides efficient sub-block partitioning and tighter boundaries. Initial threshold estimation yields a larger boundary threshold. They greatly suppress the number of search points at an earlier level from the beginning of search. The proposed method is exhaustive and robust with respect to template position and size. Experiments show that our method is up to 400 times faster than the brute force method and is significantly faster than conventional methods.

Coded Packet Immediate Access for Contention-based Wireless Relay Networks

D. Umehara, S. Denno, M. Morikura, and T. Sugiyama

Proc. of the 4th International Conference on Signal Processing and Communication Systems (ICSPCS), Vol. 1, No. 1, pp. 1–9, Gold Coast, Australia, 2010.

This paper proposes a medium access control (MAC) protocol with network coding on relay nodes for contention-based multihop wireless relay networks. The proposed protocol is called coded packet priority access (CPPA) protocol in which coded packets have higher transmission opportunity than non-coded native packets at relay nodes. In this paper, the performance of coded packet immediate access (CPIA) protocols, which are a subclass of CPPA protocols, is evaluated for single-relay bidirectional symmetric traffic and upper and lower bounds of analytical throughput are derived for any given node traffic. It is shown that the lower bound approximates to the throughput obtained from computer simulations with high accuracy. The conventional slotted ALOHA protocol with network coding (S-ALOHA/NC) is required to adapt the transmission probability of a relay node to a rational function of node traffic so as to maximize the throughput whereas the CPIA protocol achieves the maximize throughput only if the relay node transmits no native packets. Furthermore it is clarified that the CPIA protocol is superior to the S-ALOHA/NC protocol in delay for given retransmission probabilities of user nodes.

Enhancement of IEEE 802.11 and Network Coding for Single-relay Multi-user Wireless Networks

D. Umehara, C. -H. Huang, S. Denno, M. Morikura, and T. Sugiyama

Proc. of the 4th International Conference on Signal Processing and Communication Systems (ICSPCS), Vol. 1, No. 1, pp. 1–9, Gold Coast, Australia, 2010.

Network coding is a promising technique for improving system performance in wireless multihop networks. In this paper, the throughput and fairness in single-relay multiuser wireless networks are evaluated. The carrier sense multiple access with collision avoidance (CSMA/CA) protocol and network coding are used in the medium access control (MAC) sublayer in such networks. The fairness of wireless medium access among stations (STAs), the access point (AP), and the relay station (RS) results in asymmetric bidirectional flows via the RS; as a result, the wireless throughput decreases substantially. To overcome this problem, an autonomous optimization of the minimum contention window size is developed for CSMA/CA and network coding to assign appropriate transmission opportunities to both the AP and RS. By optimizing the minimum contention window size according to the number of STAs, the wireless throughput in single-relay multi-user networks can be improved and fairness between bidirectional flows via the RS can be achieved. Numerical analysis and computer simulations enable us to evaluate the performances of CSMA/CA and network coding in single-relay multi-user wireless networks.

Efficient Data Gathering for Hierarchical Sensor Networks

Y. Kishino, Y. Sakurai, K. Kamei, T. Maekawa, Y. Yanagisawa, and T. Okadome

Information Processing Society of Japan, Vol. 3, No. 4, pp. 82–93, 2010.

In this paper we propose an efficient data gathering method using a hierarchical tree topology in a high-density sensor network. The proposed method gathers sensor data using Singular Value Decomposition (SVD) for each cluster by taking advantage of periodicity and correlation among sensor data. It can reduce the amount of data in wireless communication and errors and achieve efficient data gathering. Our experimental result shows that the hierarchical network topology and data gathering by SVD can reduce the amount of data and errors when the level of network topology is high.

Single-electron Devices based on Si Nanoscale FETs

K. Nishiguchi and A. Fujiwara

Proc. of Workshop on Innovative Devices and Systems, WINDS, Hawaii, USA, 2010.

A MOSFET-based circuit utilizing single electrons is demonstrated at room temperature. A nano-wire MOSFET can transfer single electrons one after another to a storage node thanks to the extremely small current leakage of the MOSFET. The electrons transferred to the node are detected by another wire MOSFET, which is located near the node. The combination of these nano-wire MOSFETs allows real-time monitoring of the single-electron transfer, which helps microscopic understanding of individual electron movement in the MOSFET. While the MOSFET can control the average movement of single electrons, each movement of an individual electron is completely random. Such controllability and randomness of electron movement is used for high-quality random-number generation (RNG) suitable for data processing that stochastically extracts the most preferable pattern among various ones. The MOSFET-based RNG allows fast operation as well as high controllability, which leads to flexible extraction of the preferable pattern. This stochastic data processing promises high efficiency, fast operation, and low power consumption like the human brain.

Risk Management and Intelligence Management during Emergency

M. Higashida, Y. Maeda, and H. Hayashi

Journal of Disaster Research, Vol. 5, No. 6, pp. 636–637, 2010.

In the 15 years since Kobe's Hanshin-Awaji Earthquake, awareness is growing that simply gathering information may not be enough for preparing systems, executing emergency responses, and making decisions rapidly and precisely. The question has become how—and whether—emergency response information can be used effectively and efficiently for rapid disaster response, recovery, and rebuilding. We analyzed emergency response decision making from the perspective of information processing, looking for the features organizations need to process information efficiently. We also propose how to continuously improve emergency response performance.

Query Graph Pattern Optimization for Efficient Discovery of Implicit Information within Linked Data

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Information Processing Society of Japan, Vol. 51, No. 12, pp. 2298–2309, 2010.

Spreading the use of the Semantic Web and Linked Data has made it possible to explore new connections between data which were not linked before. The use of various query graph patterns allows us to explore such connections and leads us to find potentially useful information; however, this information may not be reliable owing to its linkages; for example, if the linkage between the data is weak. Moreover, in a huge set of Linked Data, there are too many patterns to follow and many of them may contain similar semantic connections. Our goal is to select query graph patterns that allow us to find reliable information efficiently from a huge number of patterns. We propose a method to reduce the number of query graph patterns while maintaining the pattern variations to meet different users' needs. To achieve high reliability for the information reached, we select the patterns made of two paths. To ensure wide variations, we classify existing patterns into some representative categories and keep all the categories while we reduce the number. By verifying with real datasets, we confirmed that we could reduce the number by up to 9.1% of its original and also underpinned the reliability of the resulting information.

Bounce Hardness Index of Gravitational Waves

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Classical and Quantum Gravity, Institute of Physics, Vol. 27, No. 24, p. 245021, 2010.

We present a method of mode analysis to search for signals with frequency evolution and limited duration in a given data stream. Our method is a natural expansion of Fourier analysis, and we can obtain information about frequency evolution with high frequency precision and high time resolution. Applications of this method to the analysis of inspiral and burst signals show that the signals are characterized by an index that we name 'bounce hardness'. The index corresponds to the growth rate of the signals.

Fundamental Oscillation of Resonant Tunneling Diodes above 1 THz at Room Temperature

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Fundamental oscillations up to 1.04 THz were achieved in resonant tunneling diodes at room temperature. A graded emitter and thin barriers were introduced in GaInAs/AlAs double-barrier resonant tunneling diodes to reduce the transit time in the collector depletion region and the resonant tunneling time, respectively. Output powers were 7 μW at 1.04 THz and around 10 μW in the 0.9–1 THz region. A change in oscillation frequency of about 4% with bias voltage was also obtained.

Performance Analysis of Slotted ALOHA and Network Coding for Single-relay Multi-user Wireless Networks

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Deployment of wireless relay nodes can enhance system capacity, extend wireless service coverage, and reduce energy consumption in wireless networks. Network coding enables us to mix two or more packets into a single coded packet at relay nodes and improve performances in wireless relay networks. In this paper, we succeed in developing analytical models of the throughput and delay on slotted ALOHA (S-ALOHA) and S-ALOHA with network coding (S-ALOHA/NC) for single-relay multi-user wireless networks with bidirectional data flows. The analytical models involve the effects of queue saturation and unsaturation at the relay node. The throughput and delay for each user node can be extracted from the total throughput and delay by using the analytical models. One can formulate various optimization problems in traffic control in order to maximize the throughput, minimize the delay, or achieve fairness of the throughput or the delay. In particular, we clarify that the total throughput is enhanced in the S-ALOHA/NC protocol on condition that the transmission probability at the relay node is set to the value on the boundary between queue saturation and unsaturation. Our analysis provides achievable regions in throughput on two directional data flows at the relay node for both the S-ALOHA and S-ALOHA/NC protocols. As a result, we show that the achievable region in throughput can be enhanced by using network coding and traffic control.
