AN11058

Design migration from TDA8024 to TDA8035

Rev. 1.0 — 1 June 2011 **Application note**

Document information

Info	Content
Keywords	TDA8035, TDA8024, migration, double implementation
Abstract	This application note describes how to migrate a design from TDA8024 to TDA8035: SW updates, HW differences, and an example based on a double layout implementation.

Revision history

Rev	Date	Description
1.0	20110601	First version

Contact information

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1. Introduction

The TDA8024 is one of the most used Contact Smart Card readers in the Pay TV market.

It has been used for more than 10 years and has created a standard in contact reader front-end interfaces for Set Top Boxes.

The TDA8035 is a successor of this device that fully supports the same functionalities and brings some additional features.

For the Set Top Boxes that traditionally use the TDA8024, it is now recommended to switch from TDA8024 to TDA8035 in the new designs.

The goal of this document is to:

- Present the differences between TDA8024 and TDA8035.
- List all the modifications that should apply to design the TDA8035 instead of TDA8024.
- Propose an implementation where TDA8024 and TDA8035 can be mounted on the same PCB.

2. Differences TDA8024 – TDA8035

2.1 Summary

Table 1. TDA8024 – TDA8035 differences summary

Item	TDA8024	TDA8035	Comments
Package	SO28 or TSSOP28	HVQFN32	-
Inactive mode	No Shutdown mode	2 Shutdown modes: Automatic SD mode and Deep SD mode	New feature of TDA8035 for lower current consumption in inactive mode
Crystal clock input	Crystal never stopped	Crystal stopped when no card activation	New TDA8035 feature for lower current consumption
Activation timing	No delay between CMDVCCN Low and VCC High	Typ. 3.4 ms delay between CMDVCCN Low and VCC High	Delay due to the crystal stop feature
DC/DC converter	Doubler mode	Tripler mode	
Internal regulator (VREG)	No internal regulator	Internal regulator for core power supply	VREG output on TDA8035 must be decoupled
Power supply strategy	2 power supply sources generally required	1 power supply source is generally enough	-
Presence pins	2 presence pins PRES (active high) and PRESN (active low)	1 presence pin PRESN (active low)	-
Chip select pin (CS)	No chip select pin	1 Chip select pin	Several TDA8035 can be cascaded.
Card class support	Classes A and B (5V and 3V)	Class A, B and C (5V, 3V, 1.8V)	-

2.2 Inactive modes

The TDA8035 offers two low consumption modes: Shutdown mode and Deep Shutdown mode while the TDA8024 only offers the inactive mode, when the device is not in a card session.

2.2.1 Shutdown mode

From a functional point of view, the TDA8024 inactive mode corresponds to the Shutdown mode of the TDA8035: it is reached when CMDVCCn goes HIGH. There is no specific management here from the host.

The only difference is the current consumption which is lower in this mode for the TDA8035: 500µA max for TDA8035, and 1.3 mA max for tDA8024.

2.2.2 Deep Shutdown Mode

This mode only exists in TDA8035. It allows reducing the current consumption down to 4µA max.

To enter this mode, the host must tie the input pins 5V3VN and 1.8VN to the ground.

This specific management must be adapted in the host as it is not available for TDA8024.

2.3 Clock input

With TDA8024, when a crystal is used, the clock is never stopped.

In TDA8035, the clock is started only when card activation is requested. This behavior allows reducing the current consumption in inactive modes, but increases the time required to start the smart card activation. (See next chapter)

2.4 Activation timing

The delay between CMDVCCN Low and VCC High is different in the two devices:

This time is very low for the TDA8024 while it is equal to 3.42 ms in the TDA8035, due to clock input stop:

As the input clock is stopped in inactive mode, when starting the card activation process, the TDA8035 must detect the type of clock input (crystal or externally provided clock). This detection time delays the real card activation (starting with VCC rise).

In some cases, it can be required to know this delay, in order to set the RST pin to High level in the right timing window.

Full details on how to manage this delay are given in the TDA8035 application note AN10997, in the Card Activation/Deactivation chapter.

2.5 DC/DC (SBM/SBP)

Both chips embed a DC/DC converter based on capacitor, but with one difference:

The TDA8024 can only work as voltage level doubler, while TDA8035 can work as a tripler.

This difference has two impacts:

- The TDA8035 has 2 more pins for the DC/DC converter: SBM and SBP (while SAM and SAP correspond to S1 and S2 of the TDA8024). A capacitor must be connected between these SBM and SBP pins.
- The TDA8035 thanks to this extra capacitor can generate a 5V power supply for the smart card with a power supply input down to 2.7V, while TDA8024 requires 4V to generate the 5V in the standard conditions (up to 65 mA).

2.6 Internal Regulator VREG

The TDA8035 embeds an internal regulator to supply the core of the IC with 1.8V. This regulator's output is available on pin VREG to be decoupled with a 100nF capacitor.

This capacitor is to add in a new design upgraded from TDA8024 to TDA8035.

2.7 Power Supply strategy

Thanks to the two additional features of the TDA8035 described above (DC/DC in tripler mode and internal regulator), it is possible to supply the TDA8035 with a single source, which corresponds to the CPU digital interface power supply level.

For example, if the host interface is applied with 3.3V, then this 3.3V can be used to supply the TDA8035's host interface, the IC core, and the DC/DC converter

This was generally not the case with TDA8024, which requires a 4V for the DC/DC converter.

2.8 PORADJ

PORADJ can be used in the same way in both chips when it is used, but the connection is different when PORADJ is not used:

For TDA8024, PORADJ must be connected to GND

For TDA8035, PORADJ must be connected to VDDI

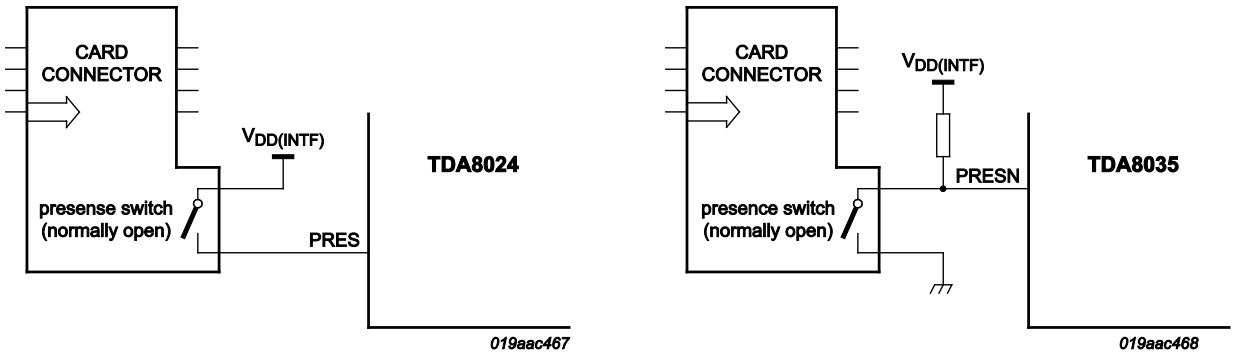
2.9 PRES

TDA8024 has two presence inputs: PRES and PRESN, which are respectively active high and active low. Only one pin can be used at a time.

TDA8035 only offers one presence pin, PRESN, which is active low.

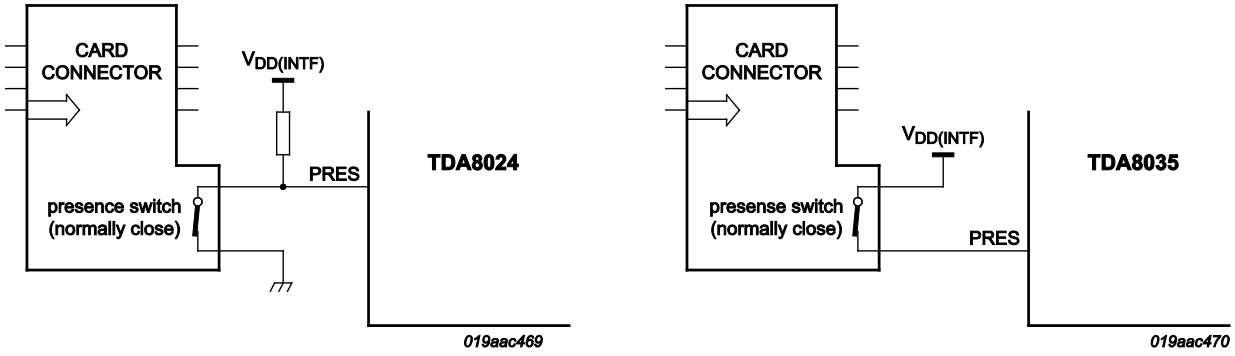
In the TDA8024 designs where PRESN is used, then no change is to apply.

In the TDA8024 designs using PRES pin, then the presence pin connection must be switched as described in the following figure, depending on the smart card connector type (normally open or normally close)



a. TDA8024 b. TDA8035

Fig 1. Presence pin change – Card connector Normally open



a. TDA8024 b. TDA8035

Fig 2. Presence pin change – Card connector Normally close

2.10 CS

TDA8035 has a Chip Select pin, allowing cascading as many devices in parallel as wanted.

In the case only one TDA8035 is needed, this pin must stay connected to VDDI. This is the case for a design where TDA8035 replaces TDA8024

2.11 1.8V

TDA8035 supports 1.8V smart cards, while the TDA8024 does not support them.

This feature uses one pin: EN1.8VN. The connection of this pin in TDA8035 design depends on the new requirements for deep shutdown mode, and of course 1.8V cards management.

If the deep shutdown mode or the 1.8V card management is required, then this pin must be connected to a host GPIO.

If neither the deep shutdown mode nor the 1.8V card management is required, then this pin must be connected to VDDI.

3. New Design Summary

In case of new design switching from TDA8024 to TDA8035, the following items must be checked and updated if required:

Table 2. TDA8024 to TDA8035 migration checklist

Item	HW/SW	Description	Comment
Deep shutdown mode	SW	Add a state in the TDA device driver	Only if the new feature Deep Shutdown Mode is required
Activation timing	SW	Update the activation timings management (CMDVCCn / RSTIN)	Only if the RST assertion must respect a timing constraint
DC/DC new capacitor	HW	Add a 100 nF capacitor between SBM and SBP for the DC/DC converter	Mandatory
VREG capacitor	HW	Add a 100 nF capacitor on VREG for the internal regulator	Mandatory
Single power supply source	HW	Use only one power supply for all TDA8035 blocks.	Optional
PORADJ	HW	Connect PORADJ to VDDI instead of GND	Only if PORADJ functionality is not used
PRES pin	HW	Change the presence detection management	Mandatory if PRES is used on TDA8024 No change if PRESN is used
CS	HW	Connect CS of the TDA8035	Mandatory
1.8V	HW	Connect EN1.8VN to VDDI or to a GPIO of the host	Mandatory to VDDI if no deep shutdown mode used and no 1.8V card management. GPIO else.

4. Double Layout implementation

For new design where the TDA8024 must be implemented in a first step (for timing, qualification… reasons), it is possible to design both TDA8024 and TDA8035 on the same PCB, allowing a reduced workload to switch once the TDA8035 has been fully qualified.

For this double implementation, some constraints must be respected, described here below.

The Cake8024_8035 evaluation board has been developed to demonstrate this use and show an example of this double implementation.

4.1 Demonstration board Cake8024_8035

This demonstration board implements a double layout, allowing it to accept any of the reader devices, in a reduced area.

The schematics and BOM for each product are shown and described in the following pages, as well as the single layout of the board.

This board layout has been designed using only 2 layers.

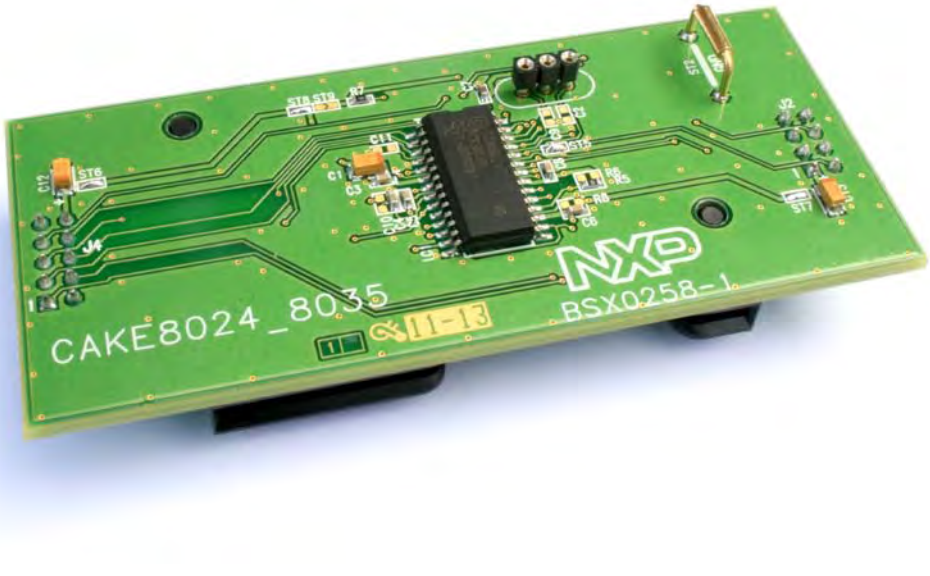


Fig 3. Cake8024_8035 in TDA8024 mode

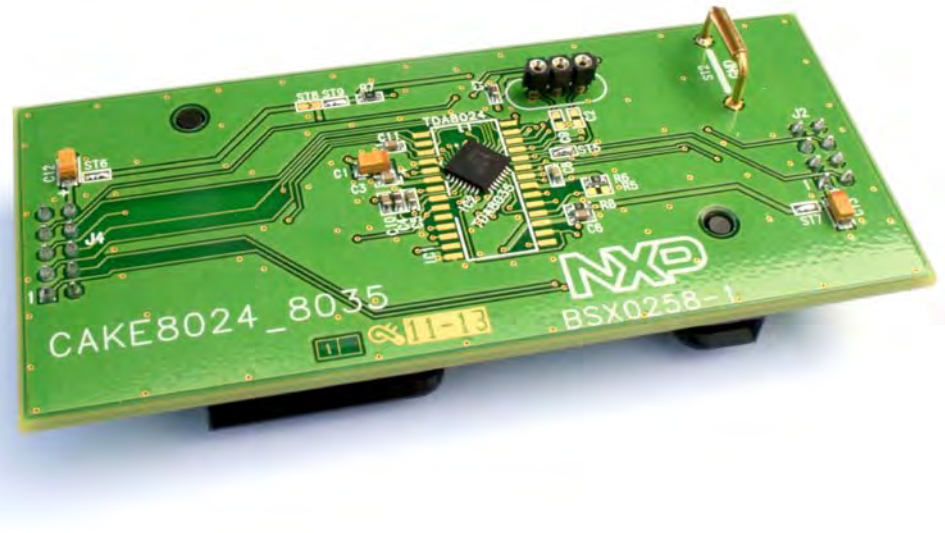


Fig 4. Cake8024_8035 in TDA8035 mode

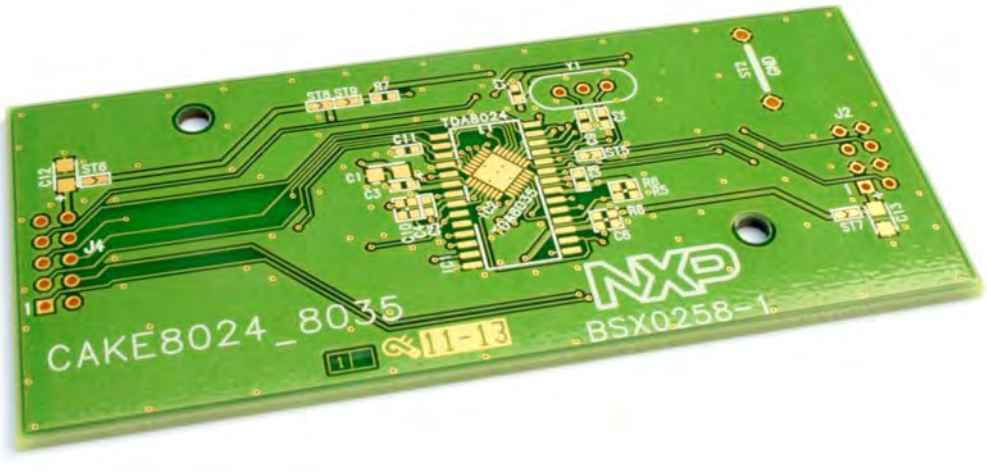


Fig 5. Cake8024_8035 naked PCB

4.1.1 Cake8024_8035 schematics (TDA8024 mode)

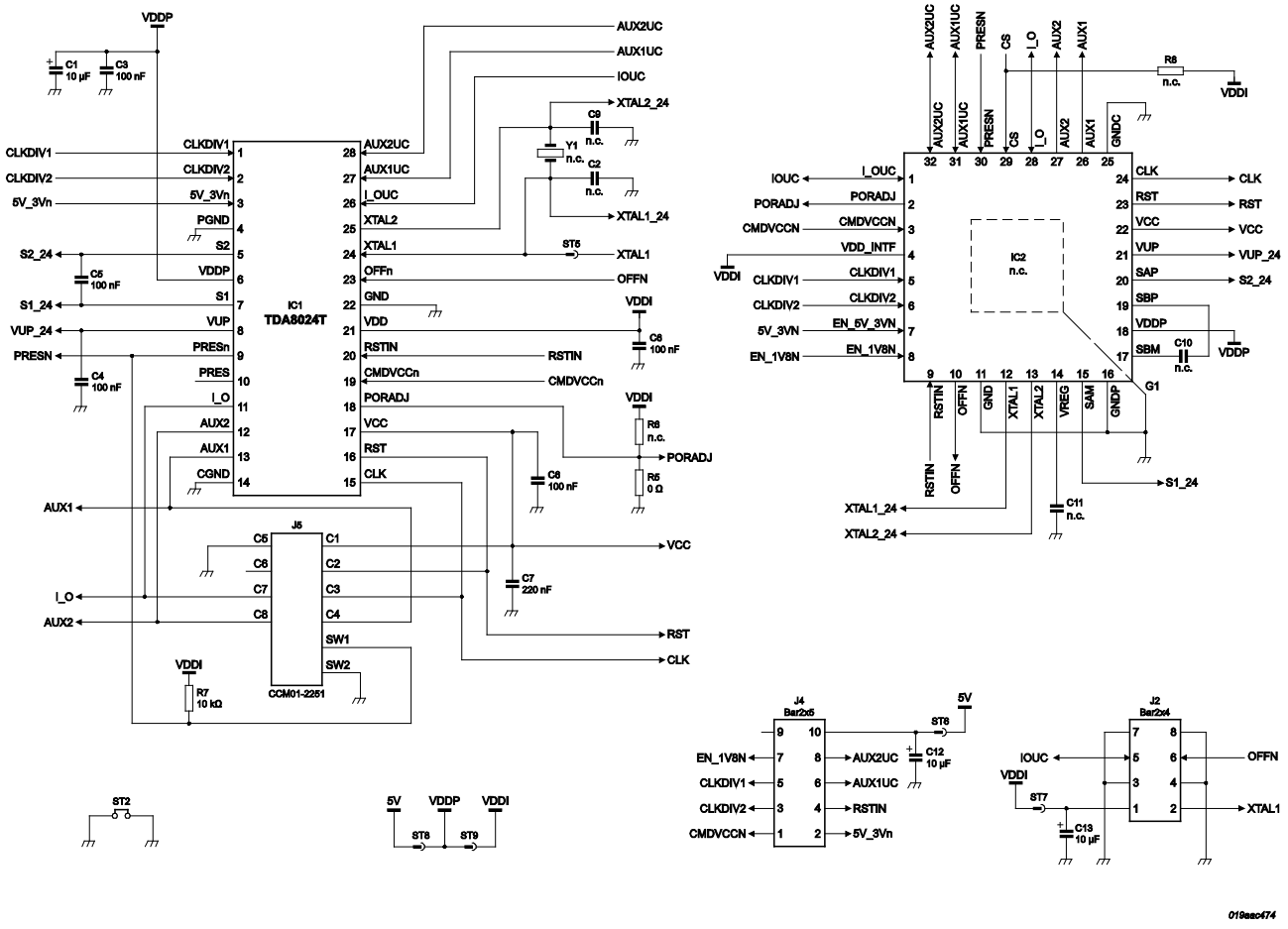


Fig 6. Cake8024_8035 schematics - TDA8024 mode

4.1.2 Cake8024_8035 schematics (TDA8035 mode)

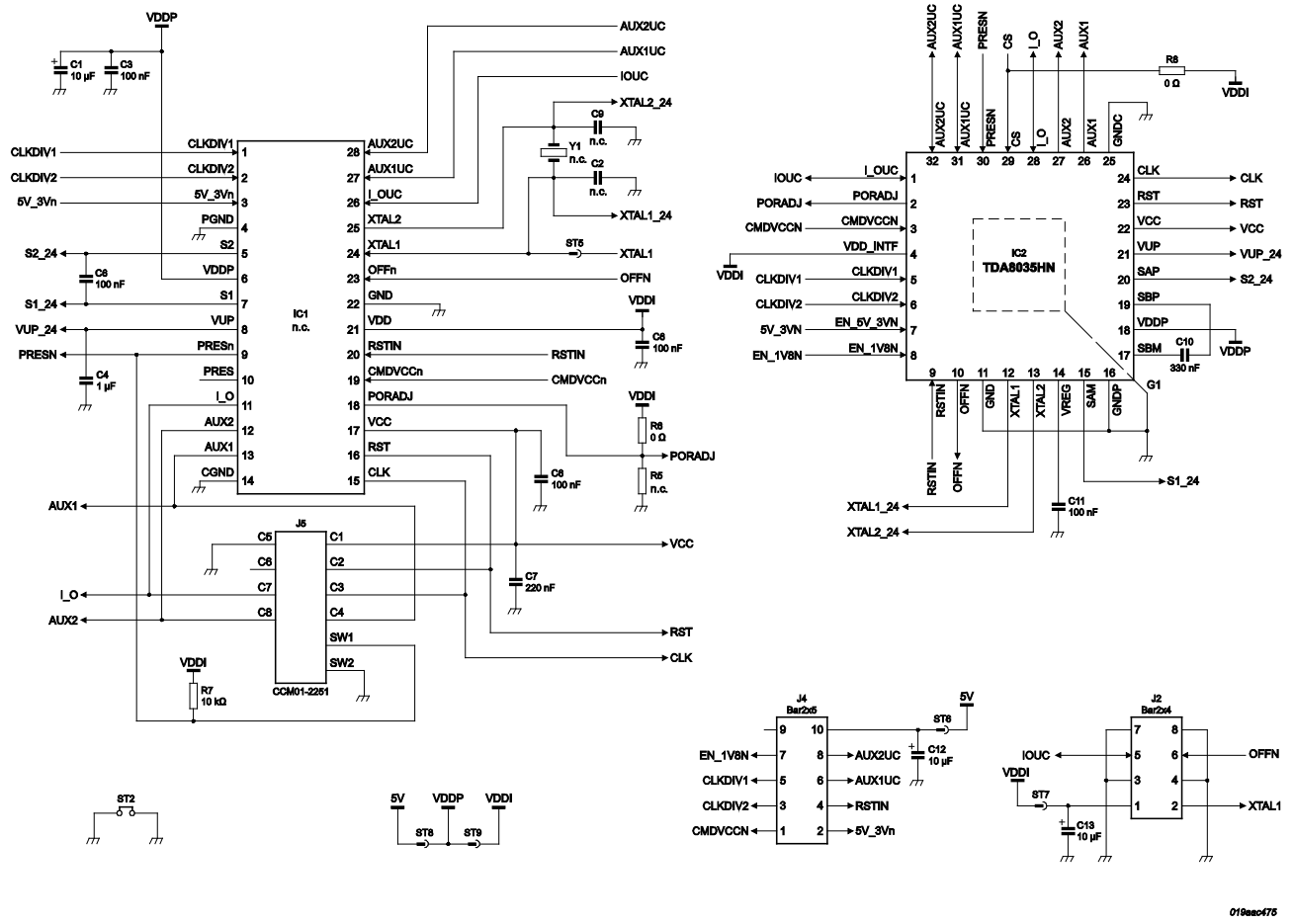


Fig 7. Cake8024_8035 schematics - TDA8035 mode

4.1.3 Cake8024_8035 BOM (TDA8024 mode)

COMPANY PART NO.	COUNT	REFERENCE	GEOMETRY	DESCRIPTION	Fournisseur
25ECNDB3FN104	5	C3 C4 C5 C6 C8	c0603	100nF, Capacite X7R 0603 16V, 5%	
25ECNDB3GQ224	1	C7	c0603	220nF, Capacite X7R 0603 25V, 10%	
25ECNDJAGL106	3	C1 C12 C13	cap_320x160x160_a	10uF, Capacite Tantalium Package TAJA AVX:TAJA106K010R, 10%, 10V-85 degres / 7V-125 degres	
25ECNTA1K0017	1	J2	con_bar_254_2x4_md	Bar2x4, Barrette male droite double rangee, 2x4 points, Pas:2.54mm, H=7mm	
25ECNTA1K0018	1	J4	con_bar_254_2x5_md	Bar2x5, Barrette male droite double rangee, 2x5 points, Pas:2.54mm, H=7mm	
25ECNTZ700001IT	1	J5	con_itt_ccm01_2251	CCM01-2251, ITT_CANNON: CM01-2251LFT, Lecteur de carte 8 voies plus detection	NXP
25EINTK000003KK	1	ST2	cav_1016	CAV_10.16, Cavalier dore 10.16mm KONTEK:3130676000500	
25ERESA3D000B	1	R5	r0603	0, Resistance Package CMS 0603 1% 0.1W	
25ERESA3D1002	1	R7	r0603	10k, Resistance Package CMS 0603 1% 0.1W	
pnsx_c0603_nc	4	C2 C9 C10 C11	c0603	N.C., Capacite type 0603 ***NON CABLE***, -	
pnsx_chev_citr_s	3	ST6 ST7 ST8	chev_citr_o_bom	A_SOUDER, Chevron Citroen 0603 !!! A SOUDER !!!	
pnsx_hc49s_NC_plot	1	Y1	xtal_hc49s_plot	N.C., Quartz package HC49/S ***NON CABLE*** sur plot femelle	
pnsx_r0603_nc	2	R6 R8	r0603	N.C., Resistance Package CMS 0603 1% 0.1W ***NON CABLE***	
pnsx_tda8024t	1	IC1	so28_sot136_1	TDA8024T, NXP: TDA8024T IC card interface package:so28	NXP
pnsx_tda8035hn_NC	1	IC2	hvqfn32_050_500x500_sot617_3	N.C. , ***NON CABLE***	
zbulle01	1			Circuit_imprime:BSX0258-1	
ztulipe03	1			BULLE06:barrette_femelle_tulipe_3points_type_E-TEC:SIB132S04701	

Fig 8. Cake8024_8035 BOM - TDA8024 mode

4.1.4 Cake8024_8035 BOM (TDA8035 mode)

COMPANY PART NO.	COUNT	REFERENCE	GEOMETRY	DESCRIPTION	Fournisseur
25ECNDA3GN105	1	C4	c0603	1uF, Capacite X5R 0603 16V, 10%	
25ECNDA3GN334	2	C5 C10	c0603	330nF, Capacite X5R 0603 16V, 10%	
25ECNDB3FN104	4	C3 C6 C8 C11	c0603	100nF, Capacite X7R 0603 16V, 5%	
25ECNDB3GQ224	1	C7	c0603	220nF, Capacite X7R 0603 25V, 10%	
25ECNDJAGL106	3	C1 C12 C13	cap_320x160x160_a	10uF, Capacite Tantalium Package TAJA AVX:TAJA106K010R, 10%, 10V-85 degres / 7V-125 degres	
25ECNTA1K0017	1	J2	con_bar_254_2x4_md	Bar2x4, Barrette male droite double rangee, 2x4 points, Pas:2.54mm, H=7mm	
25ECNTA1K0018	1	J4	con_bar_254_2x5_md	Bar2x5, Barrette male droite double rangee, 2x5 points, Pas:2.54mm, H=7mm	
25ECNTZ700001IT	1	J5	con_itt_ccm01_2251	CCM01-2251, ITT_CANNON: CM01-2251LFT, Lecteur de carte 8 voies plus detection	NXP
25EINTK000003KK	1	ST2	cav_1016	CAV_10.16, Cavalier dore 10.16mm KONTEK:3130676000500	
25ERESA3D000B	2	R6 R8	r0603	0, Resistance Package CMS 0603 1% 0.1W	
25ERESA3D1002	1	R7	r0603	10k, Resistance Package CMS 0603 1% 0.1W	
pnsx_c0603_nc	2	C2 C9	c0603	N.C., Capacite type 0603 ***NON CABLE***, -	
pnsx_chev_citr_s	3	ST6 ST7 ST9	chev_citr_o_bom	A_SOUDER, Chevron Citroen 0603 !!! A SOUDER !!!	
pnsx_hc49s_NC_plot	1	Y1	xtal_hc49s_plot	N.C., Quartz package HC49/S ***NON CABLE*** sur plot femelle	
pnsx_r0603_nc	1	R5	r0603	N.C., Resistance Package CMS 0603 1% 0.1W ***NON CABLE***	
pnsx_tda8024t_NC	1	IC1	so28_sot136_1	N.C., ***NON CABLE*** NXP: TDA8024T IC card interface package:so28	
pnsx_tda8035hn	1	IC2	hvqfn32_050_500x500_sot617_3	TDA8035HN, NXP: TDA8035HN IC Card Interface package:hvqfn32	NXP
zbulle01	1			Circuit_imprime:BSX0258-1	
ztulipe03	1			BULLE06:barrette_femelle_tulipe_3points_type_E-TEC:SIB132S04701	

Fig 9. Cake8024_8035 BOM - TDA8035 mode

4.1.5 Cake8024_8035 Layout (Top view)

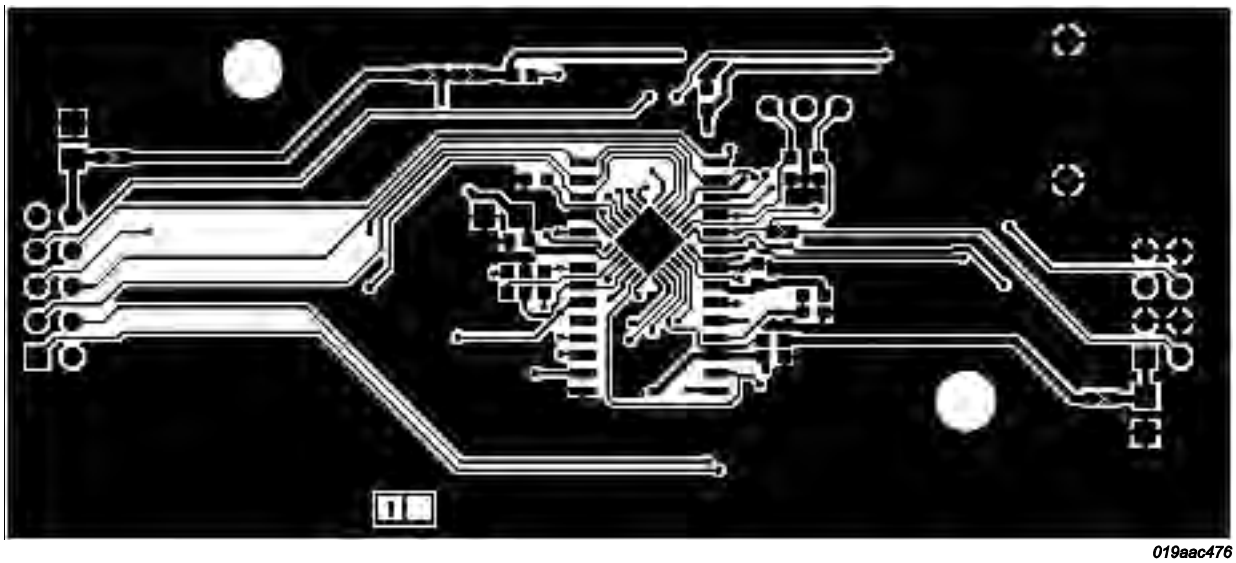


Fig 10. Cake8024_8035 Layout – Top View

4.1.6 Cake8024_8035 Layout (Bottom view)

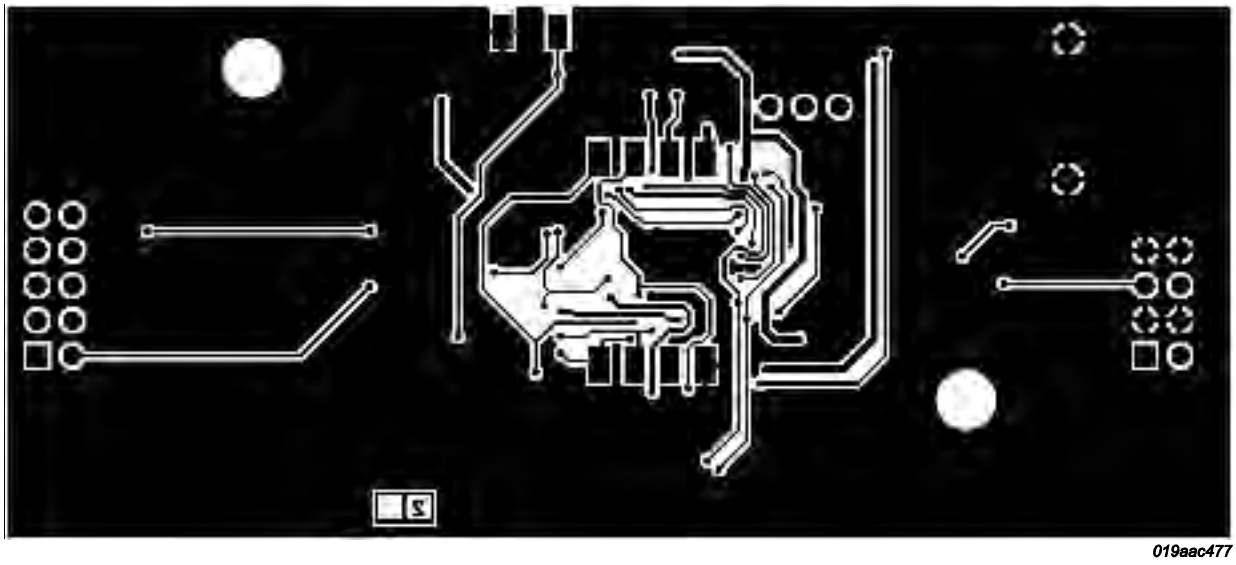


Fig 11. Cake8024_8035 Layout – Bottom View

4.1.7 Cake8024_8035 Components (Top view)

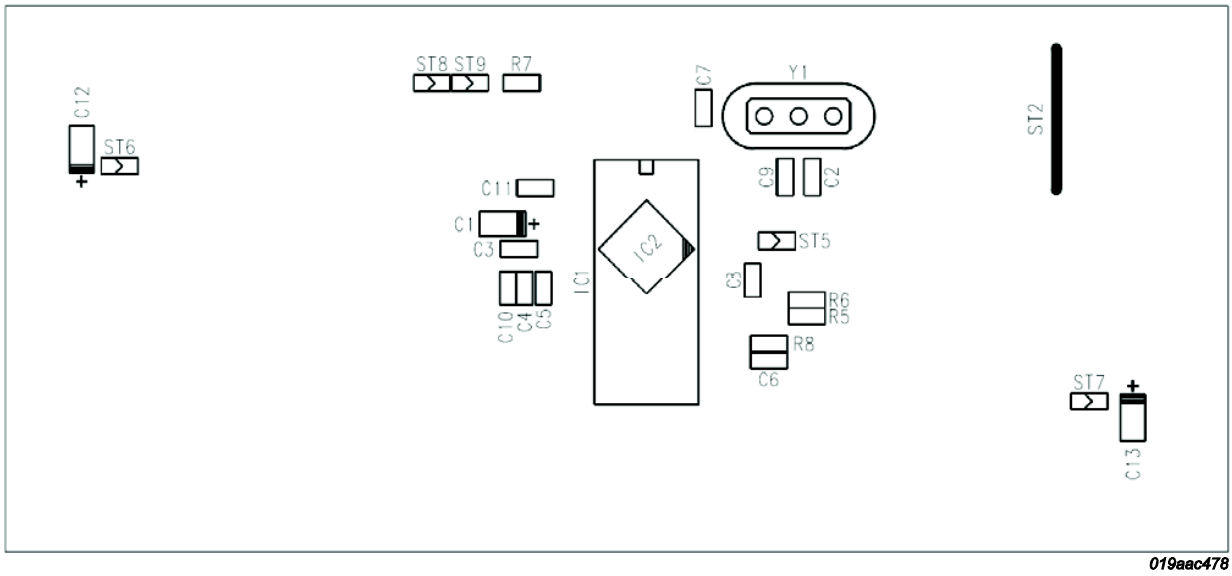


Fig 12. Cake8024_8035 Components – Top View

4.1.8 Cake8024_8035 Components (Bottom view)

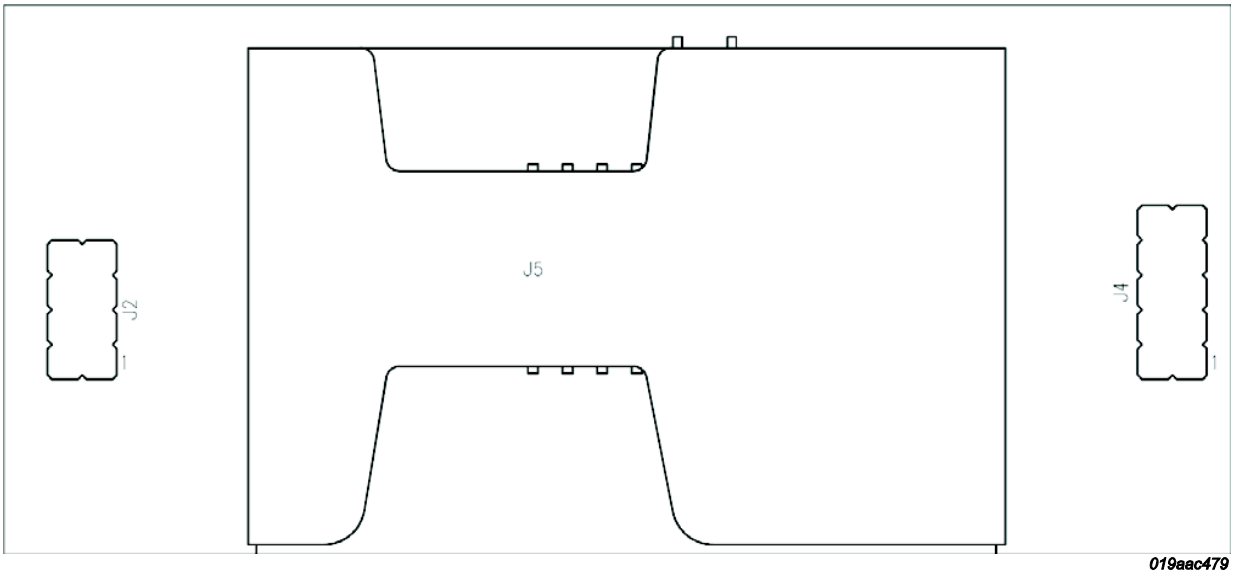


Fig 13. Cake8024_8035 Components – Bottom View

4.2 Double Implementation constraints

4.2.1 DC/DC converter

The DC/DC converter is one of the most critical parts when designing on of these devices. There are two main reasons that require taking a special care of this design part:

- A bad DC/DC layout generates noise that can disturb other signals in the PCB
- The DC/DC layout, if not correctly grounded, can disturb itself and stop functioning. This is mainly the case with TDA8024 which has a quite sensitive DC/DC block.

The general rules to implement a DC/DC layout are:

- Short connections
- Very short and low resistive connection between the DC/DC external components (capacitors) and its dedicated ground pin (GNDP or PGND)

In this double implementation layout, the first part to design is the DC/DC layout for TDA8024, which is the most critical part.

The Vup capacitor, and the VDDP decoupling, must have a maximum attention, in order to respect the above rules.

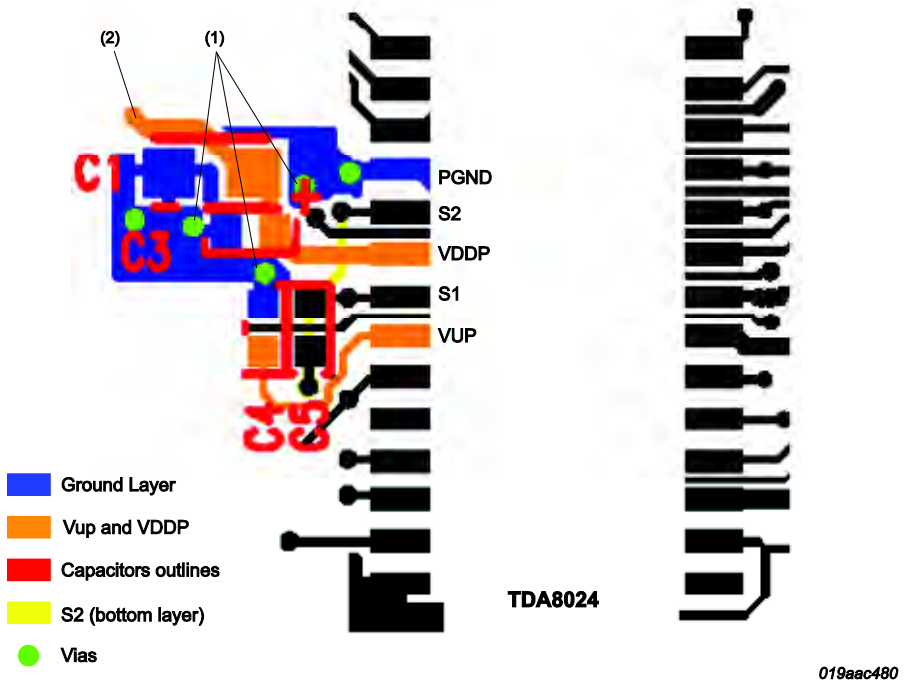
Then the TDA8035 must be placed in order to have its dedicated DC/DC pins as close as possible to the TDA8024's DC/DC pins.

The figure next page is an extract of the board layout, where the routing of the TDA8024 DC/DC is highlighted. Other signals are removed for easier understanding.

The first step to design this layout is to place the capacitors for VDDP (C1 and C3), VUP (C4), and S1-S2 (C5).

Then the track from the pin to its dedicated capacitor must be routed as short as possible.

Finally, the connection between these capacitors and the ground pin PGND (DC/DC dedicated ground pin) must be as short as possible. Basically it has to be the shortest ground connection (shorter than connection to CGND or GND pin (pin #14 and pin #22).



(1) Vias in ground layers for short connection to PGND

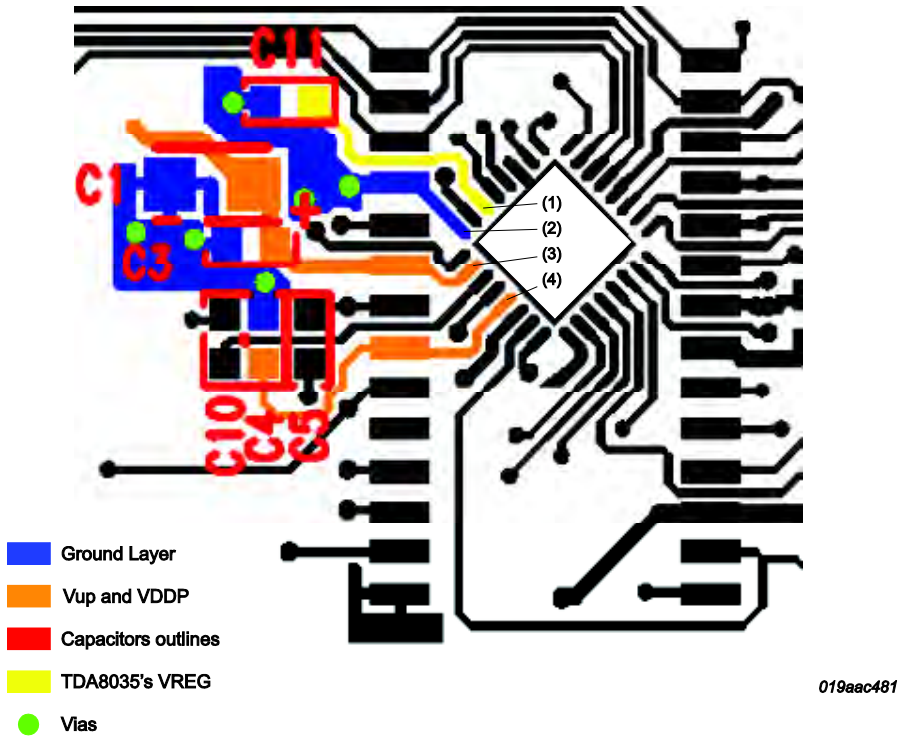
(2) VDDP power supply input

Fig 14. TDA8024 DC/DC layout

Once these signals have been routed, the TDA8035 can be placed, with short distance between TDA8035's DC/DC pins and TDA8024's DC/DC pins.

The remaining capacitors for the TDA8035 must then be placed as close as possible to the ICs. (C10 for SBM/SBP, and C141 for VREG)

On the next figure, the layout of the TDA8035 has been added to show the coexistence of both layouts.



(1) TDA8035's VREG pin
(2) TDA8035's GNDP pin
(3) TDA8035's VDDP pin
(4) TDA8035's VUP pin

Fig 15. TDA8024 + TDA8035 DC/DC layout

4.2.2 Smart card signals

The second main constraint that must be respected is the layout of the smart card signals.

Depending on the application and the targeted market, these signals may be monitored for certification (e.g. NDS…). These signals must have a low noise level to pass most of the certifications.

The main reason that causes noise on the smart card signals is the crosstalk between the signal and the clock line. Then the CLK line from the TDA to the smart card must be as short as possible and be kept far from other signals.

If possible, this line must be shielded with ground layers on each side.

The pictures below show the routing of this smart card clock signal on the reference design.

The first one is the top layout with the CLK line highlighted.

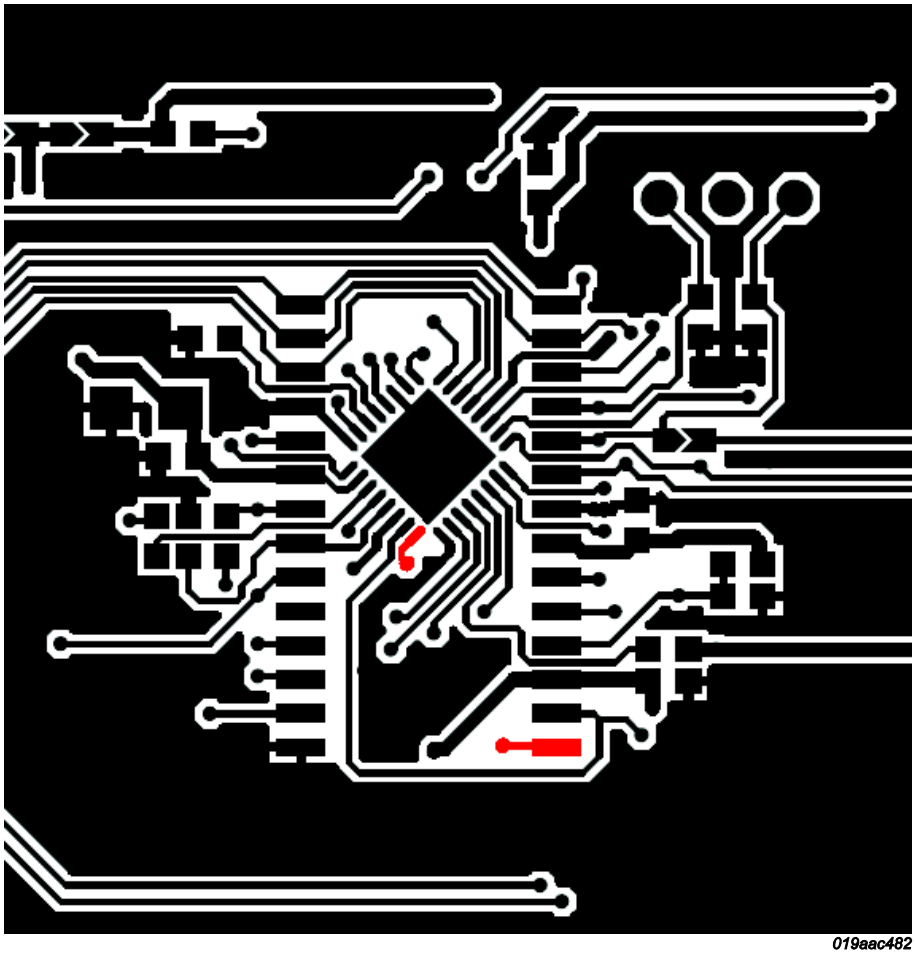


Fig 16. Top side layout – CLK highlighted

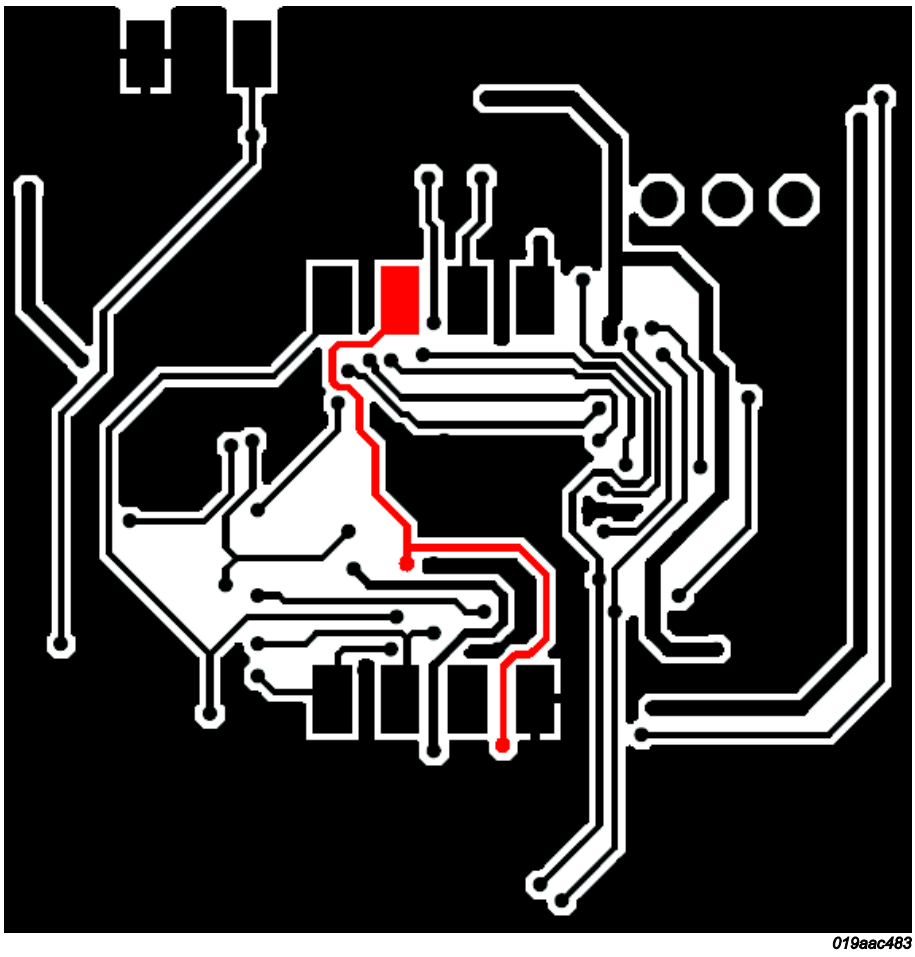


Fig 17. Bottom side layout – CLK highlighted

4.3 Layout overview

The following figure gives a full overview of the layout of this reference design: Top and Bottom layers.

Both sides are represented without ground layers: the black lines are the TOP layout, while the orange tracks are the BOTTOM.

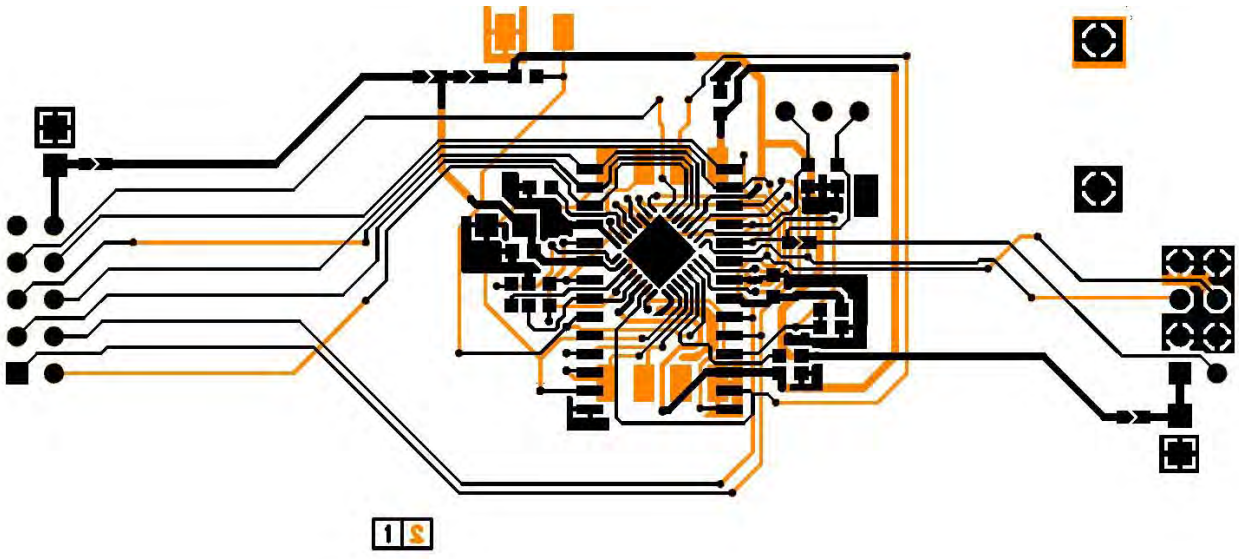


Fig 18. Cake8024_8035 both layers

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6. List of figures

7. List of tables

8. Contents

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