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Small Outline Integrated Circuit (SOIC) Package

1 Introduction

This application note provides guidelines for handling and assembly of Freescale Small Outline Integrated Circuit (SOIC) package during Printed Circuit Board (PCB) assembly.

Guidelines for PCB design, rework, and package performance information such as Moisture Sensitivity Level (MSL) rating, board level reliability, mechanical and thermal resistance data are included for reference.

2 Scope

This document contains generic information that encompasses various Freescale SOIC packages assembled internally or at external subcontractors. Specific information about each device is not provided. To develop a specific solution, actual experience and development efforts are required to optimize the assembly process and application design per individual device requirements, industry standards (such as IPC and JEDEC), and prevalent practices in the assembly environment. For more details about the specific devices contained in this note, visit www.freescale.com or contact the appropriate product application team.

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3 Small Outline Integrated Circuit

Figure 1 shows the standard SOIC offerings through Freescale. The exposed pad (denoted as -EP) version is also displayed.

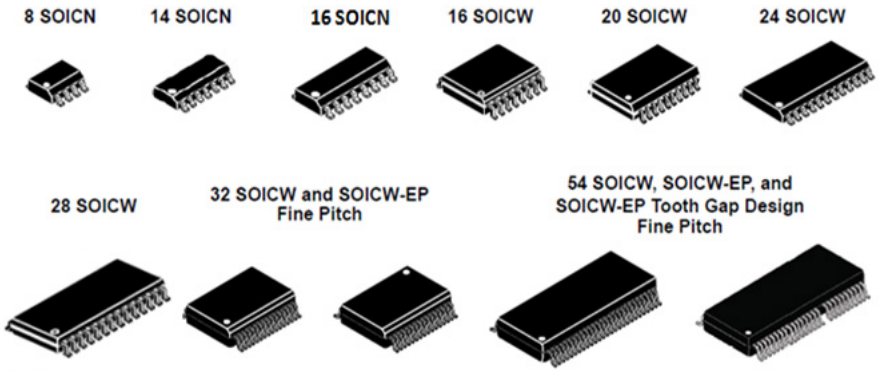


Figure 1. Standard Freescale SOIC Offerings

3.1 Package Description

The SOIC is a surface mount integrated circuit package. The standard form is a flat rectangular body, with leads extending from two sides. The leads are formed in a gull wing shape to allow solid footing during assembly to a PCB. Standard Pb-free lead finish on these packages is Matte Tin plating.

Thermally enhanced SOIC are offered with an exposed die pad and is denoted with the suffix '-EP'. The exposed pad is on the bottom of the SOIC and acts as a ground connection and/or a heat sink for the package. The pad can be soldered to the PCB to dissipate heat. This type of package is also available with an improved die attach technology to achieve low thermal resistance denoted with the prefix 'HT-' (High Thermal). The enhanced SOIC is designed for products with high power and high current requirements and is denoted with prefix 'e' (enhanced).

Table 1. SOIC Package Acronyms

Package Acronyms	Package Description
SOICN	SOIC Narrow Body Non-exposed Pad
SOICW	SOIC Wide Body Non-exposed Pad
SOICW-EP	SOIC Wide Body Exposed Pad
HT-SOICW-EP	High Thermal SOIC Wide Body Exposed Pad
eSOICW-EP	Enhanced SOIC Wide Body Exposed Pad

PB-free fine pitch SOIC's are available in Cu leadframes with Tin matte finish.

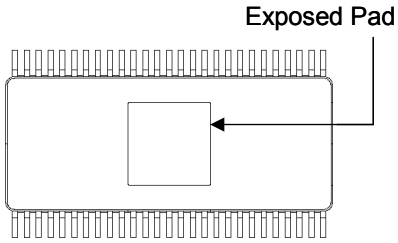


Figure 2. 54ld SOIC-EP Backside View

3.2 Package Dimensions

SOICs are offered in industry standard sizes and thicknesses with various options of lead quantity and pitch. See **Table 2**. Refer to Freescale package case outline drawings to obtain detailed dimensions and tolerances. Check with the Freescale sales team for more information.

Table 2. SOIC Package Acronyms

Package	I/O	Package Body Size (W)	Package Body Size (L)	Package Height Max	Package Pitch
SOIC 8N	8	3.9	4.9	1.75	1.27
SOIC 14	14	3.9	8.6	1.75	1.27
SOIC 16N	16	3.9	9.9	1.75	1.27
SOIC 16W	16	7.5	10.3	2.65	1.27
SOIC 20W	20	7.5	12.8	2.65	1.27
SOIC 24W	24	7.5	15.4	2.65	1.27
SOIC 28W	28	7.5	17.9	2.65	1.27
SOIC 32W	32	7.5	11.0	2.65	0.65
SOIC 54W	54	7.5	17.9	2.45	0.65

3.3 Package Cross-section

The cross-section drawings in Figure 3 show representative internal leadframe design differences between SOICW and SOICW-EP packages. Standard SOICW packages have mold compound which encompasses the entire bottom side of the package while the SOICW-EP design exposes the die pad which increases thermal performance.

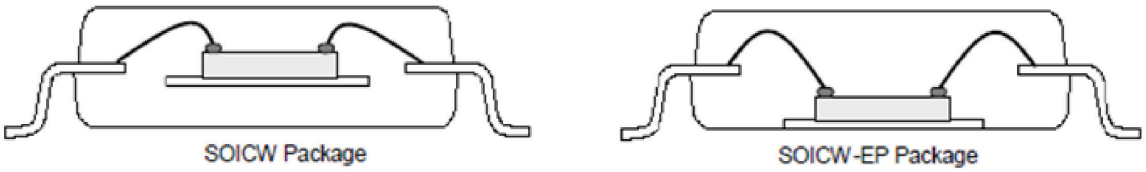


Figure 3. Difference Between Standard and Exposed Pad SOICW

4 Printed Circuit Board Guidelines

4.1 PCB Design Guidelines and Requirements

Proper PCB footprint and stencil designs are critical to ensure high surface mount assembly yields, and electrical and mechanical performance of the mounted package. The design starts with obtaining the correct package drawing. Package Case Outline drawings are available at www.freescale.com. Follow the procedures in **Section 9.1**. An example of SOICW-EP 54LD Case Outline drawing is seen in Figure 4. The goal is a well soldered SOIC gull wing lead as shown in Figure 5.

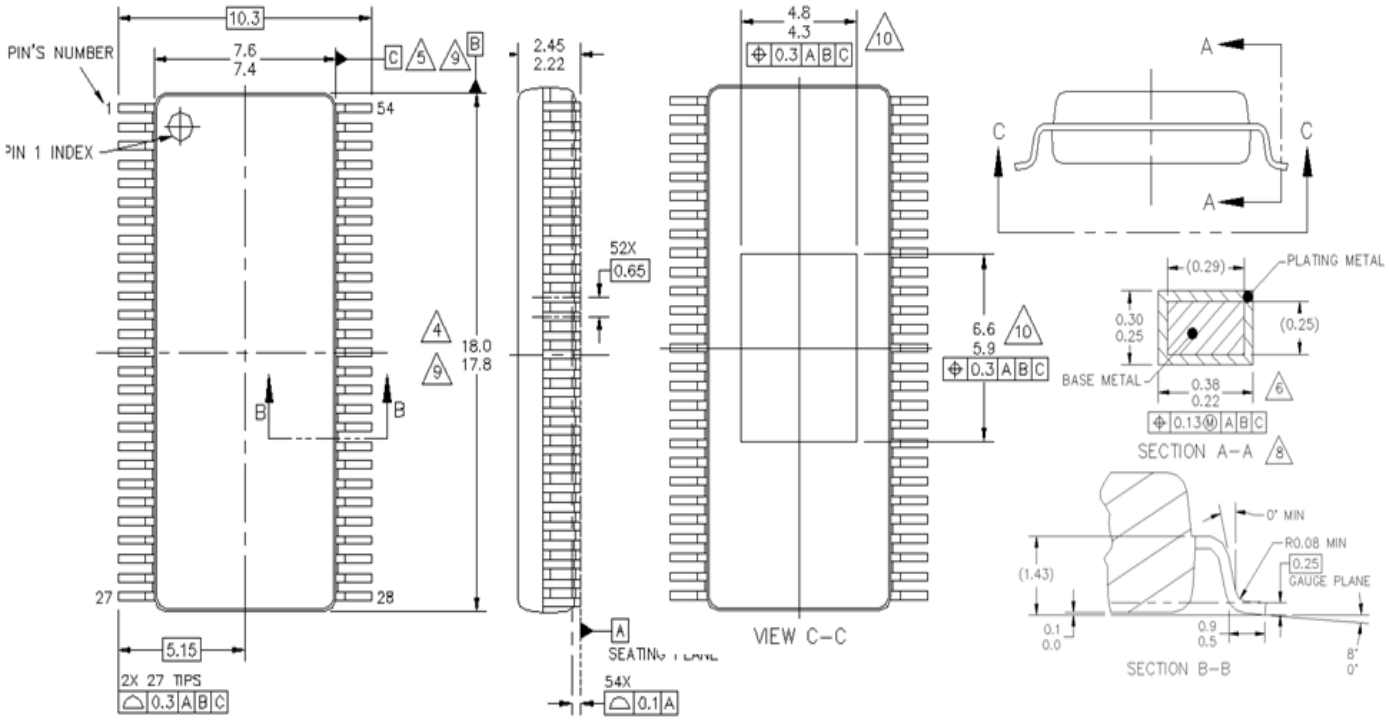


Figure 4. Example of SOICW 54LD Case Outline Drawing

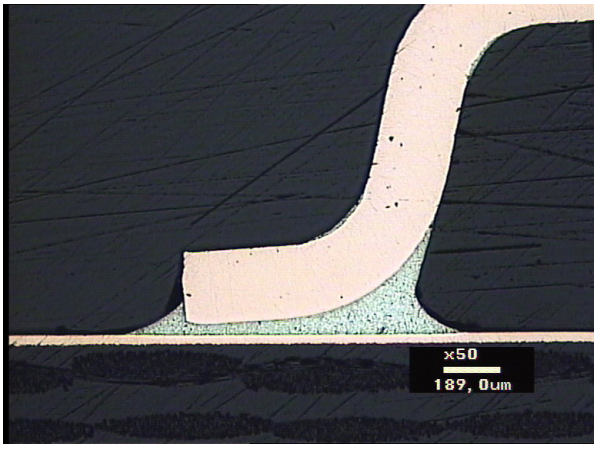


Figure 5. 50x Magnified Optical Microscope Image of a Well Soldered SOIC Lead Based on a Robust Pad Design

4.2 PCB Pad Design

Freescale follows the Generic Requirements for Surface Mount Design and Land Pattern Standards from the Institute for Printed Circuits (IPC), IPC-7351B. This document and an accompanying land pattern calculator can be purchased from the IPC's website http://landpatterns.ipc.org/default.asp. They include guideline SOICs based on assumed package dimensions.

4.2.1 General Pad Guidelines

Some general guidelines for SOIC footprints are:

- Lead foot should be approximately centered on the pad with equal pad extension from the toe and the foot
- Typically, the pad is extended 0.5 mm beyond the SOIC foot at both the heel and the toe
- Care should be taken that PCB pads do not extend under the SOIC body, which can cause issues in assembly
- Pad width should be approximately 60% of the lead pitch. See **Table 3**
- Pitch must be designed in metric using the exact dimensions of 0.65 mm and 1.27 mm

Table 3. Suggested PCB Pad Widths as a Function of Lead Pitch

Lead Pitch (mm)	Pad Width (mm)
0.65	0.38
1.27	0.60
Notes 1.Some legacy products may have alternate pitches.	

Using the example of the SOICW-EP 54LD in Figure 4, the PCB pad width should be designed at 0.38 mm (X1) for this 0.65 mm lead pitch package. To determine the placement and length of the pads, obtain the tip to tip dimension from the package drawing (see Figure 4). It has a range of 10.00 mm to 10.60 mm or a nominal dimension of 10.30 mm. Similarly, the foot length has a range of 0.50 mm to 0.90 mm with a nominal of 0.70 mm. The pad should be 1.70 mm (Y1) in length which is the 0.70 mm nominal foot length with a 0.50 mm extension on the heel and toe sides. Land Center to Center (C) is 9.60 mm, package nominal tip to tip dimension of 10.30 mm reduce by half of the foot length 0.35 mm on both sides. See Figure 6.

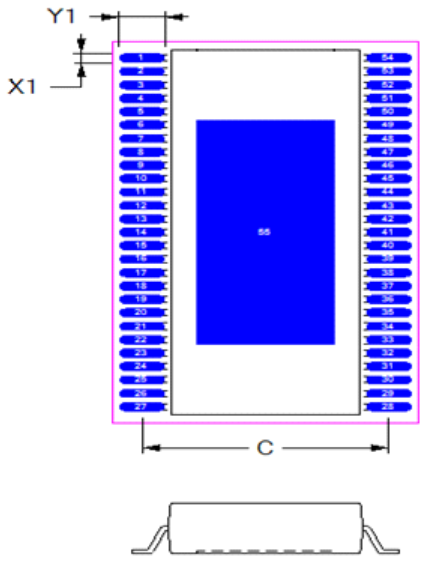


Figure 6. SOIC Land Pattern Dimensions

4.2.2 Thermal/Electrical Pad Guidelines

Exposed pad (EP) SOIC packages are thermally/electrically enhanced leadframe technology based. The bottom of the package provides the primary heat removal path as well as excellent electrical grounding to the PCB. In an EP package, the die attach paddle is down-set within the package such that the pad is exposed during the mold process, as shown in Figure 7. White arrows indicate heat flow. To optimize thermal performance, the PCB design should include a thermal plane, as shown in Figure 7.

Although the land pattern design for EP lead attachment on the PCB should be the same as that for conventional, non-thermally/electrically enhanced packages, extra features are required during the PCB design and assembly stage for effectively mounting thermally/electrically enhanced packages. In addition, repair and rework of assembled packages may involve some extra steps, depending upon the current rework practice within the company.

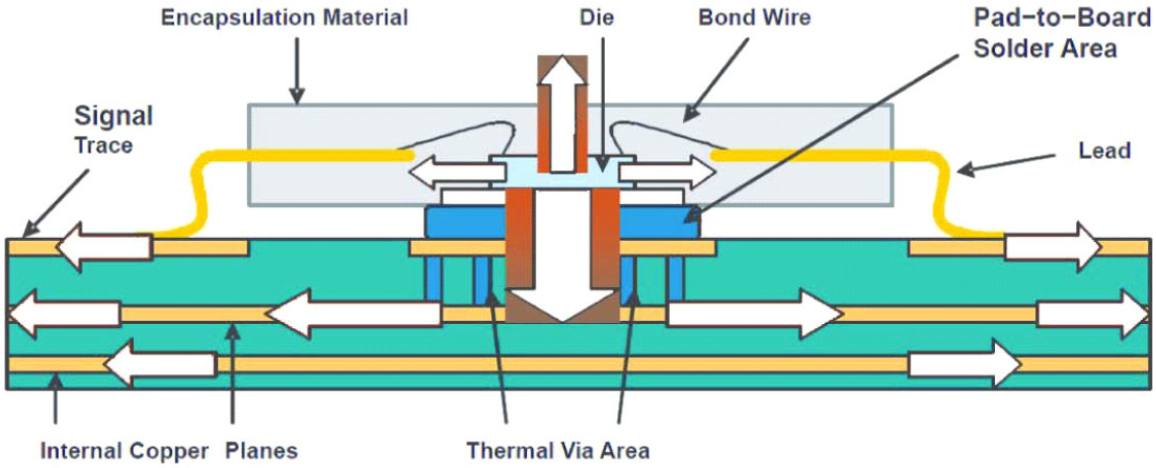


Figure 7. Cross-Section of EP Package with Heat Transfer Schematic

4.2.3 Spacing between PCB PADs for Leads and Exposed Pad

In order to maximize both removal of heat from the package and electrical performance, a land pattern must be incorporated on the PCB within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in Figure 8. The size of the land pattern can be larger, smaller, or even take on a different shape than the exposed pad on the package. However, the solderable area, as defined by the solder mask, should be at least the same size/shape as the exposed pad area on the package to maximize the thermal/electrical performance. A clearance of at least 0.25 mm should be designed on the PCB between the outer edges of the land pattern and the inner edges of leads pad pattern to avoid any shorts. This topic is discussed in more detail in **Section 5.2**.

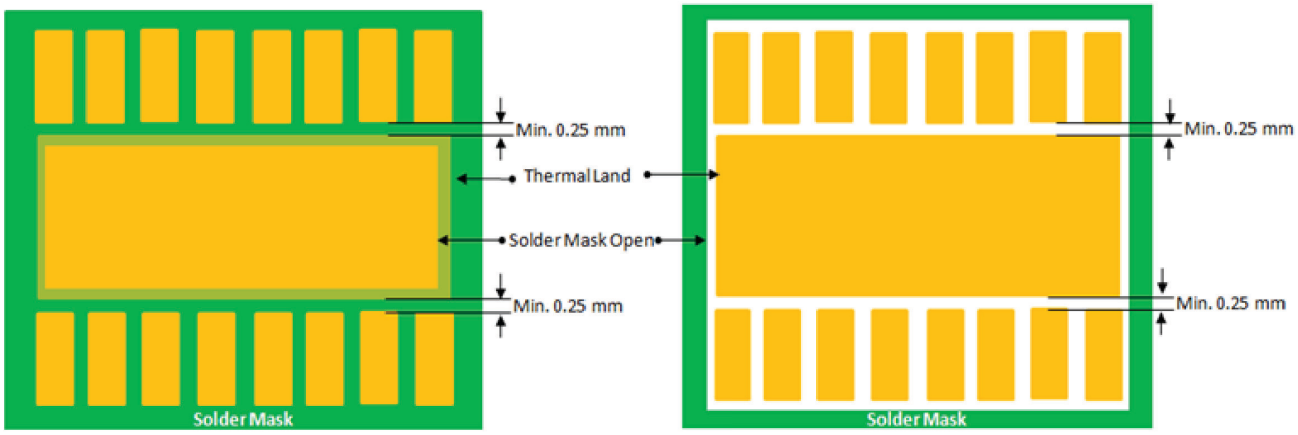


Figure 8. Example of Exposed Pad Land Pattern

4.2.3.1 Alternative Exposed Pad Design

The exposed pad solder land can be segmented into a pad array as shown in Figure 9. The pad array should be created by segmentation of a full copper area by solder mask webbing. Recommended edge length of a matrix pad is between 1.0 mm to 2.0 mm, the distance between the individual pads should be 0.2 mm to 0.4 mm. The minimum distance (width of the solder mask webbing) needs to be aligned with the PCB manufacturers design rules and manufacturing capabilities.

The segmented PCB design facilitates the solder paste flux out gassing during reflow, thereby promoting a lower voiding level of the completed solder joint. At the same time, the maximum size of a single solder void is limited by the dimensions of a single matrix segment.

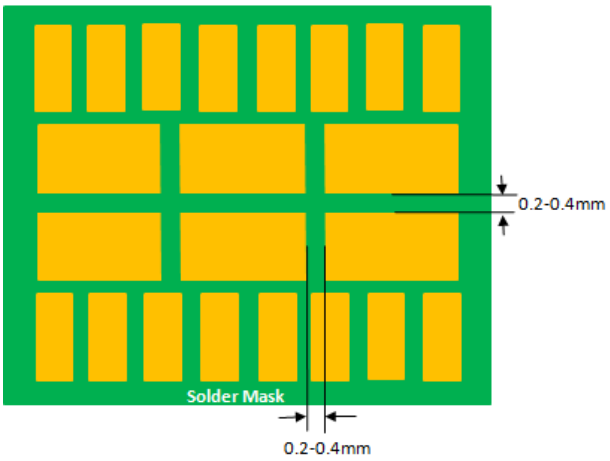


Figure 9. PCB Exposed Pad Land Pattern Segmented by Solder Mask

Alternatively, the exposed pad solder land can be segmented into a symmetric pad array as shown in Figure 10. The pad array can be created either by segmentation of a full copper area by solder mask, or copper defined outlines using NSDM defined pads. Recommended edge length of a matrix pad is between 1 mm to 2 mm, the distance between the pads should be 0.4 mm.

The segmented PCB design facilitates the solder paste flux out gassing during reflow, thereby promoting a lower voiding level of the completed solder joint. At the same time, the maximum size of a single solder void is limited by the dimensions of a single matrix segment.

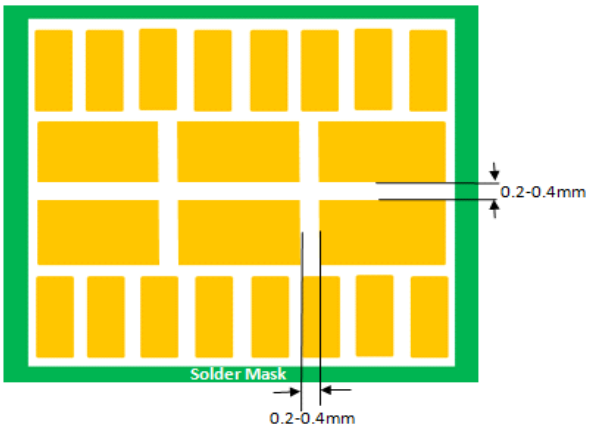


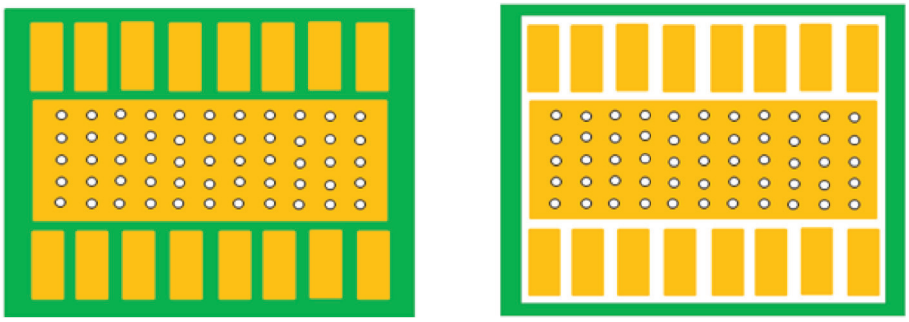
Figure 10. PCB Exposed Pad Land Pattern Segmented by Copper Defined Pads

4.2.4 Vias in the PCB EP Pad

While the land pattern on the PCB provides a means of heat transfer/electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct heat from the surface of the PCB to the ground plane(s). These vias act as "heat pipes". The number of vias is application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number required. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern at 1.2 mm grid pitch, as shown in Figure 11.

It is also recommended the via diameter should be 0.30 mm to 0.33 mm with 1 oz. copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad and the thermal land. If the copper plating does not plug the vias, the thermal vias can be "tented" with solder mask on the top surface of the PCB to avoid solder wicking inside the via during assembly. The solder mask diameter should be at least 0.1 mm (4 mils) larger than the via diameter.

NOTE: These recommendations are to be used as a guideline only.



0.3 mm Diameter at 1.2 mm Pitch Thermal Via

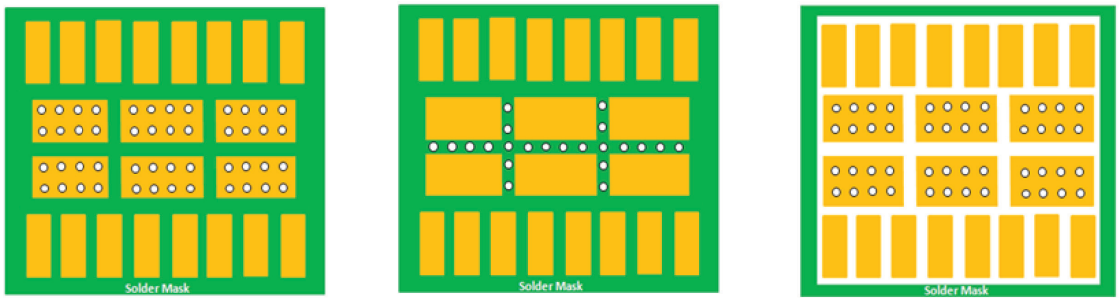
Figure 11. PCB Exposed Pad Via Grid

4.2.4.1 Vias in Alternative Exposed Pads

For solder mask defined array pad design option, there are various thermal via arrangements possible:

- Via is placed in the center of the pad, as shown in Figure 12 (left image)
- Vias are placed in the cross-points of the solder mask webbing, as shown in Figure 12 (center image)
- For copper defined array pad design option, it is recommended to place the thermal via in the center of the pad, as shown in Figure 12 (right image)

All the vias in these two pad design options must be plugged, tented or plated.



SMD Exposed Pad Land Pattern

NSMD Exposed Pad Land Pattern

Figure 12. Via Placement Options for Alternative Pad Options

4.2.5 Pad Surface Finishes

Almost all PCB finishes are compatible with SOICs, including Hot Air Solder Leveled (HASL), Organic Solderability Protectant (OSP), Electroless Nickel Immersion Gold (ENIG), and Immersion Sn and Immersion Ag.

4.2.6 Solder Mask Layer

In general, solder mask should be pulled away from both the Input/Output pads. The solder mask opening around the PCB pads can be as large as the spacing between pads. The area in between the pads may be too thin for the solder mask resulting in the solder mask lifting from the PCB. A potential solution is modification of the solder mask along the pad-to-pad spacing so only the "toes" of the pads are covered with solder mask for better PCB strength.

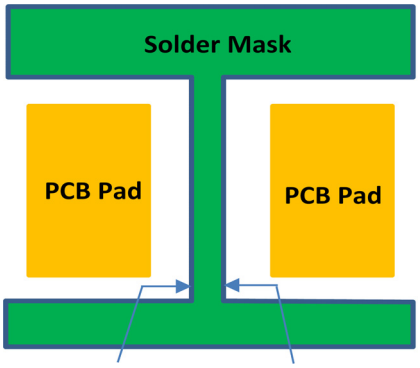


Figure 13. Pad and Solder Mask with Thin Webbing

5 Board Assembly

5.1 Assembly Process Flow

A typical Surface Mount Technology (SMT) process flow is shown in Figure 14.

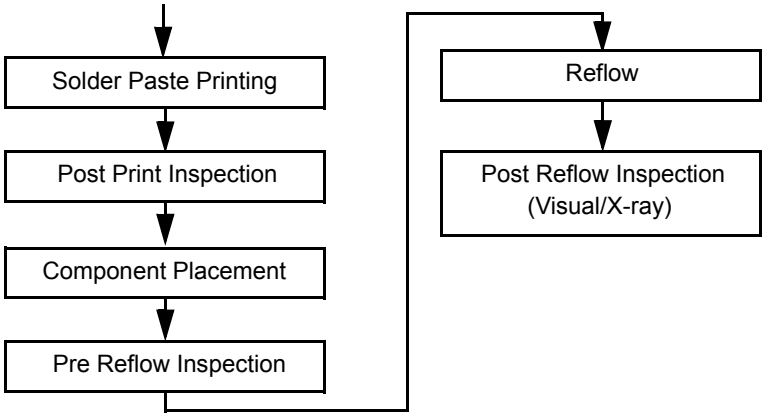


Figure 14. SMT Process Flow

5.2 Solder Stencil/Solder Paste

For maximum thermal/electrical performance, it is required that the exposed pad on the package be soldered to the land pattern on the PCB. This can be achieved by applying solder paste on both the pattern for lead attachment as well as on the land pattern for the exposed pad. While for standard (non-thermally/electrically enhanced) leadframe based packages, the stencil thickness depends on the lead pitch and package co-planarity, the package standoff must also be considered for the thermally/electrically enhanced packages to determine the stencil thickness. For a nominal standoff of 0.1 mm, the stencil thickness of 0.10 mm to 0.15 mm, depending upon the pitch, is recommended. The EP stencil aperture openings should be 0.25 mm smaller than the copper pads on PCB as shown in Figure 15. This allows for proper registration of the stencil to the pad pattern. A large stencil opening may result in poor release. To overcome this, the aperture opening should be subdivided into an array of smaller openings, similar to the thermal land pattern. These guidelines will result in the solder joint area to be about 80% to 90% of the exposed pad area.

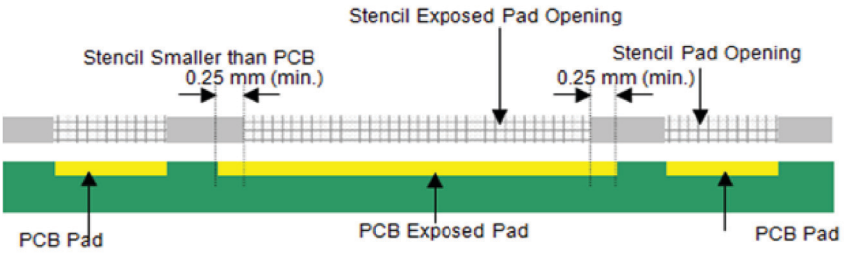


Figure 15. Reduced Solder Stencil Aperture for Exposed Pad

An array design pattern is recommended in the stencil opening for the large thermal pad region. A large opening or aperture in the thermal region allows "scooping" to occur during screen printing. Other reasons for segmenting the thermal regions include minimizing solder standoff mismatch with terminal pads, minimizing solder voids in the thermal region, and minimizing chances of bridging with terminal pads.

Several different array patterns are recommended. Smaller SOIC package sizes do not require any thermal pad pattern on the PCB and stencil, unless to minimize solder voids. On larger packages, stencil thermal openings should be segmented in smaller regions. Examples are shown in Figure 16. The spacing between segments either on the stencil or on the PCB should be 0.15 mm or more. Narrower spacing between segments can become a manufacturing issue.

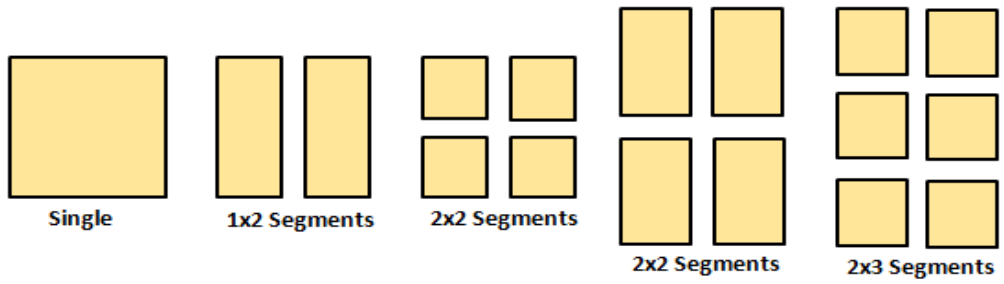


Figure 16. Segmented Stencil Openings

The stencil opening should be approximately 50% to 80% of the total PCB thermal pad area. This stencil-PCB thermal pad ratio ensures proper coverage of the thermal pad area with fewer voids and minimizes the possibility of overflow bridging to the adjacent lead.

5.2.1 Stencil Thickness

The thickness of the stencil determines the amount of solder paste deposited onto the printed circuit board pattern. Due to the fine pitch and small terminal geometry used, care must be taken when printing the solder paste onto the PCB. A 0.12 mm (5 mils) thick stainless steel stencil is recommended for 0.50 mm pitch packages. Package pitches > 0.65 mm can accommodate a 0.150 mm (6 mils) thick stencil.

Solder paste stencil thickness plays a key role in successfully building a PCB. For the large pitch SOIC, 1.27 mm, thicker stencils are the starting point, 0.125 mm to 0.150 mm (5 to 6 mils). However the thickness decision needs to be balanced by production experiences with the remaining components on the PCB and that may lead to thinner stencils. In case of thinner stencils the openings for the large pitch SOIC can be increased. For small pitch SOIC, 0.65 mm, the stencil thickness can be between 0.100 mm to 0.125 mm (4 mm to 5 mils). There is less of a chance that other components on the PCB would suggest an ever thinner stencil.

5.2.2 Solder Paste Properties

Solder paste is one of the most important materials in the SMT assembly process. It is a homogenous mixture of metal alloy, flux and viscosity modifiers. The metal alloy particles are made in specific size and shape. Flux has a direct effect on soldering and cleaning, and it is used to precondition the surfaces for soldering (by removing minor surface contamination and oxidation).

There are two different flux systems commonly available:

- The first flux system type requires cleaning such as standard rosin chemistries and water soluble chemistries. Standard rosin chemistries are normally cleaned with solvents, semi-aqueous solutions or aqueous/saponifier solutions, while the water soluble chemistries are cleaned with pure water.
- The second flux system type requires no cleaning, but normally a little residue will remain on the PCB after soldering, End user should evaluate their entire process and usage of no clean flux to ensure desired results.

The spread of solder paste during reflow partially depends upon the solder paste alloy. Given the same reflow temperature, SnPb solder alloys spread significantly better than the many lead-free pastes (i.e., SnAgCu, SnAgBiCu, etc.).

5.3 Component Placement

The high lead interconnection and insertion density requires precise and accurate placement tools. To meet this requirement, the placement machine should be equipped with optical recognition systems, i.e., vision system, for the centering of the PCB as well as the components during the pick and place motion. A placement accuracy study is recommended in order to calculate compensations required. Freescale follows EIA-481-D standard for tape & reel as well as tube orientation as shown in Figure 17. Refer to **Section 10.3** for additional details.

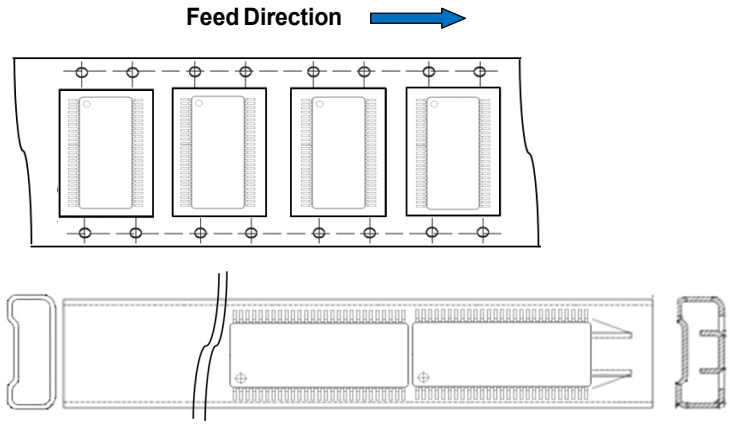


Figure 17. SOIC Orientation in Tube and Tape & Reel

5.4 Soldering

A typical profile band is shown in Figure 18. The actual profile parameters depend upon the solder paste used. The recommendations from paste manufacturers should be followed. The temperature profile is the most important control in reflow soldering, and it must be fine tuned to establish a robust process. In most cases, thermocouples should be placed under the heaviest thermal mass device on the PCB to monitor the reflow profile. Generally, when the heaviest thermal mass device reaches reflow temperatures, all other components on the PCB will have reached reflow temperatures as well.

Nitrogen reflow is recommended to improve solderability and to reduce defects (like solder balling). It is also recommended to monitor the temperature profile of package top surfaces to validate the package peak temperature does not exceed MSL classification of individual devices.

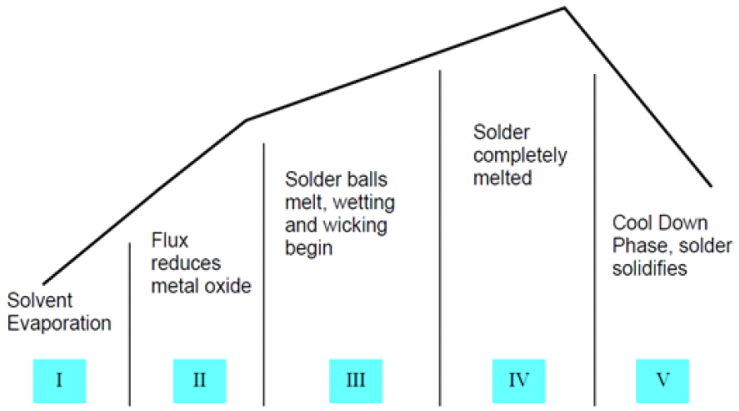


Figure 18. General Solder Reflow Phases

For all devices on the PCB, the solder paste needs to be taken into account for the reflow profile. Every paste has a flux, and the flux dominates the reflow profile for steps like soak time, soak temperature, and ramp rates. Peak reflow temperature is the melting temperature of the metals in the paste, plus a "safety" margin to ensure that all solder paste on the PCB reflows.

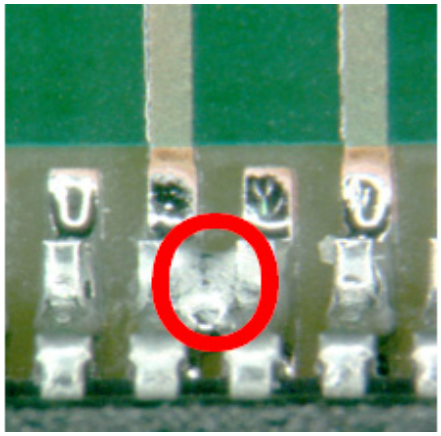
Deviation from the reflow profile recommended by the paste manufacturer should be evaluated first using a copper (Cu) coupon test. The horizontal size for a typical solder paste volume is measured as either a diameter or as "x" and "y" lengths. The Cu coupon is then reflowed and the solder paste volume is measured for either diameter or "x" and "y". The goal is to have a reflow profile with the most horizontal spread. For best results, the Cu coupon should be lightly sanded before use to remove Cu-oxide build up. PCB should be rated for multiple reflow of MSL classification. Cross referencing with the device data sheet is recommended for any additional board assembly guidelines specific to the exact device used. Freescale provides an application note with general comments on reflow profiles at www.freescale.com. AN3300 General Soldering Temperature Process Guidelines is a useful starting point.

5.5 Inspection

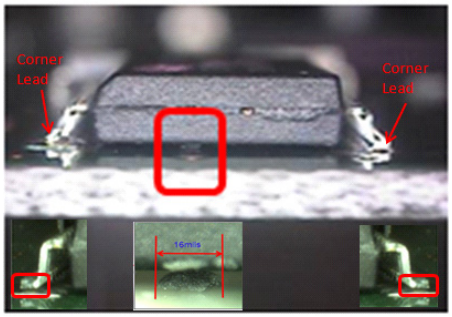
Whenever possible, non-destructive vision/optical inspection and X-ray inspection are recommended to verify any open or short circuit after reflow soldering.

5.6 Common SOIC Defects

Solder Short (Fine Pitch)



Foreign Matter Under SOIC
Causing Open Corner Leads



Insufficient Solder Paste
Causing Solder Joint Integrity Issue

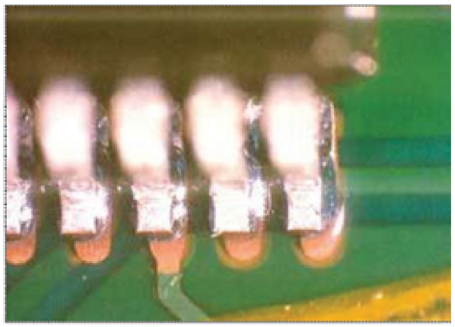


Figure 19. Three Common SOIC Defects

6 Repair and Rework Procedure

6.1 Repairing

Repair of single solder joints is generally possible but requires proper tools. A soldering iron can be used to repair soldering defects for packages that have leads which extend beyond the package periphery, including the SOIC package. Difficulty with fine pitch applications may be observed with the use of soldering irons. The soldering iron temperature and usage must be set so that the package surface temperature does not exceed its maximum allowable temperature.

6.2 Reworking

If a defective component is observed after board assembly, the device can be removed and replaced with a new device. This rework can be performed using the heating methods described in this section.

When performing the rework:

- The influence of the heating on adjacent packages must be minimized. Do not exceed the temperature rating of the adjacent package
- Heating conditions will differ due to differences in the heat capacities of the PCB (board thickness, number of layers) and mounted components used; thus, the conditions must be set to correspond to the actual product and its mounted components
- Freescale follows industry standard component level qualification requirements which include three solder reflow passes. The three reflow passes simulate board level attach to a double sided board and includes one rework pass. Any removed SOIC package should be properly disposed of, so that it will not mix in with new components

A typical rework flow process comprises six stages:

1. Tooling Preparation
2. Package Removal
3. Site Redressing
4. Solder Paste Printing
5. Package Remount
6. Reflow Soldering

NOTE**:** Freescale product quality guaranty/warranty does not apply to products that have been removed, thus, component reuse should be avoided.

In any rework, the PCB will be heated. The thermal limits of PCB and components (e.g. MSL information) have to be followed. During heating, the combination of rapid moisture expansion, materials mismatch, and material interface degradation can result in package cracking and/or delamination of critical interfaces within the components and PCB. In order to prevent moisture induced failures, it is recommended that the PCBs and components have had strict storage control with a controlled environment such as dry air or Nitrogen. In addition, a prebake (e.g. 125 °C for 24 hours for boards with SMT components or 95 °C for 24 hours for boards with temperature sensitive components) is recommended to remove the moisture from components and PCB prior to removal of the package, if the maximum storage time out of the dry pack (see label on packing material) is exceeded after board assembly.

6.3 Typical Individual Rework Process

Typical individual process steps for reworking a SOIC package are as follows:

6.3.1 Tooling Preparation

Various rework systems are available on the market. In general, the rework station should have a split light system, an XY table for alignment, and a hot air system (with a top and bottom heater for component removal). For processing MAPBGA packages, a system should meet the following requirements:

- Heating – Controlled hot air transfer (temperature and air flow) to both the SOIC package and its mounted PCB is strongly recommended. The heating must be appropriate for the correct package size and thermal mass. PCB preheating from beneath is recommended. Infrared heating can be applied, especially for preheating the PCB from the underside, but it should only augment the hot air flow from the upper side. Nitrogen can be used instead of air. Additional information can be found in **Section 6.3.2**.

- Vision system – The bottom side of the package as well as the site on the PCB should be observable. For precise alignment of the package to PCB, a split light system should be implemented. Microscope magnification and resolution should be appropriate for the pitch of the device.
- Moving and additional tools – Placement equipment should have good accuracy. In addition, special vacuum tools may be required to remove solder residue from PCB pads.

6.3.2 Package Removal

If a component is suspected to be defective and is returned, no further defects must be introduced to the device during removal of the component from the PCB as this may interfere with subsequent failure analysis. The following recommendations are intended to reduce the chances of damaging a component during removal:

- Moisture removal – Dry bake components before removal at 125 °C for 16 hours to 24 hours for boards with SMT components or 95 °C for 16 hours to 24 hours for boards with temperature sensitive components.
- Temperature profile – During de-soldering, ensure the package peak temperature is not higher, and temperature ramps are not steeper, than the standard assembly reflow process.
- Mechanics – Do not to apply high mechanical forces for removal. High force can damage the component and/or the PCB which may limit failure analysis of the package. For large packages, vacuum wands can be used (implemented on most rework systems); for small packages, tweezers may be more practical.

If suspected components are fragile, it is especially necessary to determine if they can be electrically tested directly after de-soldering, or if these components have to be preconditioned prior to testing. In this case, or if safe removal of the suspected component is not possible or too risky, the whole PCB or the part of the PCB containing the defective component should be returned.

To remove the faulty component from the board, hot air should be applied from the top and bottom heaters. An air nozzle of correct size should be used to conduct the heat to the SOIC component leads such that a vacuum pick up tool can properly remove the component. The temperature setting for the top heater and the bottom heater is dependent on the component rating. Many assembly sites have extensive in-house knowledge on rework, and their experts should be consulted for further guidance.

If the PCB is large, it is important to avoid bending of the printed circuit material due to thermal stress, so a bending prevention tool must be placed on the bottom of the printed circuit board, and a bottom heater installed to allow heating of the entire printed circuit board in order to raise work efficiency.

6.3.3 Site Redressing

After the component is removed, the PCB pads have to be cleaned to remove solder residue in order to prepare for the new component placement. This may be completed by vacuum de-soldering, solder sucker, solder wick braid, etc., after applying flux. Remaining solder residue and projections cause the solder stencil to not adhere closely to the substrate during solder paste printing, leading to improper solder paste supply during component mount.

Moreover, when the solder residue flows all the way to an adjacent through-hole, the solder paste printed on the pad can be transferred, via suction, to the through-hole during reflow, which may cause improper connection. A solvent may be necessary to clean the PCB of flux residue. A de-soldering station can be used for solder dressing. It should be noted that the applied temperature should not exceed 245 °C, which can contribute to PCB pad peeling from the PCB. This is typically a manual operation which is directly attributed to experience and skill.

Non-abrasive or soft bristle brushes should be used as abrasive brushes (e.g. steel brushes) can contribute to bad solder joints. Prior to placing a new component on the site, solder paste should be applied to each PCB pad by printing or dispensing. A no-clean solder paste is recommended.

6.3.4 Solder Paste Printing

Solder supply during rework is done using specialized templates and tools. A mini stencil with the same stencil thickness, aperture opening, and pattern as the normal stencil is placed in the component site. A mini metal squeegee blade deposits solder paste in the specific area. See Figure 20. The printed pad should be inspected to ensure even and sufficient solder paste before component placement.

In situations where neighboring parts are at close proximity with the SOIC components, and the mini stencil method is not an option, apply solder paste carefully on each pad using a paste dispensing system. The volume of solder paste must be controlled in order to prevent shorting on the component and/or neighboring components

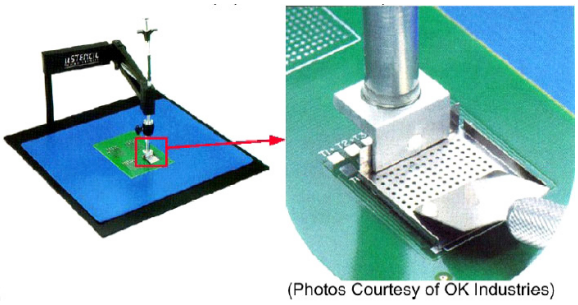


Figure 20. Mini Stencil and Mini Metal Squeegee Blade

6.3.5 Package Remount

After preparing the site, the new package can be placed onto the PCB. Handling of the replacement package should also follow the guidelines of **Section 9.2**. When remounting the package, it is recommended to use rework equipment that has good optical or video vision capability. A split light system displays images of both package leads and PCB pads by superimposing two images. Alignment of the leads and pads is completed with an adjusting XY table.

Regular lead array Package exhibits self-alignment in any direction including X-axis shift, Y-axis shift, and rotational misplacement. Exposed pad may not exhibit a strong self-alignment capability and precise placement of the component on the PCB is required.

6.3.6 Reflow Soldering

The new component is soldered to the PCB using the same temperature profile as the normal reflow soldering process, shown in **Section 5.4**. Reflow furnaces are not typically used for rework. Rather, a dedicated rework station is used that does both part removal and new part joining. During soldering, the package peak temperature and temperature ramps cannot exceed those of the standard assembly reflow process.

In IR or convection processes, the temperature can vary greatly across the PCB depending on the furnace type, size and mass of components, and the location of components on the assembly. Additionally rework stations only apply heat locally, not to the entire PCB. If nozzles are used to direct the heat, the nozzle size must be sufficiently large to encompass the entire part. Profiles must be carefully tested to determine the hottest and coolest points on the assembly. The hottest and coolest points should fall within recommended temperatures in the reflow profile. To evaluate the process, thermocouples must be carefully attached with very small amounts of thermally conductive grease or epoxy directly to the solder joint interface between the package and board.

The materials used in rework do have a higher potential to create conductive paths/corrosion etc. compared to standard materials. The PCB might need to be cleaned if not cleaned in the "normal" process or the rework was not done using "no clean" materials.

7 Board Level Reliability

7.1 Testing Details

Solder Joint Reliability (SJR) testing is performed to determine a measure of board level reliability when exposed to thermal cycling. There are several different names for board-level reliability (BLR) that customers may see. These include: second level reliability (2nd level reliability), solder-joint reliability (SJR), and temperature cycling on board (TCoB).

Information provided here is based on experiments executed on MAPBGA devices using a daisy chain BGA configuration. Actual surface mount process and design optimizations are recommended to develop an application specific solution.

- For automotive grade product applications, the widely accepted temperature range for testing is -40 °C to +125 °C
- Consumer SJR temperature cycling conditions may vary widely, depending on the application and specific user. Typically, Freescale consumer SJR testing is performed from 0 °C to +100 °C

The preferred test method will vary by market and industry. For automotive, the primary test is a version of IPC-9701A, air temperature cycling. For the consumer market, JEDEC's drop test will be the primary test (JESD22-B111). Telecommunications use both IPC-9701A and IPC-9702 (monotonic bend). FSL may not test an electronic package and may not have all the tests for each market and industry.

Table 4 shows the Freescale standard test set-up for performing board level solder joint reliability testing.

Table 4. Board Level Reliability Setup

Board Level Reliability Testing: Material and Test Setup	
PCB Board	• 1.58 mm thickness • Four Cu layers • OSP surface finish
Test Board Assembly	• Pb-free solder paste SAC387 • Reflow peak temperature for SAC assembly ~ 240 °C • Pb solder paste Sn63Pb37 • Reflow peak temperature for SnPb assembly ~ 220 °C • 0.100 mm thickness, Ni plated, laser cut and electro-polished stainless steel stencil

Cycling Conditions	• Continuous in-situ daisy chain monitoring per IPC-9701A and IPC-SM-785
	• Air Temperature Cycling (ATC) for Automotive
	  • -40 °C/+125 °C
	  • 15 minute ramp/15 minute dwell
	  • One hour cycle time
	• Air Temperature Cycling (ATC) for Commercial and Industrial
	  • 0 °C/+100 °C
	  • 10 minute ramp/10 minute dwell
	  • 40 minute cycle time

Package Test Vehicle	• Production BOM package including die (die mechanically present, without wire bond connection) • Daisy chain bond pattern on the leadframe to allow continuos monitoring

7.2 Solder Joint Reliability Results

Freescale experimentally gathers board-level reliability data for a variety of packages. To get results from these experiments (including Weibull plots) contact the Freescale sales team. Customers should interpret the Freescale solder joint reliability data to see how well they meet the final application requirements.

8 Thermal Characteristics

8.1 General Thermal Performance

Since the thermal performance of the package in the final application will depend on a number of factors (i.e. board design, power dissipation of other components on the same board, ambient temperature), the thermal package properties provided by Freescale should only serve as a guideline for the thermal application design. In applications where the thermal performance is considered to be critical, Freescale recommends to run application specific thermal calculations in the design phase to confirm the on-board thermal performance.

Exposed pad packages may require the exposed pad to be connected to the PCB for thermal and/or electrical measurement. For optimized thermal performance, it is recommended to form a thermal pass into the PCB by connecting the exposed pad to the top and/or bottom and/or inner copper layers of the PCB. The PCB copper area and number of thermal vias connected to the exposed pad required to achieve the proper thermal performance on the PCB is application specific and will depend on the package power dissipation and the individual board properties (thermal resistance of the application PCB).

8.2 Package Thermal Characteristics

Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

Additional factors that need be considered in PCB design and thermal rating of the final application amongst others are:

- Thermal resistance of the PCB (thermal conductivity of PCB traces, number of thermal vias, thermal conductivity of thermal vias)
- Quality and size of PCB solder joints (effective PCB pad size, potential solder voiding in the thermal path solder joints that may reduce the effective solder area)

The thermal characteristics of the package provide the thermal performance of the package when there are no nearby components dissipating significant amounts of heat. The stated values are meant to define the package thermal performance in a standardized environment.

Thermal properties of the individual products are usually given in the Freescale product data_sheet as appropriate. Product datasheets are available under www.freescale.com. More detailed thermal properties may be requested by customers.

8.3 Package Thermal Properties—Definition

The thermal performance of a MAPBGA package is typically specified by thermal properties such as $R_{\theta JA}$, $R_{\theta JMA}$, $R_{\theta JB}$, $R_{\theta JC}$ and Ψ_{JT} (in °C/W). Thermal characterization is performed by physical measurement and by performing complex simulation models under the following conditions:

- Two thermal board types:
  - Single-layer board (1s), per JEDEC JESD51-3 and JESD51-5 (exposed pad packages only)
  - Four-layer board (2s2p), per JEDEC JESD51-7 and JESD51-5 (exposed pad packages only)
- Four boundary conditions:
  - Natural convection (still air), per JEDEC JESD51-2
  - Forced convection, per JEDEC JESD51-6
  - Thermal test board on ring style cold plate method, per JEDEC JESD51-8
  - Cold plate method, per MIL SPEC-883 method 1012.1

8.3.1 $R_{\theta JA}$: Theta Junction-to-Ambient Natural Convection (Still Air)

Junction-to-Ambient Natural Convection thermal resistance (Theta-JA or $R_{\theta JA}$ per JEDEC JESD51-2) is a one-dimensional value that measures the conduction of heat from the junction (hottest temperature on die) to the environment (ambient) near the package in a still air environment. The heat generated on the die surface reaches the immediate environment along two paths:

- Convection and radiation from the exposed surface of the package, and
- Conduction into-and-through the test board, followed by convection and radiation off the exposed board surfaces

8.3.2 $R_{\theta JMA}$: Theta Junction-to-Moving-Air Forced Convection

Junction-to-Moving-Air Forced Convection (Theta-JMA or $R_{\theta JMA}$ per JEDEC JESD51-6) is similar to $R_{\theta JA}$, but it measures the thermal performance of the package mounted on the specified thermal test board exposed to a moving air (200 feet/minute) environment.

8.3.3 $R_{\theta JB}$: Theta Junction-to-Board

Junction-to-Board thermal resistance (Theta-JB or $R_{\theta JB}$ per JEDEC JESD51-8) measures the horizontal spreading of heat between the junction and the board. The board temperature is measured on the top surface of the board near the package. The measurement is done using a highly effective thermal conductivity four-layer test board (2s2p) per JEDEC JESD51-7 and JESD51-5 (exposed pad packages only) on a ring style cold plate. $R_{\theta JB}$ is frequently used by customers to create thermal models considering both package and application board thermal properties.

8.3.4 $R_{\theta JC}$: Theta Junction-to-Case

Junction-to-Case thermal resistance (Theta-JC or $R_{\theta JC}$ per MIL SPEC-883 Method 1012.1) indicates the average thermal resistance between the die and the case top surface, as measured by the cold plate method per MIL SPEC-883 Method 1012.1, with the cold plate temperature used for the case temperature. The case is defined as either the temperature at the top of the package (for non-exposed pad packages), or the temperature at the bottom of the exposed pad surface (for exposed pad packages). For exposed pad packages where the pad would be expected to be soldered, junction-to-case thermal resistance is a simulated value from the junction to the exposed pad without contact resistance. $R_{\theta JC}$ can be used to estimate the thermal performance of a package when the board is adhered to a metal housing or heat sink, or when a complete thermal analysis is done.

8.3.5 Ψ_{JT} (Psi JT): Junction-to-Package Top

Junction-to-Package Top (Psi JT or Ψ_{JT}) indicates the temperature difference between the package top and the junction temperature, optionally measured in a still air condition (per JEDEC JESD51-2) or in a forced convection environment (per JEDEC JESD51-6). Ψ_{JT} must not be confused with the parameter $R_{\theta JC}$. $R_{\theta JC}$ is the thermal resistance from the device junction to the external surface of the package, with the package surface held at a constant temperature, while Ψ_{JT} is the value of the temperature difference between the package surface and the junction temperature, usually in natural convection.

8.4 Package Thermal Properties: An Example

Table 5 shows an example of the thermal characteristics typically shown in a Freescale product data sheet. The example applies to a package size SOICW 32LD, Pitch 0.65 mm, Die size ~ 2.410 mm x 2.936 mm.

Table 5. Thermal Parameters of a Package (17.0 mm x 17.0 mm x 1.5 mm)

Rating	Board Type	Thermal Resistance	Value	Unit	Notes
Junction to Ambient (Natural Convection)	Single Layer board (1s)	$R_{\theta JA}$	79	°C/W	(1) (2)
Junction to Ambient (Natural Convection)	Four-layer board (2s2p)	$R_{\theta JA}$	27	°C/W	(1) (2)
Junction to Board		$R_{\theta JB}$	9	°C/W	(3)
Junction to Case (Bottom)		$R_{\theta JC}$	3	°C/W	(4)
Junction to Package Top	Natural Convection	Ψ_{JT}	11	°C/W	(5)

Notes

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and the thermal resistance.
2. Per JEDEC JESD51-2 with natural convection for horizontally oriented board. Board meets JESD51-9 specification for 1s or 2s2p board, respectively.
3. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
4. Thermal resistance between the die and the solder pad on the bottom of the package based on simulation without any interface resistance.
5. Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT

9 Case Outline Drawing, MCDS and MSL Rating

9.1 Case Outline Drawing, MCDS and MSL Information Download

Freescale offers Packaging, Environmental and Compliance information at www.freescale.com in the parametric tables and also in the device information details. Enter the part number in the search box and review the package information details of the specific part.

The complete case outline drawing and the Material Composition Declaration Sheet (MCDS), following the IPC-1752 reporting format, can be downloaded as a PDF file. Information on product specific Moisture Sensitivity Level (MSL) is also available in the part details.

9.2 Moisture Sensitivity Level

The MSL indicates the floor life of the component and its storage conditions and handling precautions after the original container has been opened. The permissible time (from opening the moisture barrier bag until the final soldering process) that a component can remain outside the moisture barrier bag is a measure of the sensitivity of the component to ambient humidity.

In many cases, moisture absorption leads to moisture concentrations in the component that are high enough to damage the package during the reflow process. The expansion of trapped moisture can result in interfacial separation, known as delamination, of the mold compound from the die or lead-frame, wire bond damage, die damage, and internal cracks. In the most severe cases the component will bulge and pop, known as the "popcorn" effect.

Thus it is necessary to dry moisture-sensitive components, to seal them in a moisture barrier antistatic bag with a desiccant and a moisture indicator card which is vacuum sealed according to IPC/JEDEC J-STD-033, and only remove them immediately prior to assembly to the PCB.

Table 6 presents the MSL definitions per IPC/JEDEC J-STD-20. Refer to the "Moisture Sensitivity Caution Label" on the packing material, which contains information about the moisture sensitivity level of Freescale products. Components must be mounted and reflowed within the allowable period of time (floor life out of the bag), and the maximum reflow temperature that shall not be exceeded during board assembly at the customer's facility.

If moisture-sensitive components have been exposed to ambient air for longer than the specified time according to their MSL rating, or the humidity indicator card indicates too much moisture after opening a Moisture Barrier Bag (MBB), the components are required to be baked prior to the assembly process. Refer to imprints/labels on the respective packing to determine allowable maximum temperature.

The higher the MSL value, the more attention is needed to store the components. Freescale packages use JEDEC standard IPC/JEDEC J-STD-020 for classification of packages.

Table 6 depicts the best case MSL for each package size at the time of this document's release. Freescale packages use JEDEC standard IPC/JEDEC J-STD-020 for classification of its packages.

Table 6. MSL Descriptions

Level Rating	Floor Life	
	Time	Conditions
1	Unlimited	30 °C/85% RH
2	1 Year	30 °C/60% RH
2a	4 Weeks	30 °C/60% RH
3	168 Hours	30 °C/60% RH
4	72 Hours	30 °C/60% RH
5	48 Hours	30 °C/60% RH
5a	24 Hours	30 °C/60% RH
6	Time On Label (TOL)	30 °C/60% RH

Table 7. MSL Capability of SOIC Packages

Package Type	Package Body Size (W)	Package Body Size (L)	MSL LEVEL	PPT
SOIC 8N	3.9	4.9	3	260 °C
SOIC 14N	3.9	8.65	3	260 °C
SOIC 16N	3.9	9.9	3	260 °C
SOIC 16W	7.5	10.3	3	260 °C
SOIC 20W	7.5	12.8	3	260 °C
SOIC 24W	7.5	15.4	3	260 °C
SOIC 28W	7.5	17.9	3	260 °C
SOIC 32W	7.5	11	3	260 °C
SOIC 54W	7.5	17.9	3	260 °C

Notes
1.For package availability, please check with sales team

10 Package Handling

10.1 Handling Electrostatic Discharge Sensitive Devices

Semiconductor Integrated Circuits (ICs) and components are Electrostatic Discharge Sensitive devices (ESDS) requiring proper precautions for handling and processing. Electrostatic Discharge (ESD) is one of several significant factors leading to damage and failure of semiconductor ICs and components. Comprehensive ESD controls to protect ESDS during handling and processing must be considered.

The following industry standards describe detailed requirements for proper ESD controls. Freescale recommends users to meet the standards before handling and processing ESDS. Detailed ESD specifications of devices are available in each device data sheet.

- JESD625-A - Requirements for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices
- IEC-61340-5 - Specification for the Protection of Electronic Devices from Electrostatic Phenomena

10.2 Handling Moisture-Sensitive Surface Mount Devices

SOIC's are Moisture/Reflow Sensitive Surface Mount Devices (SMD) requiring proper precautions for handling, packing, shipping and use. Moisture from atmospheric humidity enters permeable packaging materials by diffusion. Assembly processes used to solder SMD packages to PCBs expose the entire package body to temperatures exceeding 200 °C. As noted in **Section 9.2** during solder reflow, the combination of rapid moisture expansion, materials mismatch, and material interface degradation can result in package cracking and/or delamination of critical interfaces within the package. Cracking and/or delamination can lead to failure and reliability a concern Proper handling of SMDs must be obeyed.

Dried Moisture Sensitive SMDs are placed in tray or tape & reel, then dry packed for proper transportation and storage. SMDs are sealed with desiccant material and a Humidity Indicator Card inside of a Moisture-Barrier Bag (MBB). The shelf life of dry packed SMDs are 12 months from the dry pack seal date when stored in < 40 °C/90% RH environment.

Proper use and storage of Moisture Sensitive SMDs are required after MBB is opened. Improper use and storage will increase various quality and reliability risks. SMDs that will be subjected to reflow solder or other high temperature process must be mounted within the period of floor environment specified by MSL, or stored per J-STD-033 standard.

The baking of SMDs is required before mounting if any of following are experienced.

- SMDs are exposed to a specified floor environment greater than specified period
- Humidity Indicator Card shows > 10% for level 2a – 5a, or shows > 60% for level 2 devices when read at 23 °C ± 5.0 °C environment
- SMDs are not stored according to the J-STD-033 standard

The baking procedure, more detailed requirements and procedures of handling moisture-sensitive SMDs can be found in IPC/JEDEC J-STD-033 - Handling, Packing, Shipping and Use of Moisture/Reflow Sensitive Surface Mount Devices.

10.3 Packing of Devices

SOIC devices are contained in tube or tape & reel configuration. The tube and tape & reel are dry packed for transportation and storage. Packing media are designed to protect devices from electrical, mechanical and chemical damages as well as moisture absorption. The proper handling and storage of dry packs is recommended. Improper handling and storage (dropping dry packs, storage exceeding 40 °C/90% RH environment, excessive stacking of dry packs, etc.) will increase various quality and reliability risks.

- Tubes (also commonly referred to as Magazines or Rails):
  - Materials: Shipping tubes shall be manufactured of PVC (Poly Vinyl Chloride) or PS (Polystyrene) or PC (Poly Carbonate) materials dipped in an anti-static solution to provide anti-static capability
  - Freescale's tube designs will fit standard JEDEC package designs. See Figure 21
  - Pin One orientation end: The preferred pin one plug (tube/magazine insertion end) shall be green. IMPORTANT NOTE: If pin one indication is NOT required; then both ends shall be of the same color from one of the following allowed colors: clear, grey, white, and black
  - Opposite Pin One (also referred to as hold or tack or anchor): The preferred color shall be clear, grey, white or black
  - Examples of single and Multiple Tube Packing Configurations are shown in Figure 22 and Figure 23 respectively

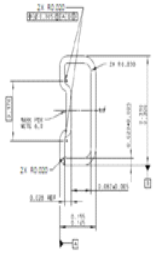
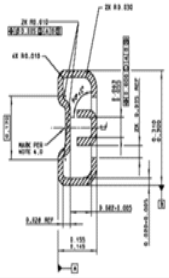
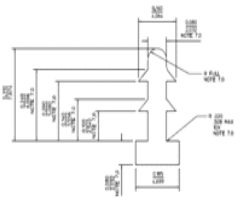
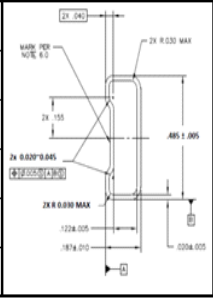
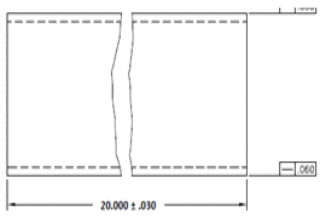
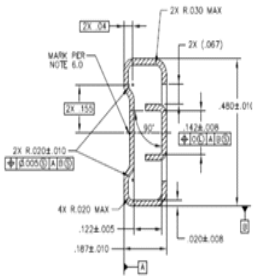
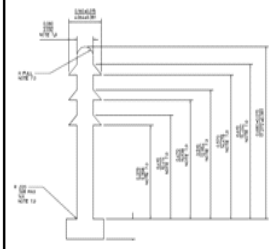
Package Type	Lead Count	Tube Sectional Shape (Entrance)	Tube Length (Inch)	Tube Sectional Shape (End)	Plug Shape and Dimension
SOIC Narrow Body (JEDEC)	SOIC 8N		20 ± 0.020 		
	SOIC 14N				
	SOIC 16N				
SOIC Wide Body (JEDEC)	SOIC 16W		20 ± 0.030 		
	SOIC 20W				
	SOIC 24W				
	SOIC 28W				
	SOIC 32W				
	SOIC 54W				

Figure 21. JEDEC Tube Example

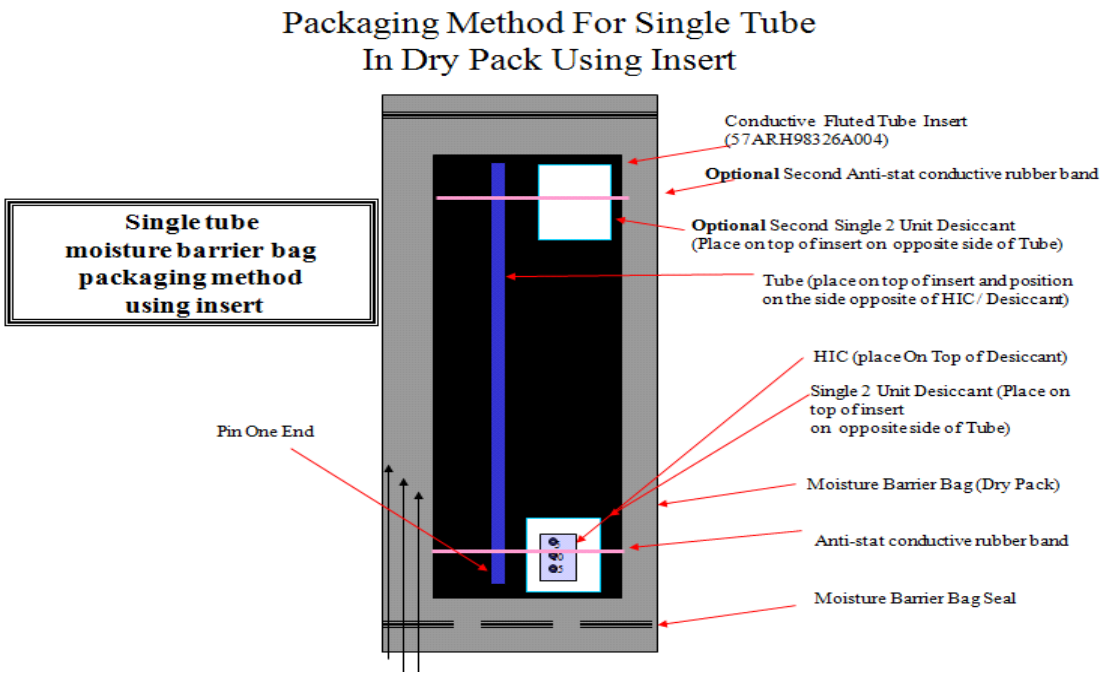


Figure 22. Sample of Single Tube Packing Method

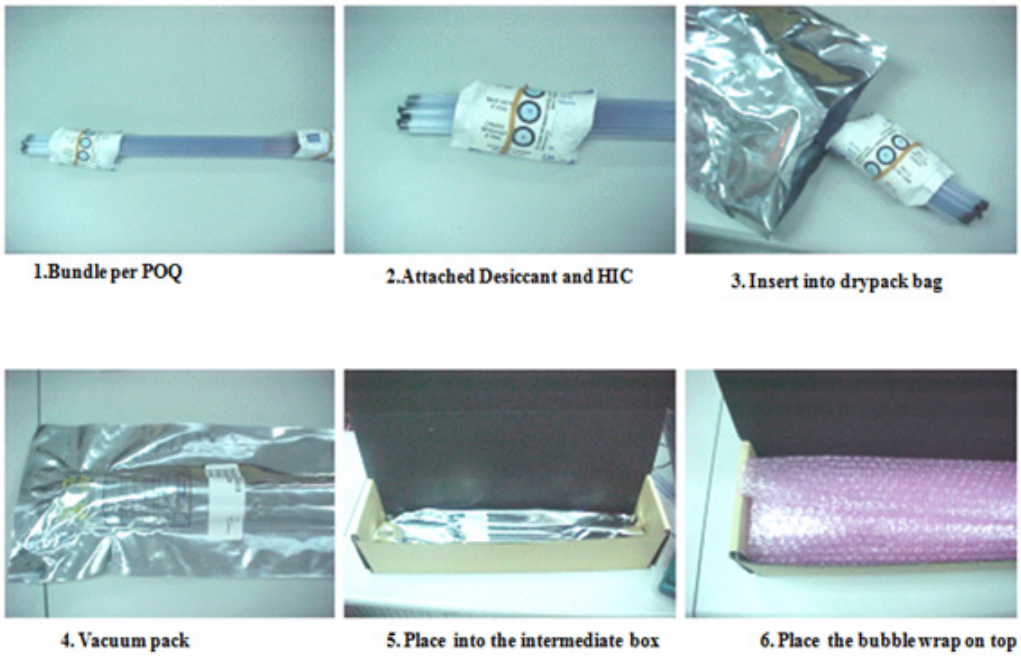


Figure 23. Sample of Multiple Tube Packing Method

- Tape & Reel:
  - — Freescale complies with EIA-481D for carrier tape & reel configuration and orientation. See Figure 24
  - — Tape & reels are NOT designed to be baked at high temperatures
  - — Each tape & reel is typically dry packed in a moisture barrier bag

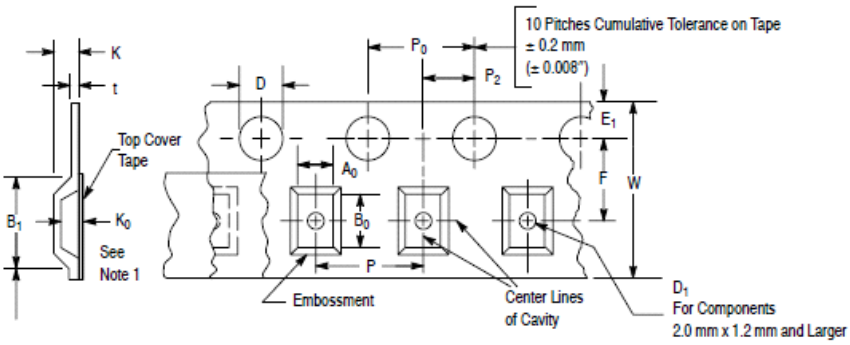


Figure 24. Carrier Tape Specifications

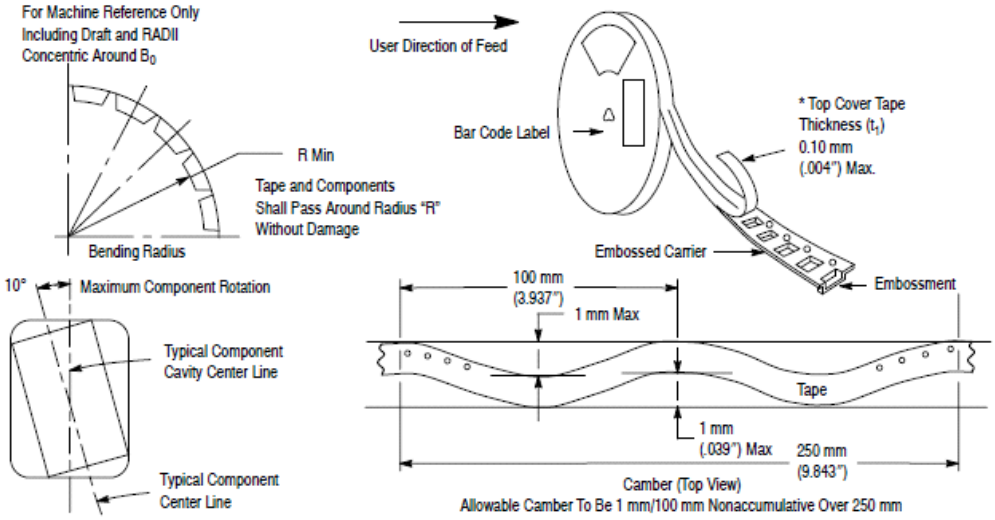


Figure 25. Tape & Reel Example

- Dry Packing:
  - Tube and tape & reels, loaded with devices, are sealed in a moisture barrier bag which is labeled and packed in dedicated boxes with dunnage for the final shipment
  - Each dry pack bag contains a desiccant pouch as well as a humidity indicator card
  - Freescale encourages the recycling and reuse of materials whenever possible
  - Freescale will not use packing media items processed with or containing class 1 Ozone Depleting Substances
  - Whenever possible, Freescale shall design its packing configurations to optimize volumetric efficiency and package density to minimize the amount of packing material entering the industrial waste stream

Freescale complies with following Environmental Standards Conformance guidelines/directives:

- ISPM 15, Guidelines for Regulating Wood Packaging Material in International Trade
- European Parliament and Council Directive 94/62/EC of 20 December 1994, packaging and packaging waste

11 References

[1] IPC/JEDEC J-STD-020, Moisture/Reflow Sensitivity Classification for Non-hermetic Solid State Surface Mount Devices, July 2004.

[2] IPC/JEDEC J-STD-033, Joint IPC/JEDEC Standard for handling, packing, shipping, and use of moisture/reflow sensitive surface-mount devices, February 2012

[3] EIA-783, Guideline Orientation Standard for Multi-Connection Package (Design Rules for Tape and Reel Orientation), November 1998.

[4] EIA/JESD51-2, Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air), December 1995.

[5] EIA/JESD51-8, Integrated Circuit Thermal Test Method Environmental Conditions - Junction-to-Board, October 1999.

[6] EIA/JESD 51-6, Integrated Circuits Thermal Test Method Environment Conditions - Forced Convection (Moving Air), March 1999.

[7] MIL SPEC-883 Method 1012.1, Thermal characteristics, February 2006.

[8] IPC-7351B, Generic Requirements for Surface Mount Design and Land Pattern Standards, June 2010.

[9]IPC-9701A, Performance Test Methods and Qualification Requirements for Surface Mount Solder Attachments, February 2006.

[10] IPC/JEDEC-9702, Monotonic Bend Characterization of Board-Level Interconnects, June 2004.

[11] IPC-SM-785, Guidelines for Accelerated Reliability Testing of Surface Mount Solder Attachments, November 1992.

[12] JESD22-B111, Board Level Drop Test Method of Components for Handheld Electronic Products, July 2003.

[13] IPC-1752, Materials Declaration Management, June 2005.

[14] EIA-481, Standards - Excerpts used to assure complete alignment.

[15] JESD615-A, Requirements for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices.

[16] IEC-101/61340-5, Specification for the Protection of Electronic Devices from Electrostatic Phenomena.

12 Revision History

Revision	Date	Description
3.0	9/2014	• Complete document update
	10/2014	• Edited Table 3 in Section 4.2.1

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