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Exploration on Power Delay Product of Basic Logic Gates for Various CMOS Logic Styles

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Abstract

Since Power dissipation is one of the important criteria in Low power VLSI design, Chip designers are making lot of efforts to reduce the power dissipation. The power efficiency of any architecture can be explained in terms of power delay product. The circuit which has less PDP is the optimized design. Therefore it is necessary to find the low power CMOS logic design styles for the basic logic gates. The methodology adopted for designing the basic logic gates are CMOS complementary logic, Pseudo nMOS logic, Dynamic CMOS logic styles. The basic logic gates taken for analysis are inverter, NAND and NOR gates. These various logic styles are designed in Cadence Virtuoso ADE L Schematic Editor environment and the technology was chosen as 180nm technology. The power delay product for dynamic CMOS logic inverter, NAND, NOR is found to be 51.35%, 62.81%, 32.4% respectively lesser when compared to the conventional CMOS logic. So out of three proposed three logic styles dynamic CMOS logic styles shows better power delay product.

Keywords: Complementary static CMOS logic, Pseudo nMOS logic, dynamic CMOS logic

1.0 INTRODUCTION :

In many situations, the area taken by a complementary CMOS logic will be larger than that required one and also the speed may be too low. In such cases, it is

necessary to realize less denser and faster gates at the cost of increased design complexity and reduced operational margin. Also scaling of technology increases power density more than expected. Since Power dissipation is one of the most important criteria for battery powered applications. Design Engineers are giving utmost importance to reduce the power dissipation. The power efficiency of architecture can be visualized in terms of power delay product. The circuit which has less PDP is the optimized design. Therefore it is necessary to find the low power CMOS logic design styles for the basic logic gates. The methodology adopted for designing the basic logic gates are CMOS complementary logic, Pseudo nMOS logic, Dynamic CMOS logic styles. The basic logic gates taken for analysis are inverter, NAND and NOR gates.

2.0 CONVENTIONAL STATIC CMOS LOGIC AND CIRCUITS (INVERTER, NAND AND NOR):

Static CMOS complementary logic is the basic style. This logic has pull down n transistor and pull up P transistor. Pull up transistor is connected to Vdd and pull down transistor is connected to Vss. Static CMOS logic is complementary in nature. That means out of two transistor, one transistor will conducts at a time , either pull up or pull down. The basic logic gates taken for analysis are inverter, NAND ,NOR gates. These three logic gates are designed in static CMOS logic style. The static CMOS circuits for inverter, NAND, NOR gate are shown in Figure 1,2,3 respectively.

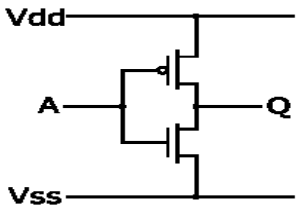

Figure 1: Static logic CMOS inverter

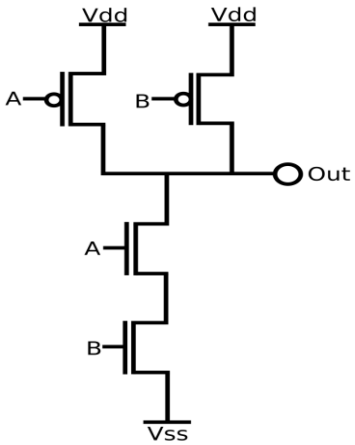

Figure 2: CMOS NAND gate

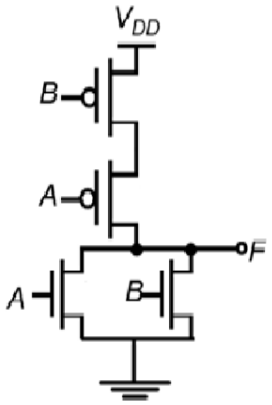

Figure 3: CMOS NOR gate

The functionality of the design are verified with the waveforms and the truthtable. The truth table of the inverter , NAND , NOR is shown in the Table 1,2,3 respectively.

Table 1: Inverter

Input	Output
0	1
1	0

Table 2: NAND gate

Input 1	Input 2	Output
0	0	1
0	1	1
1	0	1
1	1	0

Table 3: NOR gate:

Input 1	Input 2	Output
0	0	1
0	1	0
1	0	0
1	1	0

3.0 MATERIALS AND METHODS:

A) Pseudo nMOS logic and circuits(Inverter, Nand and Nor):

Pseudo nmos is nothing but it has a nMOS pull down transistor and PMOS pull up transistor which has the gate terminal grounded to Vss. Here the pMOS transistor is always turned on because the input of the PMOS gate is connected to low level. Pseudo nMOS inverter, NAND, NOR gate is shown in Figure 4

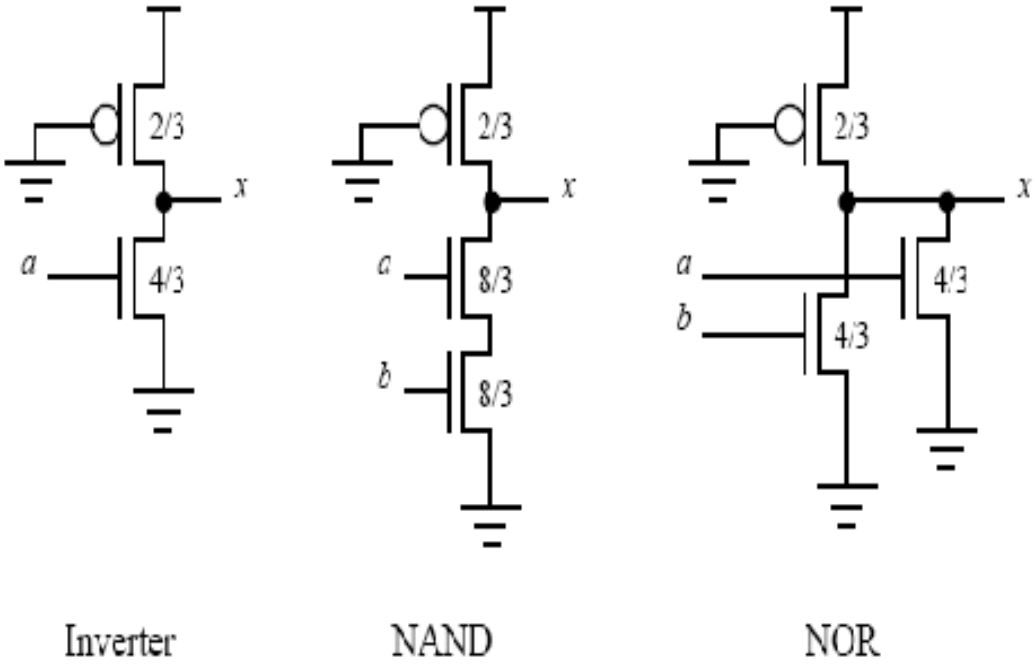

Figure 4: Pseudo nMOS circuits for inverter, NAND, NOR gate

B) Dynamic CMOS Logic and circuits(Inverter, NAND and NOR):

Dynamic CMOS logic circuit consists of pull down n logic and pull up PMOS transistor which is connected to CLK signal. In this dynamic CMOS logic, two types of phases are occurring which is precharge phase and evaluation phase. When the Clock signal is equal to zero, precharge phase occurs which means the output is connected to VDD. It is necessary to provide all the inputs during precharge phase. During precharge phase, the output is precharged to Vdd. When the clock signal becomes one, then evaluation phase starts.The nMOS logic block is evaluated during When Clock signal is high. The dynamic CMOS logic for inverter, NAND, NOR is shown in Figure5, Figure 6, Figure 7 respectively.

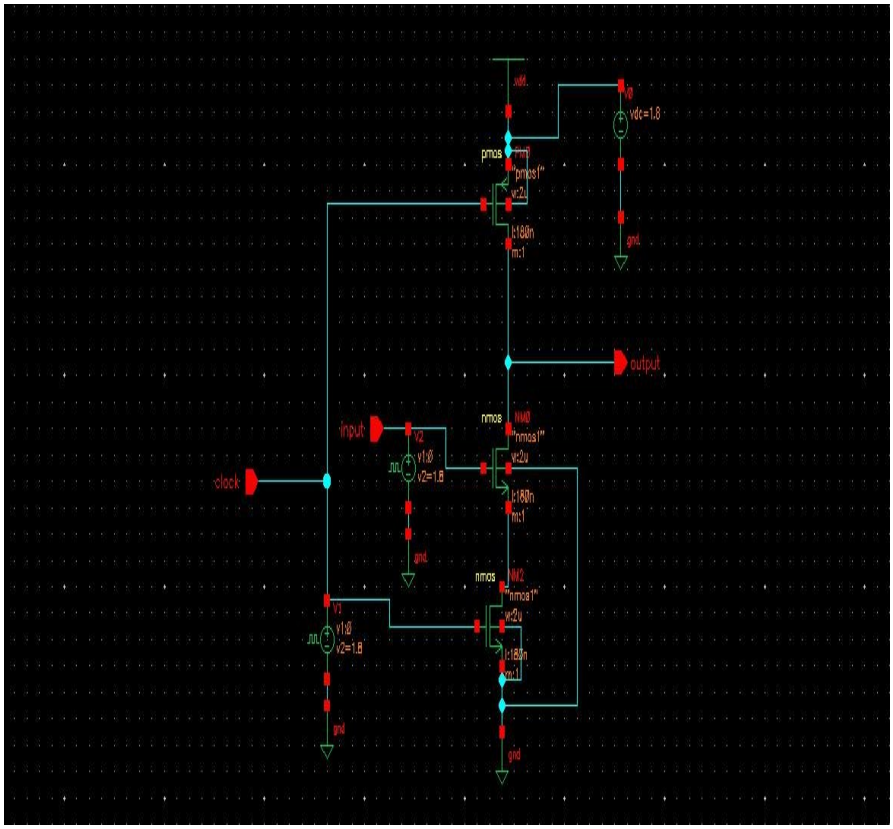

Figure 5: Dynamic CMOS logic inverter

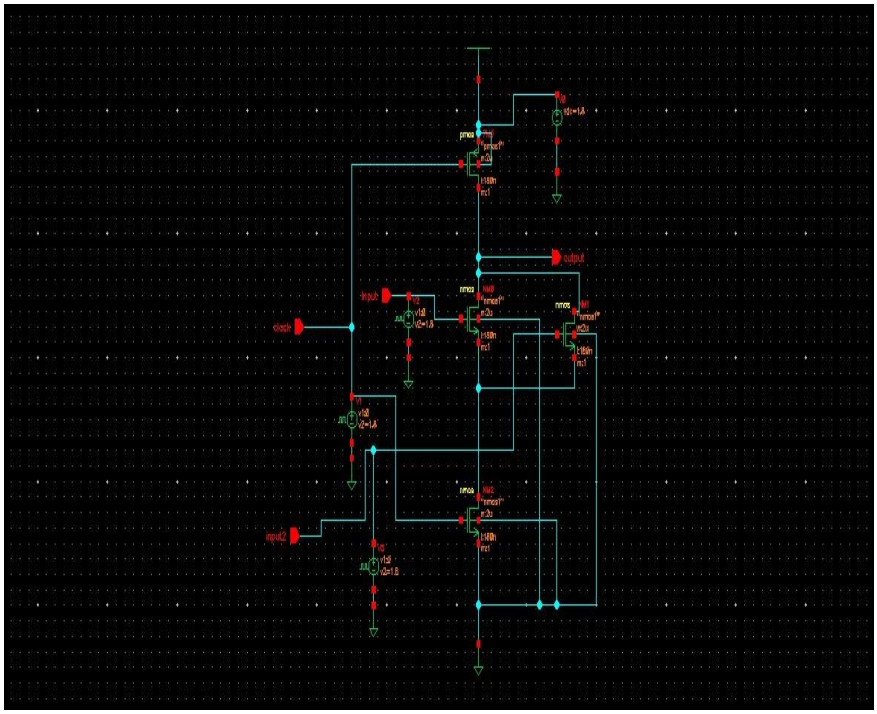

Figure 6: Dynamic CMOS NAND logic

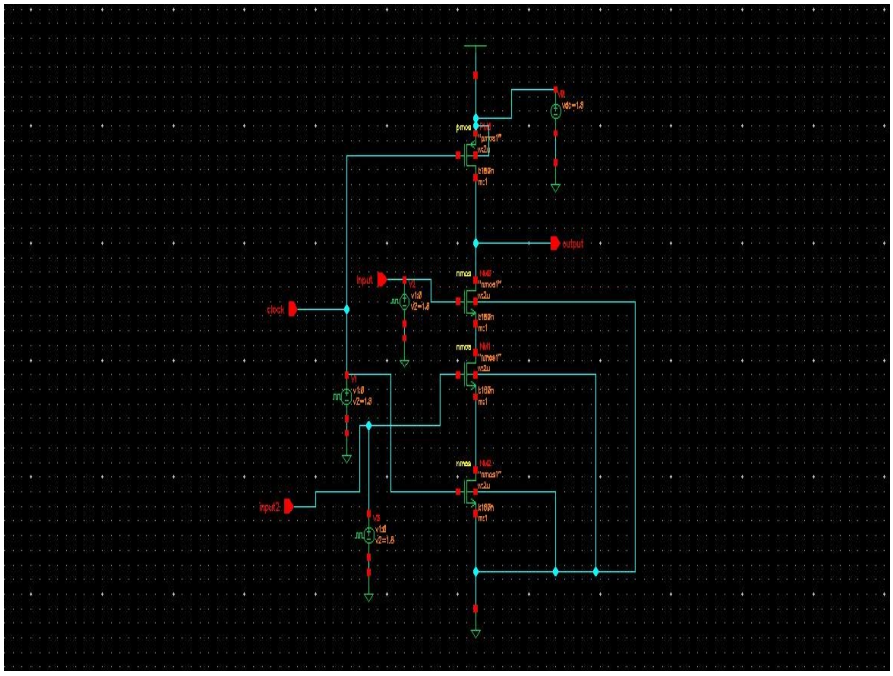

Figure 7: Dynamic CMOS NOR logic:

4.0 RESULTS AND DISCUSSIONS:

The inverter, NAND and NOR gate are simulated in three logic styles such as static CMOS logic , pseudo nMOS logic and dynamic CMOS logic. The circuit is simulated in Cadence Virtuoso ADE L Schematic Editor environment and the power and the delay are analysed. The simulation waveform for dynamic CMOS logic inverter, NOR, NAND gate is shown in Figure 8, Figure 9, Figure 10 respectively.

Figure 8: Inverter dynamic CMOS logic

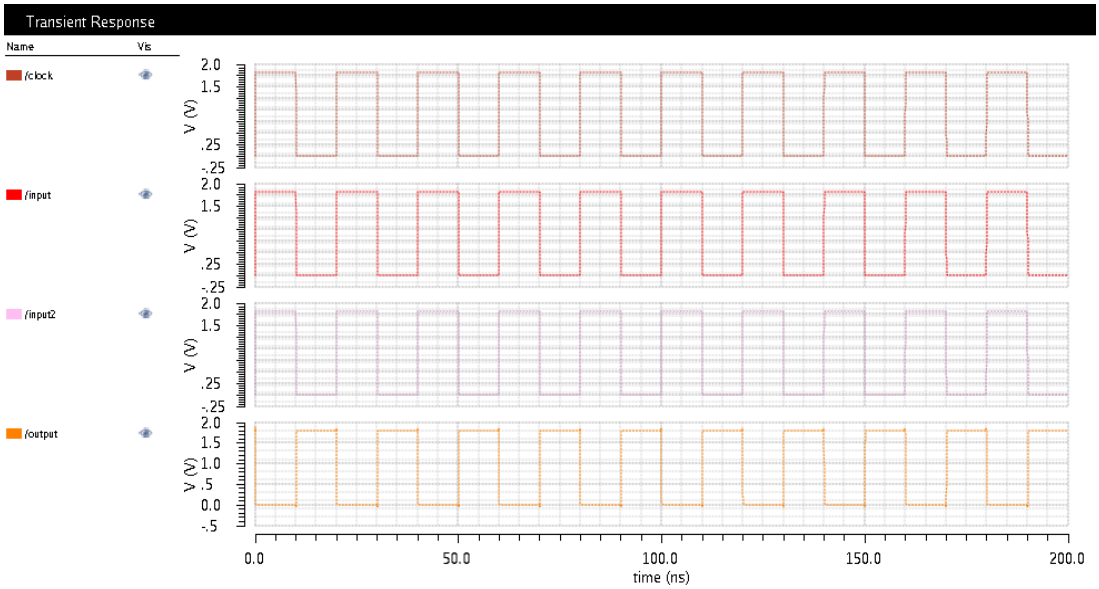

Figure 9: NOR gate dynamic CMOS gate

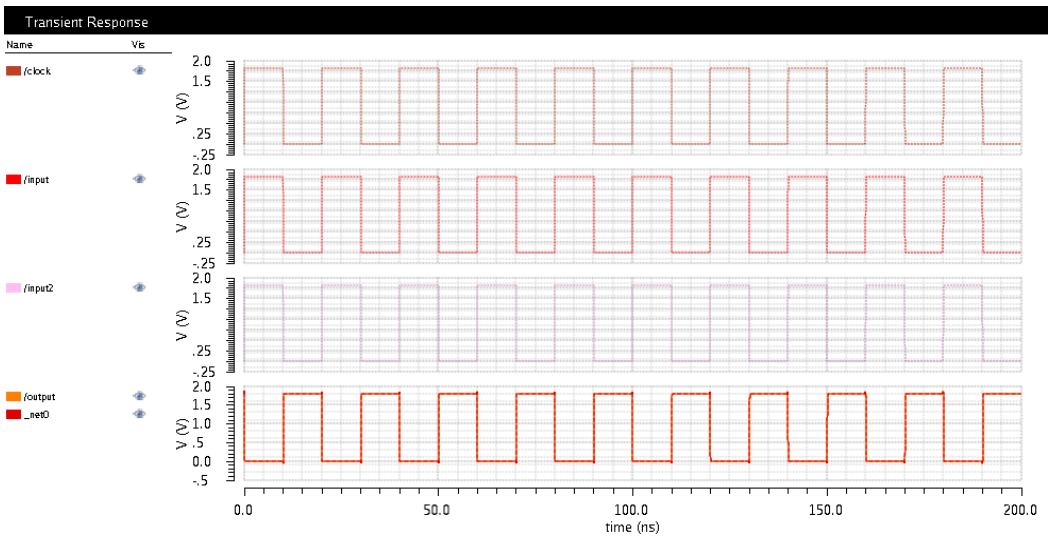

Figure 10: NAND gate dynamic CMOS gate

To find the average power, go the output waveform window, click the output waveform, then go to Tools ----> Calculator, a window will pop up. Then go to the special functions----->average power----->.then click the Evaluate buffer, and then average power can be displayed.

To find the delay, go to the output waveform window, click the input waveform and then go to Tools ----> Calculator, a window will pop up . Then go to the special functions----->delay ----->.then delay function panel will be displayed. In that signal 1 equation will be available since we are in the input wave form. To get the signal 2

equation, once again go to the output waveform window and click the output waveform, and then go to the special function delay panel copy the output wave form equation and paste it in the delay panel .The threshold voltage set for signal 1 is 0.9 Volt and for signal 2 is 0.9 volt. After set out all the parameters, click the evaluate buffer, then delay of the circuit is displayed.

The performance analysis of basic logic gates under different CMOS logic styles is shown in Table : 4

Table 4: Performance analysis of basic logic gates under different CMOS logic styles

Logic Styles	Inverter		NAND gate		NOR gate	
	Power dissipation	delay	Power dissipation	delay	Power dissipation	delay
Static CMOS complementary logic	909.0E-3	25.99E-12	1.334	29.55E-12	444.3E-3	50E-12
Pseudo nMOS logic	968.5E-3	24.8E-12	1.421	36.92E-12	888.8E-3	27.8E-12
Dynamic CMOS logic	888.9E-3	13.65E-12	890.3E-3	27.8E-12	538.2E-3	13.4E-12

In certain cases, power dissipation will be reduced delay at the cost of increase in delay. Here in CMOS VLSI circuits, there will be a tradeoff between power dissipation and delay. But the power efficiency of the VLSI circuits can be expressed in terms of power delay product. The circuit which has less power delay product is considered as the best design because that circuit only has less power dissipation and less delay.

The power delay product of basic logic gates under different CMOS logic styles is shown in Table 5. The power delay product is nothing but the product of power dissipation and delay. The circuit which has less power delay product is the optimized design. The experimental result shows that dynamic CMOS logic is better in giving less power delay product.

Table 5: Power delay product of basic logic gates under different CMOS logic styles

Logic styles	**Power Delay Product**		
	Inverter	NAND	NOR
Static CMOS complementary logic	23.624E-18	39.42E-12	22.21E-18
Pseudo nMOS logic	24.01E-18	52.46E-12	24.70E-18
Dynamic CMOS logic	12.13E-18	24.75E-18	7.21E-18

Out of three comparisons, Pseudo nMOS logic is having more power delay product. The reason for having more PDP is that the PMOS transistor in pseudo nMOS logic is always grounded. It means that the PMOS transistor is always switched on. Due to that power dissipation is more in Pseudo nMOS logic. In Static CMOS logic, both nMOS and PMOS are complementary in nature. Since number of transistors is more in static CMOS logic, there is more switching activity which causes more power dissipation. In dynamic CMOS logic, during when CLK is low level the PMOS transistor is precharged to Vdd. At the same time we are providing all the inputs to n logic block of the transistor. So that during the period when CLK is high evaluation phase starts so that unnecessary transition is avoided during the on period of the transistor. Because of avoiding unnecessary transitions in dynamic CMOS logic, power delay product is reduced.

5.0 FUTURE SCOPE:

The circuits like half adder, full adder and multiplexer can be implemented in various CMOS logic styles such as static CMOS logic styles, Pseudo nMOS logic, Dynamic CMOS logic.The power, delay and power delay product can be analysed.

6.0 CONCLUSION:

Power dissipation and delay are the major criteria in modern CMOS VLSI circuits.In this paper, the power and delay of the basic logic gates using static CMOS logic, Pseudo nMOS logic and dynamic CMOS logic are analyzed and the results are tabulated. The power delay product for dynamic CMOS logic inverter, NAND, NOR is found to be 51.35%, 62.81%, 32.4% respectively lesser when compared to static CMOS complementary logic. And also the power delay product for dynamic CMOS logic inverter, NAND, NOR is found to be 50.2%, 47.17%, 29.19% respectively lesser when compared to pseudo nMOS logic. Therefore experimental results shows that dynamic CMOS logic is better in giving less power delay product when compared to static CMOS logic and Pseudo nMOS logic. Since during when the period, Clock is low, all the inputs have applied to the transistor, so unnecessary transitions of the transistor are avoided during the on period of the clock. Due to this, Power dissipation and delay is reduced .And as a result power delay product is also reduced. Finally it is recommended that dynamic CMOS logic may be employed in places wherever power delay product is a major concern.

7.0 REFERENCES

[1] Neil H.E Weste, Kamran Eshragian, Principles of CMOS VLSI design, A systems Perspective, 2nd Edition.Pearson Education.

[2] Kamran Eshraghian, Dougles A.Pucknell,Sholeh Eshraghian(2005), Essentials of VLSI circuits and systems,PHI,New Delhi.

[3] John. P. Uyemura(2011),Introduction to VLSI circuits and systems,John Wiley, India

[4] Cadence Virtuoso tutorial. website: http://wiki.usgroup.eu/wiki/public/tutorials/fullcustomvirtuosoic6. Date Accessed 17.6.2016

[5] Preetisudha Meher, KamalakKanta Mahapatra ,"A modification in CMOS dynamic logic style: A review paper", Journal of the Institution of Engineers (India): Series B December 2015, volume 96, Issue 4, PP 391-399.

[6] M.Shoji," FET scaling in domino CMOS gates,"IEEE Journal of Solid state Circuits, vol.SC-20, no.5, Oct. 1985, pp.1067-1071.

[7] Bernhard Hoppe, Gerd Nevendorf, Doris Schmitt-Landsiedel, and Will Specks, "Optimization of high-speed CMOS logic circuits with analytical models fo signal delay, chip area and dynamic power dissipation," IEEE transactions on Computer-Aided design, vol.9, no.3, Mar.1990, pp.236-247.

[8] Chih-Liang Chen,"2.5 V bipolar /CMOS circuits for 0.25 μm BICMOS technology," IEEE JSSC, Vol.27, no.4, April 1992, pp.485-491.