TELVENT

LANDAC II Operation & Maintenance Manual

B1577-AAA-00 V0.0

Telvent
10333 Southport Dr. S.W.
Calgary, AB, Canada T2W 3X6

Phone: +1 (403)253.8848
Fax: +1 (403)259.2926
E-mail: info.canada@telvent.abengoa.com

Telvent
7000A Hollister Rd.
Houston, TX 77040-5337

Phone: +1 (713)939.9399
Fax: +1 (713)939.0393
E-mail: info.usa@telvent.abengoa.com

LANDAC II Operation & Maintenance Manual

For Reference Only

Document Approval

Rev	Date	Description	Approved	Approved
0.0	06-13-11	Initial Release	01-JUL-2011 Dan Stark, RTU Software Manager	7/1/11 Garry Macejewski, RTU Engineering Manager

Table of Contents

List of Figures

List of Tables

CHAPTER 1

Introduction

This user manual describes the operation and maintenance of the Telvent LANDAC II Substation Automation Platform.

1.1 General Functions

The LANDAC II was designed in order to prolong the life of existing LANDAC RTUs originally supplied to Commonwealth Edison beginning in 1989 and continuing over a three year period. The LANDAC II completely replaces the original LANDAC card cage including the Cluster Controller (CC), Field Interface Modules (FIMs) and Power Supply. In this redesign, several new features were implemented that assures the design will be technologically current for several years to come. The LANDAC II utilizes the latest Sage CPU (C3414) available from Telvent which supports two Ethernet Ports with independent NICs as well as the latest version of VxWorks. Compared to the original LANDAC, the LANDAC II is designed to be very IED communications intensive which is evidenced by its sixteen (16) serial communications channels and it's sixteen (16) configurable Ethernet Sockets. In order to support the multitude of possible IEDs, the LANDAC II utilizes a Web based User Interface and supports totally independent point maps for each of the configured Host interfaces. In addition to the enhanced communications capabilities, several Applications and Logging functions are designed into the LANDAC II as well.

Configuration

Equipped with a powerful browser based user-interface, its user-friendly configuration tools allow it to manage data with simple and intuitive click, drag and drop procedures. There is no special software to load or keep track of. The only requirement is a PC with Internet Explorer® version 6.0 or higher. Configuration tools include features for auto-configuration and the ability to build custom templates for standard configurations making it easy to integrate IEDs with the data set you desire. Other features make analog scaling both powerful and flexible, eliminating the headaches of mapping data with different resolutions and scaling factors to the same port.

The LANDAC II includes Telvent's entire protocol library enabling it to talk to a wide range of IEDs and master stations without added costs and without limitations (i.e., any comm. port can be configured by the user to talk any available protocol).

Communications

The LANDAC II has sixteen (16) RS232 communications ports complete with LEDs for positive visual indication of data activity, five Ethernet ports (two NICs) and a separate port for an external Dial-up modem, making it a compact yet powerful communications platform. In addition, the LANDAC II supports up to 480 Digital Inputs and 192 T/C Momentary or Latching Controls for picking up I/O points not available from IEDs. Built specifically with relay integration in mind, the LANDAC II has features that allow for pass thru connections from either the Ethernet or Dial-up port to any other port. Precision timing can be provided via GPS receiver or IRIG-B signals and bussed to all the serial ports.

Computation

In addition to its communications capabilities, the LANDAC II is equipped with a powerful CPU and plenty of memory for running automation applications. Every LANDAC II includes an IEC 61131 compliant Programmable Logic Controller runtime engine, which allows the user to build custom closed-loop logic algorithms for everything from simple "if-then" operations to sophisticated auto-sectionalizing schemes.

Climate

The LANDAC II meets or exceeds the requirements for survival in the harsh electrical environment of a utility substation. Based on field proven technology, the LANDAC II is tested against IEEE and ANSI surge withstand and fast transient specifications. It comes in a rugged metal enclosure intended for mounting into a standard 19-inch rack or relay panel. Power options include standard 125 VDC / 120 VAC and 20-60 VDC input power sources. The LANDAC II is specifically designed to make integrating IEDs in an electrical substation simple, secure, and ready for the next wave of substation automation applications.

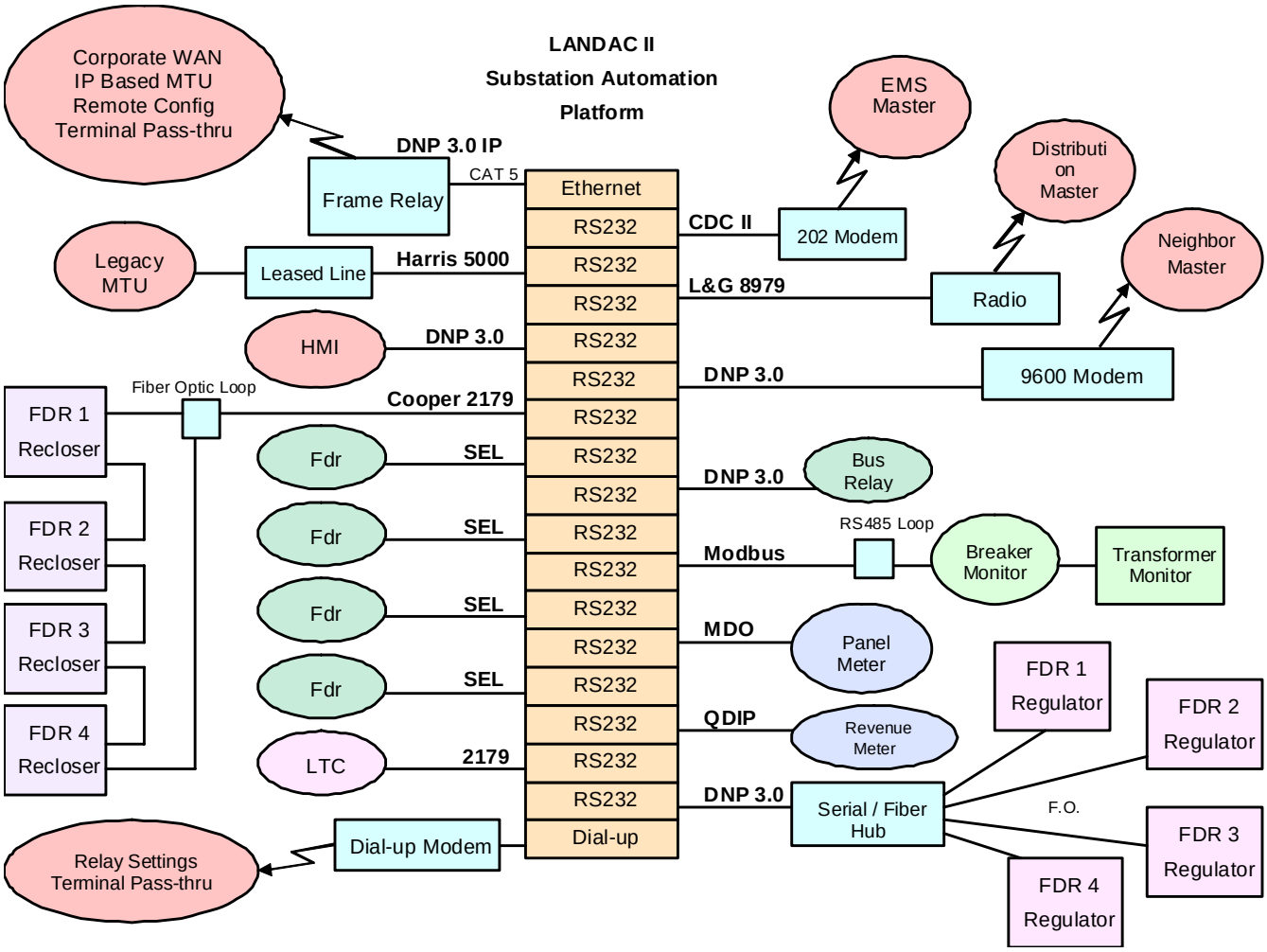
General Operational Considerations

Note: The initial setup is for a Username of "Admin" and a Password of "Telvent1!"

Note: With the release of firmware C0 and later, the initial TCP/IP address is now 172.18.150.50.

Figure 1-1 shows the LANDAC II with a broad range of devices, communications mediums and protocols. While not necessarily a configuration one might design on purpose, it shows the power of the LANDAC II and the possibilities it brings to the table. Most utilities have a wide range of new and legacy devices that need to be pulled together to form a functioning system. The LANDAC II meets the challenge without closing the door to future advancements. The LANDAC II is the perfect platform to pull everything together while leaving a clear and easy migration path into the future.

Figure 1-1 Substation Integration



The Theory of Operation chapter should be used in conjunction with the schematics and printed circuit assembly drawings. The drawings also include bills of material for those users wishing to perform component level repair of failed assemblies.

Figure 1-2 LANDAC II

Figure 1-3 LANDAC II Front View

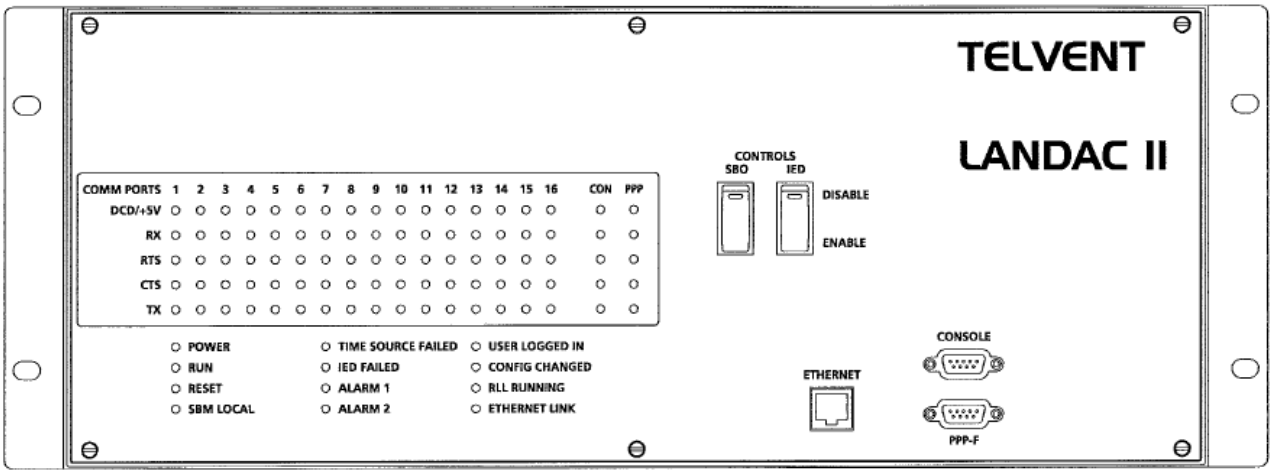
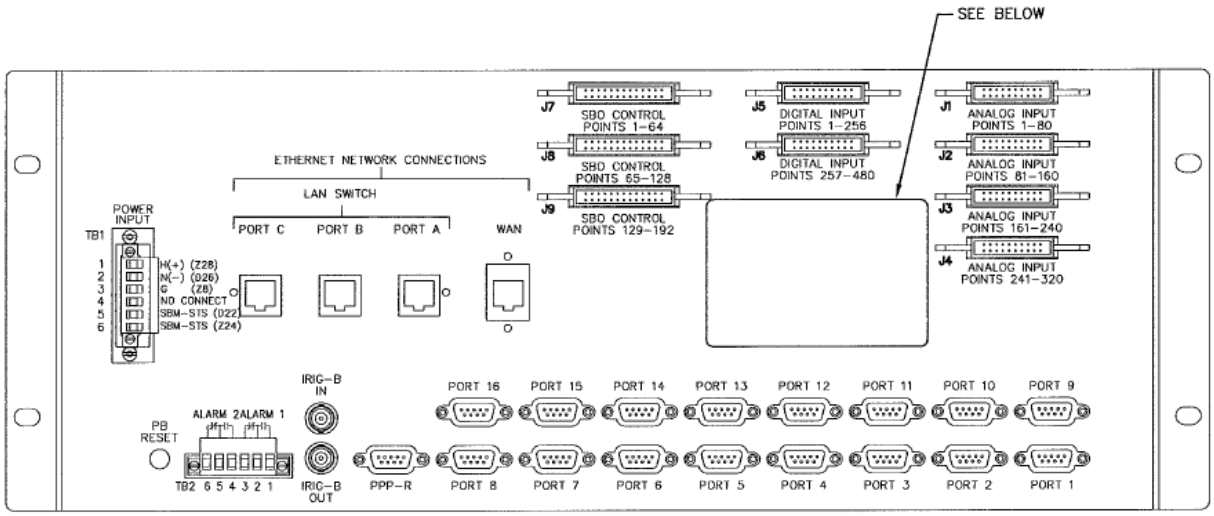
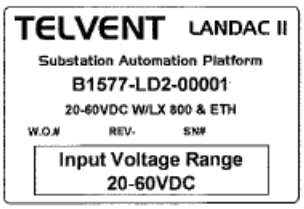


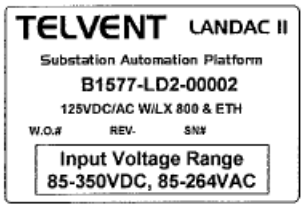
Figure 1-4 LANDAC II Rear View



LABEL DETAIL
(SEE NOTE 5)



LABEL - A



LABEL - B

1.2 Rear Panel Functions

Power Input

This is the power input according to the variance for the particular LANDAC II. The choices at time of purchase are: 85-350VDC and 85-264VAC universal supply, or 20-60VDC.

Analog Input Expansion

Using 4 Analog Input Expansion ports and 5 XT boards per bus, up to 320 analog points.

Digital Input Expansion

Using 2 Digital Input Expansion ports with 8 XT boards on bus 1 (J5) and 7 XT boards on bus 2 (J6), up to 480 status points or Form A accumulators (240 Form C accumulators).

SBO Control Expansion

Using 3 SBO Control Expansion ports and 8 XT boards per bus, up to 192 SBOs.

PB Reset

Push Button Reset.

Alarm 1 & 2 Output

Form C outputs for Alarms.

IRIG-B In & IRIG-B Out

IRG-B input and output are available from these two ports.

PPP-R

Point to Point Protocol connector. The –R simply means Rear panel. There is also a front panel PPP port connected in parallel.

LAN

Three ports for Switched Ethernet. The main Ethernet port is on the front panel.

WAN

The port for the secondary Ethernet port.

Ports 1 Through 16

Sixteen serial ports for communications with IEDs and/or masters.

1.3 Features

The LANDAC II uses the latest electronic technology for reliability, speed and maintainability. It is intended for use where limited on-board I/O is acceptable, yet is capable of polling a wide variety of IEDs or other devices.

The LANDAC II has the following new features:

- Web Browser "UIF" User InterFace configuration tool, uses Internet Explorer 6.0 (no proprietary software required)
- Full MTU / IED Protocol Library Standard
- 2 Built-in 10/100 MB Ethernet Ports
- 16 Built-in RS232 Communications Ports
- Dedicated User Configuration Port
- Dedicated Serial Dial-up Port
- Over 100 LEDs for positive visual indications:

  Power, Run, Reset, SBM Local, Time Source Failed, IED Failed, User Logged IN,

  Config Changed, RLL Running, Ethernet Link, Alarms 1 & 2

  Communications LEDs (RX, TX, RTS, CTS, and DCD/+5V on each port)
- Continuous IRIG-B output with built-in bus to all comm. ports for IRIG-B, GPS, RTC, or Protocol time synchronization

- Wide range input power supply for standard Substation voltages
- Rugged relay style metal enclosure for easy mounting
- PC/104 Bus Architecture
- Designed specifically for Electric Utility Applications (Meets IEEE 472, ANSI C37.90 SWC & C37.90.1 standards)
- Internal 3 Port Ethernet Switch
- External Digital & Analog Inputs and SBO Control Output points

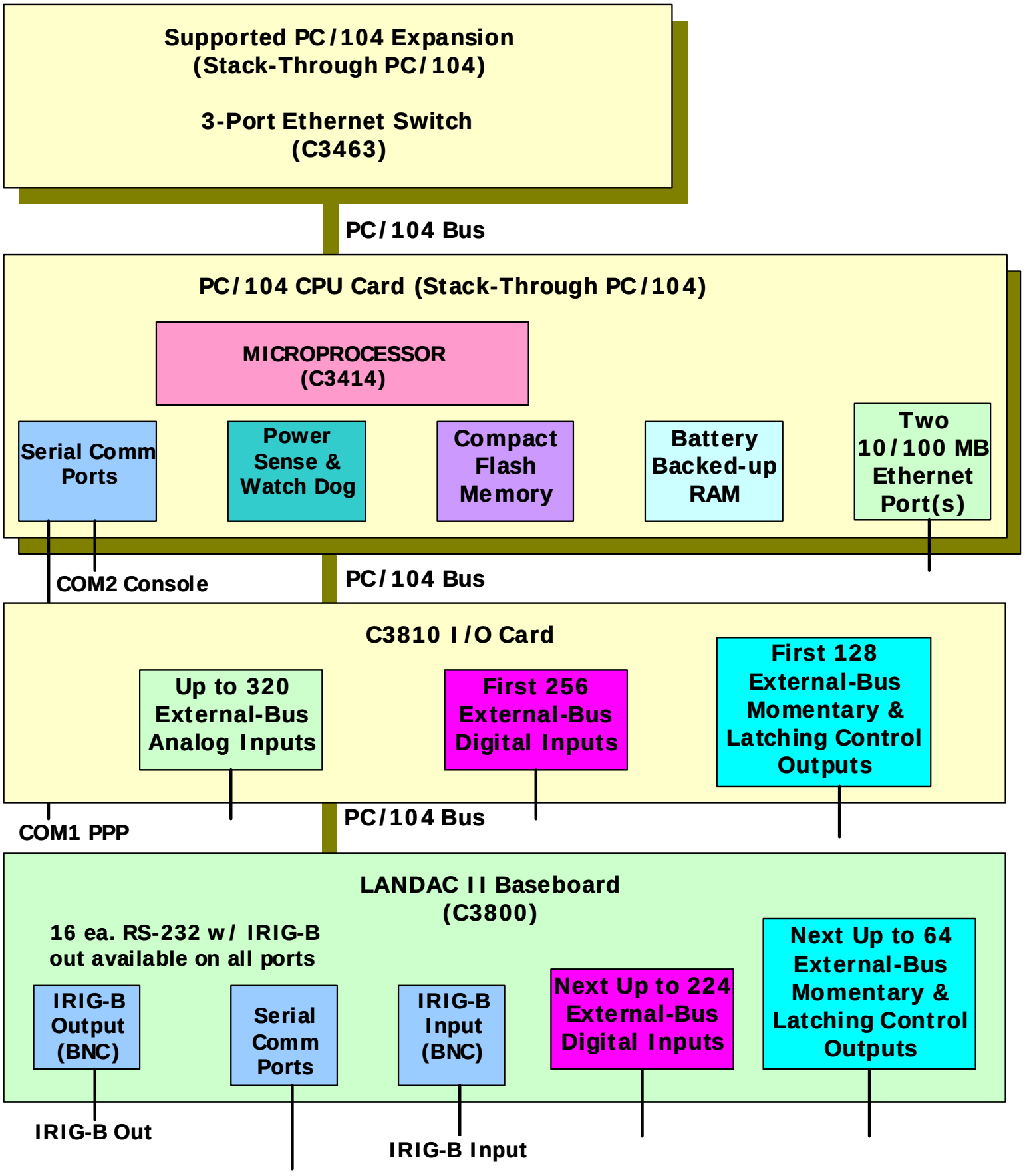
  Up to 480 Digital or 240 Accumulators Inputs

  Up to 320 Analog Inputs

  Up to 192 T/C Momentary and Latching Control Outputs

1.4 Architecture

The Figure below shows a simplified block diagram of the LANDAC II Baseboard that illustrates its general architecture and major components. The basic LANDAC II consists of a baseboard, a microprocessor daughter board, a 3-port Ethernet Switch and a C3810 I/O board.



1.5 Graphical User Interface (GUI)

The LANDAC II is easily configured using the standard web browser, Internet Explorer version 6.0 or later. The physical connection may be made in one of four ways:

- Ethernet connection using an Ethernet crossover cable directly to the front panel Ethernet port
- Ethernet connection to a network, locally or remotely
- PPP connection using a null-modem cable to the PPP-F or PPP-R port
- Console – this method commonly used to read and/or change IP address

See Appendices D and E in the config@WEB Software Users Guide for details on connections.

The GUI is designed around the classical client/server model. A web browser is all you need for your client (PC) and you can browse any Device product or any version of that product that supports our web interface. All configuration data is stored on the LANDAC II in the form of Extensible Markup Language (XML). XML data is served up to the browser within HTML pages or transformed into HTML via Extensible Stylesheet Language (XSL). In either case data is presented to the user in an intuitive format using common design elements like forms, Radio Buttons, Spin Boxes, Alert Boxes, etc. for much of the data entry.

The GUI supports File Transfer Protocol (FTP) to transfer files to/from the LANDAC II and the client. The file types include Device applications, Web pages, Configuration files, and the operating system. In short, every file within one LANDAC II can be transferred to another LANDAC II or parts of the LANDAC II file system can be upgraded as needed. This provides a powerful means of performing firmware upgrades or configuration changes.

1.6 Point Mapping

The substation products of today must interface to a wide Varity of I/O and industry standard IEDs. This creates within the LANDAC II a large database of points that must be transferred to one or more master stations.

The LANDAC II GUI supports an intuitive drag and drop point mapping scheme. Each point within the LANDAC II is named and scaled with user definable names and values. Scaling is used for local data display as well as protocol count scaling for conversion of data from one protocol to another.

1.7 Communications

The LANDAC II supports a large suite of communication protocols over many different types of communications media. Two Ethernet ports and sixteen (16) RS232 ports come as standard hardware. Three switchable Ethernet ports are standard. Also supported is an IRIG-B input on BNC. IRIG-B output is supported on all 16 RS-232 ports.

The UIF is a dedicated RS232 port that supports Point-to-Point Protocol (PPP). This port can be used for initial setup, local maintenance and configuration updates.

All Telvent substation automation products support multiple Device and IED protocols. This allows for data to be mapped from IEDs to multiple masters via different Device protocols. Example: If you were replacing your current master station software that talks Series V protocol with a system that supports DNP, your Device could talk to both the old master and the new master at the same time. This provides an excellent means of replacing legacy RTU/MTU equipment without interruption to data acquisition.

An emerging need for substation products is SCADA protocols to communicate over Ethernet all the way down to the Device. The LANDAC II supports DNP, Modbus, and IEC 104 over Ethernet.

1.8 Relay Ladder Logic (RLL)

The LANDAC II supports a RLL Runtime Target that accepts applications that can be developed using any one of the five IEC 61131-3 languages plus flow Charting. Programs are developed on an application workbench that runs only on the client. Fully developed/debugged programs can be downloaded into the LANDAC II and activated for execution.

RLL applications have access to all the data within the Device and make use of the powerful mapping capabilities of the GUI. Output data from RLL applications can be viewed in real time data displays.

1.9 Packaging

The LANDAC II is packaged in an enclosure measuring 11" deep by 7" high by 19" wide. The enclosure is suitable for mounting in a standard 19" rack, or in a panel (with suitable depth). For practical purposes, the clearance for depth must include room for appropriate cables.

1.10 Protection

All terminations contain any transient protection required for the particular input function. In addition to this, relays include matrix and kick-back diodes and digital inputs include current limiting resistors.

CHAPTER 2

Specifications

2.1 Size

ENCLOSURE	19” x 10.5” x 7” metal chassis Fits standard 19” rack / relay panel

Figure 2-1 LANDAC II Front View

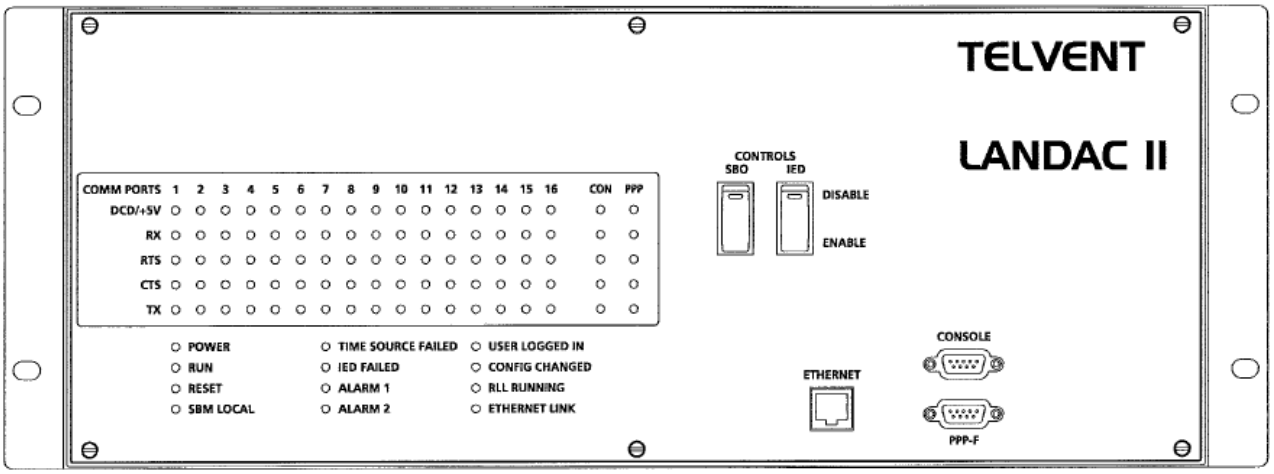
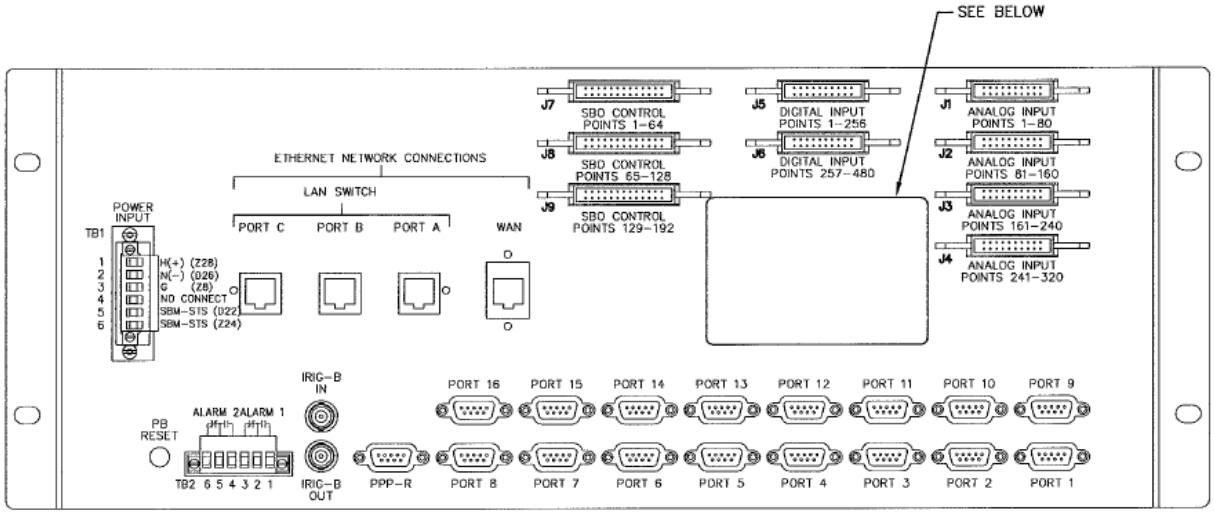
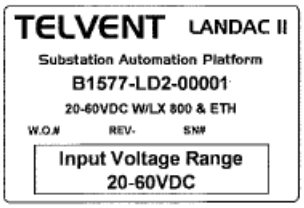


Figure 2-2 LANDAC II Rear View



LABEL DETAIL
(SEE NOTE 5)



LABEL - A

LABEL - B

2.2 Visual Indications

COMMUNICATIONS	5 LEDs per RS-232 port (DCD/+5V, RX, RTS, TX, CTS)
OTHER INDICATIONS	Power, Run, Reset, SBM Local, Time Source Failed, IED Failed, User Logged IN, Config Changed, RLL Running, Ethernet Link, Alarms 1 & 2, SBO Controls Disable, IED Controls Disable

2.3 User Computer Requirement

OPERATING SYSTEM	Windows XP & Vista with Internet Explorer Version 6 or above. If using XML to Excel macro, Microsoft Office 2003 or above.

2.4 Environmental

OPERATING TEMPERATURE	-40 to +85° C
RELATIVE HUMIDITY	5% to 95%, non-condensing
TRANSIENT PROTECTION	All user field connections designed to pass IEEE 472-1974, ANSI C37.90.1-1989 ANSI C37.90-1979 (R1982)

2.5 CPU/Memory

Please refer to the CPU Manual for CPU/Memory Specifications

2.6 User Interface

WEB BROWSER	Internet Explorer
ETHERNET	10/100BASE-T (RJ45)
PPP	RS-232 38.4kbps

2.7 Communications

ETHERNET	Two built-in 10/100BASE-T (RJ45) auto-negotiate (will adjust to the speed and half/full duplex of the connecting device)
SERIAL	16 RS-232C (DB-9) Ports
CONSOLE	RS-232C (DB-9)
DIAL-UP	RS-232C (DB-9)
SERIAL SPEEDS	300-9600 bps (38,400 for PPP)
PROTOCOLS	Synchronous and asynchronous, bit & byte

2.8 C3463 PCA Ethernet 10/100 5-Port Switching Hub

ETHERNET	Five built-in 10/100BASE-T (RJ45) auto-negotiate (will adjust to the speed and half/full duplex of the connecting device)

2.9 Power Requirements

INPUT VOLTAGE	85-350VDC / 85-264VAC 20-60VDC

Power Consumption

Input Voltage	Typical Power Consumption	Max Power Consumption @ Rated Temperature
20-60VDC	12.75 Watts	18 Watts
85-350VDC	12.75 Watts	18 Watts
85-264VAC	25 Watts	30 Watts

Note: Power consumption is measured at the Power Input terminals on the back panel.

INPUT/OUTPUT ISOLATION	500 VDC

2.10 Alarm Outputs

CONTACT FORM	Form C
MAX OUTPUT POINTS	2
CONTACT RATINGS	30 VDC @ 2A, 129 VDC @ 500 MA

2.11 IRIG-B Input

MODULATED/DEMODULATED FORMAT	Accepts IRIG-B signal through BNC connector

2.12 IRIG-B Output

DEMODULATED	Available on all 16 Communications ports
FORMAT	Pins 4&6 on RS-232C (DB-9)
DEMODULATED	Available on BNC connector

2.13 RS-232 Power (Selectable)

5VDC	Configurable on all 16 Comm ports
FORMATS	Pin 1 on RS-232C (DB-9)
POWER AVAILABLE	5W Max Total

2.14 Logic Capabilities

IEC 61131 compliant PLC runtime engine.

2.15 Digital Inputs

(Requires optional external termination (XT) module and status wetting supply as required)

2.15.1 Status Inputs

ISOLATION	Optically isolated, 1500VDC
LOOP VOLTAGES	12, 24, 48, and 129VDC
DEBOUNCE	20 msec nominal
CONFIGURATION	2 terminals per point (+ and -)
MAX INPUTS	480
POWER	XT excitation
INDICATORS	One LED per point.
XT DIMENSIONS	32pt 7x19 inch

2.15.2 Accumulator Inputs

ACCUM. FORMATS	FA, FC (1 or 2 counts/cycle)
ACCUM. INPUT RATE	20 pps max.
MAX INPUTS	480 Form A or 240 Form C

2.15.3 SOE Inputs

ACCURACY	5ms, leading edge tagged
DEBOUNCE	20ms fixed
STORAGE CAPACITY	256 events, optional 1024

2.16 Analog Inputs

Note: Analog inputs require one or more C3130 XT AI card(s).

INPUT TYPE	Single ended
INPUT RANGES	±5VDC, 0-5VDC, 1-5VDC, ±1mA, 0-1mA, 4-20mA
RESOLUTION	12 bits (11 bits plus sign)
COMPREHENSIVE ACCURACY	±0.25% FS between –40° and +85°C
REFERENCE VOLTAGES	±4.500V
CONVERSION RATE	All analogs once per second
COMMON MODE RANGE	±10V
COMMON MODE REJECTION	80 dB @ 50/60Hz
NORMAL MODE REJECTION	60 dB @ 50/60Hz
INPUT RESISTANCE	1M ohm typical
MAX INPUTS	320
XT CONFIGURATION	2 terminals per point (+ and -) with a shared shield ground.

2.17 SBO Control Outputs

(Requires optional external termination (XT) module)

DURATION	Software programmable in 5 msec. increments
MOMENTARY	KUP type 1FC/2FA 10A @ 240VAC or 10A @ 28VDC. KUEP type 1FC 3A @ 150VDC, 2FA 5A @ 150VDC, 1FX 10A @ 150 VDC.
LATCHING	KUL type 1FC/2FA 10A @ 240VAC or 10A @28VDC.
RELAY INSTALLATION	Socketed
MAX OUTPUT POINTS	192 T/C Pairs
XT DIMENSIONS	8pt 7x19 inch

CHAPTER 3

Installation

This chapter describes the normal installation and operation procedures for the LANDAC II Substation Automation Platform. Prior to installing the LANDAC II, we recommend that you perform a preliminary functional test to verify that the configuration is correct for the intended site and also to check for any undetected shipping damage. Preliminary testing should be performed after the LANDAC II has been setup using the information in the previous chapters.

3.1 General Installation Procedure

3.1.1 Rack Installation

As shown in Figure 3-1, the LANDAC II is made to be mounted in a standard 19" rack assembly. All that is needed is four screws. No special ventilation is needed.

The procedures for connecting field wiring to the RTU are provided in the following sections.

Caution: The printed circuit assembly contains CMOS devices and is sensitive to static discharge. Boards should be handled only at a grounded workstation. Avoid touching the electronic components, jumpers, connectors, or the exposed etches on the boards.

Figure 3-1 LANDAC II Dimensions

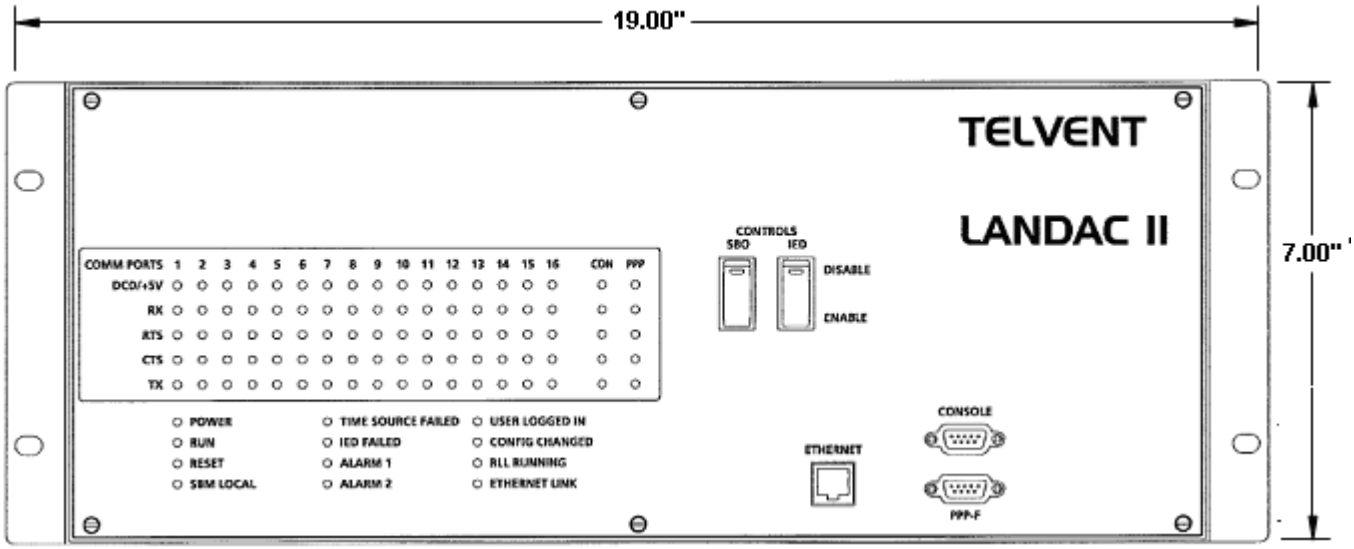
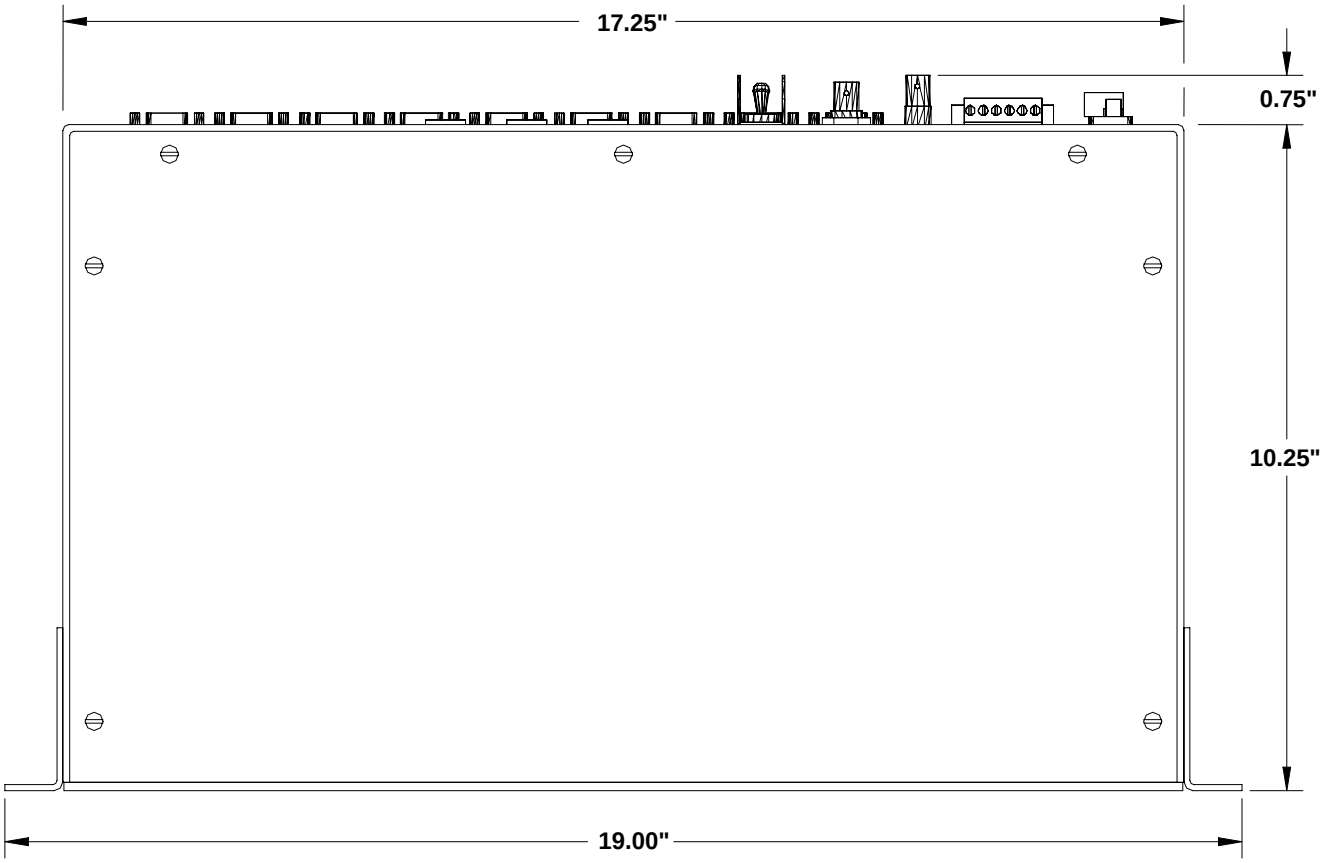


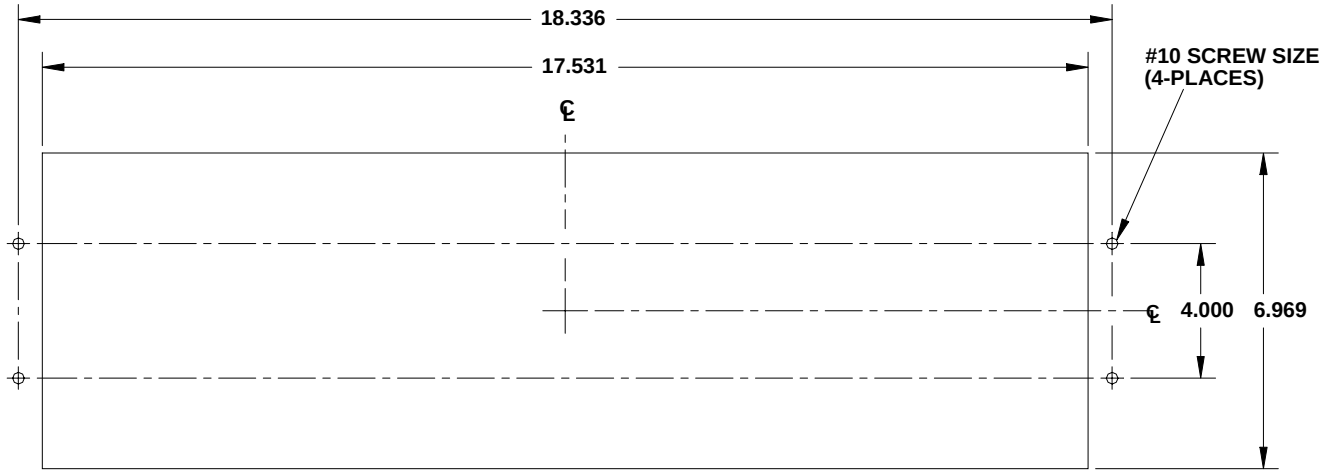
Figure 3-2 LANDAC II Dimensions



3.1.2 Panel Installation

The LANDAC II may also be installed in a panel, provided there is enough depth behind the panel to accommodate the LANDAC II plus cable connections. Follow the cutout and hole-tapping template shown in Figure 3-3.

Figure 3-3 LANDAC II Panel Mounting Template



3.1.3 User Interface Connections

There are four physical ways to connect to the LANDAC II:

- Ethernet connection to a network using a Straight-through cable to the CPU card - Best way to gain remote access
- Ethernet connection locally using an Ethernet crossover cable to the CPU card - Best way to gain local access
- PPP (Point-to-Point Protocol) connection using a null-modem cable to the UIF port - Moderately slow; can still access RTU locally or even remotely with a dedicated comm. Channel
- Console – this method commonly used to read and/or change IP address

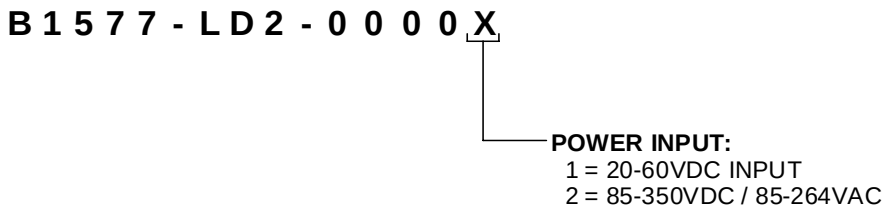
Both the PPP and the Ethernet connections use the same GUI running on Internet Explorer. The difference is that the PPP connection runs at 38,400 baud; the Ethernet connection runs at 10/100MB. When dealing with a GUI, obviously the faster connection is much better. Therefore, the primary connection to the RTU is Ethernet.

Please see Appendices D and E in the config@WEB Software Users Guide for further connection information.

3.2 Power Input

Field input power depends upon the variance of your particular LANDAC II. See "Power Input" variance in Figure 3-4. Refer to your label on the rear panel for your particular variance. After determining the correct input power, connect the power to the POWER INPUT termination on the back of the LANDAC II as shown in Figure 3-8.

Figure 3-4 LANDAC II Variance Structure



3.3 Ethernet Ports

The LANDAC II is equipped with one standard Ethernet port on the front panel. Switched Ethernet provides three more Ethernet ports on the rear panel as shown in Figure 3-5.

Switched Ethernet is a method of increasing the number of available Ethernet ports while at the same time ensuring that traffic flow (throughput) is optimized. The switched Ethernet card is "smart" because it can recognize whether you have a straight-through or cross-over Ethernet cable attached to one of the switched ports, and compensate accordingly. As a matter of good configuration practice, we recommend that you always use a cross over cable when accessing the LANDAC II directly, as shown in Figure 3-5, and always use straight through cables when connecting through a network, as shown in Figure 3-6.

In addition to the standard Ethernet port and the Switched Ethernet, the LANDAC II is equipped with a WAN Ethernet port on the rear panel. This port uses a separate NIC (Network Interface Card) from the standard and the switched ports and thus must be accessed by a separate IP address. This port allows the LANDAC II to be a component of another network.

Figure 3-5 Recommended Direct Connections with a Switched Ethernet Card

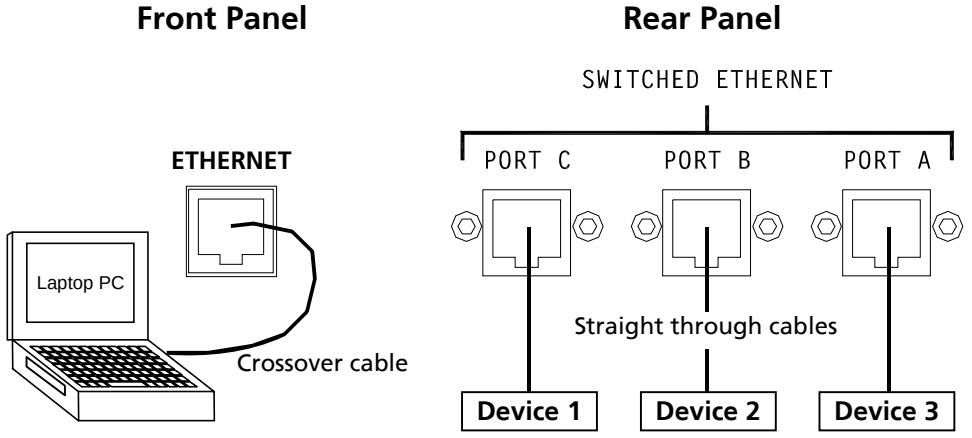


Figure 3-6 Recommended Network Connections with a Switched Ethernet Card

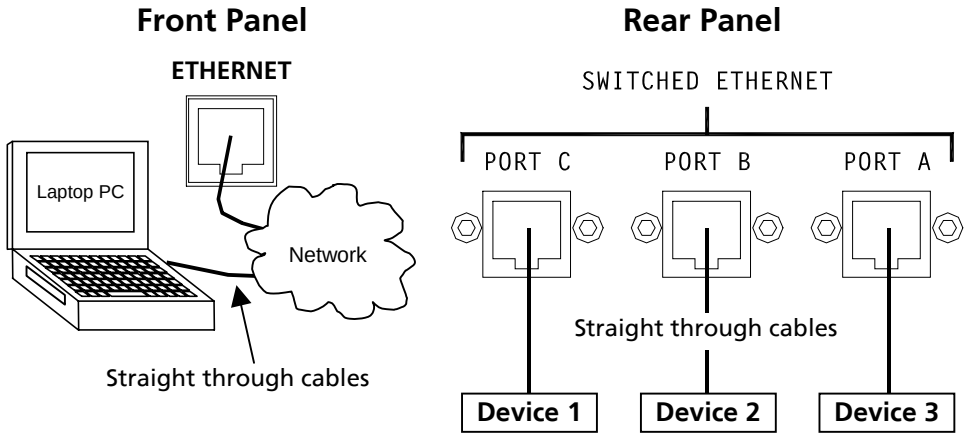


Figure 3-7 LANDAC II Front Panel

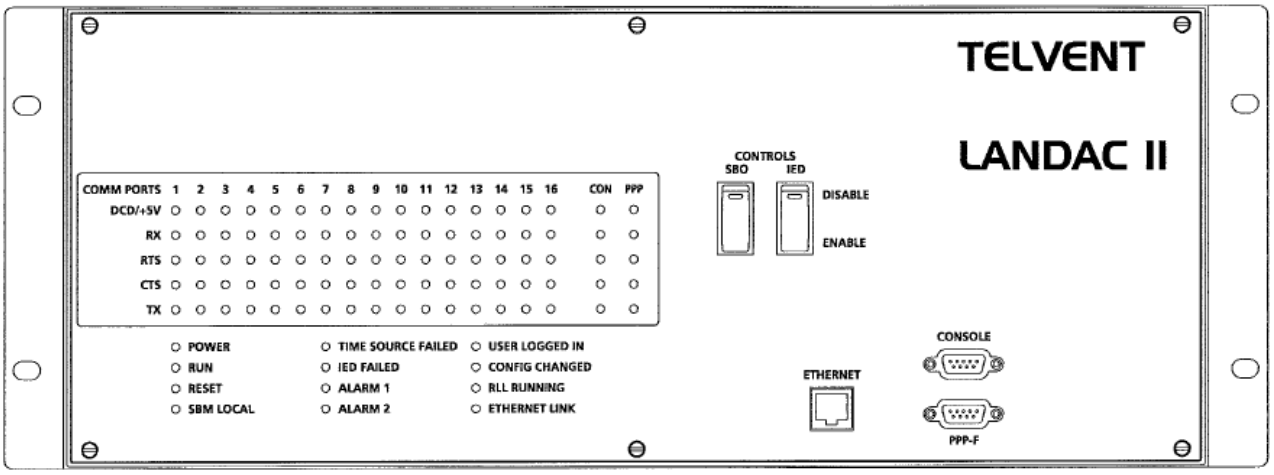
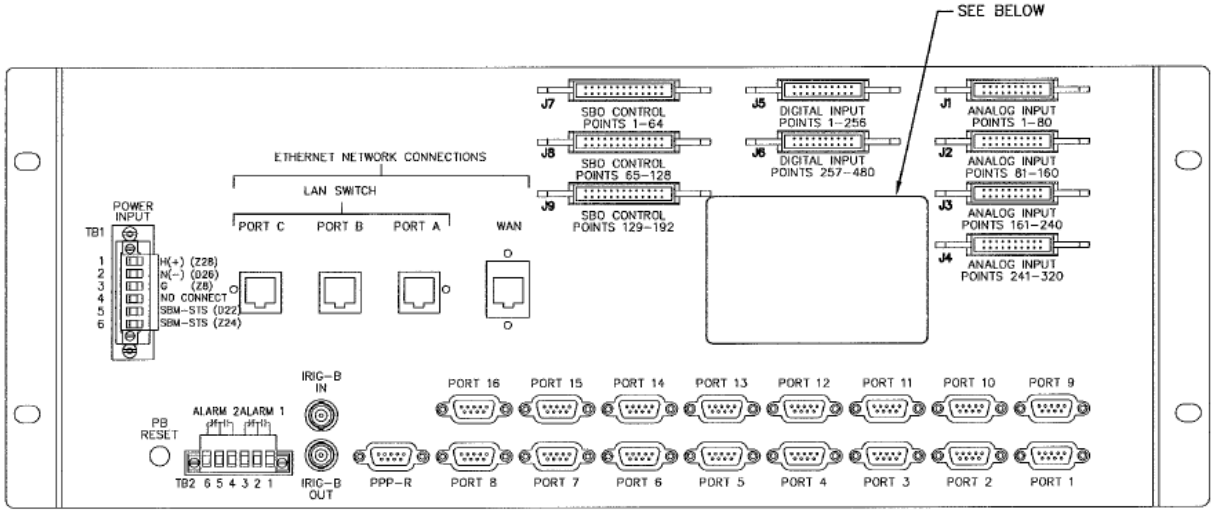
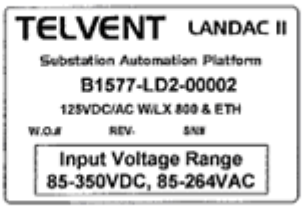


Figure 3-8 LANDAC II Rear Panel



LABEL DETAIL

LABEL - A



LABEL - B

3.4 Serial Ports

3.4.1 Front Panel (Console & PPP)

The LANDAC II has two RS232 connectors on the front panel. One is the Console, the other is PPP-F (Point to Point Protocol). The F is a reminder that there are two PPP ports; one on the Front, one on the Rear. The Front and Rear PPP ports are meant as a convenience; they are in parallel. Electrically, there is only one PPP port.

Figure 3-9 Console & PPP DB9 Pin-out

Signal	Pin #	Description	Type	Console	PPP
DCD	1	Data Carrier Detect	Input		X
RX#	2	Receive Data	Input	X	X
TX#	3	Transmit Data	Output	X	X
DTR	4	Data Terminal Ready	Output		X
DGND	5	Ground	N/A	X	X
DSR	6	Data Set Ready	Input		X
RTS	7	Request To Send	Output		X
CTS	8	Clear To Send	Input		X
RI	9	Ring Indicator	N/A		

X = Active

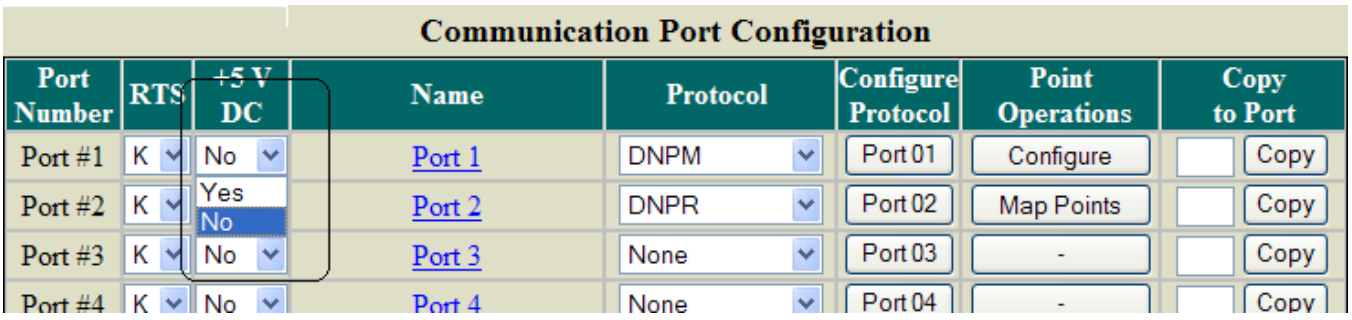
3.4.2 Rear Panel (Serial Ports)

There are 17 RS232 connectors on the Rear Panel. One of the connectors is PPP, which is in parallel with the PPP connector on the front (see above). The other 16 serial ports are used for connections to IEDs and/or MTUs.

Figure 3-10 Serial Port DB9 Pin-out

Signal	Pin #	Description	Type
DCD	1	Data Carrier Detect *	Input
PWR		+5V for aux comm. devices *	Output
RX#	2	Receive Data	Input
TX#	3	Transmit Data	Output
IRIGB	4	Timing signal	Output
DGND	5	Ground	N/A
IRIG_GND	6	IRIG Ground	N/A
RTS	7	Request To Send	Output
CTS	8	Clear To Send	Input
RI	9	Ring Indicator	N/A

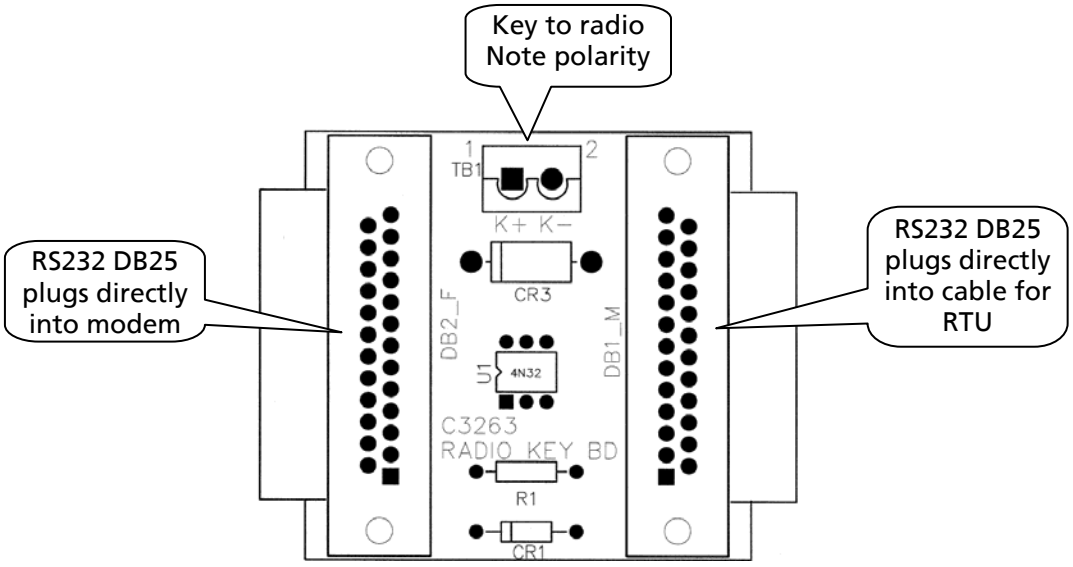
* Selectable for either DCD or PWR – "No" for DCD, "Yes" for PWR. The default is "No". See Communication Port Configuration below.



3.4.3 Radio Keying Option

Some communications devices require an open collector output to key the device for data transmission. The config@WEB RTUs do not have this output on their baseboards. The optional C3263 Radio Keying Module provides an optically isolated open collector output to perform this function. Configure the RTS (Request to Send) to K (for Keyed) in the Communications Port Configuration to control this output. The module is installed as shown in the figure below.

Figure 3-11 C3263 Radio Keying Board Installation



Communication Port Configuration

Port Number	RTS	+5 V DC	Name	Protocol	Configure Protocol	Point Operations	Copy to Port
Port #1	K	No	Port 1	DNPM	Port 01	Configure	Copy
Port #2	No		Port 2	DNPR	Port 02	Map Points	Copy

Note: RTS (Request to Send) in the Communications Port Configuration must be in the K (Keyed) position for the C3263 Radio Keying Board to work. The RTS time may be controlled with the CTS Delay (no RTU reset required after change) in the Communication Channel Configuration.

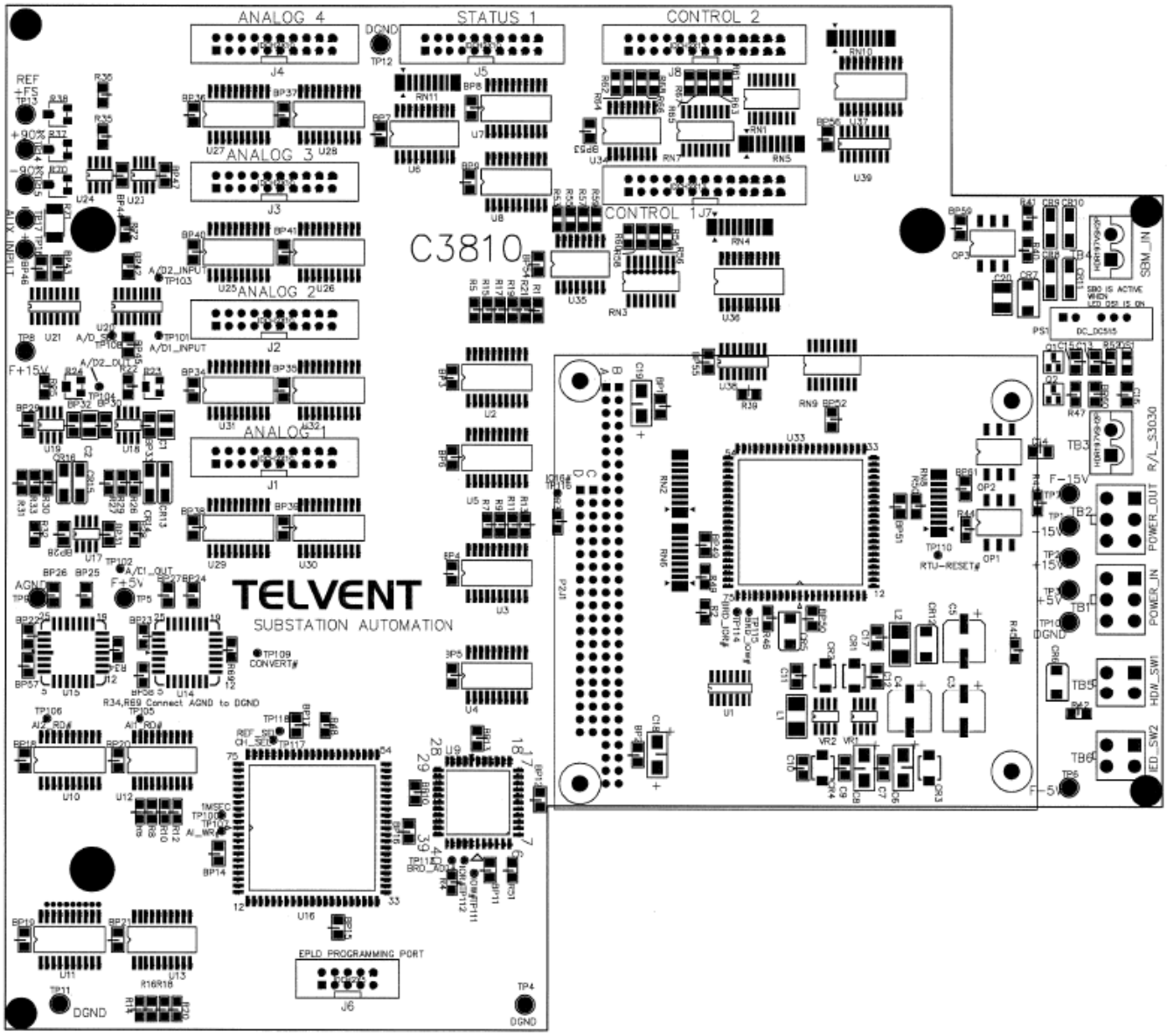
3.5 C3810 I/O Expansion Board

Internal to the LANDAC II is the C3810 I/O expansion board. This board adds additional I/O to the LANDAC II To view the C3810 Design Document, see Appendix A. The board has the following I/O complement:

- 256 Status Inputs on 1 bus connector
- 320 Analog Inputs on 4 bus connectors
- 128 SBO controls on 2 bus connectors

The C3810's PC/104 connector allows for placement of the board vertically between the baseboard and the CPU card.

Figure 3-12 C3810 I/O Expansion Board



3.5.1 Analog Input Expansion

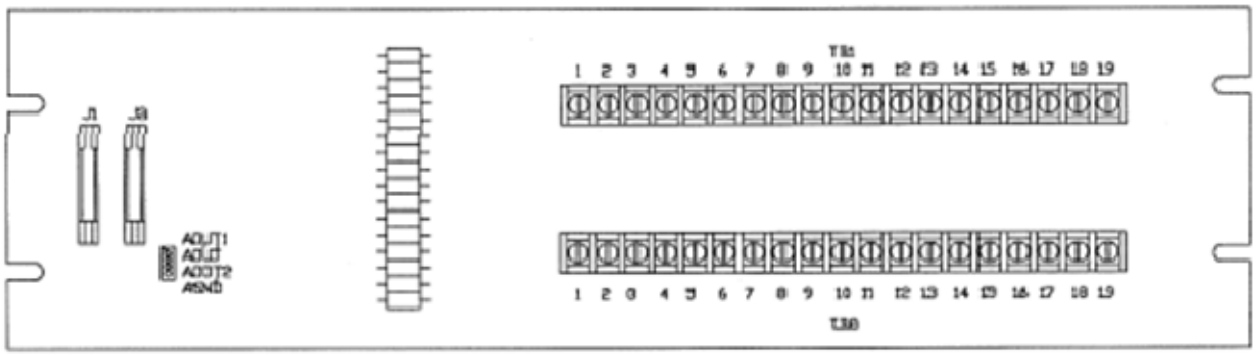
Note: Requires optional external termination (XT) module.

LANDAC II Analog Input Expansion Module, the C3130 AI XT (Figure 3-13), connects to one of four Analog Input Expansion connectors on the rear panel (see Figure 3-8).

The AI XTs are connected together with standard ribbon cables in a daisy chain. The first XT is connected from the AI Expansion connector on the LANDAC II rear panel to J1 on the XT. Subsequent XTs are daisy chained together (J2 to J1). You may continue adding XTs in this manner until a maximum of five full XTs are installed and when a total of 80 (per AI bus) input points has been reached.

The LANDAC analog inputs are differential, hence two terminals (positive and negative) are provided for each input, along with shared terminal points for the shields. It is recommended that shielded pair cables be used for each analog input, and that the shields be tied to ground only at the XT.

Figure 3-13 C3130 16-Point AI XT



3.5.2 Digital Input Expansion

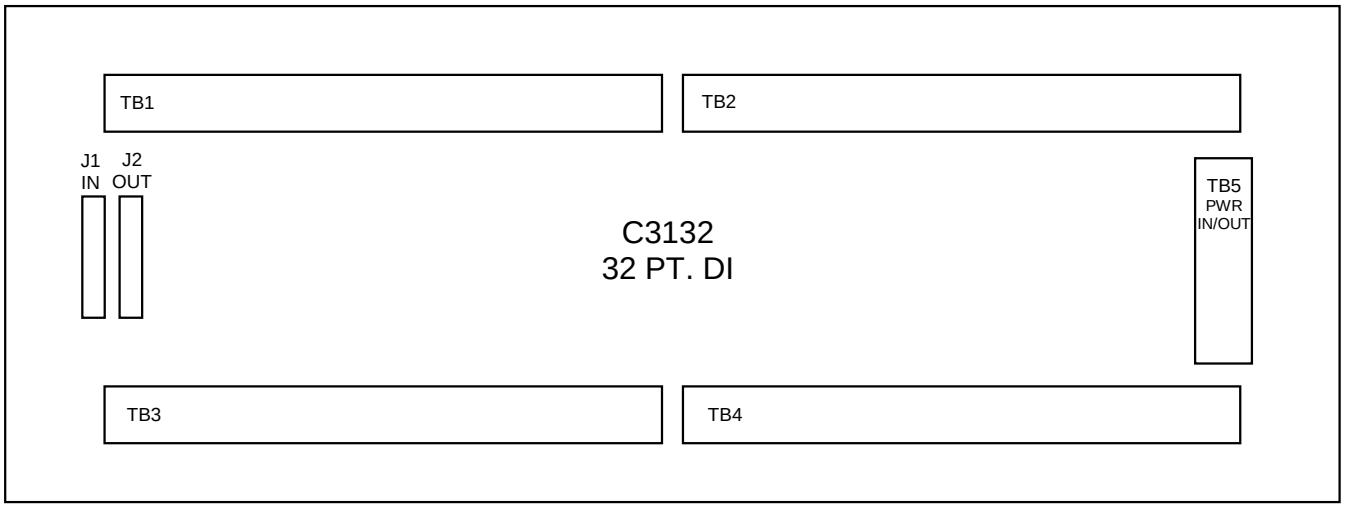
Note: Requires optional external termination (XT) module.

The LANDAC II uses the same digital input extension hardware for both status and accumulator inputs. The LANDAC II XT connection is on the rear panel (see Figure 3-8).

The DI XTs are connected together with standard ribbon cables in a daisy chain. The first XT is connected from the DI Expansion connector on the LANDAC II rear panel to J1 on the XT. Subsequent XTs are daisy chained together (J2 to J1) until a total of 256 input points has been reached on the first connector and 224 input points on the second connector.

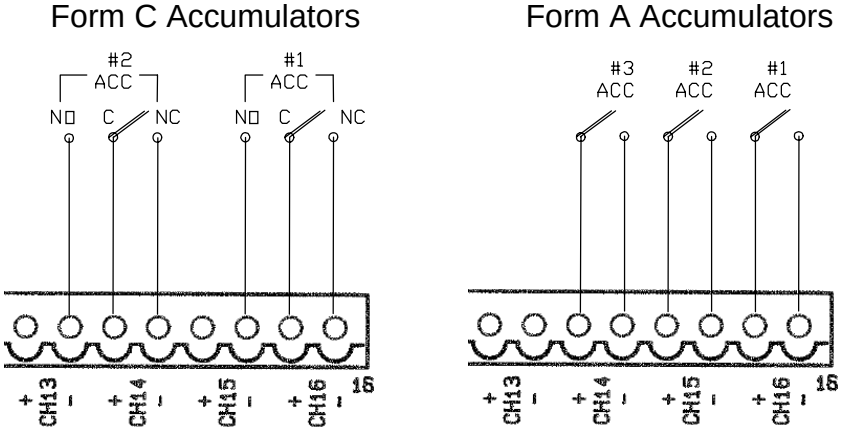
Digital inputs are added using the C3132 DI XT (Figure 3-14) which allows 32 inputs. All digital inputs include individual LEDs that are illuminated when the corresponding contact is closed.

Figure 3-14 C3132 32-Point DI XT



The DI XT provides two terminals for each digital input. The "+" sign indicates the terminal which connects to the wetting voltage. These "+" terminals are all wired together on the XT. The other terminals connect to the opto-coupler. Form A accumulators require one digital input (two wires) each and are hooked up the same as status inputs. Form C accumulators require two digital inputs (typically three wires) each and should be wired according to the example in the left side of Figure 3-15. Note that either positive terminal in the input pair can serve as the common terminal.

Figure 3-15 Accumulator Input Field Wiring



3.5.3 SBO Control Expansion

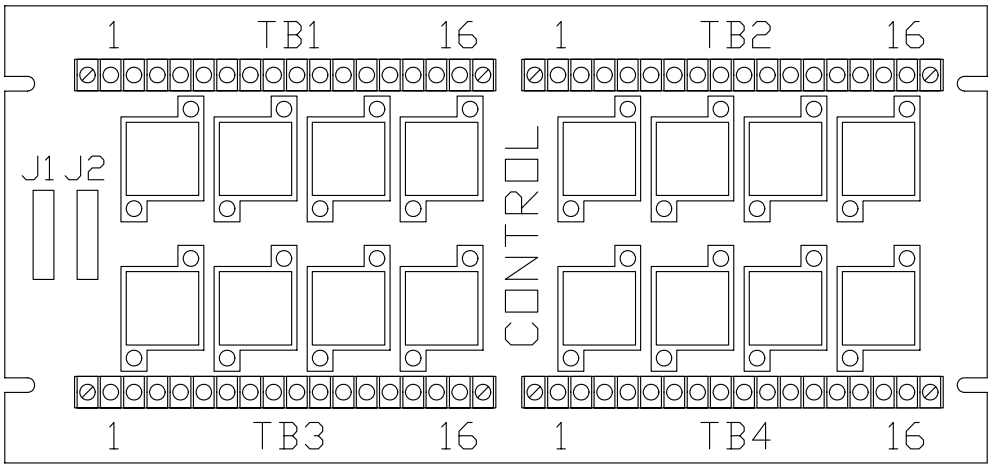
Note: Requires optional external termination (XT) module.

The rear panel of the LANDAC II includes an SBO Control Expansion connector. Using ribbon cables in a daisy-chain connection, up to 192 SBOs (384 coils) may be added to the LANDAC II.

3.5.3.1 C3133 SBO XT

The C3133 19-in. rack mount SBO XT (Figure 3-16) provides eight momentary and latching control outputs, in the form of 16 KUP or KUEP type relays. All relays are installed in sockets with mechanical restraints and have associated LEDs to indicate when a specific relay coil is energized. This XT is cabled onto the SBO bus by connecting the ribbon cable from the LANDAC II rear panel connector or OUT connector of a previous XT to the J1 (IN) connector of the C3133. The J2 (OUT) connector is used to connect to the next XT on the SBO bus.

Figure 3-16 C3133 SBO XT 8 Trip/Close Points

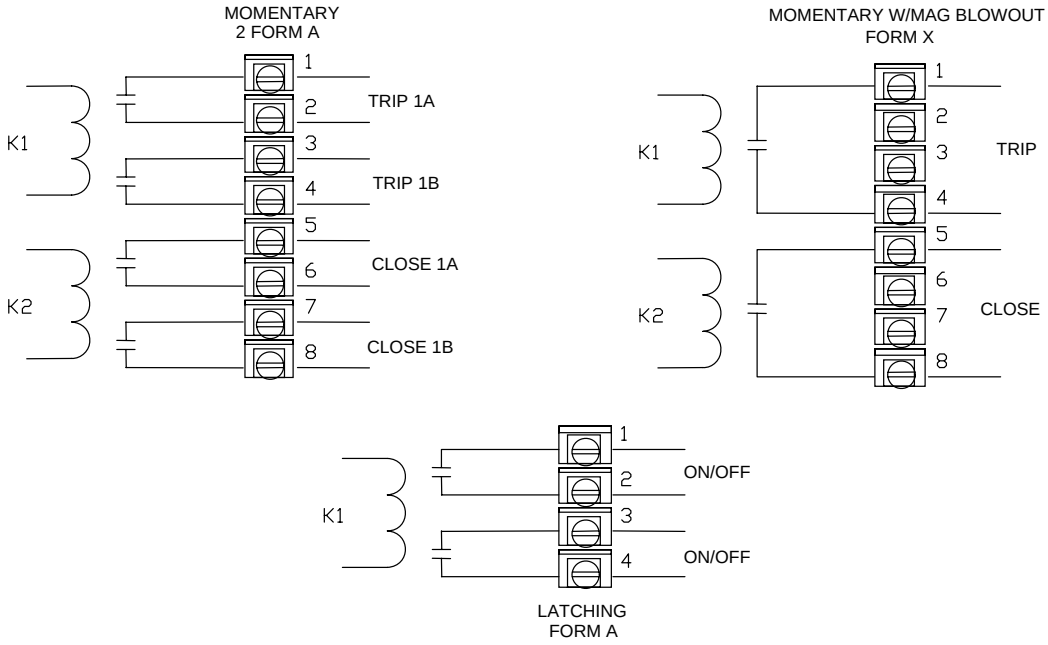


In a typical installation, the uppermost XT contains the first eight outputs, the next lower XT contains the next group of outputs, and so on. The typical SBO XTs are equipped with relays rated for 10A at 240VAC or 24VDC. For applications that require that higher DC voltages be switched, KUEP-type relays with magnetic blowout must be used. These relays have a contact rating of 10A at 150VDC and their standard contact arrangement is form X.

Warning: KUP and KUL type relays should not be used to switch 125VDC devices, even if the current is significantly less than 10A. The contact rating of these relays is greatly reduced at high DC voltages and the relay is subject to failure if the maximum current is exceeded. Consult the factory if you are unsure of the suitability of the relays installed on your SBO XTs.

Figure 3-17 illustrates the hookup procedure for the first output for the various versions of the SBO XT. The momentary and latched output functions shown (trip/close and on/off) are arbitrary; the master station that commands the RTU determines the actual functions. The firmware simply treats the SBO XT as a group of 8 or 16 relay coils without regard to their assigned functions.

Figure 3-17 SBO XT Field Wiring



3.6 Alarm Outputs

The LANDAC II has two Form C outputs on the rear panel for alarms. From the config@WEB interface, you may configure these alarms to be activated by any DI. See Chapter 2 Specifications for contact ratings.

3.7 IRIG-B In & IRIG-B Out

IRIG-B input and output are available from these two ports on the rear panel. Use RG58 coaxial cable for connections between devices for the IRIG-B signal.

3.7.1 IRIG-B signal as a Input to the RTU

If the RTU IRIG-B system is connected to a IRIG-B source, it must provide a B 0 2 X or B 1 2 X Time Code Format signal to the RTU.

Modulation/Frequency (First Digit of IRIG-B Time Code Format)

0 - Pulse Width Code

1 - Sine Wave, Amplitude Modulated

Frequency/Resolution (Second Digit of IRIG-B Time Code Format)

2 - 1kHz/1ms

Coded Expressions (Third Digit of IRIG-B Time Code Format)

0 through 7 is acceptable. The RTU IRIG-B system uses only the BCDtoy (Binary-Coded-Decimal time-of-year) Coded Expressions part of the IRIG-B data stream. The BCDtoy is included in Coded Expressions 0 to 7 of the IRIG-B data stream.

3.7.2 IRIG-B signal output from the RTU

If the RTU IRIG-B system is driven by a time source in the RTU, the Time Code Format is B 0 2 2.

Modulation/Frequency (First Digit of IRIG-B Time Code Format)

0 - Pulse Width Code

Frequency/Resolution (Second Digit of IRIG-B Time Code Format)

2 - 1kHz/1ms.

Coded Expressions (Third Digit of IRIG-B Time Code Format)

2 - BCDtoy

3.7.3 IRIG-B Reference

The following is a link to the IRIG Standard 200-04 document for IRIG Serial Time Code Formats.

https://wsmrc2vger.wsmr.army.mil/rcc/manuals/200-04/TT-45.pdf

CHAPTER 4

Maintenance

This chapter describes maintenance procedures for the LANDAC II. Those users who desire a more thorough technical understanding of the LANDAC II should refer to the Theory of Operation chapter which contains detailed descriptions of each module, and to the Drawings chapter, which contains complete schematics, bills of materials, and printed circuit board assembly drawings.

The following equipment is recommended for performing routine maintenance and repair on LANDAC II RTUs:

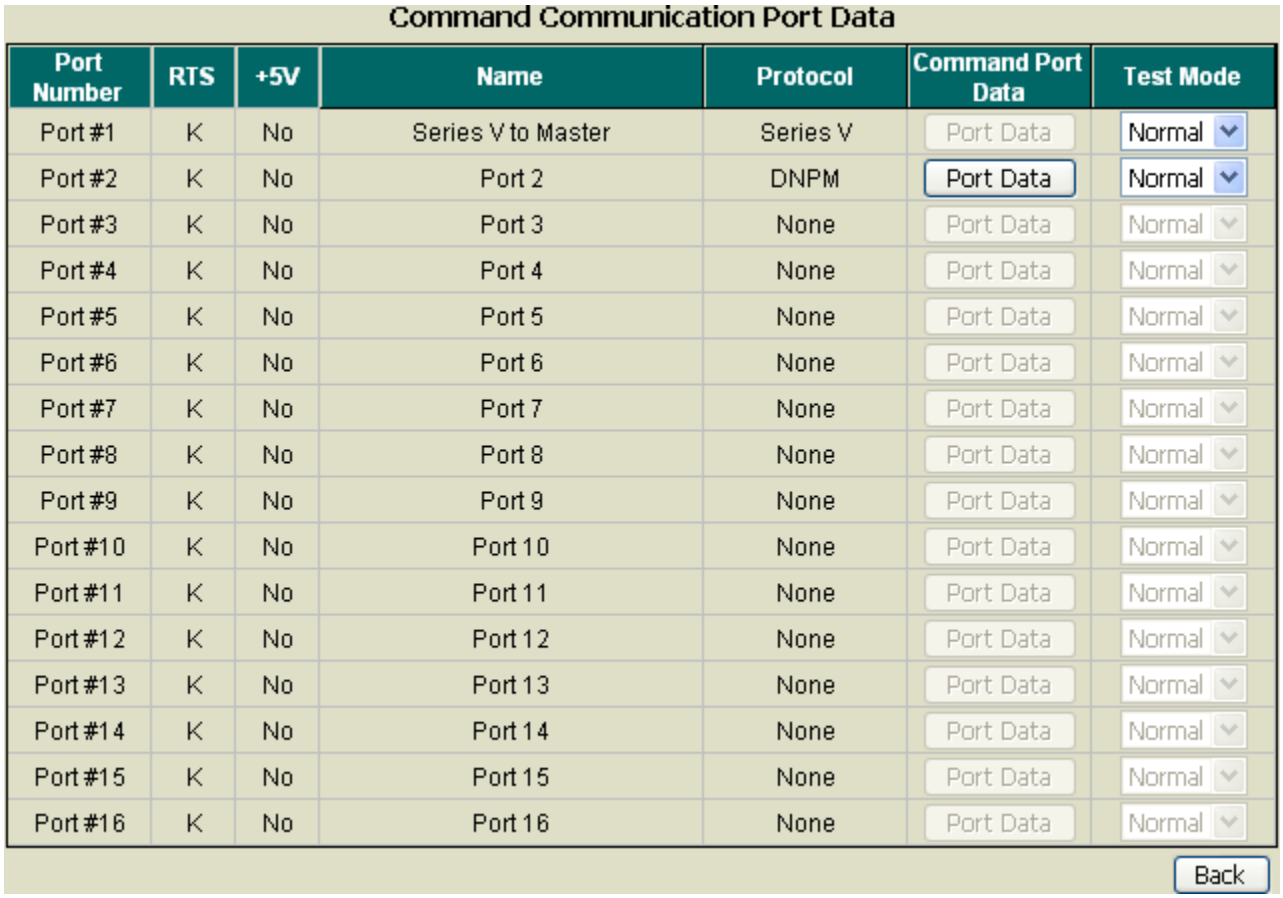
- General-purpose 3-1/2 digit DMM
- General-purpose oscilloscope

The LANDAC II requires no routine adjustments.

4.1 Comm Port Diagnostics

The RTU includes a built-in test routine that allows limited testing of the communication ports. Click the Command tab, then click Serial Comm. You will see a screen similar to Figure 4-1.

Figure 4-1 Command Communications Port Data



Under the Test Mode heading, select the type of test you wish from the pull-down menu for the port of interest. The choices and the meaning of each type of test are listed below. See Figure 4-3 for the expected results for each test.

Normal

In the normal mode, the selected comm channel functions normally. Each channel will be in this mode when the display is called up. Each channel is automatically restored to this mode when you exit from the display or the RTU is reset.

Mark

In the mark mode, the selected comm channel outputs a continuous stream of ones. Marks for the RS-232 channel are low (negative) voltage pulses, and low frequency (1,200Hz) for any attached 202 modem.

Space

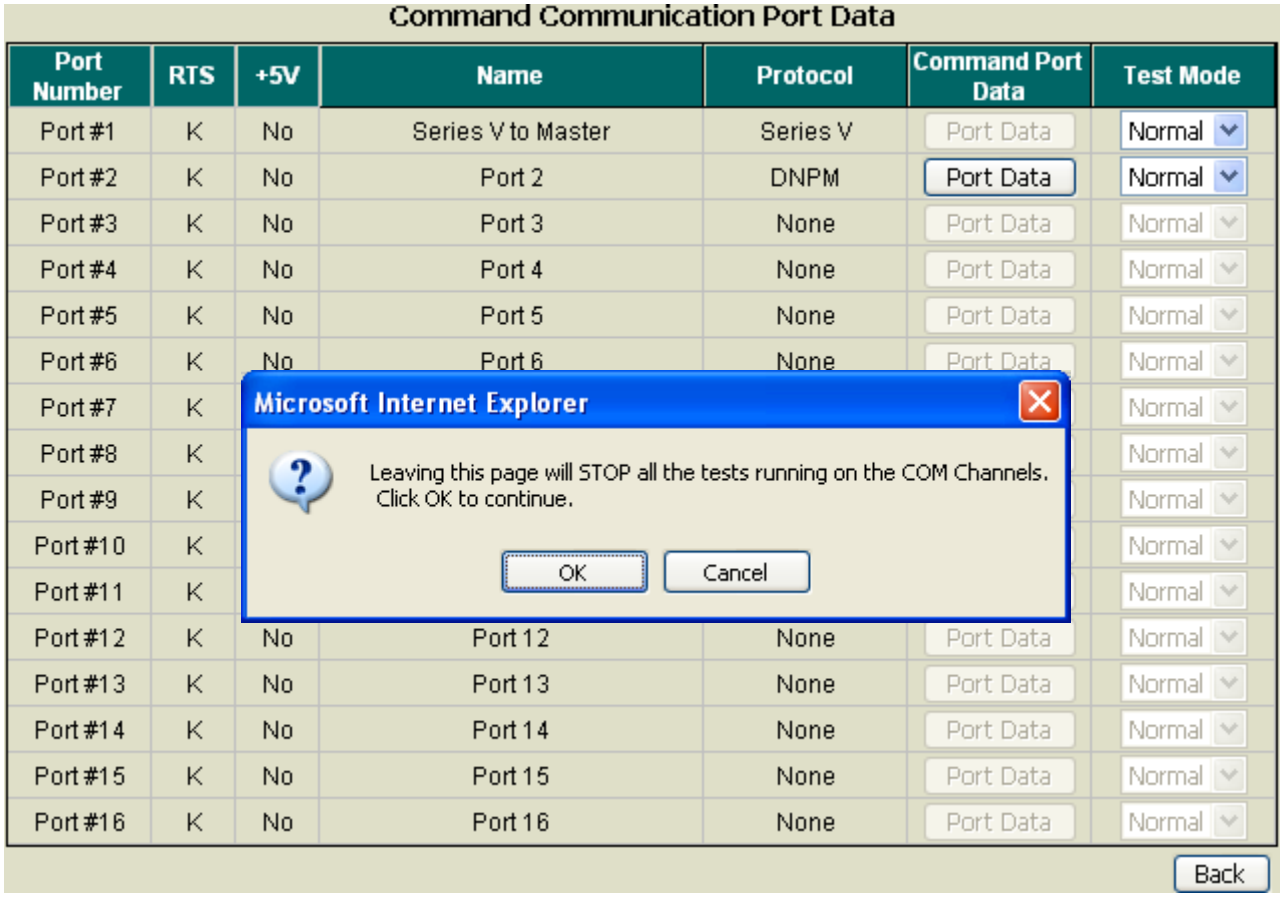
In the space mode, the selected comm channel outputs a continuous stream of zeros. Spaces for the RS-232 channel are high (positive) voltage pulses, and high frequency (2,200Hz) for any attached 202 modem.

Alt

In the Alt mode, the selected comm channel outputs a continuous stream of alternating ones and zeros at the baud rate originally selected for the channel.

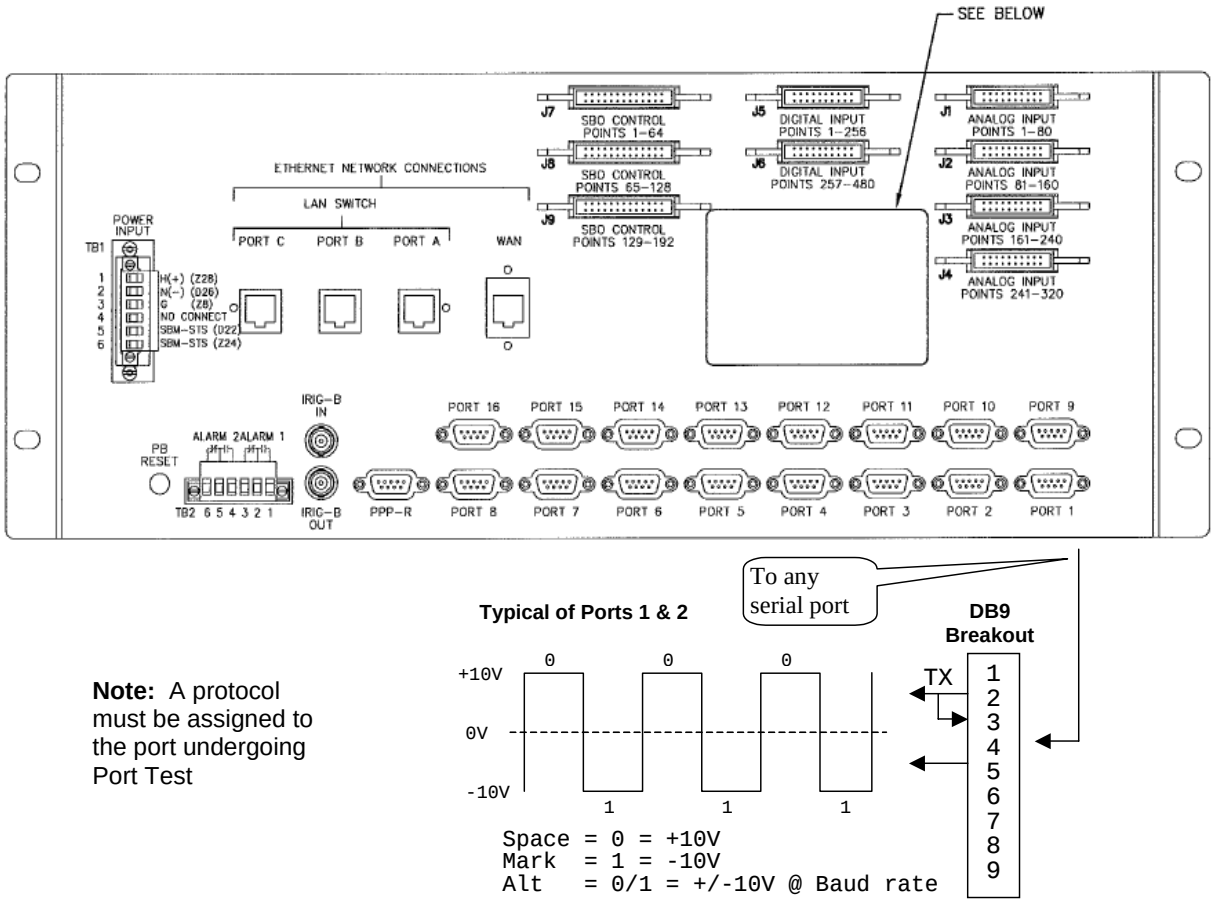
You may use a scope to see the outputs on the ports under test as shown in Figure 4-3. Notice that the test mode will terminate and return to Normal mode if you leave this screen with the pull-down menus in anything other than Normal, as shown in Figure 4-2.

Figure 4-2 Clicking the Back Button While in Test



Use a jumper between pins 2 & 3 as shown in Figure 4-3 to get the values shown in the Figure.

Figure 4-3 Comm Port Test



Note: A protocol must be assigned to the port undergoing Port Test

While doing the Port Test, the LEDs on the front panel will light according to the following table.

Table 4-1 Port Test LEDs

Test Mode Function	Front Panel LEDs
Normal	All LEDs OFF
Mark	RTS ON
Space	TX, RX, & RTS ON
Alt	Same as Space, but TX & RX dimmer

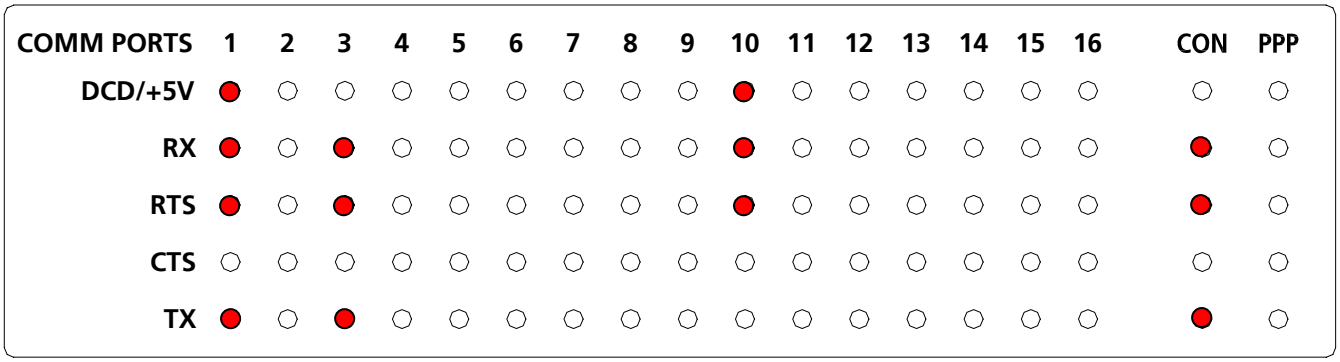
4.2 Troubleshooting

This section includes a brief guide to troubleshooting some of the more common problems that could occur in the LANDAC II. If you are troubleshooting to the component level, the use of the Theory of Operation chapter and the Drawings chapter will be helpful.

4.2.1 LED Display

The LEDs on the front panel are a prime troubleshooting aid. Below is a typical example of the LED activity.

Figure 4-4 Front Panel LEDs



There is a set of Comm lights for every serial port, including the Console and the PPP ports. The lights have the following meanings.

DCD/+5V

Dual meaning: DCD (Data Carrier Detect) in, or +5V out. Usage depends on configuration of serial port on the "Serial Communications" page of the GUI interface.

RX

Receive. This hardware driven LED indicates activity on the Receive pin (pin 2) of this port's RS232 connector.

RTS

Request To Send. This hardware driven LED indicates activity on the Request to Send pin (pin 7) of this port's RS232 connector.

CTS

Clear To Send. This hardware driven LED indicates activity on the Clear to Send pin (pin 8) of this port's RS232 connector.

TX

Transmit. This hardware driven LED indicates activity on the TX pin (pin 3) of this port's RS232 connector.

The LEDs beneath the Comm lights show conditions for many other functions in the LANDAC II.

POWER

This hardware driven LED indicates whether or not the LANDAC II has power. Normally on.

RUN

This software driven LED indicates whether or not the LANDAC II CPU is running. Look for the signature "heartbeat"; that is, a fast blink. A "steady ON" light means the LANDAC II is in either Safe mode or Crash Recovery mode. No light means the CPU is not running. Normally blinking.

RESET

This hardware driven LED illuminates while the the unit's reset signal is asserted. Normally off.

SBM LOCAL

Local control. This software driven LED indicates the position of the SBM Local/Remote switch. In Local, Field Power is removed from the devices connected to the interposing relay on the SBO control bus. Normally off.

TIME SOURCE FAILED

This software driven LED indicates that one or more of the configured time sources are in a failed state. Normally off.

IED FAILED

This software driven LED indicates that one or more of the configured IEDs is in a failed communications state. Normally off.

ALARM 1

This hardware driven LED indicates that the Alarm 1 relay has been energized. Normally off.

ALARM 2

This hardware driven LED indicates that the Alarm 2 relay has been energized. Normally off.

USER LOGGED IN

This software driven LED indicates that one or more user sessions is currently active. Normally off.

CONFIG CHANGED

This software driven LED indicates that a configuration XML file has been sent to the LANDAC II and the LANDAC II has not yet been reset making the new XML file active. Normally off.

RLL RUNNING

This software driven LED indicates that an ISaGRAF RLL program has been downloaded into the RTU and is currently active. Caution should be taken in that control operations may occur without notice depending on the functions built into the RLL program. Normally off.

ETHERNET LINK

This software driven LED indicates that the Ethernet circuit located on the CPU card has detected a valid link to another Ethernet device. This LED is always illuminated with the Switched Ethernet PC/104 card installed.

SBO CONTROLS SWITCH

SBO controls are disabled or enabled. LED is illuminated when disabled.

IED CONTROLS SWITCH

IED controls are disabled or enabled. LED is illuminated when disabled.

Note: See Appendix A for **Special Logic for Combinations of Remote / Local Switch Positions.**

4.2.2 Data Display

You can use the Data Display Menu to monitor the operation of input and output devices. The Data Display can be compared to the LEDs as a means of status verification.

4.3 LANDAC II Reference Points

The References Configuration screen allows you to enter names or keep the default names for the 16 LANDAC II reference points. Since the LANDAC II has two Analog to Digital Converters, there are 8 references for each A/D Converter. The following table lists these reference points.

Table 4-2 LANDAC II Reference Points

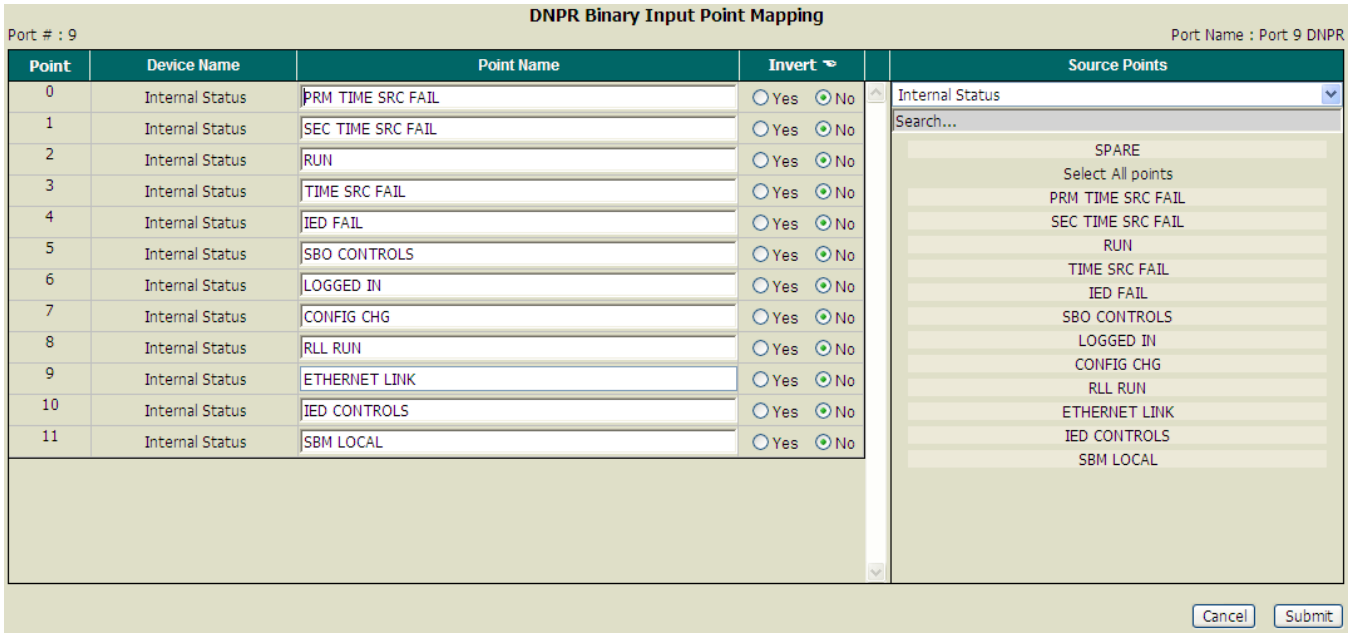
Reference	Reference Name #1	Reference Name #2	Type	EGU Min	EGU Max	EGU
Ground	ADC #1 AGND	ADC # 2 AGND	Bipolar	-5	+5	VDC
Full Scale	ADC #1 Full Scale	ADC #2 Full Scale	Bipolar	-5	+5	VDC
Positive	ADC #1 +90% Reference	ADC #2 +90% Reference	Bipolar	-5	+5	VDC
Negative	ADC #1 -90% Reference	ADC #2 -90% Reference	Bipolar	-5	+5	VDC
Temperature	ADC #1 Temperature	ADC #2 Temperature	Bipolar	-5	+5	VDC
Ground	ADC #1 AGND	ADC # 2 AGND	Bipolar	-5	+5	VDC
Ground	ADC #1 AGND	ADC # 2 AGND	Bipolar	-5	+5	VDC
AUX Input	ADC #1 AUX Input	ADC #2 AUX Input	Bipolar	-5	+5	VDC

4.4 Internal Status Points

The firmware automatically generates internal status points that are useful for monitoring important functions within the RTU. The Internal Status Points appear as source points for mapping, as shown in the example below.

Note: Internal status points are visible only when mapped to a master or any other function that is capable of mapping points. The example below happens to be a slave protocol.

Figure 4-5 Mapping Internal Status Points



PRM TIME SRC FAIL

Indicates the health of the Primary Time Source. Close means the primary time source has failed. Open means the primary time source is operational.

SEC TIME SRC FAIL

Indicates the health of the Secondary Time Source. Close means the secondary time source has failed. Open means the secondary time source is operational.

RUN

Indicates whether or not the CPU is running. In Display mode, look for the signature "heartbeat"; that is, a one-second change of status similar to the blink-rate of the Power/Run LED on the CPU card (although they won't necessarily be in sync). Normally blinking.

TIME SRC FAIL

Indicates the health of either Time Source. If two time sources are configured (primary and secondary), Close means one of the time sources has failed. Open means both sources are operational.

IED FAIL

Indicates the status of the IED. Closed means an IED (or communications with it) has failed. Open means the IED is operational. Normally Open.

SBO CONTROLS

Indicates whether SBO controls are disabled or enabled. Closed means that SBO controls are disabled. Open means that SBO controls are enabled.

LOGGED IN

Indicates whether or not someone is logged into the device. Closed means that one or more persons are logged in. Open means that no one is logged in.

CONFIG CHG

Indicates whether or not the configuration has been changed since the last reset. Closed means there has been a configuration change since the last reset. Open means there has been no configuration change since the last reset. Normally Open.

RLL RUN

Indicates whether or not an RLL program is running. Closed means there is an RLL (ISaGRAF) program running in the RTU. Open means there is no RLL program running.

ETHERNET LINK

Indicates whether or not there is a valid Ethernet link circuit connected to the Ethernet connector. Closed means there is a valid Ethernet connection to the RTU. Open means there is not.

IED CONTROLS

Indicates whether IED controls are disabled or enabled. Closed means that IED controls are disabled. Open means that IED controls are enabled.

SBM LOCAL

Indicates the position of the SBM Local/Remote switch. In Local, Field Power is removed from the devices connected to the interposing relay on the SBO control bus. Closed means that the Switch is in Local. Open means that it is in Remote.

4.4.1 Data Display

You can use the Data Display Menu to monitor the state of the Internal Status points once they are mapped to a master or some other function that is capable of mapping points. Data Display can then be used as a means of status verification.

CHAPTER 5

Theory of Operation

This section provides detailed technical design information on the LANDAC II and its various internal and external modules, including design of the firmware and hardware. Use this chapter if you want to troubleshoot and repair to component-level on the modules. This section is based on the simplified block diagrams included with the text.

Use the schematic drawings and printed circuit assembly drawings in the Drawings chapter of this manual for a more detailed study.

5.1 Basic Architecture

The LANDAC II uses several internal board assemblies that are connected together via hardware and software to produce the required point count. The base I/O complement resides on the C3800 baseboard. This board is responsible for SBO control points 129 – 192 available at J9, Status input points 257 - 480 on J6, two alarm outputs available at TB2, and the 16 RS-232 communications ports 1 – 16. The C3800 board also receives / generates the IRIG-B signal.

Additional I/O points are handled by the internal C3810 board which is responsible for SBO points 1 – 128 available at J7 and J8, Status Points 1– 256 available at J5, and all 320 Analog Inputs available on connectors J1 – J4.

Ethernet communications (LAN) is handled by the LX800 CPU with additional port connections supplied by a C3463 Ethernet Hub board. There is one LAN connection on the front of the unit at J22, and three additional port connections on the rear labeled LAN SWITCH Port A, B, & C. A single WAN interface port on the rear of the enclosure is handled by a second independent Ethernet port on the LX800 CPU.

All internal boards connect together via the PC104 interface. This makes it easy to upgrade your device as application needs change. The I/O complement is fixed. However, its 16+ communication ports, coupled with a large suite of IED protocols, allow concentration of many types of data from down-stream devices.

5.1.1 PC/104 Architecture

The open architecture of the PC/104 bus interface provides for expanded functions. You may add a PC/104-based GPS receiver.

The PC/104 architecture is a compact version of the IEEE P996 (PC and PC/AT) bus, optimized for the unique requirements of embedded systems applications. The PC/104 bus derives its name from the 104 signal contacts on the two bus connectors (64 pins on P1, plus 40 pins on P2). The main differences from the IEEE P996 are:

1. Reduced form-factor (3.550 x 3.775 inches)
2. Self-stacking, eliminating need for backplanes or card cages

3. Minimized component count and power consumption (typically 1-2 watts per module) and reduced bus drive requirement (typically 4 mA)

5.2 LANDAC II Microprocessor Overview

Please refer to the CPU Manual

5.3 Hardware Design

The LANDAC II was designed to retrofit the original LANDAC RTU card cage, and cable connect to the existing I/O already wired in the field. The unit design is based on the Sage S3030 Magnum, but with augmented I/O capabilities required for a multi FIM LANDAC retrofit. The LANDAC II enclosure height is increased an additional two inches to incorporate the additional C3810 circuit board, and additional I/O ribbon cable connections. This board along with the S3030 Magnum I/O count gives the LANDAC II the largest single unit point count of any Sage RTU.

The LANDAC II hardware design for control and status inputs are identical to other Sage RTU's and will directly connect to any and all existing termination boards of LANDAC vintage and later. The analog sub-section, however, is specific to the LANDAC, and will only connect to the C3130 analog input XT. The internal architecture of the ADC circuitry is also unique for this RTU over other Sage designs in that it incorporates 2 independent Analog Converter IC's to accomplish reading all 320 analog inputs with proper filtering and 60HZ rejection within 1 second.

5.3.1 Power Input

The power requirements of the LANDAC II depend on the variance. The two choices are: 85-350VDC and 85-264VAC universal supply, or 20-60VDC. An internal power supply accepts the input voltage, and transforms it into +5V, +/-15V for internal use.

5.3.2 LEDs

See Section 4.2.1 LED Display

5.3.3 PC/104 Bus Interface/Connector

The bus interface connector is compatible with the PC/104 Consortium specification.

Contact the Consortium at:

PC/104 Consortium
849 Independence Ave., Suite B
Mountain View, CA 94043
Phone: 650.903.8304
Fax: 650.967.0995
Email: info@pc104.org

The PC/104 standard is available on the web in downloadable PDF format at:

URL: http://www.pc104.org

5.3.4 Communication Ports

The LANDAC II has sixteen (16) RS232 communications ports complete with LEDs for positive visual indication of data activity, and two other RS232 ports for Console and PPP. Baud rates are individually selected by port for rates between 300 baud and the maximum baud rate allowed by the protocol. The Console port is dedicated at 9600 baud.

This section will discuss the operation of one RS-232 port which is identical for the remaining 15 ports. Refer to Schematic diagram C3800-002-REV-C, pages 3 – 6 in Appendix D.

The main component is the 85230 communications processor, (U1). This device handles the data to and from the CPU, generates the baud rate for the port, and is capable of handling synchronous and asynchronous communications simultaneously for two individual comm. Ports. Data communications is level shifted from TTL to RS-232 levels and back by U2, an LT1141 RS-232 to TTL converter. Signals on the left side are TTL level, while signals on the right are RS-232. A voltage for Port power is generated by enabling DTR via the Communications configuration screen. This signal will turn on the Gate of Q1 causing current flow from Drain to Source. This puts power through L1 and CR5 to the PORT PWR Pin 1. Connection to a field RS-232 communications device terminates at J2.

The internal signals are defined as follows:

Pin 1	PORT1PWR	External power for field comm. equipment, 5V@30ma. Max.
Pin 2	RX#	Receive Input from field comm. equipment, RS-232 levels.
Pin 3	TX#	Transmit Output to field comm. equipment,RS-232 levels.
Pin 4	IRIG-B	Demodulated IRIG-B signal for field comm. Equipment.
Pin 5	DGND	Signal Ground.
Pin 6	IRIG_GND	Return Ground for IRIG-B signal.
Pin 7	RTS	Request to Send signal from Telvent Device
Pin 8	CTS	Clear To Send response from field comm. Equipment.
Pin 9	NC	No connection

All RS232 communication ports share a common interrupt and receive a 14.7458 MHz clock. The internal clock gives them the ability to receive and transmit data at up to 115.2 K.

The Console and PPP Ports are handled by the LX-800 CPU internally. The C3800 only acts as an interface connection between the field and the CPU, as illustrated on Sheet 8 of the schematic diagram, C3800-002-REV-C.

Additionally, the LANDAC II has five 10/100MBit Ethernet ports derived from two independent Ethernet ports on the LX-800 CPU. The first Ethernet port of the LX-800 CPU connects to a C3863 Ethernet Hub to supply three additional LAN ports. The second Ethernet port on the LX-800 CPU is determined as the WAN port.

5.4 Select Before Operate

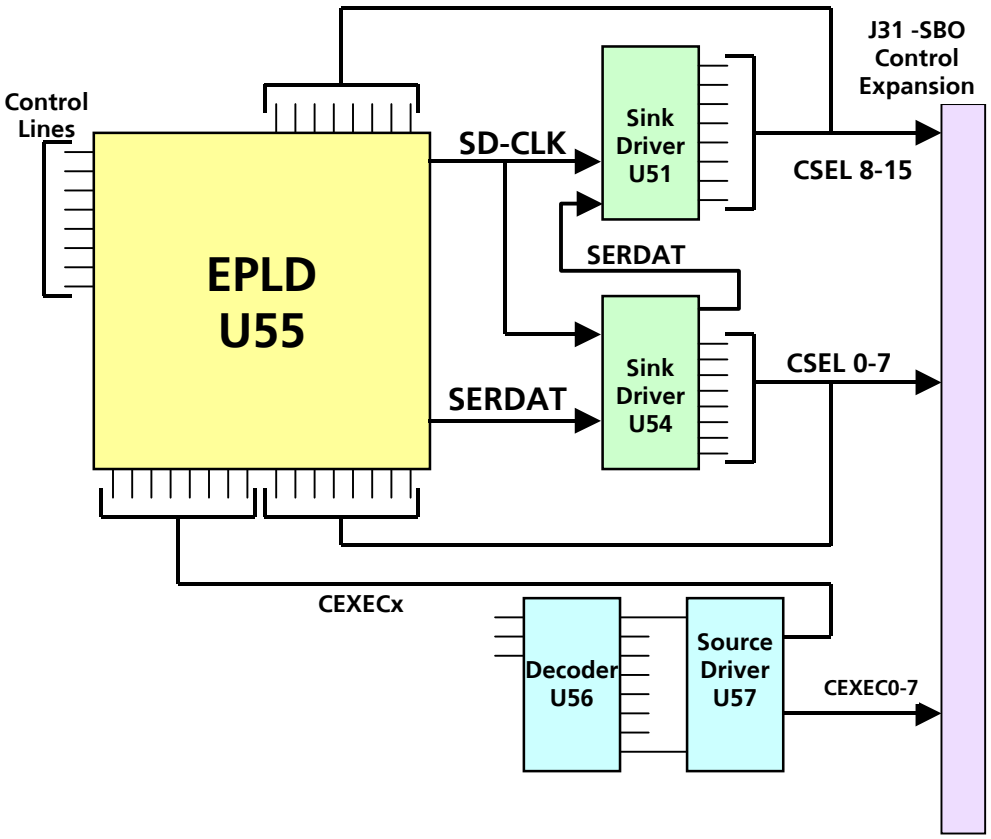
As stated above, the first 128 SBO points are generated on the C3810 board, and the remaining 64 are generated on the C3800 baseboard. Both interfaces are similar as described here, with the exception that the C3810 has additional line decoding to allow for an extra Source Driver to be added, increasing the total number of control points from 64 to 128. The following will describe the SBO operation for the C3800 baseboard. The C3800-002-REV-C Schematic diagram will be used for the following explanation.

The SBOs are controlled by an Erasable Programmable Logic Device (EPLD U55). This chip reads the information from the Data bus and performs a parallel to serial shift on the data. This data is then shifted out to two 8 bit Sink Drivers (U51,U54) to load all 16 CSEL outputs. The EPLD (U55) then decodes the address for the EXECUTE line by enabling U56 with 1 of 8 possible outputs to be driven by the 8 bit source driver (U57). Read back for the correct operation is handled through the resistor dividers back to U55.

All drivers have feedback resistor networks which allow the LANDAC II to monitor correct relay driver selection before execution is enabled. The sink drivers control the CSEL0 - CSEL15 lines. The source drivers control CEXEC0 – CEXEC7.

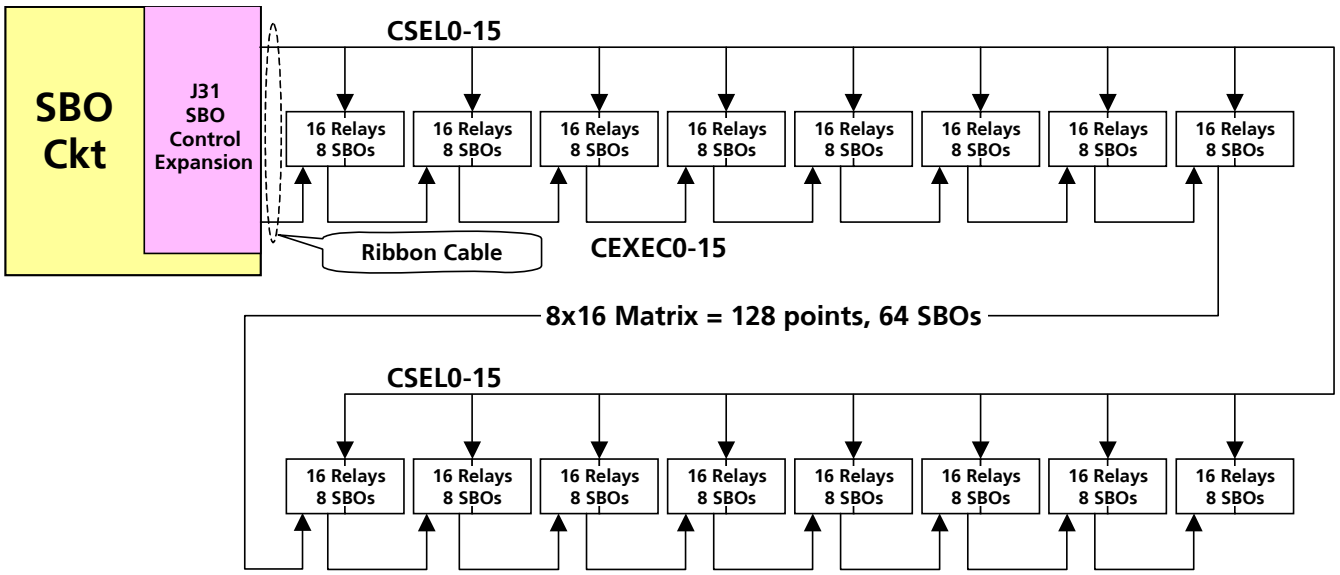
The relay driver matrix (16 X 8) can handle a maximum of 64 SBO points. Each SBO consists of a TRIP and a CLOSE relay. SBOs are limited to one at a time by hardware and firmware.

Figure 5-1 SBO Block Diagram



Another view of SBO addressing is shown in Figure 5-2.

Figure 5-2 SBO Matrix



5.5 Digital Input Expansion

The digital input subsystem accepts contact closure inputs as field status or low speed accumulator inputs. All inputs are optically isolated, and de-bounce by the firmware. Input processing is determined by the input assignment as status or accumulator, and is also firmware controlled. This allows the same hardware to be used for both types of inputs. Figure 5-3 is a simplified schematic of a typical digital input on an XT.

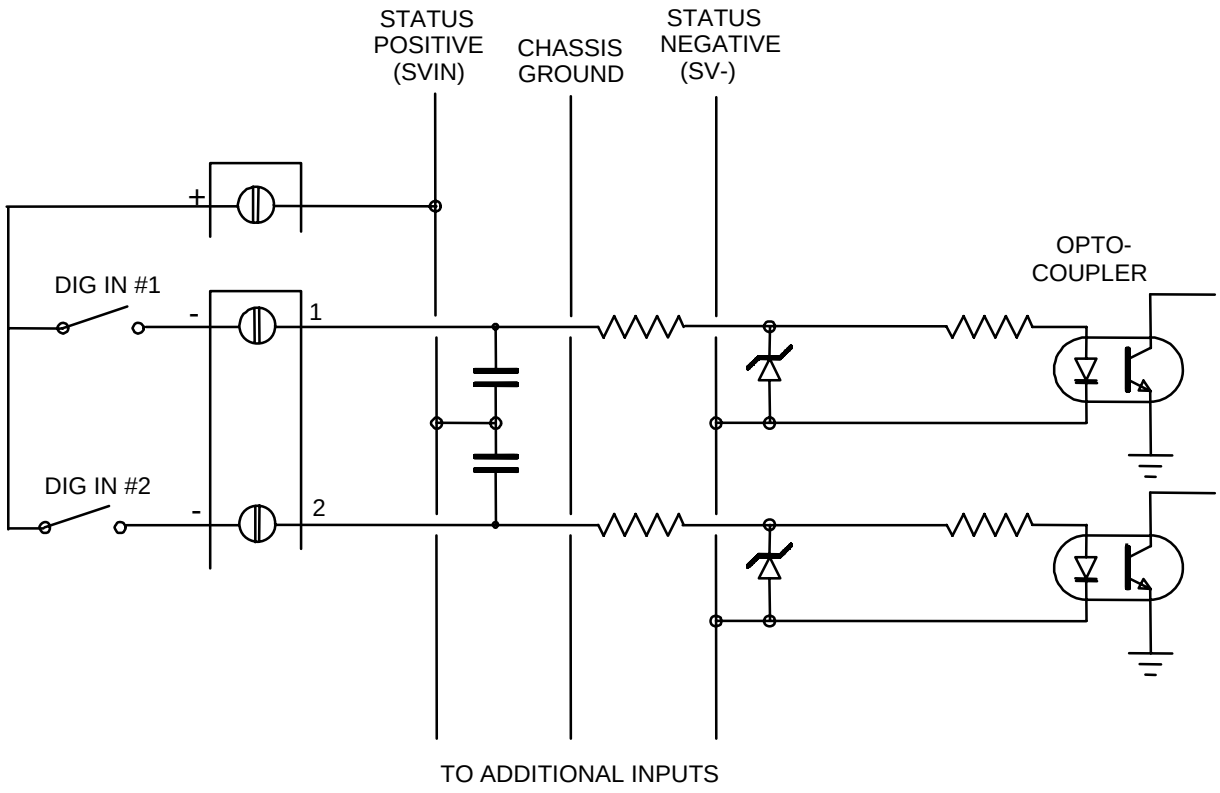
Data is allowed to settle before data onto the bus is read. A new status bank is selected by reading the I/O address of the requested status bank, ignoring the data, reading the same I/O address again, then processing the data.

The LANDAC II can address a total of 480 status inputs. The C3810 board addresses the first 256 status inputs, and the remaining 224 inputs from the C3800 baseboard. Since all status inputs are memory mapped, the circuitry on the C3800 and the C3810 are identical. Referring to the C3810, and C3132 schematics, a description of the first 32 points will be detailed.

EPLD (U16) the DI-AI EPLD is responsible for decoding SBSEL1 -7, LS-A0, LS-A1 and FIM1_DI#. The SBSEL signals and the LS-A0, A1 signals are buffered for the field by U7 and U8. The Status Data is read back through U6, controlled by the chip enable FIM1_DI#. Status Points 1 – 32 are enabled when a high is placed on SBSEL1 which in turn enables U33 of the first status XT. With LS-A0 and LSA1 both low, U33 output EN0 is active low causing U34 to enable its output and present Status Points 1 through 8 onto the Buffered Status Data bus. This bus is the input of U6, and when enabled, the data bits are placed on the processor data bus to be read. Once read, LS-A0 will go high causing U33 to enable EN1. This signal will tri-state U34, and enable U36, this time placing inputs 9 – 16 onto the Buffered Status Data Bus to again be read by the Processor during the next read cycle. This process repeats for EN2, reading Points 17 – 24 and EN3, reading points 25 – 32. Then the process starts again with BSEL2 for the next group of 32 inputs, and so on until BSEL8 is read.

Figure 5-3 shows the field side of the Status Input XT. The odd numbered terminals are the wetting voltages for the input points, the even numbered terminals are the actual input. A typical Status input is filtered by a .01UF 1000VDC Capacitor. This capacitor also serves as the main component for common mode transients from the field. The Status input voltage is then current limited by a 1Watt resistor. The size of this resistor is determined by the variance of the board, and typically ranges between 2K and 20K. A Zener diode CR1 clamps the input to be no more than 8.2V. DS1 provides visual indication of a closed status point, and the status input is optically coupled into the RTU logic by U1 an H11L1 Optocoupler. The normal state of the Optocoupler output is pulled to +5V with no status input voltage present, and driven low when voltage is present at the optocoupler input

Figure 5-3 Typical Digital Input



5.5.1 Firmware Debounce Algorithm

The Digital Inputs are processed through a digital filter to prevent erroneous Changes Of State (COS) being reported because of contact bounce. The inputs are sampled each 5 msec. Any input that does not match the state of the previous scan is time stamped and stored as a possible COS. A 20 msec counter is started for the suspect input. When the 20 msec expires, the point is again sampled. If it has remained steady it is considered to be a valid COS. The COS flag is set and the status buffer is set to the new point condition. A hardware RC network on each digital input provides additional filtering.

5.6 Analog Input Expansion

The LANDAC II is capable of reading 320 analog inputs from four groups of 5 termination panels each providing terminations and signal conditioning for 16 channels. The XT provides the current to voltage conversion, converts the differential input to a single ended signal, and attenuates the input by a factor of 0.4. The XT includes a simple low pass RC filter for noise rejection and provides approximately 60dB of common mode rejection. It includes a 16 channel multiplexer such that its output to the LANDAC II is one single –ended analog signal. The LANDAC II receives the signal from the selected XT, adds appropriate gain to satisfy the +/-3VPP input of the A/D converter, and once converted, the 12bit data is ready for reading by the processor.

Since all inputs are required to be updated each second, the LANDAC II utilizes 2 independent ADC converters that convert two points at the same time, and is read by the processor with successive reads. Below is a breakdown of the AI XT ports, their associated points, and which ADC circuit converts them.

AIXT	Analog Board Select	Points	ADC
J1	ADBSEL0 -7	1 -80	#1 (U14)
J2	ADBSEL0-7	81-160	#2 (U15)
J3	ADBSEL8-15	161- 240	#1 (U14)
J4	ADBSEL8-15	241 – 320	#2 (U15)

As an example, analog points 1 and 81 are both selected at the same time, converted by a different A/D converter, and then read separately by the processor. This ensures that all analog points will be converted every second at a rate of one point every millisecond.

Refer to C3810 schematics, pages 3 and 2 for the following circuit description. On the rising edge of the 1msec clock, the LX-800 processor writes a data pattern to the address location for the C3810 analog subsystem. The DI-AI EPLD(U16) decodes this data to drive four channel selects (A-A0 – A3), and 16 board selects ADBSEL0-15. These signals are presented to U25 – U32, 8 channel bus transceivers to drive the four AIXT ports, J1 – J4. The selected analog signal(s) are read back on Pin 6 of J1 – J4, and make up four inputs of the quad multiplexer U20. This multiplexer switches in either ports 1 & 2, ports 3 & 4, or a common set of board references. The OUTA side of U20 feeds A/D1_input, and the OUTB side of U20 feeds the A/D2_input. Instrumentation Amplifiers, U18, and U19 increase the signal gain to the full span of the A/D converter(s), U18 & U19. The signals are buffered through U17a&b before entering the A/D converter. Signal conversion takes place 4 us after the 1msec clock transitions from high to low. Conversion takes less than 10us before valid data is presented to D0-D11 pins of the converters. Bus transceivers U10 – U13 presents the valid data to the data bus when read by the processor in successive reads before the next rising edge of the 1msec clock

APPENDIX A

C3810 Design Document

LANDAC II

C3800/C3810 Design Document

29-Mar-2010

Version 0.8

This document describes the I/O structure of the Commonwealth Edison LANDAC II Upgrade Chassis. The document consists of the following sections:

C3800 Base Board
C3810 I/O Expansion Board
External Connections
External Switches
Environmental Specification
Switches Mounted on the Chassis
Board ID Register
Status Inputs
SBO controls
Analog Inputs
Special Logic for Combinations of Remote/Local Switch Positions

Each section contains I/O addressing and description of how the C3800 baseboard and C3810 I/O Expansion are used to meet the requirements of Commonwealth Edison.

The firmware provided will be the standard firmware offered with the SAGE product line with the addition of the Special Logic for Combinations of Switch Positions documented below and a CONITEL 2020 protocol master implementation.

C3800 Base Board

The existing Telvent C3800 Base Board will be used for serial I/O, part of the Status and part of the SBO control points. The features of this board are in the SAGE 3030 documentation.

C3810 I/O Expansion Board

The C3810 I/O Expansion Board will be designed and built for this project. The board has the following I/O complement:

256 Status Inputs read every 5 milliseconds
320 Analog Inputs read once per second
128 SBO controls
3 status inputs for monitoring position of 3 switches

The circuits used on this board will be copies of proven designs, reducing hardware risk in building the board and software time in that interfacing to the circuits has been completed for diagnostics and for application firmware.

The circuit for the status is copied from the C3800 baseboard with an additional board select added to allow for a total of 256 points on one status XT connector.

The circuit for the analog is copied from the C3830 PC/104 DC analog input board. Two sets of the C3830 board components are on the C3810 to allow for 320 points to be read from 4 XT connectors. The design is modified to accommodate addressing the C3130 DC analog XTs installed in the existing LANDAC RTUs.

The circuit for the SBO controls is copied from the C3400 baseboard for 128 points on two XT connectors of 64 points each.

External Connections

Analog Input – four 20 pin ribbon cable connectors – 80 points per connector
Status Input – two 20 pin ribbon cable connectors – 256 points 1st connector, 224 on 2nd
SBO Control – three 26 pin ribbon cable connectors – 64 points per connector

6 position removable Phoenix block

Position
1) Hot (+) (Existing wire Z28 on current LANDAC Power Converter)
2) Neutral (-) (Existing wire D26 on current LANDAC Power Converter)
3) Earth Ground (Existing wire Z8 on current LANDAC Power Converter)
4) No Connect
5) S01 Point 1 (Existing wire D22 on current LANDAC Power Converter)
6) S01 Point 1 (Existing wire Z24 on current LANDAC Power Converter)

External Switches

Existing SBM Switch mounted on front door

Environmental Specification

Operating Temperature: -40 to +85 DEGC.
Power Requirements: +125VDC or +48VDC
Internal power supplies: +5VDC, +12VDC, -12VDC, +15VDC, -15VDC, and +24VDC.

Switches Mounted on the Chassis

SBO Control Enable/Disable
IED Control Enable/Disable

Board ID Register

The board ID register will be at address 0x1C7 and be the ID value 0x18. At power up, the RTU firmware will read the address and verify that the I/O board drives the bus with the ID value. In addition, before performing an SBO control on the I/O expander card, the board ID register will be read and verified against the expected ID value before the output will be attempted.

The state of the SBO Control switch will be reported as Bit 0 of the C3800 board ID register.
The state of the IED Control switch will be reported as Bit 0 of the C3810 board ID register.

The SBO control flag CSEL shifting will be reported as Bit 1 of the C3810 board ID.
The state of the SBM Switch will be reported as Bit 2 of the C3810 board ID register.

Status Inputs

Requirements

480 status points spread across two buses, 256 on the first connector and 224 on the second connector.

This is met by using the status input circuits on the C3830 I/O board and the C3800 baseboard. The 256 status points on the C3810 I/O Expansion board are connected to connector J5 and the 224 points on the C3800 baseboard are connected to connector J6 on the rear of the chassis. The number of points entered into the configuration will be the total number of points for both buses. If the first bus is not fully populated and points are configured on the second bus, the first bus must contain 256 points and the point count must be increased accordingly.

Each C3800 baseboard I/O address read is 8 points, one bank from the status XT.

Each C3810 board I/O address read is 8 points, one bank from the status XT.

The I/O addresses are as follows:

C3800 Baseboard – 0x124 through 0x13F
C3810 I/O Expansion Board – 0x1A0 through 0x1BF

To latch the status bus data, the address is read and the result discarded. The address is read again and the data retained. The address is read a third time and this value is XORed with the previous read to use as the state of each point in the status bank. This data is read every 5 milliseconds and then run through the standard debounce algorithm in the RTU firmware. The range of addresses from 0x1A0 to 0x1BF will read the status bus on the C3810 expansion card (J5 connector on back of chassis). The range of 0x124 to 0x13F will read the status bus on the C3800 baseboard (J6 connector on back of chassis).

Firmware Configuration

The RTU GUI will have configuration for the total number of points connected to both connectors on the rear of the chassis. The range for the number of points ranges from 0 to 480. The point configuration parameters will be the same as for a C3800 baseboard point.

Testing the C3810 Status buses

The C3800 baseboard should have already been tested.

A C32XX I/O test fixture will be used to test the C3810 status bus.

Two C32XX I/O test fixtures will be used to do the Unit test.

SBO Controls

Requirements

192 SBO controls spread across three SBO buses.

This is met by using the 64 point SBO bus on the C3800 baseboard and adding two buses of 64 points to the C3810 I/O Expansion board. The number of points entered into the configuration will be the total number of points for all three buses. If a bus is not fully populated and points are configured on the next bus, the bus missing points must still contain 64 points and the point count must be increased accordingly.

The circuit for the 1st and 2nd SBO control bus on the C3810 will be identical to the design on the C3400 baseboard.

The address range for the C3810 SBO controls will be from 0x1C0 to 0x1C7.

The first connector (J7 on the rear of the chassis) services points 1 through 64 and is connected to the C3810 I/O Expansion Board. The second connector (J8 on the rear of the chassis) services points 65 through 128 and is connected to the C3810 I/O Expansion Board. The third connector (J9 on the rear of the chassis) services points 129 through 192 and is connected to the C3800 Baseboard.

Firmware Configuration

The RTU GUI will have configuration for the total number of points connected to the three connectors on the rear of the chassis. The range for the number of points ranges from 0 to 192. The point configuration parameters will be the same as for a C3800 baseboard point.

Testing the C3810 SBO Control buses

The C3800 baseboard should have already been tested.

Two C32XX I/O test fixture will be used to test the C3810 expansion buses.

Three C32XX I/O test fixtures will be used to do the Unit test.

Analog Inputs

Requirements

320 analogs spread across four analog buses

This is met by using the first 5 selects of the analog input bus (16 points per select, total of 80 points) on each of the four C3810 analog input bus connectors. The number of points entered into the configuration will be the total number of points for all four buses. If a bus is not fully populated and points are configured on the next bus, the bus missing points must still contain 80 points and the point count must be increased accordingly.

The circuit for the analog inputs on the C3810 will be copied from the design of the C3830 PC/104 DC Analog Input board. Like the C3830, all I/O will be 16 bit. This circuit will be doubled, with there being two Analog to Digital converters. There will be one set of select drivers which will pick the same channel to be converted on each bus at the same instant. There will be one set of references, for the analog to digital converters. Reference points will be available for mapping into protocols from each ADC. There is one output address (0x192) to select the channel, which will drive both connectors 1 & 3 or connectors 2 & 4 to the same channel for the reference or for the hardware input. Two different addresses will be used to read the data, 0x190 for the first ADC and 0x192 for the second ADC.

Two samples will be read for each point, 10ms apart for 50Hz filtering and 25ms apart for 60Hz filtering.

The first connector (J1 on the rear of the chassis) services points 1 through 80, the second connector (J2 on the rear of the chassis) services points 81 through 160, the third connector (J3 on the rear of the chassis) points 161 through 240, and the fourth connector (J4 on the rear of the chassis) points 241 through 320.

Firmware Configuration

The RTU GUI will have configuration for the total number of points connected to the four connectors on the rear of the chassis. The range for the number of points ranges from 0 to 320. The point configuration parameters will be the same as for a C3820 PC/104 DC Analog Input board point.

Two sets of references will be included in the points list. These references are the AGND, +5VDC, +4.5VDC, -4.5VDC, and the temperature point.

Testing the C3810 Analog buses

One C32XX I/O test fixture will be used to test the C3810 expansion buses.

Three C32XX I/O test fixtures will be used to do the Unit test.

Special Logic for Combinations of Remote/Local Switch Positions

The RTU shall inhibit controls in the following manner based on the state of the SBM Switch, SBO Controls Enable/Disable, and the IED Controls Enable/Disable.

The SBM switch state is shown in the "SBM LOCAL" LED on the front panel. When the SBM switch is in the local position, the LED will be on. When the SBM switch is in the remote position, the LED will be off.

When the SBO Controls Enable Switch is in the Enable position, the LED will be off. When the switch is in the Disable position, the LED will be on.

When the IED Controls Enable Switch is in the Enable position, the LED will be off. When the switch is in the Disable position, the LED will be on.

In the following table, the SBM switch is in the Off position, removing power from the device.

SBM OFF

SBO Control	IED Control	Result
N/A	N/A	Powered Off

In the following table, the SBM switch is in the Remote position providing Field Power to the devices connected to the interposing relay on the SBO control bus.

SBM Remote

SBO Control	IED Control	Result
Enable	Enable	All SBO relays, field powered devices and IED controls operate
Disable	Enable	SBO relays & field powered devices do not operate, IED controls operate
Enable	Disable	SBO relays & field powered devices operate, IED controls do not
Disable	Disable	SBO relays, field powered devices & IED controls do not operate

In the following table, the SBM switch is in the Local position removing Field Power from the devices connected to the interposing relay on the SBO control bus.

SBM Local

SBO Control	IED Control	Result
Enable	Enable	SBO relays operate, field powered devices do not operate, IED controls operate
Disable	Enable	SBO relays & field powered devices do not operate, IED controls operate
Enable	Disable	SBO relays operate, field powered devices & IED controls do not operate
Disable	Disable	SBO relays, field powered devices & IED controls do not operate

End of Document

APPENDIX B

Glossary

A/D	Analog to Digital
AC	Alternating Current
ACI	AC Input
ADC	Analog to Digital Converter
AI	Analog Input, also AIN
ANSI	American National Standards Institute
AO	Analog Output, also AOUT
ASCI	Asynchronous Serial Communications Interface
ASCII	American Standard Code for Information Interchange
ASIC	Application Specific Integrated Circuit
AWG	American Wire Gauge
baud	Modem speed in Bits Per Second
bps	Bits Per Second
bridge	A network device capable of connecting networks that use similar protocols
C	Celsius or the programming language C
CEB	Communication Expansion Board
check-back	Hardware/Software method of control output protection
CCITT	Comité Consultatif Internationale de Télégraphique et Téléphonique
CMOS	Complementary Metal Oxide Semiconductor
COMM	Communication, also COM
COS	Change of State
CPU	Central Processing Unit
CRC	Cyclic Redundancy Check; a method for error checking that detects randomly occurring single and multiple bit errors and is widely accepted for the detection of "burst" errors encountered in communication networks.
CTS	Clear To Send
DAC	Digital to Analog Converter
dBm	Decibels relative to 1mW
DC	Direct Current
debounce	Filtering of contact closure noise
DHCP	Dynamic Host Configuration Protocol – often used to refer to the network server that performs this function
DI	Digital Input
DFT	Discreet Fourier Transform
DMA	Direct Memory Access
DMM	Digital Multimeter
DNS	Domain Naming Service – often used to refer to the network server that performs this function
DO	Digital Output

DSP	Digital Signal Processor
DTR	Data Terminal Ready
DVM	Digital Volt Meter
EIA	Electronic Industries Association
EEPROM	Electrically Erasable Programmable Read Only Memory
EPLD	Electrically Programmable Logic Device
EPROM	Erasable Programmable Read Only Memory
Ethernet	A broadcast networking technology that can use several different physical media, including twisted pair cable and coaxial cable. TCP/IP is commonly used with Ethernet networks.
FB	Function Block – an element is the Function Block Diagram graphical language
FBD	Function Block Diagram graphical language – one of the IEC 61131-3 programming languages
FC	Flow Chart graphical language – one of the IEC 61131-3 programming languages
FF	Flip-Flop
FIFO	First In First Out
FIP	Fieldbus implementation based on French standard
firmware	Program held in ROM or Flash memory
Flash Memory	A type of non-volatile storage device similar to EEPROM
FMR	Feeder Management Remote
FMS	Feeder Management System
form A	Relay contact, single throw, normally open
form C	Relay contact, double throw
FRF	Full Range Factor; a method used for analog scaling; $FRF = \frac{\text{Data Value} - \text{Data Min}}{\text{Data Max} - \text{Data Min}}$
FS	Full Scale
FTP	File Transfer Protocol – A TCP/IP application used for transferring files from one system to another
GPS	Global Positioning System
GUI	Graphical User Interface
H	Hexadecimal (base 16), as in XXXXh
HEX	Hexadecimal (base 16), as in XXXXh
HDLC	High-level Data Link Control
HSPCI	High Speed Pulse Counter Input
Hz	Hertz, frequency in cycles per second
I/O	Input/Output
ID	Identification
IEC	International Electro-technical Commission
IED	Intelligent Electronic Device
IEEE	Institute of Electrical and Electronic Engineers
IL	Instruction List language – one of the IEC 61131-3 programming languages
ISA	Instrument Society of America
ISO	International Standards Organization
ISP	Integrated Software Project – Fieldbus implementation using existing IEC standards
ITU	Intelligent Terminal Unit
JEDEC	Joint Electronic Device Engineering Council

k	Kilo - kB is kilobytes, kV is kilovolts, etc.
KHz	Kilo Hertz
LAN	Local Area Network
LCD	Liquid Crystal Display
LD	Ladder Diagram graphical language – one of the IEC 61131-3 programming languages
LED	Light Emitting Diode
LRC	Longitudinal Redundancy Check; uses both "horizontal" and "vertical" parity bits to detect errors in the messages between the Master and the RTUs. This technique is also known as Geometric Coding.
LSB	Least Significant Bit
mA	Milliampere
MAP	Manufacturing Automation Protocol
MEB	Memory Expansion Bus (also, Memory Expansion Board)
MHz	Megahertz
MMI	Man Machine Interface
MMS	Manufacturing Message Specification
MSB	Most Significant Bit
msec	Millisecond
MTU	Master Terminal Unit, also Master Station
MUX	Multiplexer
NC contact	Normally Closed relay contact
NEMA	National Electrical Manufacturers Association
NO contact	Normally Open relay contact
O/S or OS	Operating System
OSI	Open Systems Interconnection
oz	Ounce
PC	Power Converter, also Personal Computer
PCI	Pulse Counter Input
PF	Power Factor
PID	Three term controller, proportional, integral, derivative closed-loop control algorithm
PLD	Programmable Logic Device
PLC	Programmable Logic Controller
POU	Program Organization Unit
PPP	Point-to-Point Protocol – A TCP/IP protocol that provides host-to-host network and router-to-router connections. Can be used to provide a serial line connection between two machines.
pps	Pulses Per Second
PWR	Power
RAM	Random Access Memory
RLL	Relay Ladder Logic
ROM	Read Only Memory
router	A device that connects LANs into an internetwork and routes traffic between them
RS232C	EIA Serial data communications standard
RST	Reset
RTOS	Real Time Operating System
RTS	Request To Send
RTU	Remote Terminal Unit

Rx	Receive
SAP	Substation Automation Platform
SBO	Select Before Operate
SCC	Serial Communications Controller
SCADA	Supervisory Control And Data Acquisition
SCTO	Soft Carrier Turn Off
SDLC	Synchronous Data Link Control
SEB	Surge Protection Expansion Board
SFB	Sequential Function Block – one of the IEC 61131-3 programming languages
SFB	Special Function Bus
SFC	Sequential Function Chart graphical language
SOE	Sequence of Events
ST	Structured Text language – one of the IEC 61131-3 programming languages
STS	Status
SWC	Surge Withstand Capability, IEEE C37.90a 1978
TCP/IP	Transmission Control Protocol/Internet Protocol
Tx	Transmit
UART	Universal Asynchronous Receiver Transmitter
UIF	User Interface Function
USART	Universal Synchronous Asynchronous Receiver Transmitter
msec	Microsecond
UVPROM	Ultraviolet erasable Programmable Read Only Memory
VAC	Volts Alternating Current
VAR	Volt-Amperes Reactive
VARH	VAR Hours
VDC	Volts Direct Current
VxWorks	Real Time Operating System made by Wind River for embedded computer systems
W	Watt
Watchdog Timer	Circuit that resets CPU if it fails to execute program
WH	Watt Hours
XB	Expansion Board
XML	Extensible Markup Language – The method used be Telvent for the storing and retrieval of config@WEB RTU data. The data is stored in the form of a series of XML files (files with an XML extension).
XT	External Termination (panel, module or assembly)

APPENDIX C

Index

APPENDIX D

Drawings

The following schematic and assembly drawings are included in this manual as a convenience to allow for troubleshooting.

Part Number	Revision	Description	# of pages
B1577-003-REV-A	A	LANDAC II Test Procedure	6 pages
B1577-LD2-0000X	C	LANDAC II Chassis Assembly	5 pages
B1577-LD2-F0001	0	LANDAC II Rack Mounting Enclosure	6 pages
B1577-LD2-F0002	0	Front Panel Fab. For LANDAC II	2 pages
C3800-000-00001	G	Assembly, PCA SAGE 3030, Substation Automation Platform	2 pages
C3800-002-REV-C	C	Schematic, Substation Automation Platform	8 pages
C3800-002-PLDA1	A	CSPLD_U44	1 page
C3800-002-PLDA2	A	COMMPLD_U30	1 page
C3800-002-PLDA3	A	PIC_PLD_U39	1 page
C3800-002-PLDA4	A	STATUS_U50	1 page
C3800-002-PLDA5	A	SBOPLD	3 pages
C3810-002-REV-B	B	Schematic SAP I/O Expansion Board	5 pages
C3810-002-PLDA3	A	SBO EPLD	3 pages
C3820-000-00001	B	Assembly, PCA S3030 Display Board	1 page
C3820-002-REV-B	A	Schematic, LED Display Board	2 pages
C3800-CB1-00001	B	Cable Assy for SAGE 3030 Power Input & Power Distribution	1 page
C3810-000-00001	B	SAP I/O Expansion Board	1 page
C3130-000-XX00X	J	Analog IN-XT	2 pages
C3132-000-X000X	K	Digital IN-XT	2 pages
C3133-A00-XX100	H	SBO XT	1 page
C3130-002-00000	O	Analog IN-XT Schematic	1 page
C3132-002-REV-C	C	Digital IN Schematic	2 pages
C3133-002-REV-A	A	SBO XT Schematic	2 pages

SYM	ECO NO.	DATE	BY	CHECK	DESCRIPTION

Telvent

B1577-LD2-0000X

LANDAC II Test Procedure

Equipment List:

Bench Top Power Supply (capable of 24 – 129VDC @ 2A)
AC / DC Digital Multi-meter
Oscilloscope
IRIG-B Signal Generator or
C3800 Stand Alone Test fixture for IRIG-B signal Generation
BNC cables and connections for Oscilloscope
C3890 RS-232 Test Boards X 2
LANDAC II Test Rack with the following:
C3825-000-00001 LANDAC II TEST BOARD
Cross over Ethernet Cable (B0000-079-11500)

Computer with 1 Serial Port, 1 Ethernet Port, 2 USB Ports
Installed Firmware
Windows XP or Equivalent with Internet Explorer 6.0

Landac II Application Code C3414-500-001F0 with Test Configuration

LAN IP address 172.18.150.50 WAN IP Address 173.18.150.50
Subnet Mask 255.255.0.0

USER Name: Admin
Password: Telvent1!

Variance Check:

Verify the variance of the assembly with the Bills of Material. Identify that all boards are installed and cabled properly. Verify the input voltage to be applied, and adjust the bench supply accordingly. Visually check that all cables and connections are properly mounted to the enclosure and connected to the proper location.

Set Up:

On the host computer set the Ethernet port to use the following IP address, 172.18.150.48, and the subnet mask to 255.255.255.0.
Disable and then enable the Ethernet port.
Connect the supplied Ethernet cable between the UUT and the host computer. Connect the I/O Test board cables to J1-J9, and Test plug into TB1. Install the two C3490 RS-232 Test boards to the 16 DB9 connectors.

Power-Up Check:

Front Panel LED's

Apply appropriate power to the board through TB1.
Upon power-up, verify that the following LED's are illuminated during RESET.

Power	Time Source Failed	User Logged In
Run	IED Failed	Config Changed
		RLL Running
SMB Local		Ethernet Link

Once the RESET has occurred (30 sec.), the following LED's will Illuminate.

Power	
Run (Blinking)	
SBM Local	Ethernet Link

SYM	ECO NO.	DATE	BY	CHECK	DESCRIPTION

Voltage Check:

Verify that all voltages are present on the main board by probing between the test point and DGND with the Multi-meter.

Voltage	Test Point	Maximum	Typical	Minimum
5V	TP17	5.25V	5.00V	4.75V
+15V	TP21	15.750V	15.00V	14.250V
- 15V	TP22	-14.250V	-15.00V	-15.750V
+12V	TP19	12.600V	12.00V	-11.400V
-12V	TP18	-11.400V	-12.00V	-12.600V
8V	TP16	8.400V	8.000V	7.600V

Reset Button Test:

Verify the operation of the Reset Pushbutton by pressing and allowing the unit to reset. Observe that the RESET LED will illuminate when the button is depressed, and will extinguish when released. The unit is completely reset and booted when the "Run" LED starts flashing approximately every second.
Enter the following IP address into Internet Explorer, "172.18.150.50". When the LANDAC II Log-In Screen loads, type in the following:

Username: Admin
Password: Telvent1!

Then Click the "Login" button.

Download Test Config:

From the "Config@WEB" (Main Menu) screen, select the "Up/Download" Tab from the top menu. Enter the "User Name" and "Password" in the "Connection" box, and then press "Connect". From the "File Type" pull down menu, select "Configuration", and then click on "Send to RTU". A Pop Up window will appear allowing you to navigate to the configuration folder. Select the XML folder and click "open". The new application will download to the UUT. When finished, click the "Reset" button and allow the unit to reset again.
'Re-Enter the setup by entering the Username and Password.

SYM	ECO NO.	DATE	BY	CHECK	DESCRIPTION

Communications Port Test:

Verify that Comm Port 1 – 16 LED's on the front panel are flashing, and that the DCD/+5V LED's are on constantly. Also on the rear test boards, verify that the LED's for Port Power are all illuminated. The Con and PPP Port LED's will not light up during this test

IRIG-B Generation Test:

View the front panel and verify that the"Time Source Failed" LED is illuminated, and that the IRIG-B LED's on the rear C3890 test boards are extinguished. Connect the IRIG-B Output from the C3800 Test Box to the IRIG-B Input BNC connector on the rear of the UUT. All 16 of the IRIG-B LED's on the two test boards should flicker, and the "Time Source Failed" LED will extinguish.
View the IRIB-B Output BNC Connector with an oscilloscope to verify that the IRIG-B signal is present. Remove the source, the signal should go away, the rear LED's will extinguish, and the "Time Source Fail" LED will re-illuminate on the front Panel.

Ethernet Hub Test:

Click on the "Data Display" Tab, and then to the "References" tab. Click back and then "References" Tab again several times. Remove the Ethernet cable from the front RJ45 port and install it in one of the rear LAN Switch connectors. Again click on the "References" tab and then Back. Repeat for all Port connections.

WAN Port Test:

Log out of the GUI, and exit out of Internet Explorer. Adjust the host computer Ethernet port to use static IP address 173.18.150.48, and a sub net mask of 255.255.255.0. Disable and then Enable the Port. Plug into the "WAN" connection port of the Landac II, and enter the IP address of 173.18.150.50. The GUI will open up the log in screen again. Ensure that you can log in and browse the RTU screens.

Field I/O Tests:

Visually look at the I/O test Board and note that the LED's for the Analog and Status Inputs flash in a systematic way. If a section is not flashing, or sections do not appear to be normal, there may be interconnection issues with the internal cables.

References:

Click on the "Data Display" tab, and select the References.
Verify the following:

ADC#1, ADC#2	AGND	0.001 +/-0.003
ADC #1, ADC #2	Full Scale	5.000 +/-0.003
ADC #1, ADC #2	+90%	4.500 +/-0.005
ADC#1, ADC #2	-90%	-4.500 +/-0.005

Analog Inputs:

Click "Back" and return to the Config@WEB Screen. Click the "Data Display" Tab, and then select "Analog Inputs". A page of 16 inputs will be displayed. Verify that the odd numbered points read over 5.00V, and the even numbered points read close to zero volts. Note that this is Page 1 of 20 pages. Click "Next" to advance pages. Pages 1, 6, 11, & 16 will show the alternating values per point, all other pages will be around zero volts for the values. The accuracy of the values are not critical, this test is to access all configured points. Inspect the LED's on the Test Board. They should be flashing in sequence in a uniform manner. Notice that only the first 5 Board Selects are actively flashing, the remaining 3 will be static. Also verify that the Voltage LED's are illuminated indicating Power available.

Status Inputs:

Click "Back" and return to the Config@WEB page, and then select "STS". The display will show a list of 16 Status Inputs with Points #1 and #9 in the "CLOSED" state, and all others in the "OPEN" state. Click Next to Page 2 of 30. Notice that the points did not change. Click "next" to advance to Page 3 of 30. This time the "CLOSED" points shifted down to Points #50, and #58. This pattern will continue for all odd numbered pages.

SYM	ECO NO.	DATE	BY	CHECK	DESCRIPTION

Control Outputs:

Click "back" to return to the "Main Page". This time select the "Command" Tab from the top of the menu, and then select "Controls". The screen will display a page of 16 controls. Select point 1 "TRIP", and then press the "Execute" button. View the Test Board and verify that the CEXEC1 and CSEL0 LED's for Group 1 Illuminate for 2 seconds. Now select point 1 "Close" and press the "Execute" button. View the test board and verify that the CEXEC1 and CSEL1 LED's Illuminate. This pattern will continue for the first 8 Control Points. Once all 16 Select LED's are tested, the remaining Execute lines can be tested by controlling every 8th Trip Point for each group of 64 control points. Repeat for Control group 2 and Group 3.

SBO Control Switch:

Switch the "SBO" switch on the front panel to the UP (Disable) Position. The LED within the Switch will illuminate. From the "Control "Tab on the screen, try to execute a control as above. The LED's on the test board should not illuminate, and there will be a "Select Failure" at the bottom of the Command SBO screen. Reset the switch to "ENABLE".

IED Control Switch:

Switch the "IED" switch on the front panel to the UP (Disable) Position. The LED within the switch will illuminate, and the "Alarm 1" LED on the front Panel will also illuminate after a short delay. Reset the switch to "ENABLE" and the LED's will extinguish.

SBM Switch:

Switch the "SBM" switch on the TEST Board to the UP (REMOTE) Position. The SBM Local LED will extinguish, and the "Alarm 2" LED on the front Panel will illuminate after a short delay. Reset the switch to "LOCAL" and the SBM Local LED will illuminate and the Alarm 1 LED extinguish.

Wrap UP:

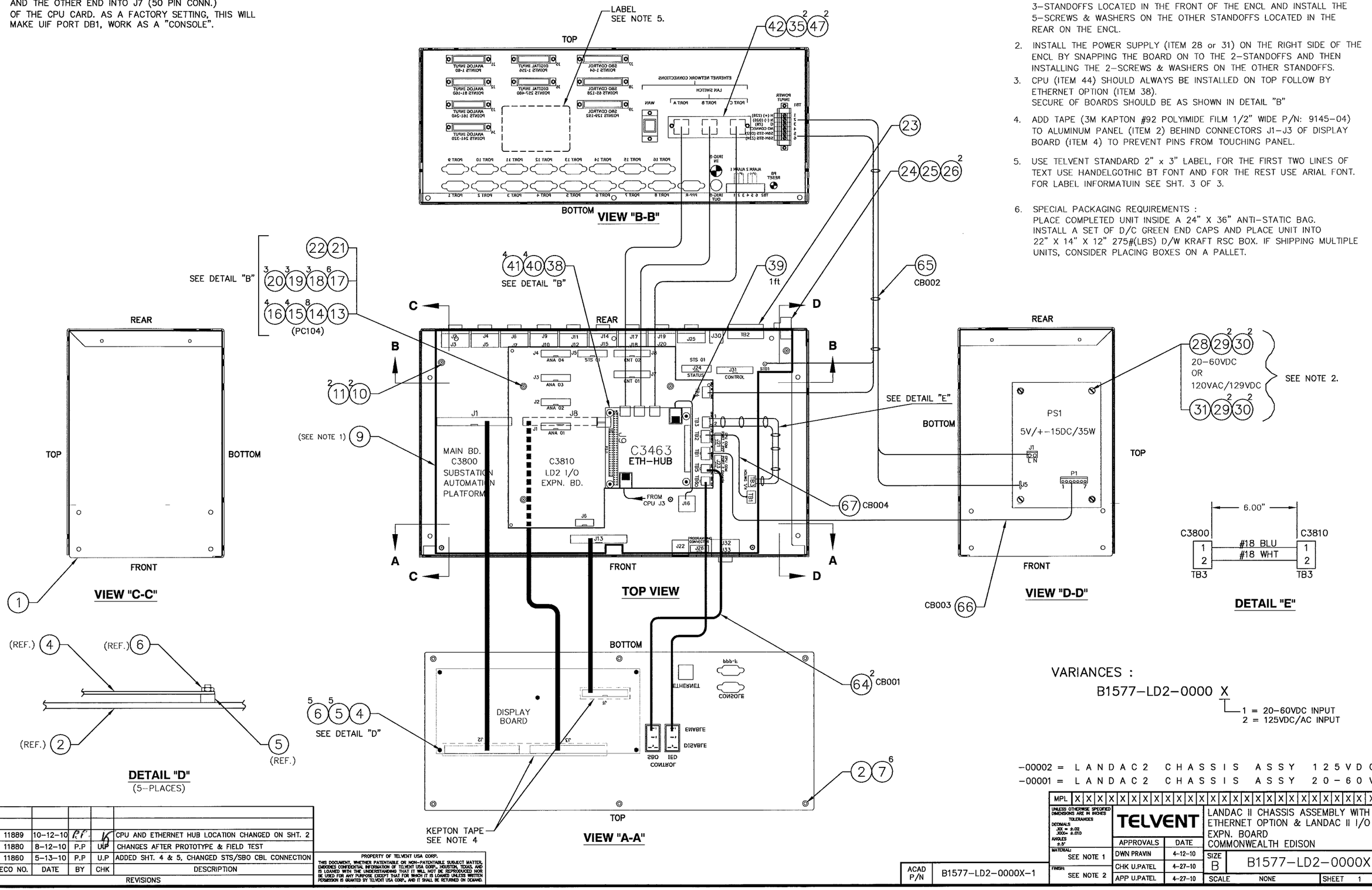
Once all test are satisfactorily completed, remove all test cableing from the unit under test. Remove Unit from test rack and install cover to top of unit with 7 attaching screws. Affix Label with test stamp and date to side area of Unit.

CPU NOTE :

INSTALL CABLE ASSEMBLY (10 PIN CBL CONN. WITHOUT RED STRIP "CONSOLE") INTO BASEBOARD CONNECTOR J1, AND THE OTHER END INTO J7 (50 PIN CONN.) OF THE CPU CARD. AS A FACTORY SETTING, THIS WILL MAKE UIF PORT DB1, WORK AS A "CONSOLE".

NOTES:

1. INSTALL BASEBOARD (ITEM 9) IN THE BOTTOM OF ENCL BY LINING UP THE CONNECTORS ON THE PCA WITH THE CUTOUTS ON THE REAR OF ENCL AND SLIDING THE PCA IN. THEN SNAP THE BOARD ON TO THE 3-STANDOFFS LOCATED IN THE FRONT OF THE ENCL AND INSTALL THE 5-SCREWS & WASHERS ON THE OTHER STANDOFFS LOCATED IN THE REAR ON THE ENCL.
2. INSTALL THE POWER SUPPLY (ITEM 28 or 31) ON THE RIGHT SIDE OF THE ENCL BY SNAPPING THE BOARD ON TO THE 2-STANDOFFS AND THEN INSTALLING THE 2-SCREWS & WASHERS ON THE OTHER STANDOFFS.
3. CPU (ITEM 44) SHOULD ALWAYS BE INSTALLED ON TOP FOLLOW BY ETHERNET OPTION (ITEM 38).
   SECURE OF BOARDS SHOULD BE AS SHOWN IN DETAIL "B"
4. ADD TAPE (3M KAPTON #92 POLYIMIDE FILM 1/2" WIDE P/N: 9145-04) TO ALUMINUM PANEL (ITEM 2) BEHIND CONNECTORS J1-J3 OF DISPLAY BOARD (ITEM 4) TO PREVENT PINS FROM TOUCHING PANEL.
5. USE TELVENT STANDARD 2" x 3" LABEL, FOR THE FIRST TWO LINES OF TEXT USE HANDELGOTHIC BT FONT AND FOR THE REST USE ARIAL FONT. FOR LABEL INFORMATUIN SEE SHT. 3 OF 3.
6. SPECIAL PACKAGING REQUIREMENTS :
   PLACE COMPLETED UNIT INSIDE A 24" X 36" ANTI-STATIC BAG.
   INSTALL A SET OF D/C GREEN END CAPS AND PLACE UNIT INTO 22" X 14" X 12" 275#(LBS) D/W KRAFT RSC BOX. IF SHIPPING MULTIPLE UNITS, CONSIDER PLACING BOXES ON A PALLET.



VARIANCES :

B1577-LD2-0000 X

1 = 20-60VDC INPUT
2 = 125VDC/AC INPUT

-00002 = LANDAC2 CHASSIS ASSY 125VDC/AC
-00001 = LANDAC2 CHASSIS ASSY 20-60VDC

SYM.	ECO NO.	DATE	BY	CHK	DESCRIPTION
B	11889	10-12-10	P.P	U.P	CPU AND ETHERNET HUB LOCATION CHANGED ON SHT. 2
B	11880	8-12-10	P.P	U.P	CHANGES AFTER PROTOTYPE & FIELD TEST
A	11860	5-13-10	P.P	U.P	ADDED SHT. 4 & 5, CHANGED STS/SBO CBL CONNECTION

REVISIONS

MPL | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES
DECIMALS
.XX = ±.02
.XXX= ±.010
ANGLES
± 5°
MATERIAL:
SEE NOTE 1
FINISH:
SEE NOTE 2

TELVENT

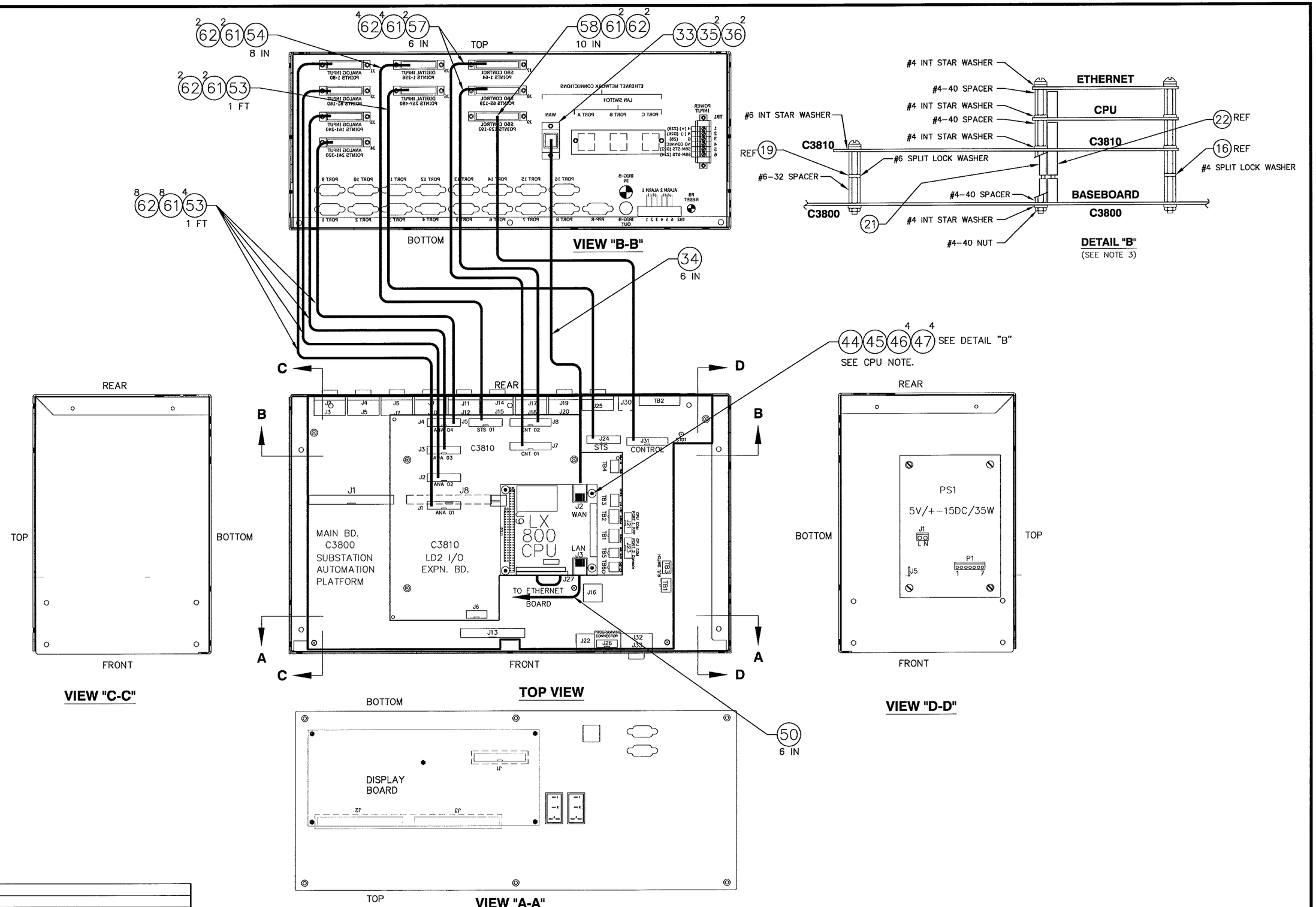
LANDAC II CHASSIS ASSEMBLY WITH CPU, ETHERNET OPTION & LANDAC II I/O EXPN. BOARD
COMMONWEALTH EDISON

APPROVALS	DATE
DWN PRAVIN	4-12-10
CHK U.PATEL	4-27-10
APP U.PATEL	4-27-10

ACAD P/N	B1577-LD2-0000X-1

SIZE B | B1577-LD2-0000X | REV C

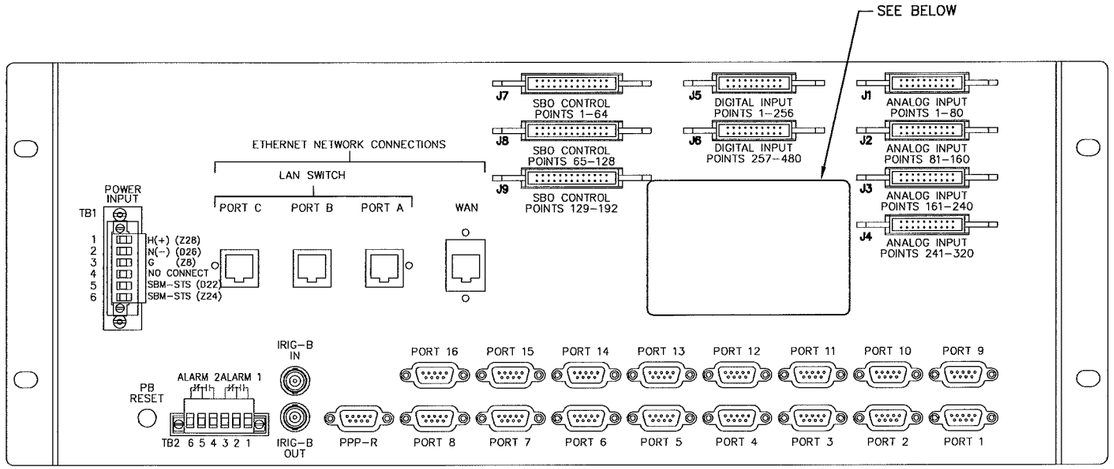
SCALE NONE | SHEET 1 OF 5



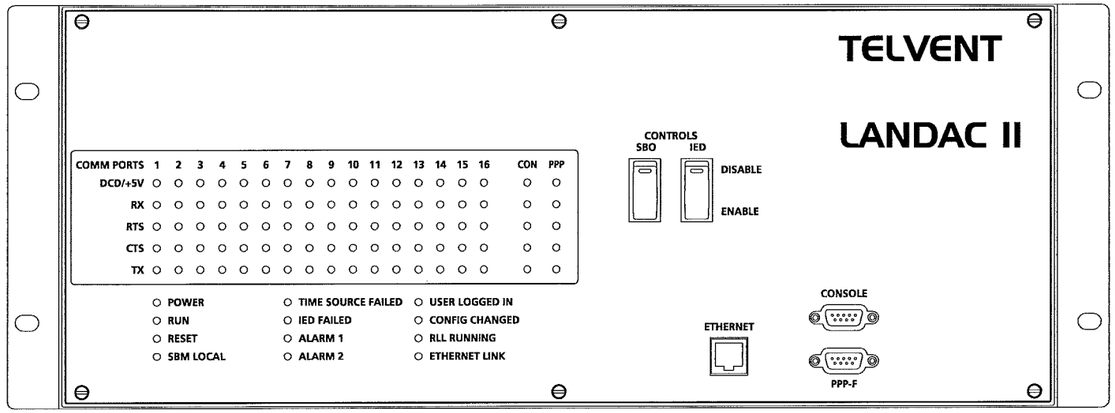
SYM.	ECO NO.	DATE	BY	CHK	DESCRIPTION
C	11889	10-12-10	P.P		SEE SHT. 1
B	11880	8-12-10	P.P	U.P	SEE SHT. 1
A	11860	5-13-10	P.P	U.P	SEE SHT. 1

REVISIONS

ACAD P/N	B1577-LD-0000X-2	APPROVALS	DATE	SIZE B
		DWN PRAVIN	4-12-10	B1577-LD2-0000X
		CHK U.PATEL	4-27-10	REV C
		APP U.PATEL	4-27-10	SCALE NONE
				SHEET 2 OF 5



REAR VIEW



FRONT VIEW

LABEL DETAIL

(SEE NOTE 5)

TELVENT LANDAC II
Substation Automation Platform
B1577-LD2-00001
20-60VDC W/LX 800 & ETH
W.O.# REV- SN#
Input Voltage Range
20-60VDC

LABEL - A

TELVENT LANDAC II
Substation Automation Platform
B1577-LD2-00002
125VDC/AC W/LX 800 & ETH
W.O.# REV- SN#
Input Voltage Range
85-350VDC, 85-264VAC

LABEL - B

QTY	QTY	ITEM	PART NUMBER	DESCRIPTION	NOTES
1	1	1	B1577–LD2–F0001	ENCL RACK MTG F/LANDAC2 COM–ED	
1	1	2	B1577–LD2–F0002	PNL FRONT F/LANDAC2 COM–ED	
1	1	3	B1577–003–REV–A	TEST PROCEDURE LD2 UNIT	
1	1	4	C3820–000–00001	PCA S3030 DISPLAY BOARD	DISPLAY BD.
5	5	5	B0002–272–00001	SPACER NY 1/8 1/4R NA 0.140	
5	5	6	B0000–861–00001	NUT HEX 6–32 FXLK	
6	6	7	B0002–173–00002	SCREW–MACH 6–32 FM SS 0330	
		8			
1	1	9	C3800–000–00001	PCA SAGE 3030 SAP MAIN BOARD	MAIN BD.
2	2	10	J0294–021–00000	SCREW–MACH 6–32 BH SS 0312	
2	2	11	J4001–109–00000	WASHER LOCK INT NO 6 CPS	
		12			
1	1	13	C3810–000–00001	PCA LD2 I/O EXPN BD	LD2 I/O EXPN.
8	8	14	B0002–980–00000	STANDOFF AL 0.625 3/16H MF 4–40	
4	4	15	B0000–534–00000	WASHER LOCK INT NO 4 SS	
4	4	16	B1002–021–00000	WASHER LOCK SPLIT NO 4 SS	
6	6	17	B0001–254–00625	SPACER AL 0.625 1/4H MF 6–32	
3	3	18	J4001–109–00000	WASHER LOCK INT NO 6 CPS	
3	3	19	J0000–180–00000	WASHER LOCK SPLIT NO 6 SS	
3	3	20	J0294–021–00000	SCREW–MACH 6–32 BH SS 0312	
1	1	21	J0000–551–10020	CONN PCB SQ 20POS PC104 F LONG	
1	1	22	J0000–551–10032	CONN PCB SQ 32POS PC104 F LONG	
1	1	23	B0002–882–10006	CONN PLG FEM 06P .197 HRZ	ALARM (TB2)
1	1	24	B0002–882–30006	CONN PLG FEM 06P .200 HRZ	POWER INPUT TB1
1	1	25	B0002–882–40006	CONN FRAME PNL MTG 06P .200	
2	2	26	B0001–238–00000	SCREW–MACH 4–40 BH SS 0187	
		27			
–	1	28	B0002–960–10001	P/S 20–60VDC 5V/+–15VDC/35W CC	PS1
2	2	29	J0294–021–00000	SCREW–MACH 6–32 BH SS 0312	
2	2	30	J4001–109–00000	WASHER LOCK INT NO 6 CPS	
1	–	31	B0002–960–00001	P/S 85–264AC/DC 5V/+–15VDC/35W CC	
		32			
1	1	33	B0002–883–00001	CONN RJ45 FEED THROUGH PNL MTG	WAN
1	1	34	B0000–079–00006	CBL ETHERNET 10B–T ST 00FT06I	
4	4	35	J4001–242–00000	SCREW–MACH 4–40 BH SS 0312	
2	2	36	B0000–861–00000	NUT HEX 4–40 FXLK	
		37			
1	1	38	C3463–000–00001	PCA ETHERNET HUB 10/100 5–PORT	ETHERNET
1	1	39	B0000–079–00100	CBL ETHERNET 10B–T ST 01FT00IN	
4	4	40	B0002–980–00000	STANDOFF AL 0.625 3/16H MF 4–40	
4	4	41	B0000–534–00000	WASHER LOCK INT NO 4 SS	
1	1	42	C3805–000–00001	PCA S3030 ETHERNET HUB TERMINATION BD	
		43			
1	1	44	C3414–000–00001	PCA CPU LX800 W/CF/IMG/LIC 1G	LX 800 CPU
1	1	45	C3800–CB4–50007	CBL ASSY FLAT FF 2M 50P 00F07I	
4	4	46	B0002–980–00000	STANDOFF AL 0.625 3/16H MF 4–40	
6	6	47	B0000–534–00000	WASHER LOCK INT NO 4 SS	
		48			
		49			
1	1	50	B0000–079–00006	CBL ETHERNET 10B–T ST 00FT06IN	
		51			
		52			
5	5	53	C3800–CB3–20100	CBL ASSY FLAT FM/BLK 20P 01F00I	J1,J2,J3,J4 & J6
1	1	54	C3800–CB3–20008	CBL ASSY FLAT FM/BLK 20P 00F08I	J5
		55			
		56			
2	2	57	C3800–CB3–26006	CBL ASSY FLAT FM/BLK 26P 00F06I	J7, J8
1	1	58	C3800–CB3–26010	CBL ASSY FLAT FM/BLK 26P 00F10I	J9
		59			
		60			
18	18	61	J0238–009–00000	WASHER FLAT SS NO4X.375X.040	
18	18	62	B0000–861–00000	NUT HEX 4–40 FXLK	
		63			
2	2	64	B1577–LD2–CB001	CBL ASSY F/LD2 REM/LOC SWITCH	
1	1	65	B1577–LD2–CB002	CBL ASSY F/LD2 PWR SPLY INPUT	
1	1	66	B1577–LD2–CB003	CBL ASSY F/LD2 PSOUT TO C3810	
1	1	67	B1577–LD2–CB004	CBL ASSY F/LD2 INTERNAL POWER	
		68			
		69			
		70			

–00002 125VDC/AC
–00001 20–60VDC

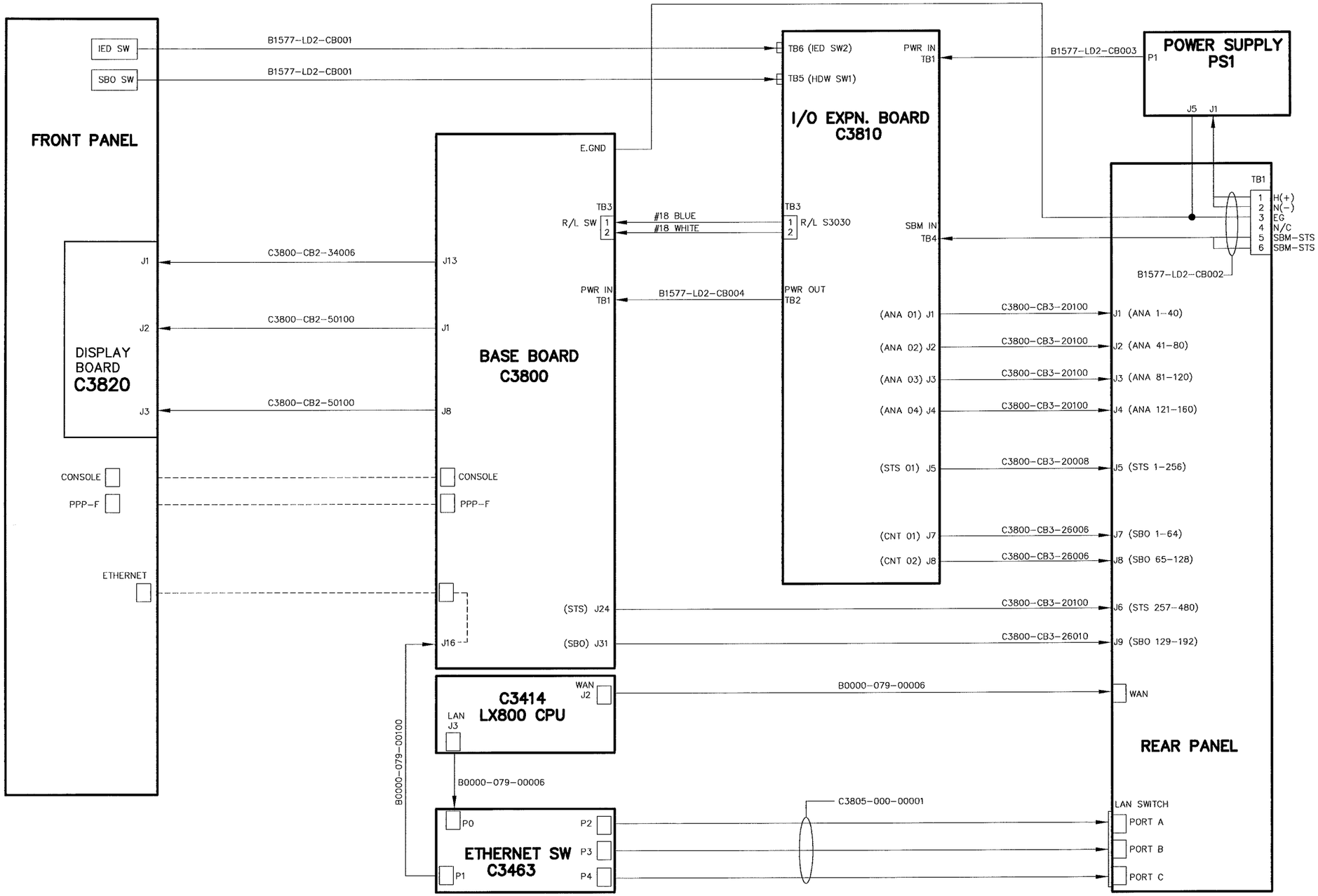
SYM.	ECO NO.	DATE	BY	CHK	DESCRIPTION
C	11889	10–12–10	P.P	U.P	SEE SHT. 1
B	11880	8–12–10	P.P	U.P	SEE SHT. 1
A	11860	5–13–10	P.P	U.P	SEE SHT. 1

REVISIONS

ACAD P/N	B1577–LD–0000X–3

APPROVALS	DATE
DWN PRAVIN	4–12–10
CHK U.PATEL	4–27–10
APP U.PATEL	4–27–10

SIZE		REV
B	B1577–LD2–0000X	C
SCALE NONE	SHEET 3 OF 5	



SYM.	ECO NO.	DATE	BY	CHK	DESCRIPTION
C	11889	10-12-10	P.P		SEE SHT. 1
B	11880	8-12-10	P.P	U.P	SEE SHT. 1
A	11860	5-13-10	P.P	U.P	SEE SHT. 1

REVISIONS

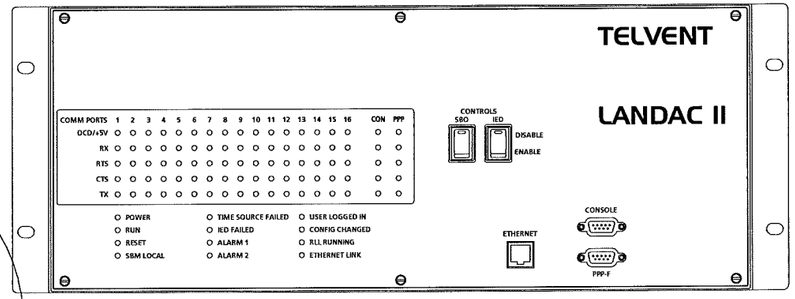
ACAD P/N	B1577-LD2-0000X-4

APPROVALS	DATE
DWN PRAVIN	4-12-10
CHK U.PATEL	4-27-10
APP U.PATEL	4-27-10

SIZE		REV
B	B1577-LD2-0000X	C
SCALE NONE		SHEET 4 OF 5

THESE FIVE WIRES MUST BE REMOVED FROM LANDAC POWER SUPPLY CONNECTOR & MUST BE CONNECTED TO NEW LANDAC II "POWER INPUT TB1."

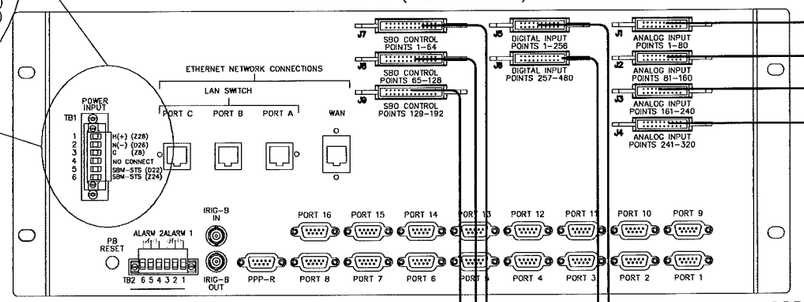
LANDAC II (FRONT VIEW)



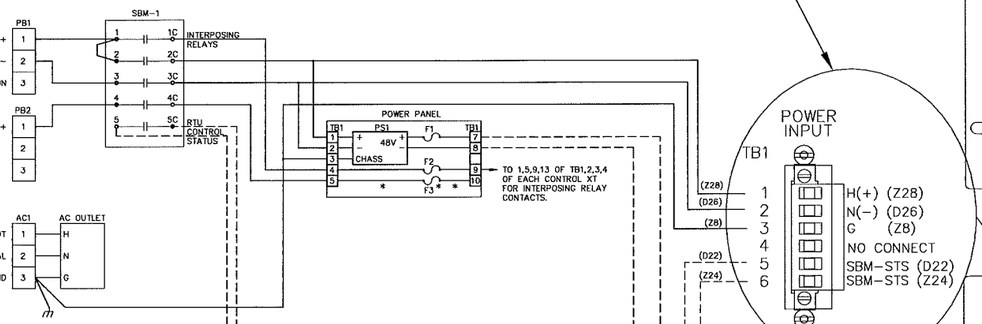
TYPICAL LANDAC II I/O POINT ASSIGNMENTS

	ANALOG	STATUS	CONTROL
J1	1–80		
J2	81–160		
J3	161–240		
J4	241–320		
J5		1–256	
J6		257–480	
J7			1–64
J8			65–128
J9			129–192

LANDAC II (REAR VIEW)



THESE ARE THE NEW CABLE CONNECTIONS REQUIRED FOR RETROFIT



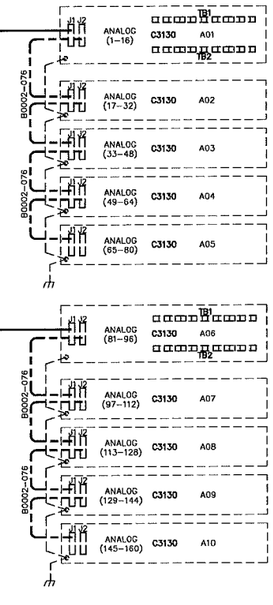
REMOTE STATION CONTROL

SBM–1 CONFIGURATION			
CONTACT NUMBER	SWITCH POSITION OFF	LOCAL	REMOTE
1 —⊣⊢— 1C			X
2 —⊣⊢— 2C		X	X
3 —⊣⊢— 3C		X	X
4 —⊣⊢— 4C			X
5 —⊣⊢— 5C			X

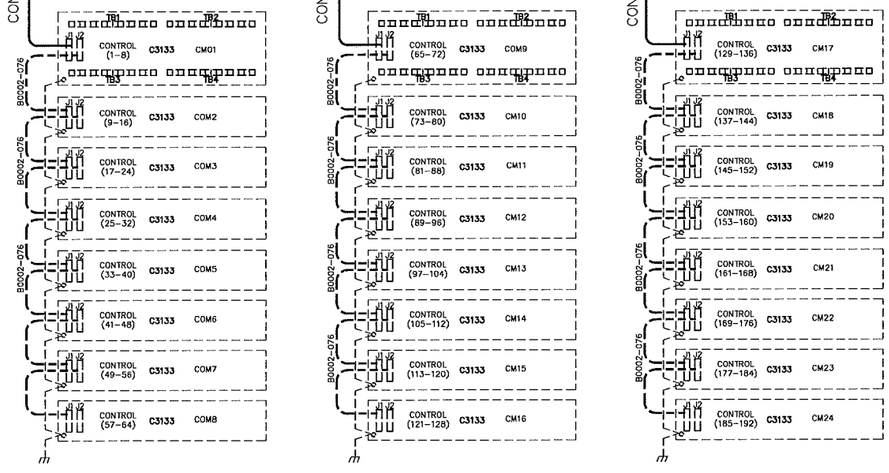
X = CONTACT CLOSED

LOCAL OFF REMOTE

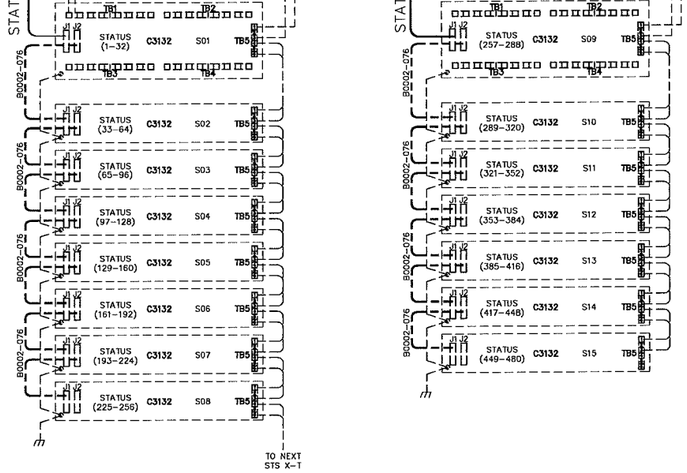
ANALOG



CONTROL



STATUS



NOTES:

1. * – F3 AND ASSOCIATED WIRING NOT NORMALLY SUPPLIED.

SYM.	ECO NO.	DATE	BY	CHK	DESCRIPTION
C	11889	10–12–10	P.P		SEE SHT. 1
B	11880	8–12–10	P.P	U.P	SEE SHT. 1
A	11860	5–13–10	P.P	U.P	SEE SHT. 1

REVISIONS

ACAD P/N	B1577–LD2–0000X–5

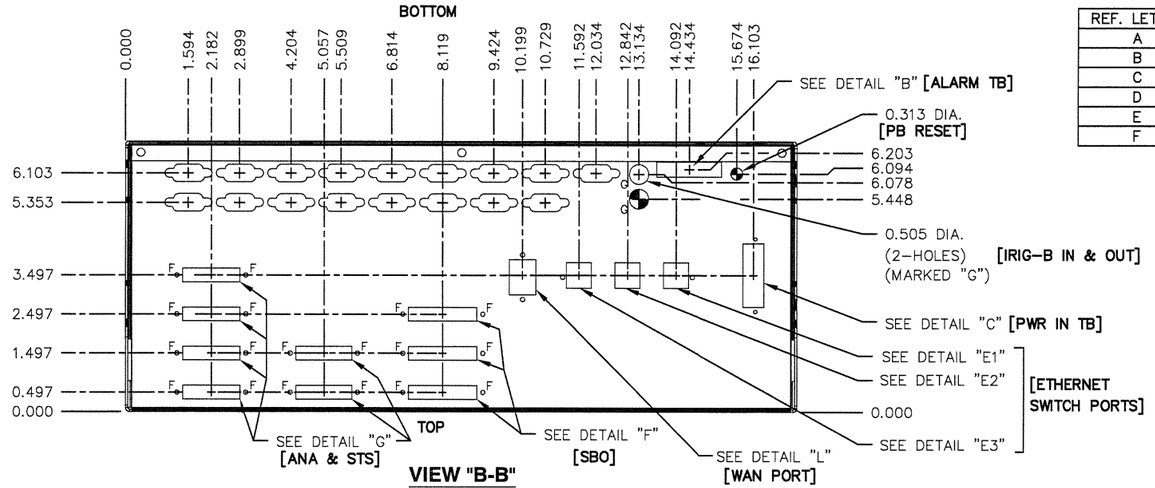
APPROVALS	DATE
DWN PRAVIN	4–12–10
CHK U.PATEL	4–27–10
APP U.PATEL	4–27–10

SIZE		REV
B	B1577–LD2–0000X	C
SCALE NONE	SHEET 5 OF 5	

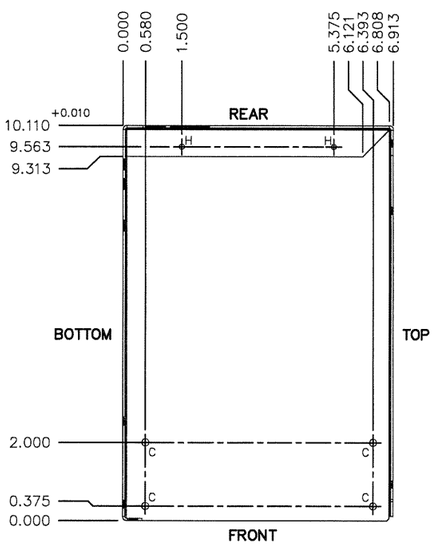
NOTES:

1. MATERIAL: 0.060" THK. ALUMINUM (5052-H32).
2. FINISH: LIGHT GRAIN CLEAR ANODIZE (ALL PIECES). SILKSCREEN BLACK PER ARTWORK SHT. 6 LOCATED BY ⌖ .
3. ALL BENDS ARE TO BE MINIMUM.
4. ALL STUDS, NUTS & STANDOFFS ARE TO PROTRUDE TOWARD THE INSIDE OF THE BOX.
5. TEXT IN [ ] IS FOR TELVENT ENG. USE & REF.

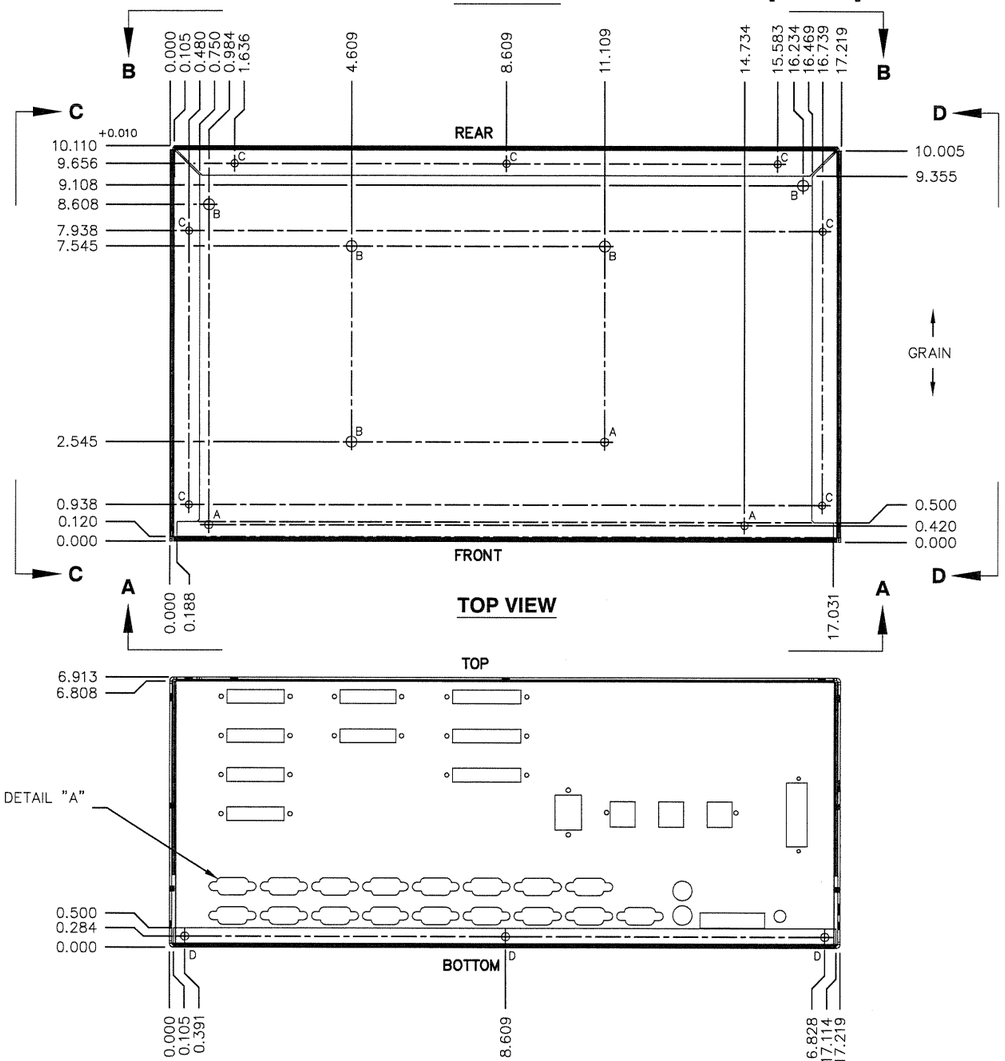
REF. LETTER	QTY	PEM TYPE	PEM PART NUMBER
A	5	SNAP TOP STANDOFF	SSC-156-16
B	7	SELF-CLINCHING STANDOFF	BSOS-8632-16
C	15	SELF-CLINCHING NUT	CLS-632-2
D	6	SELF-CLINCHING RECEPTACLE NUT	N10-632-1-ZI
E			
F	18	SELF-CLINCHING STUD	FHS-440-8



VIEW "B-B"

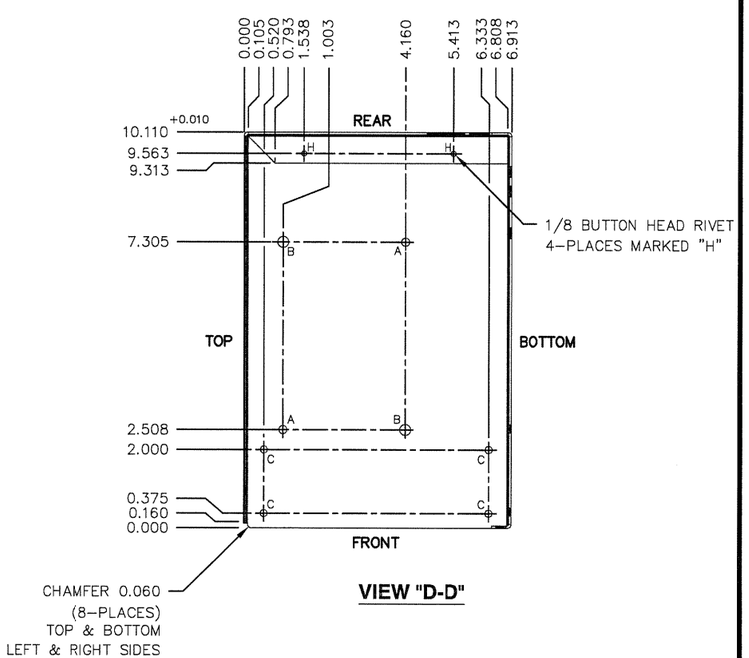


VIEW "C-C"



TOP VIEW

VIEW "A-A"



VIEW "D-D"

SYM.	ECO NO.	DATE	BY	CHK	DESCRIPTION

REVISIONS

MPL ENCL RACK MTG F/L ANDAC2 COM-ED

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES
DECIMALS
.XX = ±.02
.XXX= ±.010
ANGLES
±.5°
MATERIAL: SEE NOTE 1
FINISH: SEE NOTE 2

TELVENT

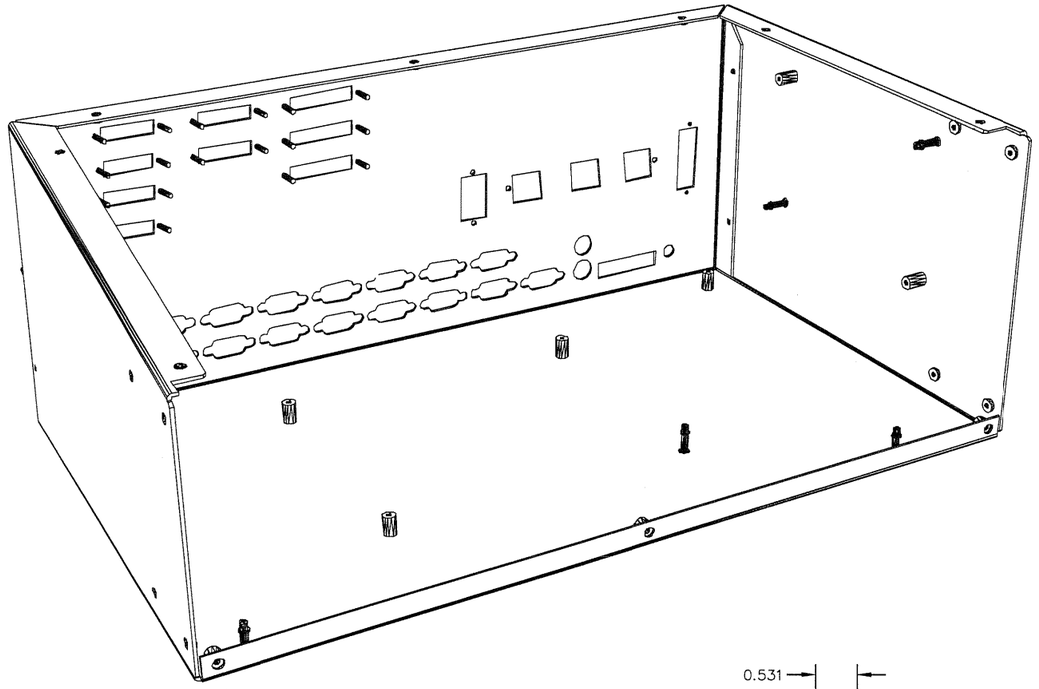
LANDAC II RACK MOUNTING ENCLOSURE 19"W X 7"H X 10"D FOR REPLACEMENT OF OLD LANDAC CHASSIS COMMONWEALTH EDISON

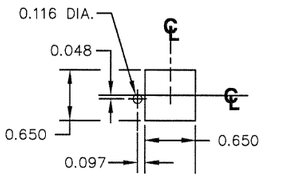
APPROVALS	DATE
DWN PRAVIN	4-5-10
CHK U.PATEL	4-19-10
APP	4-19-10

SIZE B | B1577-LD2-F0001 | REV 0

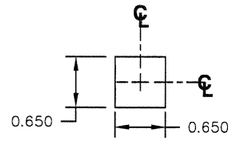
SCALE NONE | SHEET 1 OF 6

ACAD P/N B1577-LD2-F0001-1

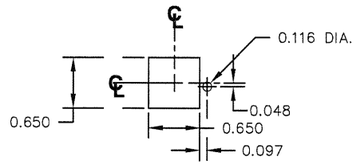




DETAIL "E3"

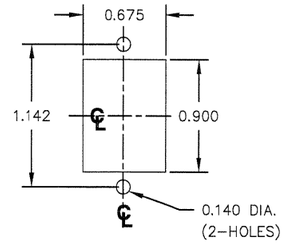


DETAIL "E2"

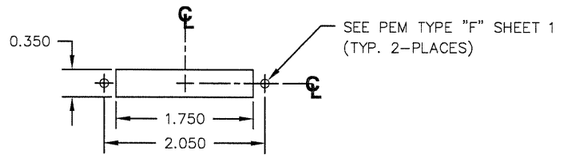


DETAIL "E1"

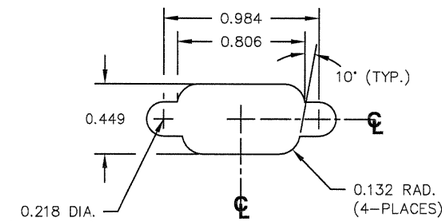
[ETHERNET SWITCH/PORTS]



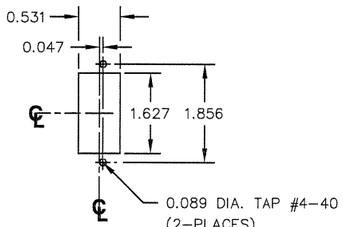
DETAIL "L"
[WAN RJ45]



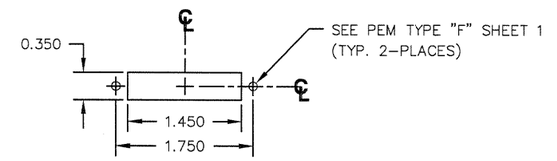
DETAIL "F"
(TYP. 3–PLACES)
[SBO]



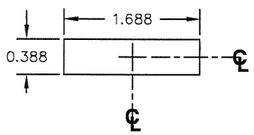
DETAIL "A"
(TYP. 17–PLACES)
[COMM PORTS]



DETAIL "C"
[PWR IN TB]



DETAIL "G"
(TYP. 6–PLACES)
[STS & ANA]



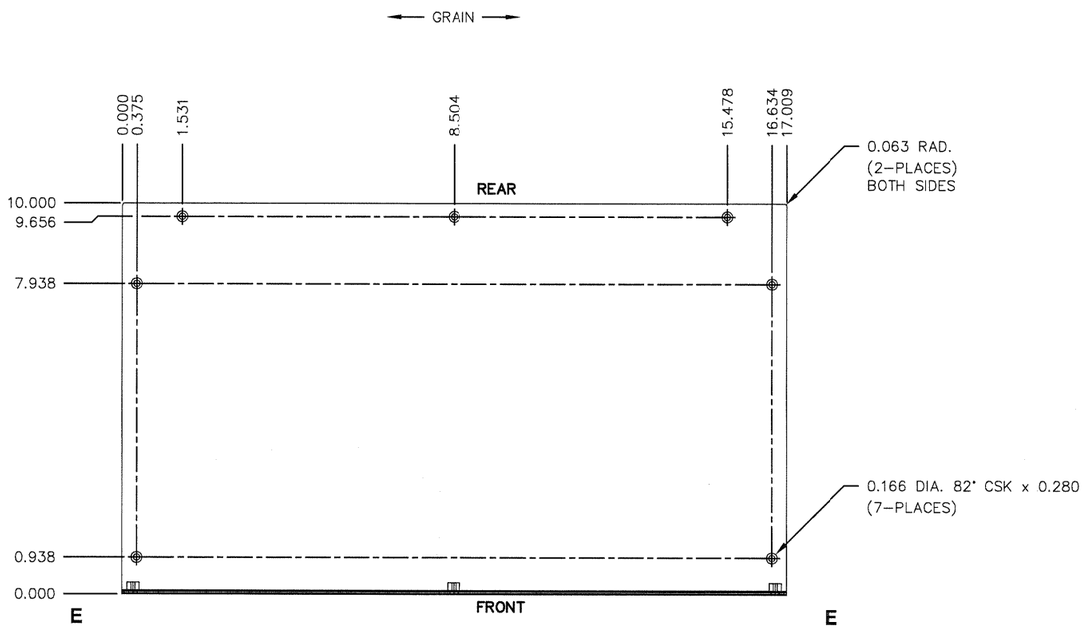
DETAIL "B"
[ALARM TB]

SYM.	ECO NO.	DATE	BY	CHK	DESCRIPTION

REVISIONS

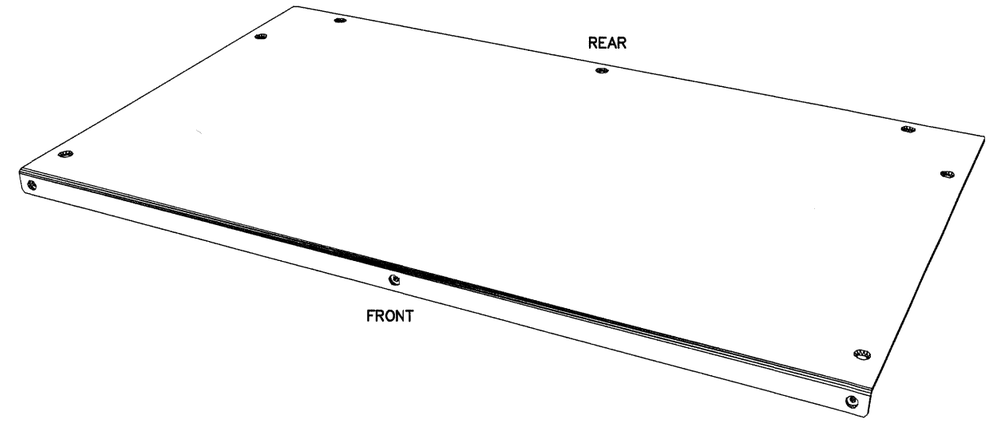
ACAD P/N	B1577–LD2–F0001–2

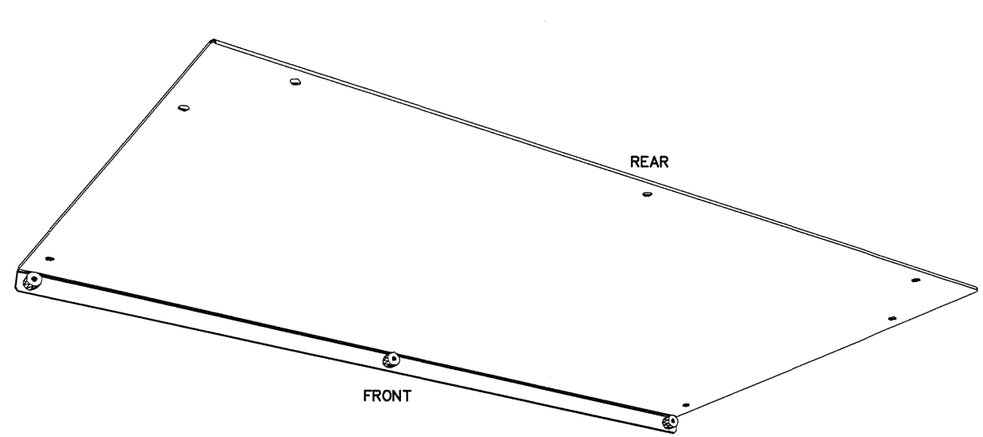
APPROVALS	DATE	SIZE		REV
DWN PRAWN	4–5–10	B	B1577–LD2–F0001	0
CHK U.PATEL	4–19–10			
APP	4–19–10	SCALE NONE	SHEET 2 OF 6	



TOP VIEW

VIEW "E-E"





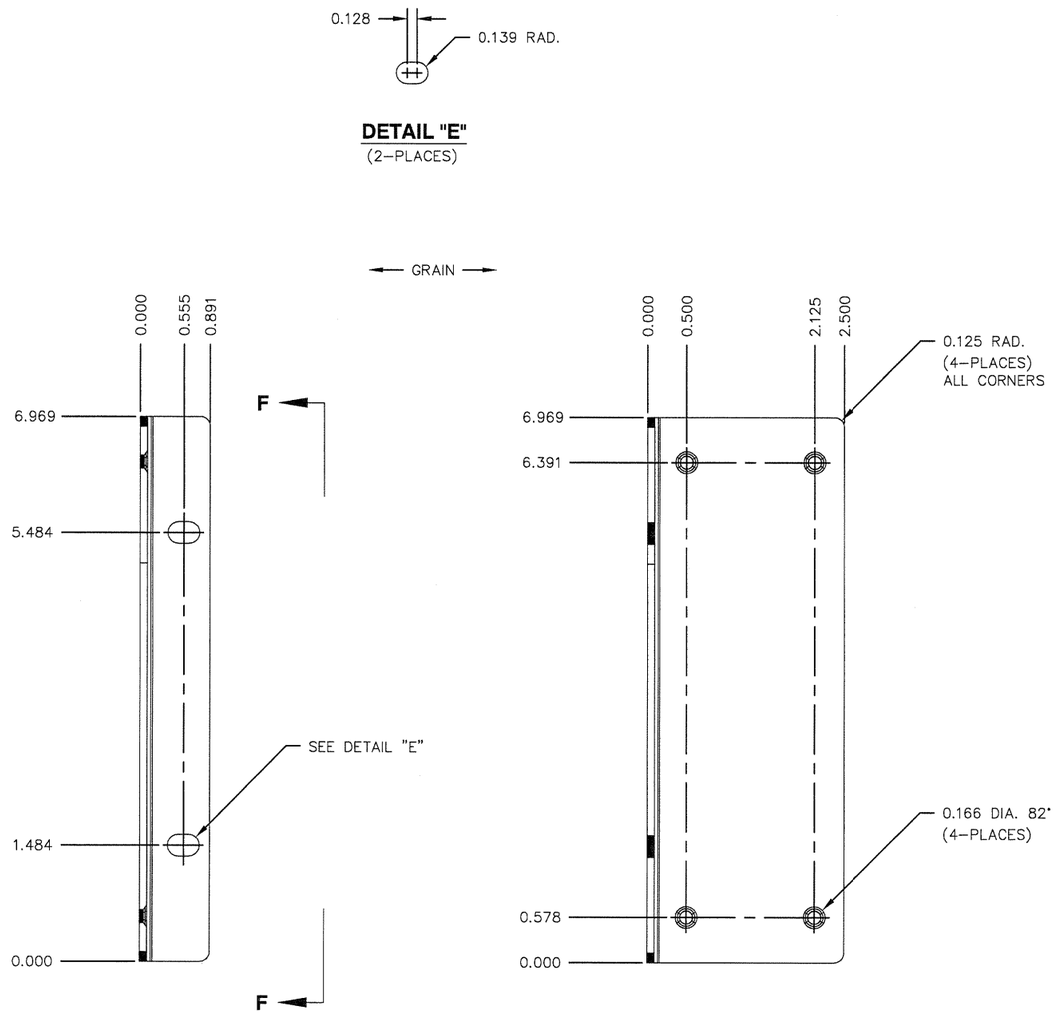
SYM.	ECO NO.	DATE	BY	CHK	DESCRIPTION

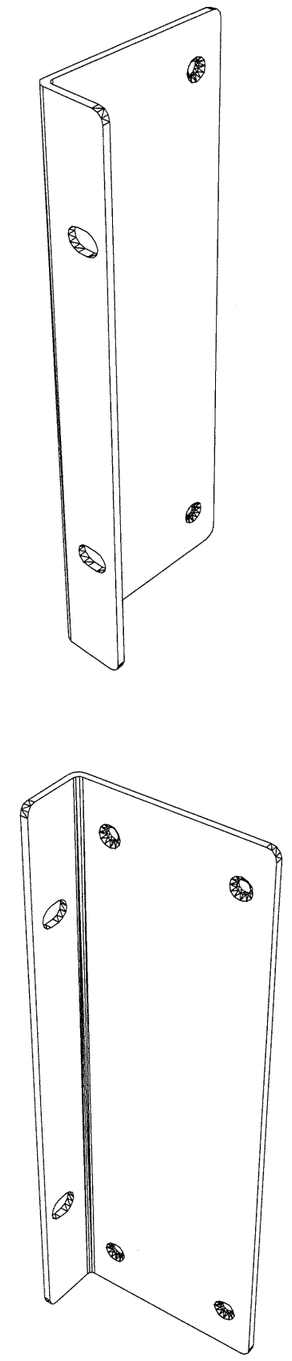
REVISIONS

ACAD P/N	B1577-LD2-F0001-3

APPROVALS	DATE
DWN PRAVIN	4-5-10
CHK U.PATEL	4-19-10
APP	4-19-10

SIZE		REV
B	B1577-LD2-F0001	0
SCALE NONE	SHEET 3 OF 6	





2-PIECES REQUIRED (LEFT & RIGHT)

NOTE: MATERIAL THICKNESS FOR THESE PARTS ONLY WILL BE 13 GAUGE (0.090 THK. ALUM).

SYM.	ECO NO.	DATE	BY	CHK	DESCRIPTION

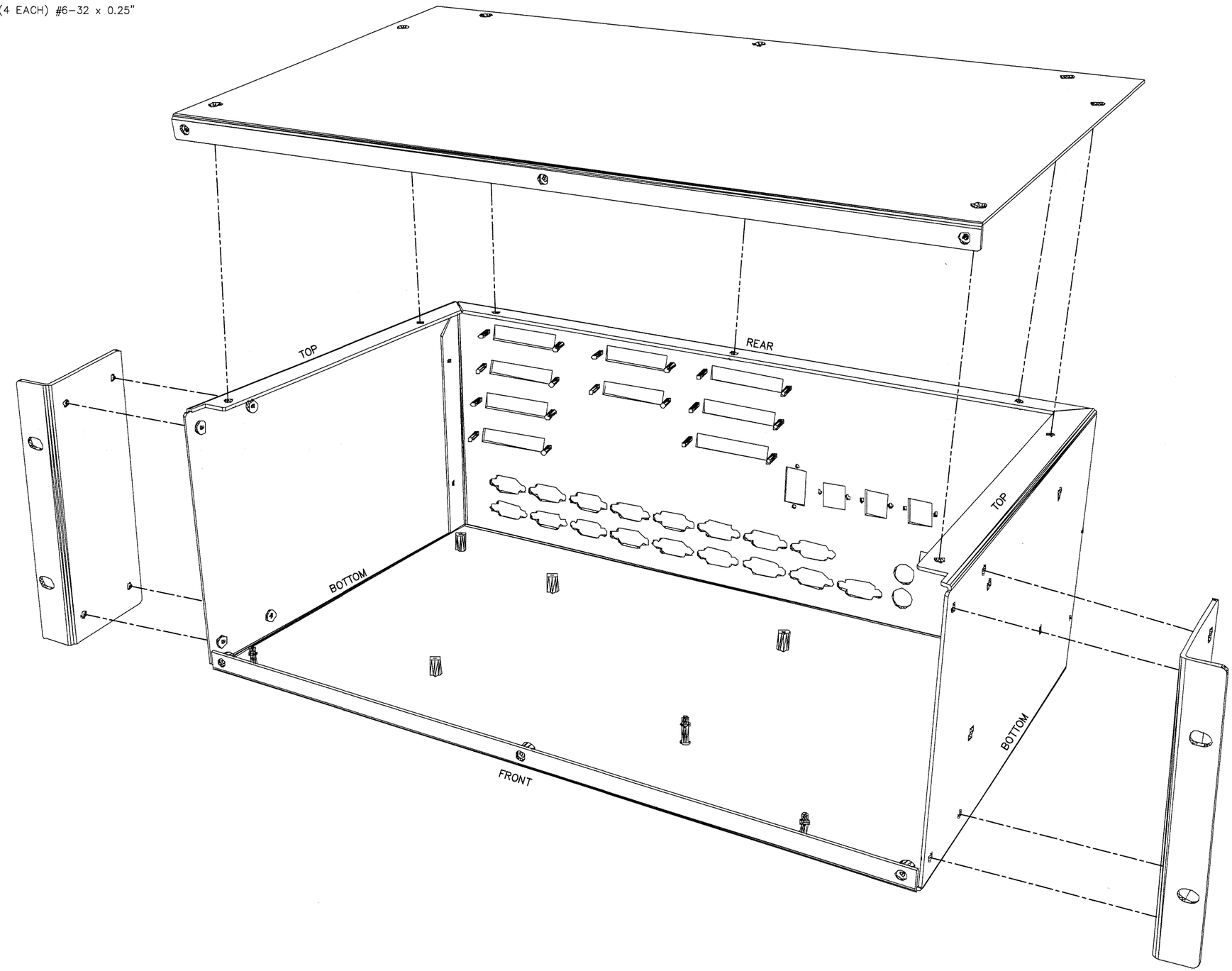
REVISIONS

ACAD P/N	B1577-LD2-F0001-4

APPROVALS	DATE	SIZE		REV
DWN PRAVIN	4-5-10	B	B1577-LD2-F0001	0
CHK U.PATEL	4-19-10			
APP	4-19-10	SCALE NONE	SHEET 4 OF 6	

ASSEMBLY NOTES:

1. INSTALL ENCLOSURE TOP USING (7) #6–32 x 0.25" UNDERCUT FLAT HEAD SCREWS.
2. INSTALL BOTH ENCLOSURE RACK MOUNTING BRACKETS USING (4 EACH) #6–32 x 0.25" UNDERCUT FLAT HEAD SCREWS.



SYM.	ECO NO.	DATE	BY	CHK	DESCRIPTION

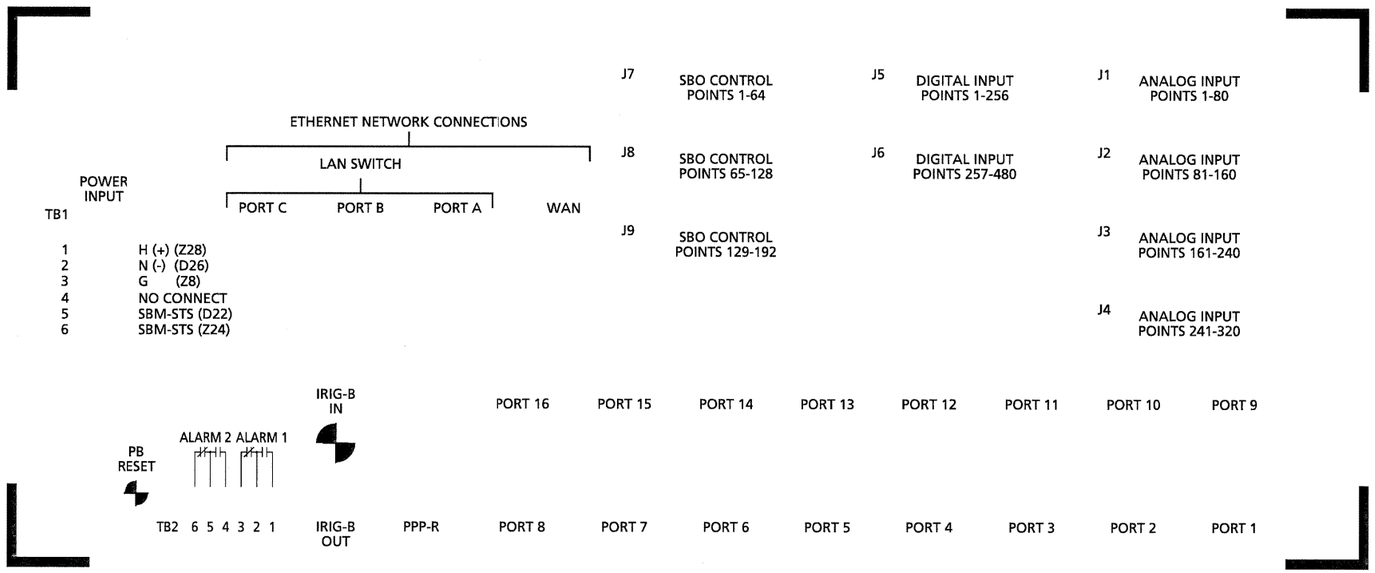
REVISIONS

ACAD P/N	B1577–LD2–F0001–5

APPROVALS	DATE	SIZE		REV
DWN PRAVIN	4–5–10	B	B1577–LD2–F0001	0
CHK U.PATEL	4-19-10			
APP	4-19-10	SCALE NONE	SHEET 5 OF 6	

NOTES:

1. SILKSCREEN BLACK PER THIS ARTWORK LOCATED BY ⌖.
2. FONT USED: FRUTIGER–ROMAN.
   TEXT HEIGHT: 0.125" (ALL TEXT EXCEPT ALARM 1 & ALARM 2: 0.100").



SILK SCREEN ON REAR SIDE OF THE BOX

SYM.	ECO NO.	DATE	BY	CHK	DESCRIPTION

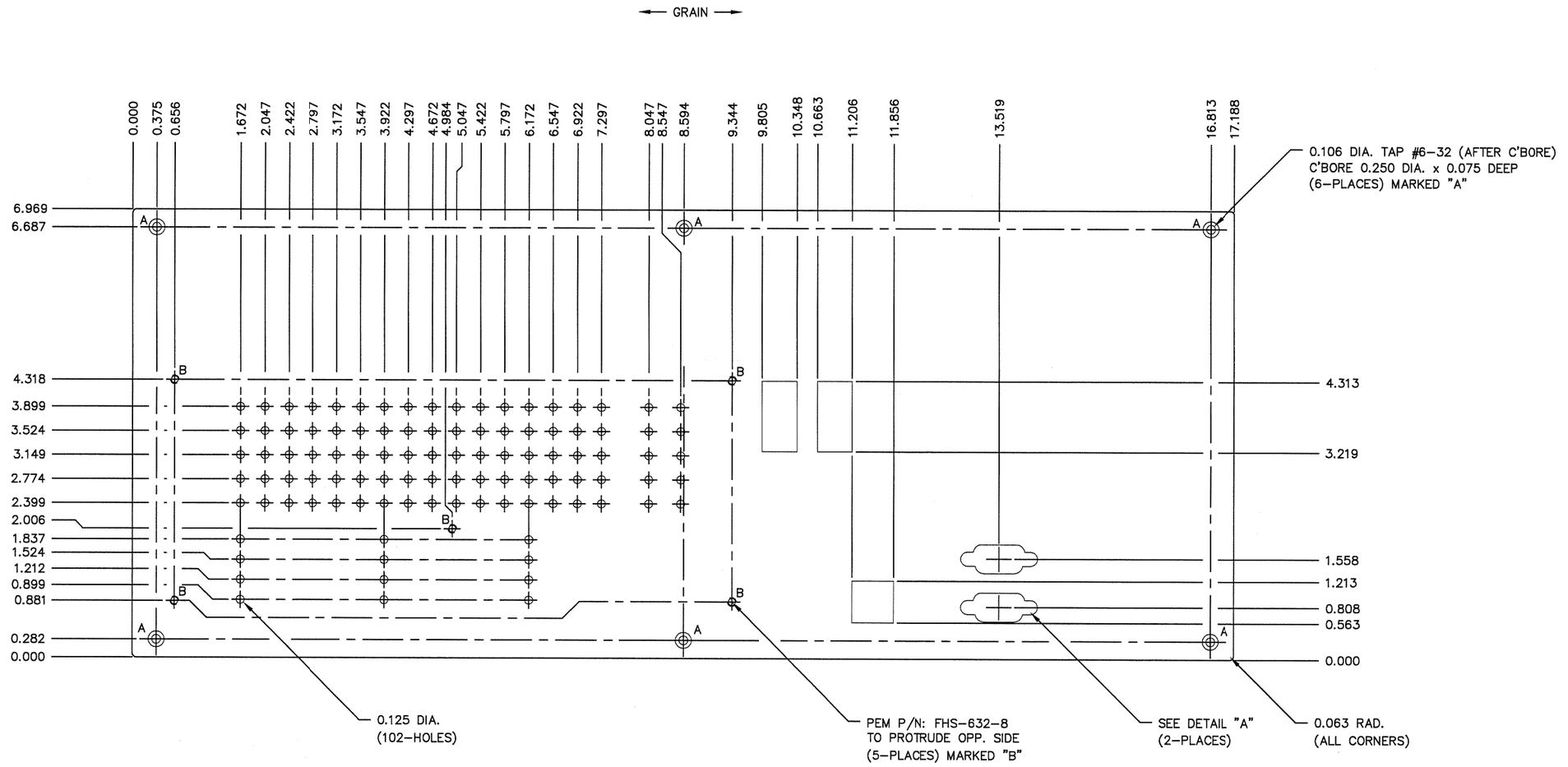
REVISIONS

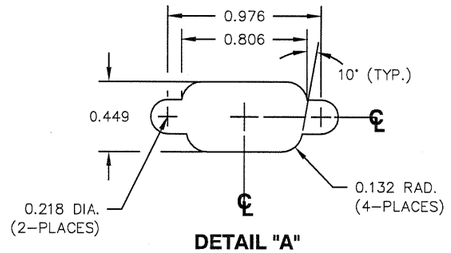
ACAD P/N	B1577–LD2–F0001–6

APPROVALS	DATE	SIZE		REV
DWN PRAVIN	4–5–10	B	B1577–LD2–F0001	0
CHK U.PATEL	4-19-10			
APP	4-19-10	SCALE NONE	SHEET 6 OF 6	

NOTES:

1. MATERIAL: 0.125" THK. ALUMINUM (5052-H32).
2. FINISH: LIGHT GRAIN CLEAR ANODIZE.





DETAIL "A"
(2-PLACES)

SYM.	ECO NO.	DATE	BY	CHK	DESCRIPTION

REVISIONS

MPL PNL FRONT F/LANDAC2 COM-ED

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES
DECIMALS
.XX = ±.02
.XXX= ±.010
ANGLES
±.5°
MATERIAL: SEE NOTE 1
FINISH: SEE NOTE 2

TELVENT

APPROVALS	DATE
DWN PRAVIN	4-5-10
CHK U.PATEL	4-21-10
APP	4-21-10

FRONT PANEL FAB. FOR LANDAC2 CHASSIS, 0.125" ALUMINUM PANEL WITH OVERLAY
COMMONWEALTH EDISON

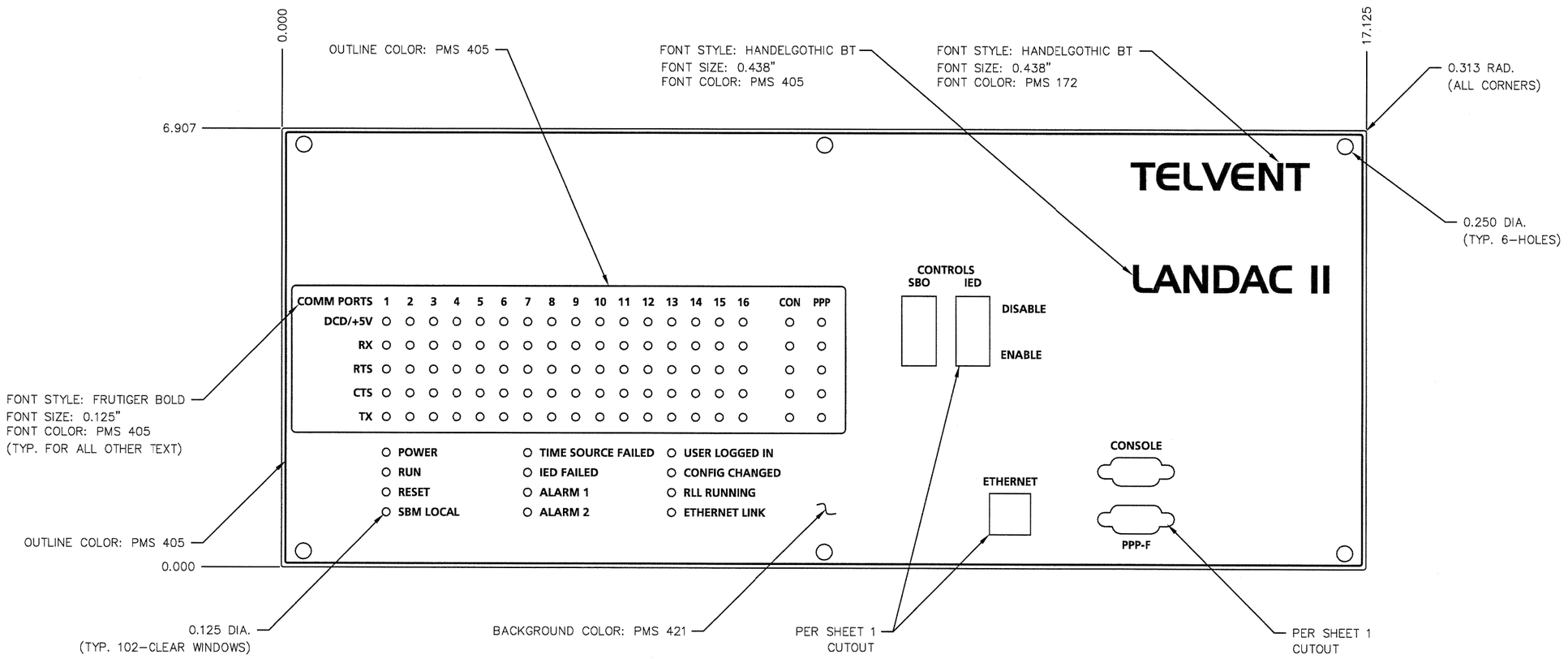
ACAD P/N	B1577-LD2-F0002-1

SIZE	B1577-LD2-F0002	REV
B		0
SCALE	NONE	SHEET 1 OF 2

NOTES:

1. MATERIAL: 10 MIL THK. VELVET GLOSS POLYCARBONATE MATERIAL BACKED WITH SCOTCH 3M 9505 ADHESIVE.

2. FINISH: AS PER COLORS AND TEXT SIZE SPECIFIED.
   COLORS USED: PMS 172 (ORANGE)
   PMS 405 (DARK GREY)
   PMS 421 (LIGHT GREY)



SYM.	ECO NO.	DATE	BY	CHK	DESCRIPTION

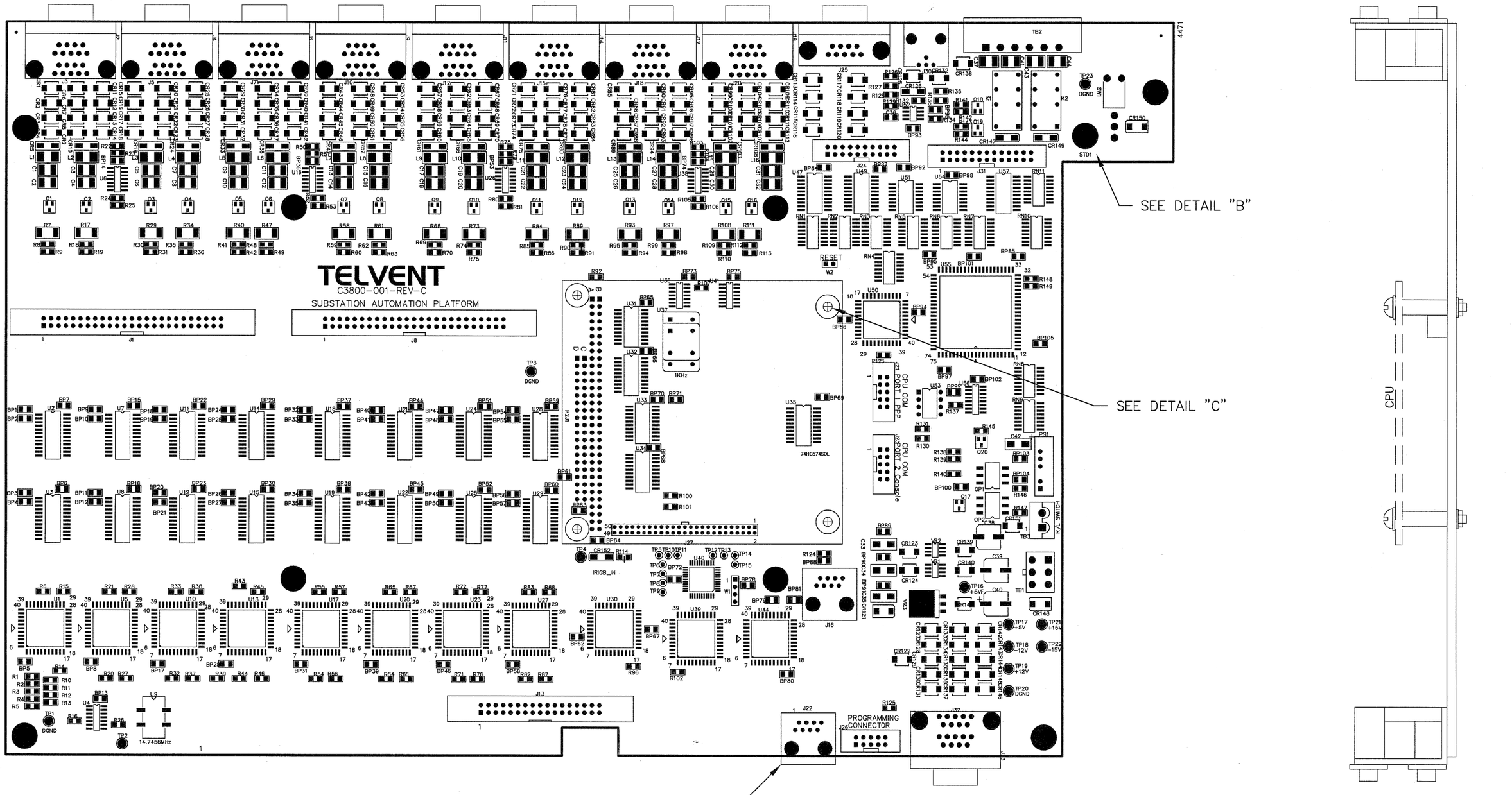
REVISIONS

ACAD P/N	B1577–LD2–F0002–2

APPROVALS	DATE	SIZE		REV
DWN PRAVIN	4–5–10	B	B1577–LD2–F0002	0
CHK U.PATEL	4-21-10			
APP	4-21-10	SCALE NONE	SHEET 2 OF 2	

NOTES:

1. CAUTION CMOS DEVICES INSTALLED – HANDLE AT GROUNDED WORK STATION.
2. MARK BOARD WITH ASSEMBLY PART NUMBER, REVISION LETTER AND SERIAL NUMBER AFTER FINAL ASSEMBLY. PLACE LABEL NEAR "U9" (IN OPEN AREA).
3. PRESS IN ITEM #91 BEFORE FLOWSOLDER. ADD HARDWARE #92–#94 AT FINAL ASSEMBLY.



SYM.	ECO NO.	DATE	BY	CHK	DESCRIPTION
G	11841	1-7-10	P.P		ADDED ITEM #3 TEST PROCEDURE C3800
F	11808	7-24-09	P.P	CJ	CHANGE DRAWING TO REV.-C SILKSCREEN
E	11805	7-20-09	P.P	CJ	ITEM #77 P/N CHG'D, REF. DESIG. CHG'D ON ITEM 43
D	11773	2-11-09	P.P	CJ	ITEM #1 WAS -001-REV-B
C	11731	6-12-08	P.P	CJ	ADDED NEW PART ITEM #10, & ITEM #2 WAS -REV-B
B	11561	08-22-05	DW	CJ	ADDED DETAIL "A"; ITEM 104 WAS C3800-525-PLDA6

REVISIONS

ACAD P/N: C3800-000-00001-1

MPL PCA SAGE 3030 SAP MAIN BOARD

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES
DECIMALS .XX = ±.02 .XXX= ±.010
ANGLES ±.5°
MATERIAL: NONE
FINISH: NONE

TELVENT

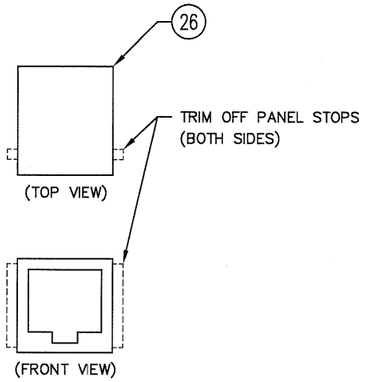
PCA SAGE 3800 (S3030), SUBSTATION AUTOMATION PLATFORM

ASSEMBLY DRAWING

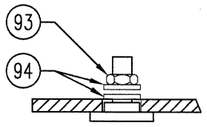
APPROVALS	DATE
DWN P.RAVIN	2-4-05
CHK C.JANIK	3-21-05
APP C.JANIK	3-21-05

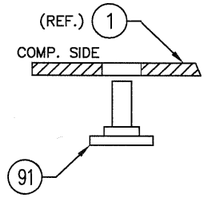
SIZE B | C3800-000-00001 | REV G

SCALE NONE | SHEET 1 OF 2

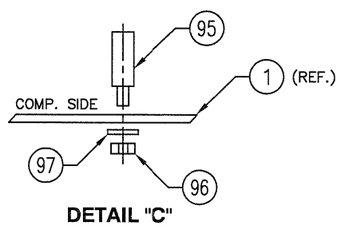


DETAIL "A"





DETAIL "B"
(SEE NOTE 3)



DETAIL "C"
(TYPICAL 4–PLACES)

QTY	ITEM	PART NUMBER	DESCRIPTION	NOTES
	56			
	57			
	58			
	59			
1	60	B0002-077-00002	SWITCH P/BT 1P 2POS RT ANGLE	SW1
1	61	B0002-116-10001	BUTTON F/MINI SWITCH .374 BLK	(USED ON SW1)
1	62	B0002-298-30006	CONN HSG RECP 06PIN M GOLD POL	TB1
1	63	B0002-882-00006	CONN HDR PCB 06P .197 HRZ	TB2
1	64	B0002-882-10006	CONN PLG FEM 06P .197 HRZ	(USED ON TB2)
1	65	B0001-882-C0002	CONN PLG PCB 02P .197	TB3
1	66	B0001-882-VHC02	CONN HDR PCB 02P .197 VSH	(USED ON TB3)
5	67	B0000-740-00000	TERM PIN TURRET H .062D/.094T	TP1,TP3,TP17,TP20,TP23
	68			
8	69	B0002-471-S2301	ICD Z85230 COMM CONTROLLER SMT	U1,U5,U10,U13,U17,U20,U23,U27
16	70	B0002-547-S0004	ICL LT1141 RS-232 DRVR/RCVR SMT	U2,U3,U7,U8,U11,U12,U14,U15,U18, U19,U21,U22,U24,U25,U28,U29
2	71	B0001-849-S0014	ICD 74AHC14 INVTR SCHMIT SMT	U4,U36
5	72	B0001-849-S0032	ICD 74AHC32 OR GATE SMT	U6,U16,U26,U38,U41
1	73	B0002-851-S0001	OSC XTAL 14.7456MHZ 100PPM SMT	U9
4	74	B0002-445-7032S	ICD EP7032S PROGRAM LOG/DEV	U30,U39,U44,U50
	75			
6	76	B0001-849-S0245	ICD 74AHCT245 XCVR SMT	U31-U34,U47,U49
1	77	B0002-460-00002	OSC XTAL 1.00KHZ 50PPM 3050	U37
1	78	B0002-880-S0001	ICD PIC 16F877A MICROCHIP PROCESSOR	U40
2	79	B0001-460-S5821	ICD UNC5821LW 8BIT SRL DVR SMT	U51,U54
1	80	B0001-363-S0004	ICL OP282GS OPAMP DUAL SMT	U52
1	81	C3800-525-PLDA5	ICD PLD PGRM EPC1064 C3800-5	U53
1	82	B0002-445-08452	ICD EP8452 PROGRAM LOG/DEV	U55
1	83	B0001-848-S0238	ICD 74HCT238 3-8 DECODER SMT	U56
1	84	B0001-460-S2982	ICD A2982SLW 8CH SOURCE DVR SMT	U57
1	85	B0001-886-S0012	ICL 78L12ACM POS V-REG SMT	VR1
1	86	B0001-885-S0012	ICL 79L12ACM NEG V-REG SMT	VR2
1	87	B0001-886-S7808	ICL UA7808CKTER 8V POS REG	VR3
1	88	B0001-848-S0574	ICD 74HCT574 D-LATCH	U35
1	89	B0001-591-00008	SOCKET DIP 08P BOT SEAL	USED ON U53
	90			
1	91	B0001-955-00832	FASTENER PCB EXT 8-32 TD	STD1 (SEE DETAIL "B")
	92			
1	93	B0002-331-00000	NUT HEX SM PAT 8-32 SS	USED ON STD1 (SEE DETAIL "B")
2	94	J4001-240-00000	WASHER LOCK INT NO 8 SS	USED ON STD1 (SEE DETAIL "B")
4	95	B0002-980-00000	STANDOFF AL 0.625 3/16J MF #4-40	SEE DETAIL "C"
4	96	J0294-022-00000	NUT HEX SM PAT 4-40 SS	SEE DETAIL "C"
4	97	B0000-534-00000	WASHER LOCK INT NO 4 SS	SEE DETAIL "C"
	98			
	99			
0	100	C3800-525-PLDA1	ICD PLD PRGRM EP7032S C3800-1	USED ON U44, SEE NOTE 1.
0	101	C3800-525-PLDA2	ICD PLD PRGRM EP7032S C3800-2	USED ON U30, SEE NOTE 1.
0	102	C3800-525-PLDA3	ICD PLD PRGRM EP7032S C3800-3	USED ON U39, SEE NOTE 1.
0	103	C3800-525-PLDA4	ICD PLD PRGRM EP7032S C3800-4	USED ON U50, SEE NOTE 1.
0	104	C3800-527-PLDA6	ICD PLD PRGRM EP7032S C3800-6	USED ON U40, SEE NOTE 1.
	105			
	106			
	107			
	108			
	109			
	110			

NOTE 1. ITEM #100 to #104 PARTS ARE PROGRAMMED AFTER MANUFACTURING.

QTY	ITEM	PART NUMBER	DESCRIPTION	NOTES
1	1	C3800-001-REV-C	PCB SAGE 3030 SAP	PCB
0	2	C3800-002-REV-C	SCH SAGE 3030 SAP	
0	3	C3800-003-REV-A	TEST PROCEDURE C3800 BASEBOARD	
105	4	B0000-678-5104M	CAP-N CE 050V M0.100 20P SMT	BP1-BP105,
36	5	B0000-679-S0105	CAP-N CE 050V M001.00 20P SMT	C1-C32,C37,C41,C43,C44
3	6	B0000-680-K4752	CAP-P TA 035V M004.700 10P SMT	C33-C35 (C42 NOT POPULATED)
	7			
3	8	J0000-066-M0100	CAP-P EL 050V M0100.0 20P SMT	C38-C40
	9			
1	10	B0000-699-5123J	CAP-N PPS 050V P12000.0 05P SMT	C36
	11			
	12			
	13			
125	14	B0001-247-S0015	DIODE SMB15C 15V Z 0600W	CR1-CR4,CR6-CR9,CR11-CR18, CR20-CR23,CR25-CR32,CR34-CR37 CR39-CR46,CR48-CR51,CR53-CR60, CR62-CR65,CR67-CR74,CR76-CR79, CR81-CR88,CR90-CR93,CR95-CR102 CR104-CR107,CR109-CR120, CR122-CR125,CR127-CR138, CR142-CR146
20	15	J1160-016-S0000	DIODE 1N4004 RS 400V 01.00A SMT	CR5,CR10,CR19,CR24,CR33,CR38, CR47,CR52,CR61,CR66,CR75,CR80, CR89,CR94,CR103,CR108,CR126, CR147,CR149,CR152
3	16	B0001-247-S0008	DIODE SMB8.0 8.0V Z 0600W	CR121,CR148,CR150
4	17	B0001-247-S0018	DIODE SMBJ18C 18V Z 0600W	CR139,CR140,CR141,CR151
	18			
	19			
	20			
2	21	B0002-521-40050	CONN HDR PCB SH4 50P .125 LTCH	J1,J8
9	22	B0002-453-02009	CONN DSUB PC DL RA 09P SF	J2J3,J4J5,J6J7,J9J10,J11J12, J14J15,J17J18,J19J20,J32J33
1	23	B0002-521-40034	CONN HDR PCB SH4 34P .125 LTCH	J13
3	24	B0002-521-10110	CONN HDR PCB SH4 KEY 2X05 .125	J21,J23,J26
	25			
1	26	B0002-281-108K8	TELE-JACK PCB MOD 8KP/8C PLMS	J22 (SEE DETAIL "A")
1	27	B0002-281-00001	TELCO JACK PCB MOD 8KP/8C PRM T	J16
1	28	B0002-521-40020	CONN HDR PCB SH4 20P .125 LTCH	J24
1	29	B0002-521-40026	CONN HDR PCB SH4 26P .125 LTCH	J31
1	30	B0002-892-00050	CONN HDR PCB 2MM M 5P CTR POL	J27
1	31	B0001-806-10001	CONN BNC DUAL PC 364 SERIES	J30
1	32	B0002-453-01009	CONN DSUB PC DL RA 09P SF	J25
1	33	J0000-551-00020	CONN PCB SQ 20POS D/ROW F PC104	P2J1
1	34	J0000-551-00032	CONN PCB SQ 32POS D/ROW F PC104	P2J1
2	35	B0000-843-00002	RLY DIP 012VDC 2FC 60VA SSS PL	K1,K2
16	36	J0000-635-S0100	INDUCTOR 100.0VH 160MA SMT	L1-L16
2	37	B0002-419-S0000	ICD H11L3/H11L1 OPTO ISO SMT	OP1,OP2
	38			
1	39	B0002-699-0515S	P/S DC-DC 05V/+-15V@.30MA SIP	PS1
20	40	B0002-624-S0005	TSTR IRLML2402 MFET SMT	Q1-Q20
57	41	B0000-821-C6811	RES SMT MF 01.00P .12W K06.81	R1,R6,R14,R15,R20,R21,R27,R28, R32,R33,R37-R39,R43-R46, R54-R57,R64-R67,R71,R72,R76, R77,R82,R83,R87,R88,R96,R92,R100 R107,R114,R123,R125,R124, R137-R145,R147-R149 R102,R126,R129,R135,R136
16	42	B0000-821-B6R20	RES SMT MF 5.00P 1W H06.20	R7,R17,R29,R34,R40,R47,R58,R61, R68,R73,R84,R89,R93,R97,R108,R111
16	43	B0000-821-C1002	RES SMT MF 01.00P .12W K010.0	R8,R18,,R30,,R35, R41,R48,R59,R62, R69,R74,R85, R90,R95,R99, R109,R112
8	44	B0000-821-C1003	RES SMT MF 01.00P .12W K100.0	R2-R5,R10-R13,
4	45	B0000-821-C0000	RES SMT MF .12W H0.00 JMPR	R16,R26,R101,R132
4	46	B0000-821-C1001	RES SMT MF 01.00P .12W K01.00	R127,R130,R131,R146
17	47	B0000-821-C56R2	RES SMT MF 01.00P .12W 56.20 OHM	R22-R25,R50-R53,R78-R81, R103-R106,R134
1	48	B0000-821-A1004	RES SMT MF 05.00P .12W M001.00	R128
	49			
	50			
5	51	J0000-585-S0103	RES NW 08 K010.00 SMT 16PIN	RN1,RN4,RN5,RN10,RN11
3	52	J0000-585-S0224	RES NW 08 K220.00 SMT 16PIN	RN2,RN6,RN8
3	53	J0000-585-S0105	RES NW 08 M01.00 SMT 16PIN	RN3,RN7,RN9
	54			
	55			

SYM.	ECO NO.	DATE	BY	CHK	DESCRIPTION
G	11841	1-7-10	P.P		SEE SHT. 1
F	11808	7-24-09	P.P	CJ	SEE SHT. 1
E	11805	7-20-09	P.P	CJ	SEE SHT. 1
D	11773	2-11-09	P.P	CJ	SEE SHT. 1
C	11731	6-12-08	P.P	CJ	SEE SHT. 1
B	11561	08-22-05	DW	CJ	SEE SHT. 1

REVISIONS

ACAD P/N	C3800-000-00001-2

APPROVALS	DATE
DWN PRAVIN	2-4-05
CHK C.JANIK	3-21-05
APP C.JANIK	3-21-05

SIZE		REV
B	C3800-000-00001	G
SCALE NONE	SHEET 2 OF 2	

RESISTOR WILL HOLD BOARD IN RESET IN THE ABSENSE OF A CPU BOARD

+5V
R92 6.81K
R107 6.81K
U36:F HCT14
RESET Sheet 2 0f 8
RTU-RESET#

J4 ROW-A / ROW-B

IOCHCK, SD7, SD6, SD5, SD4, SD3, SD2, SD1, SD0, IOCHRDY, AEN, SA19, SA18, SA17, SA16, SA15, SA14, SA13, SA12, SA11, SA10, SA9, SA8, SA7, SA6, SA5, SA4, SA3, SA2, SA1, SA0, GND

DGND, RESETDRV, +5V, IRQ9, -5V, DRQ2, -12V, ENDXFR, +12V, KEYB, SMEMW, SMEMR, IOW, IOR, DACK3, DRQ3, DACK1, DRQ1, REFRESH, SYSCLK, IRQ7, IRQ6, IRQ5, IRQ4, IRQ3, DACK2, TC, BALE, +5V, OSC, GND, GND

IOW# IOR#

TO PLDA1 THIS PAGE

IRQ7 GPS
IRQ6
IRQ5 1MSEC Clock
CPU Comm

BP61 .1uF, BP64 .1uF, BP79 .1uF, BP63 .1uF

J5

GND, SBHE, LA23, LA22, LA21, LA20, LA19, LA18, LA17, MEMR, MEMW, SD8, SD9, SD10, SD11, SD12, SD13, SD14, SD15, KEYC

MEMCS16, IOCS16, IRQ10, IRQ11, IRQ12, IRQ13, IRQ14, DACK0, DRQ0, DACK5, DRQ5, DACK6, DRQ6, DACK7, DRQ7, +5V, MASTER, GND, GND

IRQ10
GPS
IRQ12
IRQ14
+5V
DGND

1KHZ

U37 VCC 1KHz, VCC 1KHz, NC GND, NC GND

INT-1MSEC

U36:A HCT14

1MSEC
IRQ5

PC/104 BUS CONNECTORS

BP81 .1uF, BP66 .1uF, BP70 .1uF, BP68 .1uF, BP69 .1uF, BP62 .1uF, BP67 .1uF

TP4
0.0 R101
6.81K R100
RTU-ADD#

U31 74AHCT245SOL

RTU-IOR#
SD7, SD6, SD5, SD4, SD3, SD2, SD1, SD0
TO ALL SHEETS
BDATA

D7, D6, D5, D4, D3, D2, D1, D0
100K
R5, R10, R13, R2, R4, R11, R12, R3

U34 74AHCT245SOL

SA7, SA6, SA5, SA4, SA3, SA2, SA1, SA0
BSA7, BSA6, BSA5, BSA4, BSA3, BSA2, BSA1, BSA0

U33 74AHCT245SOL

SA15, SA14, SA13, SA12, SA11, SA10, SA9, SA8
BSA15, BSA14, BSA13, BSA12, BSA11, BSA10, BSA9, BSA8

U32 74AHCT245SOL

SA19, SA18, SA17, SA16
SBSEL7
B-SBSEL7
U38 pin 27
J21 Pin17

U36:B, U36:C, U36:D, U36:E HCT14

U30 EPM7032SPLCC44 PLDx2

PLDX2, BSA7, BSA6, BSA5, BSA4, TMS, BSA2, BSA3
COM_PLD#, DGND
SYNCOUT From Sheet 2
PLDX2, CS-COM1&2#, CS-COM3&4#, +5V, CS-COM5&6#, CS-COM7&8#, TCK, CS-COM9&10#, DGND, CS-COM11&12#
CS-COM13&14#, CS-COM15&16#, COM-INT1#, COM-INT2#
To Sheets 3,4,5,& 6
IRQ6, IRQ9
To J4 This Page

U44 EPM7032SPLCC44 PLDx1

RTU-RESET#, IOW#, IOR#, AEN, DGND
RTU-IOW#
RTU-IOR#
BSA15, BSA14, BSA13, BSA12, BSA11, BSA10, BSA9, BSA8, BSA7, BSA6
PLDX1, TMS
STATUS#, PLDX2, RTU-ADD#, PIC#, +5V, IOPLD#, COM_PLD#, TCK, SBO#, DGND, ALARM#
LED#
BSA5, BSA4, BSA3, BSA2, BSA1, BSA0
BADDR
BADDR
To All Sheets

REV	ECO#	DATE	BY	CHK	DESCRIPTION
C	11731	06/12/08	CGJ	CGJ	Change Value of C36 to .01uF, R95,R99,R109, R112
B	NA	05/06/05	CGJ	CGJ	First Production Release

APPROVALS		DATE
DWN	Chris Janik	14Jan05
CHK	CGJ	06May05
APP	CGJ	06May05

TELVENT

MPL | SCH SUBSTATION AUTOMATION PLTFM

SUBSTATION AUTOMATION PLATFORM

PART # C3800-002-REV-C

SIZE B | PC/104 | SHEET 1 OF 8

IRIGB_IN
D2 D1 D0 +5V RTU-RESET# BSA1 BSA0 DGND D4 D5
PLDX3 D3 IRIG_RESET# DGND SYNCOUT WRBUSY TMS DATARDY +5V IRIGB_OUT
U39
EPM7032SPLCC44
PLDx3
D6 PLDX4 D7 +5V IRQ7 TCK DGND
RTU-IOR# RTU-IOW# IRIGCS# IRIG-A0 PIC# PIC_ACK TSYNC_IN

U35
RESET LED# D0 D1 D2 D3 D4 D5 D6 D7
74HC574
GP1 GP2 GP3 GP4 GP5 GP6 GP7 GP8
Run
Local
Time Source Fail
IED Failed
User Logged In
Config. Changed
RLL Running
Ethernet Link
To Sheet 3 , J13
General Purpose LED's

D0 D1 D2 D3
SYNCOUT IRIG-A0 DATARDY
W1
DEVELOPMENT PORT
+5V DGND
U40
{Value}
RC7/RX/DT RD4/PSP4 RD5/PSP5 RD6/PSP6 RD7/PSP7 Vss Vdd RB0/INT0 RB1 RB2 RB3/PGM
NC0 RC0/TSOSO/T1CKI OSC2/CLKO OSC1/CLKI VSS Vdd RE2/CS#/AN7 RE1/WR#/AN6 RE0/RD#/AN5 RA5/AN4/SS#/C2OUT RA4/T0CKI/C1OUT
TP9 WRBUSY FCLKA DGND +5V IRIGCS# RTU-IOW# RTU-IOR#
TP15 TP14 TP7 TP8
TP13 TP12 TP6 TP5 TP10 TP11
VPP RB6 RB7 PIC_ACK
IRIG_RESET# R102 2.21K

IRIGB_IN
CR152 NRD4004 +5V
R126 6.81K
R114 6.81K DGND
R128 1M
R129 6.81K +5V
U52:A OP282 -12V +12V
R127 1.0K DGND
C36 .012uF
R136 6.81K
R135 6.81K
NRD4004 CR126
R132 0.0
IRIG_GND
J30 DUAL BNC
Top Bottom
IRIG B Input
Demodulated IRIG B Output
U52:B OP282
R134 56.2H
CR138 CR132 CR125 DGND

IRIGB_OUT
U41:A 74HC32SOIC
U41:B
U41:C
U41:D
IRIG_A IRIG_B IRIG_C IRIG_D
To Sheet 3 of 8
To Sheet 4 of 8
To Sheet 5 of 8
To Sheet 6 of 8
DGND

BP93 .1uF BP96 .1uF -12V +12V DGND
+5V DGND BP71 .1uF BP80 .1uF BP75 .1uF

PART #	C3800-002-REV-C	S 7-22-09	
SIZE	B	SHEET 2	OF 8

TO/FROM SHEET 1

COM-INT1#

+5V R96 6.81K — SYNC1 R1 6.81K — SYNC2 R6 6.81K — TR1 R14 6.81K — TR2 R15 6.81K

U1
Z85230-PLCC
COMM ADDRESS
140H-143H

IEO, IEI, INTACK, VCC, W-REQA, SYNCA, RTxCA, RxDA, TRxCA, TxDA, NC
A-B, CE, D-C, NC, GND, W-REQB, SYNCB, RTxCB, RxDB, TRxCB, TxDB
INT, D7, D5, D3, D1, D0, D2, D4, D6, RD, WR
NC, DTR-REQA, RTSA, CTSA, DCDA, PCLK, DCDB, CTSB, RTSB, DTR-REQB, NC

BSA1, CS-COM1&2#, BSA0, DGND, SYNC2, DGND, CH2-RX, TR2, CH2-TX

FROM OSCILATOR SHEET 8

FCLKA

CH1-DTR#, CH1-RTS#, CH1-CTS#, CH1-DCD#, CH2-DCD#, CH2-CTS#, CH2-RTS#, CH2-DTR#

U2 LT1141ACN — CH1-TX, CH1-RX, CH1-DTR#, CH1-DCD#, CH1-RTS#, CH1-CTS# → CH1-TX#, CH1-RX#, CH1-DTR, PORT1PWR, CH1-RTS, CH1-CTS

U3 LT1141ACN — CH2-TX, CH2-RX, CH2-DTR#, CH2-DCD#, CH2-RTS#, CH2-CTS# → CH2-TX#, CH2-RX#, CH2-DTR, PORT2PWR, CH2-RTS, CH2-CTS

U7 LT1141ACN — CH3-TX, CH3-RX, CH3-DTR#, CH3-DCD#, CH3-RTS#, CH3-CTS# → CH3-TX#, CH3-RX#, CH3-DTR, PORT3PWR, CH3-RTS, CH3-CTS

U8 LT1141ACN — CH4-TX, CH4-RX, CH4-DTR#, CH4-DCD#, CH4-RTS#, CH4-CTS# → CH4-TX#, CH4-RX#, CH4-DTR, PORT4PWR, CH4-RTS, CH4-CTS

TO/FROM SHEET 1

COM-INT1#

+5V R20 6.81K — SYNC3 R21 6.81K — SYNC4 R27 6.81K — TR3 R28 6.81K — TR4

U5
Z85230-PLCC
COMM ADDRESS
144H-147H

IEO, IEI, INTACK, VCC, W-REQA, SYNCA, RTxCA, RxDA, TRxCA, TxDA, NC
A-B, CE, D-C, NC, GND, W-REQB, SYNCB, RTxCB, RxDB, TRxCB, TxDB
INT, D7, D5, D3, D1, D0, D2, D4, D6, RD, WR
NC, DTR-REQA, RTSA, CTSA, DCDA, PCLK, DCDB, CTSB, RTSB, DTR-REQB, NC

BSA1, CS-COM3&4#, BSA0, DGND, SYNC4, DGND, CH4-RX, TR4, CH4-TX

FROM OSCILATOR SHEET 8

FCLKB

CH4-DTR#, CH4-RTS#, CH4-CTS#, CH4-DCD#

CH3-DTR#, CH3-RTS#, CH3-CTS#, CH3-DCD#

COMM ADDRESS
144H-147H

+5VF 6.2H — Q1 IRLML2402 (R7, R8 10K, R9 10K, C2 .022uF, C1 .022uF) — L1 100uH — CR5 NRD4004 — PORT1PWR

U6:A 74HC32SOIC — IRIG_A, DGND → R22 56.2H → IRIGB_P1

+5VF 6.2H — Q3 IRLML2402 (R29, R30 10K, R31 10K, C6 .022uF, C5 .022uF) — L3 100uH — CR19 NRD4004 — PORT2PWR

U6:D 74HC32SOIC — IRIG_A, DGND → R23 56.2H → IRIGB_P2

+5VF 6.2H — Q5 IRLML2402 (R40, R41 10K, R42 10K, C10 .022uF, C9 .022uF) — L5 100uH — CR33 NRD4004 — PORT3PWR

U16:A 74HC32SOIC — IRIG_A, DGND → R50 56.2H → IRIGB_P3

+5VF 6.2H — Q7 IRLML2402 (R58, R59 10K, R60 10K, C14 .022uF, C13 .022uF) — L7 100uH — CR47 NRD4004 — PORT4PWR

U16:D 74HC32SOIC — IRIG_A, DGND → R51 56.2H → IRIGB_P4

U4:B HCT14 — RTU-RESET# → RESET_LED

J1:A — PORT1PWR, CH1-RX#, CH1-TX#, CH1-RTS, CH1-CTS, PORT2PWR, CH2-RX#, CH2-TX#, CH2-RTS, CH2-CTS, PORT3PWR, CH3-RX#, CH3-TX#, CH3-RTS, CH3-CTS, PORT4PWR, CH4-RX#, CH4-TX#, CH4-RTS, CH4-CTS, DGND

Display Connector
For Ports 1 Through 4

J13:A — CON-DCD, CON-RX#, CON-RTS, CON-CTS, CON-TX#, PPP-DCD, PPP-RX#, PPP-RTS, PPP-CTS, PPP-TX#, +5V, RESET_LED, DGND, GP1, GP2, GP3, GP4, GP5, GP6, GP7, GP8, ALARM1, ALARM2, DGND

Processor Comm Port and General Purpose LED Connector

J2:A — PORT1PWR, CH1-RX#, CH1-TX#, IRIGB_P1, DGND, IRIG_GND, CH1-RTS, CH1-CTS

J4:A — PORT2PWR, CH2-RX#, CH2-TX#, IRIGB_P2, DGND, IRIG_GND, CH2-RTS, CH2-CTS

J6:A — PORT3PWR, CH3-RX#, CH3-TX#, IRIGB_P3, DGND, IRIG_GND, CH3-RTS, CH3-CTS

J9:A — PORT4PWR, CH4-RX#, CH4-TX#, IRIGB_P4, DGND, IRIG_GND, CH4-RTS, CH4-CTS

These ports are the first four bottom connectors Ports 1 – 4

GP1, GP2, GP3, GP4, GP5, GP6, GP7, GP8

From Sheet 2 General Purpose LED's

IRIGB_P4, IRIGB_P3, IRIGB_P2, IRIGB_P1, PORT4PWR, PORT3PWR, PORT2PWR, PORT1PWR, CON-RI, CON-DSR, CON-DTR, CON-DCD, CON-RX#, CON-TX#, CON-RTS, CON-CTS, CH1-RX#, CH1-TX#, CH1-RTS, CH1-CTS, CH2-RX#, CH2-TX#, CH2-RTS, CH2-CTS, CH3-RX#, CH3-TX#, CH3-RTS, CH3-CTS, CH4-RX#, CH4-TX#, CH4-RTS, CH4-CTS

CR54, CR40, CR26, CR12, CR44, CR30, CR16, CR2, CR129, CR136, CR128, CR137, CR135, CR133, CR134, CR127, CR3, CR13, CR1, CR11, CR17, CR27, CR15, CR25, CR31, CR41, CR29, CR39, CR45, CR55, CR43, CR53 — DGND

+12V: BP1 .1uF, BP3 .1uF, BP9 .1uF, BP11 .1uF
-12V: BP7 .1uF, BP6 .1uF, BP15 .1uF, BP16 .1uF
+5V: BP5 .1uF, BP8 .1uF, BP2 .1uF, BP4 .1uF, BP10 .1uF, BP12 .1uF, BP14 .1uF
DGND

PART #	C3800-002-REV-C	5-22-09	
SIZE	B	COMM1	SHEET 3 OF 8

TO/FROM SHEET 1

COM-INT1#

D7 D5 D3 D1 D0 D2 D4 D6 RTU-IOR# RTU-IOW#

+5V

R54 6.81K SYNC5

R55 6.81K SYNC6

R56 6.81K TR5

R57 6.81K TR6

SYNC5

DGND

CH5-RX

TR5

CH5-TX

U17
Z85230-PLCC
COMM ADDRESS
148H-14BH

INT D7 D5 D3 D1 D0 D2 D4 D6 RD WR

IEO
IEI
INTACK
VCC
W-REQA
SYNCA
RTxCA
RxDA
TRxCA
TxDA
NC

A-B BSA1
CE CS-COM5&6#
D-C BSA0
NC
GND DGND
W-REQB SYNC6
SYNCB DGND
RTxCB TR6
RxDB CH6-RX
TRxB CH6-TX
TxDB

NC DTR-REQA RTSA CTSA DCDA PCLK DCDB CTSB RTSB DTR-REQB NC

FROM OSCILATOR SHEET 8

FCLKA

CH5-DTR# CH5-RTS# CH5-CTS# CH5-DCD# CH6-DCD# CH6-CTS# CH6-RTS# CH6-DTR#

TO/FROM SHEET 1

COM-INT1#

D7 D5 D3 D1 D0 D2 D4 D6 RTU-IOR# RTU-IOW#

+5V

R64 6.81K SYNC7

R65 6.81K SYNC8

R66 6.81K TR7

R67 6.81K TR8

SYNC7

DGND

CH7-RX

TR7

CH7-TX

U20
Z85230-PLCC
COMM ADDRESS
14CH-14FH

INT D7 D5 D3 D1 D0 D2 D4 D6 RD WR

IEO
IEI
INTACK
VCC
W-REQA
SYNCA
RTxCA
RxDA
TRxCA
TxDA
NC

A-B BSA1
CE CS-COM7&8#
D-C BSA0
NC
GND DGND
W-REQB SYNC8
SYNCB DGND
RTxCB TR8
RxDB CH8-RX
TRxB CH8-TX
TxDB

NC DTR-REQA RTSA CTSA DCDA PCLK DCDB CTSB RTSB DTR-REQB NC

FROM OSCILATOR SHEET 8

FCLKB

CH8-DTR# CH8-RTS# CH8-CTS# CH8-DCD#

COMM ADDRESS
144H-147H

CH7-DTR# CH7-RTS# CH7-CTS# CH7-DCD#

U18

-12V +12V +5V

CH5-TX CH5-RX CH5-DTR# CH5-DCD# CH5-RTS# CH5-CTS#

CH5-TX# CH5-RX# CH5-DTR PORT5PWR CH5-RTS CH5-CTS

DGND +5V

TTL RS232

LT1141ACN

U19

-12V +12V +5V

CH6-TX CH6-RX CH6-DTR# CH6-DCD# CH6-RTS# CH6-CTS#

CH6-TX# CH6-RX# CH6-DTR PORT6PWR CH6-RTS CH6-CTS

DGND +5V

TTL RS232

LT1141ACN

U21

-12V +12V +5V

CH7-TX CH7-RX CH7-DTR# CH7-DCD# CH7-RTS# CH7-CTS#

CH7-TX# CH7-RX# CH7-DTR PORT7PWR CH7-RTS CH7-CTS

DGND +5V

TTL RS232

LT1141ACN

U22

-12V +12V +5V

CH8-TX CH8-RX CH8-DTR# CH8-DCD# CH8-RTS# CH8-CTS#

CH8-TX# CH8-RX# CH8-DTR PORT8PWR CH8-RTS CH8-CTS

DGND +5V

TTL RS232

LT1141ACN

+5VF

6.2H R68 Q9 D G S L9 100uH CR61 NRD4004 PORT5PWR

R69 10K IRLML2402 C18 .022uF C17 .022uF

R70 10K DGND

U26:A 74HC32SOIC

IRIG_B 1 2 3 R78 56.2H IRIGB_P5

+5VF

6.2H R84 Q11 D G S L11 100uH CR75 NRD4004 PORT6PWR

R85 10K IRLML2402 C22 .022uF C21 .022uF

10K R86 DGND

U26:D 74HC32SOIC

IRIG_B 12 13 11 R79 56.2H IRIGB_P6

DGND

+5VF

6.2H R93 Q13 D G S L13 100uH CR89 NRD4004 PORT7PWR

R95 10K IRLML2402 C26 .022uF C25 1uF

R94 10K DGND

U38:A 74HC32SOIC

IRIG_B 1 2 3 R103 56.2H IRIGB_P7

+5VF

6.2H R108 Q15 D G S L15 100uH CR103 NRD4004 PORT8PWR

R109 10K IRLML2402 C30 .022uF C29 .022uF

10K R110 DGND

U38:D 74HC32SOIC

IRIG_B 12 13 11 R104 56.2H IRIGB_P8

DGND

J8:A

PORT5PWR 1
CH5-RX# 2
CH5-TX# 3
CH5-RTS 4
CH5-CTS 5
PORT6PWR 6
CH6-RX# 7
CH6-TX# 8
CH6-RTS 9
CH6-CTS 10
PORT7PWR 11
CH7-RX# 12
CH7-TX# 13
CH7-RTS 14
CH7-CTS 15
PORT8PWR 16
CH8-RX# 17
CH8-TX# 18
CH8-RTS 19
CH8-CTS 20
21 22 23 24
DGND 25

Display Connector For Ports 5 thru 8

PORT5PWR 1
CH5-RX# 2
CH5-TX# 3
IRIGB_P5 4
DGND 5
IRIG_GND 6
CH5-RTS 7
CH5-CTS 8
9

J11:A

PORT6PWR 1
CH6-RX# 2
CH6-TX# 3
IRIGB_P6 4
DGND 5
IRIG_GND 6
CH6-RTS 7
CH6-CTS 8
9

J14:A

PORT7PWR 1
CH7-RX# 2
CH7-TX# 3
IRIGB_P7 4
DGND 5
IRIG_GND 6
CH7-RTS 7
CH7-CTS 8
9

J17:A

PORT8PWR 1
CH8-RX# 2
CH8-TX# 3
IRIGB_P8 4
DGND 5
IRIG_GND 6
CH8-RTS 7
CH8-CTS 8
9

J19:A

These ports are the second four bottom connectors. Ports 5 – 8

IRIGB_P8 IRIGB_P7 IRIGB_P6 IRIGB_P5 PPP-RI PPP-DSR PPP-DTR PPP-DCD PPP-RX# PPP-TX# PPP-RTS PPP-CTS PORT5PWR PORT6PWR PORT7PWR PORT8PWR CH5-RX# CH5-TX# CH5-RTS CH5-CTS CH6-RX# CH6-TX# CH6-RTS CH6-CTS CH7-RX# CH7-TX# CH7-RTS CH7-CTS CH8-RX# CH8-TX# CH8-RTS CH8-CTS

CR110 CR96 CR82 CR68 CR118 CR114 CR117 CR115 CR116 CR120 CR113 CR119 CR58 CR72 CR86 CR100 CR59 CR69 CR57 CR67 CR73 CR83 CR71 CR81 CR87 CR97 CR85 CR95 CR101 CR111 CR99 CR109

DGND

+12V

BP32 .1uF BP34 .1uF BP40 .1uF BP42 .1uF

-12V

BP37 .1uF BP38 .1uF BP44 .1uF BP45 .1uF

+5V

BP31 .1uF BP39 .1uF BP33 .1uF BP35 .1uF BP41 .1uF BP43 .1uF BP53 .1uF

DGND

PART #	C3800-002-REV-C		7-22-09
SIZE	B	COMM2	SHEET 4 OF 8

TO/FROM SHEET 1

COM-INT2#

+5V R39 6.81K

R32 6.81K SYNC9

R33 6.81K SYNC10

R37 6.81K TR9

R38 6.81K TR10

SYNC9

DGND

CH9-RX

TR9

CH9-TX

U10
Z85230-PLCC
COMM ADDRESS
180H-183H

IEO, IEI, INTACK, VCC, W-REQA, SYNCA, RTxCA, RxDA, TRxCA, TxDA, NC

A-B, CE, D-C, NC, GND, W-REQB, SYNCB, RTxCB, RxDB, TRxCB, TxDB

BSA1, CS-COM9&10#, BSA0, DGND, SYNC10, DGND, CH10-RX, TR10, CH10-TX

INT, D7, D5, D3, D1, D0, D2, D4, D6, RD, WR

NC, DTR-REQA, RTSA, CTSA, DCDA, PCLK, DCDB, CTSB, RTSB, DTR-REQB, NC

RTU-IOR#, RTU-IOW#

FROM OSCILATOR SHEET 8

FCLKA

CH9-DTR#, CH9-RTS#, CH9-CTS#, CH9-DCD#, CH10-DCD#, CH10-CTS#, CH10-RTS#, CH10-DTR#

TO/FROM SHEET 1

COM-INT2#

+5V R44 6.81K SYNC11

R43 6.81K SYNC12

R46 6.81K TR11

R45 6.81K TR12

U13
Z85230-PLCC
COMM ADDRESS
184H-187H

SYNC11, DGND, CH11-RX, TR11, CH11-TX

BSA1, CS-COM11&12#, BSA0, DGND, SYNC12, DGND, CH12-RX, TR12, CH12-TX

FROM OSCILATOR SHEET B

FCLKB

COMM ADDRESS
144H-147H

CH11-DTR#, CH11-RTS#, CH11-CTS#, CH11-DCD#, CH12-DCD#, CH12-CTS#, CH12-RTS#, CH12-DTR#

U11
LT1141ACN
TTL | RS232

-12V, +12V, +5V, DGND

CH9-TX, CH9-RX, CH9-DTR#, CH9-DCD#, CH9-RTS#, CH9-CTS#

CH9-TX#, CH9-RX#, CH9-DTR, PORT9PWR, CH9-RTS, CH9-CTS

U12
LT1141ACN
TTL | RS232

CH10-TX, CH10-RX, CH10-DTR#, CH10-DCD#, CH10-RTS#, CH10-CTS#

CH10-TX#, CH10-RX#, CH10-DTR, PORT10PWR, CH10-RTS, CH10-CTS

U14
LT1141ACN
TTL | RS232

CH11-TX, CH11-RX, CH11-DTR#, CH11-DCD#, CH11-RTS#, CH11-CTS#

CH11-TX#, CH11-RX#, CH11-DTR, PORT11PWR, CH11-RTS, CH11-CTS

U15
LT1141ACN
TTL | RS232

CH12-TX, CH12-RX, CH12-DTR#, CH12-DCD#, CH12-RTS#, CH12-CTS#

CH12-TX#, CH12-RX#, CH12-DTR, PORT12PWR, CH12-RTS, CH12-CTS

+5VF

R17 6.2H, R18 10K, Q2 IRLML2402, L2 100uH, CR10 NRD4004, PORT9PWR

R19 10K, C4 .022uF, C3 .022uF

U6:B 74HC32SOIC, IRIG_C, R24 56.2H, IRIGB_P9

R34 6.2H, R35 10K, Q4 IRLML2402, L4 100uH, CR24 NRD4004, PORT10PWR

R36 10K, C8 .022uF, C7 .022uF

U6:C 74HC32SOIC, IRIG_C, R25 56.2H, IRIGB_P10

R47 6.2H, R48 10K, Q6 IRLML2402, L6 100uH, CR38 NRD4004, PORT11PWR

R49 10K, C12 .022uF, C11 .022uF

U16:B 74HC32SOIC, IRIG_C, R52 56.2H, IRIGB_P11

R61 6.2H, R62 10K, Q8 IRLML2402, L8 100uH, CR52 NRD4004, PORT12PWR

R63 10K, C16 .022uF, C15 .022uF

U16:C 74HC32SOIC, IRIG_C, R53 56.2H, IRIGB_P12

DGND

J1:Z

PORT9PWR, CH9-RX#, CH9-TX#, CH9-RTS, CH9-CTS, PORT10PWR, CH10-RX#, CH10-TX#, CH10-RTS, CH10-CTS, PORT11PWR, CH11-RX#, CH11-TX#, CH11-RTS, CH11-CTS, PORT12PWR, CH12-RX#, CH12-TX#, CH12-RTS, CH12-CTS, DGND

Display Connector
For Ports 9 and 16

J3:A: PORT9PWR, CH9-RX#, CH9-TX#, IRIGB_P9, DGND, IRIG_GND, CH9-RTS, CH9-CTS

J5:A: PORT10PWR, CH10-RX#, CH10-TX#, IRIGB_P10, DGND, IRIG_GND, CH10-RTS, CH10-CTS

J7:A: PORT11PWR, CH11-RX#, CH11-TX#, IRIGB_P11, DGND, IRIG_GND, CH11-RTS, CH11-CTS

J10:A: PORT12PWR, CH12-RX#, CH12-TX#, IRIGB_P12, DGND, IRIG_GND, CH12-RTS, CH12-CTS

These ports are the first four Top connectors. Ports 9 – 12

IRIGB_P9, IRIGB_P10, IRIGB_P11, IRIGB_P12, PORT12PWR, PORT11PWR, PORT10PWR, PORT9PWR, PPP-RI, PPP-DSR, PPP-DTR, PPP-DCD, PPP-RX#, PPP-TX#, PPP-RTS, PPP-CTS, CH9-RX#, CH9-TX#, CH9-RTS, CH9-CTS, CH10-RX#, CH10-TX#, CH10-RTS, CH10-CTS, CH11-RX#, CH11-TX#, CH11-RTS, CH11-CTS, CH12-RX#, CH12-TX#, CH12-RTS, CH12-CTS

CR14, CR28, CR42, CR56, CR46, CR32, CR18, CR4, CR122, CR144, CR130, CR143, CR142, CR131, CR145, CR146, CR7, CR6, CR8, CR9, CR21, CR20, CR22, CR23, CR35, CR34, CR36, CR37, CR49, CR48, CR50, CR51

DGND

+12V: BP18 .1uF, BP20 .1uF, BP24 .1uF, BP26 .1uF

-12V: BP22 .1uF, BP23 .1uF, BP29 .1uF, BP30 .1uF

+5V: BP17 .1uF, BP28 .1uF, BP19 .1uF, BP21 .1uF, BP25 .1uF, BP27 .1uF, BP36 .1uF

DGND

PART #	C3800-002-REV-C		7-22-09
SIZE	B	COMM3	SHEET 5 OF 8

TO/FROM SHEET 1

COM-INT2#

D7 D5 D3 D1 D0 D2 D4 D6 RTU-IOR# RTU-IOW#

INT D7 D5 D3 D1 D0 D2 D4 D6 RD WR

+5V

R71 6.81K SYNC13

R72 6.81K SYNC14

R76 6.81K TR13

R77 6.81K TR14

SYNC13

DGND

CH13-RX

TR13

CH13-TX

U23
Z85230-PLCC
COMM ADDRESS
188H-18BH

IEO IEI INTACK VCC W-REQA SYNCA RTxCA RxDA TRxCA TxDA NC

A-B CE D-C NC GND W-REQB SYNCB RTxCB RxDB TRxCB TxDB

BSA1 CS-COM13&14# BSA0 DGND SYNC14 DGND CH14-RX TR14 CH14-TX

NC DTR-REQA RTSA CTSA DCDA PCLK DCDB CTSB RTSB DTR-REQB NC

FROM OSCILATOR SHEET 8

FCLKA

CH13-DTR# CH13-RTS# CH13-CTS# CH13-DCD#

CH14-DCD# CH14-CTS# CH14-RTS# CH14-DTR#

U24

-12V +12V +5V

CH13-TX CH13-RX CH13-DTR# CH13-DCD# CH13-RTS# CH13-CTS#

CH13-TX# CH13-RX# CH13-DTR PORT13PWR CH13-RTS CH13-CTS

DGND

TTL | RS232

LT1141ACN

U25

CH14-TX CH14-RX CH14-DTR# CH14-DCD# CH14-RTS# CH14-CTS#

CH14-TX# CH14-RX# CH14-DTR PORT14PWR CH14-RTS CH14-CTS

LT1141ACN

U28

CH15-TX CH15-RX CH15-DTR# CH15-DCD# CH15-RTS# CH15-CTS#

CH15-TX# CH15-RX# CH15-DTR PORT15PWR CH15-RTS CH15-CTS

LT1141ACN

+5VF

R74 10K R73 6.2H

Q10 IRLML2402

L10 100uH

CR66 NRD4004 PORT13PWR

C20 .022uF C19 .022uF

R75 10K

U26:B 74HC32SOIC

IRIG_D R80 56.2H IRIGB_P13

R90 10K R89 6.2H

Q12 IRLML2402

L12 100uH

CR80 NRD4004 PORT14PWR

C24 .022uF C23 .022uF

R91 10K

U26:C 74HC32SOIC

IRIG_D R81 56.2H IRIGB_P14

R99 10K R97 6.2H

Q14 IRLML2402

L14 100uH

CR94 NRD4004 PORT15PWR

C28 .022uF C27 .022uF

R98 10K

U38:B 74HC32SOIC

IRIG_D R105 56.2H IRIGB_P15

R112 10K R111 6.2H

Q16 IRLML2402

L16 100uH

CR108 NRD4004 PORT16PWR

C32 .022uF C31 .022uF

R113 10K

U38:C 74HC32SOIC

IRIG_D R106 56.2H IRIGB_P16

J8:Z

PORT13PWR CH13-RX# CH13-TX# CH13-RTS CH13-CTS PORT14PWR CH14-RX# CH14-TX# CH14-RTS CH14-CTS PORT15PWR CH15-RX# CH15-TX# CH15-RTS CH15-CTS PORT16PWR CH16-RX# CH16-TX# CH16-RTS CH16-CTS DGND

Display Connector For Ports 13-16

J12:A

PORT13PWR CH13-RX# CH13-TX# IRIGB_P13 DGND IRIG_GND CH13-RTS CH13-CTS

J15:A

PORT14PWR CH14-RX# CH14-TX# IRIGB_P14 DGND IRIG_GND CH14-RTS CH14-CTS

J18:A

PORT15PWR CH15-RX# CH15-TX# IRIGB_P15 DGND IRIG_GND CH15-RTS CH15-CTS

J20:A

PORT16PWR CH16-RX# CH16-TX# IRIGB_P16 DGND IRIG_GND CH16-RTS CH16-CTS

These ports are the second four top connectors. Ports 13 - 16

TO/FROM SHEET 1

COM-INT2#

D7 D5 D3 D1 D0 D2 D4 D6 RTU-IOR# RTU-IOW#

INT D7 D5 D3 D1 D0 D2 D4 D6 RD WR

+5V

R82 6.81K SYNC15

R83 6.81K SYNC16

R87 6.81K TR15

R88 6.81K TR16

SYNC15

DGND

CH15-RX

TR15

CH15-TX

U27
Z85230-PLCC
COMM ADDRESS
18CH-18FH

IEO IEI INTACK VCC W-REQA SYNCA RTxCA RxDA TRxCA TxDA NC

A-B CE D-C NC GND W-REQB SYNCB RTxCB RxDB TRxCB TxDB

BSA1 CS-COM15&16# BSA0 DGND SYNC16 DGND CH16-RX TR16 CH16-TX

NC DTR-REQA RTSA CTSA DCDA PCLK DCDB CTSB RTSB DTR-REQB NC

FROM OSCILATOR SHEET 8

FCLKB

CH16-DTR# CH16-RTS# CH16-CTS# CH16-DCD#

COMM ADDRESS 144H-147H

CH15-DTR# CH15-RTS# CH15-CTS# CH15-DCD#

IRIGB_P16 IRIGB_P15 IRIGB_P14 IRIGB_P13 PORT13PWR PORT14PWR PORT15PWR PORT16PWR CH13-RX# CH13-TX# CH13-RTS CH13-CTS CH14-RX# CH14-TX# CH14-RTS CH14-CTS CH15-RX# CH15-TX# CH15-RTS CH15-CTS CH16-RX# CH16-TX# CH16-RTS CH16-CTS DGND

CR112 CR98 CR84 CR70 CR60 CR74 CR88 CR102 CR63 CR62 CR64 CR65 CR77 CR76 CR78 CR79 CR91 CR90 CR92 CR93 CR105 CR104 CR106 CR107

+12V

BP47 .1uF BP49 .1uF BP54 .1uF BP56 .1uF

DGND

-12V

BP51 .1uF BP52 .1uF BP59 .1uF BP60 .1uF

+5V

BP46 .1uF BP58 .1uF BP48 .1uF BP50 .1uF BP55 .1uF BP57 .1uF BP74 .1uF

PART #	C3800-002-REV-C		6-7-22-09
SIZE	B	COMM 4	SHEET 6 OF 8

TO/FROM SHEET 1

RTU-IOW#
RTU-IOR#
BSA2
BSA1
BSA0
IOPLD#
RTU-RESET#
D0
D1
D2
D3
D4
D5
D6
D7
FCLKB
8MHZ
SPARE7
SPARE73
SPARE77
SPARE1
SPARE70
R123
6.81K
+5V
DGND

U55
PLDx2
IOWR
IORD
BA2
BA1
BA0
CSIOPLD
RESET
D0
D1
D2
D3
D4
D5
D6
D7

RB-SEL0
RB-SEL1
RB-SEL2
RB-SEL3
RB-SEL4
RB-SEL5
RB-SEL6
RB-SEL7
RB-SEL8
RB-SEL9
RB-SEL10
RB-SEL11
RB-SEL12
RB-SEL13
RB-SEL14
RB-SEL15
SERDAT
SD-CLK
NCONFIG
RTU-RESET#
MSEL0
MSEL1
NSP
NC
NC
SBO-STB
LOCAL
REMOTE#
EXEC0
EXEC1
EXEC2
EXEC3
SB-SE
EXEC3

RN7
1M
RN6
220K
RN3
1M
RN2
220K
RN10
10K
RN5
10K
FROM SHEET 6
EXE-PWR

U54
UCN5821LW
SD-CLK
SERDAT
SBO-STB
SBO-OE#
CLK
SDI
STB
OE
VDD
GND
VBB
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
SDO
CSEL0
CSEL1
CSEL2
CSEL3
CSEL4
CSEL5
CSEL6
CSEL7

SBO SINK DRIVERS

U51
UCN5821LW
FROM SHEET 1
FROM SHEET U38
CSEL8
CSEL9
CSEL10
CSEL11
CSEL12
CSEL13
CSEL14
CSEL15

SBO SOURCE DRIVERS

U56
74HCT238SOL
A0
A1
A2
E1
E2
E3
VCC
GND

U57
UDN2982SLW
VS
NC10
GND
NC11
CEXEC0
CEXEC1
CEXEC2
CEXEC3
CEXEC4
CEXEC5
CEXEC6
CEXEC7
CEXEC0
CEXEC1
CEXEC2
CEXEC3
CEXEC4
CEXEC5
CEXEC6
CEXEC7

EXE-PWR
From Sheet 6

SBO BUS #1
J31:A

RN11
10K
SBO EXECUTE MATRIX
PULL DOWN RESISTORS

RB-EXEC0
RB-EXEC1
RB-EXEC2
RB-EXEC3
RB-EXEC4
RB-EXEC5
RB-EXEC6
RB-EXEC7
RB-EXEC8
RB-EXEC9
RB-EXEC10
RB-EXEC11
RB-EXEC12
RB-EXEC13
RB-EXEC14
RB-EXEC15

SBO EXECUTE MATRIX
READ BACK REGISTERS

RN4
10K
RN8
220K
RN9
1M

U53
EPC1064
DATA
DCLK
NCASC
OE
NCS
GND
VCC
DATA
DCLK
STATUS
C_DONE
R131
1.0K
R130
1.0K
R148
R149
6.81K
PCI1
PCI0

BP105 .1uF
BP95 .1uF
BP101 .1uF
BP97 .1uF
BP98 .1uF
BP92 .1uF
BP102 .1uF
BP99 .1uF
BP86 .1uF
BP94 .1uF
BP73 .1uF
BP85 .1uF
BP84 .1uF
BP87 .1uF

Data Bus
To Sheet 1
BDATA
To Sheet 1

U50
EPM7032SPLCC44
PLDx4
PLDX4
LS-A1
SBO-OE#
TMS
TDI
TDO
TMS
TCK
RTU-RESET#
SBSEL1
SBSEL2
SBSEL3
SBSEL4
SBSEL5
SBSEL6
SBSEL7
BSA3
BSA2
BSA4
ALARM1
ALARM2
DIXT#
D7
D4
D6
BSA1
BSA0
ALARM#
LS-A0
SBO#
STATUS#

U47
74AHCT245SOL
DIXT#
CE- VCC
DIR GND
1=A>B
D0
D1
D2
D3
D4
D5
D6
D7
A0
A1
A2
A3
A4
A5
A6
A7
B0
B1
B2
B3
B4
B5
B6
B7
DI-D0
DI-D1
DI-D2
DI-D3
DI-D4
DI-D5
DI-D6
DI-D7

U49
74AHCT245SOL
LS-A0
LS-A1
SBSEL1
SBSEL2
SBSEL3
SBSEL4
SBSEL5
SBSEL6
B-LS-A0
B-LS-A1
B-SBSEL1
B-SBSEL2
B-SBSEL3
B-SBSEL4
B-SBSEL5
B-SBSEL6
B-SBSEL7

RN1
SOICRES8D1002
10.00K

J24:A
Status Bus Expansion

To J13
Sheet 3 of 8

ALARM1
ALARM2
R144
6.81K
R143
6.81K
R142
6.81K
R141
6.81K
Q19
Q18
IRFR014
CR147
NRD4004
CR149
NRD4004
K1
K2
2FCDIP
C37
.022uF
C41
.022uF
C43
.022uF
C44
.022uF
EGND
STD1
TB2:A
TB2:D
Q1-Q5
PINOUT OF FETS
D
G S

Wed Jul 22, 2009
15:05:15

PART #	C3800-002-REV-C	SBO	
SIZE	B	SHEET 7 OF 8	

7-22-09

INPUT
Terminal Block

AC Line or DC+

AC Neutral
Or DC−

EGND

Internal Input Cable
Between Terminal Block
and Power Supply Input

J1
L
N

Power Supply
85−264VAC, 85−350VDC
OR
20 − 60 VDC

+5V
+5V
GND
GND
+15V
−15V
NC

Internal Cable between
Power Supply output and
Main Logic Board

EGND
Lug and
Mounting Hole

TB1:A
From Internal
Power Supply

1
2
3
4
5
6

−15V
+15V
DGND
+5V
DGND

C38 100uF
C39 100uF
C40 100uF
CR148 SMBJ8.0

+15V
CR140 18V
78L12ACD
VR1
VIN GND GND
VOUT GND GND
C34 4.7uF
BP90 .1uF
CR124 15V
+12V
DGND

−15V
CR139 18V
79L12ACD
VR2
VIN VIN GND
VOUT VIN VIN
C33 4.7uF
BP89 .1uF
CR123 15V
−12V
DGND

+15V
CR141 18V
UA7805C
VR3
IN
DGND DGND
OUT
C35 4.7uF
BP91 .1uF
CR121 SMBJ8.0
+5VF
DGND

TB3:A
1
2
+15V
On = LOCAL
Off = REMOTE

External R/L
Switch

CR151 18V
R147 6.81K
LOCAL
DGND

OP2
H11L1S
LOCAL
DGND
+5V
DGND

+5V
R146 1.0K
RTU−RESET#
OP1
H11L1S
+5V
DGND
BP100 .1uF
REMOTE#
TO SHEET 5

CAP DELAYS SBO
POWER TILL +5V
BECOMES STABLE
DGND

+5V
R145 6.81K
Q20
Q17
IRLML2402
IRLML2402
BP103 .1uF
BP104 .1uF
DGND

PS1
IN+
IN−
ISOLATION
OUT+
COM
OUT−
5V+/−15V
C42 4.7uF
EXE−PWR
DGND

D
G S
Q1−Q5
PINOUT OF FETS

To Pages 3, 4, & 5
Tranzorbe

2MM Transition Cable

J27:A
PPP−DCD
PPP−DSR
PPP−RX#
PPP−RTS
PPP−TX#
PPP−CTS
PPP−DTR
PPP−RI
DGND
CON−DCD
CON−DSR
CON−RX#
CON−RTS
CON−TX#
CON−CTS
CON−DTR
CON−RI
DGND

J21:A
CPU Comm
Port 1
PPP−DCD
PPP−DSR
PPP−RX#
PPP−RTS
PPP−TX#
PPP−CTS
PPP−DTR
PPP−RI
DGND

CPU Comm
Port 2
J23:A
CON−DCD
CON−DSR
CON−RX#
CON−RTS
CON−TX#
CON−CTS
CON−DTR
CON−RI
DGND

J25:A
Rear PPP Port*
PPP−DCD
PPP−RX#
PPP−TX#
PPP−DTR
DGND
PPP−DSR
PPP−RTS
PPP−CTS
PPP−RI

* Front and Rear PPP Ports are wired in parallel.
Only one port can be used at a time.

J33:A
Front PPP Port*
PPP−DCD
PPP−RX#
PPP−TX#
PPP−DTR
DGND
PPP−DSR
PPP−RTS
PPP−CTS
PPP−RI

J32:A
Console Port
CON−DCD
CON−RX#
CON−TX#
CON−DTR
DGND
CON−DSR
CON−RTS
CON−CTS
CON−RI

J16 Verticle
Ethernet connector
J16
TELCO_8H
J22
TELCO_8H
TX+
TX−
RX+
RX−

Ethernet Port
Front RJ45 Connector

TP2
TO SH 3
R16 0.0
R26 0.0
U4:C
U4:D
HCT14
FCLKA
FCLKB
14.7456Mhz
VCC OUTPUT
U9
NC GND
+5V
DGND
TO SH 2
U4:E
U4:A
U4:F
HCT14
+5V
DGND

TP17
TP22
TP16
TP21
TP19
TP20
TP1
TP23
TP3
TP18
−15V
+15V
+5VF
+5V
+12V
−12V
DGND
TEST POINTS

BP65 .1uF
BP72 .1uF
BP78 .1uF
BP13 .1uF
+5V
DGND

W2
Reset for
486 CPU

R124 6.81K
SW1
RESET PUSHBUTTON
BP88 .1uF
CR150
SMBJ8.0
+5V
DGND

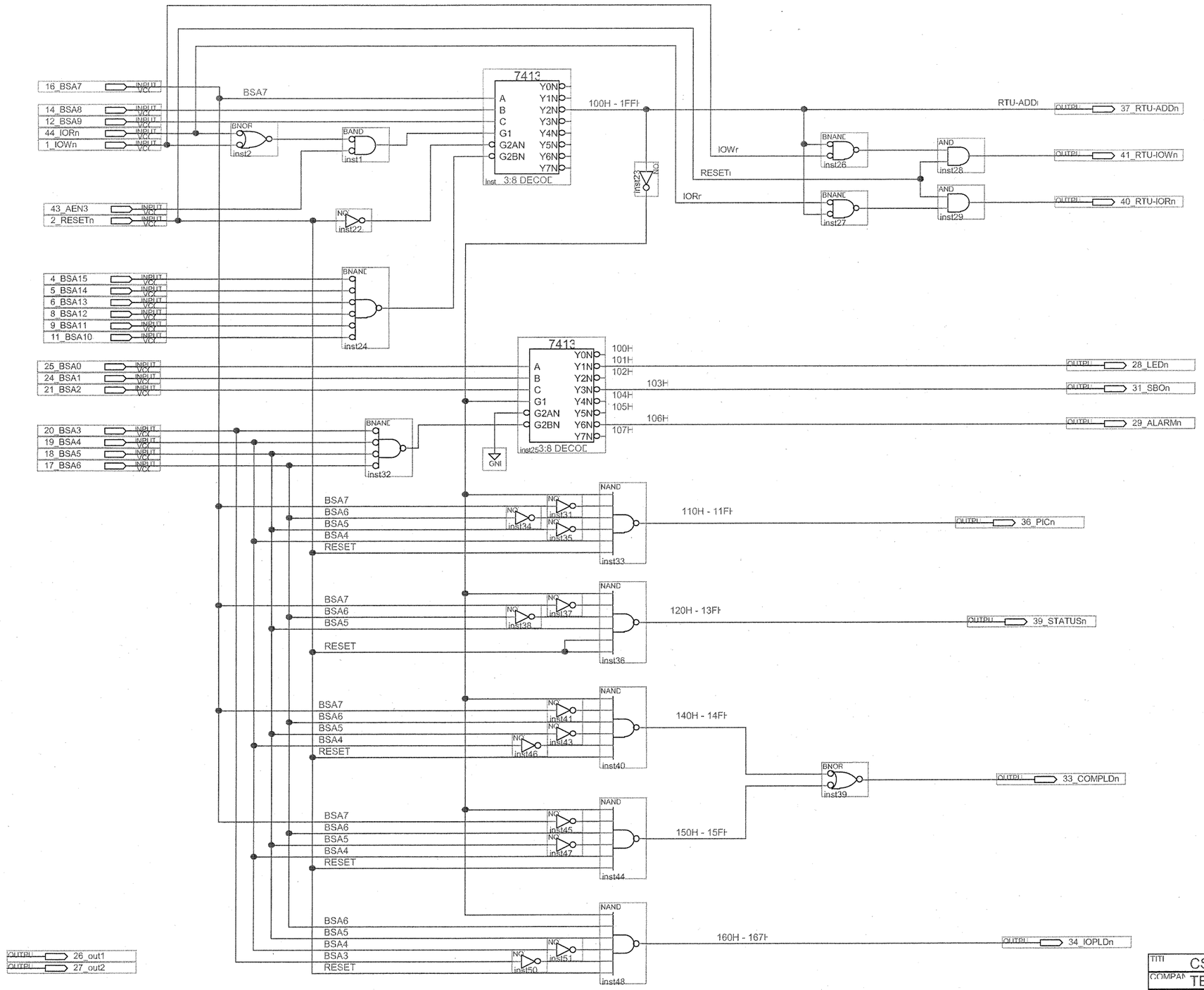
FROM BATTERY
BACKUP ON MEMORY PAGE 2

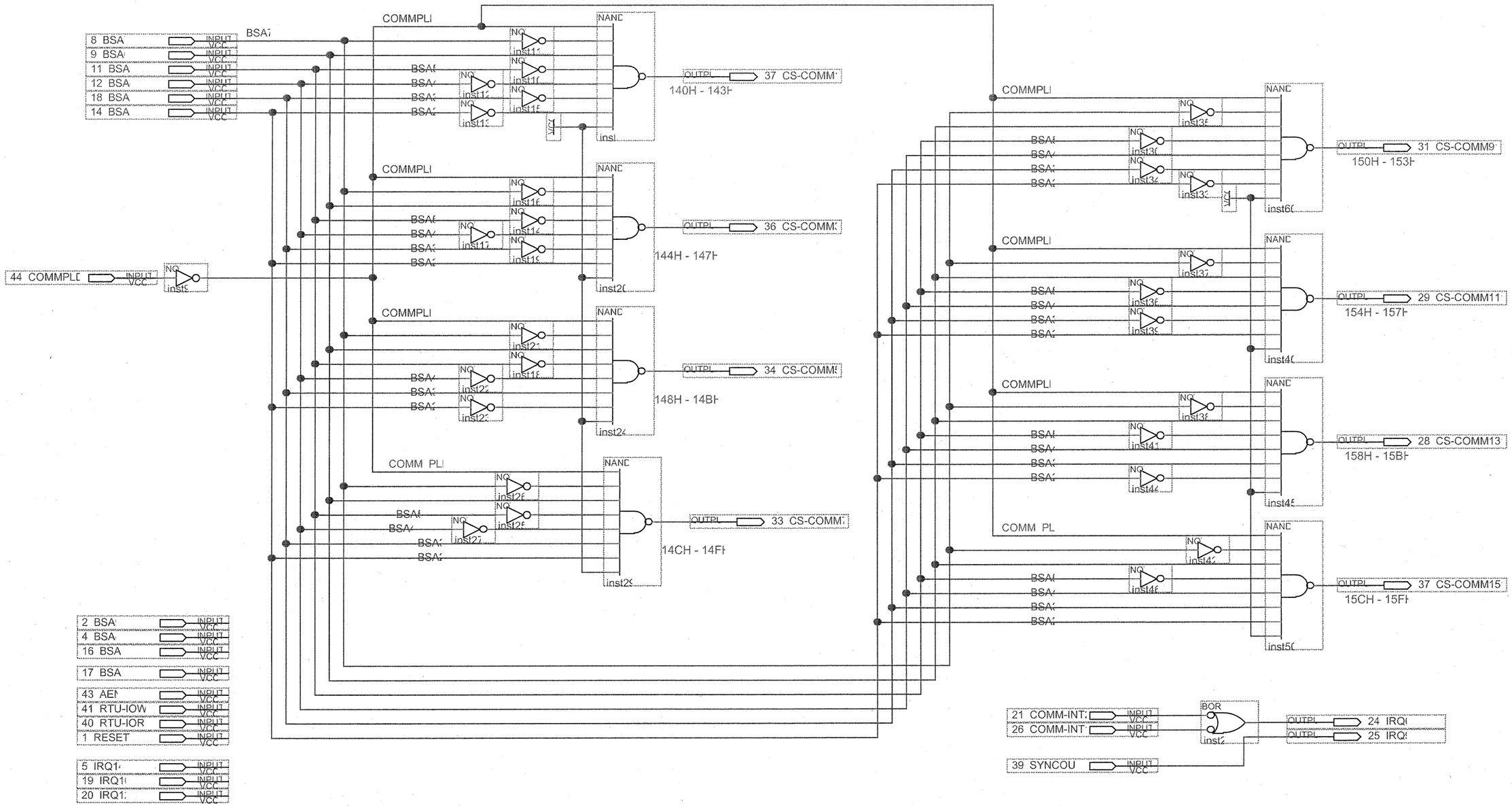
J26:A
R140 6.81K
R139 6.81K
R125 6.81K
R138 6.81K
+5V
DGND
TCK
TDO
TMS
RB7
RB6
VPP
IRIG−B
PROGRAMMING
PINS
PLDX1

THIS BUS GOES TO THE EPLDS
PLDx1, x2, x3 and x4 IN THAT ORDER

PINS 6,7,8 AND 10 ARE USED
TO PROGRAM THE IRIG−B
CHIP

PART #	C3800−002−REV−C	7-22-09	
SIZE	B	SHEET 8 OF 8	

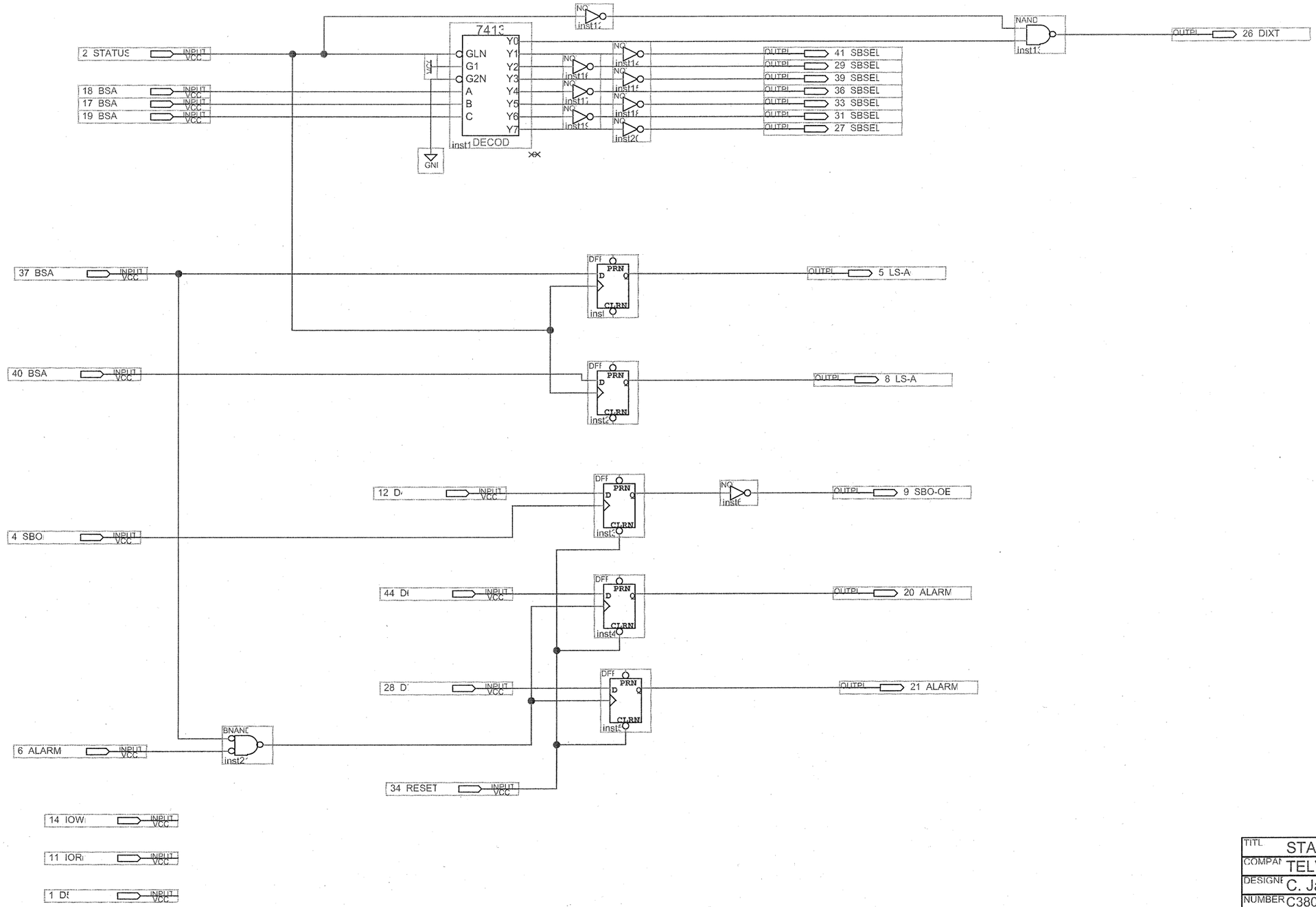

16_BSA7
14_BSA8
12_BSA9
44_IORn
1_IOWn
43_AEN3
2_RESETn
4_BSA15
5_BSA14
6_BSA13
8_BSA12
9_BSA11
11_BSA10
25_BSA0
24_BSA1
21_BSA2
20_BSA3
19_BSA4
18_BSA5
17_BSA6
INPUT
VCC
BSA7
BNOR
inst2
BAND
inst1
7413
A
B
C
G1
G2AN
G2BN
Y0N
Y1N
Y2N
Y3N
Y4N
Y5N
Y6N
Y7N
inst 3:8 DECOD
100H - 1FFH
NO
inst22
inst23
IOWr
RESETr
IORr
BNAND
inst26
inst27
AND
inst28
inst29
RTU-ADDr
OUTPU
37_RTU-ADDn
41_RTU-IOWn
40_RTU-IORn
BNAND
inst24
7413
inst25
3:8 DECOD
100H
101H
102H
103H
104H
105H
106H
107H
GNI
28_LEDn
31_SBOn
29_ALARMn
BNAND
inst32
NAND
BSA7
BSA6
BSA5
BSA4
BSA3
RESET
NO
inst34
inst35
inst37
inst38
inst41
inst43
inst46
inst45
inst47
inst50
inst51
inst33
inst36
inst40
inst44
inst48
110H - 11FH
120H - 13FH
140H - 14FH
150H - 15FH
160H - 167H
36_PICn
39_STATUSn
BNOR
inst39
33_COMPLDn
34_IOPLDn
26_out1
27_out2
TITL
CSPLD U44
COMPAN
TELVENT
DESIGNE
C.Janik
5-12-05
NUMBER
C3800-002-PLDA1
REV
A
DAT
Thu May 12 07:42:31 2005
SHEE
1
OF
1



TITL	COMMPLD_U30
COMPAN	TELVENT
DESIGNE	C.Janik 5-12-05
NUMBER	C3800-002-PLDA2 REV A
DAT	Thu May 12 07:43:43 2005 SHEE 1 OF 1

43 BSA
44 BSA
1 RESET
28 PICI
18 RTUIOR
14 dat
12 busy
11 sync
17 IRIGOU
2 IRIGB IN
19 RTUIOW
33 IRQ
25 INT AL
RTUIOW
RTUIOR
BSAC
112H
113H
110H
111H
GND
7413
3:8 DECOD
PGM TSYN
BNANE
7424
OCTAL BU
7417
REGIST
Write to 112 H
RESET
Bit 3
Bit 2
Bit 1
Bit 0
7415
MULTIPLE
00h = Irig Signa
01h = GPS Signa
02h = Not Define
03h = Internal interrup
08h = Reset
IRIGB_IN
GPS_IN
INTERNA
High Pulse Clears
27 output
29 output
31 output
24 Output
36 output
34 output
16 Output
9 IRIGRST
20 IRIGC
21 IRIG A
26 INT IRI
4 D
5 D
6 D
8 D
41 D
40 D
39 D
37 D

TITL	PIC PLD U39
COMPAN	TELVENT
DESIGNE	C. Janik S - 5-12-05
NUMBER	C3800-002-PLDA3 REV A
DAT	Thu May 12 07:44:40 2005 SHEE 1 OF 1



TITL	STATUS U50
COMPAN	TELVENT
DESIGNE	C. Janik 5-12-05
NUMBER	C3800-002-PLDA4
REV	A
DAT	Thu May 12 07:45:35 2005
SHEE	1 OF 1

plda5@64 D0 BIDIR D0
plda5@4 D1 BIDIR D1
plda5@43 D2 BIDIR D2
plda5@6 D3 BIDIR D3

plda5@44 D4 BIDIR D4
plda5@51 D5 BIDIR D5
plda5@3 D6 BIDIR D6
plda5@2 D7 BIDIR D7

plda5@8 RDn INPUT RDn
plda5@76 WRn INPUT WRn
plda5@81 CSn INPUT CSn

plda5@41 BA0 INPUT BA0
plda5@9 BA1 INPUT BA1
plda5@42 BA2 INPUT BA2

plda5@54 RESETn INPUT RESETn

VCC

OCTAL BUF.

D7 D6 D5 D4 D3 D2 D1 D0

2Y4 2Y3 2Y2 2Y1 1Y4 1Y3 1Y2 1Y1 — 2A4 2A3 2A2 2A1 2GN 1A4 1A3 1A2 1A1 1GN

74244

Board ID is CX for the Sage 3030

SBOSEL

INPUT LOCALn

R7n

GND

mrblatch

RESETn WOn RDn rdn D7 D6 D5 D4 D3 D2 D1 D0 — Q5 Q4 Q3 Q2 Q1 Q0

OUTPUT SBO-STB plda5@40
OUTPUT SOURCE_EN plda5@82

NOT

OUTPUT EXEC3n plda5@71
OUTPUT EXEC3 plda5@39
OUTPUT EXEC2 plda5@69
OUTPUT EXEC1 plda5@83
OUTPUT EXEC0 plda5@65

R1n

OCTAL BUF.

D7 D6 D5 D4 D3 D2 D1 D0

2Y4 2Y3 2Y2 2Y1 1Y4 1Y3 1Y2 1Y1 — 2A4 2A3 2A2 2A1 2GN 1A4 1A3 1A2 1A1 1GN

74244

INPUT RB_EXEC15 plda5@45
INPUT RB_EXEC14 plda5@46
INPUT RB_EXEC13 plda5@55
INPUT RB_EXEC12 plda5@48
INPUT RB_EXEC11 plda5@49
INPUT RB_EXEC10 plda5@50
INPUT RB_EXEC9 plda5@72
INPUT RB_EXEC8 plda5@56

74138

BA0 BA1 BA2 — A B C — VCC — G1 — CSn G2AN — RDn G2BN

Y0N Y1N Y2N Y3N Y4N Y5N Y6N Y7N — ROn R1n R2n R3n R4n R5n R6n R7n — 60H 61H 62H 63H 64H 65H 66H 67H

3:8 DECODER

74138

BA0 BA1 BA2 — A B C — VCC — G1 — CSn G2AN — WRn G2BN

Y0N Y1N Y2N Y3N Y4N Y5N Y6N Y7N — WOn W1n W2n W3n W4n W5n W6n W7n — 60H 61H 62H 63H 64H 65H 66H 67H

3:8 DECODER

2MHZ IS SAME
as OLD SBO-CLK

INPUT pci0 plda5@31
INPUT pci1 plda5@30

R4n

OCTAL BUF.

D7 D6 D5 D4 D3 D2 D1 D0

2Y4 2Y3 2Y2 2Y1 1Y4 1Y3 1Y2 1Y1 — 2A4 2A3 2A2 2A1 2GN 1A4 1A3 1A2 1A1 1GN

74244

INPUT RB_EXEC7 plda5@12
INPUT RB_EXEC6 plda5@13
INPUT RB_EXEC5 plda5@84
INPUT RB_EXEC4 plda5@15
INPUT RB_EXEC3 plda5@16
INPUT RB_EXEC2 plda5@22
INPUT RB_EXEC1 plda5@18
INPUT RB_EXEC0 plda5@19

R5n

OCTAL BUF.

D7 D6 D5 D4 D3 D2 D1 D0

2Y4 2Y3 2Y2 2Y1 1Y4 1Y3 1Y2 1Y1 — 2A4 2A3 2A2 2A1 2GN 1A4 1A3 1A2 1A1 1GN

74244

INPUT RB_SEL7 plda5@20
INPUT RB_SEL6 plda5@23
INPUT RB_SEL5 plda5@24
INPUT RB_SEL4 plda5@25
INPUT RB_SEL3 plda5@21
INPUT RB_SEL2 plda5@27
INPUT RB_SEL1 plda5@28
INPUT RB_SEL0 plda5@29

R6n

OCTAL BUF.

D7 D6 D5 D4 D3 D2 D1 D0

2Y4 2Y3 2Y2 2Y1 1Y4 1Y3 1Y2 1Y1 — 2A4 2A3 2A2 2A1 2GN 1A4 1A3 1A2 1A1 1GN

74244

INPUT RB_SEL15 plda5@66
INPUT RB_SEL14 plda5@63
INPUT RB_SEL13 plda5@62
INPUT RB_SEL12 plda5@61
INPUT RB_SEL11 plda5@60
INPUT RB_SEL10 plda5@37
INPUT RB_SEL9 plda5@58
INPUT RB_SEL8 plda5@57

sout

CLK-SBO — SBOCLK — RESETn — D[7..0] — WD[7..0] — W7n — W6n — W5n — W4n

SERDAT SBOSEL — OR2 — NOT

OUTPUT SERDAT
OUTPUT SD-CLK
SBOSEL

plda5@35 147456Mhz INPUT

73728Mhz — 36864Mhz — 18432Mhz 2MHZ — 921Hz

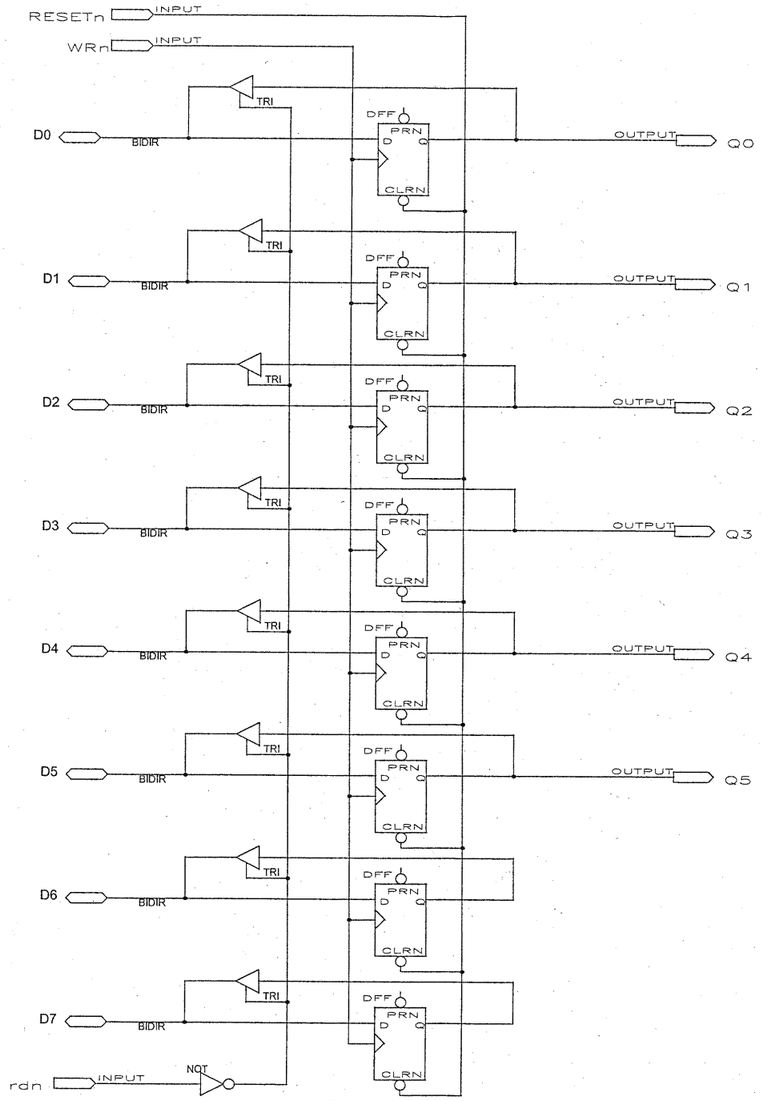
DFF PRN D Q CLRN NOT

RESETn

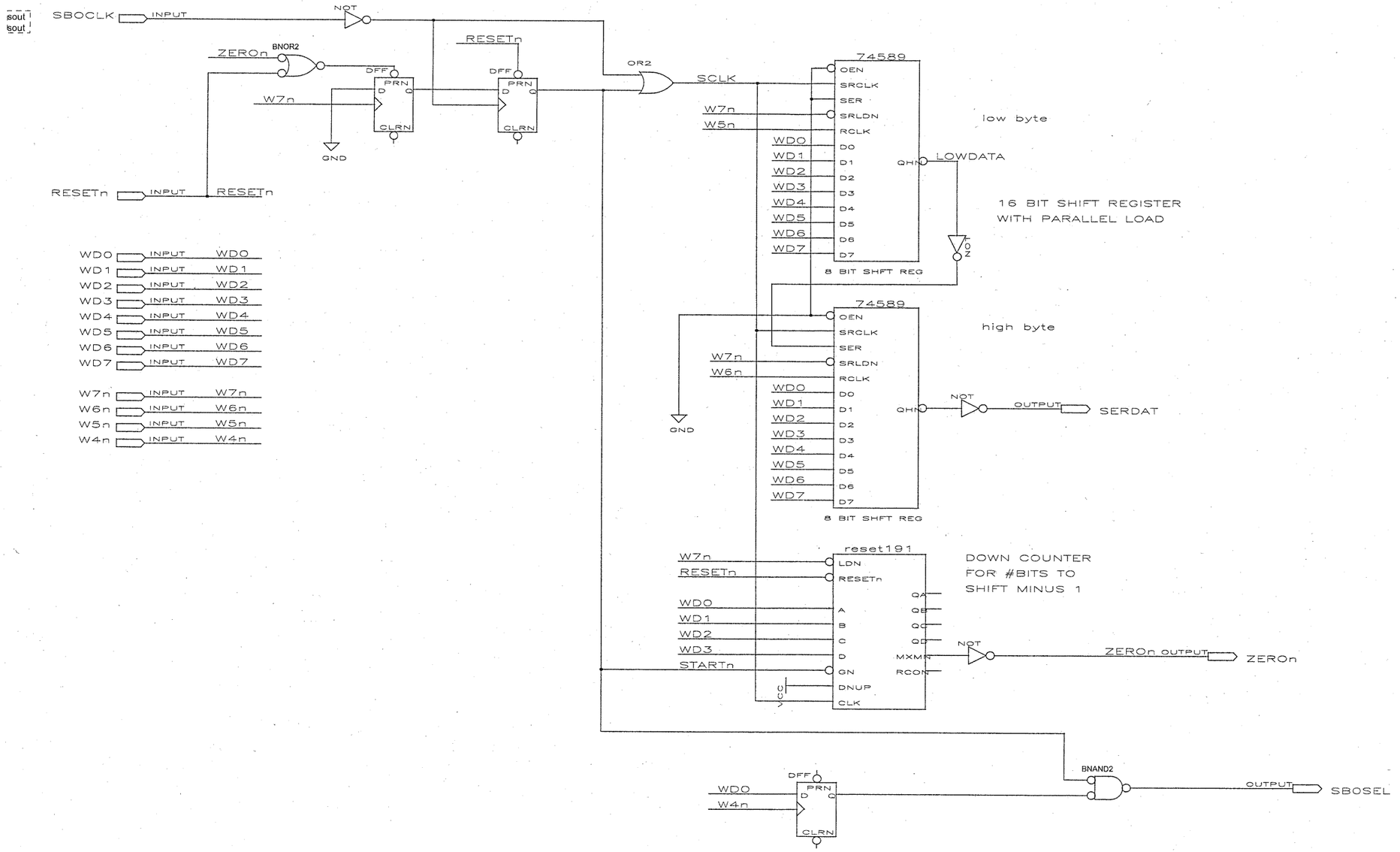
CLK-SBO

1/2MHZ
460Mhz

TITLE	SBOPLD
COMPANY	TELVENT
DESIGNER	C. Janik 5-12-05
SIZE	D
NUMBER	C3800-002-PLDA5
REV	A
DATE	8:49a 5-09-2005
SHEET	1 OF 3



TITLE	SBOPLD-MRBLATCH		
COMPANY	TELVENT		
DESIGNER	C.Janik		5-17-05
SIZE D	NUMBER C3800-002-PLDA5	REV	A
DATE 8:14a 5-09-2005	SHEET 2	OF	3



TITLE	SBOPLD-SOUT		
COMPANY	TELVENT		
DESIGNER	C. Janik		5-12-05
SIZE	D	NUMBER C3800-002-PLDA5	REV A
DATE	8:15a 5-09-2005	SHEET 3	OF 3

DATA BUS

RESISTOR WILL HOLD BOARD IN RESET IN THE ABSENSE OF A CPU BOARD

+5V
R1 6.81K
R2 6.81K
U1:F HCT14
RTU-RESET#
DGND

P1 ROW-A: A1 IOCHCK, A2 SD7, A3 SD6, A4 SD5, A5 SD4, A6 SD3, A7 SD2, A8 SD1, A9 SD0, A10 IOCHRDY, A11 AEN, A12 SA19, A13 SA18, A14 SA17, A15 SA16, A16 SA15, A17 SA14, A18 SA13, A19 SA12, A20 SA11, A21 SA10, A22 SA9, A23 SA8, A24 SA7, A25 SA6, A26 SA5, A27 SA4, A28 SA3, A29 SA2, A30 SA1, A31 SA0, A32 GND

P1 ROW-B: B1 GND DGND, B2 RESETDRV, B3 +5V +5V, B4 IRQ9, B5 -5V, B6 DRQ2, B7 -12V, B8 ENDXFR, B9 +12V, B10 KEYB, B11 SMEMW, B12 SMEMR, B13 IOW IOW#, B14 IOR IOR#, B15 DACK3, B16 DRQ3, B17 DACK1, B18 DRQ1, B19 REFRESH, B20 SYSCLK, B21 IRQ7, B22 IRQ6, B23 IRQ5 IRQ5, B24 IRQ4, B25 IRQ3 CPU Comm, B26 DACK2, B27 TC, B28 BALE, B29 +5V, B30 OSC, B31 GND DGND, B32 GND DGND

TO PLDA1 THIS PAGE

U1:C HCT14 GPS 1MSEC Clock
To Sheets 2,4 of 5
FASTCLK

+5V
BP1 .1uF
C18 4.7uF
DGND

+5V
BP2 .1uF
C19 4.7uF
R3 6.81K
IO16#

P2: C1 GND, C2 SBHE, C3 LA23, C4 LA22, C5 LA21, C6 LA20, C7 LA19, C8 LA18, C9 LA17, C10 MEMR, C11 MEMW, C12 SD8, C13 SD9, C14 SD10, C15 SD11, C16 SD12, C17 SD13, C18 SD14, C19 SD15, C20 KEYC

P2: D1 GND DGND, D2 MEMCS16, D3 IOCS16, D4 IRQ10 IRQ10, D5 IRQ11 GPS, D6 IRQ12 IRQ12, D7 IRQ13, D8 IRQ14 IRQ14, D9 DACK0, D10 DRQ0, D11 DACK5, D12 DRQ5, D13 DACK6, D14 DRQ6, D15 DACK7, D16 DRQ7, D17 +5V +5V, D18 MASTER, D19 GND DGND, D20 GND DGND

1MSEC TP100

U1:A HCT14
IRQ5
1MSEC
To Sheet 2 of 5

PC/104 BUS CONNECTORS

+5V
BP3 .1uF, BP4 .1uF, BP5 .1uF, BP6 .1uF, BP7 .1uF, BP8 .1uF, BP9 .1uF, BP10 .1uF, BP11 .1uF, BP12 .1uF, BP13 .1uF
DGND
U34 U33 U31 U35 U59 U50 U58 U25 U25 U25 U25

+5V
R4 6.81K
R5 0.0
BRD_ADD#

U2 74AHCT245SOL
BRD_IOR#
SD7 SD6 SD5 SD4 SD3 SD2 SD1 SD0
D7 D6 D5 D4 D3 D2 D1 D0

U3 74AHCT245SOL
BRD_IOR#
SD15 SD14 SD13 SD12 SD11 SD10 SD9 SD8
D15 D14 D13 D12 D11 D10 D9 D8

U4 74AHCT245SOL
SA7 SA6 SA5 SA4 SA3 SA2 SA1 SA0
BSA7 BSA6 BSA5 BSA4 BSA3 BSA2 BSA1 BSA0

U5 74AHCT245SOL
SA15 SA14 SA13 SA12 SA11 SA10 SA9 SA8
BSA15 BSA14 BSA13 BSA12 BSA11 BSA10 BSA9 BSA8

TP110 RTU-RESET#
TP111 IOW#
TP112 IOR#
TP113 BRD_ADD#
TP114 BRD_IOR#
TP115 BRD_IOW#
TP116 IO16#

TP10 DGND
U1:D HCT14
TP11
DGND

B_DATA_BUS
D15 D14 D13 D12 D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1 D0
R6 R7 R8 R9 R10 R11 R12 R13 R14 R15 R16 R17 R18 R19 R20 R21 6.81K +5V

Data Bus
To Sheet 2,3,4

U6 74AHCT245SOL
FIM1_DI# DGND
D0 D1 D2 D3 D4 D5 D6 D7
DI-D0 DI-D1 DI-D2 DI-D3 DI-D4 DI-D5 DI-D6 DI-D7

U7 74AHCT245SOL
DGND +5V
LS-A0 LS-A1 SBSEL1 SBSEL2 SBSEL3 SBSEL4 SBSEL5 SBSEL6
B-LS-A0 B-LS-A1 B-SBSEL1 B-SBSEL2 B-SBSEL3 B-SBSEL4 B-SBSEL5 B-SBSEL6

U8 74AHCT245SOL
DGND +5V
SBSEL7 SBSEL8
B-SBSEL7 B-SBSEL8

RN11 SIP8BK010-SMT 10K
+5V
DI-D0 DI-D1 DI-D2 DI-D3 DI-D4 DI-D5 DI-D6 DI-D7

J5:A Status Bus Expansion FIM #1
DI-D0 DI-D1 DI-D2 DI-D3 DI-D4 DI-D5 DI-D6 DI-D7
B-LS-A0 B-LS-A1 B-SBSEL1 B-SBSEL2 B-SBSEL3 B-SBSEL4 B-SBSEL5 B-SBSEL6 B-SBSEL7 B-SBSEL8
+5V DGND

DI_BRD_SELECT
To Sheet 2 of 5

RTU-RESET# IOW# AEN IOR# +5V DGND BRD_ADD#
To Sheet 2 of 5 FIM1_DI#
To Sheet 4 of 5 SBO#
IO16#
BRD_IOR# BRD_IOW#
To Sheet 4 of 5

PLDX1 U9 EPM7064SPLCC44 I/O EPLD
TDI TDO PLDX2 AI1_RD# AI2_RD# AI_WR# A/D_SEL TCK DGND SBO-OUT
BSA0 BSA1 BSA2 BSA3 BSA4 BSA5 BSA6 +5V
BSA7 BSA8 BSA9 BSA10 BSA11 BSA12 BSA13 BSA14 BSA15
To Sheet 2 of 5

B_ADDRESS_BUS
To Sheet 2, 4 of 5

08:10:08
Wed Sep 08, 2010

REV	ECO#	DATE	BY	CHK	DESCRIPTION
B	11876	11AUG10	CGJ	CGJ	First Production release
A	N/A	04MAY10	CGJ	CGJ	Prototype Release

TELVENT

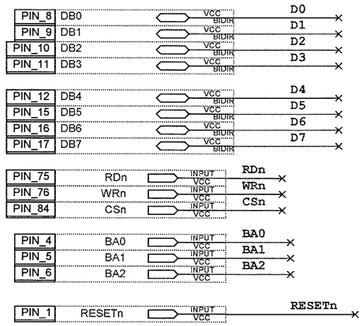
APPROVALS	DATE
DWN Chris Janik	10MAR10
CHK CGJ	05/04/2010
APP CGJ	05/04/2010

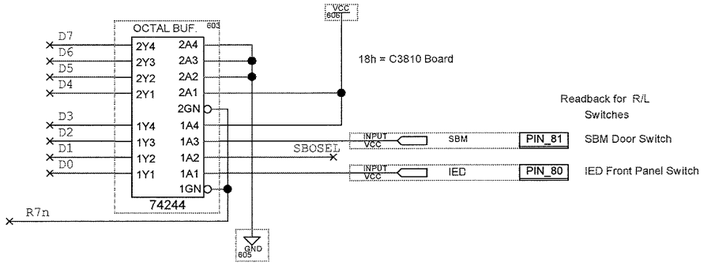
MPL SCH SAP I/O EXPANSION BD

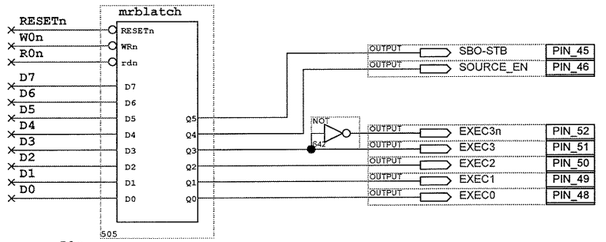
SUBSTATION AUTOMATION I/O EXPANSION BOARD

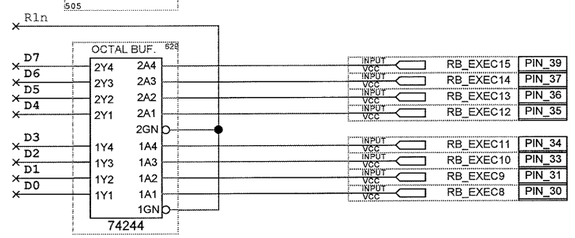
PART # C3810-002-REV-B

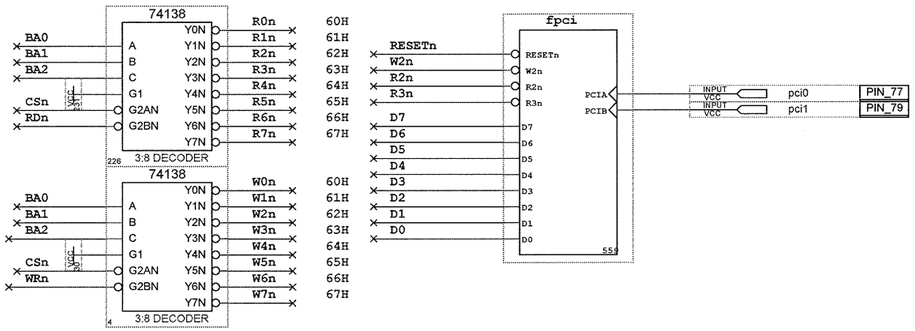
SIZE B | PC/104 | SHEET 1 OF 5

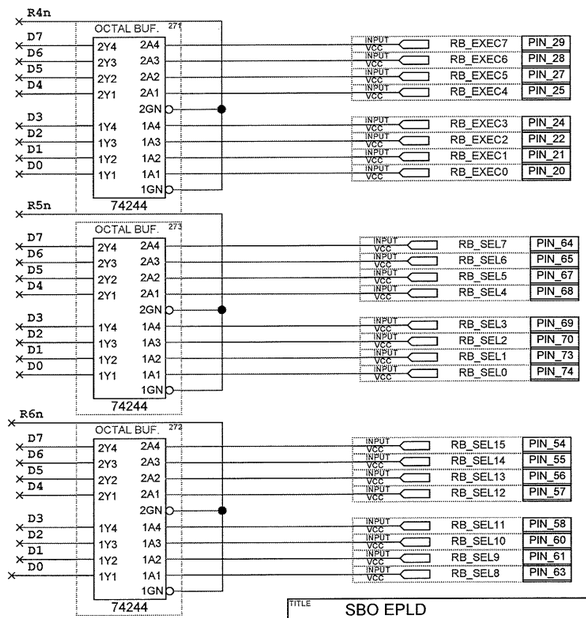


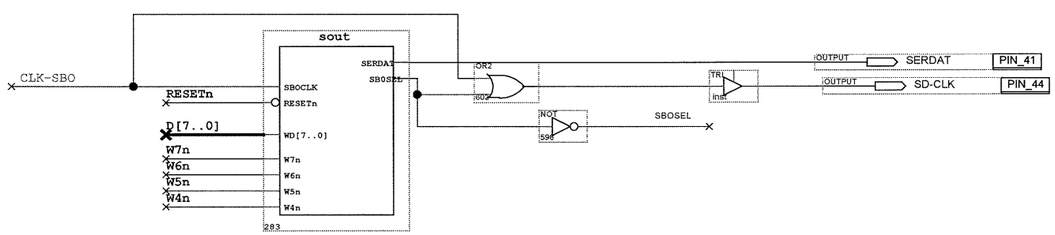


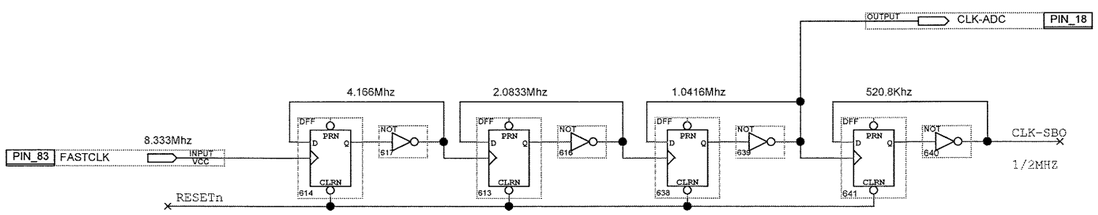




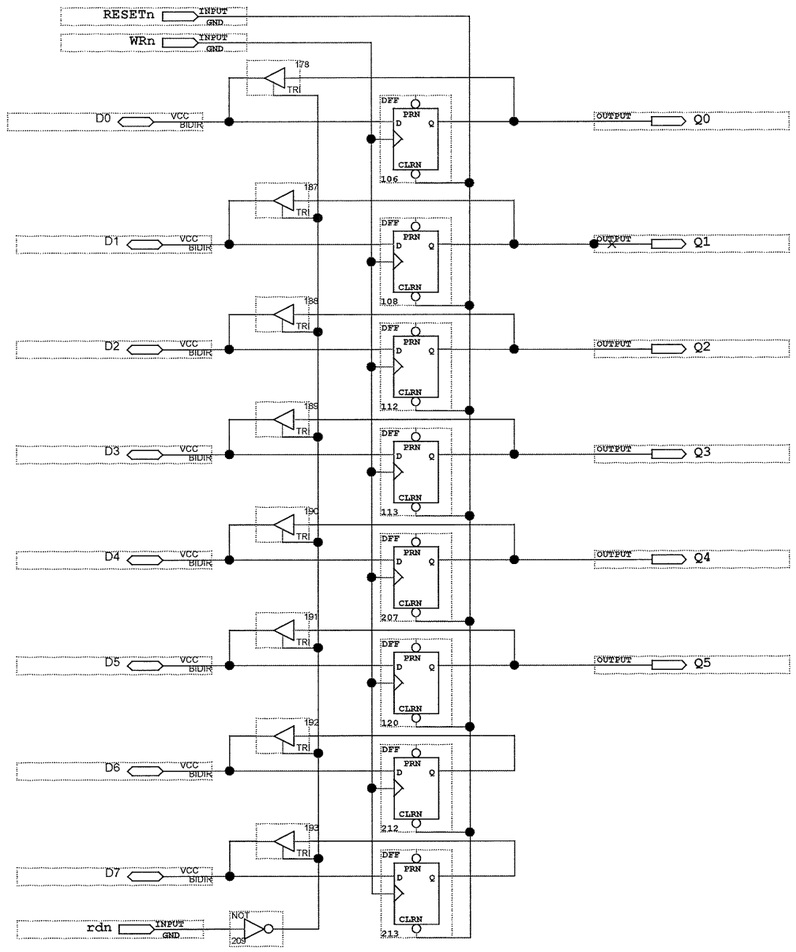




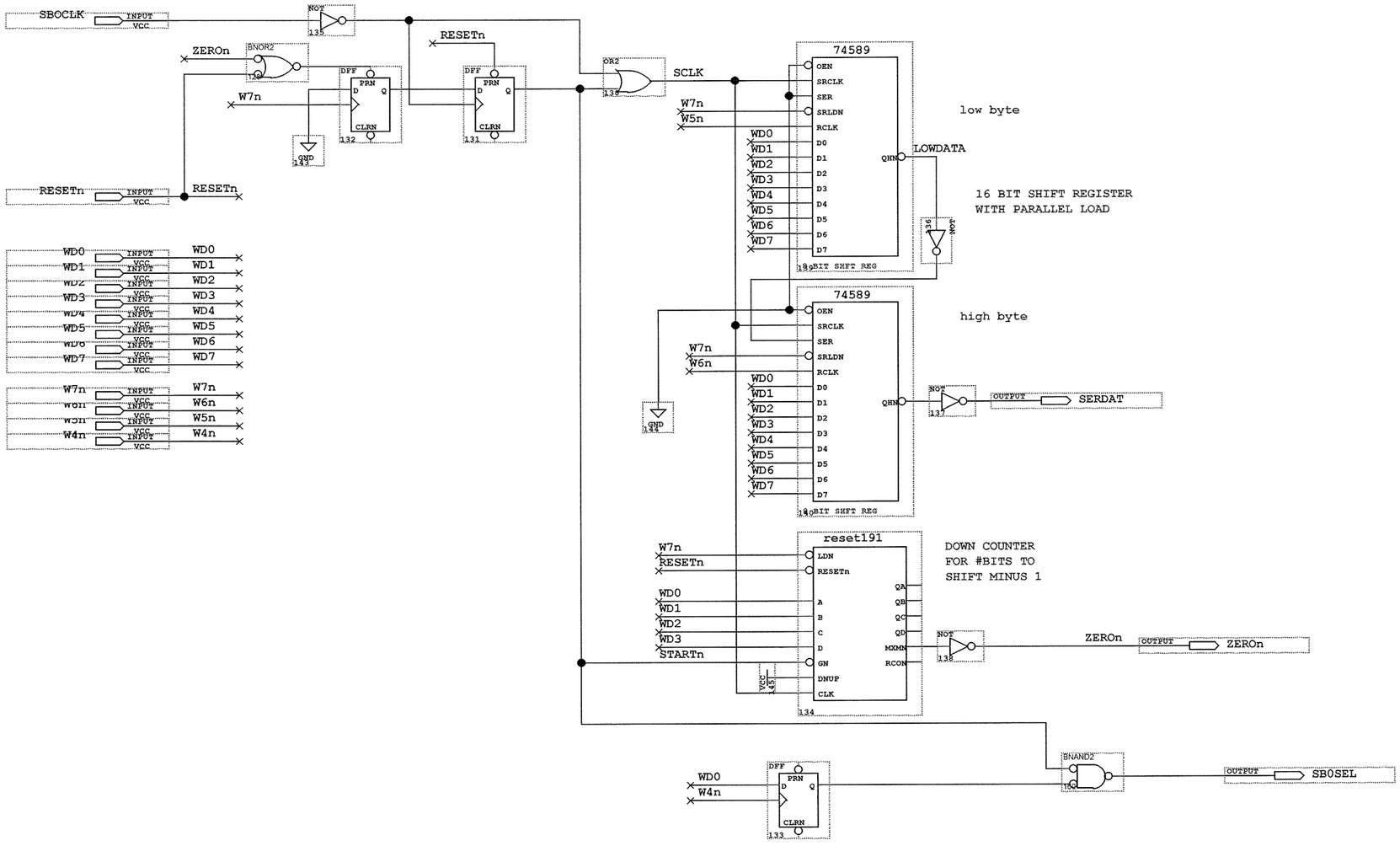




TITLE	SBO EPLD
COMPANY	TELVENT
DESIGNER	K.T. / Chris Janik 11/30/10
SIZE B / NUMBER C3810-002-PLDA3 / REV A	
DATE Thu Jul 15 07:53:56 2010 / SHEET 1 OF 3	



TITLE	IOPLD-MRBLATCH
COMPANY	Valmet Automation
DESIGNER	Keith Tooker 11/30/10
SIZE D / NUMBER C3200-002-PLDA2 / REV A	
DATE Thu Jul 15 07:52:17 2010	SHEET 2 OF 3



TITLE	IOPLD-SOUT
COMPANY	Valmet Automation
DESIGNER	Keith Tooker 11/20/10
SIZE D / NUMBER	C3400-002-PLDA2 / REV A
DATE	Thu Aug 05 10:33:00 2010 / SHEET 3 OF 3

To Sheets 1 & 4 of 5

U10
AI2_RD# DGND CE- VCC DIR GND 1=A>B +5V DGND
D15 D14 D13 D12 D11 D10 D9 D8 → A0 A1 A2 A3 A4 A5 A6 A7
B0 B1 B2 B3 B4 B5 B6 B7 → AD11 AD10 AD9 AD8
74AHCT245SOL

U11
AI2_RD# DGND CE- VCC DIR GND 1=A>B +5V DGND
D7 D6 D5 D4 D3 D2 D1 D0 → A0 A1 A2 A3 A4 A5 A6 A7
B0 B1 B2 B3 B4 B5 B6 B7 → AD7 AD6 AD5 AD4 AD3 AD2 AD1 AD0
74AHCT245SOL

U12
AI1_RD# DGND CE- VCC DIR GND 1=A>B +5V DGND
D15 D14 D13 D12 D11 D10 D9 D8 → A0 A1 A2 A3 A4 A5 A6 A7
B0 B1 B2 B3 B4 B5 B6 B7 → AD1_11 AD1_10 AD1_9 AD1_8
74AHCT245SOL

U13
AI1_RD# DGND CE- VCC DIR GND 1=A>B +5V DGND
D7 D6 D5 D4 D3 D2 D1 D0 → A0 A1 A2 A3 A4 A5 A6 A7
B0 B1 B2 B3 B4 B5 B6 B7 → AD1_7 AD1_6 AD1_5 AD1_4 AD1_3 AD1_2 AD1_1 AD1_0
74AHCT245SOL

U14 AD7870
CONVERT# BUSY_1# F-5V DGND F+5V
CLK INT RD NC1 CS CONVST CTRL
AD1_11 AD1_10 AD1_9 AD1_8 AD1_7 AD1_6 → D11 D10 D9 NC8 D8 D7 D6
VSS VIN REFOUT NC22 AGND VDD D0 → F-5V AGND F+5V
D5 D4 DGND NC15 D3 D2 D1 → AD1_5 AD1_4 DGND AD1_3 AD1_2 AD1_1 AD1_0

U15 AD7870
CONVERT# BUSY_2# F-5V DGND F+5V
CLK INT RD NC1 CS CONVST CTRL
AD11 AD10 AD9 AD8 AD7 AD6 → D11 D10 D9 NC8 D8 D7 D6
VSS VIN REFOUT NC22 AGND VDD D0 → F-5V AGND F+5V
D5 D4 DGND NC15 D3 D2 D1 → AD5 AD4 DGND AD3 AD2 AD1
AD0

U16 PLDX2 EPM7128SLC84-10
D4 +5V PLDX2 D3 D2 D1 D0 DGND SBSEL1 SBSEL2 SBSEL3 TMS SBSEL4 SBSEL5 +5V SBSEL6 SBSEL7 SBSEL8 LS-A0 LS-A1 DGND
I/O12 VCC TDI I/O15 I/O16 I/O17 I/O18 DGND I/O20 I/O21 I/O22 TMS I/O24 I/O25 VCC I/O27 I/O28 I/O29 I/O30 I/O31 DGND
I/O11 I/O10 I/O9 I/O8 DGND I/O6 I/O5 I/O4 VCC IN/OE2/GLCK2 IN/GLCRn IN/OE1 IN/GCLK1 DGND I/O81 I/O80 I/O79 Vcc I/O77 I/O76 I/O75
I/O74 I/O73 DGND TDO I/O70 I/O69 I/O68 I/O67 Vcc I/O65 I/O64 I/O63 TCK I/O61 I/O60 DGND I/O58 I/O57 I/O56 I/O55 I/O54
I/O33 I/O34 I/O35 I/O36 I/O37 Vcc I/O39 I/O40 I/O41 DGND Vcc I/O44 I/O45 I/O46 DGND I/O48 I/O49 I/O50 I/O51 I/O52 Vcc
FIM1 DI# BSA0 BSA1 BSA2 BSA3 +5V BSA4 DGND +5V ABDSEL0 ABDSEL1 ABDSEL2 DGND ABDSEL3 ABDSEL4 ABDSEL5 ABDSEL6 ABDSEL7 +5V
D5 D6 D7 D8 DGND AI_WR# +5V RTU-RESET# FASTCLK DGND 1MSEC +5V
BUSY_2# BUSY_1# CONVERT# DGND PLDX3 CH_SEL REF_SEL A-A3 A-A2 +5V A-A1 A-A0 ABDSEL15 TCK ABDSEL14 ABDSEL13 DGND ABDSEL12 ABDSEL11 ABDSEL10 ABDSEL9 ABDSEL8
A/D1_INPUT A/D2_INPUT

DI_BRD_SELECT
To Sheet 1 of 5
B_ADDRESS_BUS
SBO-OUT
From U29.9 Sheet 1 of 5
SBO-OE#
To U34.7 U35 .7 Sheet 4 of 5
AD_SELECT_BUS
From Sheet 3 of 5

U17:A OP282 F+15V F-15V
TP102
U18 AD620
F+15V IN+ RG1 RG2 IN- V+ V- OUT TRIM AGND F-15V
R26 10K
R28 0.0
TP101 A/D1_INPUT
100K R22 CW R23 10K
R29 10.0M
10K R27
AGND

AV = 1 + (49.4K/Rgain)

$$AV = \frac{49.4\text{Kohms}}{\text{R Gain}} + 1$$

$$Rgain = \frac{49.4\text{Kohms}}{AV-1}$$

TP12 R34 0.0 DGND AGND
Place Between U14 and U15
Connect Pin 21 and Pin 14

U17:B OP282
TP104
U19 AD620
R30 10K
R32 0.0
TP103 A/D2_INPUT
100K R25 CW R24 10K
R33 10.0M
10K R31
AGND

U1 Decoupling Caps
+5V DGND
BP14 .1uF BP15 .1uF BP16 .1uF BP17 .1uF BP18 .1uF BP19 .1uF BP20 .1uF BP21 .1uF

U14 U4 U5
F+15V AGND F-15V
BP28 .1uF BP29 .1uF BP30 .1uF BP31 .1uF BP32 .1uF BP33 .1uF

F+5V
BP22 .1uF BP23 .1uF BP24 .1uF BP25 .1uF BP26 .1uF BP27 .1uF BP57 .1uF BP58 .1uF
U12 U13 U7 U9 F-5V U18 U19

TP105 AI1_RD# TP106 AI2_RD# TP107 AI_WR# TP108 A/D_SEL TP109 CONVERT# TP117 CH_SEL TP118 REF_SEL TP9 AGND

8 SEPT 10

08:10:09
Wed Sep 08, 2010

PART #	C3810-002-REV-B				
SIZE	B	ANALOG	SHEET	2	OF 5

CH_SEL 00 = FIM1,3
01 = FIM2,4
10 = REFRENCES
REF_SEL 11 = AGND, Both Channels

U20 HI-509
A/D1_INPUT, A/D2_INPUT, REF_SEL, CH_SEL, +5V, F+15V, AGND, F-15V
OUTA, OUTB, A1, A0, ENABLE, V+, GND, V-
IN1A, IN1B, IN2A, IN2B, IN3A, IN3B, IN4A, IN4B
F1_XTH, F2_XTH, F3_XTH, F4_XTH, REF_OUTH, AGND

U21 HI1-508
A-A0, A-A1, A-A2, REF_SEL
A0, A1, A2, ENA
REF_OUTH, F+15V, F-15V, AGND
OUT, VDD, VEE, GND
IN1 +FS_REF
IN2 +90%_REF
IN3 -90%_REF
IN4 TEMP
IN5, IN6, IN7, IN8 AGND
10M R71, .1uF BP64
TP16 TP17 + AUX INPUT -

U23:A OP282 F+15V F-15V
TP13 +FS 1.999V
TP14 +90% 1.800V
TP15 -90% -1.800V
R72 250 AGND
R70 1K + FS ADJ
R75 10.0M, BP48 .1uF
R73 250 2.5V_REF
BP62 .1uF, R76 10.0M + 90% ADJ., R37 1K
BP63 .1uF, R77 10.0M -90% ADJ, R38 1K
R74 250

U23:B OP282 AGND
R35 10.2K, R36 10.2K

U24 LT1019 2.5Vref
F+15V, AGND
VIN, REF, TEMP, TRIM, GND, NC1, NC7, NC8

U25 74AHCT245SOL
+5V, DGND, VCC, CE-, GND, DIR 1=A>B
A-A3..A-A0 F3-A3..F3-A0
J3:A
F3_XTH, F3-A0..F3-A3, F3_BDSEL0..F3_BDSEL7
A/D #1 ANALOG IN BUS FIM 3 ANALOG INPUT

U26 74AHCT245SOL
ABDSEL15..ABDSEL8 F3_BDSEL7..F3_BDSEL0

U27 74AHCT245SOL
A-A3..A-A0 F4-A3..F4-A0
J4:A
F4_XTH, F4-A0..F4-A3, F4_BDSEL0..F4_BDSEL7
A/D#2 ANALOG IN BUS FIM 4 ANALOG INPUT

U28 74AHCT245SOL
ABDSEL15..ABDSEL8 F4_BDSEL7..F4_BDSEL0

U29 74AHCT245SOL
A-A3..A-A0 F1-A3..F1-A0
J1:A
F1_XTH, F1-A0..F1-A3, F1_BDSEL0..F1_BDSEL7
A/D#1 ANALOG IN BUS FIM 1 ANALOG INPUT

U30 74AHCT245SOL
ABDSEL7..ABDSEL0 F1_BDSEL7..F1_BDSEL0

U31 74AHCT245SOL
A-A3..A-A0 F2-A3..F2-A0
J2:A
F2_XTH, F2-A0..F2-A3, F2_BDSEL0..F2_BDSEL7
A/D #2 ANALOG IN BUS FIM 2 ANALOG INPUT

U32 74AHCT245SOL
ABDSEL7..ABDSEL0 F2_BDSEL7..F2_BDSEL0

U38 U39 U40 U41 U42 U43 U44 U45
BP34..BP41 .1uF
+5V, DGND, +5V

U8 U6 U11
BP42..BP47 .1uF
F+15V, AGND, F-15V

AD_SELECT_BUS

To Sheet 2 of 5

08:10:09
Wed Sep 08, 2010

PART #	C3810-002-REV-B				
SIZE	B	ANALOG INPUT	SHEET	3	OF 5

TO/FROM SHEET 1

B ADDRESS BUS

B DATA BUS

U33

EPM7128SLC84-10

PLDX3

RB_SEL0 RB_SEL1 RB_SEL2 RB_SEL3 RB_SEL4 RB_SEL5 RB_SEL6 RB_SEL7

RN7 100K

RN6 22K SIP8BK223-SMT

CSEL0 CSEL1 CSEL2 CSEL3 CSEL4 CSEL5 CSEL6 CSEL7

R61 R62 R63 R64 R65 R66 R67 R68 10K

EXE-PWR FROM SHEET5

RB_SEL8 RB_SEL9 RB_SEL10 RB_SEL11 RB_SEL12 RB_SEL13 RB_SEL14 RB_SEL15

RN3 100K

RN2 SIP8BK223-SMT 22K

CSEL8 CSEL9 CSEL10 CSEL11 CSEL12 CSEL13 CSEL14 CSEL15

R53 R54 R55 R56 R57 R58 R59 R60 10K

+5V R78 1.5K

0.0056uF C21 DGND

SERDAT SD-CLK SBO-STB

FROM SHEET 1 U9

SBO-OE#

U34 U35 UCN5821LW

SBO SINK DRIVERS

CONTROL_SELECT_BUS

J7:A J8:A

SBO BUS FIM #1 SBO BUS FIM#2

CONTROL_EXECUTE_BUS

EXEC10 EXEC11 EXEC12 EXEC13 EXEC14 EXEC15 SERDAT SD-CLK SBO-STB SB-SE EXEC0 EXEC1 EXEC2 EXEC3 EXEC3#

SBO SOURCE DRIVERS

U38 U39 74HCT238SOL

U36 U37 UDN2982SLW

EXE-PWR From Sheet 5

R39 6.81K

RN4 SIP8BK010-SMT 10K

RN10 SIP8BK010-SMT 10K

SBO EXECUTE MATRIX READ BACK REGISTERS

RN9 RN8 RN1 RN5 100K 22K SIP8BK223-SMT

BP49 BP50 BP51 BP52 BP53 BP54 BP55 BP56 .1uF

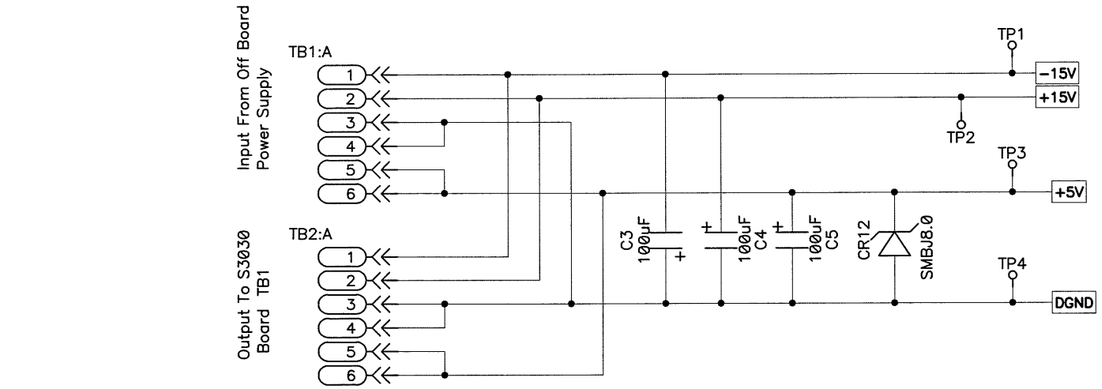
U2 U51 U54 U57 U62

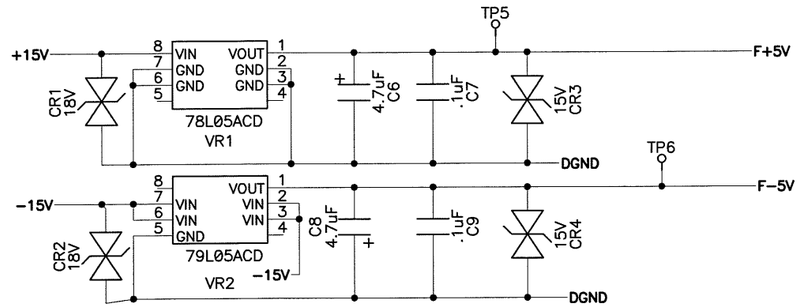
8SEP10

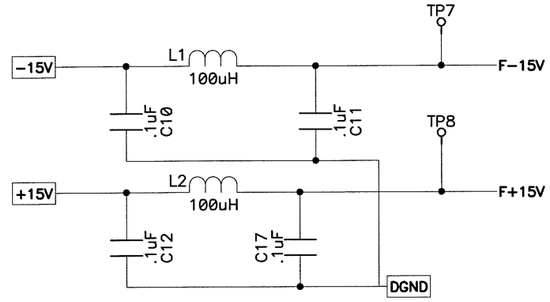
08:10:10

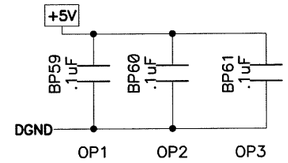
Wed Sep 08, 2010

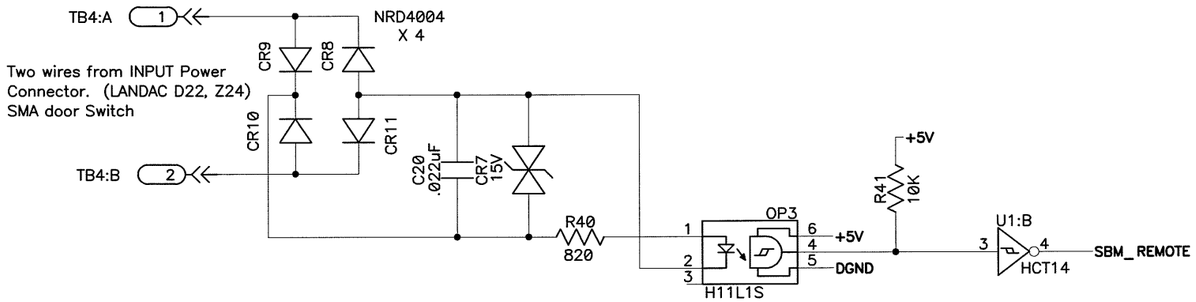
PART #	C3810-002-REV-B		
SIZE	B	SBO	SHEET 4 OF 5

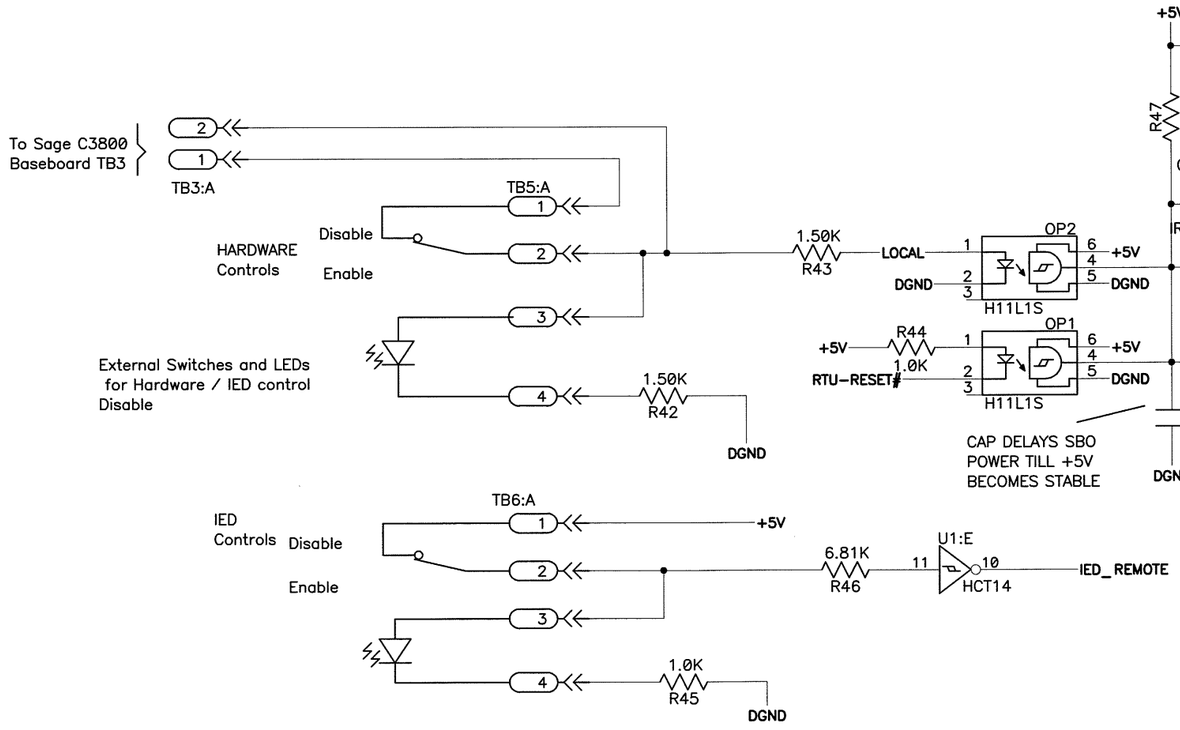


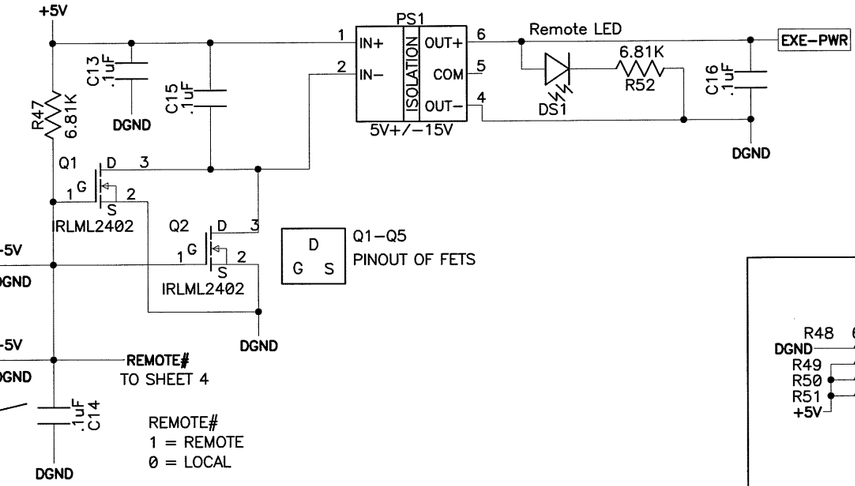


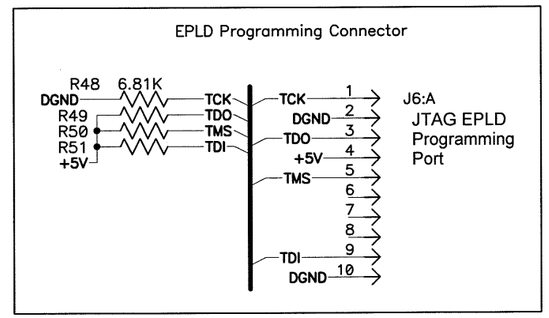










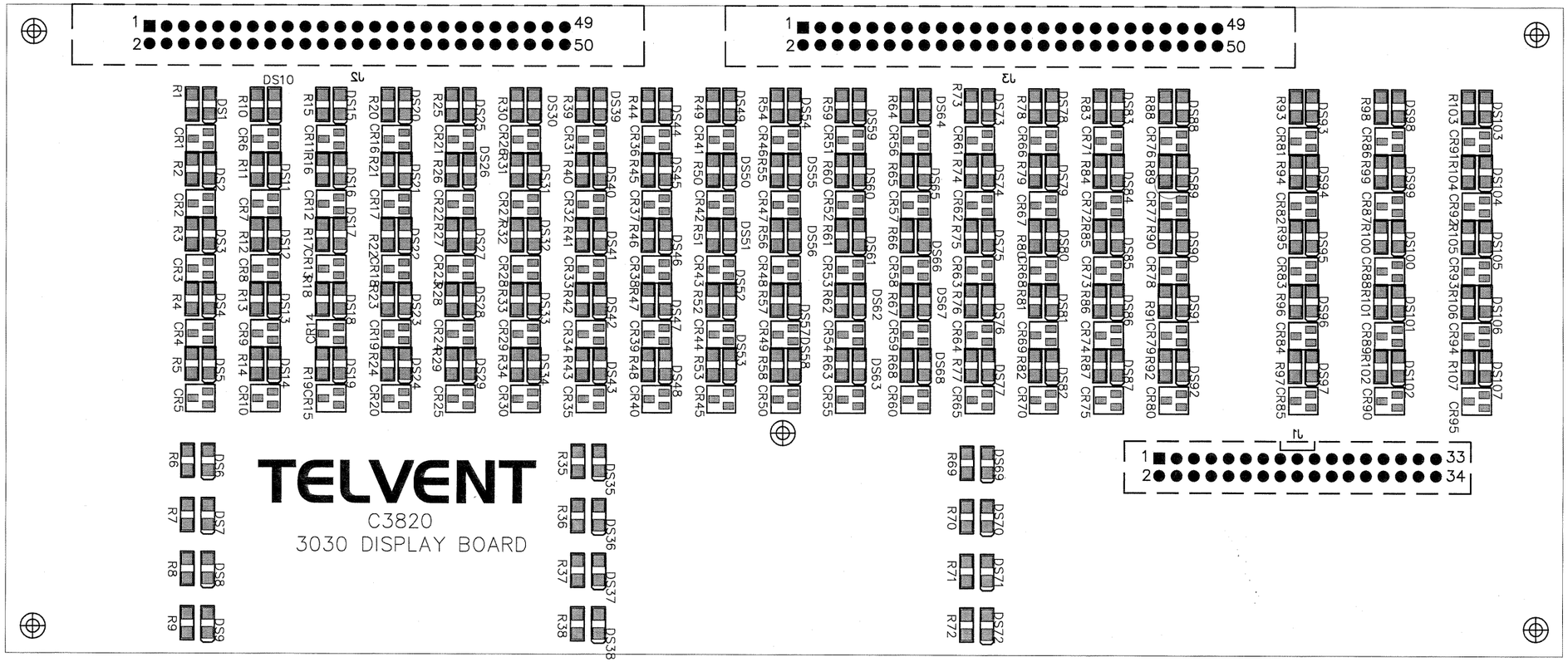


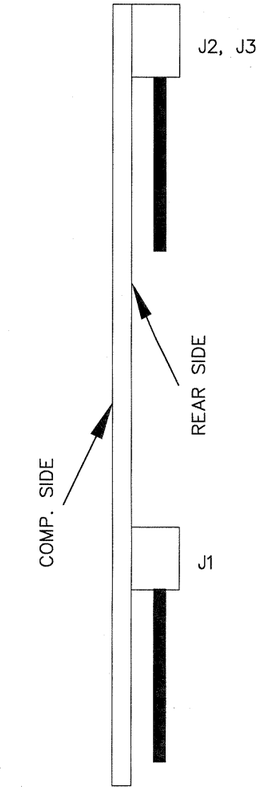
08:10:10
8SEP10 Wed Sep 08, 2010

PART #	C3810-002-REV-B				
SIZE	B	R/L CONTROL	SHEET	5	OF 5

NOTES :
1. CAUTION! CMOS DEVICE INSTALLED – HANDLE AT GROUNDED WORK STATION.
2. J1, J2, & J3 ARE SOLDER TO REAR SIDE OF THE BOARD, WITH CBL POSITION DOWN AS SHOWN.

QTY	ITEM	PART NUMBER	DESCRIPTION	NOTES
1	1	C3820-001-REV-A	PCB S3030 DISPLAY BOARD	
0	2	C3820-002-REV-A	SCH S3030 DISPLAY BOARD	
0	3	C3820-003-REV-A	TEST PROCEDURE C3820 LED DISPLAY BD	
107	4	B0000-871-S0001	LED RED SMT 1.6V T-3/4	DS1-DS107
107	5	B0000-821-C6811	RES SMT MF 01.00P .12W K06.81	R1-R107
95	6	B0001-840-S0914	DIODE MMBD914LT1 SIGNAL 1A SMT	CR1-CR95
	7			
2	8	C3800-CB2-50100	CBL ASSY FLAT FM/TRN 50P 1F001	J2, J3
1	9	C3800-CB2-34006	CBL ASSY FLAT FM/TRN 34P 0F061	J1
	10			
	11			
	12			





SYM.	ECO NO.	DATE	BY	CHK	DESCRIPTION
B	11842	1-7-10	P.P		ADDED ITEM #3 TEST PROCEDURE C3820
A	11582	2-24-06	P.P	CJ	R93, R94, R95, R96 WAS MISSING

REVISIONS

ACAD P/N: C3820-000-00001

MPL PCA S3030 DISPLAY BOARD

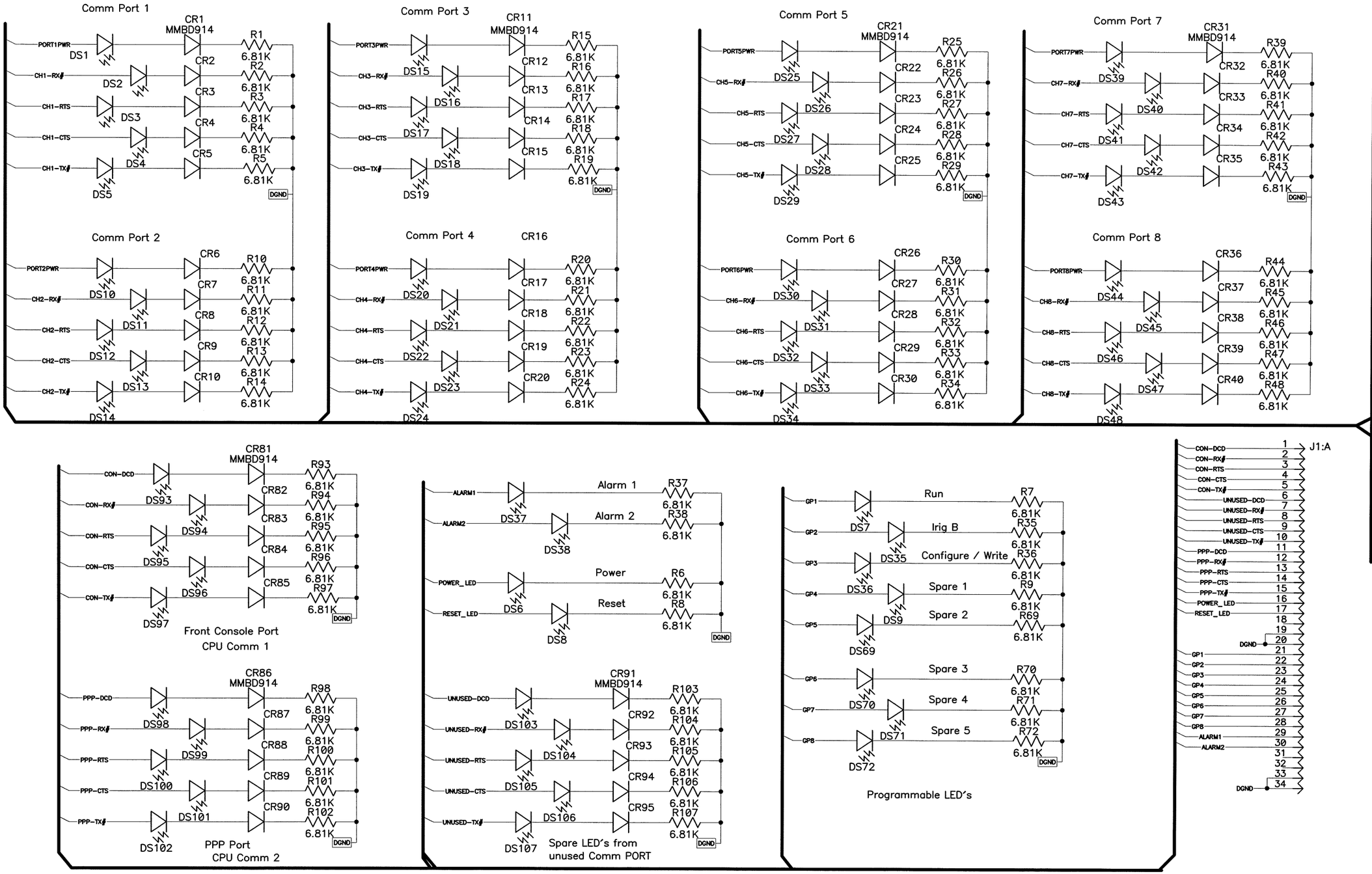
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES
DECIMALS .XX = ±.02 .XXX= ±.010
ANGLES ±.5°
MATERIAL: NONE
FINISH: NONE

TELVENT

PCA S3030 DISPLAY BOARD ASSEMBLY

APPROVALS	DATE
DWN PRAVIN	2-21-05
CHK C.JANIK	2-28-05
APP C.JANIK	2-28-05

SIZE B | C3820-000-00001 | REV B
SCALE NONE | SHEET 1 OF 1

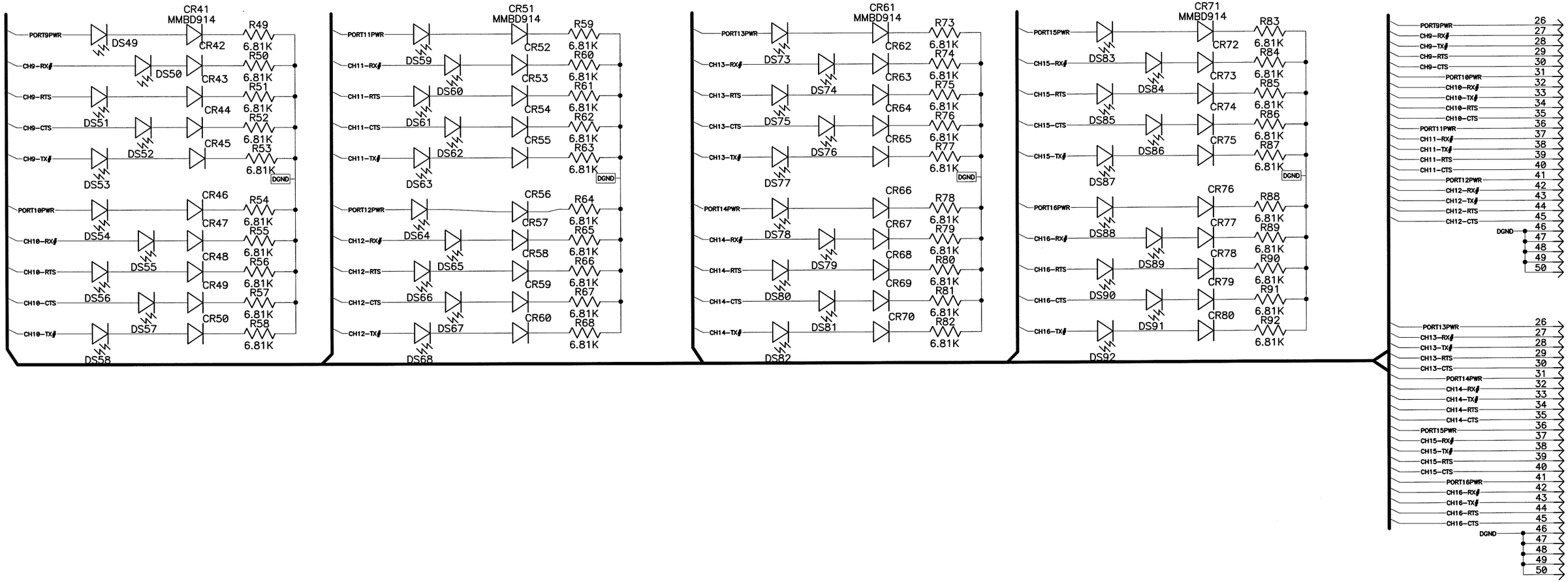


REV	ECO#	DATE	BY	CHK	DESCRIPTION
A		11/01/04			Initial Prototype Copper Release

TELVENT

APPROVALS		DATE
DWN	Chris Janik	09/03/04
CHK		11/01/04
APP		11/01/04

MPL	SCH LED DISPLAY BOARD SUB CTRL
	SCH LED DISPLAY BOARD SUBSTATION CONTROLLER
PART #	C3820-002-REV-B
SIZE	B
SHEET	1 OF 2

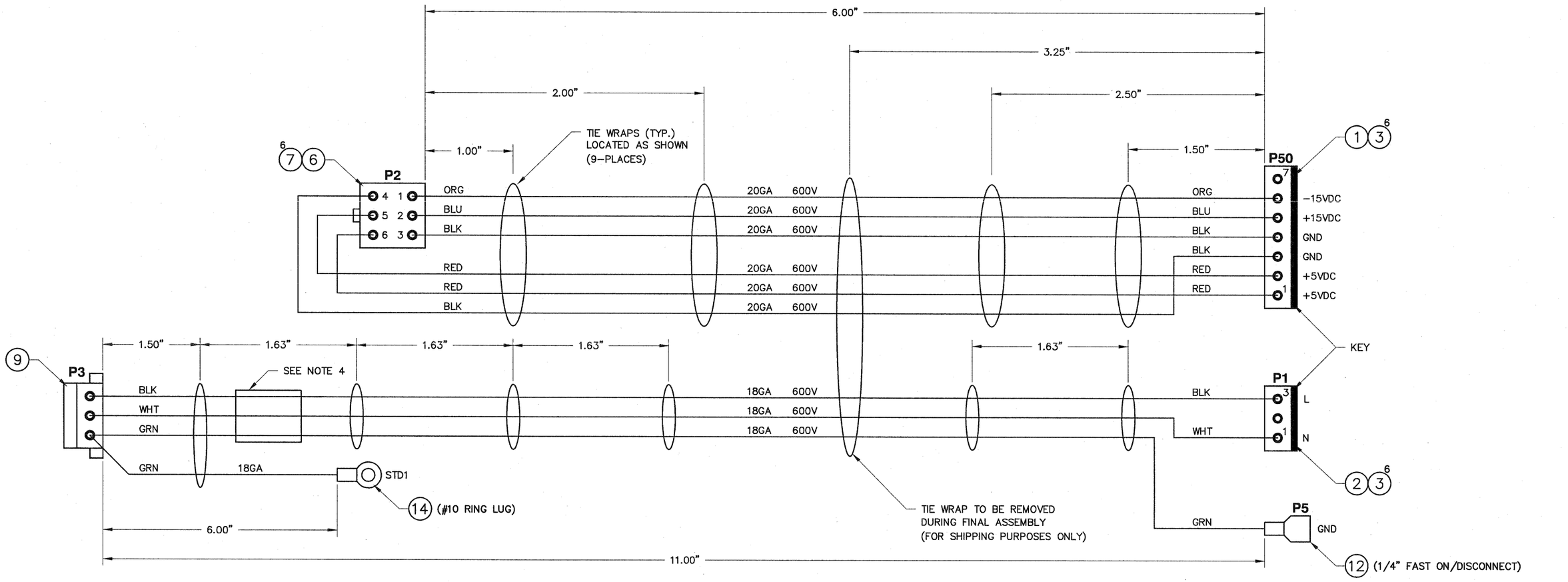


PART #	C3820-002-REV-B		
SIZE	B	11/d/04	SHEET 2 OF 2

NOTES:

1. FOR USE WITH TELVENT 3030/CONVERTER CONCEPTS POWER SUPPLY.
2. ALL CONNECTORS ARE SHOWN FROM WIRE ENTRY SIDE.
3. USE PVC WIRE GAUGE AS SPECIFIED BELOW AND CABLE TIE AS INDICATED.
4. TYPE PART NUMBER AND COMPANY NAME (TELVENT) ON VENDER SUPPLIED LABEL.

QTY	ITEM	PART NUMBER	DESCRIPTION	NOTES
1	1	B0000-724-20007	CONN FREE HNG CR 07P MLX 41695	
1	2	B0000-724-20003	CONN FREE HNG CR 03P MLX 41695	
8	3	B0000-723-00001	CONN PIN CR TIN 18-24GA WIRE	
	4			
	5			
1	6	B0002-297-30006	CONN HSG PLUG 06PIN M GOLD POL	
6	7	B0002-296-30002	CONN PIN CR GOLD 18-24 F MOLEX	
	8			
1	9	B0002-882-20003	CONN PLG MALE 03P .200 HRZ	
	10			
	11			
1	12	B0000-550-00000	LUG RCPT 22-18 .250 V .125	
	13			
1	14	B0000-592-00000	LUG RING 22-16 #10 .312 N .140	
	15			



SYM.	ECO NO.	DATE	BY	CHK	DESCRIPTION
B	11533	04-14-05	DW		ITEMS 1 & 2 WERE B0000-724-0000X
A	11531	03-28-05	DW	CJ	MANUFACTURING RELEASE MODIFICATIONS

REVISIONS

ACAD P/N: C3800-CB1-00001

MPL CBL ASSY F/3030 POWER INPUT

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES
DECIMALS
XX = ±.02
XXX= ±.010
ANGLES
±.5°
MATERIAL: NONE
FINISH: NONE

TELVENT

CABLE ASSY FOR TELVENT 3030 POWER INPUT & POWER DISTRIBUTION

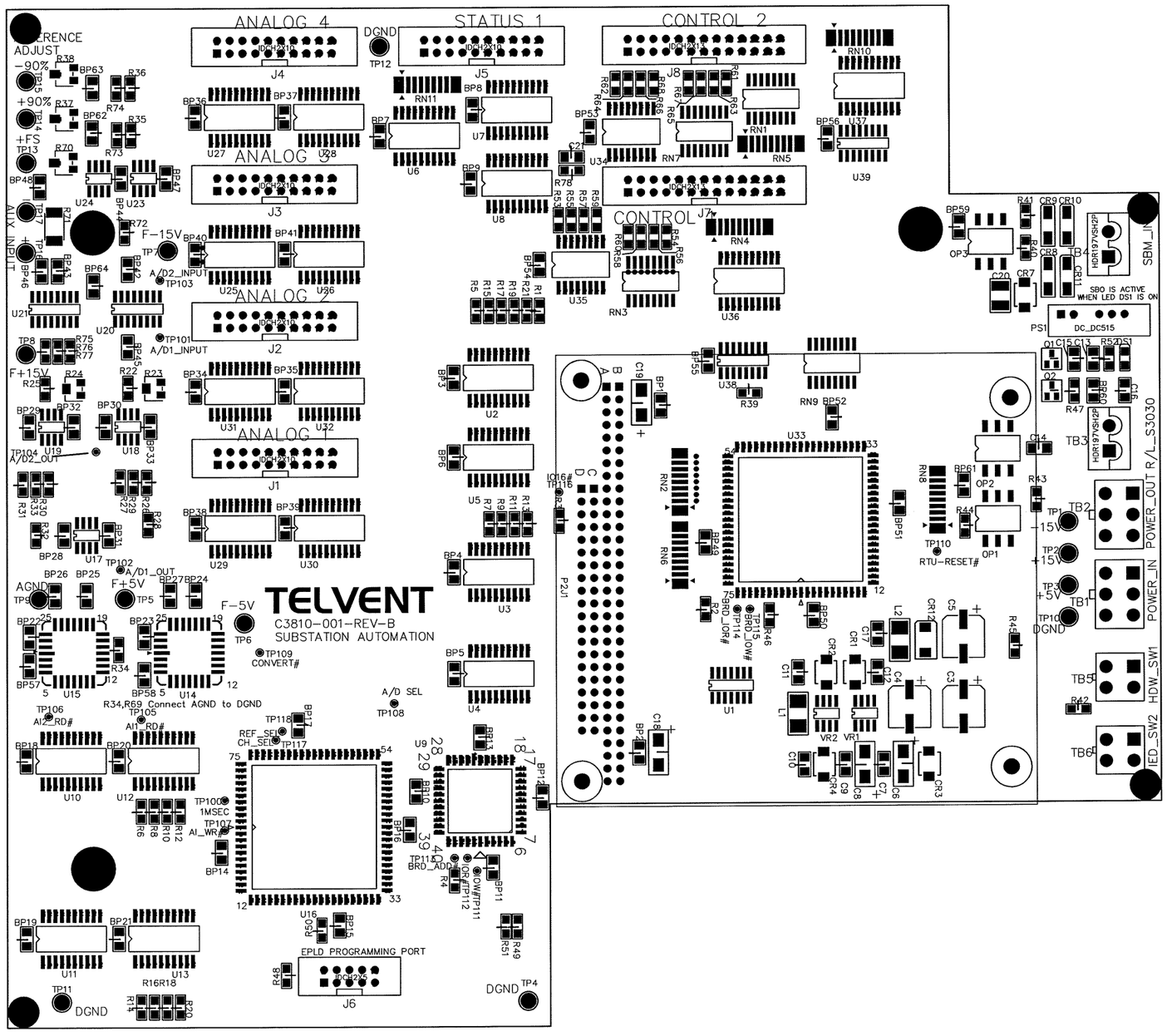
APPROVALS	DATE
DWN D.WATKINS	11-12-2004
CHK C.JANIK	02-27-2005
APP C.JANIK	02-27-2005

SIZE B | C3800-CB1-00001 | REV B

SCALE NONE | SHEET 1 OF 1

NOTES :

1. CAUTION! CMOS DEVICES INSTALLED – HANDLE AT GROUNDED WORK STATION.
2. MARK BOARD WITH ASSEMBLY PART NUMBER, REVISION LEVEL AND SERIAL NUMBER AFTER FINAL ASSEMBLY. AND BEFORE INSPECTION.



QTY	ITEM	PART NUMBER	DESCRIPTION	NOTES
1	1	C3810-001-REV-B	PCB SAP LD2 I/O EXPANSION BD	
0	2	C3810-002-REV-B	SCH SAP LD2 I/O EXPANSION BD	
0	3	C3810-003-REV-A	TEST PROCE SAP LD2 I/O EXPN BD	
	4			
19	5	B0001-849-S0245	ICD 74AHCT245 XCVR SMT	U2-U8,U10-U13,U25-U32
1	6	B0001-847-S0014	ICD 74HC14 INVERTER SCHMIT SMT	U1
2	7	B0001-848-S0238	ICD 74HCT238 3-8 DECODER SMT	U38,U39
	8			
2	9	B0002-466-S0620	ICL AD620 INSTR AMP SMT	U18,U19
2	10	B0002-467-S0003	ICH AD7870 CMOS 12B ADC PLCC	U14,U15
1	11	B0002-445-7032S	ICD EP7032S PROGRAM LOG/DEV	U9
1	12	B0002-472-S0001	ICL ADG508 8CH MUX SMT	U21
1	13	B0002-472-S0000	ICL HI-509 4CH DIFF ANA MUX SMT	U20
1	14	B0002-439-S0003	ICL LT1019 VREF PRCSN 2,5V SMT	U24
2	15	B0001-363-S0004	ICL OP282GS OPAMP DUAL SMT	U17,U23
2	16	B0001-460-S5821	ICD UNC5821LW 8BIT SRL DVR SMT	U34,U35
2	17	B0001-460-S2982	ICD A2982SLW 8CH SOURCE DVR SMT	U36,U37
2	18	B0002-445-7128S	ICD EP7128S PROGRAM LOG/DEV	U16,U33
1	19	B0001-886-S0005	ICL 78L05ACM POS V-REG SMT	VR1
1	20	B0001-885-S0005	ICL 79L05ACM NEG V-REG SMT	VR2
	21			
74	22	B0000-678-5104M	CAP-N CE 050V M0.1000 20P SMT	BP1-BP47,BP49-BP64,C7,C9-C17
1	23	B0000-697-5152J	CAP-N PPS 050V P1500.00 05P SMT	C21
1	24	B0001-694-S0000	CAP-N CE 1KV M000.022 20P SMT	C20
4	25	B0000-680-K4752	CAP-P TA 020V M004.700 10P SMT	C6,C8,C18,C19
3	26	J0000-066-M0100	CAP-P EL 050V M0100.0 20P SMT	C3,C4,C5
	27			C21 (NOT POPULATED)
1	28	B0000-871-S0001	LED RED SMT 1.6V T-3/4	DS1
	29			
4	30	J1160-016-S0000	DIODE 1N4004 RS 400V 01.00A SMT	CR8-CR11
1	31	B0001-247-S0008	DIODE SMB8.0 8.0B Z 0600W	CR12
3	32	B0001-247-S0015	DIODE SMB15C 15V Z 0600W	CR3,CR4,CR7
2	33	B0001-247-S0018	DIODE SMBJ18C 18V Z 0600W	CR1,CR2
	34			
4	35	B0000-821-C0000	RES SMT MF .12W H0.00 JMPR	R5,R28,R32,R34,
5	36	B0000-821-C1501	RES SMT MF 01.00P .12W K01.50	R42-R45,R78
21	37	B0000-821-C1002	RES SMT MF 01.00P .12W K010.00	R26,R27,R30,R31,R41,R53-R68,
2	38	B0000-821-C1003	RES SMT MF 01.00P .12W K100.00	R22,R25
1	39	B0000-821-B1005	RES SMT MF 05.00P 1W M010.00	R71
2	40	B0000-821-E1022	RES SMT MF 01.00P .12W K10.2	R35,R36
28	41	B0000-821-C6811	RES SMT MF 01.00P .12W K06.81	R1-R4,R6-R21,R39,R46-R52
1	42	B0000-821-C8250	RES SMT MF 01.00P .12W H0825	R40
5	43	B0000-821-C1005	RES SMT MF 01.00P .12W M10.0	R29,R33,R75-R77
3	44	B0001-889-S0102	POT CM M K01.00 .25W SMT	R37,R38,R70
2	45	B0001-889-S0103	POT CM M K010.00 .25W SMT	R23,R24
3	46	B0000-821-C1500	RES SMT MF 01.00P .12W H150.00	R72-R74
3	47	J0000-587-SB103	RES NW 08 K10.00 SIP 09P SMT	RN4,RN10,RN11
	48			
	49			
4	50	J0000-585-S0104	RES NW 08 K100.00 SMT 16PIN	RN1,RN3,RN7,RN9
4	51	J0000-587-SB223	RES NW 08 K22.00 SIP 09P SMT	RN2,RN6,RN8,RN5
	52			
2	53	J0000-635-S0100	INDUCTOR 100.0UH 160MA SMT	L1,L2
14	54	B0000-740-00000	TERM PIN TURRET H .062D/.094T	TP1-TP4,TP7,TP9-TP17
1	55	J0000-551-10020	CONN PCB SQ 20POS PC104 F LONG	P2J1
1	56	J0000-551-10032	CONN PCB SQ 32POS PC104 F LONG	P2J1
	57			
1	58	B0002-699-0515S	P/S DC-DC 05V/+-15V@.30MA SIP	PS1
3	59	B0002-419-S0000	ICD H11L3/H11L1 OPTO ISO SMT	OP1-OP3
	60			
2	61	B0002-298-30004	CONN HSG RECP 04PIN M GOLD POL	TB5,TB6
2	62	B0001-882-VHC02	CONN HDR PCB 02P .197 VSH	TB3,TB4
1	63	B0001-882-C0002	CONN PLUG PCB 02P .197 VSH	INSTALL IN TB3
2	64	B0002-298-30006	CONN HSG RECP 06PIN M GOLD POL	TB1,TB2
	65			
1	66	B0002-521-10110	CONN HDR PCB SH4 KEY 2X05 .125	J6
5	67	B0002-521-10020	CONN HDR PCB SH4 SLT 2X10 .125	J1-J5
2	68	B0002-521-10026	CONN HDR PCB SH4 SLT 2X13 .125	J7,J8
	69			
2	70	B0002-624-S0005	TSTR IRLML2402 MFET SMT	Q1,Q2

SYM.	ECO NO.	DATE	BY	CHK	DESCRIPTION
B	11891	11-4-10	P.P		ADDED ITEM 23 & 63 AND ITEM 46 MPL CHG'D
A	11877	8-10-10	P.P	C.J	ITEM #1 & #2 WAS REV-A

REVISIONS

ACAD P/N	C3810-000-00001

MPL PCA SAP LD2 I/O EXPANSION BD

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES
DECIMALS .XX = ±.02 .XXX= ±.010
ANGLES ±.5°
MATERIAL: NONE
FINISH: NONE

TELVENT

SAP I/O EXPANSION BOARD

LANDAC II
CECO

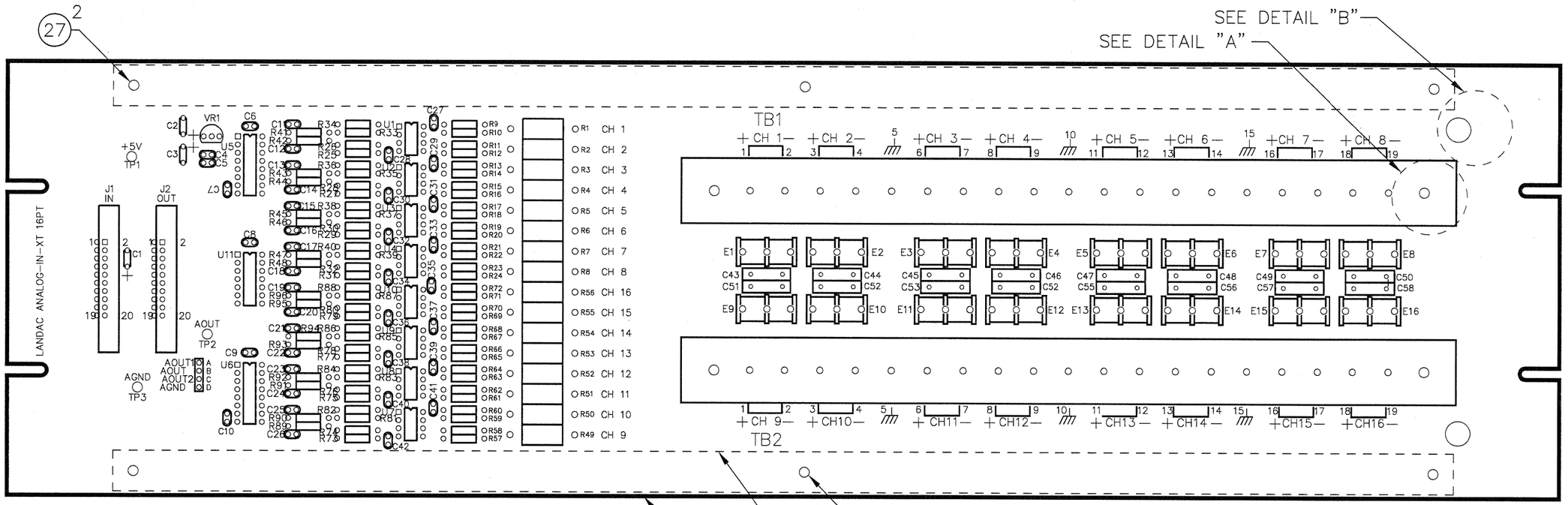
APPROVALS	DATE
DWN PRAVIN	4-8-10
CHK C.JANIK	5-4-10
APP C.JANIK	5-4-10

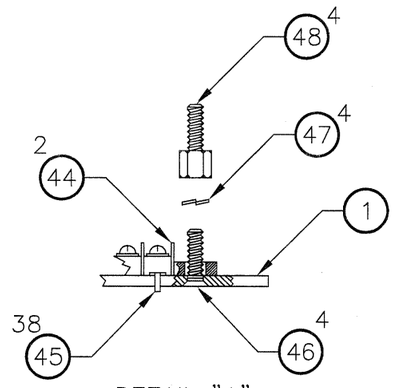
SIZE B | C3810-000-00001 | REV B

SCALE NONE | SHEET 1 OF 1

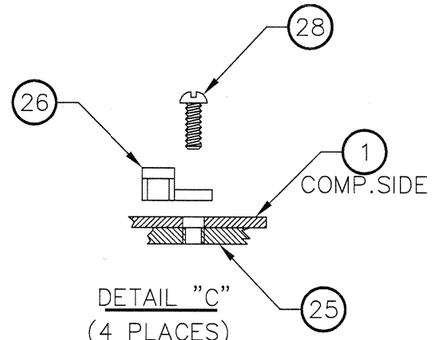
NOTES:

1. MARK BOARD WITH ASSEMBLY PART NUMBER, REVISION LEVEL AND SERIAL NUMBER AFTER FINAL ASSEMBLY.
2. CAUTION! CMOS DEVICES INSTALLED – HANDLE AT GROUNDED WORK STATION.
3. METSO SUPPLIED ITEM.
4. ITEM 28 IS TO BE USED WITH ITEM 26.

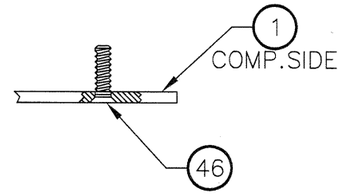




DETAIL "A"
(4 PLACES)
(FOR VARIANCES –1X00X ONLY)
(REMOVABLE TERMINAL BLOCKS)



DETAIL "C"
(4 PLACES)
(ALL VARIANCES)
(AT TERMINAL BLOCKS)



DETAIL "B"
(1 PLACES)
(ALL VARIANCES)
PRESS IN EDGE HOLE

VARIANCES:

C3130–000– XX00X

- 1 = 1–5VDC, +/–5VDC, 49.9K.
- 2 = 4–20mA, 250ohm.
- 3 = +/–1mA, 5.032K.
- 4 = +/–1mA, 4.5K.
- 5 = +/–1mA(3V), 3.012K (WITH +/–2V OVER RANGE) SPECIAL.
- 6 = +/–2.5mA, 2.006K.
- 7 = +/–5mA, 0–5mA, 1.002K.

0 = MOV'S SUPPRESION,
1 = GAS TUBE SUPPRESSION.

0 = NON–REMOVABLE TERMINAL BLOCKS.
1 = REMOVABLE TERMINAL BLOCKS. (SEE DETAIL "A")

EXAMPLES OF VARIANCES:

–00001 = ANALOG IN–XT WITH 1–5VDC, +/–5VDC, MOV'S.
–11002 = ANALOG IN–XT WITH 4/20MA, REMOVABLE TERMINAL BLOCKS, GAS TUBES.
–10003 = ANALOG IN–XT WITH +/–1MA, REMOVABLE TERMINAL BLOCKS, MOV'S.

RESISTOR VALUE — INPUT CURRENT

MPL P C A L D A N A – I N – X T X X X X X X X X X X X

SYM.	ECO NO.	DATE	BY	CHK	DESCRIPTION
J	11603	10–10–06	P.P		SILK SCREEN CORRECTED, & B.O.M. CORRECTED
I	11074	4–24–02	P.P	DM	REVISED & REDRAWN IN AUTOCAD, ADDED BOM TO DWG, ADDED NEW VAR. –11002
H	8957	91–5–30	GW	CJ	NEW "CF" FORMAT DWG. COMPONENT CHANGES

REVISIONS

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES
DECIMALS .XX = ±.02 .XXX= ±.010
ANGLES ±.5°
MATERIAL: NONE
FINISH: NONE

TELVENT

APPROVALS	DATE
DWN GW	88–2–3
CHK CJ	88–2–8
APP CJ	88–2–8

PCA LANDAC
ANALOG–IN–XT
16 POINTS
ASSEMBLY DRAWING

ACAD P/N C3130–000–XX00X–1

SIZE B | C3130–000–XX00X | REV J

SCALE NONE | SHEET 1 OF 2

QTY -11005	QTY -11003	QTY -11002	QTY -01007	QTY -01006	QTY -01003	QTY -0003	QTY -0002	ITEM	PART NUMBER	DESCRIPTION	NOTES
1	1	1	1	1	1	1	1	1	C3130-001-REV-D	PCB LD ANA-IN-XT 16PT	
0	0	0	0	0	0	0	0	2	C3130-002-00000	SCH LD ANA-IN-XT 16PT	SEE NOTE 3
1	1	1	1	1	1	1	1	3	B0001-847-00000	ICD 74HC00 NAND QUAD 2-INPUT	U11
2	2	2	2	2	2	2	2	4	B0001-847-04051	ICD 74HC4051 8CH MUX	U5,U6
								5			
8	8	8	8	8	8	8	8	6	B0001-874-10001	ICL AD706 DUAL PICO AMP OP AMP	U1-U4,U7-U10
1	1	1	1	1	1	1	1	7	B0001-885-00000	ICL 79L05ACZ V-REG -5V 100MA	VR1
								8			
39	39	39	39	39	39	39	39	9	B0000-798-00000	CAP-N CE 050V M000.1000 20P RL	C4-C42
3	3	3	3	3	3	3	3	10	B0001-870-00000	CAP-N CE 050V SR30 Z5U 105 20%	C1-C3
16	16	16	16	16	16	16	16	11	B0001-694-00000	CAP-N CE 999V M000.0200 20P RL	C43-C58
								12			
								13			
16	16	16	16	16	16	16	16	14	B0002-228-B1581	RES MF 01.00P 00.25W K001.58	R41-R48,R89-R96
32	32	32	32	32	32	32	32	15	B0001-888-00000	RES MF 00.10P 00.12W K200.00	R25-R40,R73-R88
32	32	32	32	32	32	32	32	16	B0001-887-00000	RES MF 00.10P 00.12W K499.00	R9-R24,R57-R72
								17			
2	2	2	2	2	2	2	2	18	B0002-521-10020	CONN HDR PCB SH4 SLT 2X10 .125	J1, J2
0	0	0	0	0	0	0	0	19	B0002-291-00004	CONN HDR PCB 04P S.100 .120	W1 (INTERCHANGEABLE)
1	1	1	1	1	1	1	1	20	B0002-291-00032	CONN HDR PCB 32P S.100 .120	VARIABLE
2	2	2	2	2	2	2	2	21	B0002-290-00000	JUMPER MINI 0.100 1R 2P GOLD	W1 (A-B,C-D)
								22			
3	3	3	3	3	3	3	3	23	B0002-740-00000	TERM PIN TURRET H .062D/.094T	TP1, TP2, TP3
								24			
2	2	2	2	2	2	2	2	25	B8135-006-00000	BAR SUPPORT PCB RELAY	
4	4	4	4	4	4	4	4	26	J0000-252-00001	CBL TIE NYL AHR #08 TA1S8	SEE DETAIL "C"
2	2	2	2	2	2	2	2	27	J6011-011-00000	SCREW-MACH 6-32 BH SS 0375	
4	4	4	4	4	4	4	4	28	J0000-450-00000	SCREW-MACH 6-32 BH SS 0437	SEE NOTE 4
								29			
								30			
								31			
-	-	-	16	-	-	-	-	32	J0000-566-10020	RES WW 0.025P 00.12W K001.002	R1-R8,R49-R56
-	-	-	-	16	-	-	-	33	J0000-566-20060	RES WW 0.025P 00.12W K002.006	R1-R8,R49-R56
16	-	-	-	-	-	-	-	34	J0000-566-30120	RES WW 0.025P 00.12W K003.012	R1-R8,R49-R56
								35			
								36			
-	-	16	-	-	-	-	16	37	J0000-658-00000	RES WW 0.025P 00.25W H250.00	R1-R8,R49-R56
-	16	-	-	-	16	16	-	37	J0000-566-00001	RES WW 0.025P 00.12W K005.032	R1-R8,R49-R56
								38			
								39			
16	16	16	16	16	16	-	-	40	B0002-181-00001	SURGE SUPPR GAS 230V HD FORMED	E1-E16
-	-	-	-	-	-	32	32	41	B0002-476-00000	VARISTOR 130V 184V MOX V130LA1	E1-E16
								42			
-	-	-	2	2	2	2	2	43	B0001-189-00000	TB PCB S.438 8-32 19 BE	TB1,TB2
2	2	2	-	-	-	-	-	44	B0001-935-00019	TB PCB S.438 8-32 19 ME GBPAX	TB1,TB2
38	38	38	-	-	-	-	-	45	B0001-956-00001	JACK PC MNT F/0.062DIA PIN	USED ON TB1, TB2
5	5	5	1	1	1	1	1	46	B0001-955-00832	FASTENER PCB EXT 8-32 TD TIN	SEE DETAIL A & B
4	4	4	-	-	-	-	-	47	J4001-240-00000	WASHER LOCK INT NO 8 SS	USED ON TB1, TB2
4	4	4	-	-	-	-	-	48	B0001-263-00000	SPACER SS 0.500 1/4H MF 8-32	USED ON TB1, TB2

SYM.	ECO NO.	DATE	BY	CHK	DESCRIPTION
J	11603	10-10-06	P.P		SEE SHT. 1
I	11074	4-24-02	P.P	DM	SEE SHT. 1
H	8957	91-5-30	GW	CJ	SEE SHT. 1

REVISIONS

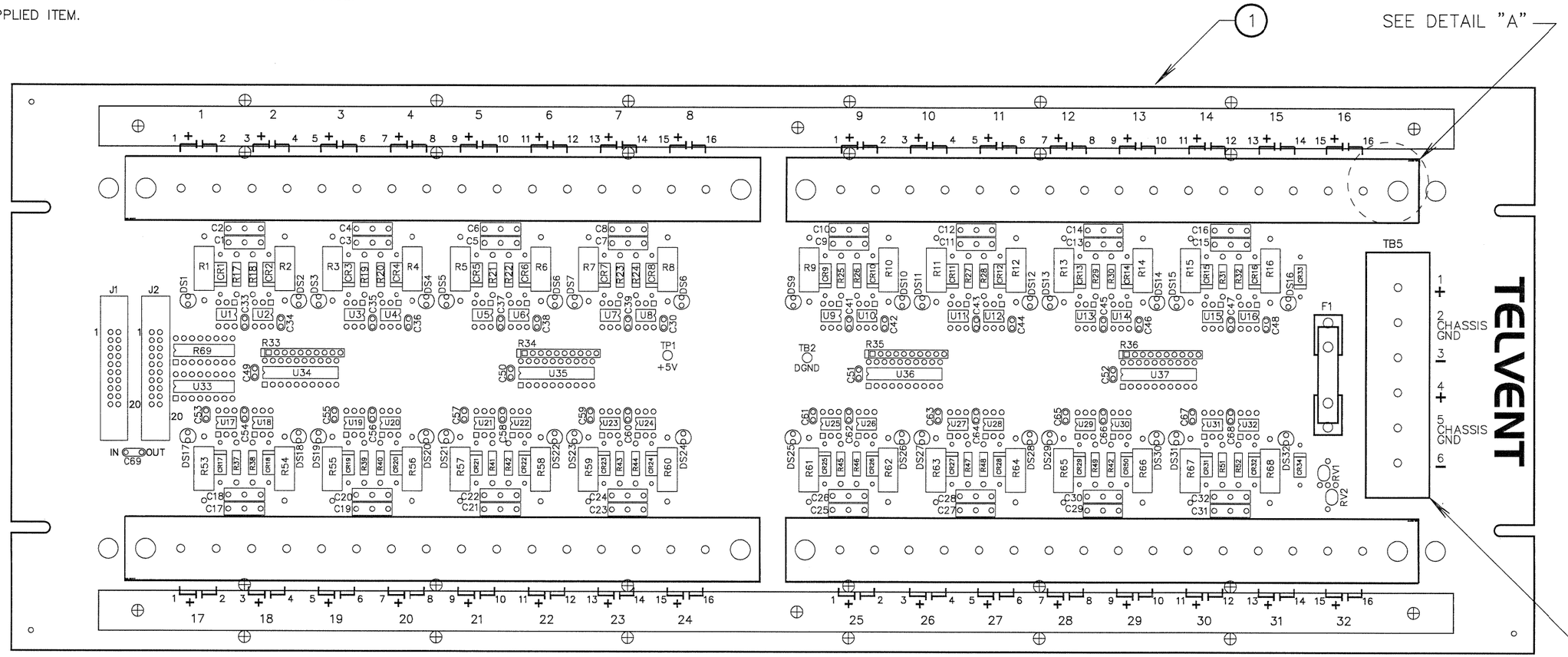
ACAD P/N	C3130-000-XX00X-2

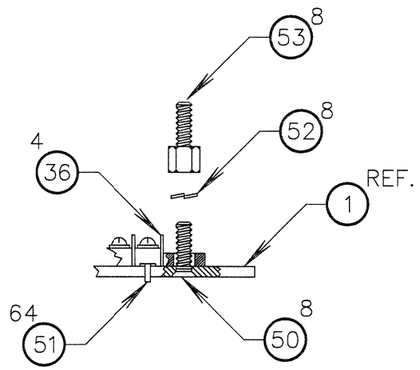
APPROVALS	DATE
DWN GW	88-2-3
CHK CJ	88-2-8
APP CJ	88-2-8

SIZE		REV
B	C3130-000-XX00X	J
SCALE NONE	SHEET 2 OF 2	

NOTES:

1. CAUTION! CMOS DEVICES INSTALLED – HANDLE AT GROUNDED WORK STATION.
2. MARK BOARD WITH ASSEMBLY PART NUMBER, REVISION LEVEL AND SERIAL NUMBER AFTER FINAL ASSEMBLY.
3. SEE DETAIL "A" FOR ASSEMBLY WITH REMOVABLE TERMINAL BLOCKS.
4. TERMINAL BLOCK TB5 IS NOT REMOVABLE WITH ANY VARIANCE.
5. TELVENT SUPPLIED ITEM.





DETAIL "A"
(8 PLACES)

(FOR VARIANCES –1000X ONLY)
(REMOVABLE TERMINAL BLOCKS)

(WITH REMOVABLE TERMINAL BLOCKS)	–10005 = P C A	L D	D – I N – X T	3 2 P T	4 8 D C W / R T B
(WITH REMOVABLE TERMINAL BLOCKS)	–10004 = P C A	L D	D I – X T	3 2 P T	1 2 9 V W / R T B
(WITH REMOVABLE TERMINAL BLOCKS)	–10003 = P C A	L D	D I – X T	3 2 P T	2 4 / 4 8 V W / R T B
(WITHOUT REMOVABLE TERMINAL BLOCKS)	–00005 = P C A	L D	D – I N – X T	3 2 P T	4 8 D C W O / R T B
(WITHOUT REMOVABLE TERMINAL BLOCKS)	–00004 = P C A	L D	D – I N – X T	3 2 P T	1 2 9 V W O / R T B
(WITHOUT REMOVABLE TERMINAL BLOCKS)	–00003 = P C A	L D	D I – X T	3 2 P T	2 4 / 4 8 V W O / R T B

MPL P C A L D X X X X X X X X X X X X X X X X X X X X X X X X

REVISIONS					
SYM.	ECO NO.	DATE	BY	CHK	DESCRIPTION
K	11625	2–9–07	P.P	CJ	VAR. –10004 & –10005 ITEM #27 & #28 QTY. CORRECTD
J	11423	4–12–04	P.P	CJ	ITEM 1 WAS –001–REV–E
I	10353	5–9–00	P.P	D.M	REVISED & REDRAWN IN AutoCAD, ADDED BOM TO DWG.
H	8752	9–14–90	GW	K.T	ITEM 1 WAS –REV–D; ITEM 3 WAS –00000
G	8621B	5–1–90	GW	CJ	ITEM 26 WAS B9103–003; ITEM 28 WAS J0332–007.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES
DECIMALS .XX = ±.02 .XXX= ±.010
ANGLES ±.5°
MATERIAL: NONE
FINISH: NONE

TELVENT

APPROVALS		DATE
DWN	GW	2–10–88
CHK	CJ	2–15–88
APP	CJ	2–15–88

PCA LANDAC
D–IN–XT BOARD
32 PT
ASSEMBLY

ACAD P/N: C3132–000–X000X–1

SIZE B | C3132–000–X000X | REV K

SCALE NONE | SHEET 1 OF 2

QTY -10005	QTY -10004	QTY -10003	QTY -00005	QTY -00004	QTY -00003	ITEM	PART NUMBER	DESCRIPTION	NOTES
1	1	1	1	1	1	1	C3132-001-REV-F	PCB LD D-IN-XT 32PT	
						2			
0	0	0	0	0	0	3	C3132-002-REV-C	SCH LD DIGITAL INPUT XT 32 PT	NOTE 5
						4			
1	1	1	1	1	1	5	B0001-847-00138	ICD 74HC138 3-8 LINE DECODER	U33
4	4	4	4	4	4	6	B0001-847-00240	ICD 74HC240 BUFFER	U34-U37
32	32	32	32	32	32	7	B0002-419-00000	ICD H11L3/H11L1 OPTO ISO	U1-U32
						8			
						9			
32	32	32	32	32	32	10	B0001-247-00000	DIODE P6KE8.2 Z 8.2V 0600W	CR1-CR32
2	2	2	2	2	2	11	J1160-016-00000	DIODE 1N4004 RS 400V 01.00A	CR33,CR34
						12			
32	32	32	32	32	32	13	B0000-871-00000	LED RED CYL 1.7V T1.75	DS1-DS32
						14			
36	36	36	36	36	36	15	B0000-798-00000	CAP-N CE 050V M000.1000 20P RL	C33-C68
32	32	32	32	32	32	16	B0001-694-00000	CAP-N CE 999V M000.0200 20P RL	C1-C32
1	1	1	1	1	1	17	B0002-377-00000	CAP-N CE 050V 0.1000MF 20P RL	C69
						18			
2	2	2	2	2	2	19	B0000-372-00000	FUSE CLIP PC MOUNT	2 USED FOR F1
1	1	1	1	1	1	20	J4003-014-00000	FUSE 00.250A 3AG 250V #312 NB	F1
						21			
1	1	1	1	1	1	22	B0001-285-39100	RES NW 08 H390.00 DIP 16P 02%D	R69
4	4	4	4	4	4	23	B0002-505-10300	RES NW 08 K010.00 SIP 09P 02%B	R33-R36
						24			
32	32	32	32	32	32	25	B9402-034-00000	RES CC 05.00P 00.25W H820.00	R17-R32,R37-R52
-	-	32	-	-	32	26	B0000-412-00000	RES CC 05.00P 01.00W K002.20	R1-R16,R53-R68
-	32	-	-	32	-	27	B0002-169-00000	RES CC 05.00P 01.00W K020.0000	R1-R16,R53-R68
32	-	-	32	-	-	28	B0001-576-D6220	RES CC 05.00P 01.00W K006.20	R1-R16,R53-R68
2	2	2	2	2	2	29	B0002-476-00000	VARISTOR 130V 184V MOX V130LA1	RV1,RV2
						30			
2	2	2	2	2	2	31	B0000-740-00000	TERM PIN TURRET H .062D/.094T	TP1,TP2
						32			
2	2	2	2	2	2	33	B0002-521-10020	CONN HDR PCB SH4 SLT 2X10 .125	J1,J2
						34			
-	-	-	4	4	4	35	B0001-191-00000	TB PCB S.438 8-32 16 ME	TB1-TB4
4	4	4	-	-	-	36	B0001-935-00016	TB PCB S.438 8-32 16 ME	TB1-TB4
1	1	1	1	1	1	37	B0001-191-00006	TB PCB S.438 8-32 06 BE	TB5
						38			
						39			
						40			
						41			
						42			
						43			
2	2	2	2	2	2	44	B8135-006-00000	BAR SUPPORT PCB RELAY	SEE ASSY. DETAIL NOTES.
						45			
						46			
6	6	6	6	6	6	47	J6011-011-00000	SCREW-MACH 6-32 BH SS 0375	SEE ASSY. DETAIL NOTES.
						48			
						49			
8	8	8	-	-	-	50	B0001-955-00832	FASTENER PCB EXT 8-32 TD TIN	SEE DETAIL "A"
64	64	64	-	-	-	51	B0001-956-00001	JACK PC MNT F/0.062DIA PIN	SEE DETAIL "A"
8	8	8	-	-	-	52	J4001-240-00000	WASHER LOCK INT NO 8 SS	SEE DETAIL "A"
8	8	8	-	-	-	53	B0001-263-00000	SPACER SS 0.500 1/4H MF 8-32	SEE DETAIL "A"
						54			
						55			
						56			
						57			
						58			
						59			
						60			

SYM.	ECO NO.	DATE	BY	CHK	DESCRIPTION
REVISIONS					
K	11625	2-9-07	P.P		SEE SHT. 1
J	11423	4-12-04	P.P	CJ	SEE SHT. 1
I	10353	5-9-00	P.P	D.M	SEE SHT. 1
H	8752	9-14-90	GW	K.T	SEE SHT. 1
G	8621B	5-1-90	GW	CJ	SEE SHT. 1

ACAD P/N	C3132-000-X000X-2

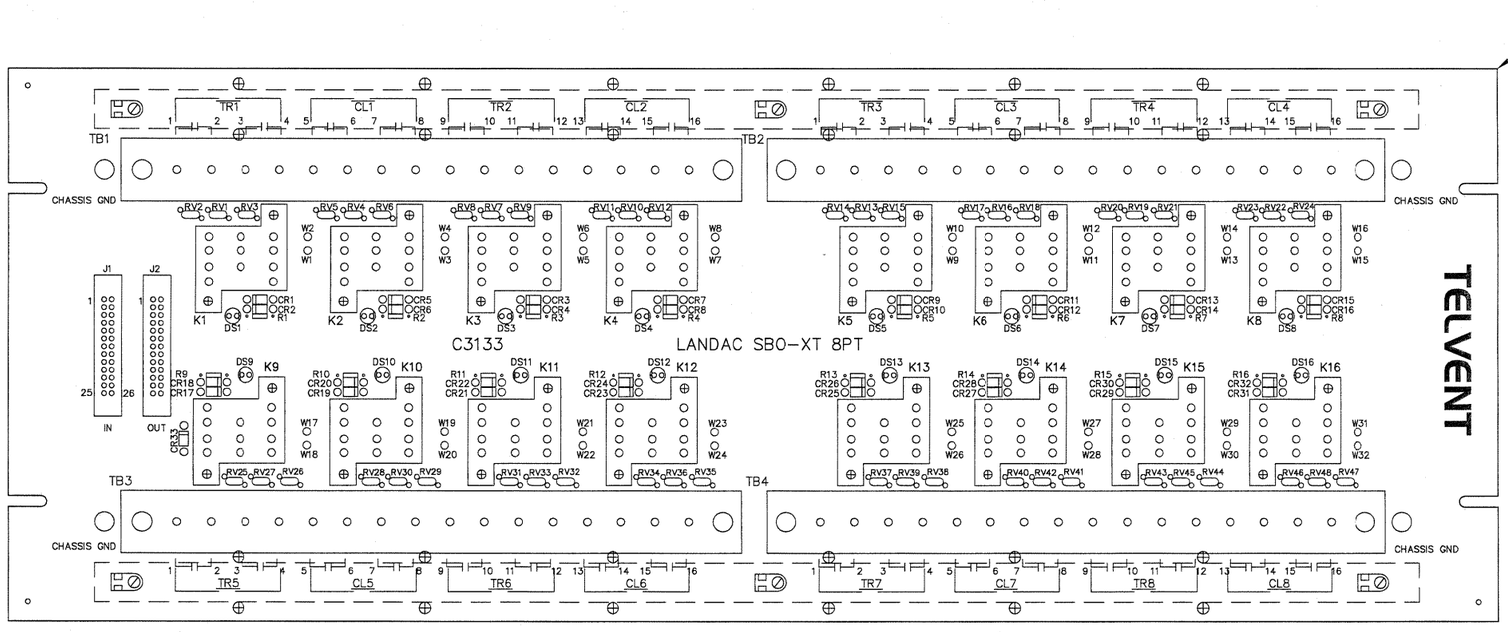
APPROVALS	DATE
DWN GW	2-10-88
CHK CJ	2-15-88
APP CJ	2-15-88

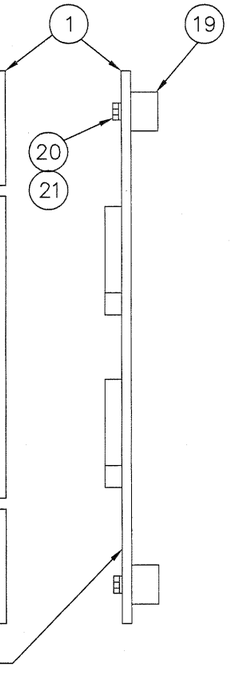
SIZE		REV
B	C3132-000-X000X	K
SCALE NONE	SHEET 2 OF 2	

NOTES :

1. MARK BOARD WITH TOP ASSEMBLY PART NUMBER, REVISION LEVEL AND SERIAL NUMBER AFTER FINAL ASSEMBLY.

QTY -32100	QTY -31100	QTY -22100	QTY -21100	QTY -12100	QTY -11100	ITEM	PART NUMBER	DESCRIPTION	NOTES
1	1	1	1	1	1	1	C3133-001-REV-D	PCB LD SBO-XT 8 PT	
						2			
0	0	0	0	0	0	3	C3133-002-REV-A	SCH LD SBO CONTROL 8 T/C PTS	
						4			
33	33	33	33	33	33	5	J1160-016-00000	DIODE 1N4004 RS 400V 01.00A	CR1-CR33
						6			
16	–	16	–	16	–	7	B0001-406-00001	LED RED CYL DIF 1.8V T1.75	DS1-DS16
–	–	–	48	–	–	7	B0002-476-00000	VARISTOR 130V 184V MOX V130LA1	RV1-RV48
16	–	–	–	–	–	8	B0002-476-00000	VARISTOR 130V 184V MOX V130LA1	RV2,RV5,RV8,RV11,RV14,RV17,RV20,RV23 RV26,RV29,RV32,RV35,RV38,RV41,RV44,RV47
–	–	48	–	–	–	9	B0002-476-00000	VARISTOR 130V 184V MOX V130LA1	RV1-RV48
–	16	–	–	–	–	10	B0002-476-00000	VARISTOR 130V 184V MOX V130LA1	X
16	–	16	16	16	–	11	B0002-228-B1002	RES MF 01.00P 00.25W K010.00	R1-R16
						12			
16	16	16	16	16	16	13	B0001-080-00000	SOCKET RLY 11PIN REC PC 10A	K1-K16
						14			
4	4	4	4	4	4	15	B0001-191-00000	TB PCB S.438 8-32 16 ME	TB1-TB4
						16			
2	2	2	2	2	2	17	B0002-521-10026	CONN HDR PCB SH4 SLT 2X13 .125	J1, J2
						18			
2	2	2	2	2	2	19	B8135-006-00000	BAR SUPPORT PCB RELAY	
6	6	6	6	6	6	20	J0000-450-00000	SCREW-MACH 6-32 BH SS 0437	
6	6	6	6	6	6	21	J0000-252-00001	CBL TIE NYL AHR #08 TA1S8	
						22			
–	–	–	–	–	–	23	B0001-719-00024	RLY EN 24VDC 1FX 010A@150V MB	K1-K16
–	–	–	–	–	–	24	B0001-075-00000	SPRING RELAY 1.9Hx1.4W RLY	K1-K16
–	–	–	–	–	–	25	B0001-076-00000	POP RIVT OP 5-32D	K1-K16
						26			
–	–	–	–	–	–	27	B0001-084-00000	RLY 24VDC 2FC 010A PWR PL	K1-K15 (ODD ONLY)
–	–	–	–	–	–	28	B0001-075-00000	SPRING RELAY 1.9Hx1.4W RLY	K1-K15 (ODD ONLY)
			–	–	–	29	B0001-076-00000	POP RIVT OP 5-32D	K1-K15 (ODD ONLY)
						30			





VARIANCE STRUCTURE : – X X 1 0 0

- 1 = NO MOV'S
  2 = MOV'S ALL LOCATION
  3 = MOV'S FORM X
- 1 = NO LED'S
  2 = LED'S
- 1 = ALL RELAY SOCKETS POPULATED

W = WITH
W O = WITHOUT

H	11689	10-9-07	P.P		ITEM 8 QTY. WAS 23
G	11424	4-12-04	P.P		ITEM 1 WAS -001-REV-C, & ADDED B.O.M.
F	8975A	91-6-26	GW	WE	NEW CF-FORMET. COMPONENT CHANGES.
SYM.	ECO NO.	DATE	BY	CHK	DESCRIPTION

REVISIONS

ACAD P/N: C3133-A00-XX100

MPL | PCA | LD SBO XT | XX/MOV | XX/LED

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES
DECIMALS XX = ±.02 .XXX= ±.010
ANGLES ±.5°

MATERIAL: NONE

FINISH: NONE

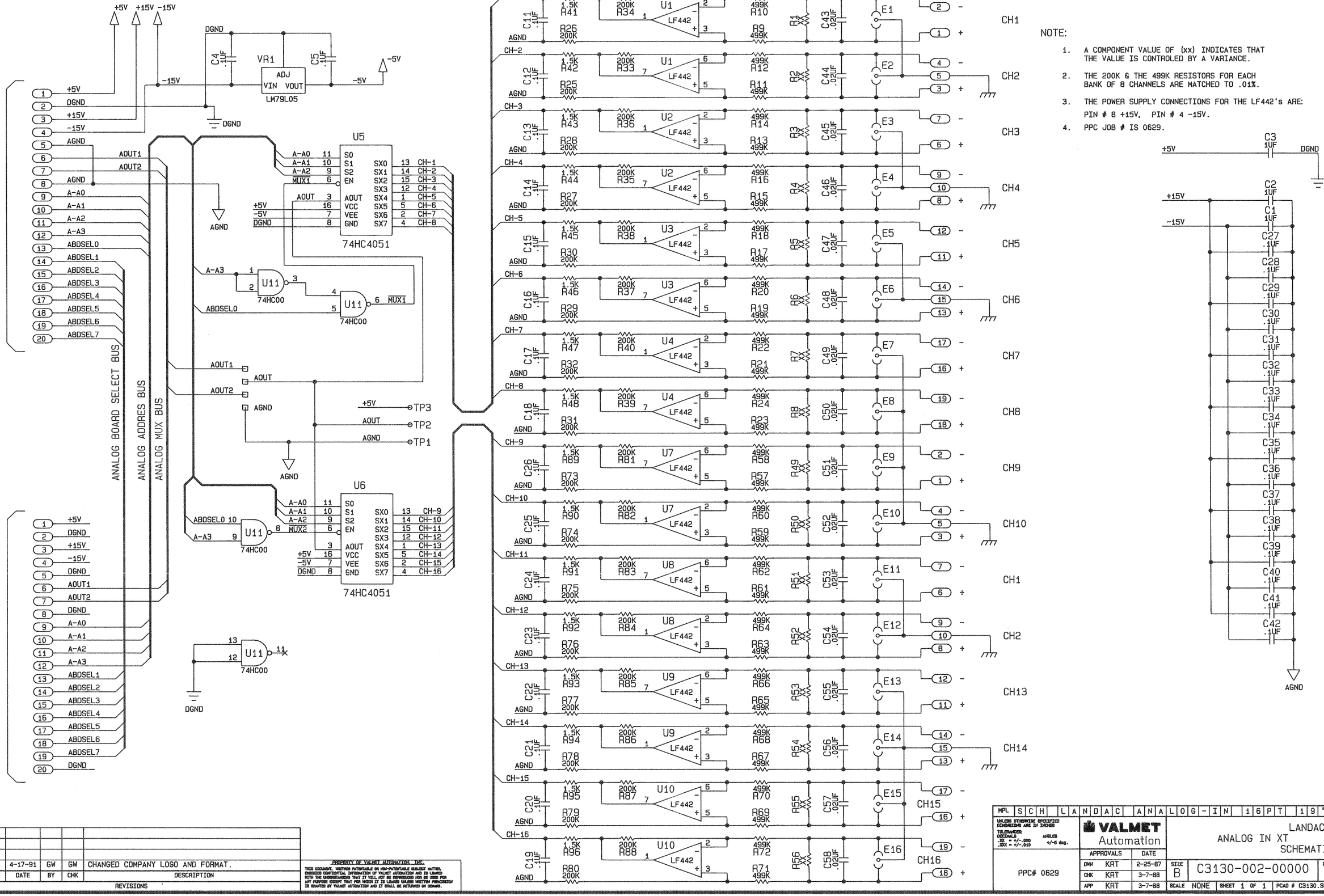
TELVENT

PCA LANDAC SBO-XT, 8PT, WITH OR WITHOUT LED'S/MOV'S ASSEMBLY DRAWING

APPROVALS	DATE
DWN GW	10-17-88
CHK C.JANIK	10-26-88
APP C.JANIK	10-26-88

SIZE B | C3133-A00-XX100 | REV H

SCALE NONE | SHEET 1 OF 1



SYM	ECO #	DATE	BY	CHK	DESCRIPTION
0	-	4-17-91	GW	GW	CHANGED COMPANY LOGO AND FORMAT.

REVISIONS

MPL | SCH | LANDAC ANALOG-IN 16PT 19"

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: DECIMALS .XX = +/-.005 .XXX = +/-.010 ANGLES +/-5 deg.

PPC# 0629

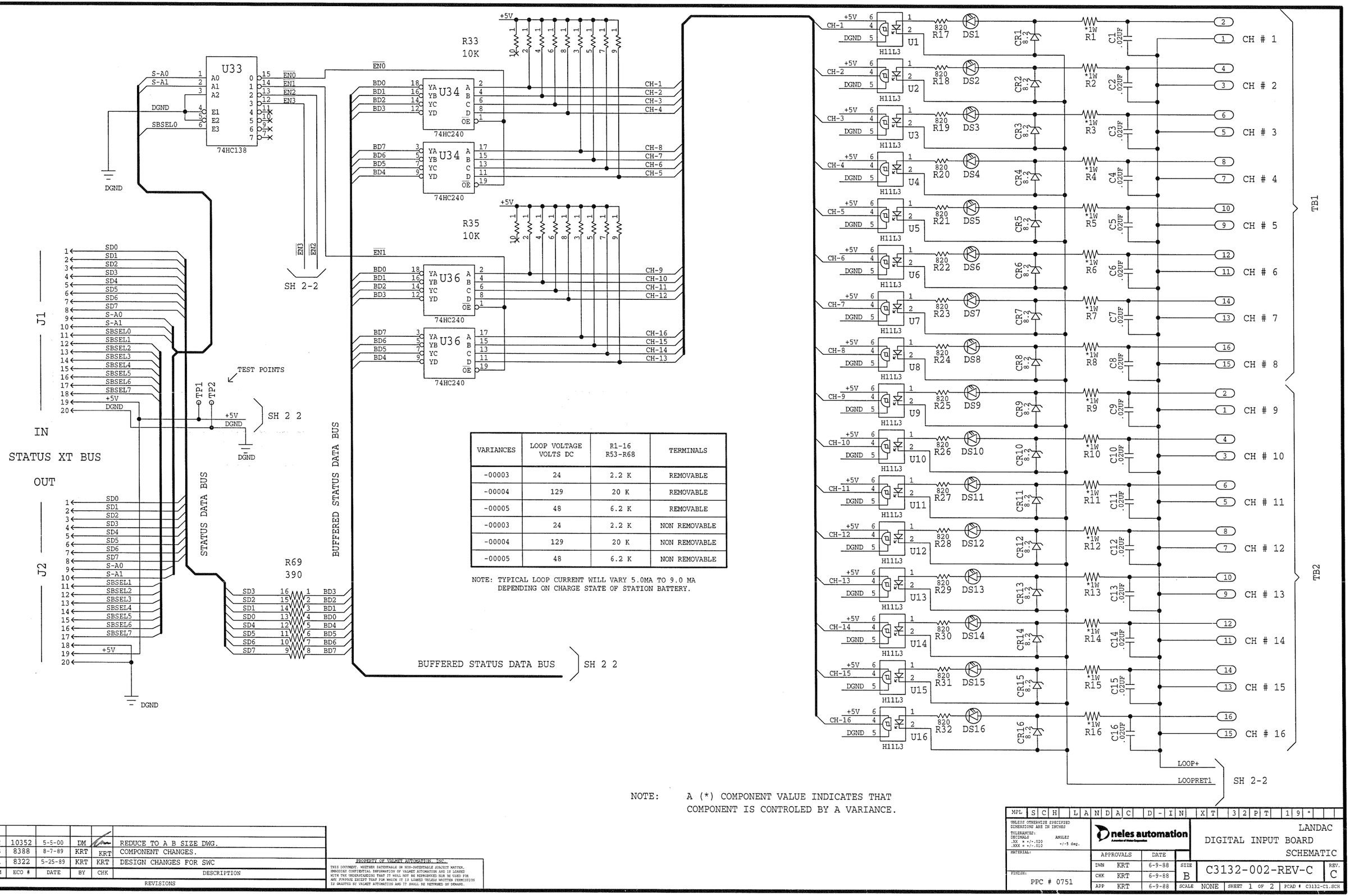
VALMET Automation

APPROVALS		DATE
DWN	KRT	2-25-87
CHK	KRT	3-7-88
APP	KRT	3-7-88

LANDAC
ANALOG IN XT
SCHEMATIC

SIZE	DRAWING NO.	REV.
B	C3130-002-00000	0

SCALE NONE | SHEET 1 OF 1 | PCAD # C3130.SCH



VARIANCES	LOOP VOLTAGE VOLTS DC	R1-16 R53-R68	TERMINALS
-00003	24	2.2 K	REMOVABLE
-00004	129	20 K	REMOVABLE
-00005	48	6.2 K	REMOVABLE
-00003	24	2.2 K	NON REMOVABLE
-00004	129	20 K	NON REMOVABLE
-00005	48	6.2 K	NON REMOVABLE

NOTE: TYPICAL LOOP CURRENT WILL VARY 5.0MA TO 9.0 MA DEPENDING ON CHARGE STATE OF STATION BATTERY.

NOTE: A (*) COMPONENT VALUE INDICATES THAT COMPONENT IS CONTROLED BY A VARIANCE.

SYM	ECO #	DATE	BY	CHK	DESCRIPTION
C	10352	5-5-00	DM		REDUCE TO A B SIZE DWG.
B	8388	8-7-89	KRT	KRT	COMPONENT CHANGES.
A	8322	5-25-89	KRT	KRT	DESIGN CHANGES FOR SWC

REVISIONS

MPL SCH LANDAC D-IN XT 32PT 19*

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: DECIMALS .XX ± +/-.020 .XXX ± +/-.010 ANGLES +/-5 deg.
MATERIAL:
FINISH: PPC # 0751

neles automation

APPROVALS		DATE
DWN	KRT	6-9-88
CHK	KRT	6-9-88
APP	KRT	6-9-88

LANDAC
DIGITAL INPUT BOARD
SCHEMATIC

SIZE B | C3132-002-REV-C | REV. C

SCALE NONE | SHEET 1 OF 2 | PCAD # C3132-C1.SCH

R34
10K

R36
10K

EN2

EN3

U35 74HC240 — BD0 BD1 BD2 BD3 → CH-17 CH-18 CH-19 CH-20

U35 74HC240 — BD7 BD6 BD5 BD4 → CH-24 CH-23 CH-22 CH-21

U37 74HC240 — BD0 BD1 BD2 BD3 → CH-25 CH-26 CH-27 CH-28

U37 74HC240 — BD7 BD6 BD5 BD4 → CH-32 CH-31 CH-30 CH-29

EN2
EN3
BUFFERED STATUS DATA BUS
SH 1-2

3AG .250 AMP 250V
F1

TB5
1 S-PWR+ — LOOP+
2 EGND — EGND
3 S-PWR- — LOOPRET1
1N4004 CR33
LOOPRET2
1N4004 CR34
1 S-PWR+
2 EGND
3 S-PWR-
E1

SH 1-2,SH2-2
SH 1-2,SH2-2
SH 1-2

+5V
C33 .1UF C34 .1UF C35 .1UF C36 .1UF C37 .1UF C38 .1UF C39 .1UF C40 .1UF C41 .1UF C42 .1UF C43 .1UF C44 .1UF C45 .1UF C46 .1UF C47 .1UF C48 .1UF
DGND

+5V
C53 .1UF C54 .1UF C55 .1UF C56 .1UF C57 .1UF C58 .1UF C59 .1UF C60 .1UF C61 .1UF C62 .1UF C63 .1UF C64 .1UF C65 .1UF C66 .1UF C67 .1UF C68 .1UF
DGND

TB3

U17	CH-17	R37	DS17	CR17 8.2	R53 *1W	C17 .02UF
U18	CH-18	R38	DS18	CR18 8.2	R54 *1W	C18 .02UF
U19	CH-19	R39	DS19	CR19 8.2	R55 *1W	C19 .02UF
U20	CH-20	R40	DS20	CR20 8.2	R56 *1W	C20 .02UF
U21	CH-21	R41	DS21	CR21 8.2	R57 *1W	C21 .02UF
U22	CH-22	R42	DS22	CR22 8.2	R58 *1W	C22 .02UF
U23	CH-23	R43	DS23	CR23 8.2	R59 *1W	C23 .02UF
U24	CH-24	R44	DS24	CR24 8.2	R60 *1W	C24 .02UF
U25	CH-25	R45	DS25	CR25 8.2	R61 *1W	C25 .02UF
U26	CH-26	R46	DS26	CR26 8.2	R62 *1W	C26 .02UF
U27	CH-27	R47	DS27	CR27 8.2	R63 *1W	C27 .02UF
U28	CH-28	R48	DS28	CR28 8.2	R64 *1W	C28 .02UF
U29	CH-29	R49	DS29	CR29 8.2	R65 *1W	C29 .02UF
U30	CH-30	R50	DS30	CR30 8.2	R66 *1W	C30 .02UF
U31	CH-31	R51	DS31	CR31 8.2	R67 *1W	C31 .02UF
U32	CH-32	R52	DS32	CR32 8.2	R68 *1W	C32 .02UF

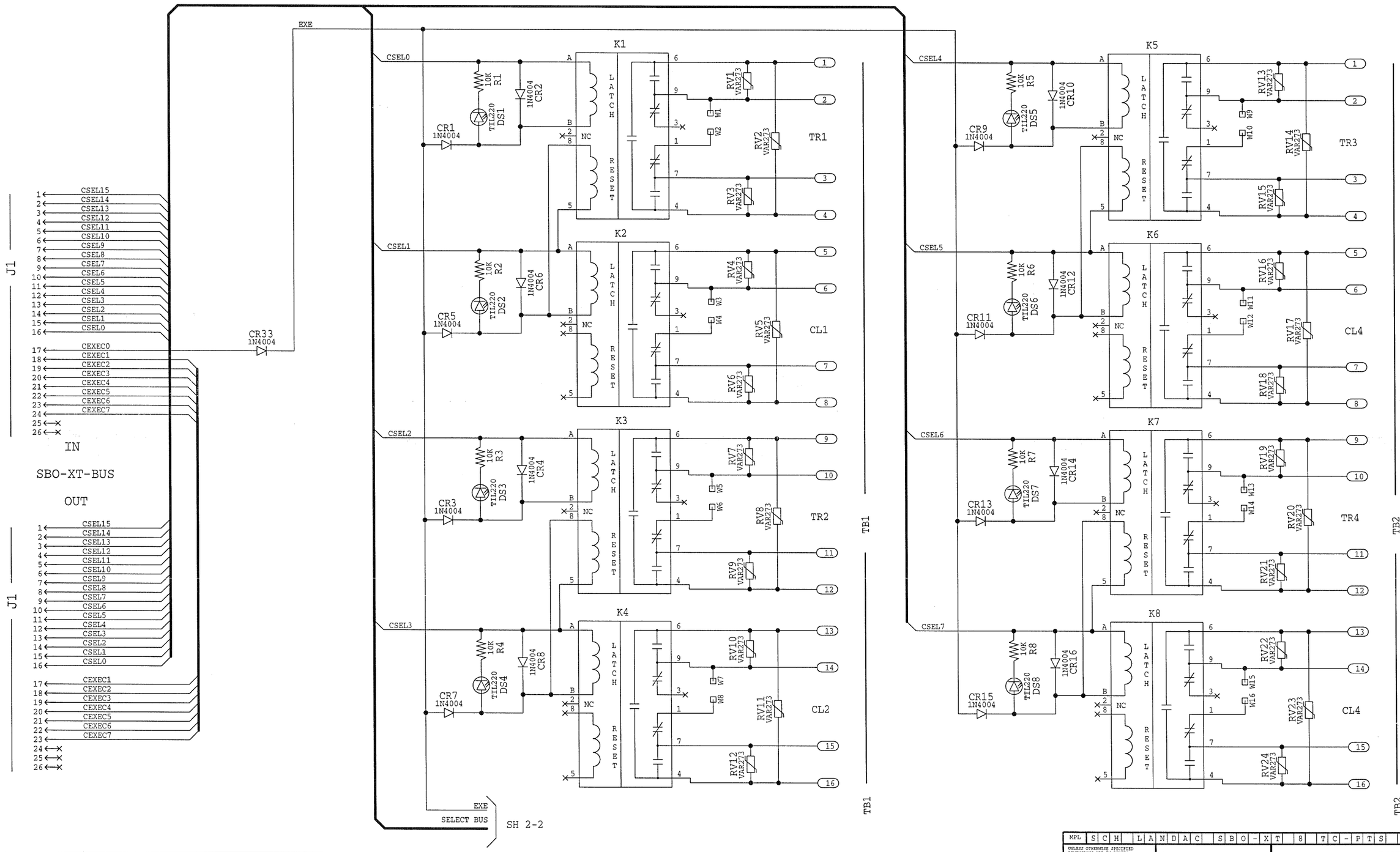
All: +5V, DGND, H11L3

TB3: 2/1 CH # 17; 4/3 CH # 18; 6/5 CH # 19; 8/7 CH # 20; 10/9 CH # 21; 12/11 CH # 22; 14/13 CH # 23; 16/15 CH # 24

TB4: 2/1 CH # 25; 4/3 CH # 26; 6/5 CH # 27; 8/7 CH # 28; 10/9 CH # 29; 12/11 CH # 30; 14/13 CH # 31; 16/15 CH # 32

LOOPRET2
LOOP+

SIZE		REV.
B	C3132-002-REV-C	C
SCALE NONE	SHEET 2 OF 2	PCAD # C3132-C2.SCH



SYM	ECO #	DATE	BY	CHK	DESCRIPTION
-	10350	5-8-00	DM		RESCALE TO B SIZE DRAWING.
A	8550	2-8-90	GW	CJ	RESISTORS R1-R16 WERE 2.74K.

REVISIONS

MPL SCH LANDAC SBO-XT 8 TC-PTS

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES:
DECIMALS
.XX = +/-.020
.XXX = +/-.010
ANGLES
+/-5 deg.
MATERIAL:
FINISH:

neles automation
A subsidiary of Metso Corporation

APPROVALS		DATE
DWN	TOOKER	4-16-88
CHK	TOOKER	4-26-88
APP	TOOKER	4-26-88

SBO-XT LANDAC SCHEMATIC

SIZE B | C3133-002-REV-A | REV. A

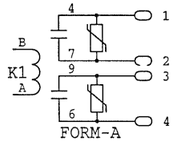
SCALE NONE | SHEET 1 OF 2 | PCAD # C3133-A1.SCH

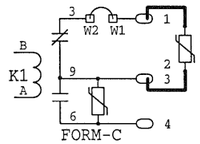
SH 1-2

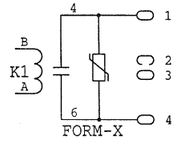
SELECT BUS

EXE

EXAMPLE OF EACH OUTPUT TYPE

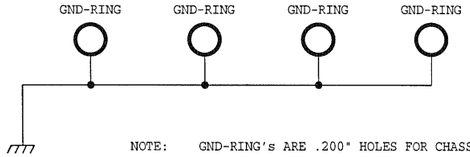




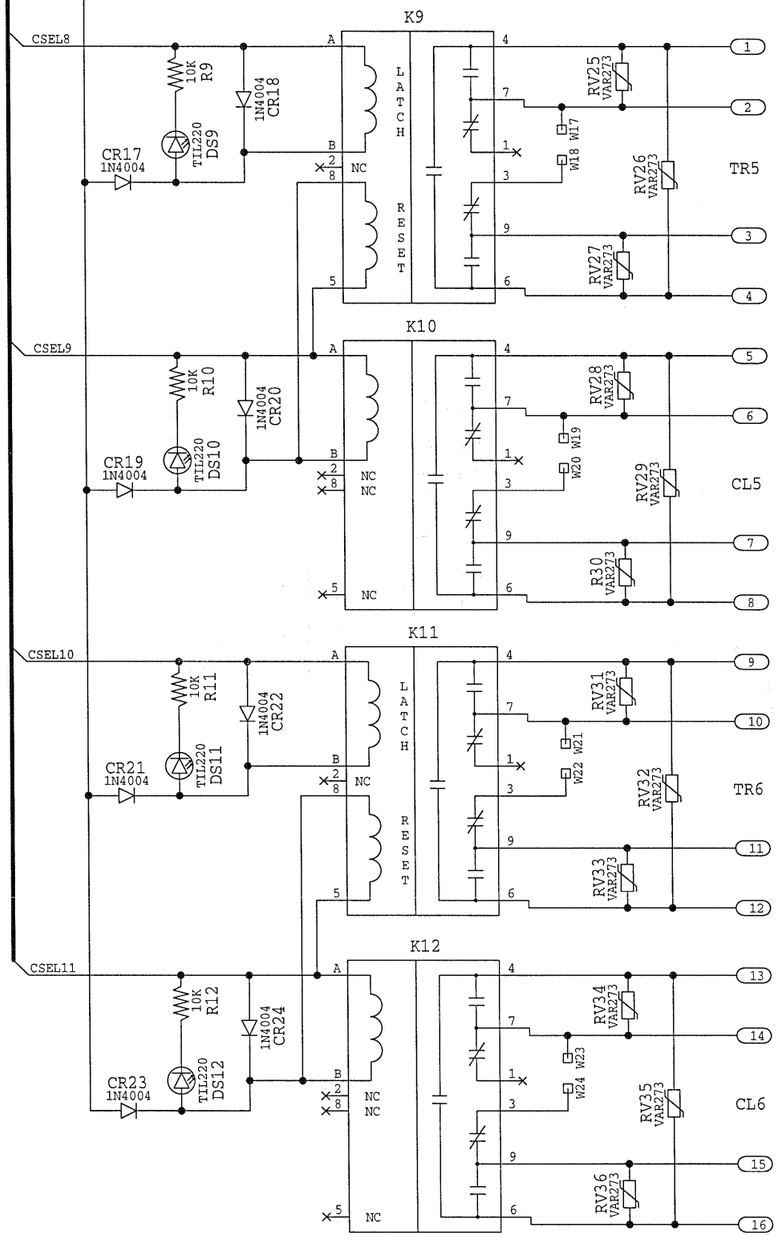


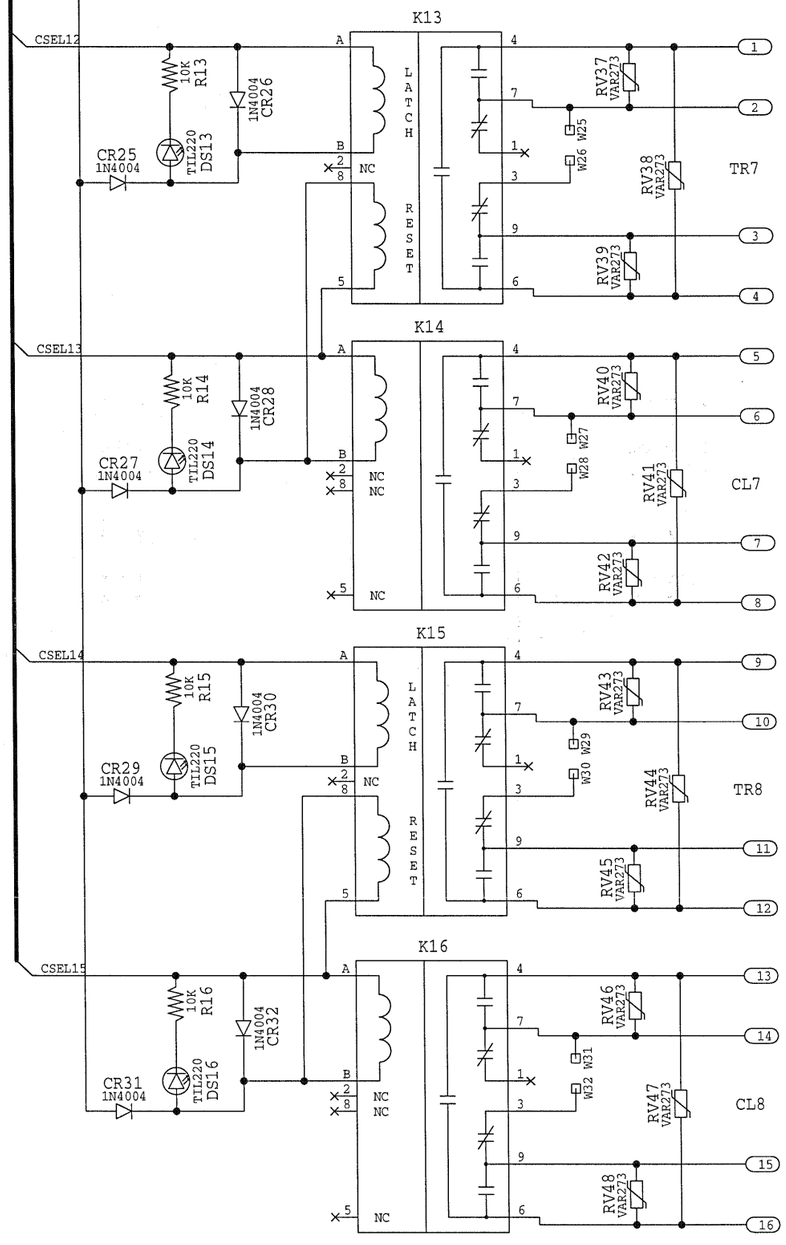
NOTE: MOV's ARE OPTIONAL

FOR LATCHING TYPE RELAY's, RELAYS,
K2,4,6,8,10,12,14,16 ARE NOT POPULATED



NOTE: GND-RING's ARE .200" HOLES FOR CHASSIS GROUND CONNECTIONS
EACH SLOT FOR BOARD MOUNTING ALSO HAS CHASSIS GROUND CONNECTION





SIZE		REV.
B	C3133-002-REV-A	A
SCALE	SHEET 2 OF 2	PCAD # C3133-A2.SCH