Control Loop Design

by Lloyd Dixon

TOPIC 7

Switching Power Supply Control Loop Design

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Summary:

This paper surveys many practical aspects of control circuit design. Topics include: different approaches for achieving Nyquist stability criteria, transient response vs. phase margin, low frequency accuracy vs. the shape of the Bode plot, why it is dangerous to depend on conditional stability, achieving the maximum crossover frequency of a switched loop., other factors which may limit loop bandwidth, sources of error, and where to place the gain needed for correction.

Other practical aspects include large signal behavior and how to minimize offset error delays of compensation capacitors in the feedback path.

Control Loop Basics

The control loop in a high performance switching power supply requires high gain, to achieve good regulation, and high bandwidth, to achieve rapid response to sudden changes of line or load.

Control loop gain inevitably declines at high frequency, limiting bandwidth. The frequency at which the loop gain crosses through 1 (0dB) is defined as the crossover frequency, *fc*. The declining loop gain at high frequency is accompanied by phase lag (in addition to the normal 180° phase shift associated with negative feedback). The amount of additional phase lag is a function of how rapidly the gain drops with frequency. According to Nyquist' stability criteria, *the loop will be unstable if the additional phase lag exceeds 180° at the crossover frequency.*

If the excess phase lag at *fc* is very close to the 180° limit, the loop will be stable but the transient response will exhibit under-damped oscillations (ringing). A clean transient response requires considerably less than 180° excess phase lag at *fc*. The amount less than 180° is referred to as *phase margin*. Thus a phase lag of 117° at *fc* corresponds to a 63° phase margin.

Fig. 1 shows the gain - phase plots of two average current mode control loops and their transient response to a step change in load current. Both loops cross over at 10 kHz.

Bode plots are simplified gain - phase plots that are convenient for depicting the frequency characteristics of a feedback loop.

The 1 POLE loop has one active pole from 10Hz to over 100kHz. Thus the phase lag at *fc* is 90° and the phase margin is also 90°. Note that with the –1 slope associated with a single pole, the gain does not rise rapidly at lower frequencies. The lower

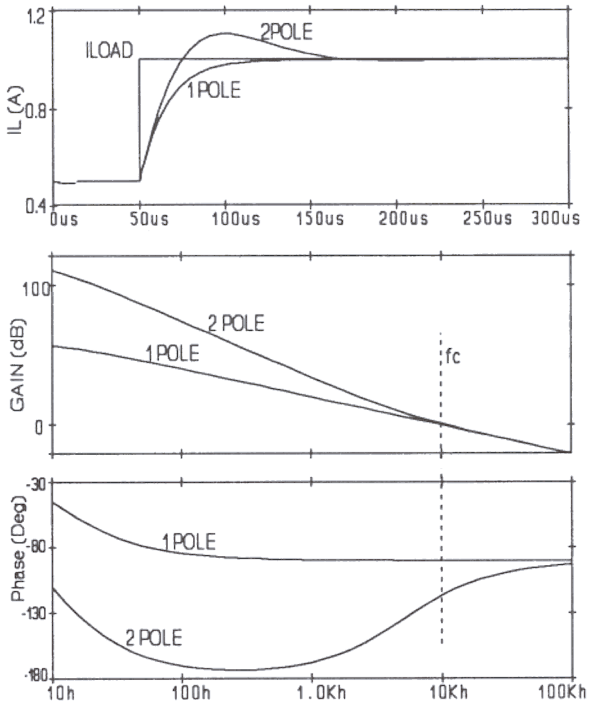

Fig. 1 - Gain - Phase Plot and Transient Response

Control Loop Design

gain/bandwidth will hurt power supply characteristics such as regulation and audio susceptibility. Note also that the transient response is slower. The area between the *ILOAD* step change and the 1 POLE response curve represents a charge deficit in the output capacitor that is never made up, except by the output voltage ultimately sagging and calling for more current.

In the 2 POLE loop, if the two poles were active through and well above *fc* (10kHz), the phase lag at *fc* would approach 180°—almost zero phase margin. The transient response would exhibit severe ringing. But the 2 poles are not active above 5kHz. A zero in the control amplifier causes a −2 to −1 slope transition at *fc*/2. This results in 117° phase lag, or a phase margin of 63°. Below 5kHz (*fc*/2), the −2 slope causes the gain to rise rapidly at lower frequencies, optimizing gain-bandwidth. With the −1/−2 zero transition at *fc*/2, transient response is critically damped—see Figure 1. The initial charge deficit is not only smaller, the slight overshoot compensates precisely for the initial deficit. This is characteristic of a critically damped system.

At frequencies well below the zero at *fc*/2, phase lag does approach 180°, and the phase margin vanishes. This is *desirable* because it is associated with the −2 slope which rises rapidly at lower frequencies, improving gain-bandwidth. 180° phase lag is also *acceptable*. Adequate phase margin is required only at *fc*. The circuit will not misbehave with 180° phase lag at frequencies *below fc*, as long as there is adequate phase margin *at fc*.

Two poles are shown occurring near 10Hz: the power circuit inductance with its series resistance, and the control circuit operational amplifier reaching its gain limit. Loop gain flattens out, and excess phase lag diminishes toward 0°.

Conditional Stability: The criteria for loop stability permits the phase shift to actually *exceed* 180° (negative phase margin) at frequencies below *fc*. This is called "conditional" stability because it depends upon the strict requirement that the phase shift be 180° (preferably much less) at the unity gain crossover frequency. Thus, the 180° limitation applies *only* at *fc* where the gain is 1, not at any lower frequency even though the gain may be high.

It is usually not wise to depend upon conditional stability. Under conditions such as startup or large rapid load changes, operational amplifiers in the loop may be driven "into the stops". This is equivalent to a temporary reduction in loop gain and crossover frequency. If phase shift exceeds 180° at the temporarily lower *fc*, the circuit will likely commence a large signal oscillation from which it cannot recover.

In summary, the gain characteristic should have a −1 (1 pole) slope as it traverses the unity gain crossover frequency. A zero at *fc*/2 will result in a −2 (2 pole) slope at lower frequencies. This will provide optimum bandwidth and critically damped transient response. The phase lag approaches 180° at lower frequencies, but this is quite acceptable. However, it is unwise to go beyond 180° and depend on conditional stability.

With inadequate phase margin, the ringing frequency will be at or near *fc*.

Crossover frequency: The unity gain crossover frequency, *fc*, is usually the best starting point for optimum control loop design, working back toward lower frequencies to obtain the best possible gain-bandwidth.

Theoretically, *fc* of a *linear* closed loop system could be at any frequency, provided the criteria for adequate phase margin are fulfilled. In practice, it becomes necessary to cross over the linear system when cumulative phase shifts of various loop components become too great to compensate. This problem is compounded when gain and phase shift of various loop elements change, sometimes unpredictably, due to tolerances and temperature effects.

Switching power supplies control loops have additional complications that can limit *fc*. The right half-plane zero encountered in the output of continuous mode boost and flyback topologies is not only near-impossible to compensate, it moves in frequency as a function of load. With voltage mode control, loop gain varies as a function of input voltage. With discontinuous operation or with current mode control, voltage loop gain varies with load. All of this can make it extremely difficult to achieve a high *fc* while adhering to Nyquist' stability criteria under all conditions of operation.

One reason current mode control can provide better control loop performance is that the current

loop and the outer voltage control loop are both simplified, making it much easier to achieve high crossover frequency in both loops. For example, in a buck-derived regulator, the current loop has to deal only with the inductor pole, while the output loop deals only with the output capacitor and its variable ESR zero.

Slope limitations: Buck derived topologies are relatively easy to compensate, especially if current mode control is used. A high *fc* could be realized under Nyquist' criteria alone, but another limitation is encountered that is unique to switched loops: After the waveforms applied to the PWM comparator inputs converge, (causing the power switch to turn off), the waveforms should then *cross over* and diverge (or at a minimum coincide). Otherwise, subharmonic oscillation will occur under certain operating conditions. With peak current mode control, slope compensation corrects this problem (and reduces the loop gain). This problem exists in *any* switched loop, but it is more likely to be the limiting factor in buck-derived circuits. The solution requires limiting the control amplifier gain at the switching frequency, which indirectly limits *fc* to 1/3 to 1/10 of *fs*.

Other phase margin considerations: The most usual method of assuring adequate phase margin and clean transient response with minimum loss of gain-bandwidth is to put a control amplifier zero at *fc*/2, making a loop gain slope transition from –2 below *fc*/2 to –1 above. To attenuate switching noise, a control amplifier pole is sometimes added at a frequency above *fc*. This pole converts the –1 slope at *fc* to a –2 slope at higher frequencies. It should be 1 decade above the previously placed zero, and also above $2 \cdot fc$, to maintain adequate phase margin. (Be careful—this high frequency pole may impair response for peak current limiting.)

A completely unique situation arises in the voltage loop of a high power factor preregulator. The loop gain must be very low at $2 \cdot fLINE$ (120Hz) to minimize 2nd harmonic distortion feedback. The crossover frequency, although well below *fLINE*, must be as high as possible to obtain reasonable loop dynamics. The optimum solution is to use a –2 slope *above fc* up to $2 \cdot fLINE$, with a pole slightly above *fc* to transition to a –1 slope *below fc*.

Control Loop Design Examples

Definitions:

Rt: "transresistance"—the translation of inductor current to a voltage, v_i. In its simplest form, *Rt* = current sense resistor *Rs*. With a current transformer, *Rt* = *Rs*/*N*.

Vs Sawtooth voltage, peak-peak

fs Switching frequency

fci Current loop crossover frequency

fcv Voltage loop crossover frequency

Average Current Mode Control Loop

Fig. 2 is the circuit diagram of a buck regulator with an average current mode control loop. Fig. 3 is the small signal equivalent circuit. Fig. 4 is the Bode gain plot of the PWM/power circuit, the current amplifier, and the overall current loop gain.

Conditions:

Vi = 7-14V	*Vo* = 5V	*L* = 10µH
C = 5000µF	*Rc* = .02	*Io* = 15 → 20A
Rt = .05Ω	*Vs* = 5V	*fs* = 100kHz

Description: Referring to Fig. 2, Inductor current I_L is sensed and converted into equivalent voltage v_i by transresistance *Rt*. Current amplifier (CA) amplifies the differential between v_i and current programming voltage *VSET*. The amplified error applied to the PWM comparator controls the duty cycle of the power switch. This in turn controls the average inductor input voltage, changing current until v_i equals *VSET*. I_L then equals *VSET*/*Rt*.

Goal: Obtain the highest crossover frequency, fci, consistent with equal slopes at the PWM comparator inputs during the OFF time, and with a single active pole (-1 slope) at crossover.

Strategy: The PWM/power section has a 1-pole slope above resonance (from the filter inductor). For the overall –1 slope required at crossover, the CA gain must be flat from below *fci* to above *fs*. A zero in the CA makes the transition from –1 to –2 slope below *fci*/2 to achieve low frequency boost, with critically damped transient response.

Implementation:

Sawtooth slope:

$dv_S/dt = Vs/Ts = 5V/10\mu sec = 0.5V/\mu sec$

Inductor current downslope (during OFF time), converted into an equivalent voltage downslope by transimpedance *Rt*:

$$di/dt = Vo/L = 5V/10\mu H = 0.5A/\mu sec$$

$$dv_i/dt = Rt\, di/dt = .05\times 0.5 = .025V/\mu sec$$

Current Amplifier gain for equal slopes at the PWM comparator input:

$$G_{CA} = \frac{v_{CA}}{v_i} = \frac{0.5}{.025} = 20$$

Back off gain by 25% to allow for additional downslope from ESR voltage waveform passed through voltage amplifier. Use $G_{CA} = 15$:

$$Rii = 5k,\ Rfi = 75k$$

Current loop PWM/power section gain (at frequencies above *L-C* series resonance at 712Hz):

$$i_L = \frac{Vin\, d}{\omega L};\quad v_i = Vin\, d\frac{Rt}{\omega L};\quad d = \frac{v_{CA}}{Vs}$$

$$G_P = v_i/v_{CA} = \frac{Vin}{Vs}\,\frac{Rt}{\omega L} = \frac{-j159Vin}{fs}$$

Overall current loop gain:

$$G_I = \frac{159Vin}{f}\cdot 15 = \frac{2385Vin}{f}$$

Set Gain = 1 and *Vin*=7V to find *fci* min.:

$fci = 2385Vin = 16.7kHz$ min at $Vin=7V$

Current Amp. compensation: Zero at *fci*/2 (8kHz)

$$Cfi = \frac{1}{2\pi f Rfi} = \frac{1}{6.28\cdot 8kHz\cdot 75k} = 260pF$$

When the current loop is closed, its gain is a transconductance: $i_L/VSET = 1/Rt$. The closed loop gain is flat until it rolls off at the open loop crossover frequency, *fci*. This characteristic makes it easy to include in the outer voltage loop.

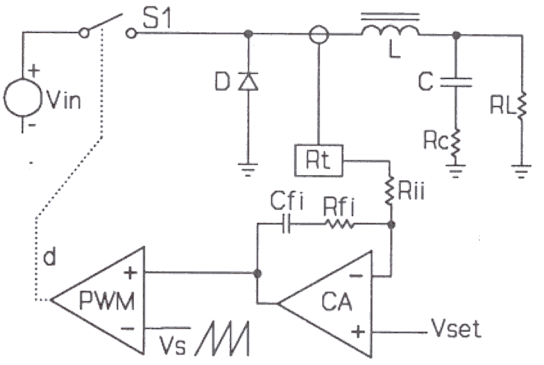

Fig. 2 - Average Current Mode Current Loop

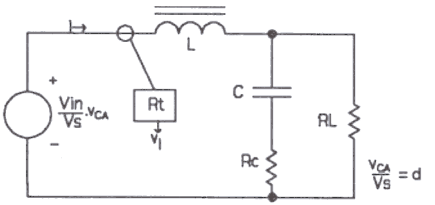

Fig. 3 - Current Loop Small Signal Equiv. Ckt

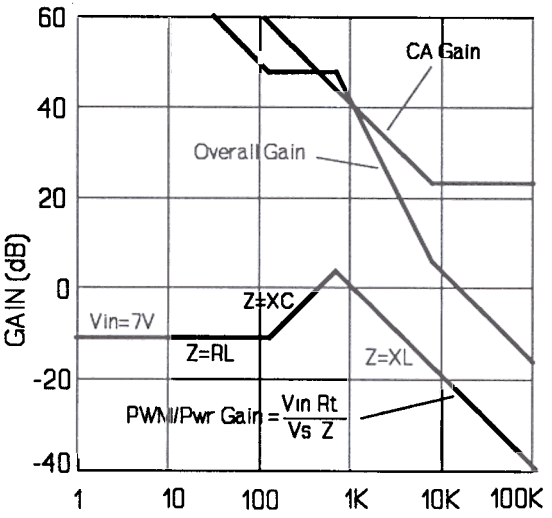

Fig. 4 - Current Loop Bode Plot

Demonstration: Fig. 5 shows the stability and transient response of the current loop with compensation as calculated above. The bottom two curves are the current programming voltage, *VSET*, and v_i, which equals $I_L \times Rt$. The top two curves are the two PWM comparator inputs: sawtooth voltage *Vs*, and the current amplifier output, v_{CA}.

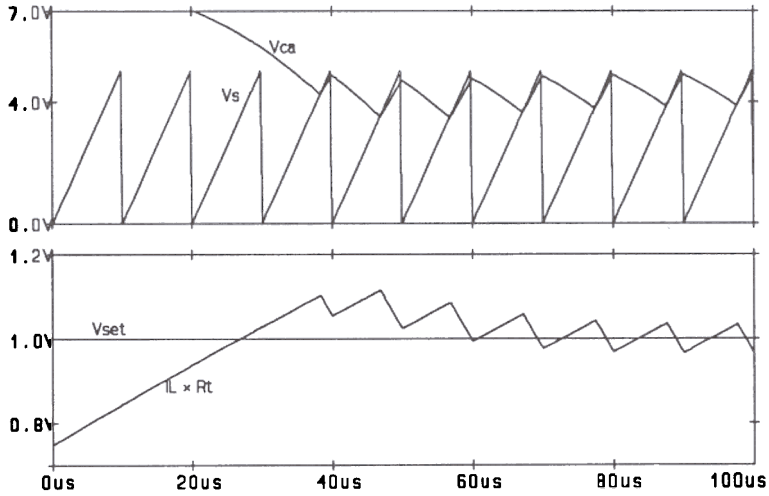

Fig. 5 - Current Loop Waveforms with Current Change

At the beginning of the demonstration, I_L has been regulating at 15A (0.75V across *Rt*). At time 0, *VSET* changes instantaneously from 0.75V to 1V. This new demand for 20A cannot possibly be fulfilled by any control circuit action. The CA output is driven to its 7V limit, calling for the power switch to be fully ON. But it takes 25µsec (several switching periods) for I_L to reach 20A at its max. slew rate of *(Vin–Vo)/L* = 0.2A/µsec. The control loop is temporarily open.

While I_L is slewing from 15A to 20A, the error input to the CA causes feedback capacitor *Cfi* to charge, developing a voltage offset. When I_L reaches 20A, the *Cfi* offset holds the CA output out of the normal PWM input range (see Fig. 5). Thus I_L rises above 20A until the *Cfi* offset is discharged back to normal. This is not an operational flaw—it is actually beneficial. During the initial 25µsec while I_L is low, the output filter capacitor has a charge deficit. The *excess* current after 25µsec rapidly *restores this charge deficit*. If this overshoot did not occur, Vout would sag. The charge deficit would then be restored over a longer time by action of the voltage loop in an actual power supply. The overshoot results in better performance. Note that this is *not* the same as the overshoot associated with critical damping of the current loop. The current loop is in fact open during this time—this is a large signal phenomenon.

Adding the Voltage Loop

Fig. 6 is the circuit diagram of a buck regulator with a voltage control loop added to the average current mode control loop previously discussed. Fig. 7 is the voltage loop small signal equivalent circuit. Fig. 8 is the Bode gain plot of the power circuit (including the closed current loop), the voltage amplifier, and the overall voltage loop gain.

Conditions:

$Vi = 7 \rightarrow 14V$	$Vo = 5V$	$L = 10\mu H$
$C = 5000\mu F$	$Rc = .01–.02$	$Io = 15 \rightarrow 20A$
$Rt = .05\Omega$	$Vs = 5V$	$fs = 100kHz$

Description: Referring to Fig. 6, a voltage error amplifier (VA) replaces *VSET* in Fig. 2. The VA amplifies the error between *Vo* and the 5V reference. The VA output, v_{VA}, programs a constant inductor current according to the transconductance 1/*Rt* of the closed current loop.

Goal: Obtain the highest crossover frequency, *fcv*, consistent with equal slopes at the PWM comparator inputs during the OFF time, and with a single active pole (-1 slope) at crossover.

Strategy: Referring to Fig. 8, the power circuit gain equals the current loop transconductance 1/*Rt* times output impedance *Zo* which varies with

frequency. Current loop transconductance is flat up to *fci* (16.7kHz), where it rolls off with a –1 slope.

The biggest problem is with variation of *Rc*, the output capacitor ESR, and the zero it places in the loop. In this example it is assumed that *Rc* varies within a 2:1 range (.01 to .02Ω). The zero, f_{ESR} ranges between 1.6 and 3.2kHz, which is below the desired crossover frequency, *fcv*. The power circuit gain is flat from f_{ESR} through *fcv* up to min *fci*, the current loop gain roll-off at 16.7kHz.

The VA gain is made flat at switching frequency *fs*. Inductor ripple current flowing through ESR *Rc* generates a sawtooth waveform which is amplified and inverted by the VA and applied to the CA non-inverting input. This sawtooth is *in phase* with the sawtooth across *Rt* at the other CA input. Thus the OFF-time slope at the PWM comparator input is worsened. An allowance was made for this in the CA gain, but the VA output slope must be limited to 1/2 the slope across *Rt*, limiting VA gain at *fs*.

The VA gain has a zero at *fci* (16.7kHz), below which it has a –1 slope. Thus the overall voltage loop gain has a –1 slope from *fc* down to f_{ESR}. Crossover *fcv* varies with Rc from 4 to 8kHz. Below f_{ESR}, the overall voltage loop gain has a –2 slope. This boosts the voltage loop gain at lower frequencies, but also makes it important that max f_{ESR} is below minimum *fcv*.

There are two other alternatives:

1. Wide ESR zero range. If max f_{ESR} is closer to min *fci* than the above example, it will be impossible to safely cross over anywhere above f_{ESR}. VA gain must be very low and flat from well below f_{ESR} all the way up to *fs*. Overall gain rises only as the power circuit gain rises below min f_{ESR}, resulting in *fcv* way below min f_{ESR}. This is a most undesirable situation.

2. Min ESR zero above desired *fcv*. (this might be the case with ceramic output filter capacitors.) The power circuit gain has a –1 slope from the $R_L C$ pole (127Hz) all the way up to *fci*. The VA gain must be flat above *fcv*/2, and is limited by slope considerations. A zero in the VA gain gives the overall gain a –2 slope below *fcv*/2. This desirable situation can be created with electrolytic output filter capacitors by using a much higher voltage rating than necessary. (For the same size and cost, the higher voltage capacitor has the same ESR but lower capacitance, thus higher ESR zero frequency.) The penalty is a lower output surge impedance less capable of standing up to a large signal incident such as a sudden large load change.

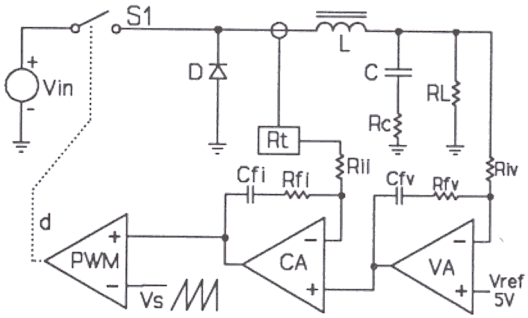

Fig. 6 - Average Current Mode Voltage Loop

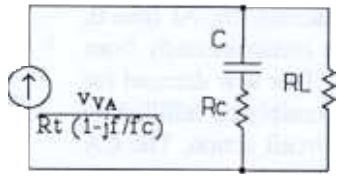

Fig. 7 - Voltage Loop Small Signal Equiv. Ckt

Implementation:

Inductor current downslope (during OFF time), converted into an equivalent voltage downslope by *Rc*, the output capacitor ESR:

$$di/dt = Vo/L = 5V/10\mu H = 0.5A/\mu sec$$

$$dv_v/dt = ESR\, di/dt = .02 \times 0.5 = .01\, V/\mu sec$$

Because of slope limitations at the PWM comparator, the sawtooth slope at the VA output must be limited to 1/2 the slope across *Rt* (*dvi/dt*). Thus the voltage amplifier gain at *fs* is:

$$G_{VA} = \frac{v_{VA}}{v_o} = \frac{dvi/dt}{2\,dvv/dt} = \frac{.05}{2\times.02} = 1.2$$

Riv = 10k, *Rfv* = 12k

A zero is put in the VA gain where current loop transconductance rolls off at min *fci* (16.7kHz):

$$Cfv = \frac{1}{2\pi f_{ZERO} Rfv} = \frac{1}{6.28 \cdot 16.7kHz \cdot 12k} = 800pF$$

The VA gain below this zero is:

$$G_{VA} = \frac{v_{VA}}{v_O} = \frac{-j1.2f_{ZERO}}{f} = \frac{-j20{,}000}{f}$$

The power circuit gain between the *ESR* zero frequency and fci (16.7kHz) is:

$$\frac{v_O}{v_{VA}} = \frac{Rc}{Rf} = \frac{.02}{.05} = 0.4$$

Overall voltage loop gain, and crossover freq., *fcv*:

$$G_V = \frac{20{,}000}{f} \cdot 0.4 = \frac{8000}{f}\ ; \quad fcv = 8\text{kHz}$$

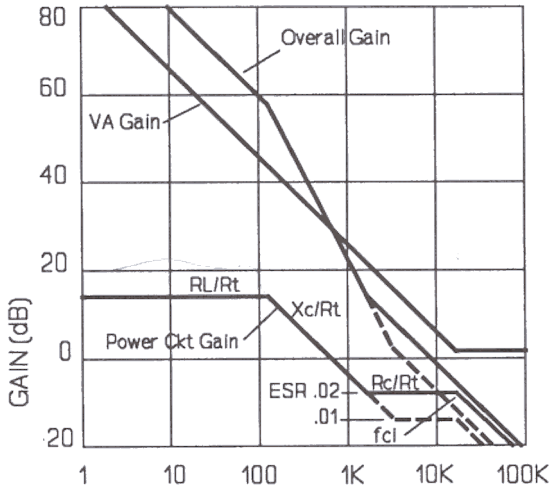

Fig. 8 - Voltage Loop Bode Plot

Demonstration: Fig. 9 shows the stability and transient response of the voltage loop. The bottom two curves are the voltage eror amplifier output, v_{VA}, and v_i, which equals $I_L \times Rt$. The top two curves are the two PWM comparator inputs: sawtooth voltage Vs, and the current amplifier output, v_{CA}. The output voltage is not shown. (The charge deficit vs. time revealed in the current waveform causes a max *Vout* deviation of only 13mV.)

This demonstration is identical to the earlier current loop demonstration, except that the voltage at the CA input which programs the current is the output of the voltage error amplifier, v_{VA}. During the time the control circuit is "in the stops" while the inductor current slews to its new value, the feedback capacitor *Cfv* around the VA also charges to a voltage offset. This further increases the I_L overshoot, which now almost exactly cancels the earlier charge deficit.

After the current transition from 15A to 20A load has been completed, a 2:1 line voltage change is demonstrated. At 100µsec, the input voltage is changed instantaneously from 7V to 14V. Note how the duty cycle is reduced in the very first switching cycle. The longer OFF time increases inductor ripple current and the V_{CA} ripple, but the slopes at the PWM input remain nearly coincident as seen in the upper waveforms.

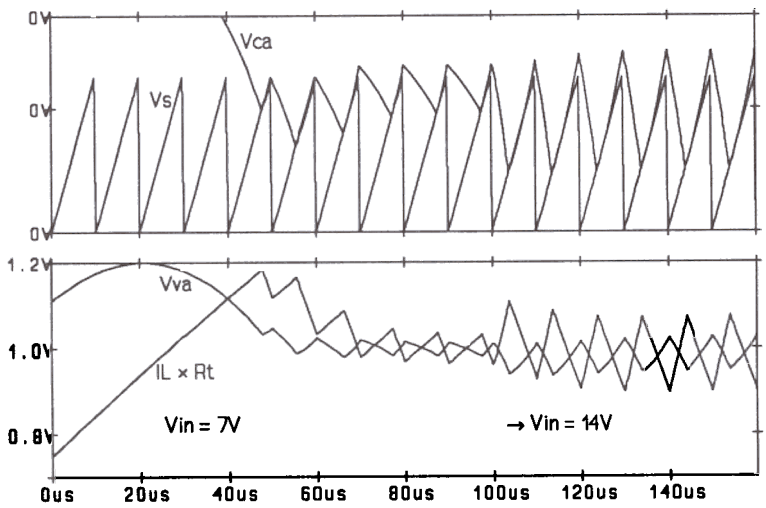

Fig. 9 - Waveforms with Load and Line Changes

Flyback with Average Current Mode Control

Fig. 10 is the circuit diagram of a flyback regulator operating in the continuous inductor current mode. Fig. 11 is the corresponding Bode gain plot.

Conditions:

$Vi = 6 \rightarrow 12V$	$Vo = 5V$	$L = 1.375\mu H$
$C = 50{,}000\mu F$	$Rc = .002$	$Io = 20A$
$Rt = .05\Omega$	$Vs = 5V$	$fs = 100kHz$

Description: The flyback topology is popular because of its simplicity, having one magnetic device which is also capable of providing isolation. Discontinuous flyback operation is simple, but suffers from high peak secondary current—80A for a 20A output. When the power switch turns off, 80A peak is suddenly delivered to the output, putting a tremendous burden on the output filter capacitors. Continuous mode operation can almost halve this peak current, easing the burden on the output capacitors.

The big problem with continuous mode flyback circuits is the right half-plane (RHP) zero which appears in the loop gain characteristic. The crossover frequency, fc must be well below the RHP zero frequency. This is more difficult because the RHP zero moves considerably with load and with Vin. The designer's dilemma is that if the inductor is made large to remain in continuous conduction at light loads, the RHP zero frequency is very low. If the inductor is made small, the circuit cannot be operated with light loads, because the loop gain drops too much when the mode boundary is crossed.

Average current mode control helps solve this problem in several ways: (1) It controls average output (diode) current, thus the RHP zero is dealt with and "buried" in the current loop. (Conventional current mode control controls the wrong current—inductor current—and does not deal with the RHP zero. (2) Because of the gain provided by the current error amplifier, the current loop can operate across the mode boundary and maintain acceptable regulation. This allows the inductor to be smaller (limited only by higher peak current considerations), which raises the RHP zero frequency permitting a higher crossover frequency.

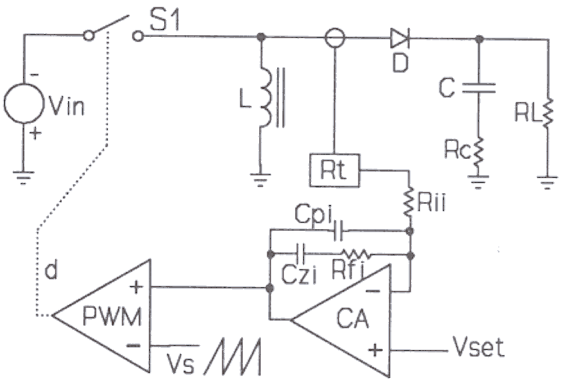

Fig. 10 - Flyback Avg. Output Current Control

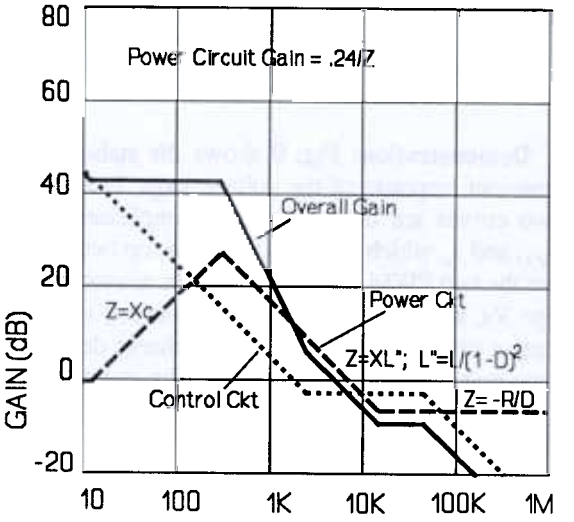

Fig. 11 - Flyback Bode Plot

There are two unique considerations in the design of the average current mode control loop for the flyback circuit. First, the *diode* current is being sensed, averaged and controlled, not the inductor current. The diode current is a large amplitude essentially rectangular waveshape. It is necessary to integrate this waveform to obtain its average current. The integrating capacitor, *Cpi*, added to the CA feedback network must be small or it would hurt the loop bandwidth. The CA output has a sawtooth ripple component from the integration, analogous to the sawtooth inductor ripple current.

Second, the sawtooth waveform at the CA output

is 180° out of phase with the sawtooth waveform seen in the buck regulator. Rather than concern about too much slope during the OFF time, the concern now is with the ON–time slope. The worst–case ON–time slope should be 1/2 the slope of sawtooth voltage *Vs*.

Implementation:

Sawtooth slope:

$$dv_S/dt = Vs/Ts = 5V/10\mu sec = 0.5V/\mu sec$$

During the ON time, the voltage across trans-resistance *Rt* is zero, so V_{SET} is across the 50K integrator input resistor *Rii*. The integrator is set up for $dv_{CA}/dt = \frac{1}{2}dVs/dt$ under worst case condition of $V_{SET}max = 1.2V$ (corresponding to current limit).

$$\max I_{Rii} = \frac{V_{SETmax}}{Rii} = \frac{1.2V}{50K} = .024mA$$

$$Cpi = \frac{\max I_{Rii}\, 2T_s}{V} = 100pF$$

The minimum RHP zero frequency occurs with min *Vin* and min load resistance. (D = *Vo/(Vi+Vo)*)

$$f_{RHPZ} = \frac{(1-D)^2 R_L}{D \quad L} = 14.5\,\text{kHz}$$

Since there is so much excess phase shift associated with the RHP zero, we will steer clear of it and cross over at 5 kHz. The PWM/power circuit gain at 5kHz is:

$$\frac{v_i}{v_{CA}} = \frac{Vin}{V_S}\frac{Rt}{D(1-D)\,Z}; \quad \text{where } Z = X_L'' = \frac{2\pi fL}{(1-D)^2}$$

$$\frac{v_i}{v_{CA}} = .39$$

The CA gain must be flat from *fc*/2 to well above crossover to maintain an overall -1 slope. To cross over at 5kHz, the CA gain must be the reciprocal of the PWM/power circuit gain:

$$\frac{V_{CA}}{V_i} = 1/1.39 = 0.719$$

$$Rfi = 0.719\,Rii = 0.719 \times 50K = 36K$$

A pole at *fc*/2 (2500Hz) provides a -2 slope for low frequency gain boost:

$$Cfi = \frac{1}{2\pi f Rfi} = 1768\,\text{pf}$$

Some Practical Control Loop Problems

Compensation Capacitor Problems: It is usually essential to use capacitors in compensation networks around the error amplifiers in the control loop. Compensation capacitors which break the DC path between op-amp input and output operate with a DC bias voltage. This is not a problem under strictly small-signal operating conditions. But when line or load changes occur, or during startup, the amplifier output voltage must change. This requires a change in the DC bias across the series compensation capacitors. The charging current required can cause significant errors or delays in the transient response of the power supply.

Small capacitors with short time constants which provide high frequency compensation (such as adequate phase margin at crossover) don't usually cause problems. The problem is with larger capacitors (with long time constants) which are put in series with the feedback path around the amplifier for two reasons: (1) To break open a DC path around the amplifier which is causing a DC offset error, or (2) To boost the low frequency gain to obtain near-perfect regulation.

Transient behavior: What is the good of improving the DC regulation if the transient response is hurt? (The answer might be that your customer only looks at DC regulation.) Consider what happens with a significant and rapid load change. Without the series capacitor, there will be a DC path around the amplifier and finite DC gain. Assume that the output voltage changes from 5.1V with light load to 5.0 volts at full load. A series capacitor provides a low frequency zero which greatly improves regulation. Assume perfect regulation: 5.0V at light and at full load. But when the load suddenly decreases, Vout *will* swing momentarily to 5.1V, then return precisely to 5.0V. Later, when the load suddenly increases, Vout *will* swing

momentarily to 4.9V, then return precisely to 5.0V. The output voltage envelope is twice as great with the capacitor as without it.

So think twice about adding a low frequency zero just for the sake of DC regulation. If the gain is too low without the boost capacitor, look for ways to optimize the loop gain by some other method, such as optimizing the compensation scheme.

If a series capacitor is essential, make sure the output voltage swing of the op-amp is restricted in some way. Otherwise, the series capacitor can charge to a large offset voltage during startup or other transient conditions, thus taking a longer time to recover. If the op-amp output is not internally clamped, apply an external clamp. A transconductance amplifier is easy to clamp directly across the output. Any amplifier can be clamped with a Zener diode from output to inverting input. Leave 1 or 2 Volts headroom for AC components riding on the control signal.

DC current offsets: When there is DC resistance between op-amp input and output, there will inevitably be DC error caused by current flow through this resistance. In exercising control throughout the full range of operating conditions, the op-amp output must swing over a range of voltages. The current offset error is minimized by biasing the op-amp inputs at a DC voltage exactly in the middle of this output voltage range. There will be no current offset error when the output is in the middle of this range, but there will be ± regulation error at the operating extremes.

For example, if the control IC permits, divide down the reference voltage applied to the non-inverting op-amp input so that its voltage is at the mid-range of the output swing. This is a good practice even when a series boost capacitor is used, because the capacitor bias voltage will be close to zero, requiring no time to charge at start-up.

If the op-amp voltage is fixed internally, consider canceling the mid-range DC offset current by providing a compensating current to the op-amp input.

Amplifier bandwidth limits: Needless to say, if the compensation scheme requires more gain at high frequency than the op-amp can provide, there's a problem. One such problem area is the current amplifier in an average current mode control loop. In order to minimize power dissipation in the current sense resistor, it is desirable to use a very small resistance value. Although the op-amp input offset spec may be low enough to permit a very small sense voltage with reasonable accuracy, the small sense voltage will require more op-amp gain-bandwidth than nay be available..

Noise filtering: High frequency poles are often added in a control loop to attenuate noise spikes that might otherwise propagate through the loop, causing spurious turn-on and unpredictable operation. In general the pole frequencies should be at least 2-3 times *fs*, to avoid signal distortion and impaired response to sudden overloads, for example. This is especially important with conventional peak current mode control, which is very noise sensitive, but also sensitive to the effects of waveform distortion caused by over-filtering.

References:

[1] R. D. Middlebrook, "Topics in Multiple-Loop Regulators and Current-Mode Programming," *IEEE PESC*, June, 1985

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