United Electronic Industries

The High-Performance Alternative

DNx-AI-204

—

User Manual

24-channel 0-20/4-20/±24 mA input board
for the PowerDNA Cube and RACK series chassis

August 2018

PN Man-DNx-AI-204

CE

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Table of Contents

List of Figures

Chapter 1 Introduction

This document outlines the feature set and use of the DNx-AI-204, an 18-bit, 24-channel, 0-20/4-20/±24 mA analog-to-digital boards.

This chapter contains the following information for the AI-204:

- Organization of This Manual (Section 1.1)
- AI-204 Board Overview (Section 1.2)
- Features (Section 1.3)
- Specification (Section 1.4)
- Device Architecture (Section 1.5)
- Indicators (Section 1.6)
- Connectors and Wiring (Pinout) (Section 1.7)
- PowerDNA Explorer for AI-204 (Section 1.8)

1.1 Organization of This Manual

This AI-204 User Manual is organized as follows:

- **Introduction**
  Chapter 1 provides an overview of DNx-AI-204 analog input board features, device architecture, connectivity, and logic.
- **Programming with the High-Level API**
  Chapter 2 provides an overview of the how to create a session, configure the session, and read input on the AI-204 with the UEIDAQ High-Level Framework API.
- **Programming with the Low-Level API**
  Chapter 3 is an overview of low-level API commands for configuring and using the AI-204.
- **Appendix A - Accessories**
  This appendix provides a list of accessories available for use with the AI-204 board.
- **Index**
  This is an alphabetical listing of the topics covered in this manual.

NOTE: A glossary of terms used with the PowerDNA Cube/RACK and I/O boards can be viewed and downloaded from www.ueidaq.com.

Manual Conventions

To help you get the most out of this manual and our products, please note that we use the following conventions:

Tips are designed to highlight quick ways to get the job done or to reveal good ideas you might not discover on your own.

NOTE: Notes alert you to important information.

CAUTION! *Caution advises you of precautions to take to avoid injury, data loss, and damage to your boards or a system crash.*

Text formatted in **bold** typeface generally represents text that should be entered verbatim. For instance, it can represent a command, as in the following example: “You can instruct users how to run setup using a command such as **setup.exe**.”

Bold typeface will also represent field or button names, as in “Click **Scan Network**.”

Text formatted in `fixed` typeface generally represents source code or other text that should be entered verbatim into the source code, initialization, or other file.

Before you begin:

Before plugging any I/O connector into the Cube or RACK chassis, be sure to remove power from all field wiring. Failure to do so may cause severe damage to the equipment.

No HOT SWAP

Always turn POWER OFF before performing maintenance on a UEI system. Failure to observe this warning may result in damage to the equipment and possible injury to personnel.

Usage of Terms

Throughout this manual, the term “Cube” refers to either a PowerDNA Cube product or to a PowerDNR RACKtangle™ rack mounted system, whichever is applicable. The term DNR is a specific reference to the RACKtangle, DNA to the PowerDNA I/O Cube, and DNx to refer to both.

1.2 AI-204 Board Overview

The DNx-AI-204 boards are 24-channel, 0-20/4-20 mA current input boards.

DNA-AI-204, DNR-AI-204, and DNF-AI-204 boards are compatible with the UEI Cube, RACKtangle, and FLATRACK chassis respectively. These board versions are electronically identical but differ in mounting hardware. The DNA version is designed to stack in a Cube chassis. The DNR/F versions are designed to plug into the backplane of a RACK chassis.

1.2.1 Input Current & Resolution

The AI-204 boards support 0-20/4-20/±24 mA input ranges. Programmable gains of between 1 and 10 combined with the board's 18-bit analog-to-digital converter provide resolutions as low as 19.1 nA.

1.2.2 Sample Rate & Sample Averaging

The DNx-AI-204 provides sample rates as high as 1000 samples per second on each channel (24 kS/s aggregate). The AI-204 is designed with an oversampling engine, which allows the board to automatically acquire as many samples as possible for the given gain/speed and average them, dramatically improving noise immunity.

1.2.3 AutoZero

The DNx-AI-204 also provides automated offset compensation, which removes offset fluctuations over temperature and/or time. This allows reduction of the temperature drift to a few microamps over the full specified range.

1.2.4 Isolation & Environmental Conditions

The DNx-AI-204 offers 350 V_{rms} of isolation between the board and other I/O boards as well as between the I/O connections and the chassis. Like all UEI DNx series I/O boards the DNx-AI-204 offers operation in extreme environments and has been tested to 5g vibration, 100g shock, from -40 to +85 °C temperatures and at altitudes up to 70,000 feet.

1.2.5 Accessories

The AI-204 is supported by a variety of cable and screw terminal options.

For those wishing to create their own cables, all connections are through a standard 62-pin "D" connector allowing OEM users to build custom cabling systems with standard, readily available components.

1.2.6 Software Support

The DNx-AI-204 series includes software drivers supporting all popular operating systems including Windows, Linux, QNX, VxWorks, and most other popular real-time operating systems. Windows users may take advantage of the powerful UEIDAQ Framework which provides a simple and complete software interface to popular Windows programming languages and data acquisition and control applications (e.g., LabVIEW, MATLAB).

Software support includes access to an extensive set of example programs.

1.3 Features

The AI-204 boards include the following features:

- DNx-AI-204 for use in “Cube”, RACKtangle®, and FLATRACK™ I/O chassis
- 24 differential analog input channels
- Maximum sampling rate of 1000 Hz per channel
- 18-bit resolution
- ± 3 µA accuracy
- 350 V_{rms} Isolation
- Dynamic autozero support
- Embedded averaging engine
- Designed to withstand 5g Vibration, 50g Shock, -40 to +85°C Temperature, and Altitude up to 70000 ft or 21000 meters

1.4 Specification

The technical specifications for the DNx-AI-204 board are listed in **Table 1-1**.

Table 1-1 . DNx-AI-204 Technical Specifications

Analog Inputs	
Number of channels	24 fully differential current inputs
Input configuration	Multiplexed
ADC resolution	18 bits
Sampling rate	1000 samples/s per channel, maximum (24 kS/s aggregate)
Input Ranges	0-20 / 4-20 / ±24 mA
Input resistance	100 Ω ± 15 Ω
Gains	1, 2, 5, 10
Minimum resolution	191 nA (Gain = 1), 95.4 nA (Gain = 2), 38.1 nA (Gain = 5), 19.1 nA (Gain = 10)
Input accuracy (Gain = 1, sample rate 250 samples/sec or less)	±3 µA at 25 °C ±5 °C ±30 µA over full temp range (worst case) ±5 ppm / °C (typical)
Input accuracy (Gain = 1, sample rate >250 samples/sec)	±12 µA at 25 °C ±5 °C ±45 µA over full temp range (worst case) ±10 ppm / °C (typical)
Input bias current	±5 nA max, ±0.5 nA typical
Common mode rejection	96 dB typical
Common mode range	-5 V to + 25 V
Power supply rejection	> 120 dB
Isolation	350 Vrms
Overvoltage protection	-55V to +55V
General Specifications	
Operating temperature	tested -40 °C to +85 °C
Vibration *IEC 60068-2-6* *IEC 60068-2-64*	5 g, 10-500 Hz, sinusoidal 5 g (rms), 10-500 Hz, broad-band random
Shock *IEC 60068-2-27*	100 g, 3 ms half sine, 18 shocks @ 6 orientations 30 g, 11 ms half sine, 18 shocks @ 6 orientations
Humidity	0 to 95%, non-condensing
Power consumption	2.0 W max
MTBF	540,000 hours

1.5 Device Architecture

Figure 1-1 is a block diagram of the architecture of the AI-204 board.

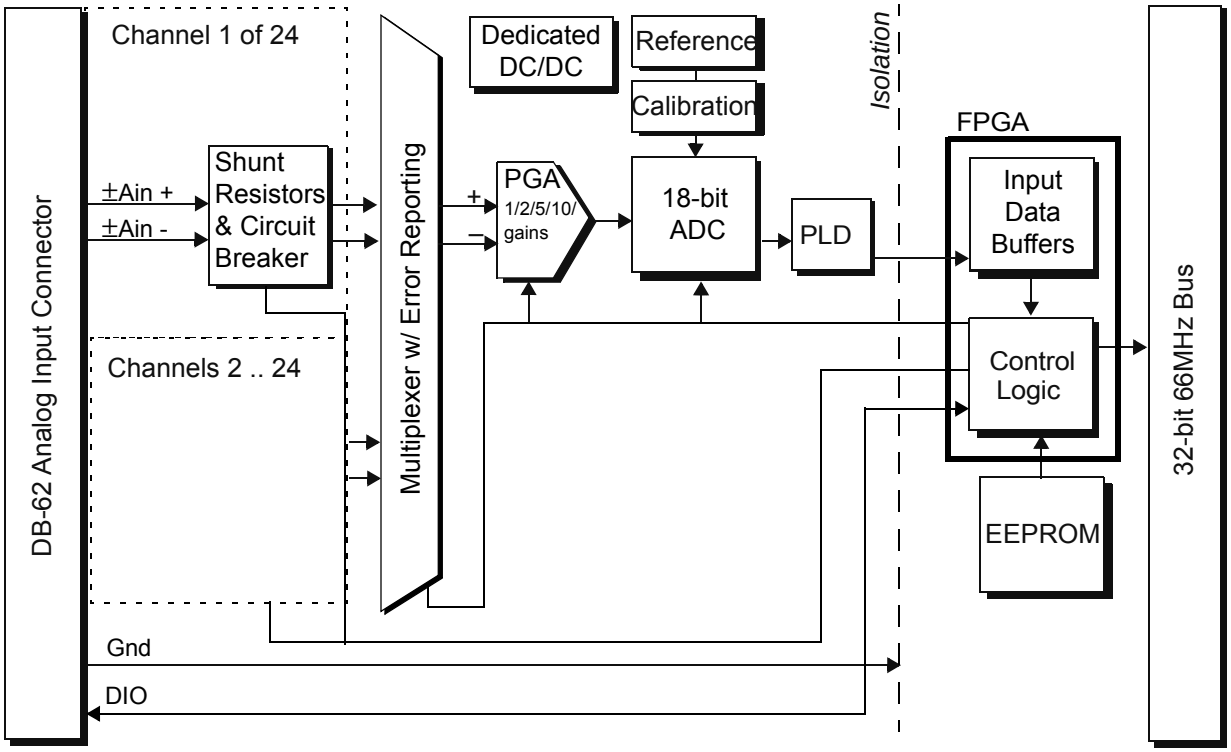

Figure 1-1 Block Diagram of the AI-204 Board

The AI-204 has twenty-four differential input channels designed for analog current measurement with 18-bit resolution.

Differential input lines (Ain+ and Ain- in **Figure 1-1**) of each channel enter through the DB-62 connector pins into a circuit breaker and shunt resistors.

1.5.1 Circuit Breakers, Multiplexer & Program-mable Gain

The circuit breaker at the input of each channel is enabled by default.

Control logic schedules the sequencing of ±Ain input lines of each channel and ground reference to sequentially pass through the multiplexer. Channel data can be optionally gained using the precision programmable gain amplifier (PGA).

The AI-204 supports 4 user-programmable gains: 1, 2, 5, and 10x gains.

Input ranges are listed below:

Gain	Input Range [mA]
1	± 24 mA
2	± 12.5 mA
5	± 5.0 mA
10	± 2.5 mA

If the input current exceeds the input range for longer than 100 ms, then the circuit breaker will disconnect the circuit.

Users can reconnect circuit breakers via Framework or low-level function calls.

Clocks, ADC and Circuit Breakers When Using an External Clock

By default, the AI-204 uses an on-board clock source that is constantly running to read the ADC and provide circuit breaker capabilities.

If you are using an off-board clock (e.g., if you are synchronizing to a 1PPS or IEEE-1588 PTP time source), the ADC and the circuit breaker protection will be disabled when you define your clocks for the AI-204 because all clocks start synchronously. The ADC and circuit breaker protection are re-enabled when the AI-204 receives a trigger.

For more information about the code used to define AI-204 clocks for 1PPS / PTP synchronization:

- When programming with the low-level API, refer to the “PowerDNA 1PPS / PTP Synchronization” section of the *PowerDNA API Reference Manual.* See the `DqSyncDefineLayerClock()` API.
- When programming with the high-level Framework, refer to the “Synchronization using the UeiDaq framework” chapter in the *UeiDaq Framework User Manual*. See the API in the “Creating I/O sessions” subsection.

1.5.2 Control Logic

The multiplexer control, gain control, and ADC clocking control and data lines are managed by a programmable logic device (PLD) which is wired through an isolation barrier to the board’s main controller.

The PLD is responsible for acquiring ADC data from all user-configured channels and manages selecting the next channel using the multiplexer, setup of settling timing delays, configuring each channel’s gain and averaging the ADC data with lower data rates getting more samples per average.

The resulting data is passed into the main controller’s input data buffer at a maximum rate of up to 1000 samples per second. An FPGA based 128 sample moving average is available in point-by point mode.

In addition to analog inputs AIn+ and AIn-, the board also has ground reference lines and digital I/O lines. Each digital I/O line is wired through isolation directly to the main controller: DIO0/1 are inputs, DIO2 is an output.

1.5.3 Autozero

The DNx-AI-204 provides automated offset autozero compensation, which removes any offset fluctuations for every signal reading when running the device over temperature and over time. This reduces temperature drift to a few microvolts over the full specified range.

Autozero is enabled by default. When enabled, internal references are sampled and measurements are stored for the autozeroing calculation. The firmware schedules the sampling of the internal reference for the different gains programmed through the channel multiplexer automatically.

1.5.4 Timestamping

Users can optionally timestamp the acquired samples. The timestamp will be stored as the first or last entry in the user-defined list of channels to acquire. Whether to store the timestamp in the first position or in the last position is user-programmable.

1.6 Indicators

The indicators on the AI-204 front panel are described in **Table 1-2** and illustrated in **Figure 1-2**.

Table 1-2 AI-204 Indicators

LED Name	Description
RDY	Indicates board is powered up and operational
STS	Indicates which mode the board is running in: • **OFF**: Configuration mode (e.g., configuring channels, running in point-by-point mode) • **ON**: Operation mode (e.g., running in ACB, DMap, or VMap mode)

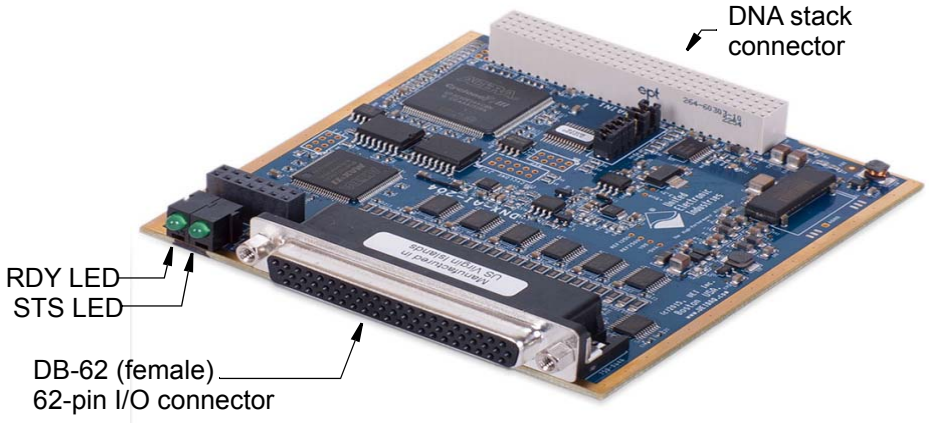

Figure 1-2 DNA-AI-204 Analog Current Board

1.7 Connectors and Wiring (Pinout)

Refer to **Figure 1-3** below for the AI-204 pinout.

Note: Do not connect to any pins marked as Reserved.

62	AIN0+	42	AGND	21	RESERVED
61	AIN0-	41	AIN1-	20	AIN1+
60	AIN3+	40	AIN2-	19	AIN2+
59	AIN3-	39	AIN4-	18	AIN4+
58	AIN6+	38	AIN5-	17	AIN5+
57	AIN6-	37	AIN7-	16	AIN7+
56	AIN9+	36	AIN8-	15	AIN8+
55	AIN9-	35	AIN10-	14	AIN10+
54	AIN12+	34	AIN11-	13	AIN11+
53	AIN12-	33	AIN13-	12	AIN13+
52	AIN15+	32	AIN14-	11	AIN14+
51	AIN15-	31	AIN16-	10	AIN16+
50	AIN18+	30	AIN17-	9	AIN17+
49	AIN18-	29	AIN19-	8	AIN19+
48	AIN21+	28	AIN20-	7	AIN20+
47	AIN21-	27	AIN22-	6	AIN22+
46	DIO0	26	AIN23-	5	AIN23+
45	AGND	25	RESERVED	4	RESERVED
44	DIO2	24	AGND	3	RESERVED
43	AGND	23	AGND	2	DIO1
		22	RESERVED	1	RESERVED

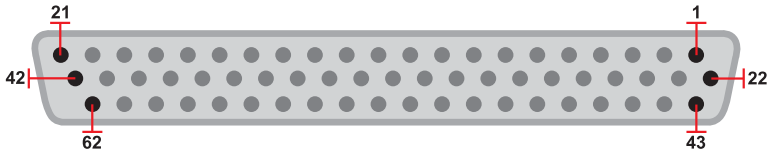

Figure 1-3 Pinout Diagram of DNx-AI-204 Analog Input Board

1.8 PowerDNA Explorer for AI-204

PowerDNA Explorer is a GUI-based application for communicating with your RACK or Cube system. You can use it to start exploring a system and individual boards in the system. PowerDNA Explorer is provided in the installation directory.

Figure 1-4 shows the PowerDNA Explorer main window for the AI-204.

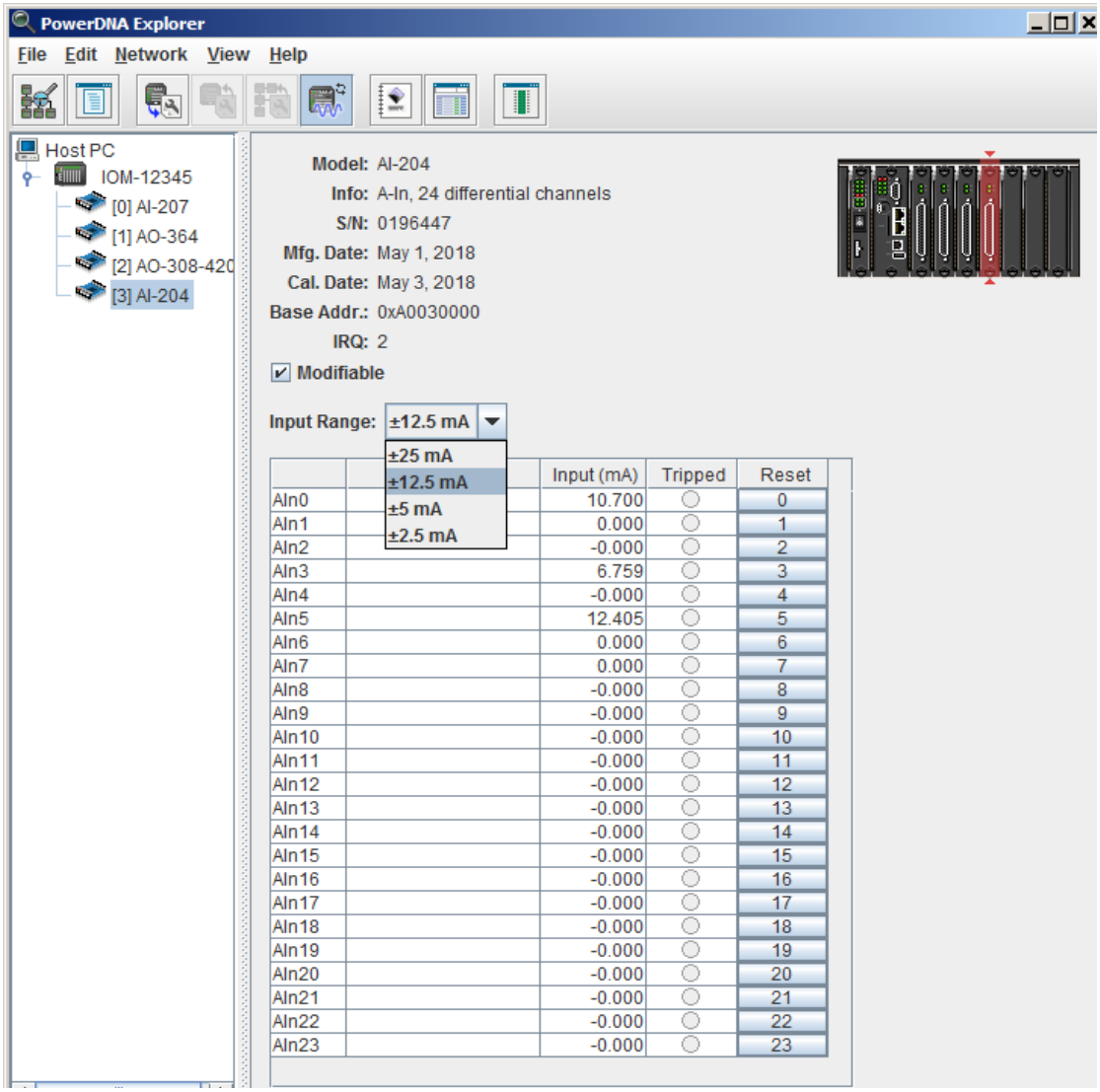

Figure 1-4 PowerDNA Explorer Display for the AI-204 Board

To update the expected input range, select `±25mA, ±12.5mA, ±5mA or ±2.5mA` from the **Input Range** pulldown menu. If the channel receives currents outside of the range you select, the circuit breaker will trip.

The PowerDNA Explorer main window displays input current readings and contains the following columns (refer to image on previous page):

- **AIn*x***: The channel number
- **Name**: A name or note that you wish to give to the channel
- **Input (mA):** Input current reading (in mA)
- **Tripped**: Circuit breaker tripped indicator
- **Reset**: Circuit breaker reset (click to reengage circuit breaker)

To read current values, click the **Read Input Data** button in the toolbar, or select *Network >> Start Reading Input Data* from the menu bar.

Chapter 2 Programming with the High-Level API

This chapter contains the following information about using the UeiDaq Framework High-Level API to control the AI-204:

- About the High-level Framework (Section 2.1)
- Configuring the Resource String (Section 2.2)
- Configuring the Input (Section 2.3)
- Configuring and Using Circuit Breakers (Section 2.4)
- Configuring the Timing (Section 2.5)
- Reading Data (Section 2.6)
- Cleaning-up the Session (Section 2.7)

2.1 About the High-level Framework

UeiDaq Framework is object oriented and its objects can be manipulated in the same manner from different development environments, such as Visual C++, Visual Basic, or LabVIEW.

UeiDaq Framework is bundled with examples for supported programming languages. Examples are located under the UEI programs group in:

- *Start » Programs » UEI » Framework » Examples*

The following sections focus on the C++ API, but the concept is the same no matter which programming language you use.

Please refer to the “UeiDaq Framework User Manual” for more information on use of other programming languages.

2.2 Configuring the Resource String

UeiDaq Framework uses resource strings to select which device, subsystem, and channels to use within a session. The resource string syntax is similar to a web URL:

```
<device class>://<IP address>/<Device Id>/<Subsystem><Channel list>
```

For the AI-204, the device class is **pdna**. The following syntax examples are of resource strings that define analog input lines 0,1,2,3 on device 1 at IP address 192.168.100.2:

- “`pdna://192.168.100.2/Dev1/Ai0:3`” (as a range)
- “`pdna://192.168.100.2/Dev1/Ai0,1,2,3`” (as a list)

NOTE: Timestamps may also be acquired by adding a `ts` channel as the last channel in the resource string.
For example: “`pdna://192.168.100.2/dev0/Ai0:3,ts`”.
The time unit for the acquired timestamp is seconds.

2.3 Configuring the Input

The `CreateAICurrentChannel()` method is used to configure one or more current input channel(s) for current measurements:

```
// Create an AI channel for current measurement
aiSession.CreateAICurrentChannel(
                        “pdna://192.168.100.2/Dev0/Ai0,1”,
                        minAmps, maxAmps, enableCB, inputMode);
```

The `CreateAICurrentChannel` method configures the following parameters:

- **Minimum range**: specifies the lowest current to be measured (f64)
- **Maximum range**: specifies the highest current to be measured (f64)
- **Circuit breaker**: specifies whether the circuit breaker is explicitly enabled, explicitly disabled, or set from a setting stored in the device's EEPROM (enumerated type, see Section 2.4.1)
- **Input mode**: set the input mode to differential: `UeiAIChannelInputModeDifferential`

The input gain is automatically selected to fit the specified input range.

For example, the AI-204 supports four gains:

Gain	Current Range
1	± 24 mA
2	± 12.5 mA
5	± 5.0 mA
10	± 2.5 mA

Table 2-1 AI-204 Gains and Input Current Ranges

Specifying an input range of ±1 mA will select the gain of 10. Specifying an input range of 0 to +7 mA will select the gain of 2.

2.4 Configuring and Using Circuit Breakers

Each current input channel comes with a circuit breaker that can monitor the measured current and open the circuit when measurements are out of range. A circuit breaker trips when the measured current is below the minimum input range or above the maximum input range.

2.4.1 Configuration

You can configure circuit breakers by using the `CreateAICurrentChannel()` method as described in above or by using the channel object methods or a property node under LabVIEW.

Possible configuration values include the following:

- Disabled (`UeiFeatureDisabled`): circuit breaker is disabled. If the input current exceeds the specified input range, the current measurement will clip to the maximum or minimum range value.
  See **Table 2-1** for input current range values associated with each gain setting.
- Enabled (`UeiFeatureEnabled`): circuit breaker is enabled. If the input current exceeds the specified input range for longer than 100ms, the circuit breaker will disconnect the circuit to protect input resistors from overcurrent. After a circuit breaker trips, measurements will be approximately 0mA.
- Auto (`UeiFeatureAuto`): circuit breaker is enabled or disabled depending on a setting stored in the EEPROM. You can use PowerDNA Explorer to change the setting and save it in the EEPROM.

2.4.2 Getting Status

The circuit breaker status can be accessed with the `CUeiCircuitBreaker` object.

```
// Create a circuit breaker object and link it to the session's stream

CUeiCircuitBreaker cb(aiSession.GetDataStream());
```

After the circuit breaker object is created, you can use the `ReadStatus` method to retrieve the status masks.

```
// Read CB status

uInt32 currStatus, stickyStatus
cb.ReadStatus(&currStatus, &stickyStatus);
```

Each bit in the current status mask corresponds to a circuit breaker. The bit value is 1 if the CB is currently tripped and 0 if it is not.

The AI-204 does not support sticky status. The purpose of the sticky status mask is to show whether the CB tripped since last time status was read regardless of the current state.

2.4.3 Manual Reset

Use the `Reset` method on a circuit breaker object to reset one or more breakers.

The mask parameter specifies which circuit breaker to reset (1 to reset, 0 to leave alone).

```
// Reset breakers for channels 0 and 2

cb.Reset(0x5);
```

2.5 Configuring the Timing

You can configure the AI-204 to run in simple mode (point by point), high-throughput buffered mode (ACB mode), or high-responsiveness (DMAP) mode. In simple mode, the delay between samples is determined by software on the host computer. In buffered mode, the delay between samples is determined by the AI-204 on-board clock and data is transferred in blocks between PowerDNA and the host PC.

The following sample shows how to configure data transfers using simple mode. Please refer to the “UeiDaq Framework User’s Manual” to learn how to use other timing modes.

```
// configure timing of input for point-by-point (simple mode)

aiSession.ConfigureTimingForSimpleIO();
```

2.6 Reading Data

Reading data is accomplished by using *reader* object(s). There is a reader object to read raw data coming straight from the A/D converter. There is also a reader object to read data already scaled to volts or temperature units.

The following sample code shows how to create a scaled reader object and read samples. The data is in milliamps.

```
// create a reader and link it to the analog-input session’s stream

CUeiAnalogScaledReader aiReader(aiSession.GetDataStream());

// the buffer must be big enough to contain one value per channel

double data[2];

// read one scan, where the buffer will contain one value per channel

aiReader.ReadSingleScan(data);
```

2.7 Cleaning-up the Session

The session object will clean itself up when it goes out of scope or when it is destroyed. To reuse the object with a different set of channels or parameters, you can manually clean up the session as follows:

```
// clean up the session

aiSession.CleanUp();
```

Chapter 3 Programming with the Low-Level API

This chapter provides the following information about using the low-level API to program the AI-204:

- About the Low-level API (Section 3.1)
- Low-level Functions (Section 3.2)
- Low-Level Code Examples (Section 3.3)
- Gain Settings and Circuit Breaker Limits (Section 3.4)

3.1 About the Low-level API

The low-level API provides direct access to the DAQBIOS protocol structure and registers in C. The low-level API is intended for speed-optimization, when programming unconventional functionality, or when programming under Linux or real-time operating systems.

When programming in Windows OS, however, we recommend that you use the UeiDaq high-level Framework API (see **Chapter 2**). The Framework extends the low-level API with additional functionality that makes programming easier and faster.

For additional information regarding low-level programming, refer to the "PowerDNA API Reference Manual" located in the following directories:

- On Linux systems:
  <PowerDNA-x.y.z>/docs
- On Windows systems:
  Start » All Programs » UEI » PowerDNA » Documentation

3.2 Low-level Functions

Table 3-1 provides a summary of AI-204-specific functions. All low-level functions are described in detail in the PowerDNA API Reference Manual.

Table 3-1 AI-204 Low-level Functions

Function	Description
`DqAdv204Read`	Reads either floating point values in milliamps or raw values
`DqAdv204SetMovAvg`	Sets the moving average
`DqAdv204SetAutozero`	Gets/sets autozero on/off in point-by-point mode
`DqAdv204EnableCB`	Enables the circuit breaker
`DqAdv204CBStatus`	Gets the circuit breaker status and reengage CBs that are tripped

3.3 Low-Level Code Examples

Application developers are encouraged to explore the existing source code examples when first programming the AI-204. Sample code provided with the installation is self-documented and serves as a good starting point.

Code examples are located in the following directories:

- On Linux systems: <PowerDNA-x.y.z>/src/DAQLib_Samples
- On Windows: *Start » All Programs » UEI » PowerDNA » Examples*

Sample code for data acquisition modes have the name of the mode and the name of the I/O boards being programmed embedded in the sample name.

For example, `SampleVMap204` contains sample code for running the an AI-204 using VMap data acquisition mode. Note that immediate mode samples are named `Sample<I/O board name>`, (i.e., `Sample204`).

3.3.1 Data Collection Modes

The AI-204 supports the following acquisition modes:

- **Immediate** (point-to-point): Designed to provide easy access to a single I/O board at a non-deterministic pace. Acquires a single data point per channel. Runs at a maximum of 100 Hz.
- **RTDMAP/RTVMAP**: Designed for closed-loop (control) applications. Users set up a “map” of I/O boards and channels from which to acquire data. Input data is stored in I/O board FIFOs at a rate paced by its hardware clock; a single API call (refresh) paced by the user application causes data to be collected directly from I/O board FIFOs and packed for delivery to the user application.
  - RTDMAP collects only 1 data sample per channel per refresh
  - RTVMAP can collect multiple samples per channel per refresh
- **ADMAP/AVMAP**: designed with the same concept as rtDMAP/VMAP except that timebase for transfers is controlled by the CPU board in the UEI chassis (IOM) instead of paced by the user application.
- **ACB**: Designed for data acquisition applications that require all channel data to be delivered without gaps but can accept slight delays in delivery. Data is acquired at the full speed of the I/O board and then stored in an advanced circular buffer (ACB). Data from the ACB is transferred to the user application based on user-programmed events (e.g., data storage crosses a frame boundary of the circular buffer).
  Not available on UEIPAC products.

NOTE: API that implement data acquisition modes and additional mode descriptions are provided in the *PowerDNA API Reference Manual*.

3.4 Gain Settings and Circuit Breaker Limits

The following gain factors are available for the AI-204:

Gain	Input Range [mA]	Notes
1	± 24 mA	Select this for 0-20 or 4-20 mA
2	± 12.5 mA	-
5	± 5.0 mA	-
10	± 2.5 mA	-

Table 3-2 . Gain Factors and Respective Input Ranges

The **circuit breaker** functionality is enabled by default. If the input current exceeds the input range for a gain specified above for longer than 100ms, then the circuit breaker will disconnect the circuit. The circuit breakers can be reengaged to reconnect the circuit.

If the input measurement reads 0 mA, it is advised to call `DqAdv204CBStatus` to check if the circuit breaker has been tripped.

Appendix A

A.1 Accessories

The following cables and STP boards are available for the AI-204 input board.

DNA-CBL-62

This is a 62-conductor round shielded cable with 62-pin male D-sub connectors on both ends. It is made with round, heavy-shielded cable: 2.5 ft (75 cm) long, weight of 9.49 ounces or 269 grams; up to 10ft (305cm) and 20ft (610cm).

DNA-STP-62

The STP-62 is a Screw Terminal Panel with three 20-position terminal blocks (JT1, JT2, and JT3) plus one 3-position terminal block (J2). The dimensions of the STP-62 board are 4w x 3.8d x1.2h inch or 10.2 x 9.7 x 3 cm (with standoffs). The weight of the STP-62 board is 3.89 ounces or 110 grams.

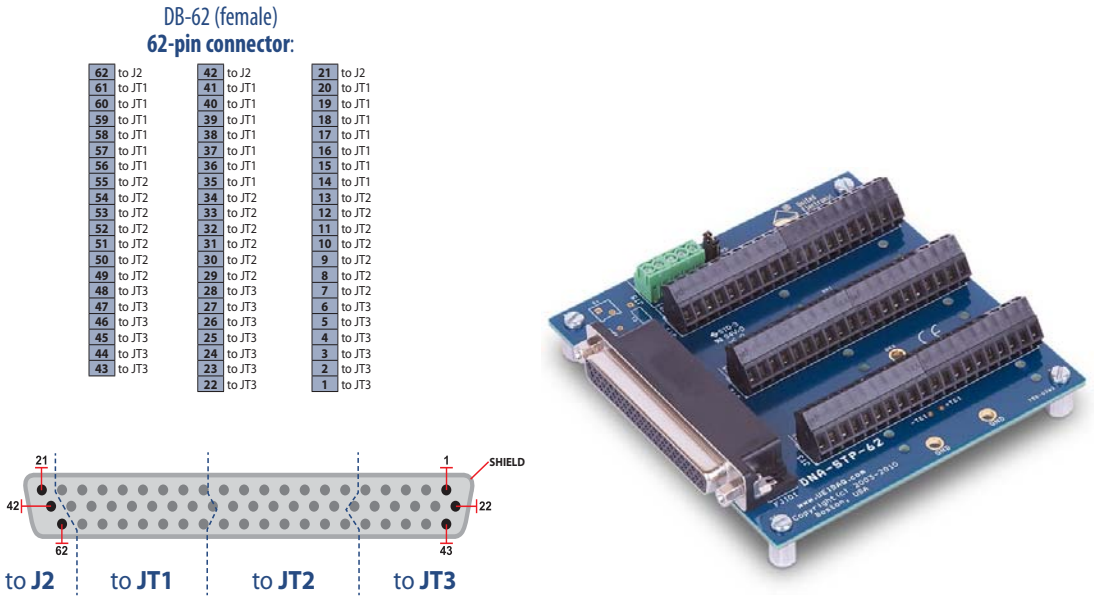

Figure A-1 Pinout and Photo of DNA-STP-62 Screw Terminal Panel

Index