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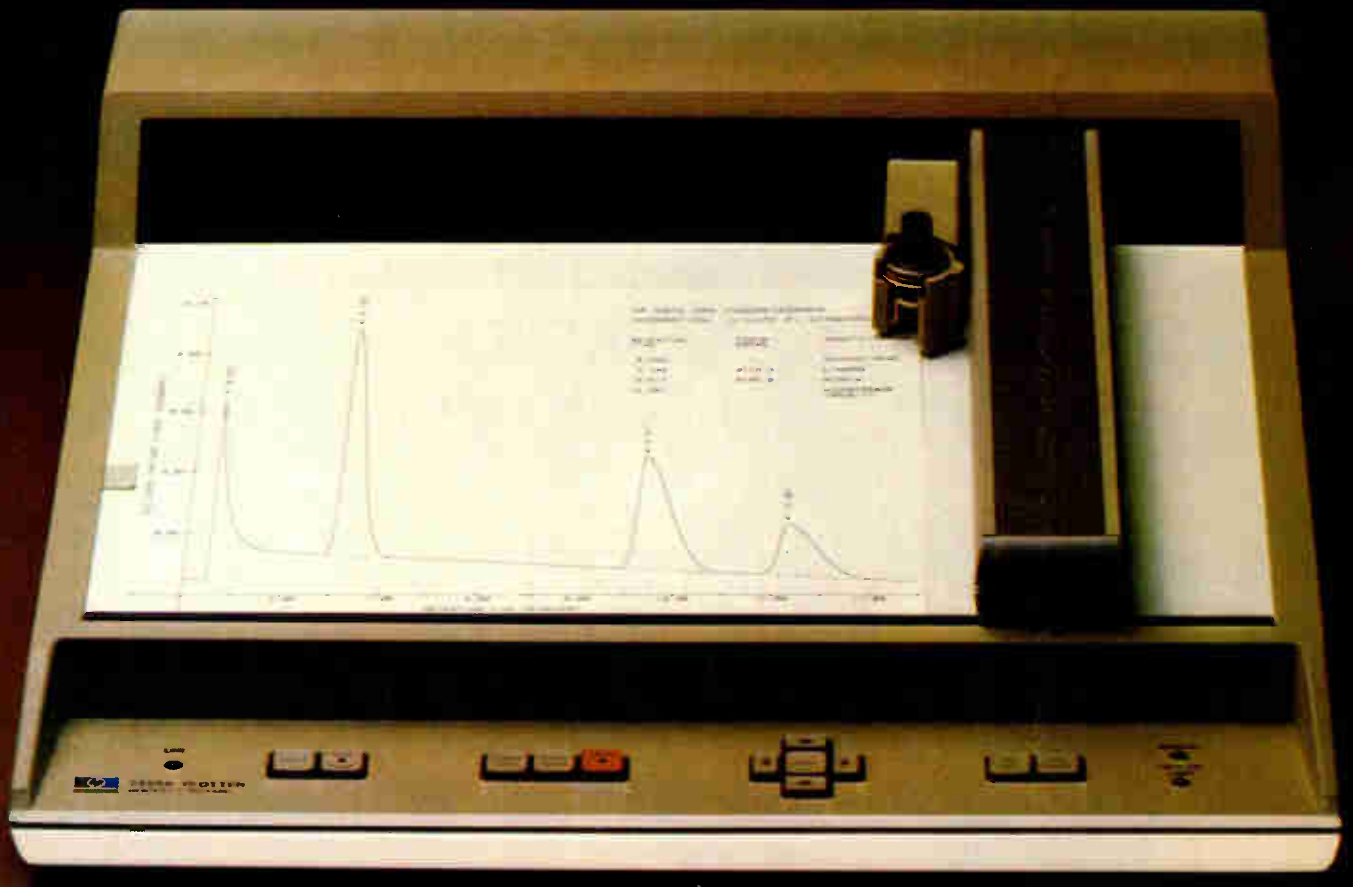

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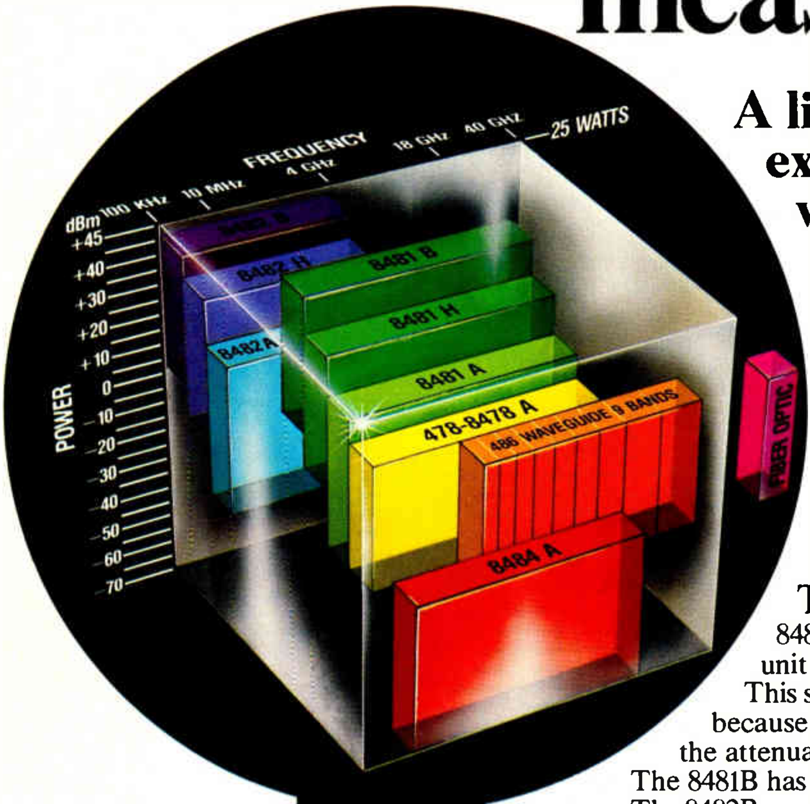

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Electronics
The International Magazine of Electronics Technology
Vol. 52, No. 10 • May 10, 1979

Highlights

Cover: Chip converters take big 12-bit bite, 105
Now reaching 12 bits of resolution in several solid-state technologies, single-chip data converters are eating into a traditionally hybrid market. But hybrid devices still have the edge in performance, says this special report.
Cover is by Art Director Fred Sklenar.

Will IBM stay No. 1 in France? 81
Not if CII-Honeywell Bull has its way. Next year, aided by the $100 million and more it spends each year on research and development, it hopes to deliver more computers to French customers than any other company.

Bubble memories rate their own test system, 117
If the arrival of specially designed test instrumentation is proof of a technology's maturity, then bubble memories have definitely made the grade. A new tester thoroughly analyzes quarter-megabit devices in a matter of minutes.

ZIF connectors oust standard backplanes, 133
Zero-insertion-force connectors can be mounted on motherboards to create an excellent package for bus-structured microprocessor systems.

. . . and in the next issue
Special report on new computer architecture . . . preview of the National Computer Conference . . . introducing a new 16-K static RAM.

Electronics

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Publisher's letter

In developing new technologies, "talent may be more vital than size," comments Steve Bisset, president of tiny Megatest Corp. in Santa Clara, Calif. The test of this statement came when Megatest, started by two people in 1975 and now 85 to 90 strong, persuaded giant Rockwell International Corp. to give the go-ahead for the small firm to develop a general-purpose characterization system for the larger firm's upcoming bubble memory.

Megatest worked on the project on a crash basis for a year. Aided by close cooperation from Rockwell, it developed the bubble memory test system described on page 117 by Bisset and Rockwell coauthors Steve Bristow, technical staff engineer, and Tom Chen, manager of research engineering.

Was Rockwell nervous about assigning such an important project to a small company with no background in bubble memory testing? "They were concerned at the beginning, in the middle, and up to the end," Bisset admits. "But apparently they're satisfied—it works."

For its part, Rockwell considers the smooth interface between the companies a key factor in the success. Company size was not the main problem, according to Bristow. "Megatest was the most qualified of those interested in bubble memory testing at the time. It takes a small company to take the risk."

Besides making an important contribution to electronics technology, the bubble memory tester project added a new dimension to Megatest. The firm found its original niche in designing instruments for high-volume production testing of large-scale integrated circuits. But in the bubble memory field, there is no high-volume production testing niche as yet. So the company took a new direction: general-purpose equipment for engineering characterization. Megatest sponsored the development entirely with its own capital, taking all the risks in order to retain all the rights.

The advanced software technology laboratory set up by the Texas Instruments equipment group in 1978 is an unusual example of the transfer of technology from military to civilian uses. The nucleus of the lab, headed by Roger Bate, was formed by a group that had worked on a TI contract with the Army Ballistic Missile Advanced Technology Center in Huntsville, Ala., from 1972 to 1977.

The unusual aspect of this military project was that the team turned from writing software to designing methods of writing software. In short, the result was a software methodology that is now being used internally by TI. And it's significant. As Dallas bureau manager Wes Iversen points out in the story on page 85, the corporate-wide goal is a 25% improvement in programmer productivity by 1985 using the techniques defined during the Huntsville project. It could add up to a $379 million savings in that year alone.

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Readers' comments

Leave well enough alone

To the Editor: Though I agree in general with the ideas expressed in Pat Caudill's "Using assembly coding to optimize high-level language programs" in the Feb. 1 issue [p. 121], I should like to point out a few problems.

To support his contention that certain simple loops and data manipulations should be coded in assembly language, the author shows three examples of optimizing with assembly code. All three contain errors such that none will work. In just 22 lines of code there are four errors. I think an error every six lines is rather excessive, but this does indicate one of the normally hidden costs of assembly language.

The errors in Fig. 1 are: JR NC,LP1 should read JR C,LP1. Also the logic used is not the same as in the Fortran original—128 loops × 1 input, instead of 64 loops × 2 inputs. This difference could be important if reading the status port cleared the ready flag.

In Fig. 2, line 18 should read MOV M,C ; STORE LOW BYTE. In Fig. 3, line 6 should read LD A,(BVALUE).

In contrast, the high-level language equivalents are all error-free. In rewriting these routines the total memory saved was 90 bytes—about $1 in 2708. Correcting each of those four errors will take at least, say, half an hour. Is it worth it? Frankly it is unlikely unless large quantities are being made or unless, as in the first example, a high-level language routine is not fast enough to keep up with hardware.

As memory prices continue to plummet, it becomes less and less attractive to optimize high-level language programs with assembly language, with the exceptions noted.

Chris Lusby Taylor
Brussels, Belgium

■ **The author replies:** *Perhaps I should have pointed out more strongly that "if it ain't broke, don't fix it." These techniques should be used when the product is out of spec and needs to be brought into line. Usually this is because of a need to increase execution speed rather than to decrease memory requirements.*

Examining the examples, I found

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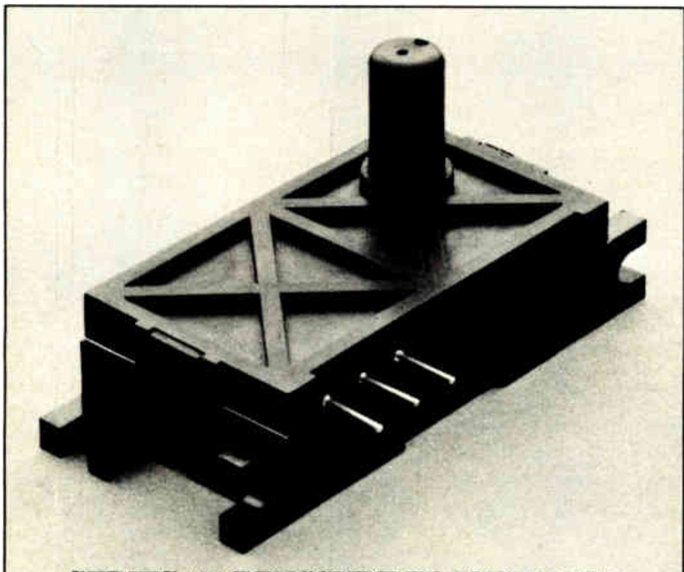

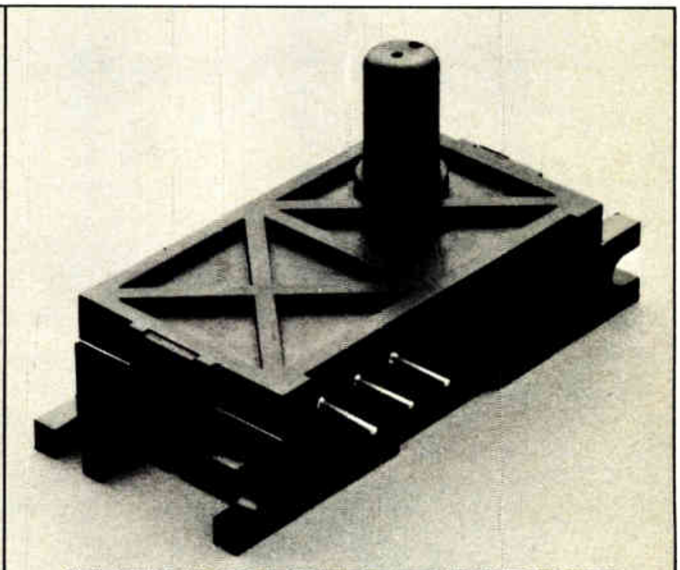

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Circle 7 For Data

Readers' comments

two mistakes in the assembly language versions in Figs. 1 and 2. In Fig. 1, it is the Fortran program that is incorrect. The conditional statement in line 10 should be:

10 IF (IMP(8) .AND 1) .EQ.0) GO TO 10

This routine was subjected to one level of loop unwinding to lower the loop overhead. Its actual time per byte is only 43.63 microseconds. This loop unwinding is also required on a 2-megahertz 8080 assembly language routine.

I would like to thank Mr. Taylor for pointing out the other mistakes.

Switch the track

To the Editor: D. C. Mitchell's program in "HP-67/97 tracks communications satellites" [March 1, p. 146] contains a fault. Using the inputs of his example, the program generates elevation (E) and straight-line distance (d) numbers that differ from those in the Oscar 7 tracking-data table. Either Mr. Mitchell used different coordinates than those stated for Milan, Mich., or there is a bug. Also, the STO C instruction in line 008 is not necessary.

Aside from these comments, I'd like to thank Mr. Mitchell for sharing a really useful program. I can recall several occasions when I tried in vain to calculate series of azimuths and elevations for real-time manual tracking of communications satellites (especially non-synchronous ones!). The old HP-35 just wasn't up to the task. How I wish I had had my HP-67 and Mr. Mitchell's program then.

Robert G. Savage
Aiea, Hawaii

■ *The longitude and latitude of Milan were inadvertently switched in the text. Exchanging these two values in the appropriate program registers should yield values in substantial agreement with the figures that were given in the table.—ED.*

Correction

A typographical error in the Electro79 preview drastically lowered the $3,300 price of Rockland Systems Corp.'s new model 751A Brickwall bandpass filter [April 12, p. 182].

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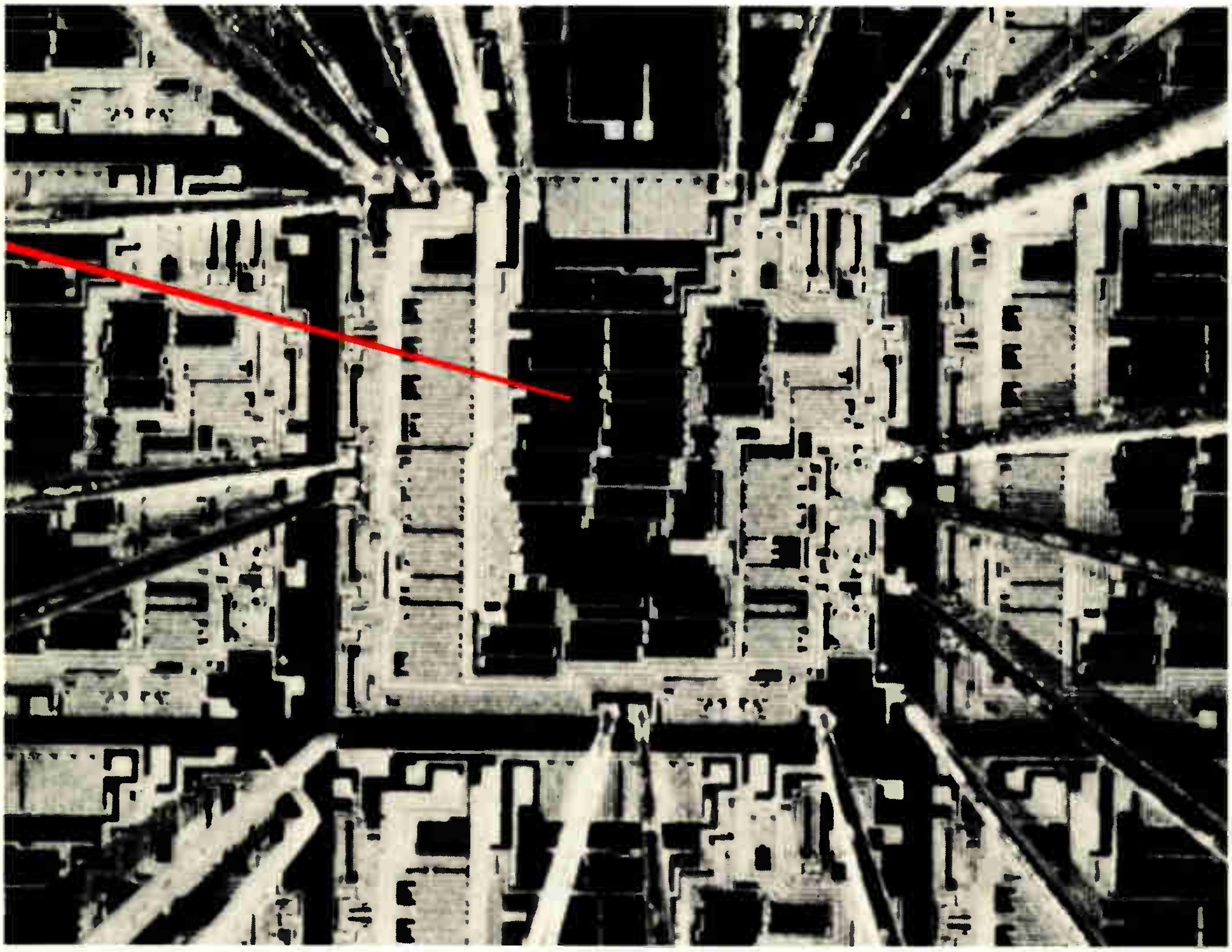

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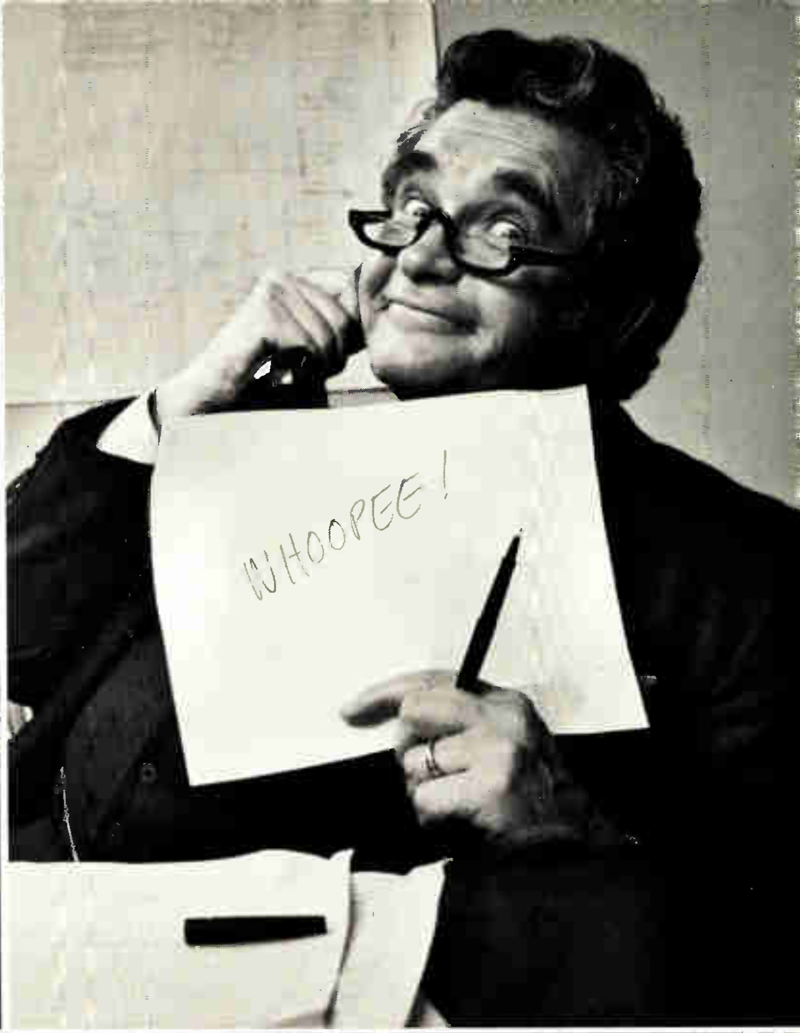
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People

New Bell Labs president sees LSI, software causing changes

"Exciting times in an era of the rapid introduction of new technology" is the prediction of Bell Telephone Laboratories' new president, Ian M. Ross. He expects a burst of new growth in the research and development efforts of the world's largest industrial laboratory.

In particular, he foresees the addition of many new features to the telephone communications system once digital technology and stored program control spread beyond the exchange level down to the private branch exchange and farther.

In telephone equipment, the major technological thrust has been the development of large-scale integration and software to implement the stored program control that will provide more flexible and varied services, Ross says. When it started some years ago with the No. 1 electronic switching network, it was economical only in big systems. Now, he says, "we can afford it for the small switches and private branch exchanges—we even have microprocessors in telephone terminal equipment."

One catch. Still, there is a catch: software, so important to stored program control, cannot be patented. "We are very interested in protecting our proprietary interests in software," says Ross, who was trained as an electrical engineer. He would prefer to see patents in software, noting that it is not Government policy at present.

In addition, as more Bell people work with software, there is another catch: the number of patent applications goes down. Since some people measure productivity by that figure, it seems as though Bell scientists are not inventing as much as before. This is not unique to Bell, Ross notes. It also applies to the country's overall research and development effort, which has a larger software content than ever.

Ross, 51, has been with the laboratory since 1952 and was executive vice president before being named to

Software boom. Ian M. Ross looks for software inventions to multiply at Bell Labs.

his new post. In observing still another way in which Government policies have an impact on Bell's operations, he looks upon the "unlikely" divestiture of Western Electric "with alarm" because, among other things, the free flow of information between the labs and Western's very practical inputs to Bell scientists on the potential cost of a product would be jeopardized.

Noting that the laboratories' budget this year for its 18,200 employees is in the neighborhood of $1 billion (up a thousand employees and $100 million from the year before), Ross feels that "our owners are giving us very good encouragement to do our work." He hopes the Federal government "won't do anything to impede that support."

Motorola's Katzir to focus on the auto aftermarket

When Levy Katzir was vice president of Motorola Inc.'s multinational operations in 1977, its Italian car radio and television manufacturing division was losing lots of money. Within two years, though, the 14% market share for car radios was increased to 30% by "paying more attention to the customer," he says. New products, such as pull-out radios to foil thieves, were matched to customer interest, and decentralized distribution introduced.

Now Katzir, 47, is the new gener-

al manager of Motorola's Automotive Products division and the same increased attention to the customer is behind its reorganization. Operating losses at its Angers, France, automotive alternator and electronic ignition plant and at its British and its U. S. car radio businesses dragged the division's 1978 earnings down to $9.5 million on sales of $202 million.

The reorganization, Katzir says, gives greater power to product-line managers developing items like auto radios and electronic controls, as well as diagnostic systems for the microprocessor-based controls. They will be able to respond more quickly to what the market seems to want either by increasing production in key areas or by introducing new products and have therefore been given responsibility for distribution and sales departments, as well as for manufacturing. Katzir's structuring went into effect in late March and has already resulted in the departure of several executives.

New concentration. But perhaps the biggest change is Katzir's new direction for the division: it will concentrate on the automotive aftermarket. This is a break with almost 50 years of tradition for Motorola, which was built selling radios to Detroit auto makers and their dealers. But sales to original-equipment manufacturers like Ford Motor Co., are shrinking to "insignificant levels," says Katzir. That's why he is resorting to what is, for Motorola, "unconventional" strategy: emphasizing the consumer, not the OEM.

Born in Antwerp, Belgium, he grew up in Israel where he lived for 37 years. Not a holder of a college degree, he gained his knowledge of communications and electronics in Israeli army schools and at the British Institute of Engineering.

He started his own company and, under license, manufactured Motorola's two-way communications gear in Israel beginning in 1955. Motorola bought his business in 1964 and made him its managing director. Katzir remained there until called in 1971 to Motorola's Chicago headquarters to run its foreign operations. □

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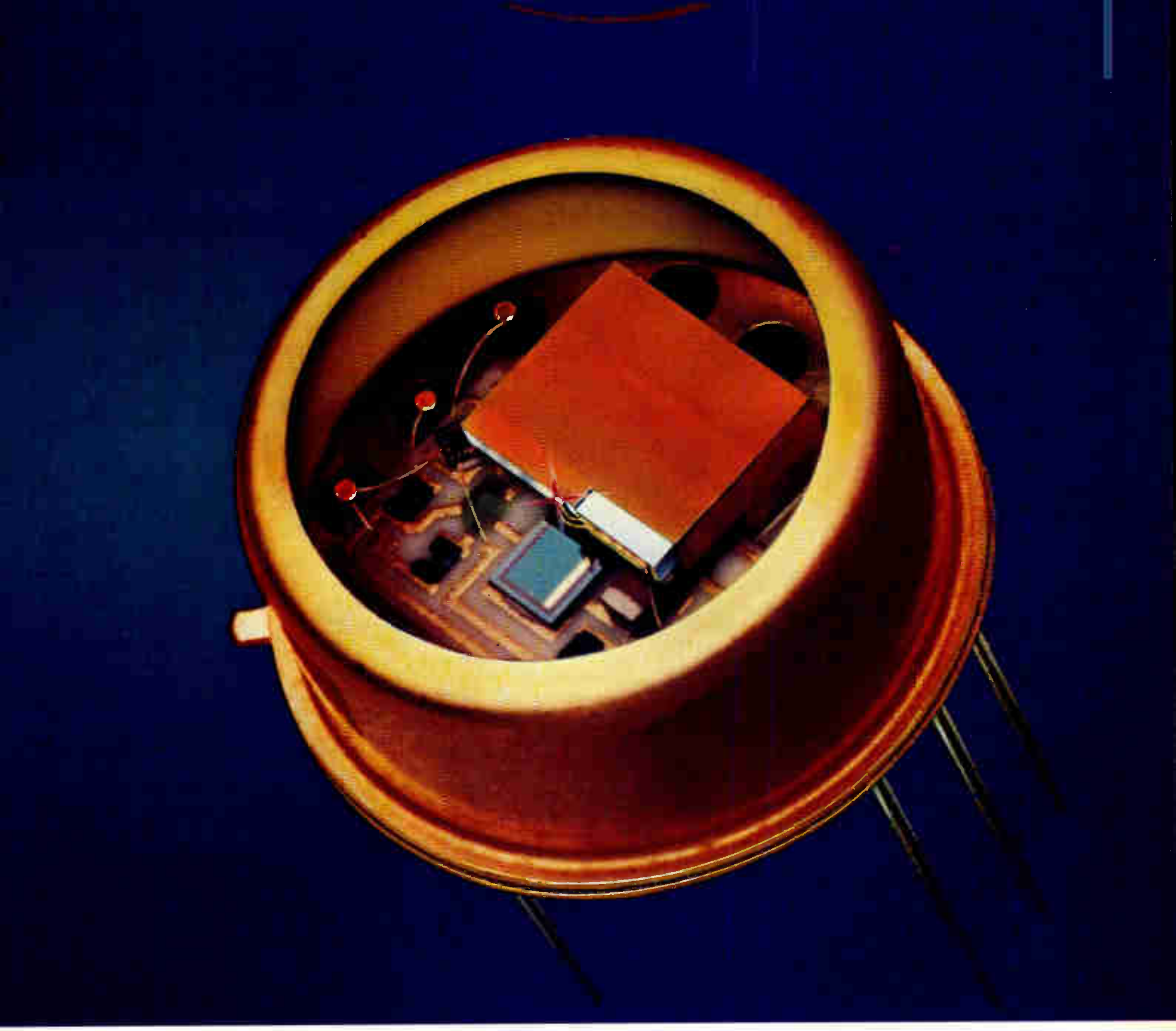

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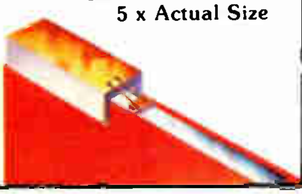

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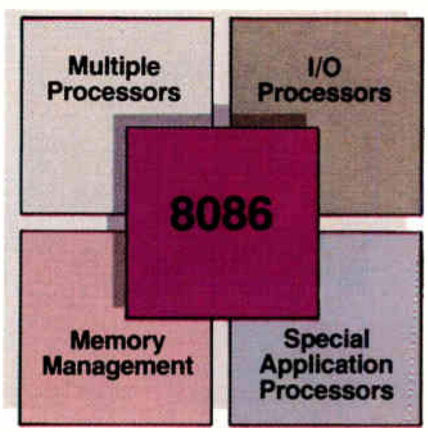

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Circle No. 21 for information

"See us at NCC , June 4-7, New York City." Booth #1420

PROJECTION MASK ALIGNER

Editorial

The big little world of electronics . . .

There occurred at Electro79 one of those unusual and fortuitous confluences of electronic heavy hitters. Gathered in New York last week along with the thousands of engineers, sales people, and peripheral personnel attending the annual conference was a clutch of top executives from companies around the world. They were in the city to take part in an Electro panel session on no less compelling a subject than worldwide problems and opportunities for the electronics industries.

From Japan, China, West Germany, France, Britain, the Netherlands, the United States, and even Texas they came, men having in common a global outlook, a sense of electronics as a kind of technological Esperanto.

The conclusion to be drawn from their presentations is that the business of electronics is truly international, and that the obstacles, aspirations, and aims are strikingly similar. But there are still some differences in execution, some approaches that defy homogenization.

For example, while Japan, France, and West Germany must all sell their electronic products around the world, each nation goes about the business of competing in a different fashion. Consider how each pursues the VLSI solution. For the Japanese, it means a strong government hand. For the French, it entails a search for joint ventures with foreign companies. For the West Germans, it is a reliance on the expertise of its big three semiconductor manufacturers.

One other impression drawn from the session is that a potentially big new force is waiting anxiously to make its entrance: China. The message from that rapidly opening society is "Give us the broad, across-the-board know-how, and we will manufacture our own products. We are ready."

. . . still offers opportunities for the entrepreneur

One message coming through loud and clear at the session on electronics worldwide is that Europe and Japan have their sights set on overhauling the U. S. lead in advanced electronics. That's hardly news; but another Electro seminar carried a counterpoint message.

A group of corporate venture capitalists told an audience of over 100 that U. S. electronics entrepreneurs are in the clover. After a mid-1970s drought, venture capital is available in some abundance (p. 88).

All well and good, but where are the bold souls who will exploit this bonanza? Where are the men and women with the ideas, the guts, and the managerial abilities to break new ground in the electronics industries?

One place we suspect they may be found is among our readership. Should you be pondering the prospects of entrepreneuring, we suggest that it is time to reach a decision. Not only are the potential personal rewards Midas-like, but—as the past 20 years of the electronics industries show—you can make a significant contribution to technology.

One point that needs underlining: you need more than a good idea to convince venture capitalists to support you. Those Brooks Brothers suits and Ivy League manners at the Electro seminar failed to disguise the bottom-line brains within. Of course, there is good reason for the hardheaded approach. Innumerable venture-capital units have foundered on the rocks of ill-advised investments.

To get an idea of what venture capitalists want, look at publications like Capital Publishing Corp.'s "Guide to Venture Capital Sources." Essentially, these investors are gambling on the abilities of the entrepreneurs they back, and the question such guides can answer is what these abilities are. Then you must decide if you measure up.

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Meetings

University/Industry/Government Microelectronics Symposium, IEEE, Texas Tech University, Lubbock, Texas, May 21–23.

Semicon/West, Semiconductor Equipment and Materials Institute (Mountain View, Calif.), San Mateo Fairgrounds and Dunfey Hotel, San Mateo, Calif., May 22–24.

Huntsville Electro-Optical Technical Symposium and Workshop, Society of Photo-Optical Instrumentation Engineers (Bellingham, Wash.), Huntsville Hilton, Huntsville, Ala., May 22–25.

Failure Avoidance Seminar, Integrated Circuit Engineering Corp. (Scottsdale, Ariz.), Hilton Inn, Jamaica, N. Y., May 23–24.

International Television Symposium and Technical Exhibition (Montreux, Switzerland), Montreux Palace Hotel, May 27–June 1.

International Symposium on Multiple-Valued Logic, IEEE, Beaufort Hotel, Bath, England, May 29–31.

15th Symposium on Electron, Ion and Photon Beam Technology, IEEE, Sheraton Boston Hotel, Boston, May 30–June 1.

Conference on Laser Engineering and Applications, IEEE and Optical Society of America, Washington Hilton Hotel, Washington, D. C., May 30–June 1.

1979 International Summer Consumer Electronics Show, Electronic Industries Association, McCormick Place, Chicago, June 3–6.

NCC '79—1979 National Computer Conference, IEEE, American Federation of Information Processing Societies, *et al.*, New York Hilton and Americana Hotels, New York, June 4–7.

Automated Testing for Electronics Manufacturing, Benwill Publishing Corp. (Boston), Radisson Ferncroft Hotel, Danvers, Mass., June 4–7.

ICC '79—International Conference on Communications, IEEE, Sheraton Boston Hotel, Boston, Mass., June 10–14.

Symposium on Applications of Ferroelectrics, IEEE, Sheraton-Ritz Hotel, Minneapolis, Minn., June 13–15.

Joint Automatic Control Conference, IEEE and American Institute of Chemical Engineers, University of Washington, Seattle, June 16–21.

Power Electronics Specialists Conference, IEEE, Bahia Hotel, San Diego, Calif., June 19–21.

33rd Annual Convention of the Armed Forces Communications and Electronics Association, Afcea (Falls Church, Va.), Sheraton Park Hotel, Washington, D.C., June 19–21.

Second Joint Intermag—Magnetism and Magnetic Materials Conference, IEEE and American Institute of Physics, Statler Hilton Hotel, New York, July 17–20.

Short courses

Machine Vision, Automatic Assembly, and Productivity Technology, summer session, Massachusetts Institute of Technology, Department of Electrical Engineering and Computer Science, MIT, Cambridge, Mass., June 11–15.

First Annual National Conference on Recent Advances in Microcomputers, sponsored by Clemson University and the University of South Carolina, June 19–21. For program information, contact John Gowdy, Continuing Engineering Education, College of Engineering, Clemson University, Riggs Hall, Clemson, S. C. 29631.

Microprocessors and Microcomputers, George Washington University, July 30–Aug. 3. For information, write to Director, Continuing Engineering Education, George Washington University, Washington, D. C. 20052, or call toll-free (800) 424-9773.

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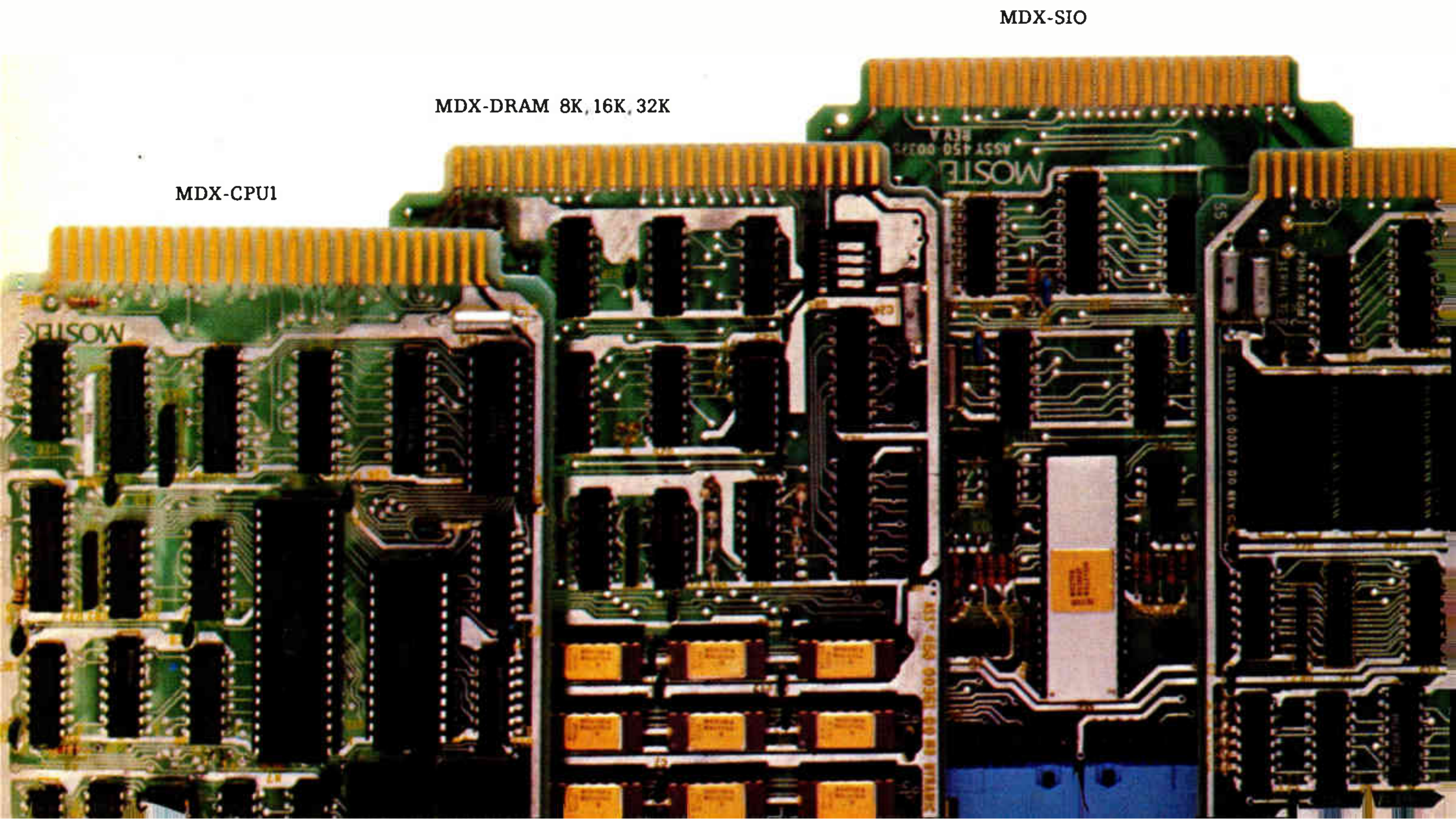

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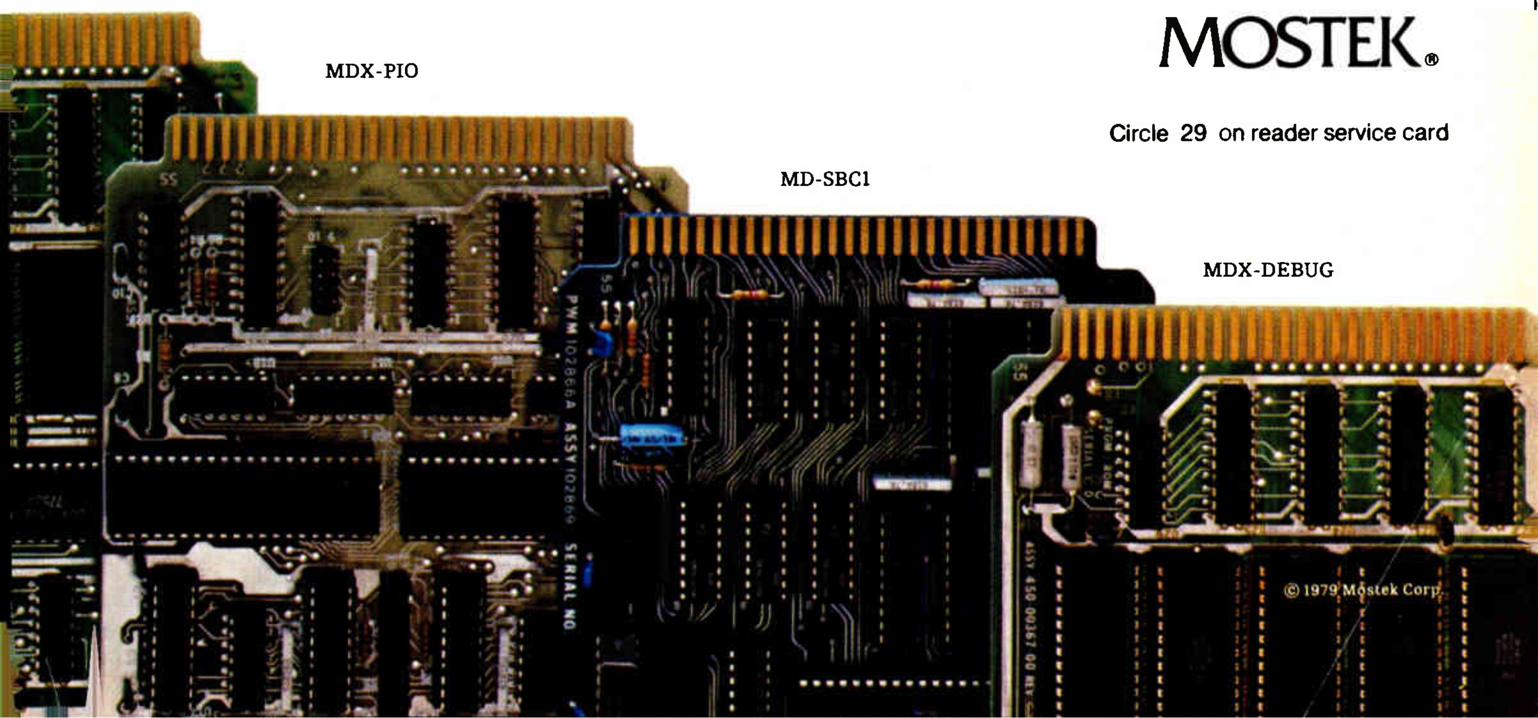
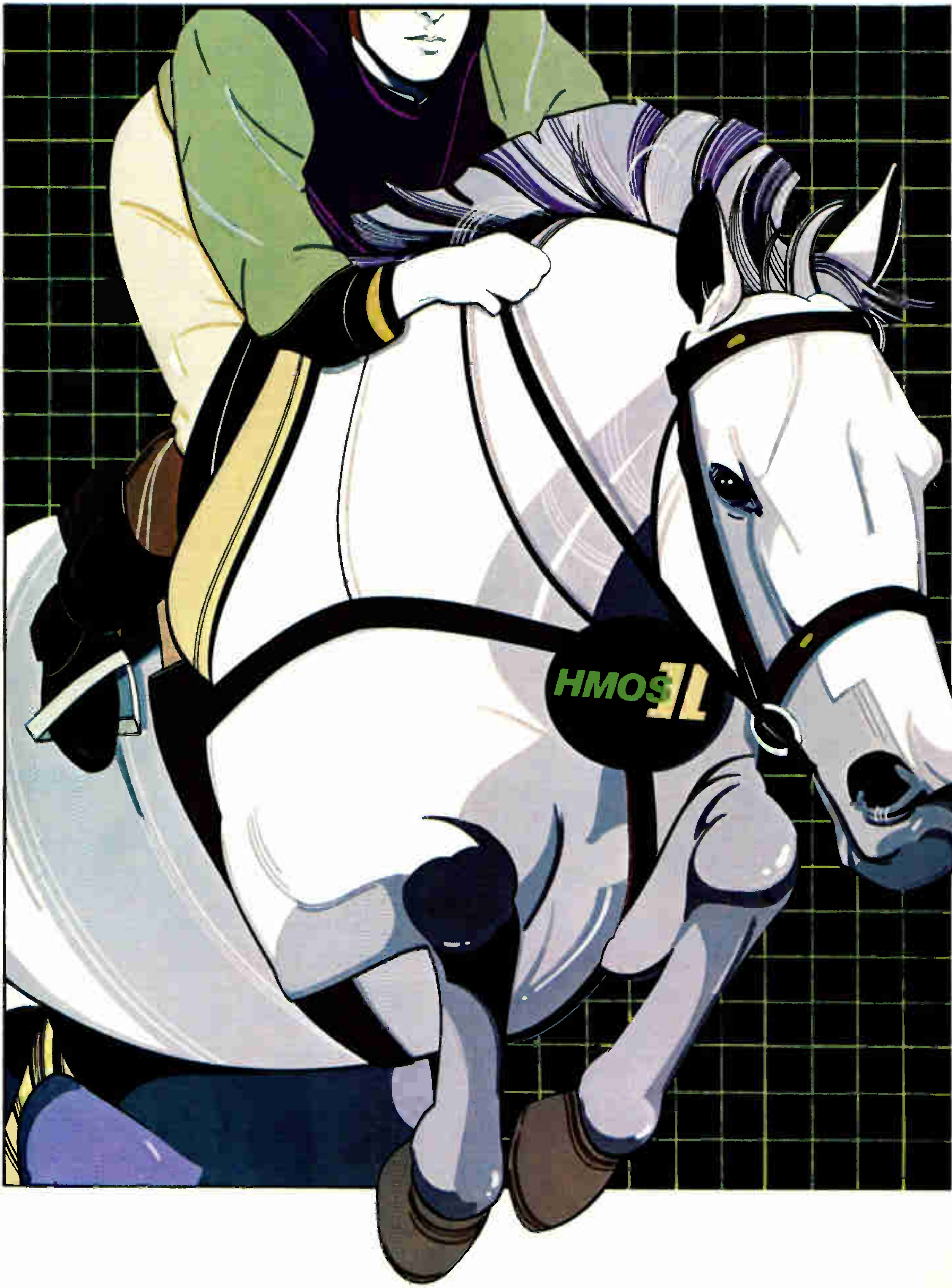


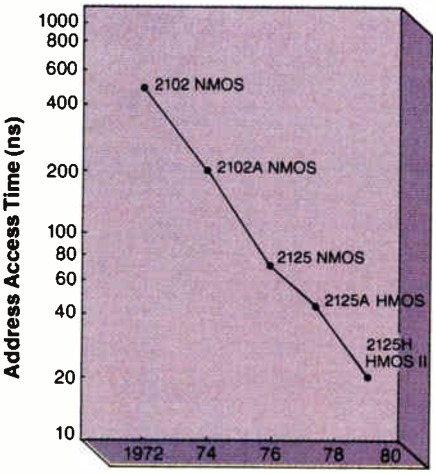

HMOS II

New Breed of MOS.

Intel introduces HMOS II*– and a new family of static RAMs that cross the finish line in 20 ns.

Intel just set a new pace for high performance memory with HMOS II. It's our patented next generation MOS technology so advanced it delivers speeds faster than bipolar and even our own first generation HMOS process. HMOS II gives designers the fastest, lowest power static RAMs ever—plus traditional MOS economy and reliability. Our new 1K and 4K RAMs are fully compatible, higher speed upgrades of Intel's time-tested 2115A/2125A and 2147 devices.

History of MOS speed



Intel's continued process and scaling improvements have doubled MOS speeds every two years. The above graph demonstrates this trend with Intel's 1K x 1 static RAMs.

1K fast statics that leave bipolars behind

Designers building cache, writeable control store or buffer memories will find our 16-pin 2115H/2125H 1K RAMs ideal. For new designs, two versions deliver record access speeds of 20 ns and 25 ns, with a speed/power product twice as good as slower bipolar RAMs.

Our 35 ns and low power 30 ns models can be used as direct plug-in replacements for 93415A and 93425A bipolar RAMs. They'll cut power dissipation up to 36%. And, best of all, they're available now.

New, faster 4K with no power increase

Intel's new 2147H gives you all the advantages of our 18-pin 4K x 1 industry standard 2147, with twice the speed and no increase in power. With access times as fast as most 1K RAMs, it's important news for anyone designing buffer, cache, control store and main memory systems. If you're presently working with 1K RAMs, you can increase density or reduce board space by a factor of four. In a 4K format, the 2147H makes possible a new dimension of higher performance systems.

The 2147H's low active power dissipation and automatic power down on deselection also mean dramatically reduced power consumption compared to constant current static RAMs. In fact, because most devices are deselected at any given time, the larger your system, the lower your power dissipation per bit. It all adds up to simplified designs and major savings in cooling and power supplies.

HMOS II fast static RAMs

Part No.	Maximum Access Time (ns)*	Power Consumption (mA)* Active	Standby
4096x1			
2147H-1	35	180	30
2147H-2	45	180	30
1024x1**			
2125H-1	20	125	
2115H-2 2125H-2	25	125	
2115H-3 2125H-3	30	100	
2115H-4 2125H-4	35	125	

*Over full 0° to 75°C operating temperature range.
**All 2115H versions have open-collector outputs, all 2125H versions have tri-state outputs.

All HMOS II components are fully static and can be used in clocked and unclocked systems. They are directly TTL compatible in all respects: inputs, outputs and operation from a single +5V supply.

Order 2115H/2125H and 2147H RAMs from your Intel distributor. Or, for more information, contact your local Intel sales office or write: Intel Corporation, 3065 Bowers Avenue, Santa Clara, CA 95051.

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*HMOS II is a patented process of Intel Corporation.

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Currently our Plug-In scopes family includes 14 mainframes and 21 plug-in units in the 5000-Series, and 19 mainframes and 35 plug-ins in the 7000-Series. (With them, you can use compatible logic and spectrum analyzers and other special purpose plug-ins.) Among the newer arrivals: a logic analyzer with 16 digital acquisition and display channels. A calibrated 60 GHz spectrum analyzer that's transportable. And the newest: A 1 GHz real time oscilloscope with 10 mV/div sensitivity and 20 cm/ns photographic writing rate. Plus more milestones just ahead.

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Tektronix Plug-In scopes meet your critical measurement demands. From circuit design to plasma physics research. From balancing rotating machinery to measuring the accuracy of D to A converters.

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Electronics newsletter

Run-time operating system for 16-bit micros to be unveiled

Data General Corp. of Westboro, Mass., is about to introduce what's billed as the first native run-time operating system for 16-bit microcomputers. Called Micron, **it may mark a major industry transition from emphasis on hardware to one on software,** according to Data General spokesmen. The operating system is the basis of the company's new software thrust, including seven utility programs written in Pascal. Micron is an executive software package for single-user, multitask environments; normally disk-based, its programs can be burned into programmable read-only memory for dedicated applications. The new software also is compatible with Data General's advanced operating system, making Pascal available even to time-sharing users of the firm's Eclipse large minicomputer.

Data General's announcement, expected later this month, may be the largest commitment yet by a major computer maker to powerful, highly structured, high-level Pascal and could influence ANSI's Pascal standardization effort. Deliveries are scheduled for midsummer.

Computer 'speaks' on phone—no matter who's calling

Computers that answer telephones? At next month's National Computer Conference, Dialog Systems Inc. of Belmont, Mass., will show a vector-processor–based system that answers up to eight incoming calls, understands single-word instructions put to it over the telephone, and responds to those orders. Called the model 1800, **the system sells for less than $100,000, is speaker-independent (works with any caller),** and will find use in areas such as banking, retailing, government, and automatic telephone-switching networks. The company designed its own vector processor for the system; with a machine cycle time of 120 ns and three parallel buses operating independently and simultaneously, speech can be processed in real time.

National eyes fiber optics for industrial uses

Already making light-emitting diodes, National Semiconductor Corp. of Santa Clara, Calif., plans to use them in a series of low-cost, LED-fed fiber-optic transmitter-receiver pairs **for short-haul industrial communications or distributed-processing systems.** The family is expected to include a receiver packaged as an interface device for less than $50 and a hybrid pair at less than $50 for data rates up to 100 Mb/s and distances up to 3 km, followed by a monolithic receiver for shorter distances and data rates below 1 Mb/s targeted to sell for less than $10 in volume. National is designing the packages to plug into standard optical connectors to help hold down system costs. Another design feature is the use of a high-performance p-i-n diode for detection.

TI to apply 32-K technology to 8-K E-PROM

Look for Texas Instruments Inc. to extend its family of single-supply erasable programmable read-only-memory parts later this year with introduction of an 8-K device. To be designated the TMS2508, it will use the single 5-V supply technology developed by the Dallas company for its higher density 2532 and 2516 E-PROMs. **Because of its 32-K technology roots, performance characteristics of the pin-compatible 8-K part are expected to be strong,** with access times in the 300-to-350 ns range. In today's market, the only other single-supply 8-K devices available come from Intel Corp., which supplies partials of its single-supply 16-K E-PROM parts. Availability of the new 8-K memory could come as early as June.

Electronics newsletter

Cosmic rays cause soft errors, warns IBM researcher

The semiconductor industry is no longer laughing at the soft errors in random-access memories caused by alpha particles [*Electronics*, June 8, 1978, p. 42]. But as they research very large-scale integration, they had better prepare to handle a more cosmic problem, an International Business Machines Corp. researcher warns. J. Ziegler of IBM's Thomas J. Watson Research Center, Yorktown Heights, N. Y., says cosmic rays produce a variety of elementary atomic particles when they strike silicon, including muons, **which in turn produce the largest number of electron-hole pairs in the silicon.** These pairs cause the soft errors. The cosmic radiation will apparently cause the most trouble when minimum line widths approach 1 μm.

Heart attack may curtail Feerst's IEEE campaign

Irwin Feerst, perennial petition candidate for president of the Institute of Electrical and Electronics Engineers, may not be able to pursue his campaign this year until he recovers from a heart attack sustained late last month while vacationing in Florida. **Or ill health could force him to drop out entirely** from a three-way race developing among Feerst, board of directors candidate Burkhard H. Schneider, and another petition candidate, Leo Young.

Texas inventor says diode idea was his

Claiming origin of the concept of a semiconductor diode as receptor-detector in a fiber-optic communications system, Texas inventor and freelance writer Forrest M. Mimms III is planning legal action against Bell Laboratories. **Mimms says he did work on the concept as early as 1966 and can point to an outline of the idea in a 1973 book he wrote.** He says he offered the idea to Bell Labs the same year, only to be rejected. The labs' light-powered telephone [*Electronics*, Nov. 23, 1978, p. 38] uses the concept. Bell will say only that it has discussed Mimms' claim with him and that the light phone is based primarily on a high-efficiency photodiode developed at the labs.

Addenda

If minicomputer maker Computer Automation Inc. has its way, a 16-bit machine that is **cheaper to throw away than repair** will hit the market in several months. Called the Scout and billed as a "consumable" unit, it splits functions among 11 separate cards (6.25 by 8.30 in.) instead of putting them on a single board. The key feature is a self-diagnostic go/no-go light-emitting diode on each card. In a typical four-card configuration, the unit should sell for less than $1,000 in quantity, says the Irvine, Calif., firm. . . . Energy Conversion Devices Inc., Troy, Mich., has announced an agreement with Arco Solar Inc. for a joint 18-month program to develop solar cells. **Arco will pay Energy Conversion $3.3 million** for product development and the right to a nonexclusive license. The program will be based on Energy Conversion's recent development of a new alloy potentially suitable for low-cost solar cells. . . . Now that the year is well into the second quarter, companies are beginning to look for the softening of the economy predicted for the second half of the year. Leslie Alperstein, director of research for the New York investment firm of Bache Halsey Stuart Shields Inc., says the economy is at the turning point, which is the reason for "a wide discrepancy in the estimates" for the future. **His firm feels that the dip will start in the third quarter and last for three quarters.**

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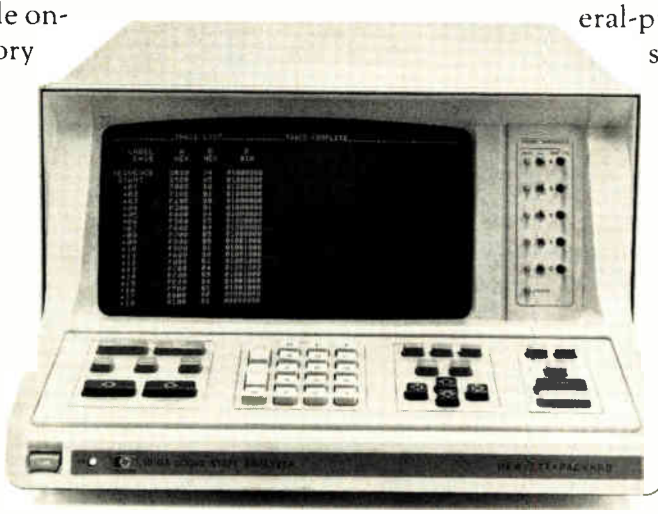

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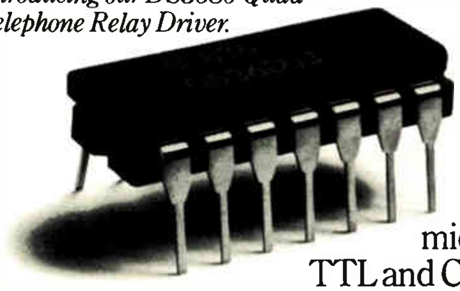

Here's a relay driver that'll drive down operation costs and drive home design efficiency on all your telephone systems.

Input current requirements for the DS3680 are extremely low, typically 10 microamps. The relay driver interfaces with TTL and CMOS logic and can be operated from a −10 to −56 volt battery.

The DS3680 is an ideal alternative to standard TTL and opto-coupler relay drivers. It does a superbly dependable job of isolating a noisy central office battery from your logic power supply.

It also has a fail-safe disconnect, so if the input is open, the driver is off. The "stand-off" voltage between any two pins is 70 volts. In "stand-by" mode, power is only 50 microwatts/driver. A built-in diode clamp resists high voltage "back swing" when the relay is switched off.

The DS3680 accepts 50 mA loads. Comes in fourteen pin dual in-line packages. And has a ±20 volt common mode input range (excellent level shifting plus high noise immunity).

So call your local National rep about our new DS3680 Quad Telephone Relay Driver, and be sure to ask about the rest of our growing line of telecommunications products including, CODEC's, filters, SLIC's and telephone dialers.

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National Semiconductor

Light-powered phone operates without an internal light source

by John Gosch, Frankfurt bureau manager

Siemens researchers rely on vibrating plastic membrane to modulate laser light piped in from central point

Laboratory scientists at Siemens AG are hard at work on a radically simplified type of laser-powered telephone handset.

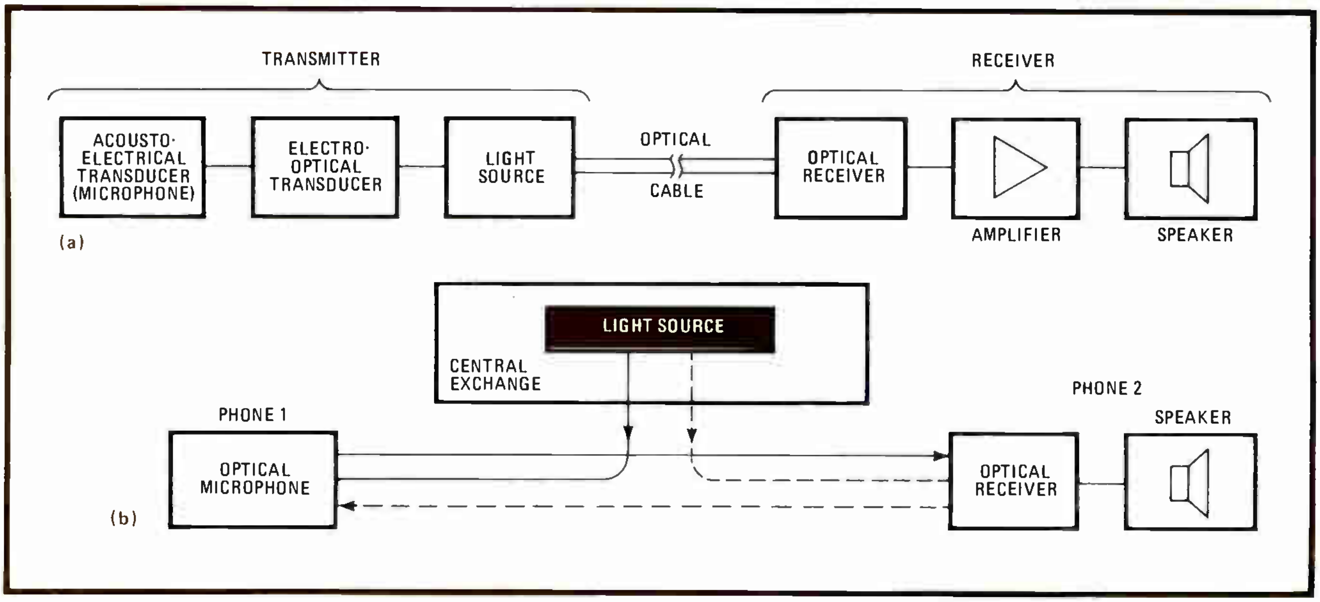
"We expect to have a prototype light-powered phone for analog voice communications ready in less than two years," says Ingrid Fromm, a physicist who heads the development effort at the Siemens labs in Munich. Appropriately called the Optophon, the laboratory prototype Siemens has developed is the basis for a later device that will undergo field tests, possibly in West Berlin, she says. The West German post office there is already service testing a number of optical-fiber links from various firms in West Germany [*Electronics*, Nov. 13, 1975, p. 56, and Sept. 28, 1978, p. 72].

By developing a so-called "optical microphone" for the transmitter portion of their phone, the Germans are aiming at a unit that will have far fewer parts than Bell Labs' fiber-optic telephone [*Electronics*, Nov. 23, 1978, p. 39]. The microphone, incorporating a thin, mirrored membrane, uses the voice to modulate laser light directly. The transmitter does not need the transducer and modulator of a more conventional fiber-optic voice link, in which the transducer converts the voice to an electrical signal and the modulator electrically modulates the light source.

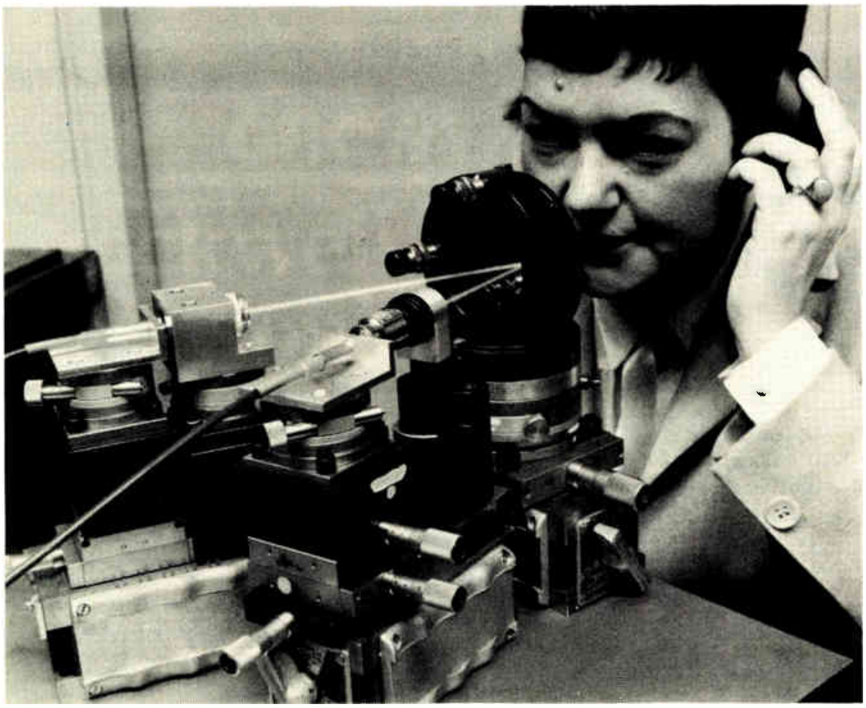
Moreover, the Siemens handset will not even have a light source, reducing parts count still further. The light source would be housed instead in the central exchange that sends the light to the handset over an optical fiber cable.

At the receiver end, the modulated light strikes a photoelectric element that converts the light into electrical signals. These are fed to an electromagnetic earpiece of the kind used in an ordinary phone receiver to produce sound. Another photo element in the receiver serves as the input for an electronically driven horn that constitutes the ringer for the telephone. Light striking the element is converted into electrical pulses and applied via a multivibrator circuit to piezoceramic plates. These, in turn, produce a 2-kilohertz acoustic "ring" signal.

Siemens' laboratory version of the



Central source. Separate transmitter elements of usual fiber-optic phone system (a), are replaced in Siemens' Optophone (b), by "optical microphone." Single light source at central exchange would provide signal carrier for phones in the system.



Light listener. Siemens' Ingrid Fromm tries out laboratory setup of light-powered telephone. She is speaking into vibrating membrane developed to modulate light.

phone carries duplex voice communications over a 20-meter-long fiber-optic cable linking two Optophon sets in different rooms. The light source is a 25-milliwatt helium-neon laser, although in future systems a smaller laser diode could supply sufficient light, according to Fromm. The laser supplies light to the phone only when a call is made.

Membrane. The light strikes the optical microphone's thin membrane made of a soft plastic that has a good surface for holding the aluminum coating. Siemens has made its membranes of Teflon and Kapton but has had the most success with Hostaphan, a polyetheleneterephthalate with elasticity constant in all directions made by the German firm of Kalle in Wiesbaden.

In the lab setup the membrane is 30 millimeters in diameter, 8 micrometers thick, and coated with a reflective layer of aluminum. As words are spoken, the sound waves cause the membrane to vibrate and to vary the angle of reflection of the light. The reflected light is coupled into a second glass fiber in the transmitter, but the movement of the membrane varies the degree of coupling and hence the light intensity in the fiber.

Fromm points out that the two fibers must be precisely aligned with respect to each other if the membrane is to work. This is achieved by placing the fibers along minute guide grooves in the microphone assembly, she says.

The frequency range of the system is from 300 to 3,000 hertz, the common range in telephony. The microphone modulates between 80% and 100%, and modulation distortion is less than 5% over the band.

The Siemens engineers estimate they could build an Optophon link about 2 kilometers long without repeaters, judging from the values they have obtained for fiber attenuation and losses in the optical components. Fromm believes such links would be attractive in short-haul private and military networks. For local public telephone networks, links must be longer—between 1.5 and 3 km without repeaters, the range of line lengths to an average subscriber. Such links will be possible when light sources increase in power and fiber attenuation decreases, she says. □

Peripherals

8-inch disks begin to mushroom

If hardware appears on schedule later this year to back up promises, the on-line memory-storage business for small computers will shape up as a new ball game. The cause: arrival of the 8-inch-diameter, fixed-media (hard) disk drive—an eagerly awaited peripheral that offers several advantages.

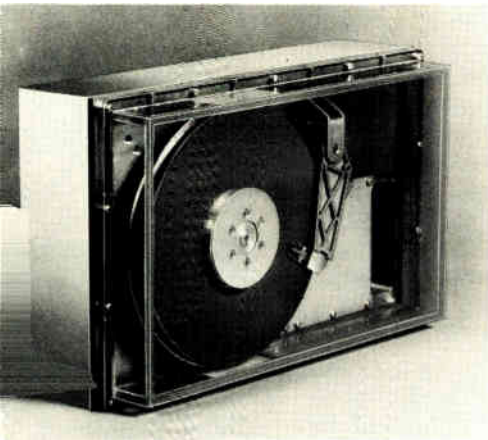
Physically the same size as a floppy-disk drive, the new 8-inch hard-disk units offer some 5 to 60 times the storage capacity and generally can access data 4 times faster than floppies. Though, at an expected price of $1,350 to $3,000, the new drives are anywhere from 3 to 5 times as expensive as floppies, they appear to be an answer to the prayers of small-computer builders for a larger-capacity memory that takes up less cabinet space than current 14-in. hard disks. Based on current Winchester-technology the new drives promise higher reliability, too.

Bowing. New hard drives will surface at next month's National Computer Conference, from Pertec Computer Corp.'s Peripherals division. And other suppliers such as Micropolis Corp., Shugart Associates Inc., Control Data Corp., and Kennedy Corp. will be introducing drives, though not at the NCC.

"It's an onslaught," remarks Stuart Mabon, president of Micropolis in Canoga Park, Calif. "I expect to see as many as 10 companies with them this year. It's the biggest thing in magnetic recording since floppies came on in 1973–75."

Why are hard 8-in. drives bursting out all over in the spring of 1979? In Mabon's opinion, two factors spur the timing. One is IBM's validation of the technology with its own "Piccolo Drive," already being shipped in its small-business System/34 and /38, he says.

Strong user demand is the other factor since the newer 16-bit micro-



Shrink. Rotary position arm helps cut size of Pertec's 8-in. hard disk.

computers require much more memory than floppies can provide.

Also influencing the timing is the improved availability of the disk media itself, adds Lee Benedict, product marketing manager at the Pertec division in Chatsworth, Calif. He points out that the "IMI debacle" slowed other manufacturers by making them more cautious: International Memories Inc., Sunnyvale, Calif., announced the first 8-in. unit last year [*Electronics,* April 27, 1978, p. 40], but was unable to begin deliveries until this January.

Says IMI's director of market support, George Campbell, "Our original plans were on the ambitious side." But now he says IMI is shipping more than 100 a month of its $1,500, 11-megabyte model 7710.

Two directions. The new disk drives seem to be falling into two camps. Some are aimed at directly replacing flexible-disk units. With the same cabinet dimensions as a floppy drive, such units employ conventional stepping-motor positioning, have a typical access times of 80 milliseconds, and limit storage capacity to 5 megabytes or so. In comparison, the floppies have an average access time of 280 to 350 ms and currently store a maximum of 1.6 megabytes.

The other approach follows IBM's lead with its model 62PC 8-in. drive, which has the latest rotary voice-coil positioning, 27-ms average access, and capacities up to 64.5 megabytes and is somewhat more expensive. Micropolis' Mabon and Pertec's Benedict opt for this tack because they see as the heavyweight demand area on-line uses that floppy units never had the performance to meet.

The Pertec drive, model D8000, with 50-ms average access time and up to a 20-megabyte capacity, will be ready for evaluation in August. Samples go for $3,000, and production quantities for $1,800 to start out, with reductions expected as competition heats up.

Micropolis offers its new hard-disk drive, called the Microdisk, for about the same sample price, beginning in June. Access time is 32 ms, in 9- to 45-megabyte configurations. Volume manufacturing is expected by late 1979 at an OEM cost of $1,350 for 1,000 or more.

Kennedy Corp. will have its first drives, yet unpriced and with 4 to 12 megabytes, in late summer, and Shugart's new unit may come in September. Control Data, though, won't name a date. **-Larry Waller**

Radar

Hughes processor has programmability

For the military, putting large-scale integrated devices into airborne gear has been a tough act to get off the ground. Device technology moves so fast that government procurement agencies cannot freeze it into hardware specifications. And development cycles for avionics equipment are long, and, for LSI, there are perennial second-sourcing problems. But an advanced airborne signal processor currently undergoing flight testing in one of the newest multimode radar systems, the AN/APG-65, bids to bring the services up to date fast in the flashy digital LSI world.

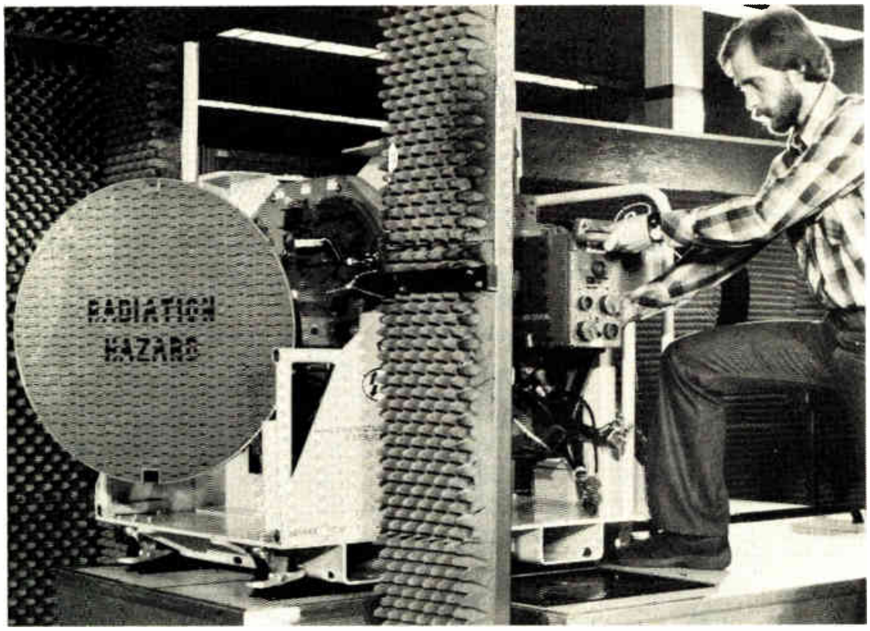
Called a programmable signal processor, it was developed by Hughes Aircraft Co., Culver City, Calif., where a team of designers and software specialists have spent years on it. Their aim is to give the U. S. Navy and Air Force a previously unheard of radar capability: the flexibility to reprogram quickly in the field with tape for different tasks. Present radar systems are locked into hardware that essentially cannot be changed without undergoing extensive redesign.

If coupled with improved radar-beam technology, the new processor could help pick up targets at much longer ranges than at present, and its multimode nature could control firing missiles at many targets simultaneously, rather than singly. The importance of the new radar is underscored by its being rushed into the hottest U. S. aircraft around: the Navy's F-18 Hornet strike fighter. It will also be retrofited into the Air Force F-15. First units will go into aircraft beginning in the middle of 1980.

A combination of advanced LSI devices and innovative computer architecture allows Hughes to build the programmable machine to perform 7.2 million operations per second, much faster than mainframe general-purpose computers. Generally, in signal processing the radar analyzes the return and picks out real airborne targets using special algorithms that sort through such spurious data as unimportant movement on the ground, general clutter, and enemy countermeasures.

Pipelines. Hughes considered that signal processing has a "structured nature, so data and control paths can be kept almost completely separate from one another with little or no penalty," explains Richard R. Fachtmann, assistant manager of the signal processing laboratory at the Hughes Radar Systems Group. This, in turn, allows what he calls the equivalent of "simultaneous fetch" of instructions from separate memories and results in great flexibility for the order in which data is stored and manipulated. The architecture of the Hughes processor, therefore, bears little resemblance to that of a conventional computer, being laid out in separate pipelines for virtually simultaneous parallel execution of instructions.

As many as nine instructions in different phases of execution can be



Extractable. Technician adjusts programmable signal processor developed by Hughes in its position aboard AN/APG-65 radar being set up within an anechoic chamber.

performed at the same time," he explains. The processor is "an ensemble of high-speed pipelined structure, distributed memories, and multiple parallel arithmetic circuits configured to perform particular types of processes."

A mixture of semiconductor LSI technologies chosen for speed implements the processor architecture, including Schottky transistor-transistor logic clocked at 150 nanoseconds and emitter-coupled logic at an even faster 50 ns. This approach puts the parts count at about 12,000, of which 5,000 or so are ICs.

The all-digital nature of the radar and the new processor should yield what the Air Force calls "a new level of reliability," or a mean time between failures of more than 106 hours. Hughes says this is approximately three times better than the best existing radar system, and 10 times that of most of the radars now being used. Such reliability should make the units cheaper for the services in the long run, despite higher initial acquisition costs.

A big contributor to the reliability advance is the proven nature of all its semiconductors, which, Fachtmann says, "come from outside vendors, standard suppliers, all second-sourced." Furthermore, because the unit is divided into 11 plug-in card modules, replacement and repair should not be difficult to perform. **-Larry Waller**

Memories

Mostek to sell IBM add-ons

At a time when suppliers of add-on memory systems for IBM mainframes are being severely squeezed by the late-1978 round of IBM price cuts, Mostek Corp. is quietly making plans to jump into the market with a series of add-ons designed for the top-of-the-line 303X machines.

Officials at the Carrollton, Texas, company say they have already completed advanced tests on the new Mostek 830 series and are now ready to begin marketing the systems to original-equipment manufacturers. The new product line, which also includes an IBM 370/168-compatible system, is scheduled to bow at the National Computer Conference in New York next month.

Ready. Despite one-time industry fears that 16-K dynamic devices would not be fast enough for use with IBM's high-speed 3033 processor [*Electronics*, June 22, 1978, p. 48], the potential timing problems have now been overcome by various interfacing techniques, says Gene Kruschke, large systems program manager for Mostek's memory systems group.

Mostek's 832, 833, and 868 systems will use MK4116 dynamic random-access memories built by Mostek to provide up to 16 megabytes of memory within a single 26-by-30-inch unit for use with System/370 models 3032, 3033, and 168 machines, respectively. Maximum 831 system capacity for use with the IBM 370 model 3031 processor is pegged at 8 megabytes using the same 16-K chips.

Among other things, Mostek is counting on a system design optimized for both easy field maintenance and easy upgrading to next-generation chips to give its product line staying power in the $500 million IBM add-on marketplace. By selling only to OEMs, the firm will be going head to head against Intersil Inc. The Cupertino, Calif., company is the prime force in the OEM add-on market, since National Semiconductor reportedly lost much of its OEM base following its move to begin marketing to end users last year.

Homegrown. Kruschke contends that by building its own chips, Mostek will have an edge over Intersil, which also has a new family of add-on systems that use 16-K dynamic chips. Unlike Mostek, Intersil is expected to purchase its 16-K RAMs from an outside vendor.

As Kruschke sees it, Mostek's major competition in the 303X add-on market will come from Intersil and from Intel Corp., which markets its systems directly to end users. Other competitors, he believes, will become less of a factor in part because of continuing downward price pressure, which followed IBM's cutting of end-user prices by 30% to $75,000 per megabyte last year [*Electronics*, Dec. 21, 1978, p. 38].

Because Mostek will market only to OEM customers, prices for the 830 series, to be competitive with Intersil's, are unavailable.

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currently selling 1 megabyte of memory for $50,000. The systems are built with 4-K static devices. According to Kent Mueller, marketing director for Intel's Commercial Systems division in Phoenix, the company has no plans to go to higher density chips this year. Instead, Mueller indicates, it will wait until 16-K static chips are available, rather than changing current board designs to accommodate 16-K dynamic parts. **-Wesley R. Iversen**

Solid state

C-MOS touch given micros, op amps

Operational amplifiers are usually built with bipolar transistors, and microcomputers most often use n-channel devices, but Intersil Inc. says one technology can do both well: complementary MOS. In fact, with the addition of a one-chip microcomputer family and a line of operational amplifiers, the Cupertino, Calif., company will have nearly reached its goal of across-the-board C-MOS alternatives to analog and digital integrated circuits.

Each of the two latest product announcements (see "Intersil's C-MOS drive")—which include 11 op-amp offerings spun off a single design and the first members of a microprocessor family that mirrors in C-MOS the popular MCS-48 line from Intel Corp. in nearby Sunnyvale—is significant beyond the lower power requirement inherent in this technology. The op amps, for example, can operate with a supply of as low as ±0.5 volt—significantly less than the ±1-V bipolar op-amp design touted by National Semiconductor Corp. [*Electronics*, March 29, 1979, p. 115].

Other phases. Also, the C-MOS op-amp design offers a programmable quiescent current that may be set between 10 microamperes and 1 milliampere, according to the bandwidth and current-drive capability required. Further, the devices have an input impedance even higher than that of op amps built with junction field-effect transistor—10^{12} ohms.

The first microprocessor part, Intersil's IM87C48, has erasable programmable read-only memory (E-PROM) on chip and is therefore equivalent to Intel's 8748 prototyping version of the ROM-based 8048 microcomputer. Making it is to Intersil's credit, since the E-PROM process, a tough one by any measure, is even more difficult to combine with a microcomputer circuit.

The company's E-PROM expertise comes from experience with its 6653 and 6654, 4-kilobit devices that are the only C-MOS E-PROMs on the market. Its 87C48 is not only pin- and function-compatible with the Intel part, but offers an extended operating temperature range—also inherent with C-MOS—of −40° to +85°C.

The main attraction of Intersil's latest C-MOS efforts, however, is in the low power. "We can now offer a complete data-acquisition system—from analog-to-digital converter, sample-and-hold circuits, amplifiers, and multiplexers, all the way to the digital controller—in C-MOS," says Jerry Zis, director of analog product marketing, "and the entire system can be battery-operated."

The one-chip microcomputer is a natural in C-MOS—battery-operated equipment such as handheld data loggers which cannot afford the ½-watt consumption of the 8748, can serve the 50-milliwatt worst-case dissipation of the 87C48. Moreover, the C-MOS part can operate in a standby mode with its clock stopped, drawing a scant 500 microwatts.

Prices. Since it is a prototyping part, the 87C48 carries a high price tag of $82.50 in unit quantities, but that is not much more than the Intel equivalent. Other parts in the microcomputer family will be priced at a 10% to 20% premium over n-channel equivalents. **-Raymond P. Capece**

Intersil's C-MOS drive

The goal of Intersil is shared by both analog and digital product areas: to establish complementary MOS in those standard products where the low-power technology was not exploited before. Here are the new families.

As for linears, in all, 11 op-amp products are available, all built around one basic design. Variations in the 76XX family, packaged as single, dual, triple, and quad versions, include:

- Programmable quiescent currents of 10 microamperes, 100 μA, or 1 milliampere.
- Externally compensated versions for optimizing ac characteristics.
- Versions with common-mode input protection to 200 volts.
- A version that allows input voltage swings to exceed supply voltages.

In the digital area, Intersil will at first closely parallel Intel Corp.'s MCS-48 and MCS-41 families of microcomputer chips, then will branch off to proprietary products that best serve the low-power market. To begin:

- The 87C48, equivalent to Intel's 8748, single-chip microcomputer with 1 kilobyte of erasable programmable read-only memory and 64 bytes of random-access memory. Samples are being shipped now.
- The 87C41, equivalent to Intel's 8741 programmable peripheral interface chip. Samples are being shipped now.
- The 80C48 and 80C41, masked-ROM versions of those two parts, due at year-end. Also coming is a proprietary 2-kilobyte version of the 80C41.
- The 80C49, equivalent to Intel's 8049 one-chip microcomputer with 2 kilobytes of ROM and 128 bytes of RAM. Samples will be ready by year-end.
- The 80C35, equivalent to Intel's 8035, which has 64 bytes of RAM but uses outboard ROM for program storage, due at year-end.

Trade

China seeks Western technology

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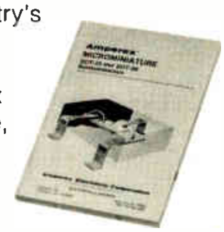

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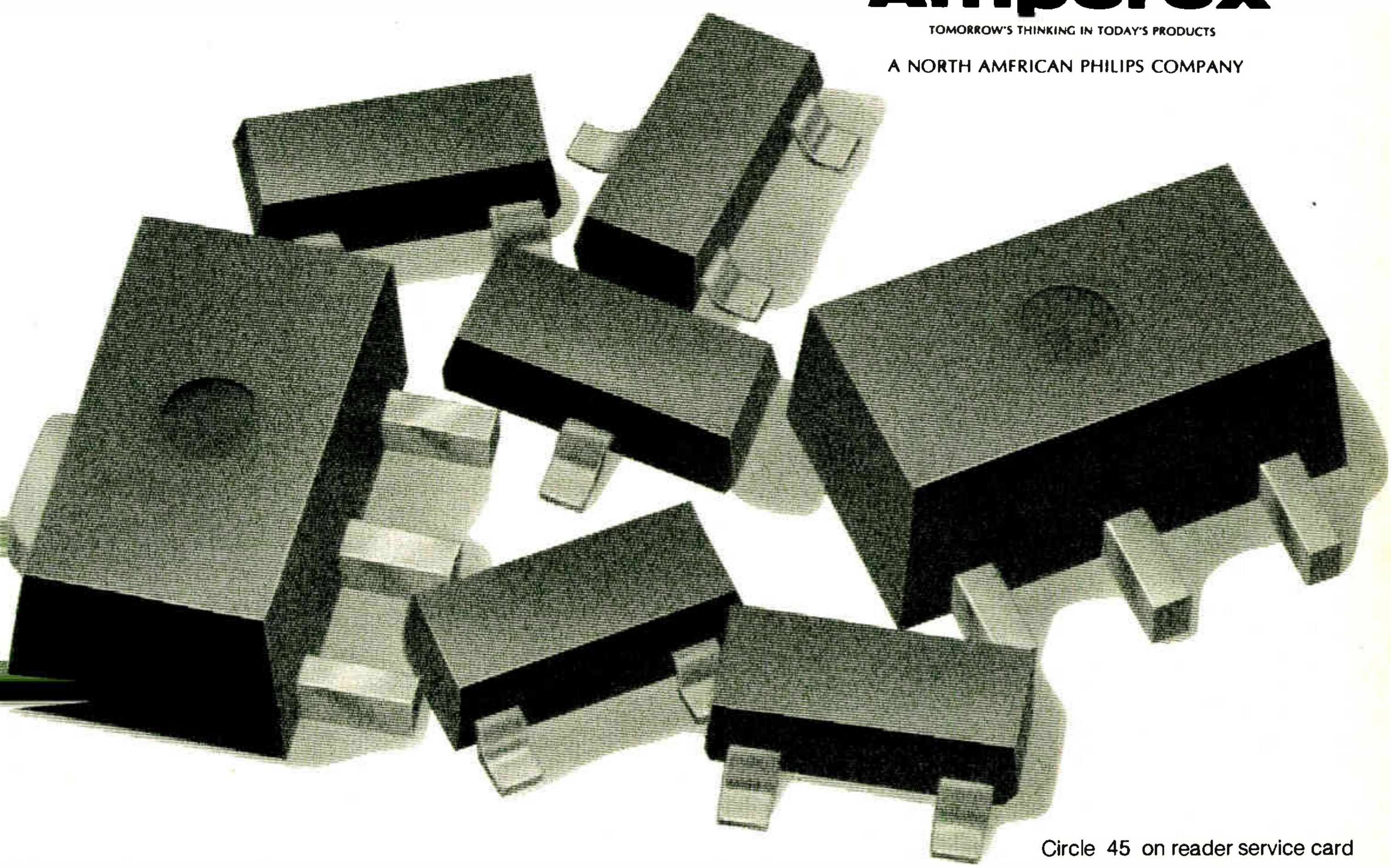


At Electro. China's Luo Pei-lin spoke of technological partnerships.

now leading the Western world into a second Industrial Revolution. That is the thrust of the message delivered by Luo Pei-lin, vice president of the Chinese Electronics Society, late last month at Electro79, the annual convention of the Institute of Electrical and Electronics Engineers held in New York City.

At a panel discussion on electronics problems and opportunities around the world, Luo made clear China's interest in technological partnerships. It wants external assistance—initially as imports to meet the demand for products, but also as help in building up domestic industries quickly to meet that demand. He called self-sufficiency China's most important goal. There is little interest in developing an export industry, he said.

The Chinese also want to improve engineering education. While not mentioned at the Electro session, the Chinese Electronics Society has asked the IEEE about ways to sponsor study in the U.S. (The CES corresponds to the IEEE's elective societies, the Chinese Electrical Engineering Society corresponds to the IEEE's power society.)

Prominent in the work going on in China are space electronics and computer projects. Seven domestic satellites have already been launched and plans are under way for satellite communications systems. In computers, the Chinese have a series of million-instruction-per-second mainframes and Nova- and PDP-11-compatible minicomputers in production. Chinese semiconductor makers are just now going to medium-scale integration, Luo said, with work under way in all major processes. Research has also begun in fiber optics and bubble memories.

An IEEE delegation to China last year reported that electronics manufacturing needs considerable modernization [*Electronics*, Jan. 4, 1979, p. 92]. Luo confirmed at Electro that production is definitely one area where China needs outside expertise.

Other speakers at the panel of top executives, chaired by Texas Instruments' president J. Fred Bucy, emphasized how determined their nations are to overtake the American lead in advanced electronics technology. Among the points made:

- Japan's VLSI project, due to end next March, will see the basic technology it has developed applied by the six semiconductor firms that worked with the government, said Michiyuki Uenohara of Nippon Electric Co. It looks as though each firm will go its own way in designing the mainframe computers that are the project's ultimate goal.
- Germany is about to launch a major program to strengthen domestic VLSI programs, said Hans Reiner of Standard Elektrik-Lorenz. In part, the effort is spurred by the failure of U.S. semiconductor makers to provide adequate design assistance to overseas system houses and to match the low reject rates of similar Japanese products, he said.
- The British government is acting as a venture capitalist in funding Inmos Ltd., the new semiconductor maker, because the country has done so poorly in translating its impressive research and development efforts into products, said Ian Mackintosh of Mackintosh Consultants Ltd. of England. Also planned is an office-electronics project.
- France is bent on strengthening all its electronic industries as replacements for other, dying industrial sectors, said Pierre Bonelli of Sema-Metra. Semiconductor advances are the key, he says, so the government is encouraging technology exchanges and joint ventures with American firms. **-Benjamin A. Mason**

Companies

Fairchild's situation attracts takeover

It should come as no surprise that Fairchild Camera and Instrument Corp. would be a takeover target for a company like Gould Inc., a $1.8 billion conglomerate headquartered in Rolling Meadows, Ill., near Chicago. Fairchild, in Mountain View, Calif., reportedly has been closely scrutinized by several companies with a takeover in mind the last few years.

Buy in. "Basically, there's a lot of interest out there in semiconductor manufacturing and technology," observes one industry analyst. He points out that the easiest way for a nonelectronics company to get into the business is by acquisition. Fairchild, with $534 million in 1978 net sales, has a reasonable enough size and reputation to be attractive.

But Silicon Valley neighbors speculate about other factors that may be sparking interest in Fairchild. One obvious one is that "there aren't a whole lot [of semiconductor makers] available to buy," as an industry analyst notes. He points out that large companies that are not growing very fast often become takeover candidates partially because prospective buyers think they can improve operations.

Fairchild, long the spawning ground for new companies, technology, and talent, has not matched the brisk growth rate of some of its newer competitors. Intel and National Semiconductor, for example, are growing some two to three times faster.

Moreover, Fairchild's net 1978 income was only $24.8 million, and royalties from patents, which contributed $10.8 million to pretax profits, are due to stop at the end of this year, according to a spokesman for the company.

Some observers blame this performance on unfocused management. Responds a Midwestern executive who buys quantities of Fair-

Electronics review

child microprocessors on hearing of Gould's $300 million offer in cash and common stock: "It's great news for us because Gould has a reputation as a good manager, and that's what Fairchild needs."

Strong points. To be sure, at over half a billion dollars in sales, Fairchild is making its mark. Its well-respected Sentry and Xincom automatic tester lines, for example, are selling very well, pouring in more than 23% of the total 1978 sales. Its bipolar technology is an industry leader, and its military business is a good deal larger than is commonly realized, according to one company executive.

However, some believe that Fairchild's future as a strong electronics company will depend on key changes. "In my mind, one big mistake for the last decade now is in the MOS area," observes Mel Eklund, vice president of Integrated Circuit Engineering Corp., a Scottsdale, Ariz., consulting firm.

"They're not really pushing MOS with their heart in it," he continues. "They apparently seem to feel that their bipolar prowess will pull them out of it." He says that Fairchild's bipolar capability is good, especially the 100K emitter-coupled-logic family, but wonders how large that market really is.

Gould, though primarily known for its battery technology, has been expanding its production base the last several years through mergers and acquisitions that include electronics-oriented firms. A company like Fairchild would position it to capture a bigger share of the growing electronics marketplace, Gould executives believe.

In 1977, Gould bought Modicon Corp., a leader in processor-based programmable controllers. It followed with two other electronics company purchases in 1978: Hoffman Electronics Corp., an El Monte, Calif., maker of navigation and communications gear; and Biomation, a Santa Clara, Calif., leader in digital logic analyzers. Gould also developed the ink-jet printer used by IBM that has been licensed to other vendors. **-William F. Arnold**

Software

TI offers routines in plug-in ROM

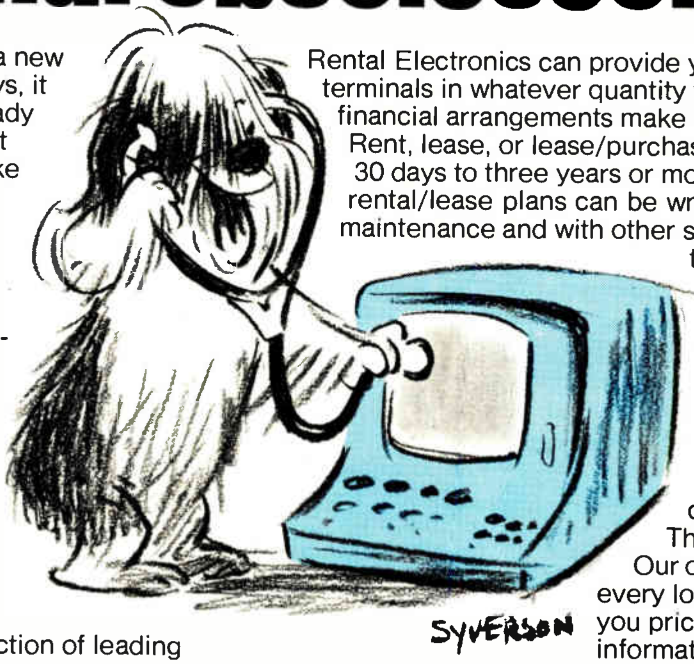
With more of its new products aimed at industrial process control and other applications, Texas Instruments Inc. is offering a series of executive software routines. The series is packaged in plug-in erasable-programmable read-only memories that offer sophisticated program development to a not-so-sophisticated computer user.

Referred to as Timber (for TI Modular Based Executive in ROM), the new package was announced last week. Timber is housed in four 2716-type E-PROMs used in conjunction with TI's low-priced TM990/302 module-level development system [*Electronics*, Dec. 7, 1978, p. 82]. With user-summoned routines that can be employed in building-block fashion, Timber is a subset of TI's earlier TIPMX package (TI Pascal Microprocessor Executive) announced last year.

But unlike its predecessor, Timber does not require a 990 minicomputer development system. With a Timber package, a 302 development module, a 990/201 memory expansion board, and a terminal, a user can have—for as little as $3,200—a system capable of developing a typical industrial-process applications program using assembly language routines and with a minimum of programmer effort, according to TI officials.

Timber routines packaged in ROM provide end-application capabilities including memory management, interrupt servicing, real-time clock handling, interprocess communication, and synchronizing priorities in multitask environments. With the plug-in ROMs and the 302 module, the link-edit abilities associated with sophisticated software development systems are not required. The configurable Timber package comes with documentation that helps take the inexperienced user through a demonstration process in the erasable ROM, which is later erased and

How Rental Electronics helps you avoid terminal obsolescence.



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Hewlett-Packard 2621A/P Terminals Enhanced 9 x 15 dot character cell, full 128-character ASCII character set in 24 80-character lines. Two pages of continuously scrolling memory. RS232C and Bell 103A compatible. 110 to 9600 baud. 2621/P includes built-in printer operating at 120 cps.

Tally T-2000 Hush-Tone Line Printer Acoustically designed enclosure. Operates at 125 (Model 2100) and 200 lines/minute (Model 2200) with standard 64 character USASCII. Line spacing switch selectable, 6 or 8 per inch.

ADDS Regent 200 Terminal 24 lines x 80 characters, 25th "status" line shows operating mode. 128 character ASCII. RS232C/CCIT V.24 communications interface operating 75 to 19.2 BPS, switch selectable. Buffered transmission, auxiliary ports.

Beehive Micro B 1A Terminal 128 ASCII character set; switch selectable scroll/non-scroll mode; X-Y addressing; 24 x 80 display format; single key memory lock; fully buffered communications to auxiliary peripheral device.

Lear Siegler ADM-3A Data Entry Display Terminal 12" diagonal, 24-line screen. 64 ASCII characters. Full or half duplex operating modes, switch selectable, baud rates from 75 to 19,200. RS232C interface, 20mA current loop.

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Circle #49 for information

display it first showed last summer as the keyboard for the system. The flight progress strips are, in effect, displayed on this CRT terminal, together with a list of commands for moving and changing the data.

Matrix. An array of infrared beams crisscrosses the face of the CRT from the top, bottom, and sides. The beams are produced by light-emitting diodes placed about a half inch apart. The controller selects information displayed on the screen by touching it with a finger and breaking the beams. The beams are aimed to overcome parallax problems common to a curved viewing area. Logic determines the selection.

Sanders will deliver a computer subsystem and six consoles, each consisting of two 25-inch CRTs, the interactive display, and data-entry devices, to the FAA's National Aviation Facilities Experimental Center in February 1980. If the system proves satisfactory, all 20 en-route traffic control centers around the nation should have the system in place by 1984, according to Edwin J. Rearnick, Etabs systems manager at Sanders. **-Pamela Hamilton**

Computers

Barton receives architecture award

As electronics technology has gotten more complex, it has bred specialties among its practitioners. One of the newest coming into prominence is computer architecture. Now it is important enough to have its own award for excellence.

The Institute of Electrical and Electronics Engineers' Computer Society and the Association for Computing Machinery created the award—which includes a $1,000 check—this year and appropriately enough named it after John Mauchly and J. Presper Eckert, the inventors in 1946 of Eniac, the first electronic digital computer.

Late in April, at the Sixth Annual Symposium on Computer Architecture in Philadelphia, the two pio-

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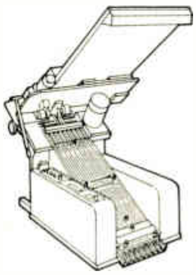

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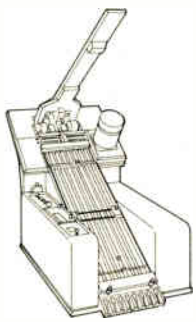

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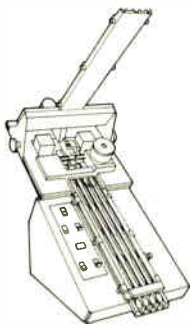

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Circle 53 on reader service card

Architects. Computer system designer Robert Barton of Burroughs Corp., right, received his award for achievement in architecture last month from computer pioneers John Mauchly, left, and J. Presper Eckert.

neers presented a certificate and the check to the first winner of the Eckert-Mauchly award to Robert Barton, director of systems organization research at Burroughs Corp.

Leader. Barton lead the team that designed Burroughs' first large computer system some 20 years ago. Labeled the B5000, it was one of the first commercial computers to feature virtual memory, a master control program operating system and a multiprogramming capability that allowed more than one program to be executed simultaneously—items that have since become commonplace.

Also, as the award noted, Barton pioneered in the concept of designing computer hardware and software at the same time. Summing up, the award credited Barton with helping to make "computers simpler to understand, simpler to engineer and construct and easier to use for everyone's benefit."

In accepting the award, Barton noted that it was an article on Eckert and Mauchly's Eniac that first hooked him on computers. "I'm honored to receive this award because these two are as close to being my heroes as anyone."

Barry Borgerson, director of research and technical planning at Sperry Rand's Univac division, Blue Bell, Pa., and chairman of the conference, said that the symposium was evidence that "architecture is growing as a field of preference. Now it has established an award to recognize accomplishment in that field." **-Anthony Durniak**

SCIENCE/SCOPE

The first production model of a radar that can track an artillery shell in flight and determine its origin before it hits has been delivered to the U.S. Army for tests. The Hughes-built system, called the AN/TPQ-37 artillery-locating radar, is designed to let crews return hostile fire more quickly and accurately than ever before. The system erects a sensitive electronic barrier over a broad area and can detect any projectile piercing the screen. After tracking a shell and plotting its path, the system's computer backtracks the trajectory to the firing location. The TPQ-37 is similar to the smaller, highly mobile TPQ-36 that Hughes developed for locating hostile weapons.

Communications via satellite continue to cost less every year despite inflation. The International Telecommunications Satellite Organization, crediting improved technology and efficiency of its Intelsat network of satellites, has cut its monthly charge for a full-time, two-way telephone circuit by 16 percent to $960. The same service in 1965 initially cost $5334. If that charge had risen with inflation, the cost today would be about $11,000. Intelsat, a consortium of more than 100 nations, has lowered its rates for nine consecutive years. The satellites presently providing the service were designed and built by Hughes.

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A newly developed closed-cycle cooler that chills the Sidewinder missile's infrared sensor to -320 degrees F will simplify logistics support and reduce life cycle costs. The air-to-air missile's infrared eye must be super-cooled to increase its sensitivity to a target aircraft's engine heat. In the past, the Sidewinder has used an open-cycle nitrogen or argon gas cooling system that needed complex logistics support and could be turned on only for limited intervals before needing recharging. With the new closed-cycle cooler, a combat pilot may leave the missile sensor on throughout a mission with no concern for mission duration.

Under contract to the U.S. Air Force, Hughes built 10 advanced development models of the closed-cycle cooler, which are now undergoing tests. An additional 42 coolers are being built for evaluation and flights tests under an AIM-9L product improvement contract (AIM-9M) with the Navy.

Five-year plan of FAA held inadequate . . .

The Federal Aviation Administration's proposed 40% boost in fiscal 1981 spending to $350 million for airport facilities and equipment is already drawing fire from Congress and some segments of the general aviation community—as well as from avionics makers who would be the principal beneficiaries and feel the increase is inadequate. The five-year program, called the Airport and Airway Improvement Act of 1979, calls for expenditures of $6.6 billion beginning with the fiscal year starting Oct. 1, 1980. Facilities and equipment budgets would be increased by annual increments of $35 million, raising funding to $490 million in 1985. But critics note that even the FAA concedes that **the bulk of the $1.2 billion for facilities and equipment would be used only to modernize existing physical facilities,** with the remainder going for air traffic control.

. . . as proposed 6% avionics tax irks Congress

Lobbyists for makers of avionics are upset with the FAA proposal to levy a 6% excise tax on sales of new avionics and aircraft for noncommercial aviation. So are general aviation users, already unhappy with the FAA's proposal of a 10% tax on retail fuel for general aviation only, replacing an existing tax of 7 cents on each gallon. The FAA defends the changes by noting that the new taxes **would raise general aviation's contribution to FAA service costs to only 25% from the present 14% level.**

FAA money for research, engineering, and development in Transportation Secretary Brock Adams' proposal would start at $90 million in fiscal 1981 and rise $5 million per year for a five-year program totaling $500 million. Congressional committee staffers are critical of this aspect of the plan and of its provision permitting the FAA to carry over unspent funds to future years. "Both the carry-over provisions and the neat incremental increases for both R&D and facilities and equipment clearly indicate that [the] FAA has no firm program plan," says one House committee analyst. "They are simply guessing at costs. And the carry-over provisions would only give them a bankroll to cover whatever they finally decide on."

FCC may simplify licensing rules for Satcom receivers

The Federal Communications Commission is considering dropping its licensing requirement for receiver-only satellite earth stations after another Government agency protested that the process is unnecessary, costly, and time-consuming and slows technological growth. The Commerce Department's National Telecommunications and Information Administration (NTIA) wants the FCC to replace licensing with a requirement that **earth station owners file geographical coordinates and proposed use of terminals.** Prior notice would allow communications carriers like telephone companies to protest possible microwave signal interference by earth stations and protect against unauthorized use of broadcast satellite signals.

Satcom scanner, digital TASI readied by AT&T

Bell Laboratories is pushing to improve communications satellite capability and efficiency with a system "that would concentrate a satellite's transmission in a narrow beam sweeping across the country, **somewhat as an electron beam in a television set scans a screen,"** according to Billy B. Oliver. The vice president for planning and design for AT&T's Long Lines division told a Senate hearing that the satellite scanning transmitter would be in addition to a system's several fixed beams to serve major metropolitan areas.

AT&T is also researching an advanced digital version of the time-assigned speech interpolation (TASI) technique for domestic use that **"would nearly quadruple the call-handling capacity of a group of circuits without degrading quality."** The initial analog version of TASI, introduced into overseas calling in the early 1960s, interjects other transmissions into the natural conversational pauses that account for 60% of a circuit's time. Oliver says AT&T expects to begin offering the benefits of such technologies to private-line customers after July, when the Federal Communications Commission moratorium is lifted on direct AT&T competition in the domestic satellite market.

White House using Congress as lever on Japan trade

Growing congressional threats to impose trade sanctions against Japan are privately delighting the White House. Chairman Charles A. Vanik of the House Ways and Means subcommittee on trade says **the group's consensus is to prohibit Japanese companies** from competing for some $10 billion in U. S. Government procurement of electronics, office machines, and automobiles unless Japan opens purchases by Nippon Telegraph and Telephone Public Corp. to U. S. competition. "We're really upset about NTT's policy," says the Ohio Democrat, whose subcommittee will get first crack at the multilateral trade treaty now in final negotiations. Although Ambassador Robert S. Strauss, special trade representative for President Carter, outwardly opposes congressional action that would limit his freedom to negotiate, one White House staffer sees the threat of congressional sanctions as "the best lever we've got. Vanik's proposal makes our plan much more palatable by comparison."

Engineering foundation proposed for U. S. by IEEE's Weinschel

The creation of a National Engineering Foundation to help accelerate U. S. productivity and innovation was proposed to the Institute of Electrical and Electronics Engineers by Bruno Weinschel, president of Weinschel Engineering Co., Gaithersburg, Md., and an IEEE vice president. Weinschel says an engineering parallel to the National Science Foundation (NSF) is necessary **because NSF's orientation to basic research limits its usefulness in areas of productivity and innovation** with applications appearing only "after a delay of one or two decades." He also believes universities must offer more applications-oriented courses so the U. S. can "reestablish our competitiveness in sophisticated manufacturing engineering." He also wants increased support of research and development by companies with less than 1,000 employees.

California tests of energy control set for July

Southern California Edison Co., working with AT&T, is to begin tests in July using residential telephone lines that will not only read electric meters and monitor peak demand but will also permit the utility to prevent overloads by remotely cycling down power to individual users. This was disclosed to a Senate hearing at the end of April by AT&T vice president Dennis Sullivan, who is responsible for residential market management, planning, and product management. Sullivan told the Commerce, Science, and Transportation communications subcommittee that the tests in Southern California's Valencia-Newhall area will let the utility **"remotely cycle down power to swimming-pool heaters, pumps, air-conditioners and the like."** To obtain customer evaluations of two-way home-information systems using telephone lines, AT&T also is readying a six-month test involving 160 customers in the second 1980 quarter.

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For complete technical data, write for Engineering Bulletin 6250B to: Technical Literature Service, Sprague Electric Company, 35 Marshall Street, North Adams, Mass. 01247.

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Sample Listing

① **Jones, John J**
② Chmn & CEO, Microprocessor Div of Computers Inc, 1023 W Warner Ave, Dayton, OH 45479, Tel (513) 555-2000. ③ **Born:** Mar 26, 1926, Philadelphia, PA. ④ **Education:** MBA, Harvard Business School, 1950; BSEE, Univ of Ill., 1946; PhD (Hon), Yale Univ, 1977. ⑤ **Professional Experience:** Natl Bur of Standards, 1956-74, Adm Eng; Litton Ind, 1954-56, Sr Eng; NCR Corp, 1950-54, Eng. ⑥ **Directorships:** Computers Inc since 1975. ⑦ **Organizations:** IEEE since 1946, Sec Head 1972-73; AAAS since 1971; Midwest Ind Mgt Assn since 1974. ⑧ **Awards:** Fellow, IEEE, 1977; Public Service Award, City of Dayton, 1976. ⑨ **Patents Held:** 8 in computer circuits, incl Special Circuit for Microcomputer Chip Design 1975. ⑩ **Achievements:** founded Microprocessor Inc 1974; project manager on first application of microprocessors for standard interfaces 1975. ⑪ **Books:** 4 incl *Small Circuits and Their Applications* (editor), McGraw-Hill, New York, 1975. ⑫ **Personal:** married 1950 to Mary (Smith), children John Jr, Jane Anne, Kevin. ⑬ **Residence:** 344 W 34th St, Dayton, OH 45403, Tel (513) 555-4343.

① Name
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⑤ Previous affiliations/dates/highest positions
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Contents

Fax system uses ink-jet printer

Noiseless ink-jet recording on plain paper is one feature of a facsimile transmission system that West Germany's Siemens AG has introduced and will deliver shortly. Another is that **the equipment allows automatic reception,** which means an operator need not be present when messages are coming in. Designated the HF2050 and about the size of a normal typewriter, the equipment uses an ink-jet printer with 12 nozzles. When printing at 3 minutes per page, the printer records messages with a density of 3.85 lines/mm. The density at two minutes per page is 3.08 lines/mm. Price of the system is approximately $6,300.

Philips sees small overall growth for color TV sales

The world market for color TV sets will rise 3% this year, and the developing countries will help stabilize the market for black-and-white receivers. That's the gist of a forecast made by NV Philips Gloeilampenfabrieken in the Netherlands. Breaking down the total market (without the Eastern Bloc and China) into major areas, Philips sees Europe and Japan scoring an increase in color set sales of 7% and 5%, respectively, this year. **Latin America should come in at 14%,** it predicts. The U. S., on the other hand, will register an unspecified decline. As for the 1979 black-and-white receiver market, sales in Europe will drop by 2% to 3%, while those in Japan and the U. S. will go down by 5% and 8%, respectively. Offsetting these declines will be rising sales in the Third World.

GEC, Philips eye private office information market for viewdata systems

Convinced that the business sector will be the first to pay off, Britain's General Electric Co. Ltd. and now Philips Data Systems Ltd. are offering private office information systems using low-cost viewdata terminals and accessing the customer's own computer-controlled disk data base. **Such systems, using privately developed viewdata software, would be one tenth the cost of conventional on-line cathode-ray-tube terminals** and would meet a general requirement for recording, storing, and accessing office and shop-floor information. GEC Private Viewdata Systems Ltd. will use Data General's NOVA minicomputers for small office systems of up to 32 data ports and its own GEC 4060 for larger installations. Its 4000 series computers are already used in the now public Prestel service, the British Post Office's viewdata service, and in the first private viewdata system supplied to a Dutch publisher. Philips plans to use its P857 office minicomputer with magnetic disk but will later add its optical disks [*Electronics*, Nov. 23, 1978, p. 75] as a low-cost archival store and is preparing a viewdata interface for its WP5000 word processor.

SEMS expanding both ends of its two mini lines

SEMS, the minicomputer subsidiary of France's Thomson-CSF in the Paris suburb of Louveciennes, is enlarging its Mitra and Solar lines at both the top and the bottom. The company says the unveiling in late April of its Mitra 225 is only the first in a series this year. François de Villepin, director of Thomson's computer group, says the Paris-based conglomerate is placing an especially high priority on the low end of both lines in order **to cash in on what he believes will be a burgeoning market for office computers in Europe.** The Mitra 225, which fits in at the top of its line, is built around what SEMS calls a "Monobus," capable of handling 1,200 16-bit words per second. Main memory capacity is 512,000 16-bit words; the central processing unit uses four 4-bit-slice microprocessors. The basic unit, with 32,000 words of MOS memory, costs about $20,000.

International newsletter

West Germans make blue LEDs using silicon carbide

Using a technology worked out at the Technical University of Hanover in West Germany, researchers at Siemens AG have developed experimental blue-light–emitting diodes based on silicon carbide. **The diodes' forward voltage is 4 V at 50 mA.** Their external quantum efficiency at an emission wavelength of 480 nm is 4×10^{-5}—about one hundredth that of commercial nitrogen-doped gallium-arsenide-phosphide LEDs. Although lab samples have already been made, Claus Weihrich, who heads the LED development team at Siemens' research labs in Munich, cautions that "volume production of blue LEDs cannot be expected in the near future because large-area single-crystal silicon-carbide substrates cannot be made." Even so, the company is convinced that silicon carbide is a more promising material for blue LEDs than gallium nitride or zinc sulfide, which other firms are working with.

British Post Office to set up experimental teleconferencing system

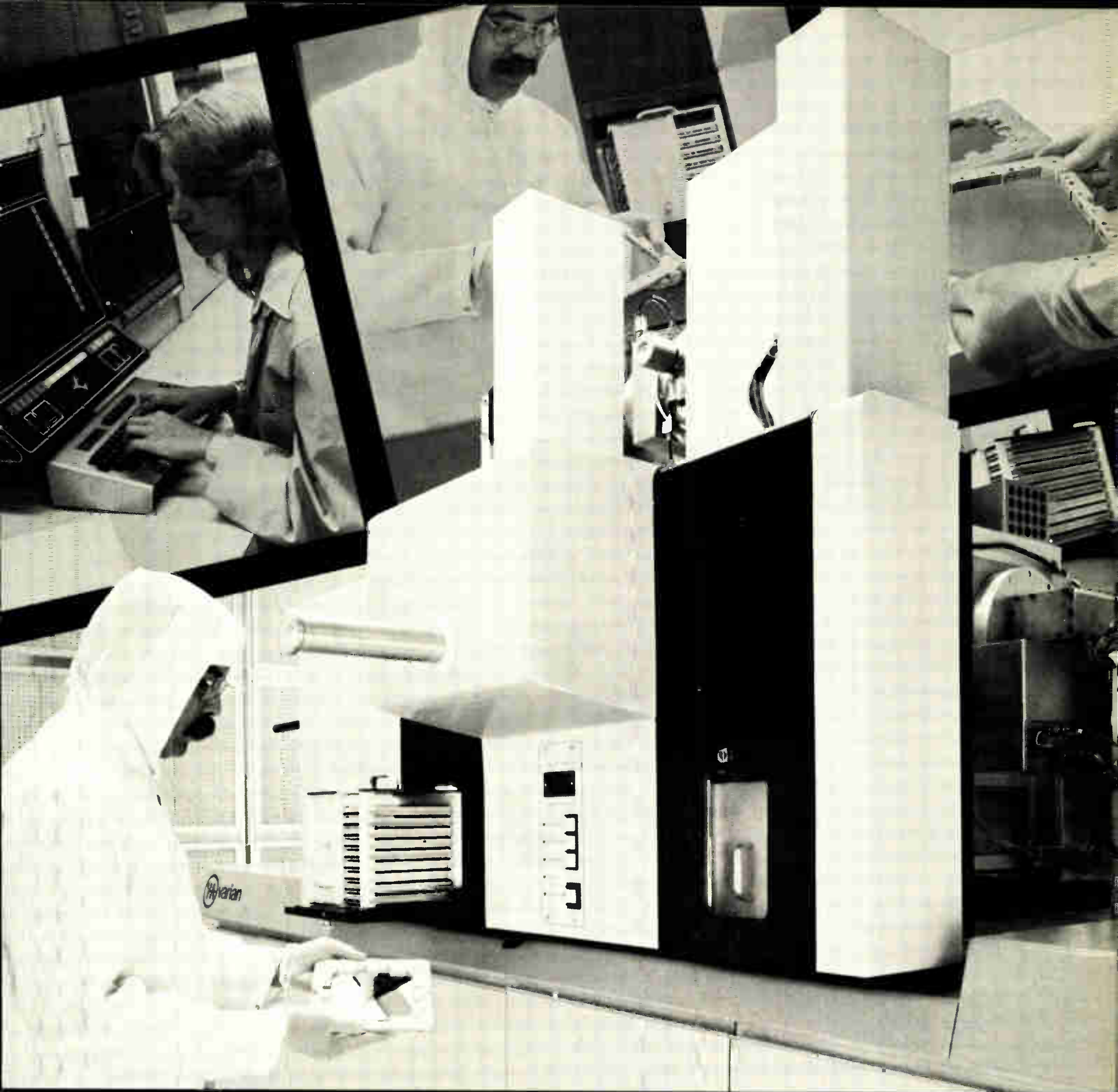
The British Post Office is planning an experimental teleconferencing service for 1981 that would provide for meetings of up to four people on a customer's premises together with slow-scanning 625-line transmission of documents and sketches ("scribble pad"). At present, the post office provides a 625-line, 5-MHz "Confravision" service—similar to the Bell System's Picturephone service in the U.S.—between studios in five cities using broadband trunk microwave links. But by reducing TV standards to a 313-line, 1-MHz bandwidth, engineers at the BPO's Martlesham, Ipswich, research center aim to **pipe the signal over the local telephone network using existing twisted-pair telephone lines.** Document and scribble-pad transmission will be provided via a 4.8-kb/s modem over the switched telephone network, allowing a refreshing rate of 50 seconds and 5 seconds, respectively. Use of a private 48-kb/s modem and line cuts these times by 90%. The year-long trial, to involve 50 terminals, will determine the need for and requirements of such a public service.

Implant-isolation technique moving to device stage

High-density n-MOS electrically alterable read-mostly memories and high-reliability discrete transistors with extremely low leakage currents are just two applications slated for a novel technique of dielectric isolation in which oxygen is implanted into silicon. The technique is now being developed at the University of Kent at Canterbury in collaboration with Middlesex Polytechnic, with the help of a small $8,000 grant from Britain's Science Research Council. It works by **implanting oxygen into a silicon substrate to form a buried silicon-dioxide dielectric layer.** After annealing, the top layer of silicon is of sufficiently good quality to grow an appropriately doped epitaxial layer, thus forming an isolated silicon pocket as in a silicon-on-sapphire structure. The researchers have proved the feasibility of the technique and now want to produce working devices.

Thomson-CSF unit to make memories for Amdahl computers

Thomson-CSF, the French electronics conglomerate, will be making MOS memories for Sunnyvale, Calif.-based Amdahl Corp.'s mainframe computers at its new plant in Ireland. The three-year contract, rumored for months, is with Thomson's Citec (Compagnie Industrielle pour les Techniques Electroniques) subsidiary, which will manufacture memories of up to 16 megabytes at its plant in Toulouse. Thomson says **the contract will give Citec experience in high-density, multilayer printed circuits** that could enable Thomson to compete in the U. S. market.



This is the most technically advanced Electron Beam Lithography System you can buy.

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Circle 65 on reader service card

Analog LSI testing

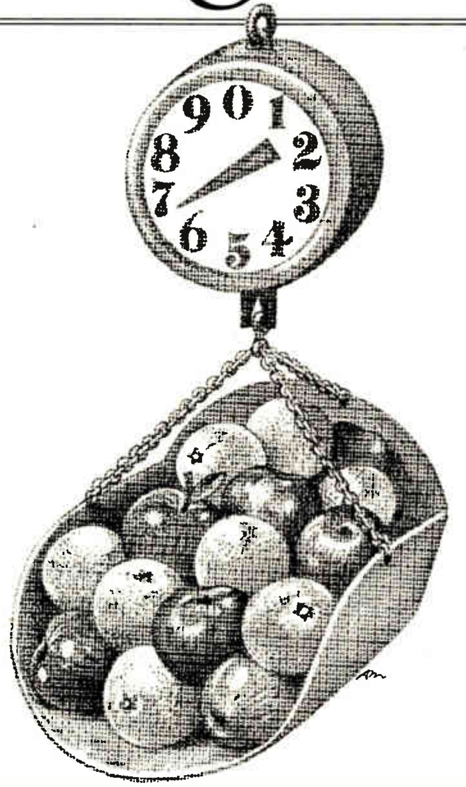
Measuring Apples and Oranges together.

According to the ancient wisdom, one can't mix apples and oranges in the same operation. But, as you well know, recent advances in integration techniques, by combining both linear and digital circuitry on the same substrate, have created just such a mix.

Moreover, the new technology promises to spawn a revolution every bit as dramatic as the growth of EDP. So measurement or testing of these exciting yet complex devices will soon have to be achieved consistently in high-volume production.

Expectations of explosive growth derive from the fact that analog LSI has now made possible efficient and economical Analog Signal Processing (ASP). Demand for ASP in electronic control applications is already high, pent up for many years in such major markets as telecommunications, home, automotive, and industrial controls.

After all, we live in an analog world. Nature-generated phenomena like temperature, pressure, speed, and sound produce analog indications. Now those indications can be cheaply converted for digital processing, and digital signals reconverted for useful work applications. And the race is on.



Consider, for example, just one area — telecommunications — in which the industry is moving toward voice transmission in digital form. ASP devices such as codecs and filters will be installed, one to a telephone line, to help make that changeover. Since there are presently some 200 million phones in the U.S. alone, and world-wide demand is expected to add about 60 million more each year by the mid-1980's, the potential magnitude of this single market segment is conservatively upwards of a quarter-billion units.

In the home, automotive, and general industrial markets, ASP growth should be equally spectacular for the next decade and more, with literally thousands of high-volume applications and replacements.

Happily, testing analog LSI devices need not become a stumbling block in any case. The techniques which are drawn together in this new apples-and-oranges world — complex ac testing, high-speed logic testing, discrete-device testing and laser trimming — have long been areas of expertise and leadership for Teradyne.

And with the development of the A300 family of analog LSI test systems, Teradyne has combined the broader test capability, higher accuracy, greater throughput, and added software-evaluation tools that the new devices require.

Teradyne's A300 Analog LSI Test and Trim Systems are the only high-volume systems specifically designed for the apples-and-oranges technology. As such, they provide a vital link to high-volume production and usage of present and planned analog LSI devices.

Once again, Teradyne has developed an important set of tools to help further the device technology critical to your future.

So let the revolution begin.

For more information on the A300 Series, write Teradyne, 183 Essex Street, Boston, MA 02111.

TERADYNE

Unit multiplies two 64-bit numbers in 284 nanoseconds

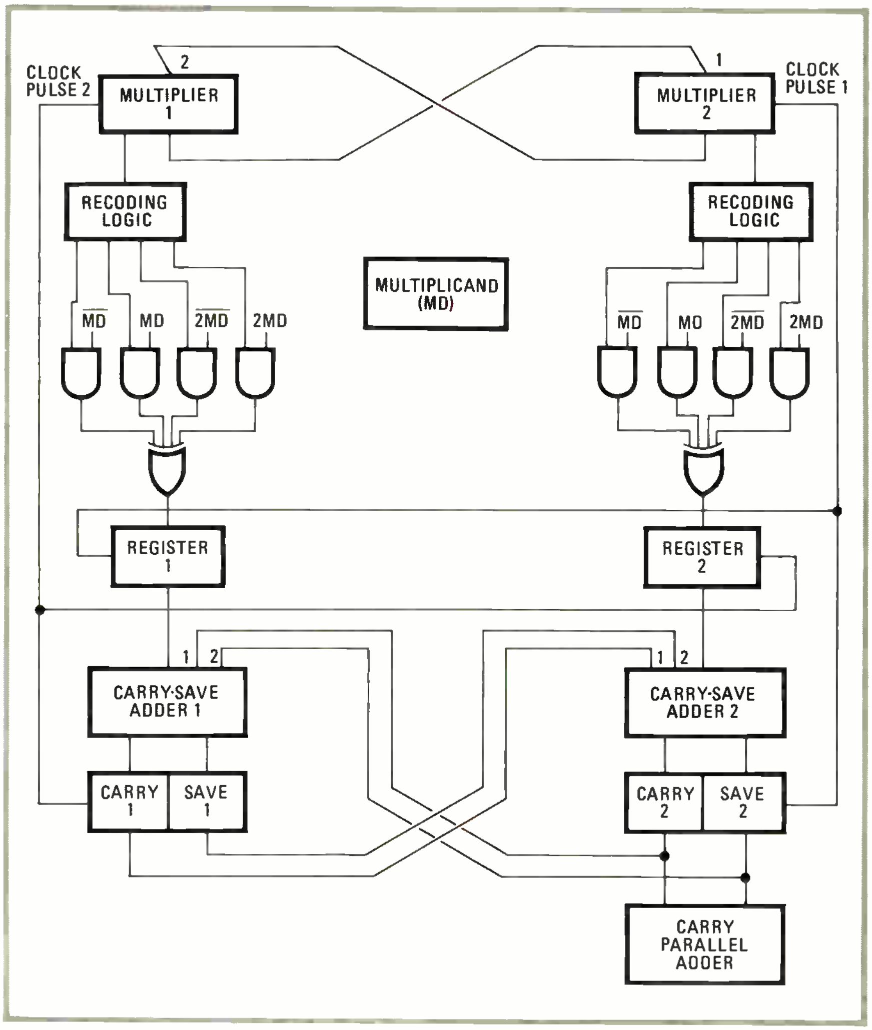
by Kevin Smith, London bureau manager

'Twin-beat' technique, use of carry-save adders, and multiplier recoding all contribute to high speed

Most present-day small minicomputers use microcode to tackle multiplication tasks because faster, hard-wired multipliers are too expensive. But at least one computer design group has now demonstrated that fast multipliers can be produced economically on a single printed-circuit board by the use of large-scale integrated bit-slice multipliers.

Manchester University's computer science department is developing a single-board multiplier for its projected MU6-G super-minicomputer that will give the product of two 64-bit numbers in 284 nanoseconds [*Electronics*, April 26, p. 63].

Says J. B. Gosling, who designed the unit, "The 64-bit MU6-G will have a conventional software multiplier, but for those uses like computer graphics and scientific number crunching that need a fast multiplication capability, the hardwired multiplier will be available as an option that plugs directly into the central processing unit." In fact, the multiplier could find many uses where the program speed is dependent on the multiplication time—computerized tomography, for one.



Speedy. Manchester University multiplier achieves noteworthy speed by performing two carry-save additions during one register-latching cycle, using carry-save adders, and recoding the multiplier so that the adders accept 2 bits at a time. Use of ULAs reduces the chip count.

Arrayed. Key to the unit's high performance and projected low cost is a 2-bit-slice multiplier chip engineered in an uncommitted logic array (ULA) from Plessey Ltd.'s Allen Clark Research Centre in Caswell, Northants. Made with a speedy emitter-coupled-logic process, it has gate delays of 1.5 ns.

Use of the ULA chip, Gosling says, "offers at least a tenfold reduction in component count compared with multipliers constructed from standard Schottky TTL and ECL while providing a hundredfold improvement in speed compared with software multipliers." It was also chosen to avoid the high design costs of a fully custom design.

The Plessey array consists of 100 logic cells, each equivalent to a two-input AND or NAND gate. These can be customized by a double-layer metalization. The problem, says Gosling, "was to hit on a design that offered high performance yet could fit in a low-cost 24-pin package."

The group opted for the "twin-beat" multiplier design—so called because it packs two carry-save additions into one register-latching cycle—that was used in their earlier MU-5 computer and in a modified form in the IBM 360/91 but has otherwise gone unnoticed by the computer industry. Yet, Gosling claims, "the twin-beat multiplier is the most cost-effective technique available and is one of the fastest in both theory and practice."

The twin-beat technique exploits the fact that a carry-save multiplication can propagate through a carry-save adder in 5 nanoseconds, whereas it takes 10 ns to latch the result into a storage register for each stage. By passing the output from one adder to the second during the 10-ns latching cycle, the number of operations per cycle is doubled.

Speedup. In addition to the twin-beat technique, two other features give the multiplier its high speed. First, the use of carry-save adders cuts out the propagation delays associated with the earlier carry parallel adders.

Second, multiplier recoding increases speed by grouping the multiplier into units of 2, 3, or more bits for the adder, but at the expense of additional logic. In this case, recoding is into 2-bit units, halving the number of cycles.

The twin-beat technique also lends itself to large-scale integration. Gosling was able to use most of the ULA, employing 98 of the 100 available cells and 21 of the 24 available pins. The resulting chip has a 1.3-ns internal gate speed and a clock period of 12 ns, or 6 ns per multiplication.

Using nine of these ULAs and 32 additional 10K logic family circuits to implement the final-stage carry parallel adder and the setup logic, he has assembled a 16-bit unit that multiplies in 115 ns. The total delay comprises nine 8-ns delays in the carry-save adders plus a 25-ns delay in the carry-parallel adder and a 18-ns delay in the setup logic. Use of 100K logic chips in the peripheral circuitry, Gosling adds, would cut the multiplication time to 88 ns.

The more, the better. At the 16-bit level the technique, though fast, is not the fastest around. But as bits are added, it becomes increasingly attractive, and for a full 64-bit multiplier using 33 ULAs, the 284-ns multiplication time is truly impressive. Process improvements from Plessey would further enhance the figures. In particular, a small array of subnanosecond gates will soon be available that could reduce the peripheral logic by 15 packages.

Further out, a 144-cell array is under development that would cut the multiplier's "beat," or 2-bit multiplication, time to 3 or 4 ns, giving a total multiplication time of 148 ns. This figure could be cut to 94 ns for a split multiplier, in which the multiplicand is split and both halves are multiplied simultaneously.

Use of the Macrocell array developed by Motorola Inc. [*Electronics*, Feb. 15, p. 113] would make a bigger, 64-pin package available and allow more bits to be packed on chip, Gosling notes. Either way, he claims, hardwired multipliers are now economical for the smallest minicomputers and even microcomputers.

West Germany

Computerized X-ray process shows blood rate as color TV picture

Though West Germany's DESY electron-synchrotron center in Hamburg generally investigates high-energy physics and other areas of research remote from everyday needs, occasionally it does come up with a highly practical idea. The latest one aids medical diagnosis.

Together with researchers at Hamburg University's Institute for Mathematics and Medical Data Processing, engineers at DESY—the acronym for Deutsches Elektronen-Synchrotron—have developed a computer-based X-ray technique that shows a doctor in full color how well blood circulates in organs.

In conventional diagnostic radiolo-

Colorful. Computerized angiography technique from DESY aids diagnosis of organ disorders by combining 128 X-ray pictures into one TV picture whose colors are a function of the rate of blood flow. Color scale at top (barely visible) eases interpretation.

gy, even as improved by computerized tomography [*Electronics*, Oct. 14, 1976, p. 89], the diagnosis is based solely on the size, form, and structure of organs shown in one or more X-ray projections. But an organ's behavior as a function of time, which can give an earlier indication of an impending or already existing disorder, can only be inferred from a laborious analysis of a series of X-ray pictures. In essence, DESY's technique does this analysis automatically, encoding the result in color.

Called computerized angiography, DESY's approach starts out like conventional angiography: a contrast medium is injected into an organ by way of a catheter inserted into an artery. The medium's density, as shown in the X-ray picture, indicates the rate of blood flow through the vessels. Any blockage or too slow a propagation rate reveals that something is wrong in the organ.

Outcome. The examiner analyzes only one image of the organ. Shown on a color-TV monitor (see photo), the image has above it a scale with color tones ranging from red at one extreme to yellow at the other and corresponding to blood-propagation delays of up to about 3 seconds. Equal colors represent equal rates of propagation. By comparing image with scale, the examiner can tell virtually at a glance where the blood is being slowed down. The rate can be determined to within ±200 milliseconds, says Gregory C. Nicolae, the Roumanian-born DESY engineer responsible for the technique's hardware development.

A DESY-built microprogrammed multiprocessor system implements the technique with any existing combination of medical X-ray machine and TV picture amplifier. It exposes the patient to X rays for about 2½ seconds—the normal period used in human radiology—taking a series of 128-by-128-millimeter pictures at about 50 per second for a total of 128.

The system digitizes all pictures in real time. Each full picture or a selectable rectangular area within the picture is handled as a matrix with a maximum of 65,536 picture elements, or pixels. The horizontal resolution can be set to either 256 or 512 pixels per line. Each pixel is 0.5 mm^2 and is represented by 8 bits. This means that each can be assigned one of 256 different intensity, or gray, levels.

Next, the system compares the gray level of a pixel in one picture with that of the corresponding pixel in the successive pictures in the 128-image series. The results are combined into 65,536 intensity-vs-time curves, each having 128 values. The wanted parameter—in this case, the delay in the spread of the contrast medium—is then extracted and assembled into a new picture, called the function image, which contains all the information on blood flow of interest to the examiner.

Finally, using a raster-scan display processor, the system converts the function image into color signals in a process similar to that used in color television. (Color pictures are of course easier to analyze than gray ones.) These signals are then fed to the TV monitor.

It takes about 2 minutes to process the 128 X-ray pictures into a single color TV picture, Nicolae says. Alternatively, the pixels' values can be stored and processed later to produce picture information on video tape, for example.

The components for the multiprocessor system come from various U.S. suppliers. Among the most notable parts are bit-slice processors of Advanced Micro Devices' Am2900 family and Z80 microprocessors from Zilog. **-John Gosch**

France

Hypercube 'federates' eight microcomputers

To launch a new component in France, the obvious choice is the annual Salon des Composants in Paris. But it was the wrong show at which to arouse interest in a new concept in array computers, laments Roger Dupuy, a professor of computer technology at Pierre and Marie Curie University, part of the University of Paris.

Dupuy put a prototype board for the Hypercube F8 array computer on display at the early April show at the Fairchild Camera and Instrument Corp. stand, hoping to find a firm that will follow through and market the machine, which was developed by his group at the university's Institut de Programmation with research funds from the government. He turned up no prospects, but he plans to try again in Paris at next week's Micro-Expo '79 show.

Dupuy, a software specialist who turned his hand to hardware as well with the advent of microprocessors and low-cost semiconductor memories, maintains that a Hypercube F8 with 512 kilobytes of main memory could be built to sell for about $23,000. He says that it is roughly the equivalent of a low-end IBM System/370, with full-fledged computer features like master-slave operation, parity checks, memory mapping, memory protection, and forbidden instructions.

What's more, two high-level languages are available: Basic and Minibol. "The Hypercube would be ideal for computer service houses that handle bookkeeping and inventory for their clients," he says.

Eight. Dupuy describes the Hypercube F8 as "a federation of microcomputers." There are eight of them, each on a single board with its own F8 microprocessor, 64 kilobytes of random-access memory, and 1 kilobyte of programmable read-only memory to initialize operation. Communications among the eight microcomputers, each of which also has its own operating system, are handled by a fast bipolar processor—a Signetics Corp. 8X300.

Also crucial to the system is a Control Data Corp. 100-megabyte disk drive, split up so that each microprocessor has its own specified zone to work with. Each microcomputer thus has a sizable on-board RAM backed up by its "own" disk memory. This arrangement is an important departure, Dupuy maintains, from earlier array computers,

which tied processors to a single giant memory.

In the Hypercube setup, some of the microcomputers do the actual data processing and the rest take care of running the peripherals. One is assigned to controlling the disk file and is heavily buffered to prevent long lineups for access to the disk. When a data stream enters the system from a microcomputer that controls an input/output peripheral, it is fed to a free microcomputer for processing.

The microcomputers signal when they are free by putting a request for inputs into a section of their RAM that is scanned continuously by the 8X300. This is done without stealing cycles from the microprocessors, which would slow them down.

Time enough. Each F8 has access to the on-board RAM during the first half of its 2-microsecond machine cycle. The fast-stepping 8X300, with its 250-nanosecond cycle, therefore has time to read or write a byte into the memory during the second half of the F8's machine cycle.

The control bus that ties the microcomputers to the 8X300 is a standard Signetics bus with eight lines for data and two lines for control signals. Data transfers between microcomputers are made over a separate data bus at a rate of 2 megabits per second. Each memory block is thus ported to its companion F8, the Signetics bus, and the data bus.

With this arrangement come substantial advantages over classic multiprogrammed computers. For one thing, the hardware is relatively straightforward, since it is built around standard chips. For another, because the one-board modules are all the same, maintenance is simplified—mostly a matter of changing boards. **-Arthur Erikson**

Great Britain

One-board color TV chassis fits four different-sized receivers

As a wall against the mounting wave of competition from Japan and the Far East, which could rise to tidal proportions when the first PAL patents expire in 1981, Thorn Consumer Electronics Ltd. has come out with a single-board chassis that it is billing as the ultimate in color television standardization.

In readiness for the coming free-for-all, R. V. Arnaboldi, the firm's engineering director, and his design team have long been laying plans for a highly integrated one-board color TV chassis that makes maximum use of automated component-insertion techniques. The result is the TX9, a single 156-square-inch board carrying all the set's electronics—just 410 components, versus 618 previously—that will replace four earlier models and will drive Thorn's new range of 14-, 16-, 18-, and 20-inch TV receivers without the need for any component or electrical change.

"The concept of a single-board chassis common to sets of several different screen sizes is," the London-based subsidiary of Thorn Electrical Industries Ltd. says, "an innovation in color TV technology."

Automation. One big advantage is that it gives Thorn the critical volume to justify automated assembly techniques. At its Gosport factory, the company has installed a $20 million automated assembly line that inserts 70% of all components, but such is its output that Thorn has had to close one of its three UK plants, laying off over 2,000 workers.

Several factors contribute to the shrinkage in chassis size down to one board. The intermediate-frequency filter section is made smaller by the use in all models of surface-acoustic-wave filters. To develop them, Thorn worked closely with Plessey Ltd.'s Allen Clark Research Centre. It also worked later with Mullard Ltd., to guarantee two sources.

The use of i-f filters, says chief engineer Alan Yarker, gives more permanent i-f alignment than mechanical i-f stages using coils and capacitors. It also cuts production setup operations by one third. Further, different European frequency standards can readily be met by plugging in suitable SAW filters.

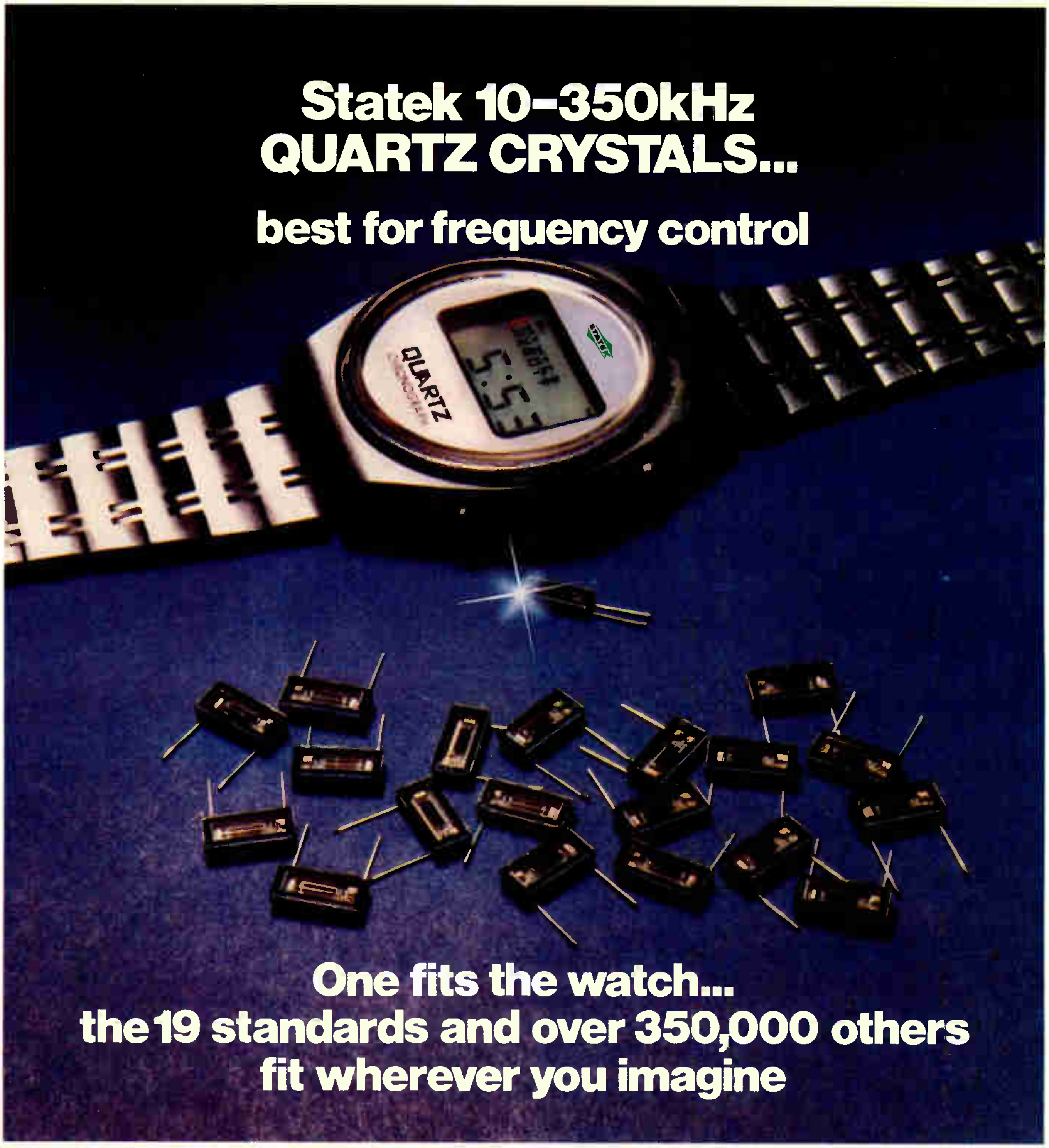
Help. Though Arnaboldi claims the new line of TV receivers is more than competitive with Japanese products, it nonetheless relies heavily on Japanese technology. The tube is a bipotential high-brightness design made by Hitachi Ltd. and based on its 90°-neck in-line tubes. Mullard is gearing for 90° in-line tube production and hopes eventually to make the new tube.

Also, one of the seven color-processing integrated circuits was developed in collaboration with Nippon Electric Co. This bipolar circuit, the luma-chroma-video processor, replaces three ICs in a conventional television and is used by NEC in its NTSC sets. It developed a PAL version for Thorn, which Philips will produce with the fast blanking time needed for teletext and viewdata.

Extensive use of ICs has eliminated more than 400 solder joints, with big increases in reliability, says Yarker. It has also simplified the design of the low-voltage power supply, which has to deliver an extremely low 40 watts to the chassis. A large output choke in the thyristor-controlled supply damps current spikes, and a regulator IC allows for fluctuations between 185 and 285 volts.

Also novel is the use of a diode-split transformer secondary to provide a compact high-voltage supply delivering 1 milliampere at 24 kilovolts, sufficient to drive even the largest tube in the range.

But consumers looking for instant price reductions when the new sets are ready in September will be disappointed. In common with other British manufacturers, Thorn—the largest indigenous manufacturer—has been facing diminishing margins for some time. It is therefore pinning its hopes on increasing profits and a short breathing space before the real competition begins. **-Kevin Smith**



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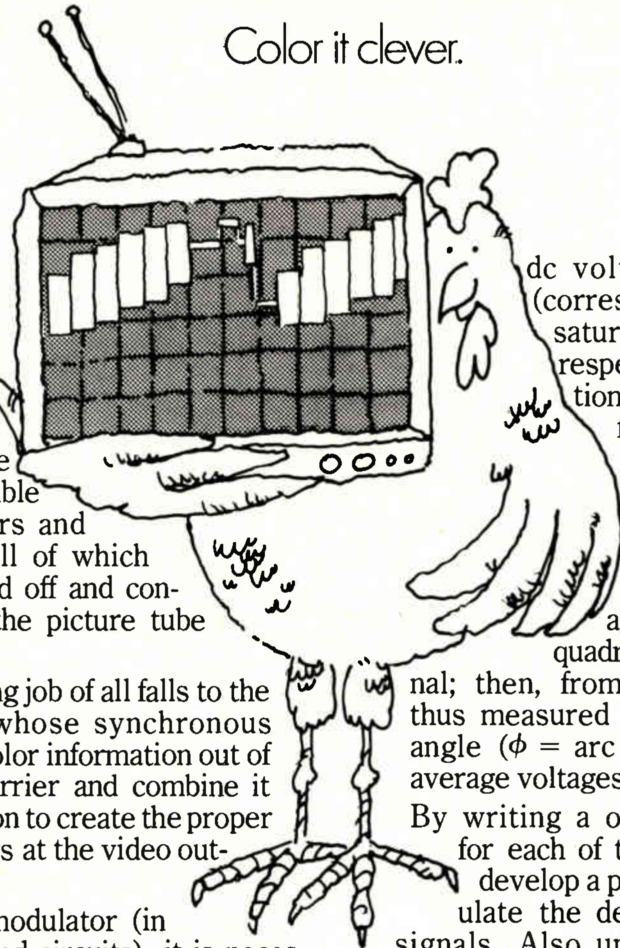


Converting a color television signal into a screen full of "The Muppets" is only slightly less complicated than unscrambling an egg. The rf signal appearing at the receiver front end is a jumble of modulated subcarriers and synchronizing signals, all of which must be delicately picked off and converted into information the picture tube can handle.

The toughest unscrambling job of all falls to the chroma demodulator, whose synchronous detectors must pull the color information out of a phase-modulated subcarrier and combine it with brightness information to create the proper mixtures of primary colors at the video output stage.

To test the chroma demodulator (in today's TV sets, integrated circuits), it is necessary to apply a modulated test signal at the appropriate subcarrier frequency and then accurately measure a number of phase-sensitive output voltages at the device output.

In practice, most of today's chroma demodulators are tested on Teradyne J273 Linear IC Test Systems equipped with a "chroma generator" specially designed to develop the convoluted waveforms that are required. The output of the chroma generator's output consists of 16 segments, each of which is programmable in time, dc level, and subcarrier level. In addition, three separate "event" outputs can be programmed to provide keying pulses wherever they are needed. Finally, a gated voltmeter can be programmed to measure, in any given segment, dc voltage, ac voltage, or phase (corresponding to brightness, color saturation, and color information, respectively). Since color information is actually transmitted in the form of phase angles, phase measurement is especially critical in chroma testing.

The chroma voltmeter is more than equal to the task. First it measures the average values of the in-phase and quadrature components of the signal; then, from the ratio of the two values thus measured the voltmeter derives phase angle (ϕ = arc tan of the ratio of the two average voltages).

By writing a one-line software instruction for each of the 16 segments, the user can develop a periodic waveform that will simulate the desired range of chroma input signals. Also under software control are a number of other variables, including voltmeter operating modes, subcarrier frequency and amplitude, and scale factor and attenuation of the video waveform. Test procedures differ for the American and European systems (NTSC and PAL), and this choice is also made in software.

Thanks to the J273 and its chroma generator, today's chroma demodulator can be rigorously tested on the production line in well under a second. The story doesn't end there, of course, for device designers are now busy adding more circuits to the same chip, while Teradyne's linear-test engineers are just as busy developing new automatic test techniques.

After all, once you have unscrambled an egg, why not build a hen?

TERADYNE

CII-HB aims at IBM's spot in France

Spearhead is R&D group that spends $100 million a year, with new advanced research unit roaming computer frontiers

by Arthur Erikson, Managing Editor, International

In the computer business, *chutzpah* can be defined as trying to match market shares with IBM. And CII–Honeywell Bull's president and director general, Jean-Pierre Brulé has it. Now that he has managed to turn the "French-computer" company into a money-maker, he is aiming to oust IBM by the end of 1980 as the market leader for deliveries in France.

If CII-HB does not manage that formidable feat, it won't be because the company scrimped on spending for research and development. Its budget for R&D currently runs more than $100 million a year, enough to support some 2,500 employees. That puts it at the top of the list in the computer sector for France. Worldwide, of course, IBM is far and away the biggest R&D spender, with outlays of more than $1.1 billion in 1977, according to Business Week, an American magazine.

But CII-HB can stake a fairly legitimate claim to second place. It swaps research results with Honeywell Information Systems Inc., which owns 47% of CII-HB, and the combined R&D spending for the two tops $200 million.

Even at that level, CII-HB cannot afford to do the wide-ranging basic research that IBM does. Nonetheless, it can and does patrol the frontiers of computer technology selectively. The patrol leader is 40-year-old François Maison, the company's scientific director, who also heads a new 80-person advanced-research center started up this spring at Louveciennes, some 15 miles west of Paris. Most of CII-HB's 2,500 R&D people spend their working days developing new hardware. The new group, in contrast, will have no specific product goals. "It will work only on new technologies," Maison explains.

Major thrusts. But it will not work on all technologies, obviously. There will be a considerable effort in integrated circuits and magnetics, where CII-HB already has considerable expertise. The other major thrusts in hardware will be fiber optics and printers. To no one's surprise, there will be a lot of work going on, too, in advanced programming languages and in new architectures for computers, mainly multiprocessors.

Still another mandate for the new center is to set up an effective dialogue with the 1,000-odd scientists and engineers working on computer-related technologies in government and university laboratories. That way, CII-HB can get basic research done that it cannot do itself. Also, of course, the Louveciennes crew will coordinate all the advanced research throughout the firm. "The hardest job in research management is to stop a project when you realize it is going bad," Maison maintains.

Like every other computer maker, CII-HB has to stay on the leading edge of semiconductor technology. So Maison has his people out there, too, although he studiously eschews the character-string "VLSI" that most people in the business use when talking about new generations of integrated circuits. "I don't see any real dividing line between large-scale integration and very large-scale integration," is the way the R&D chief explains it.

Chief researcher. François Maison heads CII-Honeywell Bull's 2,500-person R&D establishment that is budgeted at $100 million.

Whatever you call it, CII-HB is continuously updating its facilities for computer-aided design (CAD) of integrated circuits with up to tens of thousands of transistors on a chip. When it does a design, CII-HB carries the job all the way through to a set of tapes for making masks. Although it tracks all the major processing technologies, most often its designs are for n-channel silicon-gate MOS circuits or for bipolar current-mode logic (CML). The n-MOS ICs are usually microprocessors or custom designs for peripherals; the mainframes for the company's next generation of computers will be based on CML, actually a variant of emitter-coupled logic but having a voltage level of only 400 millivolts instead of the 800-mV levels typical of ECL circuits.

With its CAD, CII-HB has three

basic attacks on integrated-circuit designs. One uses a library of building blocks like gates and flip-flops to build up circuits, which "is fast, but wastes chip real-estate," observes Maison. A second method is to use an uncommitted logic array, which is the technique the company is using for CML.

The third way to accomplish it is to design the circuit from scratch using random logic. This, Maison feels, is suitable only for mass-produced circuits like random-access memories. CII-HB uses industry standards for its RAMs, but is good enough at designing them to have to its credit a 16-K memory chip done for a semiconductor house (Maison will not name it) that was having trouble doing the job itself.

Not too much. Maison's crew, though, is not driving willy-nilly toward the biggest possible chips with the largest number of gates packed onto them. When everything is factored in—chip size, wafer size, component density, packaging, and the like—a plot of cost versus the number of gates takes on a U shape, according to his calculations. Carrying the integration on a single chip too far, then, does not make sense.

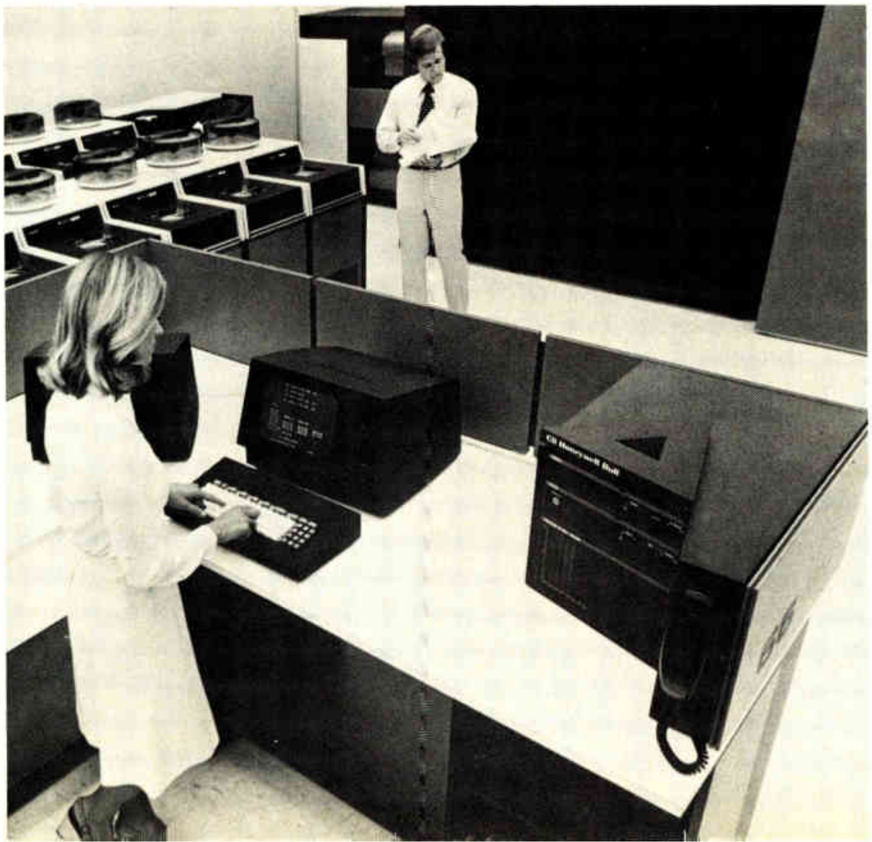
"It is a pin problem," he explains. "For a really large chip, you need more than 140 pins to connect with the outside world and 80 is the limit now." Thus, Maison does not see any one-chip substitutes for the boards now used in big computers—Amdahl Corp.'s 470V6, for example, has some with 3,000 gates and 700 pins. As a rough rule of thumb, he hazards a limit of 1,000 gates per chip for MOS circuits for large computers, with more possible for minicomputers.

Moving toward natural language

Research and development is not all hardware at CII-Honeywell Bull, of course: there is the push to higher-level programming languages. "We are trying to move the boundary between the outside world and the computer as close to natural language as possible," says Etienne Morel, who is spearheading the effort as part of the company's accelerated R&D drive. At the same time, Morel says, there is a drive to make programs more efficient and more reliable. An optimizer that cleans up loosely written programs has already been developed. Also, Morel's group now is working on a verifier that will analyze programs and spot logical shortcomings.

CII-HB software-development teams have already scored with a high-level language it calls LIS (an acronym for the French phrase for systems implementation language). LIS will be the basis for a system language that will be implemented for the nine-nation European Community and it is essentially the "green" language that was one of the two left in the running for the U. S. Department of Defense's universal language for programming real-time systems.

Onward and upward. CII-Honeywell Bull's R&D effort is paying particular attention to new frontiers in integrated circuits and magnetics, as well as in fiber optics and printers.



As for data storage, Maison sees no real competition between semiconductor memories and disk memories. Semiconductor memories get faster and cheaper, but disk memories get denser—and thus cheaper—following much the same curve. So CII-HB is pushing magnetics, particularly the integrated thin-film recording heads it has developed. Only 10 micrometers thick, they are about one tenth the size of a classic ferrite head. They can also be mass-produced: using lithography techniques similar to those for semiconductor fabrication, CII-HB produces 912 at a time on the substrate. Presumably, there is even better to follow: work has already started on a magneto-resistive-film read-only head that has a signal output some 10 to 15 times higher than the integrated heads and is independent of the disk speed.

A fiber future. Still other hardware needed for future generations of computers, Maison is convinced, are fiber-optic links. Here, CII-HB sees a need for bandwidths of at least 200 megahertz to interconnect computer cabinets with 100 or more simultaneous links multiplexed onto the fiber. The electronics for the multiplexer and for the driver, which will have to adapt automatically to the gain of a laser source, look so difficult that Maison expects not to see optical links between computer cabinets for some time. Before them, there will be slower links to connect low-speed peripherals to central processors. □

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Software

TI tackles programming on broad front

Its Advanced Software Technology department operates as a corporate-wide group tackling all parts of the problem

by Wesley R. Iversen, Dallas bureau manager

It's a technology seesaw. As the cost of today's increasingly complex computer hardware continues to come down, the cost of the software for driving that hardware is pushing upward at an alarming rate.

Electronics executives everywhere express a growing concern over the so-called software problem. But perhaps nowhere in the corporate world is the problem being attacked as methodically as it is at Texas Instruments Inc.

"A lot of companies are doing things like what we're doing. But there aren't many, if any at all, that have tried to put it together into one organization as we have," observes Roger R. Bate, a 56-year-old Ph.D. who rides herd over what the Dallas company calls its Advanced Software Technology department (AST).

Formed in 1976, AST is responsible for the development of methodologies, tools, standards, and equipment aimed at holding costs down by improving software productivity and reliability. In particular, says Bate, the development of procedures to keep TI software projects running on schedule is of central importance.

Though formally a part of TI's Equipment Group, which handles most of the company's large Government and military contracts, AST is increasingly providing a broad range of software and software support services to other TI operations.

With some 100 software specialists on its payroll, AST is divided into 10 operating branches, each with specific functions. One branch provides support to various projects in the form of borrowed software specialists who serve as consultants, troubleshooters, and, in some cases, project software managers. Another group offers a curriculum of in-house software education courses and has trained more than 1,500 TI employees over the last two years with offerings ranging from Pascal programming to the DX-10 operating system used on the company's family of 990 minicomputers. Still another branch develops specific language processors such as Pascal and Jovial compilers, while others concentrate on leading-edge research in computer software, architectures, and systems.

Weighing productivity. In terms of concrete measurement of AST's value to Texas Instruments, Bate says the numbers collected to date are inconclusive because of the well-known vagaries of gauging software productivity. But Bate says he is certain of one thing: the software projects that

Saying it softly. Programmers at work in TI's Advanced Software Technology department serve the entire corporation. The 100 software specialists on the department's payroll are split into 10 branches that handle such functions as troubleshooting and in-house education.

Probing the news

adhere from the beginning to AST's recommended disciplines, techniques, and methodologies tend to run on schedule. Those that do not tend to fall behind. "That's the one thing that's been more important than anything else we've done," Bates declares.

Tom Miller agrees. As strategy manager for TI's TMS9900 microprocessor family in Houston, Miller notes that AST has "participated in both the definition and development of all of our Pascal-oriented products," including Timber (for TI Modular-Based Executive in ROM) introduced by the company last week (see p. 48). In all of those projects, Miller continues, the "review and formalization procedures" required by AST methodologies were valuable in "identifying problem areas very early," thus preventing schedule slips caused by false starts.

The fact that the 9900 group's software technicians have been trained in standard AST methods is also a significant help when project personnel leave or are transferred, Miller points out. "If you have discontinuities where someone works on a project for three months and then quits and another person comes in and has to reinvest those three months, plus three months of his own . . . that sort of thing is almost completely minimized by the AST organization and the influence it has in the company," Miller observes.

Indeed, AST influence is growing. Bate has been named chairman of a corporate-wide steering committee for a TI project approved last January known as the Integrated Software Support System (ISSS). As explained by Douglas S. Johnson, an AST employee who is heading a working group for the initial phase of the ISSS project, the goal is to improve programmer productivity all over TI by 25% using methodologies, software tools, and equipment defined and developed by AST. The 25% goal is not unreasonable, Johnson says, adding that the savings to TI could amount to as much as $379 million cumulatively by 1985.

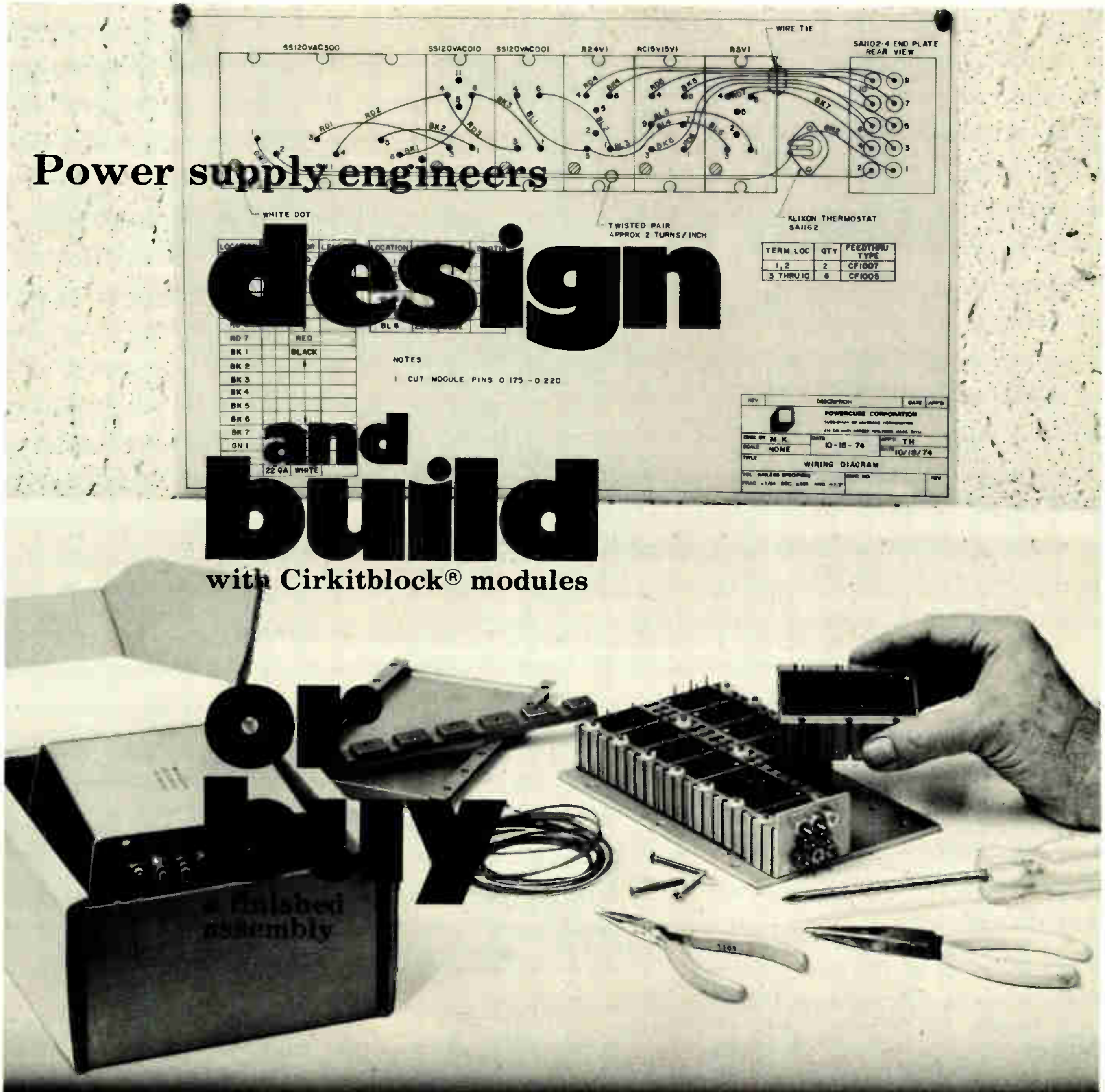
Among initial ISSS tasks to be completed this year is a definition of software productivity. "We're not convinced that source lines of code per man-month are really the best thing we've got, or that they're even believable," says Johnson of today's most widely used yardstick.

Universal methodology. Also scheduled for this year is the establishment of a single TI software methodology applicable across the entire corporation. Applications will extend from conventional corporate data-processing tasks, such as handling personnel and payroll, to such diverse software areas as semiconductor component design automation, automated manufacturing with robots, and development of the powerful software packages needed by TI's Equipment Group for large military contracts and by the geophysical services operation for seismic data processing. Software development for TI products ranging from 990 minicomputers to appliance-controlling microprocessors to industrial control and consumer products will also fall under ISSS.

"The idea is to build a methodology that can be tailored easily to any one of those applications, but still have many consistent features," Johnson explains. "We won't insist that everyone use a particular programming language, for example. But we will insist that there be some common characteristics to the design documentation produced."

More tools. Once the methodology is in place and the measure of productivity is defined, remaining steps in the project include AST development of new software tools, as well as hardware and equipment necessary to move TI incrementally toward the 25% productivity goal by 1985. Such equipment could include individual terminal-like work stations on every programmer's desk, for example, that would have all necessary capabilities for text editing and might even be portable enough for a loyal TI programmer to take it home for after-hours work.

In addition to the gain of internal efficiencies, there is, of course, another potential benefit of the ISSS project to be had by TI. Included as part of the program tasks are a series of analyses to determine cost and other requirements for eventual marketing of an ISSS system. □



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Investment

Venture capital booming again

More money is available than there are deals;
new firms with $250 million have doubled the market in past year

by Benjamin A. Mason, New York bureau manager

After several years of lying low, the U. S. venture capital community is on the prowl again. Responding to massive infusions of new capital, venture capital companies of all sizes and descriptions are hunting for entrepreneurs to finance.

Long a prime area for venturing (as the cognoscenti call it), the electronics industries can expect another round of funding. Indeed, from the standpoint of the electronics entrepreneur, it may be something of a seller's market. "There's a lot of money chasing a very few deals," said one participant in a venture capital seminar late last month at Electro79 in New York City.

"Over the past 12 months, some 15 to 20 new funds with over $250 million in capital have been formed," says seminar participant Yung Wong, the investment manager for Time Inc.'s venture investment program. "For those who have been bitten by the entrepreneurial bug, this is a good time to obtain venture capital."

Moreover, new companies are only half the story. Venture Capital, a monthly publication that watches the industry, estimates that in 1978 between $525 million and $560 million in new money became available from newly established and existing venture capital firms. "Also, there are probably another 20 groups looking for money [to invest], and that means another $250 million available," says Jane E. Koloski, assistant publisher of the Wellesley Hills, Mass., publication.

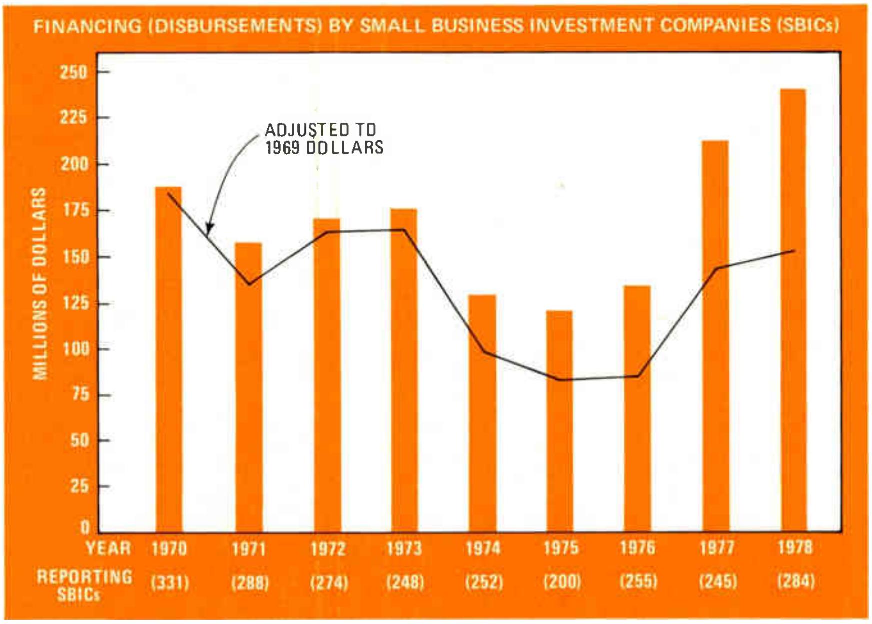
Equally telling is the jump in the amount of money actually invested. The figure tells the story of investment by what are known as small business investment companies (SBICs), a major factor in the venture capital industry. In terms of constant dollars, SBIC disbursements are still below their levels in the early years of the decade—but they are continuing to rise.

Early in the cycle. How long the rise will continue is open to question—for as the figure suggests, venture investments tend to be cyclical. However, the venture capitalists at the Electro seminar clearly believe the current boom is still young.

The seminar participants were from corporate venture capital efforts (that is, arms of existing businesses, usually large ones), and they cited a resurgence of interest among such companies as a key factor in the boom. Seminar organizer Kenneth W. Rind, a principal in Xerox Development Corp. of Los Angeles, noted that the venture capital cycle mimics the cycle of new stock issues for small companies.

While that cycle has shown an upturn, it is providing nowhere near the amount of capital it did before 1973. Less of the available money is going into the stock market, and more if it is going into venture investment companies. Add increasing U .S. corporate liquidity and the growing presence of foreign companies seeking investment opportunities, and the result is an increasing corporate presence in venturing.

Corporate investors often are in venturing as much for access to new technologies, markets, and potential acquisitions as for profits. Other types of venture capital firms are in the game strictly for the bottom line.



Making a comeback. The cyclical venture capital industry, like the economy, has made a strong comeback since it declined in 1974–75. Table shows activity of SBICs.

Individuals or small conclaves of partners that invest their own money fall in the latter group. The Arthur Rock Co. of San Francisco is an example well known in the electronics industries. Its president, Arthur Rock, reports, "I'm more busy now than I've ever been." Another type is the firm that pools investment funds from several sources, often from institutions like retirement funds. The influence of banks, insurance companies, and the like is burgeoning here, as well as in the corporate sector, reports Jane Koloski of Venture Capital.

Eye electronics. Whatever the type of investment company, there is no doubt about the interest in electronic ventures. Xerox's Rindt says that the track record of electronic venturing includes many sparkling successes, beginning with IBM Corp. One reason for the current interest, he says, is the passel of strong survivors of the late 1960s' explosion of electronic ventures—like Intel, Data General, and Mostek.

However, venture capitalists almost invariably want the profits to start flowing within a couple of years after they make their investment. They are seeking at least 20% pretax profits and 30% return on investment, said seminar participant Reuben Wasserman, vice president of advance planning for Gould Inc.'s Instrument and Controls group in Burlington, Mass.

One result of these goals is the venture capitalists' interest in companies that are past the initial stages of research and development. "There is very little money for startups that require a whole new technological or market development," says Donald T. Valentine, president of Capital Management Services Inc., Menlo Park, Calif. An example of a startup situation that does build on existing technology and a known market base is the one in 8-inch Winchester disk drives. "There's almost no one visible now, but in two years, there will be half a dozen new companies with these products," he says.

The condition of the industry sector is also important, Valentine points out. "For the last five years and for the next five, the businesses being financed are systems companies," he says. □

Solid state

Sales strength seen

TI says U. S. semiconductor sales will rise 16% to 26% in major markets with computers leading the way

by Wesley R. Iversen, Dallas bureau manager

Despite an expected slowing of the economy later this year, Texas Instruments Inc. is projecting continued strength in the U. S. semiconductor market during 1979, with growth rates in major equipment market segments ranging from 16% to 26%.

Sales to small- and medium-size computer customers will be down during the second half due to higher interest rates and the slowing economy, the company says. But according to figures prepared by TI's U. S. semiconductor marketing vice president, Ed O'Neill, the computer segment overall is expected to lead the way in 1979 with 26% growth over 1978 to $970 million. Including all segments, the overall U. S. semiconductor market is seen growing at a hefty 20% rate to $4 billion this year. This would outstrip the 17% rate, to $9.6 billion, projected for worldwide semiconductor sales by TI president J. Fred Bucy at the Dallas company's annual meeting last month [*Electronics*, April 26, 1979, p. 33].

As the biggest semiconductor manufacturer of them all, TI's crystal ball reading for the $4 billion U. S. market is less than the projected $4.043 billion market reported as the industry consensus at the beginning of the year [*Electronics*, Jan. 4, 1979, p. 112]. But O'Neill puts last year's U. S. semiconductor sales at $3.33 billion, whereas the industry consensus was a $3.581 billion figure. This accounts for his 20% growth prediction, which tops both the 12.9% growth prediction reached by industry consensus and the 15.3% growth predicted by the Semiconductor Industry Association.

Slow spots. TI projects the slowest U. S. semiconductor growth rates in the consumer and Government markets, where the company says sales will increase by 16% to $1.01 billion and $670 million, respectively. Contributing to the slower consumer growth will be a flat year for automobile production at 9.3 million units and an 8% drop in color TV sales from the 10.3 million units moved in 1978, TI expects. The government end of the business will be boosted by continuing strength in the tactical equipment category with

MAJOR U.S. SEMICONDUCTOR EQUIPMENT MARKETS
(IN MILLIONS OF DOLLARS)

	1978	1979	Increase
Consumer	870	1,010	16%
Computer	770	970	26%
Industrial	1,110	1,350	22%
Government	580	670	16%
Total U.S.	**3,330**	**4,000**	**20%**

Source: Texas Instruments Inc.

the use of JAN (joint Army-Navy) devices.

The industrial market—which TI says will be paced by as much as 24% growth in telecommunications with the continued conversion from electromechanical to electronic switching—is expected to weigh in with a 22% growth overall to $1.35 billion.

Continuing escalation in customer demand through the first four months of 1979 has extended lead times to 16 to 20 weeks for low-power Schottky logic and bipolar and MOS memory products. Despite this, TI officials note that double ordering has not become a major problem. O'Neill credits that in large part at TI to an allocation program begun by the company during the second half of last year that assures customers of product delivery. Though demand currently exceeds capacity, product pricing has not gone up, the TI marketing official says.

Ups and downs. In terms of semiconductor product types, TI sees sales of discrete devices rising by 11% this year, with drops in the silicon transistor market being partially offset by increasing sales of power and optoelectronics products. Integrated functions are projected to grow at 17%, paced by low-power Schottky as the preferred logic for new designs and by strong growth in linear circuits such as bipolar–field-effect-transistor operational amplifiers, plasma display drivers, and switching regulators, in which TI has been active.

With a 31% growth projected for sales of integrated systems, the trend toward higher complexity and lower costs in semiconductor memory will continue, TI says. Continued rapid growth in microcomputers is also seen. Applications for 4-bit devices such as the popular TMS1000—the Dallas company says it has now produced more than 12 million—will continue to proliferate in toys and games and in the home telephone market, among others. Automotive engine control will be one of the markets for 8-bit devices, while TI expects its 9900 family of 16-bit machines to continue finding important niches in instrumentation, industrial controls, and other uses. □

Electronics abroad

South Korea starts own Silicon Valley

Institute in industrial park has five-year charter to start domestic industry by providing technical backup

by William F. Arnold, San Francisco regional bureau manager

Eyeing the growing electronics marketplace, countries across the world are attempting to emulate the success of the U. S. and Japan. European schemes, for example, include direct investment by multinational companies, joint ventures between domestic and overseas corporations, acquistion of U. S. companies, government seed money to spur research and new markets, and even direct government formation of new companies dealing in high-technology.

South Korea has some rather different ideas on how to become the next big electronics manufacturing country—one that will produce both semiconductors and computing systems, government officials say. In so doing, the country is finally abandoning its role as an offshore assembly area, which rising labor costs, coupled with advancing industrialization and the attendant large consumer electronics market, is fast making untenable anyway.

To get into the act, the Korean government is taking two major thrusts to help its local companies, which are mostly oriented toward consumer electronics. Conventionally enough, it is encouraging the popular joint-venture route, such as the $10 million deal to set up a cooperative plant between American Microsystems Inc. of Santa Clara, Calif., and Gold Star, described as Korea's General Electric. Much less conventionally, the government has created a novel catalyst in the form of the Korean Institute of Electronics Technology (KIET).

Funds. Armed with a just-approved $29 million loan from the World Bank and another $30 million from the Korean government, KIET plans to offer companies the training, research and development, mask making, software development, testing, and whatever else it takes to help a modern electronics industry get off the ground.

The institute's technology service center will be part of a new 2,000-acre electronics park in Gumi, in the south, according to KIET president Sang Joon Hahn. He says the first 100,000-square-foot building, housing 4-inch-wafer-fabrication lines for both linear and MOS devices, is due to be finished in September. When the entire eight-building complex is completed in 1981, it will house production lines, test equipment, and development teams and include dormitories to house technicians undergoing training. KIET's staff also will have grown by then from 150 to about 500.

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supporting in five years. As Sang says, "Otherwise people could become stagnant. With continued government support, no one would want to work very hard." KIET has an independent board of directors because the South Korean government does not want to add to its state agencies. Observes Glen R. Madland, president of Integrated Circuit Engineering Corp., Phoenix, which has done consulting work in Asia, "The South Koreans are an interesting combination of Asian thinking and Western entrepreneurial practice." He notes that South Koreans make decisions quickly in contrast to the sometimes drawn-out group consensus process that is characteristic of the Japanese.

Sang is aware that KIET "will have to develop capabilities step by step, not just jump to something new for its own sake." This means that at first it will be tied to the heavily consumer-oriented linear bipolar technology. Korea "is not a great manufacturer of digital equipment yet," he says. But Sang indicates that, in 18 months or so, after KIET has established a basic capability, it will bring in equipment like electron-beam mask-making machines to prepare for more advanced circuits.

Gradually or not, KIET officials hint that Korea could be producing microprocessor chips and memories by 1981. They also express interest in microcomputer and minicomputer systems. Trends elsewhere in the world, notably in Japan, show that progressive electronics companies usually graduate from consumer to more sophisticated wares.

In training. The better to train local engineers, KIET has about 50 engineers scheduled to come to U. S. companies. Of these, 9 will be in semiconductor processing, 12 in IC design, 15 in software, and 7 in systems hardware, states Young D. Kwon, director of KIET's U. S. branch in Cupertino, Calif., in the heart of Silicon Valley. Moreover, the South Korean government has backed the Kyungbook National University near Gumi that will be producing 600 electrical engineers a year on top of the 100 or so from Seoul University, Kwon says. Also, Gold Star recently had 10 engineers being trained at American Microsystems Inc., Santa Clara, Calif.

Gold Star and Taihan are two broad-based conglomerates that are

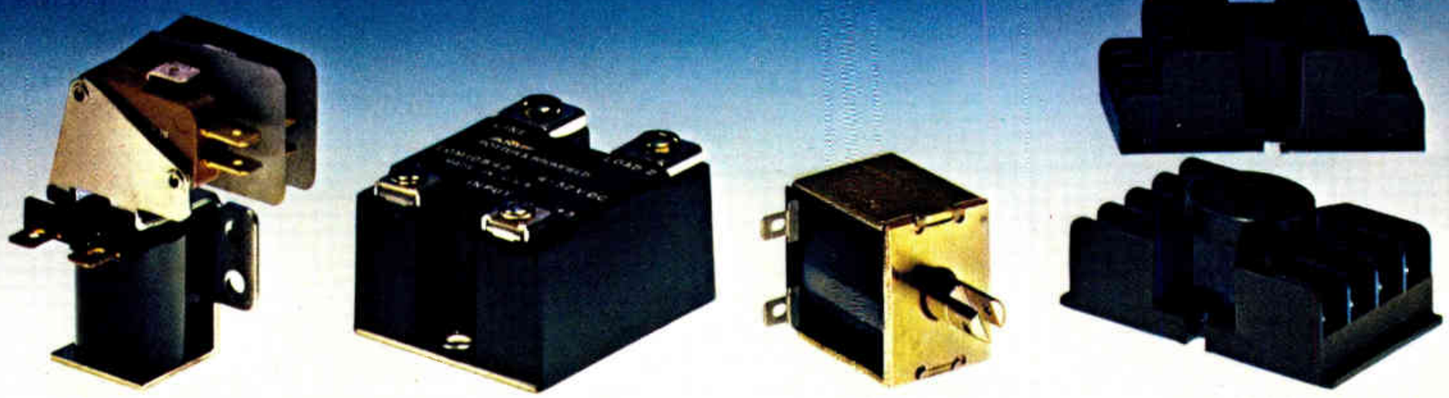
Capital city. Seoul, South Korea's capital, is a bustling metropolis whose population has soared to more than 7.5 million.

already building their first semiconductor plants at Gumi, Kwon reports. Once in operation, they will join Samsung, which up to now has been Korea's only source, Kwon says. Samsung's Seoul plant currently produces 1,000 complementary-MOS wafers a day. KIET expects "at least" five IC plants in Gumi in the next two years, Kwon continues.

On the computer side of Gumi park, a joint venture of Hyosung and Japan's Hitachi Ltd. has bought land for a plant, and Kwon says that Gold Star, Samsung, and Taihan are negotiating with U. S. companies to build computing systems under license. Kwon estimates that the South Korean government will invest three times as much on the computer as on the semiconductor side, although the exact figures have not yet been compiled.

Sensible? How sound is the South Korean approach? Kenneth Zerbe, who was AMI's senior vice president, secretary, and treasurer before he recently left to become Apple Computer Inc.'s vice president of finance and administration, says that AMI's first joint venture "made good economic sense—the market in Korea is large enough to support the investment." Also, he says, "there is export potential, although the venture initially will support the local consumer market first."

Zerbe says that AMI will have as many as six circuits under joint development with Gold Star. Although starting an advanced electronics industry is far from easy, ICE's Madland avers that the Gumi electronics park alone could eventually be as big as TI. □



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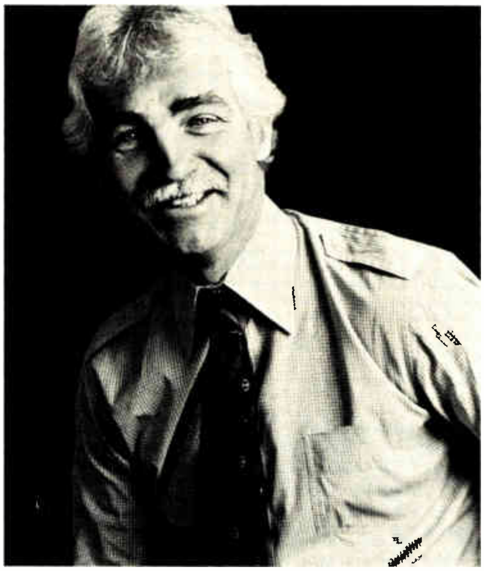

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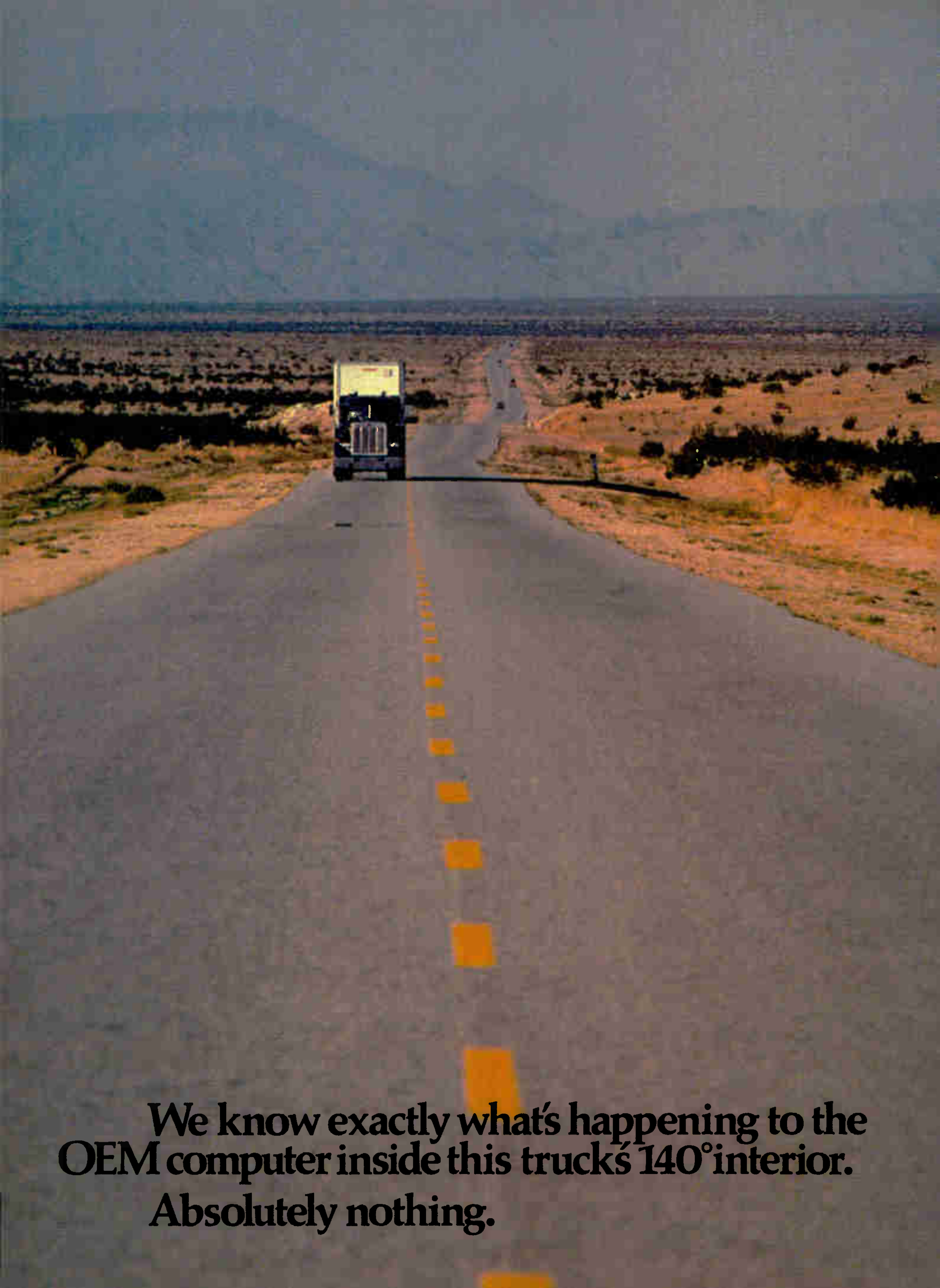
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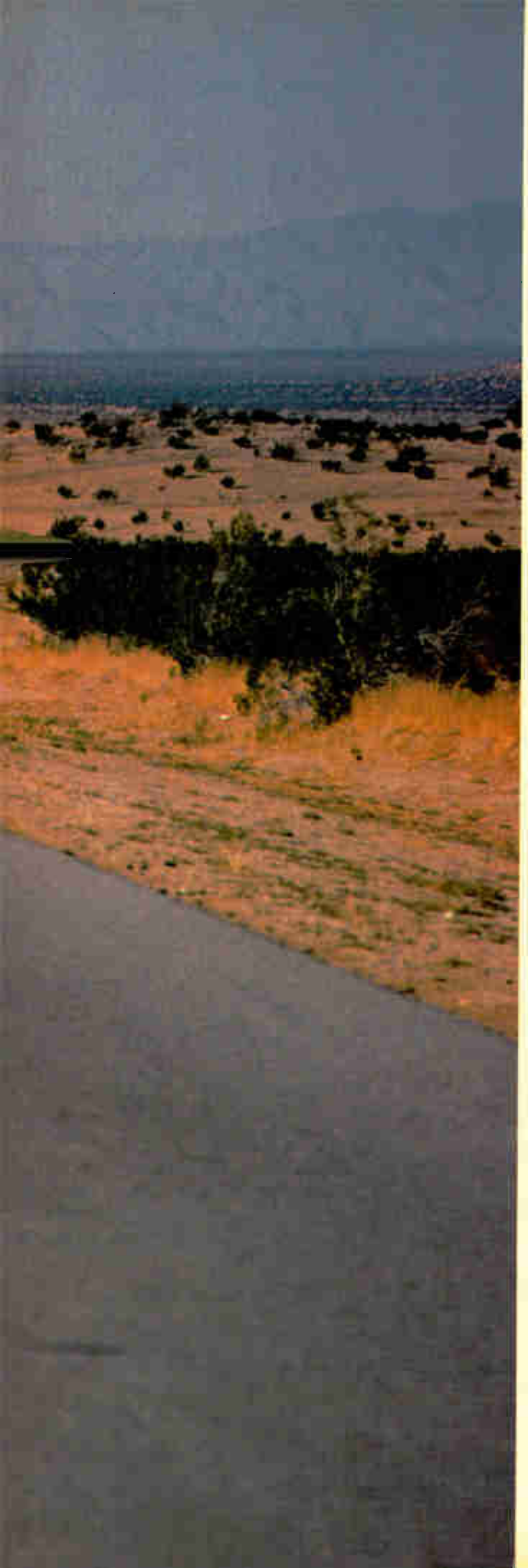

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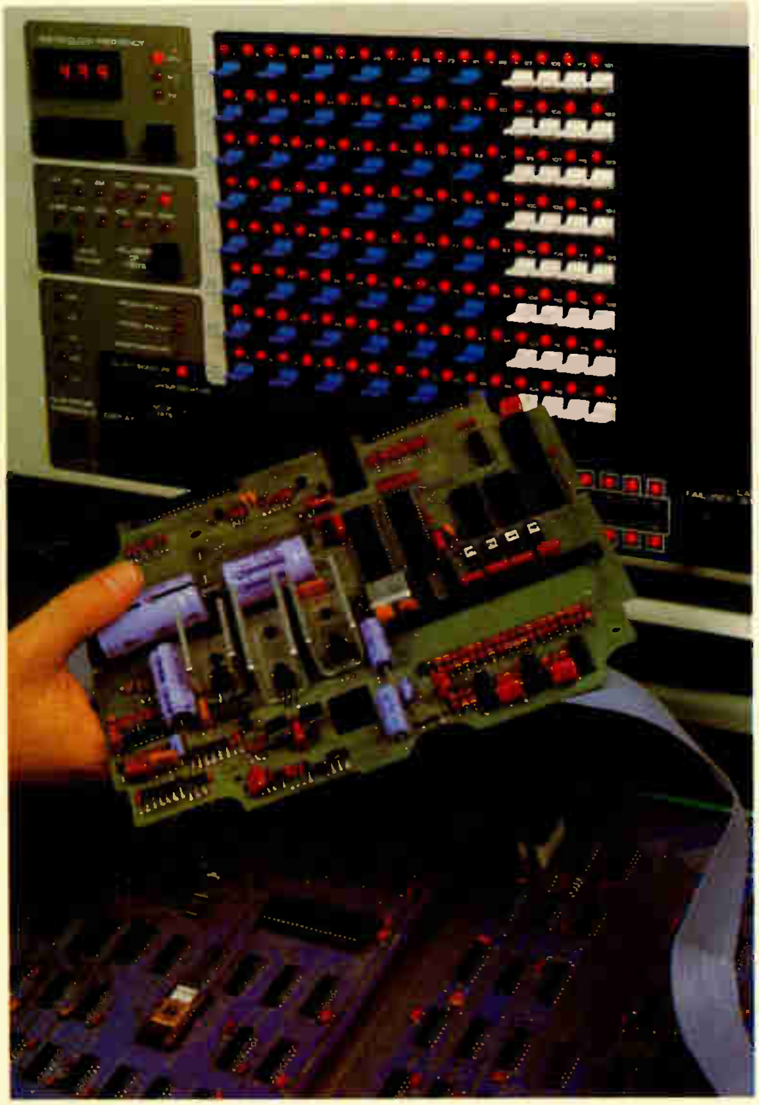

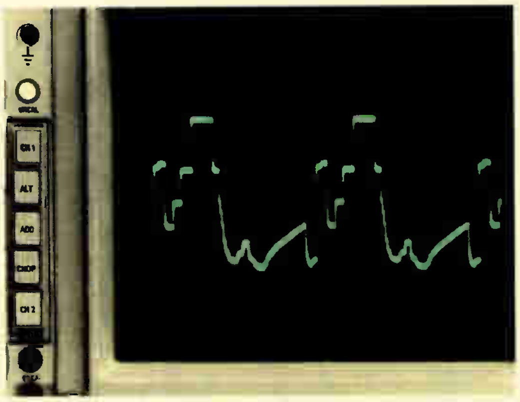

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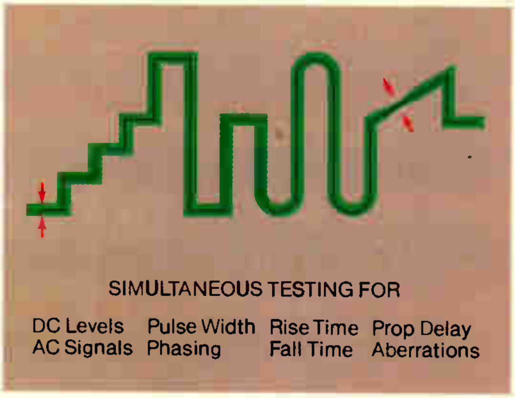

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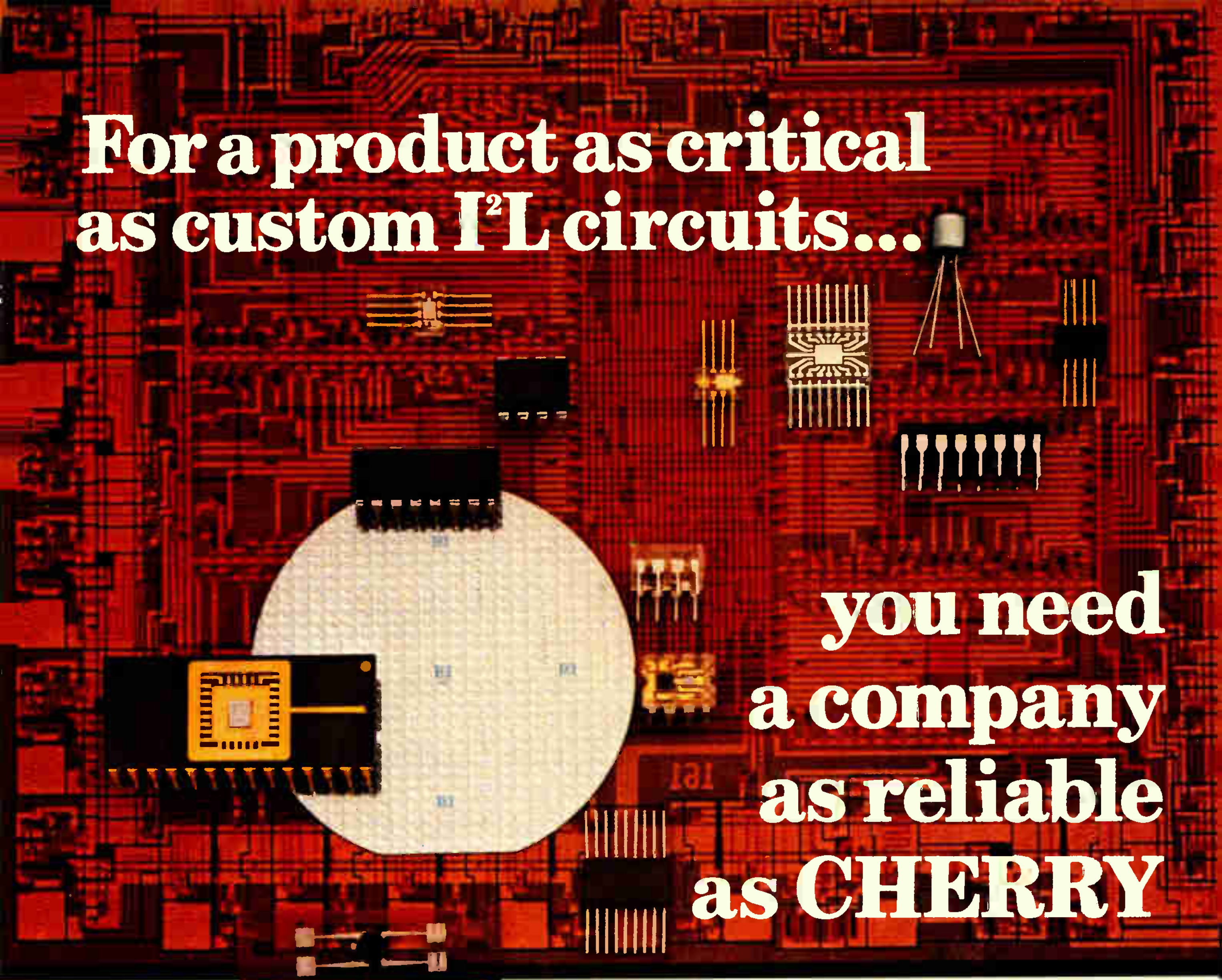

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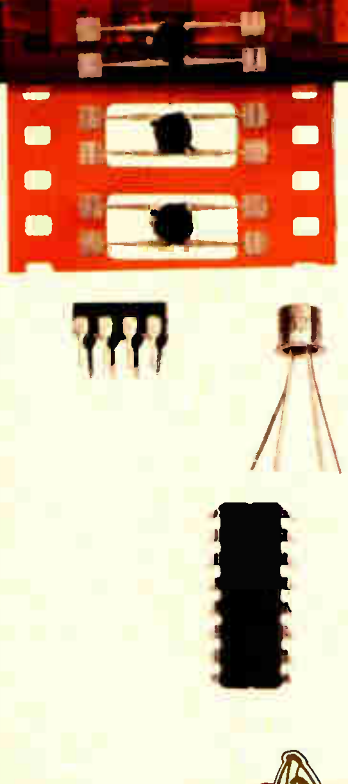

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Monolithic approach bears fruit in data conversion

Improved circuit design and processing are boosting chip resolution, though hybrids still yield best performance, says this special report

by Nicolas Mokhoff, *Components Editor*

□ Another monolithic incursion is at hand as the big digital semiconductor companies move in on a data-conversion market that since its inception has been nurtured by hybrid circuit and module makers.

Large solid-state houses like Texas Instruments, Motorola, and National Semiconductor are making serious efforts at incorporating most, if not yet all, the functions of the analog-to-digital or digital-to-analog converter on a single piece of silicon. Twelve-bit resolution seems almost within their grasp. Yet the only traditionally analog house to be attempting to do likewise is Analog Devices.

The technologies involved are not unfamiliar to hybrid stalwarts like Burr-Brown and linear chip specialists like Precision Monolithics. Standard bipolar, standard complementary-metal-oxide-semiconductor, and mixtures of the two kinds of process are mostly what are being tried. But since the big digital houses can pick and choose among the various semiconductor technologies and opt for the one that yields inherently less expensive and more reliable products, they are a definite threat to those whose resources are more limited.

In a nutshell:

- National Semiconductor Corp., Santa Clara, Calif., is attacking the 8- and 12-bit precision a-d market with innovative design techniques in C-MOS that will be truly stand-alone microprocessor-compatible parts.
- Motorola Semiconductor Products division in Austin, Texas, is making not only 8-bit a-d C-MOS converters compatible with its upcoming MC 146805 C-MOS microprocessors but are also supplying samples of very fast ("flash") converters—an 8-bit d-a, for instance, with a 25-megahertz speed due solely to its being a bipolar part.
- Texas Instruments Inc. of Dallas, Texas, the biggest semiconductor manufacturer in the world, is also waking up from a long digital hibernation and threatening to take a chunk out of the data-converter field; specifically, it is carving away at the 8- to 12-bit a-d market with both special-function and low-cost standard devices.
- Signetics Corp., Sunnyvale, Calif., is pushing ahead with its bipolar specialty, integrated injection logic, expanding from 8-bit to 10-bit and 12-bit microprocessor-compatible d-a converters.
- Advanced Micro Devices., Sunnyvale, Calif., is using untrimmed diffused resistors instead of thin-film networks to achieve 12-bit monotonicity in its Am 6012 d-a converter. Eliminating thin films from integrated converter circuits allows AMD to tag the part at under $10 in large quantities, a breakthrough for monolithic 12-bit d-a devices.
- Not to be upstaged, Analog Devices Inc., Norwood, Mass., the barometer of the converter industry from the module products of its earliest years to its present-day chips, is using all of its available technologies and circuit ingenuity to offer a potpourri of devices including microprocessor-compatible parts. It is soon to release an 8-bit successive-approximation C-MOS a-d converter, the AD

TABLE 1: HOW BIPOLAR AND MOS MONOLITHIC DATA CONVERTERS COMPARE		
Functions	Bipolar	MOS
Passive elements	diffused, implanted, or thin-film resistors	diffused, implanted, or thin-film resistors; MOS capacitors
Untrimmed accuracy	~ 0.2%	~ 0.1%
Long-term stability	~ 0.01%	~ 0.01%
Trimming	zener zap, Nichrome fuse, or laser wafer trim	polysilicon fuse, electrically programmable read-only memory, or laser wafer trim
Analog switching	current	current, voltage, or charge
Amplifiers and comparators		
Gain (internally compensated)	80 – 100 dB	60 – 80 dB
Dc offset (untrimmed)	~ 1 mV	~ 20 mV
Gain-bandwidth product	1 – 10 MHz	1 – 10 MHz
Rms noise, audio band	0.1 – 10 μV	10 – 100 μV
Dynamic range	120 – 140 dB	80 – 100 dB
Die area per amplifier	400 – 1,000 mil^2	150 – 500 mil^2
Voltage reference	band gap, zener diode	$V_{TE} - V_{TD}$, zener diode
Temperature coefficient (untrimmed)	50 – 100 ppm/°C	10 – 20 ppm/°C
Long-term stability	0.1%	0.1%
Implementation of other functions		
Sample-and-hold	complex	simple
D-a conversion	simple	simple
Monolithic filters	frequency-locked	switched capacitor, charge-coupled devices, or bucket-brigade device
Combined analog and digital circuits	I^2L + analog, EFL + analog	n-MOS, C-MOS
Strongest points	low-noise; high current and voltage compatibility; design experience; proven stability; −55° to +125°C	low-cost; filters available; microprocessor and memory compatibility; technology investment

7574, which is compatible with 6800 and 8080 microprocessors, and is also introducing bipolar converters, both a-d and d-a, in monolithic and hybrid forms.

■ The higher-performance market continues to be dominated by hybrid converters not only from Analog Devices but also from hybrid specialists like Beckman Instruments Inc., Fullerton, Calif., and Harris Semiconductor Products division, Melbourne, Fla. What makes these two companies unusual is the breadth of their resources, in terms both of pure technology and of the products bred from the cross fertilization of these corporations' interests.

■ Although committed to integrated circuits, RCA Corp.'s Solid State division, Somerville, N. J., enjoys the same advantages. Few commercial converter products are available from RCA at present, but the first of many C-MOS and bipolar ICs is expected to emerge towards the end of the year.

Meanwhile, makers of strictly monolithic converters are all busy exploring different combinations of process technologies and sophisticated analog and digital circuit designs, to discover which approaches best fit which converter requirements. For instance, at this year's International Solid State Circuits Conference [*Electronics*, Feb. 15, 1979, p. 129], two full sessions were devoted to data acquisition, with engineers from prominent semiconductor manufacturers describing how clever circuit techniques in a proper process can be made to enhance functions needed for conversion. Moreover, their papers were not reports of blue-sky laboratory adventures but of products that are already being tried out as samples by key customers.

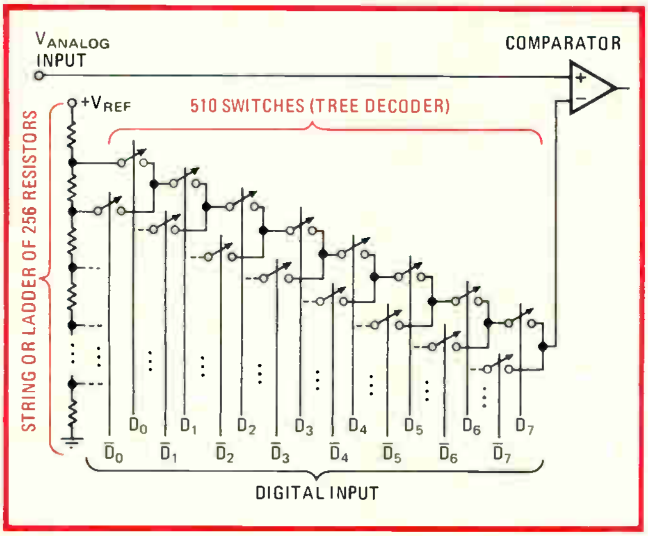
MOS versus bipolar

One strong advocate of using MOS technology for precision analog functions is David Hodges, professor of electrical engineering and computer sciences at the University of California at Berkeley. In Table 1 he trades off its advantages for this purpose against those of bipolar processes. He concedes to bipolar enthusiasts their accumulated design experience and the proven stability as well as the large dynamic range, lower noise and dc offset, and high-frequency response of bipolar devices. He also admits that MOS designers have still a large investment to make in developing a technology relatively untried in this area. On the other hand, he points out that MOS is a low-cost process, compatible with most microprocessors and memories and also well able to implement the filtering functions needed to counter the high noise of MOS transistors.

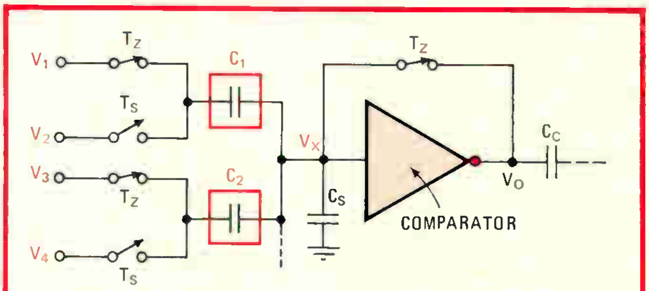
Other MOS advantages are that voltage references exhibit a fivefold improvement in temperature coefficients over bipolar. Also, analog switching may be implemented by current, voltage, or charge methods, whereas bipolar devices can use only current switches. As for the ability of dense MOS devices to pack more functions on each chip, it is to be noted that amplifiers and comparators occupy half the die area they do on bipolars; sample and hold circuits are simple, and there is even a choice of ways in which to implement monolithic filters.

The variety of approaches to the fabrication of monolithic converters has led to another phenomenon—two manufacturers specifying one converter characteristic in two different ways. The semiconductor houses, in addition to taking the most cost-effective approach, are cashing in on the specmanship game that prevails throughout the data-converter community. As far as resolution, accuracy, and linearity are concerned, specifying a-d and d-a converters is open to a good deal of individual interpretation. As when transistor-transistor logic (TTL) first became popular, it is a follow-my-leader situation. The first TTL makers specified the on- and off-voltage and everyone else pretty much took that as the industry standard. In monolithic data converters, the leader was Analog Devices, and its definitions are taken as the ball park for companies specifying the parameters of their often rather different devices.

What this basically means is that if companies A and B both say a part can resolve an analog signal to 10 digital bits, the device of company A may be 10-bit accurate but company B's may only be accurate to within 8 bits, due to the interpretation of the converter's linearity. The interpretation, or misinterpretation, of



1. The big tree. Making analog-to-digital conversions with the usual MOS potentiometric technique is cumbersome. At 8 bits, 256 resistors and 510 analog switches are needed for the tree-decoder configuration. In addition, placing 8 switches from each tap to the comparator input results in a prohibitive total switch on-resistance.



$$V_O = -A\,[C_1(V_2 - V_1) + C_2(V_4 - V_3)]/(C_1 + C_2 + C_S)$$
$$V_O = -A\,(\Delta Q_1 + \Delta Q_2)/(C_1 + C_2 + C_S)$$

2. Comparator is the key. Modifying the input circuits to the comparator allows multiple differential input voltage pairs to use the same node (V_x) as summing point. In National Semiconductor design, charge instead of voltage is measured, amplified, and later summed with other input charges on in effect a real-time basis.

these and other specifications avalanche through other parameters as well, much to the chagrin of a potential user. Yet divergent specifications for the same type of part cannot be attributed solely to the manufacturer's desire to accumulate profit. It is part of a growth syndrome that every new segment of the semiconductor industry goes through before the emergence of clearcut leaders that set de facto standards.

Be that as it may, the new semiconductor makers in the field have a bag of circuit designs that reflect the state of the art in both MOS and bipolar technology. Leading the charge for the MOS side is National Semiconductor. A unique circuit design approach enables National to halve the area occupied by analog switches in a typical 8-bit d-a converter [*Electronics*, March 15, 1979, p. 39]. "The MOS technologies offer many new basic circuit approaches that can be applied to converter products," says Thomas Frederiksen, design manager of data-acquisition products. "One example is the auto-zeroed MOS sampled-data comparator, which consists of a cascade of capacitor-coupled gain stages, where each stage is a slightly modified logic inverter."

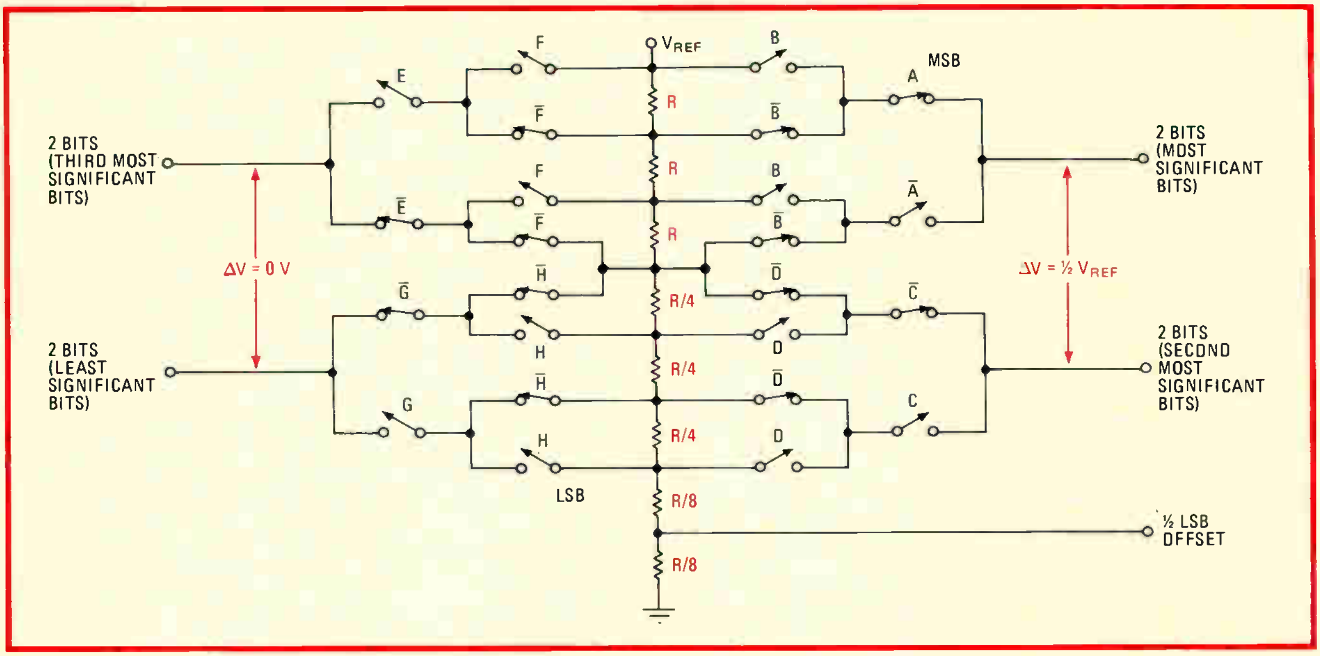
The 2^nR ladder . . .

To go back a year or two, this sampled-data comparator was first used in a National p-channel MOS a-d device, the first monolithic successive-approximation converter. Here a sampled-data comparator switched in known voltage values from a multiply tapped string (ladder) of diffused resistors connected between a reference voltage and ground. This resistor string (itself a relative of the classical R-2R ladder) was equipped with a tap for each of the 2^8 possible analog output voltage levels. It was therefore known as the 2^nR potentiometric technique and became the optimum method of voltage scaling in MOS a-d converters. For instance, it has been used in several monolithic 8-bit a-d converters, including the National ADC0816 C-MOS 8-bit 16-input-channel data-acquisition chip, and also in Intel Corp.'s 8022, a microprocessor complete with a unique on-board 8-bit a-d converter.

To National, however, it appeared that the MOS potentiometric a-d had no future beyond 8-bit designs. Even at 8 bits the converter needs 256 (2^8) resistors and 510 ($2^{8+1}-2$) analog decoding switches, laid out in a tree decoder to reduce the number of drive lines needed for the switches (Fig. 1). Such a configuration eases the layout problem, but places eight switches in series from each tap on the resistor ladder to the comparator input and therefore greatly increases the total switch on-resistance. Worse yet, this many resistors and switches have typically occupied up to 50% of the total die area. Evidently, a simple application of the 2^nR potentiometric technique to 10- and 12-bit a-d converters would roughly double and quadruple their numbers, demanding a monstrously large chip.

. . . with a difference

To avoid this, Frederiksen and his team have modified the 2^nR approach, essentially by expanding the input capabilities of the comparator, the key element in any a-d converter. The new design uses a combination of capacitors and resistors allowing a multiplicity of differential input voltage pairs (Fig. 2). Using input capacitors enables the comparator to compare the directly differential input voltage with the sum total of the effects at the other differential inputs. This is because what is measured is the change in charge, not voltage, at the comparator input. And this charge at input node V_x is amplified, so that many inputs are available for both the input analog signal and the known digital-to-analog converter inputs. If the charge transfer to the input by the d-a is equal and opposite to the charges transferred by the analog differential input, a comparator equilibrium is obtained. At equilibrium, there is no net change in charge at node V_x, a charge-balanced condition. When the sampled analog input value exceeds or is less than the known quantity, the comparator's output is one definite logic state. These states then are summed to come up with the equivalent digital code. The successive-approximation technique then can be implemented with a fast real-time comparison, instead of having to run



3. The result. This innovative circuit allows successive-approximation searches to be made on the same eight resistors by switching in proper taps through 32 switches and measuring the charge across one of four capacitors. Resolution of the ADP0801 converter thus is 8 bits, linear to within ±¼ least significant bit above the quantization error level. A compatible C-MOS and silicon-chrome process is utilized.

through 256 resistors looking for the proper values.

The novelty consists in the capacitor being used to convert voltage into charge and then algebraically summing these charges. Along with the increase in density achieved through a modified MOS comparator comes an additional die area savings made by a resistor ladder of unique design.

In context

The ladder and the new charge-balancing comparator is being used in a 8-bit a-d IC. A single resistive ladder (shown in Fig. 3) is divided into four coarse MSBs and four fine LSBs by the taps of ¼ V_{REF} in its upper portion and taps of 1/16 V_{REF} in its lower portion respectively. The two most significant bits, A and B, increment in ¼ V_{REF} steps and the second 2 bits (C and D) increment in 1/16 V_{REF} steps. By also using voltage scaling, which is provided by ratio-ing the input capacitors, this same ladder is used for the 4 least significant bits (LSBs). The comparator then properly combines all 8 bits over the full dynamic range that 8 bits will provide. Figure 3 shows the first interval of a successive-approximation search when the known d-a input is generating voltage differences of ½V_{REF} and 0 V. At that time the switches are set for A$\overline{BCDEFGH}$. Each of the subsequent steps of the successive approximation uses the same set of capacitors and resistors over and over again.

The complete 8-bit a-d converter requires only 8 resistors, 4 capacitors, and 32 switches and is fabricated from a compatible C-MOS and silicon-chromium process. It has achieved linearity to within ±¼ LSB and can in fact offer 8 bits of linearity with a 100-millivolt input signal.

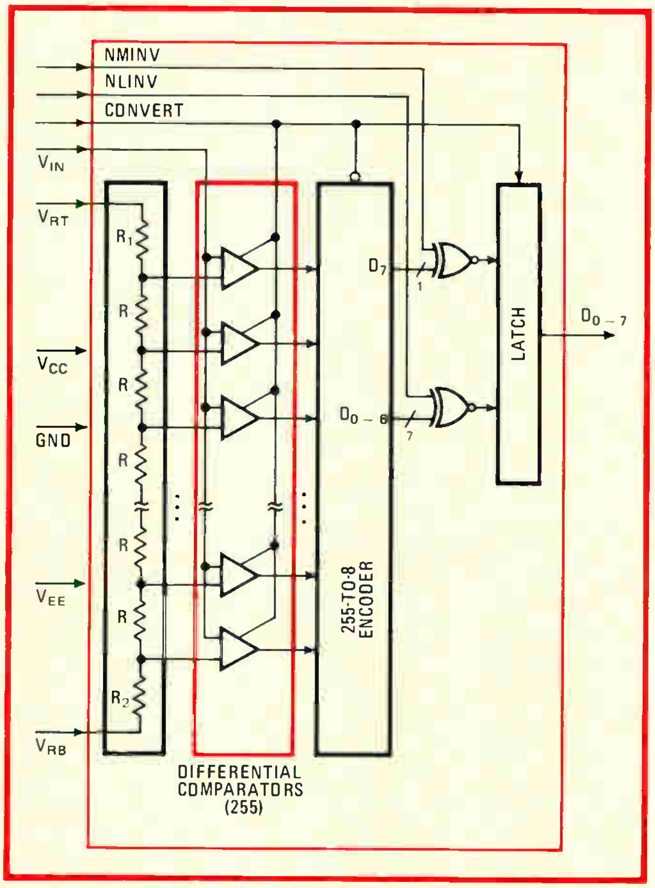
TABLE 2: PRESENT AND FUTURE a-d CONVERTERS FROM TEXAS INSTRUMENTS INC.

Resolution (bits)	Accuracy (%)	Speed	Model number	Application
4 – 7	3 – 4%	< 200 μs	TL 507	appliance and oven control
		> 1 ms		low-cost automotive
8 – 10	0.2 – 0.05%	< 200 μs	ADC0816/ TMS9913	computer and micro-computer interface
		>1 ms	TL 505 A	TMS 1000 microprocessors (5-V, single-polarity bi–MOS technology)
10 – 12	0.2 – 0.01%	< 200 μs	to come	computer and micro-computer interface
		>1 ms	TL 501/ TL 502	3½-digit panel meter
> 13	⩽0.005%	< 200 μs	to come	instrumentation
		> 1 ms	TL 500/ TL 502	4½-digit multimeter

Resolution = accuracy

"For the first time a user can buy an 8-bit monolithic and expect to have 8 bits of accuracy," says Frederiksen. "Underspecifying a converter becomes a thing of the past: now we have a ±¼ LSB linearity, which basically means that the error is only due to the inherent quantization error any converter exhibits, with an additional ±1/16 of a bit."

The same approach is being used in a 12-bit a-d part that National has in the wings. There, four 3-bit a-d converters require a total of only 33 resistors and 64 switches. Besides the 12 bits, there is a sign bit with the polarity of the input voltage handled by interchanging the input switch timing for a negative differential input. This provides an extra bit of resolution without doubling the ladder size. The completely microprocessor-compatible device will contain on-board logic that automatically provides a 2's complement digital output code. To top it off, the 13-bit device will have half the conversion time of the 100-microsecond ADP0801. The 40-pin package will owe its density and speed to silicon-gate C-MOS processing, which produces circuits one half to one third



4. Completely parallel. Triple-diffused bipolar technology from TRW enables 255 strobed comparators, clock buffers, combinational logic, and an output buffer register to be placed on a 261-by-264 mil² die. Parallel comparisons of reference and input voltages yield the dazzling 35 million samples per second of an 8-bit a-d conversion.

the size of their metal-gate equivalents.

Silicon-gate C-MOS is also around the corner at Motorola's Integrated Circuit division in Austin, Texas. "We're looking for an order of magnitude improvement in speed using silicon gate over metal gate," says Mike Hadley, manager of C-MOS product planning and applications. "We plan to use it in our upcoming line of C-MOS digital logic as well as for our converters."

Why C-MOS

Microprocessor compatibility is the key to Motorola's work in data converters. Its first C-MOS 8-bit a-d part in the 10- to 30-μs conversion range will be bus-compatible with C-MOS 8-bit microprocessors, and the company is pushing the work in that converter as hard as it is the work in the MC146805 microprocessor. A final a-d design strategy is just now being defined, with the choice hanging between a charge-balancing technique like National's and a capacitive switching network like the one used in the Touch-tone multiple-frequency receiver chip from Silicon Systems Inc. of Irvine, Calif. [*Electronics*, Feb. 15, 1979, p. 105].

Switched capacitors, which function much like resistors, are one of the most exciting interactions between circuit design and process development to have happened in a long time. So far used mainly for filters, they are distinctly attractive for use in C-MOS converters, where they offer even greater density.

In relation to bipolar converters, the low power consumption of C-MOS is almost always to its advantage but its far higher density is less so. At present, placing more functions on the converter IC is not in its maker's best interests, since that limits the generality of the chip. Ultimately, though, dedicated microprocessors with a-d devices on board will undoubtedly emerge, since the real estate is available—it is only a matter of designing the two separately and, time and experience permitting, putting them both on a single piece of silicon. Motorola is pursuing this line of thought persistently but cautiously and is looking towards a next generation of microprocessors with on-board converters like the Intel 8022, only at higher resolutions.

Meanwhile, however, one function it will definitely incorporate in its converters is the band-gap reference. Although not far enough along the learning curve to compete effectively with the bipolar zener type. C-MOS band-gap references are superior to n-MOS band-gap references, say the Austin engineers.

Dealing with noise

In addition, inherent noise is being minimized in Motorola's upcoming part by clever design—the comparator used in the a-d samples the input data at 100 kilohertz, well above the 10-kHz noise frequency inherent in the MOS transistors, which makes for a very quiet comparator. In fact, its proprietary C-MOS circuits will be running 30% faster than the n-MOS devices, which effectively eliminates noise infringement problems.

Another type of noise that could be a threat, however, is the interference picked up when a converter is located far from what is being measured. For instance, Hadley foresees a system interface generation where an a-d converter on board a microprocessor will be located at a distance from a central processor. Though noise between the a-d and microprocessor would be negligible, noise from the transmission path could be significant. But that hurdle will be jumped when its time comes.

In the meantime, Motorola has parallel efforts going for the various parts of a full C-MOS system. Besides the stand-alone microprocessor and a-d converter, this includes latches, decoders, and transceivers, all designed to work at 4.5 volts at worst-case temperatures at full speed, yet meet all the internal timing requirements. Such an ambitious goal makes 12-bit C-MOS converters a remote possibility with 8-bit types evolving as winners. The company feels that the user's cry for 12-bit parts seems to be for dynamic range rather than accuracy. Besides, at present, the projected volume does not justify a plunge into the 12-bit area in C-MOS.

If the MOS converters are on one schedule at Motorola behind most other MOS participants, the bipolar versions adhere to a different timetable with their own distinct objectives at the division in Phoenix, Ariz. There the MC3508 and MC3510, a couple of 8- and 10-bit digital-to-analog converters, are being manufactured and the MC3512, a 12-bit d-a, is scheduled to be introduced in the fourth quarter of this year.

Bill Carns, of linear marketing, sees Motorola attacking the high end of the precision market in a different manner. He observes that many high-technology hybrid houses, for instance, have pursued the thin-film-on-monolithic-substrate for quite a while, but in the end resort to hybrids in which the active circuits are put on one chip, separate from the thin-film resistor ladders on a second chip. This makes for easier testing of two single chips, as well as for convenience in passively laser-trimming the resistors.

Commitment

Carns emphasizes that Motorola is committed to thin-film resistor technology, applied to single silicon substrates. With expertise achieved in laying down matched resistors on the same silicon substrate as the current switches, methods of actively trimming the network can be developed to achieve better accuracy. The advantage a manufacturer like Motorola has is a broad base of technologies and processes from which to choose the combination best suited to the intricacies of a 12-bit a-d or d-a converter.

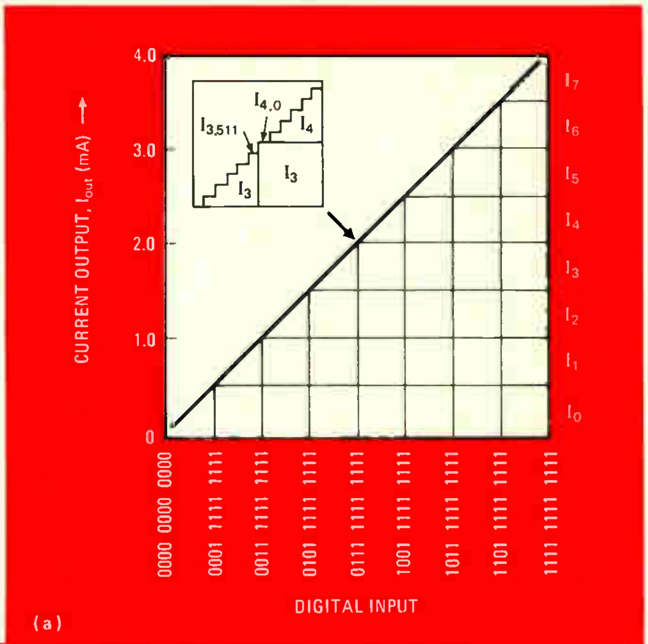
Motorola is even prepared for the high-speed video market. Its 10318 d-a "flash" converter operates at up to 25 MHz, an amazing feat in view of the fact that thin-film resistors on board the chip also provide 8 bits of linearity. Here, the settling time is within 10 ns. This kind of very high-frequency performance cannot be touched by MOS converters and may be the last significant bastion left to bipolar devices.

Signetics Corp., however, is concentrating on getting density rather than speed from its high-density bipolar process, integrated injection logic (I^2L). Developed by its parent company, NV Philips Gloeilampenfabrieken of the Netherlands, the process readily puts digital and analog functions on one chip, and Signetics is using it exclusively for its line of 5018 microprocessor-compatible monolithic d-a converters.

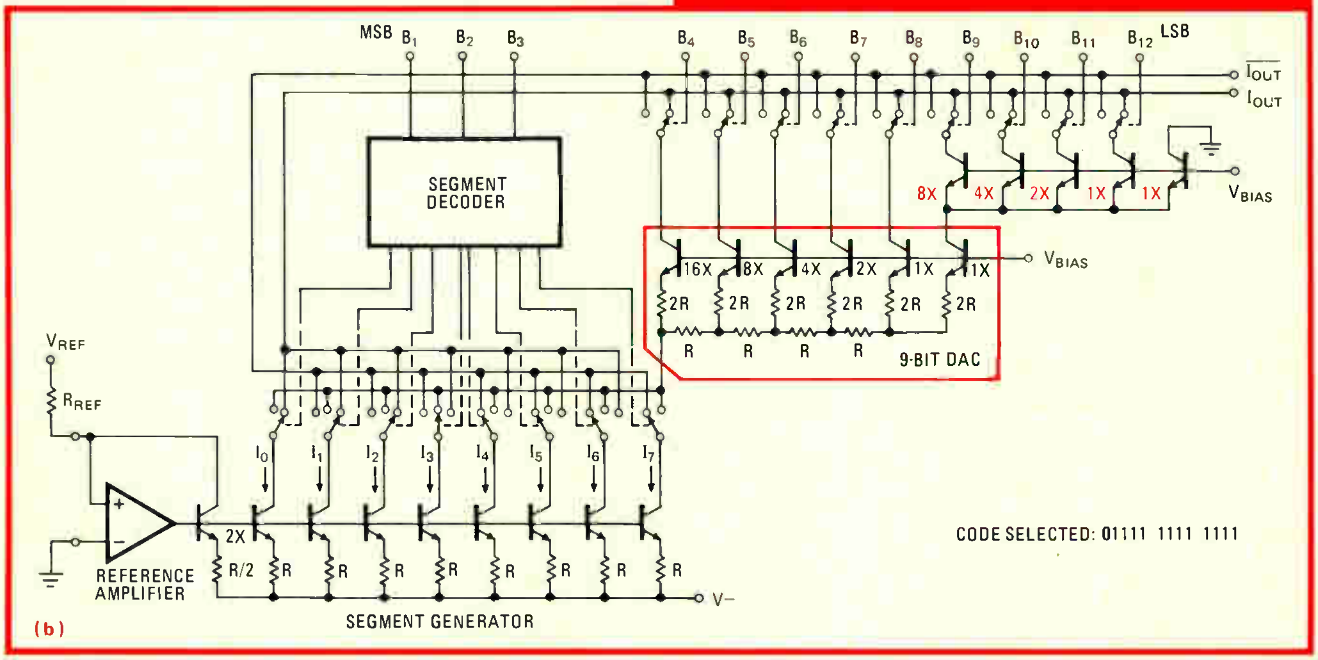
"We don't see anything coming near the speed-power product of I^2L," says Phil Marcoux, interface product marketing section head. "The process that comes closest is C-MOS, but the die is about half again as large as for an I^2L circuit."

The 5018 family, which consists of voltage and current output models, both with ±0.2 and ±0.1% accuracies, will be extended into the 10-bit area before midyear. Beyond that, 14-bit converters in a two-chip configuration are a possibility.

Texas Instruments also is aiming at the low and high end of the converter market but unlike Motorola does not segregate the MOS and bipolar technologies corre-



5. Segmented d-a converter. By dividing the 4,096 output levels of a 12-bit unit into 8 groups of 512 steps each (a), AMD assures monotonicity without using precision thin-film resistors. Diffused resistors of the 9-bit d-a unit (b) determine monotonicity, while linearity is assured by the eight main diffused resistors of equal value.



spondingly. "There is a very large market for the inexpensive and flexible type of IC converters," says Mary Perkins, applications engineer for linear interface products, "but we also see ICs being used for 10 and 12 bits of precision in certain applications. The amount of effort spent in any area will depend upon the volume of the individual markets."

TI will fill only large orders but, when it does decide upon a market, it can pick and choose from a wealth of technologies and designs to come up with an optimum price/performance profile for the device. Its present roster of parts (Table 2) is not impressive for its variety, but it is evidence of the two directions this giant is heading in the converter field: toward low cost, low speed and 4-to-8-bit resolution, and toward high speed and 12-bit and higher resolutions.

A mixture of products does not necessarily reflect a need for mixture of technologies. According to Perkins, if a design goal can be met with a single standard technology, then that will be the road to take, for in the end the product will be more reliable and cost less. However, TI thinks nothing of combining bipolar and MOS on its 8-bit-accurate TL 505 a-d or using integrated injection logic (I^2L) for its 507 microprocessor-compatible 7-bit converter. Also not ruled out is the possibility of placing a 505 converter on board a TMS 1000 4-bit microprocessor, as Intel did with its 8-bit 8022.

Enter switched capacitors

For future MOS-based converters, TI is pursuing switched capacitors, which, for one thing, take up less area than resistors. Consequently, TI's version of National's 0816 data-acquisition system chip measures only 100 by 100 mils, about a quarter of the area of the 0816.

This successful National part has just begun being second-sourced by TI as TMS9913. It uses a 4-bit address code in effect to multiplex its 16 analog inputs, each of which it resolves into 8 bits in 100 μs—a moderate conversion speed. The address input is latched, as is the three-state output. (Another company looking at second-sourcing the bipolar 0816 is Mostek Corp. of Carrollton, Texas, which is further adding to the device's reputation by contemplating a C-MOS version.)

How will TI mix technologies on the same chip? Thus far, it has adopted a split of 95% bipolar, 5% MOS—though the ratio could as easily be the reverse. Its choice reflects what it sees as demanded by the market, for other proportions are technologically possible.

Bipolar speed

Also proving that nothing beats bipolar for very high-frequency conversion is the TDC 1007J, a 35-MHz 8-bit a-d converter made with emitter-coupled logic (ECL) by TRW's LSI Products, Redondo Beach, Calif. Here, it was a matter of optimizing a comparator design and building 255 identical comparators into a fully parallel converter, a most efficient means of achieving high speed (Fig. 4).

As at National, TRW spent a lot of midnight oil on optimizing the comparator circuitry. Each comparator is provided simultaneously with a different reference voltage and input voltage. When the clock switches the device from the sample to a hold mode, each comparator produces a logic level output. The latched AND gates use these results to develop a 1-out-of-256 code, which then is ORed to form an 8-bit word.

Such a pipelined operation yields a 35-MHz speed only when combined with a bipolar derivative of the current-mode form, like ECL. TRW processes the circuits in a triple-diffusion step-down procedure, a five-mask process unique in the industry. The converter's differential nonlinearity is within ±½ LSB. Its drawback is a power dissipation of 2.5 watts. Even Motorola's d-a buzzer, the MC 10318, uses 500 milliwatts. But such power figures must be endured when speed is the goal.

A different goal, one of low differential nonlinearity, is being pursued at another bipolar stronghold, Advanced Micro Devices. Having achieved microprocessor compatibility with its 8-bit Am 6008 d-a converter a couple of years ago, the company is just starting to deliver a 12-bit Am 6012 that is based on the same

TABLE 3: PERFORMANCE OF MONOLITHIC 12-BIT d-a CONVERTERS

	Part number	Settling time (ns, typical)	Differential nonlinearity (maximum over temperature)	Price (quantities of 100 and up)	Speed-accuracy-price product (raw)	Speed-accuracy-price product (normalized)
top grade, military temperature range	Am 6012 ADM	250	± 0.012%	$ 49.95	150	1.0
	HI 562-2	200	± 0.025%	$ 70.00	350	2.3
	AD 7541 TD	500 (estimated)	± 0.025%	$ 69.00	863	5.8
	MP 7621 TD	1,000 (estimated)	± 0.025%	$ 79.50	1,988	13.3
	HI 5612-2	150	± 0.025%	$ 128.00	480	3.2
	AD 565 TD	200	± 0.025%	$ 85.00	425	2.8
low grade, commercial temperature range	Am 6012 DC	250	± 0.025%	$ 9.95	62	1.0
	HI 562-5	200	± 0.025%	$ 19.50	98	1.6
	AD 7541 JN	500 (estimated)	± 0.05%	$ 16.50	413	6.7
	MP 7621 JN	1,000 (estimated)	± 0.05%	$ 16.00	800	12.9
	HI 5612-5	150	± 0.025%	$ 36.50	137	2.2
	AD 565 JN	200	± 0.025%	$ 16.00	80	1.3

SOURCE: ADVANCED MICRO DEVICES

TABLE 4: RESISTOR LADDER COMPARISONS					
Ladder type	Number of resistors	Initial accuracy required for monotonicity (%)	Tracking required for monotonicity (ppm/°C)		Tracking required for ± ½ LSB differential nonlinearity (ppm/°C)
			0 initial error	½ LSB initial error	¼ LSB initial error
Straight R–2R	37	± 0.05	5	2.5	1.25
Segmented 3 bits + 9 bits	24	± 0.4	40	20	10

technology. This part is unique in that it is the first single-chip 12-bit d-a that yields 12 bits of accuracy without individual trimming of its resistors. That is because the circuit design permits the use of boron (in place of thin-film) resistors, which are diffused into the silicon substrate along with the boron transistor bases and need no further modification.

The bottom line is that for the first time a major semiconductor manufacturer can offer a single-chip 12-bit d-a converter for under $10 apiece in quantities of 100. On top of that, the Am 6012 settles within a comfortable 250 ns and displays a differential nonlinearity of ±0.012%, giving it the best speed-accuracy-price product on the market for comparable 12-bit d-a converters (Table 3).

A matter of preference

According to AMD's linear IC design manager, John Schoeff, few transducers are more linear than ±0.1%, so "we found that most people aren't buying converters for straight-line accuracy but for the amount of resolution that will give fine-tuned control to the system the DAC is being used in." This shifts the emphasis from high linearity to differential nonlinearity—in other words, from close conformance with an ideal straight line to a measure of the uniformity of each step in the transfer characteristic between the digital code input and the analog current output.

To guarantee differential nonlinearity, or monotonicity, all classical binary-weighted (R-2R) 12-bit d-a converters require a linearity of ±½ least significant bit (±0.012%) that in turn demands very tight resistor matching and tracking. Table 4 shows the maximum tracking error that can be allowed over a 100°C range to maintain monotonicity. With an R-2R ladder, ±½ LSB differential nonlinearity requires a tracking temperature coefficient of ±1.25 parts per million per °C.

The technique used in the Am 6012 therefore trades off these advantages of the R-2R and the 2^nR network. The 2^nR approach provides monotonicity without requiring high linearity, but if used alone to implement a 12-bit d-a converter would be too dense and too slow. It would require 4,096 low-tolerance resistors, as against the minimum number of high-tolerance resistors of the R-2R approach; its switch decoder tree would also make it much slower than the other approach. The 2^nR and R-2R combination, however, actually requires fewer resistors, and those untrimmed, than does the classic thin-film R-2R network.

Figure 5a shows the transfer characteristic for the segmented d-a converter, as the Am 6012 is described. The 4,096 output levels are composed of eight groups of 512 steps each. Each group is generated by a 9-bit d-a and each of the segment slopes is determined by one of eight equal current sources (Fig. 5b). The resistors that determine monotonicity are in the 9-bit d-a. The major carry of the 9-bit d-a is repeated in each of the eight segments and, to maintain a given differential nonlinearity over temperature, requires eight times lower initial resistor accuracy and tracking than the MSB resistor of a 12-bit R-2R device (Table 4).

All this is achieved with untrimmed resistors, which AMD is able to match simply by diffusing boron into silicon at 1,000°C. In addition, compared to d-a parts using thin-film resistors, the Am 6012 took half as long to design and testing has been greatly simplified.

Resistor pros and cons

Indeed, by going to diffused resistors, Schoeff feels that a number of major pitfalls in the design of d-a converters were entirely avoided. First, thin-film resistors are hard to work with because of the basically amorphous nature of their material; also, even when made of silicon chromium instead of nickel chromium, they are vulnerable to moisture seeping into the package. Second, no expensive laser trimming equipment had to be bought and set up.

Finally, even zener zapping would have worked less well. As is evident from the precision achieved in linear ICs by Precision Monolithics Inc., in which all trimmable resistors are zener-zapped, it is a superior technique of adjusting resistor values because it takes place in the silicon bulk and is not prone to long-term fluctuations due to oxidation at the surface level. But in the case of the Am 6012, it would have complicated the overall system design with its very stringent design rules, according to Schoeff.

How does this new bipolar approach stack up against a 12-bit monolithic C-MOS device that has laser trimming done straight on the wafer? Table 5 compares the Am 6012 with Analog Devices' AD 7541, a full four-quadrant multiplying C-MOS d-a, two converters that exhibit major functional commonality. Besides listing key parameters, the table attempts to highlight what it is about the bipolar and C-MOS technologies that most strongly influences products made in either of them.

Can we expect a similar effort in bipolar a-d devices within AMD? The answer is yes, and the company's first step is to produce an 8-bit part with a conversion time of 1 to 2 μs using a double-layer metal design. More characteristically, 12-bit a-d devices using a low-level current-mode logic are soon to follow and can be produced cost-effectively primarily because of the circuit design innovations applied from the d-a designs.

Meanwhile, Analog Devices is bringing out a microprocessor-compatible successive-approximation 8-bit a-d part for $5. The C-MOS AD 7574 converts in 15 μs and purports to guarantee no missing codes over the full operating temperature range. The device is mentioned here only to show how flexible the converter giant can be, enhancing any parameters it wants to by dipping into

TABLE 5: COMPARING BIPOLAR AND C-MOS 12-BIT d-a CONVERTERS		
Specifications (maximum over temperature range)	Am 6012	AD 7541
Resolution	12 bits	12 bits
Differential nonlinearity (DNL)	± 0.012 / ± 0.025%	not specified
Nonlinearity (NL)	± 0.05%	± 0.012 / ± 0.024%
Full-scale temperature coefficient	± 20 / ± 40 ppm/°C	not specified
Zero scale error	± 0.05 / ± 0.1 LSB	± 0.8 LSB
Setting time to ± ½ LSB	450 ns	1 μs
Propagation delay	60 ns	not specified
Output voltage compliance	+10 to −5 V	0 V
Full-scale current	4 mA	1 mA
Output capacitance	25 pF	200 pF
Power supply sensitivity	± 0.001% / %	± 0.02% / %
Power supply range for full accuracy	+5, −12 to ± 18 V	+15 V only
Power supplies required	2	1
Power dissipation	312 mW	40 mW
Features		
Outputs	differential, complementary	differential, complementary
	R_{out} high for all codes	R_{out} low, varies with code
	C_{out} constant for all codes	C_{out} varies with code — needs op amp phase comparators
	high compliance	no compliance
	no latchup	Schottky clamp needed on output
	no op amp null required	must null op amp V_{OS}
Supply variation	linearity and gain error independent of supply	linearity and gain error highly supply-sensitive
Reference input	2-quadrant multiplying; high-Z input available	4-quadrant multiplying; low input Z
Output range	flexible — two external matched resistors	10-V full-scale for 10-V reference; includes output and reference resistors
Logic threshold	adjustable	fixed
Reliability	no static protection needed	anti-static handling required
Process	standard bipolar diffused resistors no trimming	C-MOS, double-layer metal thin-film resistors laser-trimmed
Package	narrow, 20-pin	narrow, 18-pin

any technology and coming up with 8-, 10-, 12-, and even 18-bit devices packaged in monolithic, hybrid, or modular form. Table 6 reflects this flexibility with a preview of products to come from Analog Devices.

ECL to the fore

In fact, a module using ECL is the first device to be released by Analog Devices as a result of its acquisition last year of Computer Labs Inc., Greensboro, N. C., a supplier of those high-resolution, high-precision converters that can still only be implemented in modular designs. The MOD-1205 printed-circuit card is a 12-bit a-d converter, linear to 13 bits, that converts at a 5-MHz rate. It operates off ±15, −5.2 and −6 V, uses 10 K ECL internally, and produces digital words at Schottky TTL levels. This kind of device is not bought for hooking up to a microprocessor. Mostly for radar-oriented applications, the card sells for a hefty $3,995.

Another noteworthy entry in Table 6 is Analog Devices' second-sourcing of Burr-Brown's ADC80, the successful 12-bit a-d counterpart to that company's 12-bit d-a DAC-80, also second-sourced by Analog Devices.

The developer of the DAC-80 family of hybrids, however, is not idling in the wings. The Tucson, Ariz., company is expanding into high-reliability converters built to military specification.

As a first step, there is its DAC 87-CBI-V/MIL 12-bit d-a device (Fig. 7). This is a souped-up version of the DAC-80, qualified to MIL-M-38510 in accordance with the testing procedures prescribed in MIL-STD-883. This means that the ±0.3% full-scale range is guaranteed over the full −55°C to +125°C temperature range. Also linearity error of ±½ LSB and monotonicity is also good over that range, rather than just 0 to 70°C.

Other ventures

The company's military venture does not stop there. Precision op amps, voltage-to-frequency converters, and multiplier/dividers are in the offing as well in both bipolar and MOS technologies, depending on which technology does more to enhance the highest-precision parts.

The success of these Burr-Brown bipolar hybrids is

TABLE 6: FUTURE DATA CONVERTERS FROM ANALOG DEVICES						
Conversion function	Resolution (bits)	Speed/ throughput rate	Approximate price (quantities of 100)	Technology	Construction	Other comments
a-d	12	5 MHz	–	ECL	board	5 x 5 x 0.4 in. printed-circuit board
a-d	12	3 μs	under $100	I^2L	hybrid	geared to be price/performance leader
a-d	12	–	–	bipolar	–	second source to Burr-Brown
16-channel data-acquisition system	12	35 kHz	under $100	I^2L	hybrid	TTL-switchable between single-ended and differential inputs
8-channel data-acquisition system	12	–	under $12	C-MOS	monolithic	integrating type
a-d	4½ digits	–	–	C-MOS	monolithic	quad-slope, low-cost
d-a	12	200 ns	$17.50	I^2L	monolithic	562-pin-compatible
d-a	12	–	–	bipolar	hybrid	includes output amplifier
d-a	12	–	–	bipolar	–	low power
d-a	12	500 ns	under $15.00	C-MOS	monolithic	serial or 2-byte load
d-a	12	400 ns	–	C-MOS	monolithic	untrimmed
a-d	10	30 μs	–	I^2L	monolithic	complete microprocessor interface
a-d	8	15 μs	$7.50	C-MOS	monolithic	complete microprocessor interface
8-channel data-acquisition system	8	–	–	C-MOS	monolithic	includes on-chip RAM
d-a	8	–	–	bipolar	monolithic	complete microprocessor interface, voltage output
d-a	8	–	–	bipolar	–	second source to Burr-Brown

due largely to their function completeness. They require a minimum amount of external circuitry for efficient operation. They have become so popular that Beckman Instruments, another high-volume hybrid manufacturer, is second-sourcing a C-MOS version of the d-a and plans eventually to do the same for the a-d counterpart.

Meanwhile, though, Beckman is giving priority to a couple of other 12-bit C-MOS d-a products. One second-sources Analog Devices' 7521 multiplying d-a that exhibits a low 20 mW of power dissipation. The other is a Beckman original, the C-MOS 12-bit 7545 d-a converter. Although labeled a microprocessor-compatible part, it lacks the proper on-board timing and control circuitry to be used in a two-chip configuration with 8-bit processors. The advantage is on-board latches that accept the digital data in a 4-bit followed by an 8-bit operation, two steps that yield 12-bit accuracy for the output analog signal.

An alternative version of the 7545, the 7546 d-a has extra output amplifiers on board for both unipolar and bipolar adjustable by ±500 mV. Settling time suffers in return, being 10 μs for the 7546 as against 2 μs for the 7545, both within the full scale of 0.01% linearity.

In praise of hybrids . . .

"This flexibility and precision one can only achieve in hybrids," says Leroy Little, senior development project engineer at Beckman. "Hybrids have always been two steps ahead of monolithics. Whatever semiconductor technology can fit on a single chip, the hybrid can enhance and outmaneuver."

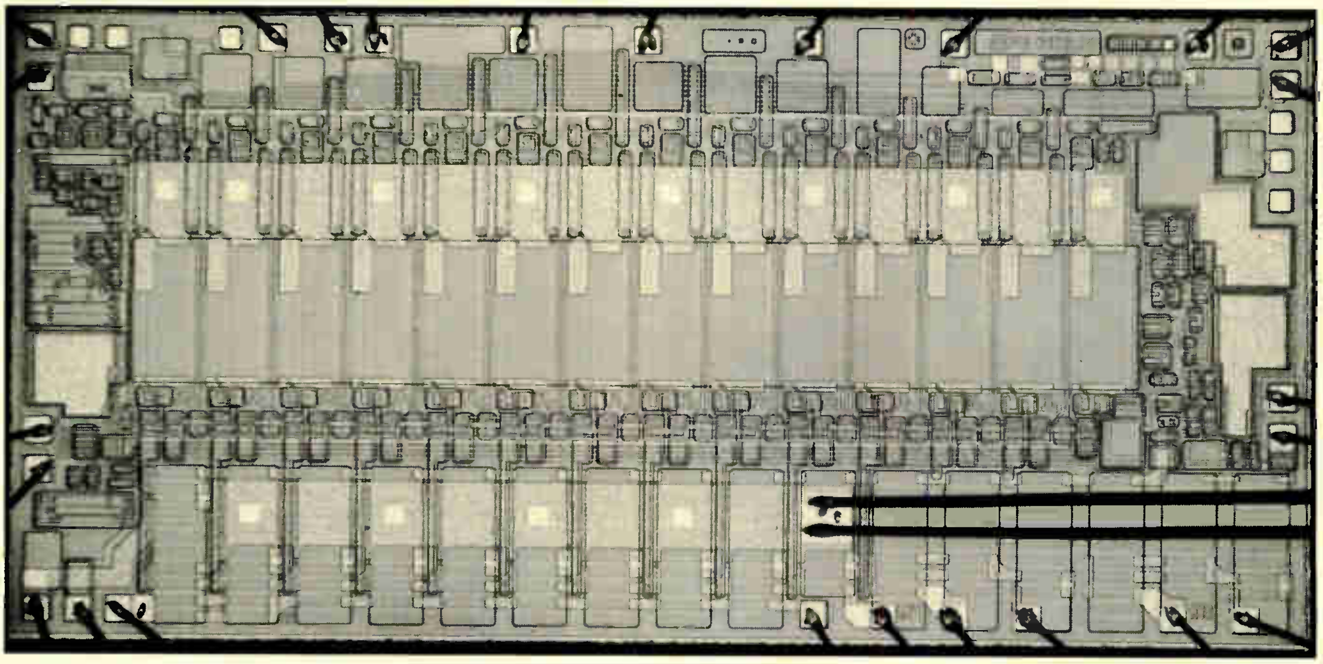
Both Little and William Miller, newly appointed product marketing manager for hybrid microcircuits, feel confident the processing problems of incorporating complex analog functions on a single substrate will keep the cost/performance balance sheet tilted against the monolithic houses through the next couple of years.

"We haven't seen anything from Silicon Valley that comes close to offering the performance of hybrid data converters," says Miller, "and even when single chippers of equal precision hit the streets, potential users will be very cautious about designing in this new breed of converters." But when that onslaught is felt, hybrid manufacturers will be forced into the 16-bit resolution market for applications in instrumentation and measurement equipment.

. . . and their high performance

Until then Beckman expects to introduce more 12-bit parts, with 12-bit a-d C-MOS devices in the short term. Twelve bits is the magic number because of the company's long experience with thin-film resistors, both in military applications and in full line of stand-alone resistor dual in-line packages that are considered among the best. The nickel-chromium resistors are passively laser-trimmed and packaged separately from the active circuits—the only way to go to insure true 12-bit precision and linearity, according to Beckman. Beckman sees monolithics infringing upon hybrid territory only when linearity is achieved in a cost-effective manner: acceptable yields of production parts that are linear (not merely differentially nonlinear) to within ±½ LSB and selling for under $20. Anything better than ±½ LSB would not be cost-effective because yields would be too low. It's all in how much precision one is willing to buy.

The hybrid approach is also practiced at Harris Semiconductor of Melbourne, Fla. The need for rapid development of microprocessor-controller input/output functions in one package such as multiplexing, gain scaling, sample-and-holds, as well as a-d and d-a conversion, will initially oblige manufacturers of both monolithic and



6. Fast and accurate. An output current settling time of 200 ns to 0.01% of the full-scale range is claimed for the Harris 562 thanks to a dielectric isolation process. This bipolar part has its resistors laser-trimmed on the wafer, making it a truly monolithic 12-bit d-a converter.

hybrids to go the hybrid route, according to J. Cornell, director of analog products. "These functions will initially be implemented as hybrids or board-level systems and move toward monolithic functions as appropriate VLSI analog technology emerges."

On the other hand, as Robert Webb, acting technical director for standard analog products at Harris Semiconductor, puts it: "We don't want to stack products with technology prematurely and then be forced into makeshift fixes. Right now we could implant JFET amplifiers together with high-frequency complementary bipolar transistors on silicon-gate C-MOS, if we wanted to. But at this stage of the game, the end product would not be cost-effective." Instead, Harris can go shopping in its technology supermarket and combine the proper ingredients into an ideal price/performance hybrid.

But Harris bakes the hybrid cake differently, for it is perhaps the first company with a broad line of both precision digital and analog products to have realized the cost-effectiveness of leadless chip-carriers placed in standard DIPs. "The yield of hybrids that use leadless chip-carriers is substantially higher than straight ceramic hybrids with wire-bonded integrated circuits," says Webb, "and consequently we can try many variations on mixed technologies using that concept."

Coming shortly

In addition to utilizing this leadless chip-carrier in hybrid converters, Harris will also market other converters and linear ICs that are used in data-acquisition devices in the leadless chip-carriers. Possibilities to come are the HI-5608, a 50-μs 8-bit d-a converter, and two 10-bit a-d converters in the 6-μs conversion range that are microprocessor-compatible. Where the leadless chip-carrier concept will come into big play is in producing the HI-5900, a 16-channel data-acquisition system front-end that includes a C-MOS multiplexer, JFET bipolar gain-programmable amplifier, and bipolar sample-and-hold chips.

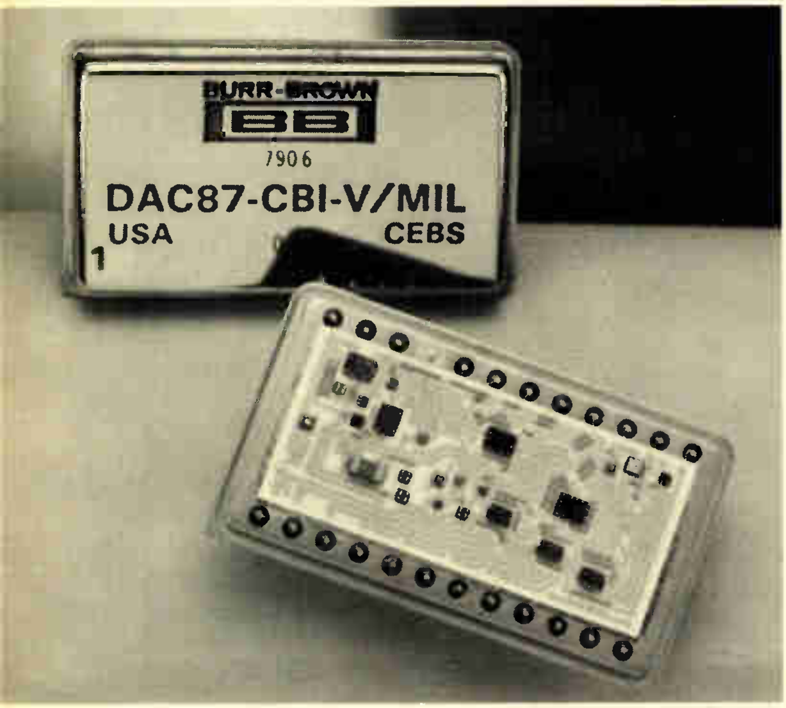
The monolithic objective, though, is to find ways of taking advantage of the low power dissipation and high density offered by C-MOS and increase the speed by innovative circuit designs. Harris's dielectric isolation technique seems to be one way of getting there (Fig. 6).

The company can enhance the performance of a competitor's successful part by using this technique, which apparently reduces internal parasitics, so that rise and fall times during switching become faster and settling time is reduced.

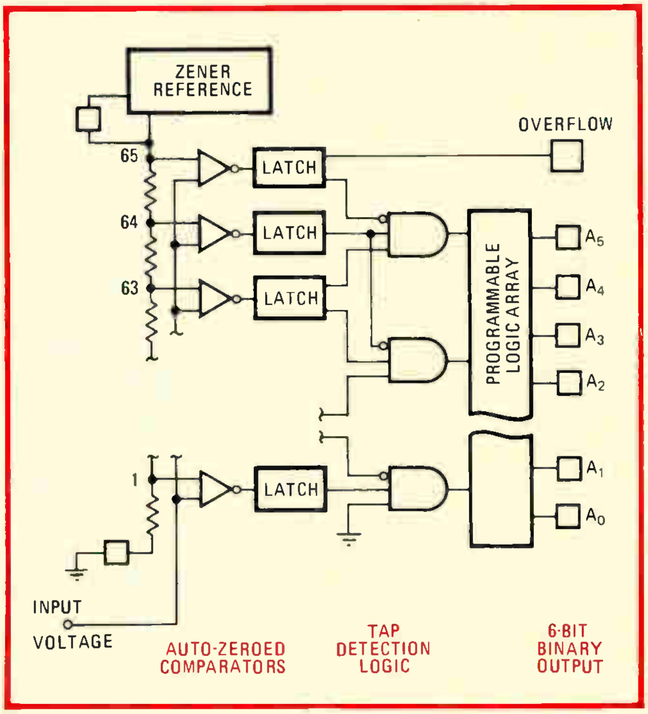
One-upmanship

A case in point is the ubiquitous 12-bit d-a 562 originated by Analog Devices some time ago and specified for a settling time of 1.5 μs. Precision Monolithics Inc., which is second-sourcing the Analog part in a monolithic version, is also specifying 1.5-μs settling time. But Harris slashed the settling time to 0.2 μs, thereby booking its version into wide applications in CRT displays, precision instruments, and full-blown video data-acquisition systems. Linearity is also guaranteed for 12 bits ± 1 LSB over the full temperature range of $-55°C$ to $+125°C$ by laser-trimming the film resistors. Such a combination of speed and accuracy is comparable to the developments now making their debut from purely monolithic houses, like AMD and its 12-bit Am 6012.

RCA Corp.'s Solid State division has another, if not better way. Known as a prime mover of silicon-on-sapphire technology for digital circuits and microprocessors, RCA may also be leading the linear world into the VLSI era with C-MOS on sapphire. There was a hint of this at the ISSCC, where Andrew Dingwall, leader of the technical staff at the company's Solid State Technology Center, described a C-MOS-on-sapphire 6-bit a-d converter that operates at 15 MHz. As a direct counter to



7. Rough and tough. The first of many hybrids from Burr-Brown designed for the rugged military environment is the DAC-87-CBI V/MIL. The functionally complete 12-bit device withstands −55°C to +125°C with a total untrimmed error of ±0.3% of full-scale range.



8. A great combination. This experimental 6-bit a-d converter from RCA combines parallel conversion techniques and dielectric isolation processing techniques in a "flash" 15-MHz C-MOS chip. The sapphire substrate isolates MOS parasitics.

20-to-40-MHz hybrid a-d types, traditionally high-cost items, it could be a cost-effective answer to video needs.

There is nothing magical about silicon on sapphire. It is simply another dielectric isolation technique and as such provides high-speed performance because it keeps parasitic capacitance very low. In RCA's process, C-MOS devices with dielectrically isolated silicon-gate MOS transistors are formed over insulating sapphire substrates. This allows complex logic operations to be carried out at the 40-MHz clock rates necessary to "flash"-convert parallel streams of data.

A crowd of comparators

On board are 65 auto-zeroed sample-and-hold matched comparators occupying 24 square mils each, a density that RCA claims could only be achieved on sapphire. As shown in Fig. 8, the applied analog voltage is compared simultaneously with taps from a reference-voltage resistor ladder. The ladder-tap voltage value that comes closest to the input signal value is then selected by testing the output of each comparator immediately above and below it. Finally a programmed logic array translates the selected value into a binary output.

The comparator is so designed as to maintain a constant charge on the sample-and-hold capacitor, thus keeping input signal loading capacitance to a tiny 0.1 picofarad per comparator stage. The a-d converter can therefore operate from a 75-ohm source at 15 MHz without special buffering.

The converter is not slated for commercial applications at this time. Nevertheless, the part has been successfully tried out in a flat-panel television set operating at 9.55 MHz, or twice the subcarrier sampling rate of a color TV, suggesting an important future application.

As for more down-to-earth parts, RCA is only just feeling the converter market out. "Our converter contribution consists of the CA 3161 and CA 3162," says George Granieri, product marketing manager of industrial bipolar integrated circuits. "They are a decoder/driver and a 3-digit a-d converter and together make up a low-cost a-d readout system the user can put together himself."

Granieri states that RCA is on the brink of having numerous mixes of technologies fall out into interesting products. A simple 8-bit a-d converter that will be compatible with the company's C-MOS microprocessor, the 1802, should be available as a sample before midyear, with gradual sophistication of additional functions placed on board later.

Onward with bi-MOS

RCA, of course, has at its disposal its technology center where new technologies, and circuit techniques can be discriminately picked and incorporated for commercial consumption. In the linear area, it is banking on the mixed bipolar and MOS linear technology, bi-MOS. Operational amplifiers and comparators in bi-MOS with impressive input bias current characteristics, typically on the order of 50 picoamperes, are just some of the functions to be included on board future data converters. Although said to exhibit higher noise, Granieri says that the 40 nanovolts-hertz$^{1/2}$ measured is no worse than for some rival bi-FET devices. Competition between bi-FET and bi-MOS linear parts has been growing rapidly and could be discussed at some length, but that is the subject of another story. □

Bubble memories demand unique test methods

Complex test system must adjust magnetic fields, find operating margins, and map bad loops

by Steve Bisset, *Megatest Corp., Santa Clara, Calif.*, and Steve Bristow and Tom T. Chen, *Rockwell International Corp., Richardson, Texas*

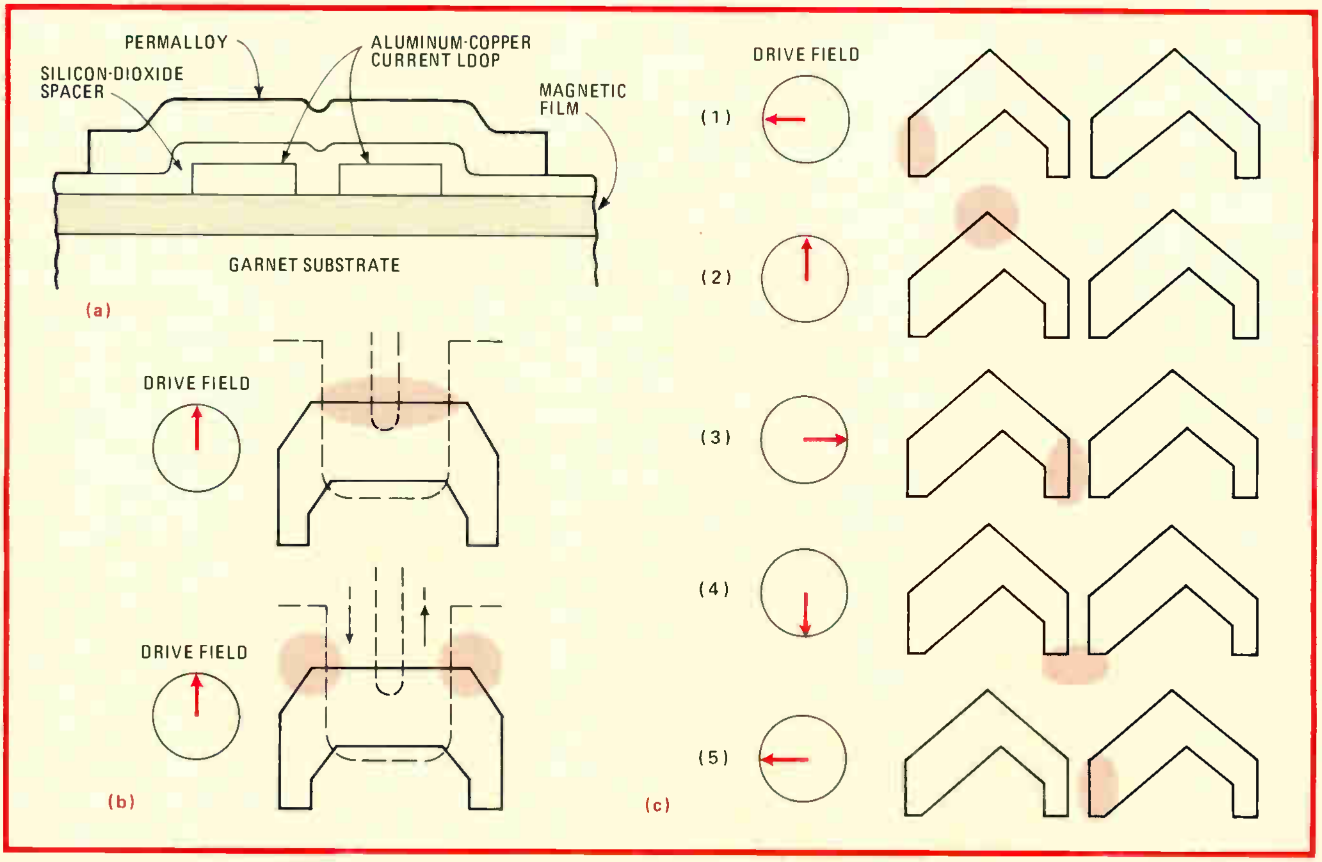
☐ Reliable, reasonably priced test procedures play a vital role in the commercial acceptance of any new microelectronic technology. Bubble memory devices are no exception. They bring with them a fresh rash of characterization problems requiring specially designed test systems, for the varying magnetic fields that manipulate the bubbles must be carefully timed and balanced, while their high-density shift-register architecture and submegahertz clock rates result in test times of several minutes per device. Between them, all these requirements exert a significant upward pressure on high-volume testing costs.

There are four stages in the bubble memory manufacturing process at which tests are typically needed, exclusive of quality assurance testing:

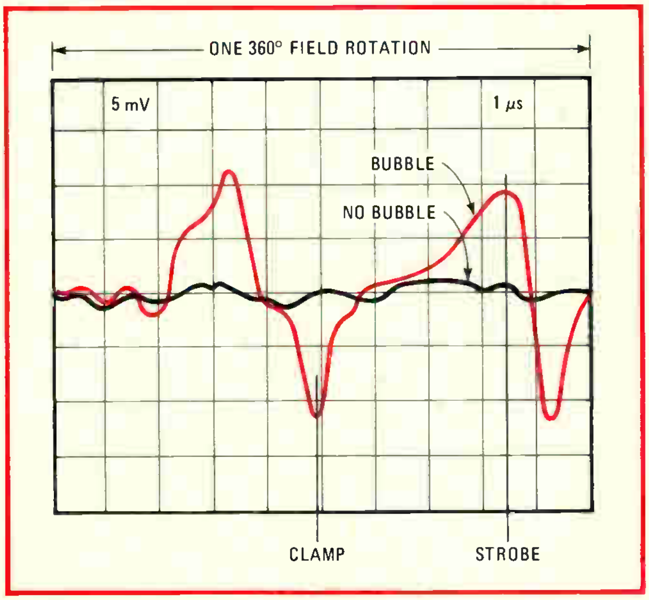
■ Wafer probing is carried out before the individual memory chips are separated. This must be done without the drive-field coils that will later be wound around each die. The drive field is approximated using coils placed above and below the wafer; several hundred watts are required to drive these coils.

■ A bias search is done before the device's bias field magnets are installed. An electromagnet supplies the bias field so that operating regions may be checked at several field levels and an optimum level found.

■ After the permanent bias-field magnets are mounted



1. Internal operations. The cross-sectional view (a) is that of a bubble gate component. The replication operation, viewed from above in (b), is achieved by providing a sharp current pulse to the gate's loop to collapse the bubble domain in the center. The drive field's magnitude and phase can be varied to test for proper pattern spacing and processing as well as bubble propagation (c).



2. Differential detection. The voltage across the detector at two points—clamp and strobe—during a cycle is compared to sense a bubble passing under it. Detector sensitivity is tested by varying the clamp and strobe points and the comparator thresholds.

above and below the memory chip, magnetization must be checked and precisely adjusted to compensate for variations in packaging and processing.

■ Following installation of the magnetic shields the memory is subjected to rigorous final testing under many variations of worst-case operating conditions. Defective storage loops are identified and mapped, in some cases on a special extra loop, in others on some external medium, such as a specification sheet or electrically programmable read-only memory.

Interface circuits

The active sections within a bubble memory device include current-loop circuits (gates), detectors, drive-field coils, and bias-field magnets. A test system for bubble devices must have interface circuits capable of altering the control parameters associated with these sections so as to permit device characterization as well as fault analysis.

The gates are formed by depositing a conductor loop beneath a permalloy pattern; the loop, when energized, creates a local magnetic field. The gates are responsible for generating (or nucleating), transferring, replicating, and annihilating bubbles (Fig. 1a). Each operation is dependent upon the phase, width, and amplitude of the current pulse through the gate's loop.

A very strong current pulse can reverse the magnetization within the loop and nucleate or generate a reversed magnetic domain—a bubble. A strong current pulse in the opposite direction can be used to collapse or annihilate a bubble that is within the loop. The field generated by the loop can also be used to attract or repel a bubble, steering it from one path to another; this is the basis of the transfer and swap functions. Replication is implemented with a narrow current loop. In this case a strong current pulse will cut or split the bubble domain into two separate bubbles as shown in Fig. 1b.

A bubble memory test system must be capable of supplying pulse waveforms adjustable in amplitude, phase, and width. These parameters should be very flexibly programmable to fully characterize the device's operating margins. Some of the pulses must be greater than 360° in width; they must be able to overlap propagation cycle boundaries (see Fig. 1c).

Reading output

The tester must also sense or read the bubble memory device's output of stored data, so it needs circuitry that interfaces the device's bubble detector. A bubble is sensed by measuring the change its presence causes in the permalloy detector's resistance. The magneto-resistive effect is responsible for this change. The resistivity of a permalloy film varies as a function of the angle between the magnetization vector and the direction of the current flow through the film.

The resistance of the permalloy film is also influenced by the direction of the rotating bubble-propagation drive field. This effect is much larger than that caused by the presence of a bubble; the actual bubble signal would appear as a small perturbation on the overall output signal. This is dealt with by using a dummy detector circuit in close proximity to the first detector. The rotating field signal appears as a common-mode signal in both detectors. It is easily eliminated, leaving the differential bubble signal standing alone.

Typically, the tester's sensor samples the differential output voltage at one point as the bubble passes under the bubble detector—the clamp point—and compares it to the voltage at a second point as the bubble continues passing under the detector—the strobe point (Fig. 2). This provides an indication of detector sensitivity. The tester should also have dual comparators to test for the noise margin on the outputs. The phase of the clamp and strobe points must be programmable, as must be the threshold of each comparator.

A bubble memory's permanent bias magnets generate a uniform field nearly perpendicular to the plane of the magnetic film in which bubbles define themselves by their reversed polarity. The bias field is set at a slight tilt with respect to the perpendicular in order to create a small in-plane field component that insures bubble nonvolatility when the device is not in operation.

The bubble-propagation drive field is generated in the plane of the magnetic film by two coils wound around the device at 90° to one another. The two coils are driven by currents with triangular, trapezoidal, or sinusoidal waveforms; the two drive currents are 90° out of phase with one another. The magnetic fields generated result in an in-plane field vector that rotates to drive the bubbles along the permalloy pathways.

Field margin testing

The tester must be able to vary the magnetic environment it generates in order to determine the performance margins of the bubble devices at various production stages. More specifically, it needs to vary the magnitude of the drive field from a peak current of a few hundred milliamperes in the device's own coils to several amperes in the big wafer-probing coils. At the wafer probing and bias search stages, before the device's own permanent bias magnets are mounted, the tester must drive bias magnet coils as well.

An overly strong bias field will tend to collapse the bubbles; too weak a value may allow spontaneous nucleation of extra bubbles, or cause bubbles to revert to stripe domains (stripeout). Either case is a data loss. Figure 3a is a typical operating margin limit curve for the bias field (H_B) and the drive field (H_D). Within the range of bubble stability between collapse and stripeout, the size of the bubble is determined by the strength of the bias field. Most of the permalloy patterns that direct bubble propagation require a specific bubble size to operate properly.

There is a minimum value of drive field strength below which the bubbles will move unreliably or not at all. If the drive field is too strong, the magnetic field under the permalloy patterns will cause stripeout or bubble nucleation at low bias-field values. At elevated temperatures, an overly strong drive field may also cause spontaneous nucleation. This is worsened by the excessive device temperature caused by increased power dissipation in the drive coils at high drive currents.

Each chip function exhibits a different operating region. The gates have multidimensional margins: they are affected by the amplitude, phase, and width of the loop current pulse as well as by the strength of the bias and drive fields.

Once a nominal set of pulse parameters is found, the operating regions for the various functions can be compared. Figure 3b shows typical operating regions for bubble propagation, transfer-out, replication, transfer-in, generation and detection functions. The overall operating region of the chip is the intersection (shaded area) of all these regions. Chip design is optimized in part by designing each function so as to maximize the intersection of the various operating regions.

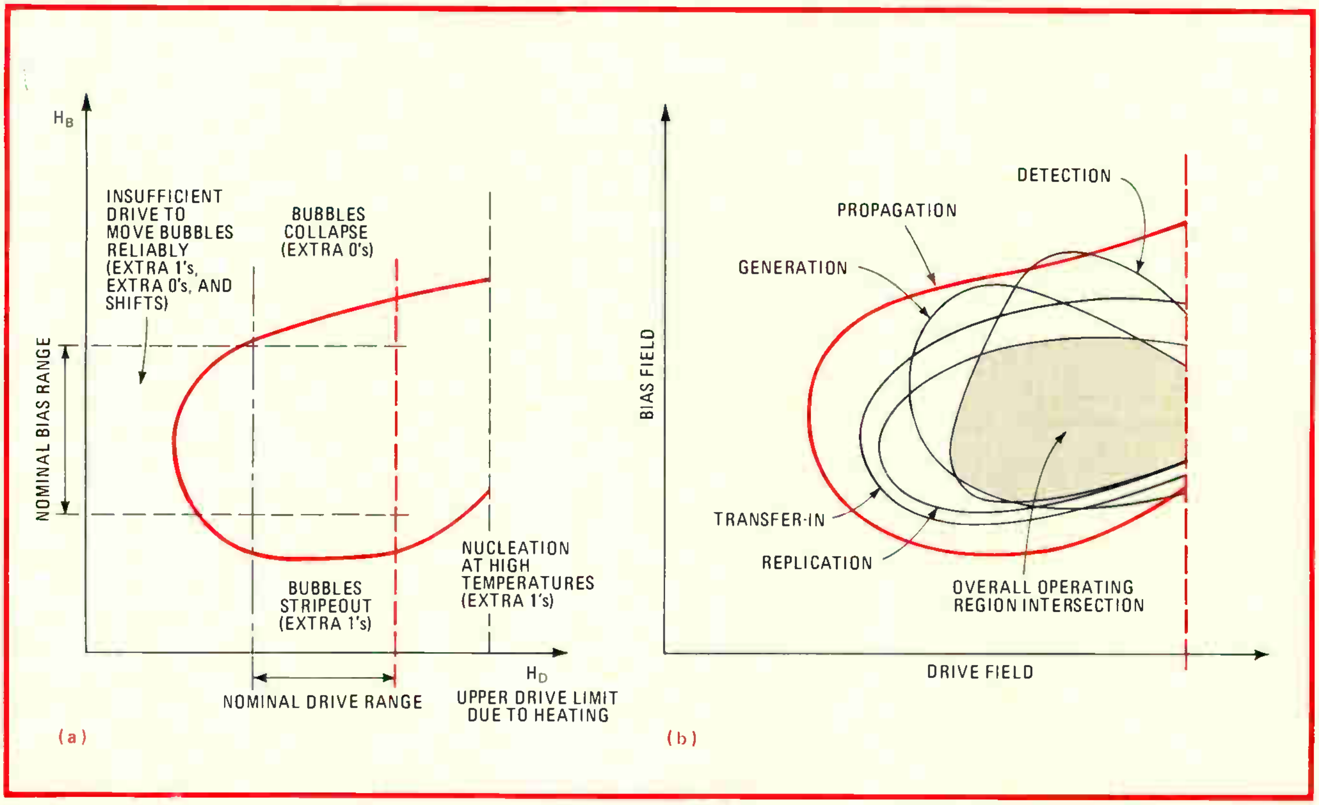
Isolating the functions

To analyze factors limiting chip performance, it is necessary to isolate the operating region for each function. Since the bubble device is serial, it would appear to be impossible to determine which circuit function failed in response to a change in bias or drive field. However, fault isolation can be achieved by making a momentary change in the field.

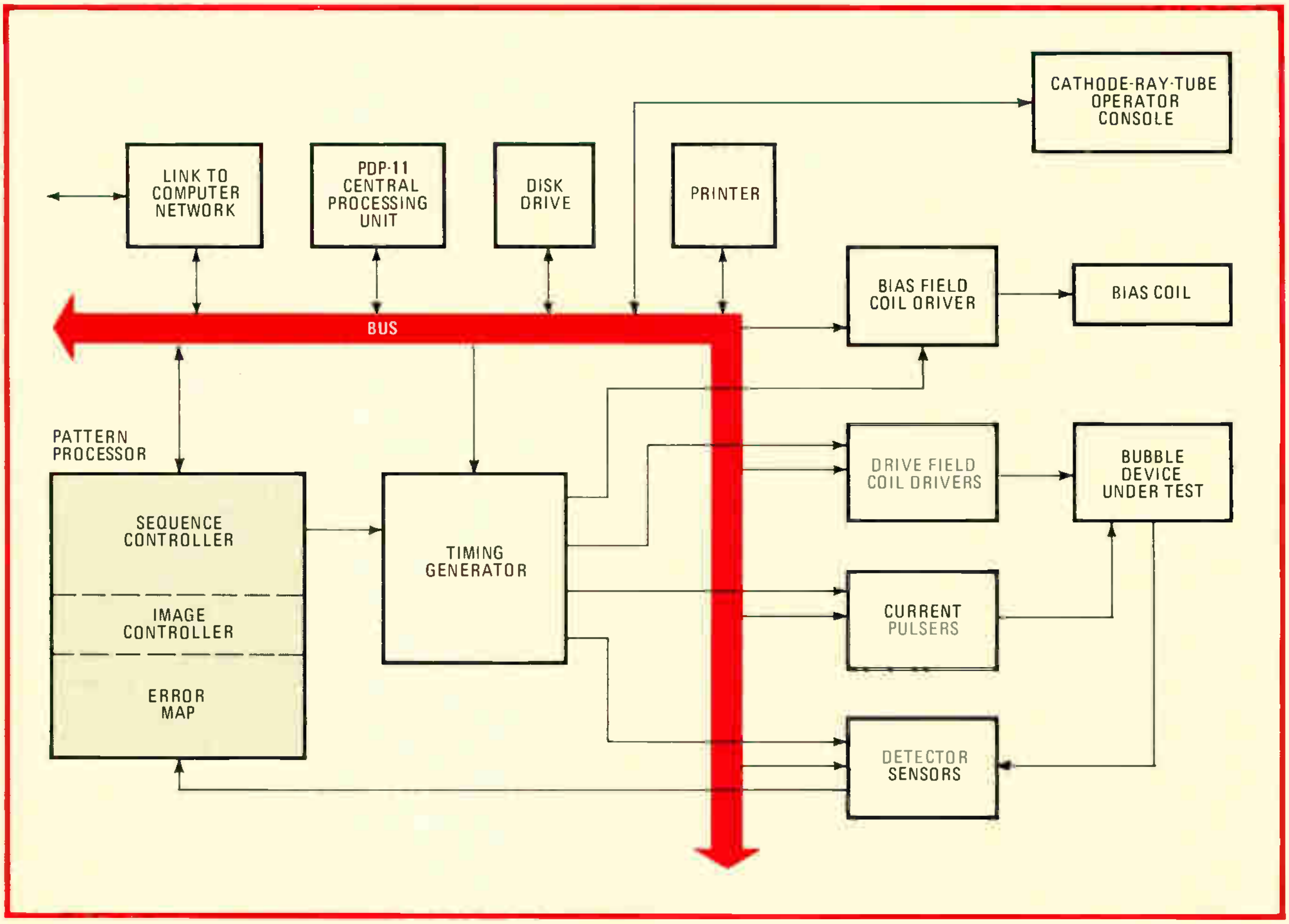
For example, to analyze the operating region of the transfer-in function, operating conditions under which all chip functions work must first be established. Then, during the cycle in which the transfer-in function occurs, the tester steps the amplitude of the bias field and/or the drive field to an alternate value; when the transfer-in cycle is over, it returns the fields to nominal values. The alternate value can be varied to characterize the transfer-in function without greatly affecting the operation of any other function.

Thus, to be capable of device characterization, it is necessary for the test system to be able to switch bias and drive field values on the fly. A portion of the test system is devoted to controlling the interface circuits in the complex manner required (see Fig. 4 for a functional block diagram).

Unlike semiconductor devices, bubble devices have no residual or background charge problems. Data storage is



3. Operating margins. The magnitude of the drive field (H_D) and bias field (H_B) limit the operating margins (a) of a bubble device. Each function exhibits a different operating region (b). The intersection of all these regions determines the device's overall operating region.



4. Tester architecture. Putting a magnetic-bubble memory through its paces calls for a machine made up of many functional subsystems. Circuits that interface the device, on right-hand side of diagram, are controlled by the processors and computer on left-hand side.

in terms of discrete units; there is no such thing as half a bubble. But there is a potential problem of bubble pattern sensitivity, involving the interaction between bubbles. This sensitivity is of a localized, two-dimensional nature. Two nearby bubbles will repel each other; if a bubble is surrounded by other bubbles, the resultant increased field may tend to cause a collapse. The interaction between bubbles is quite significant. In fact, experimental devices have been made where the presence or absence of one bubble is used to control the propagation path of another.

Pattern sensitivity testing

In order to test for problems caused by this sensitivity, the test system programmer can load the memory device with various patterns of 1s (represented by bubbles) and 0s (array spaces without bubbles) and check to see that they emerge unchanged. Any changes in the patterns when read from the device being tested are stored in the tester's error map. Errors can then be analyzed to locate problems and identify faulty storage loops.

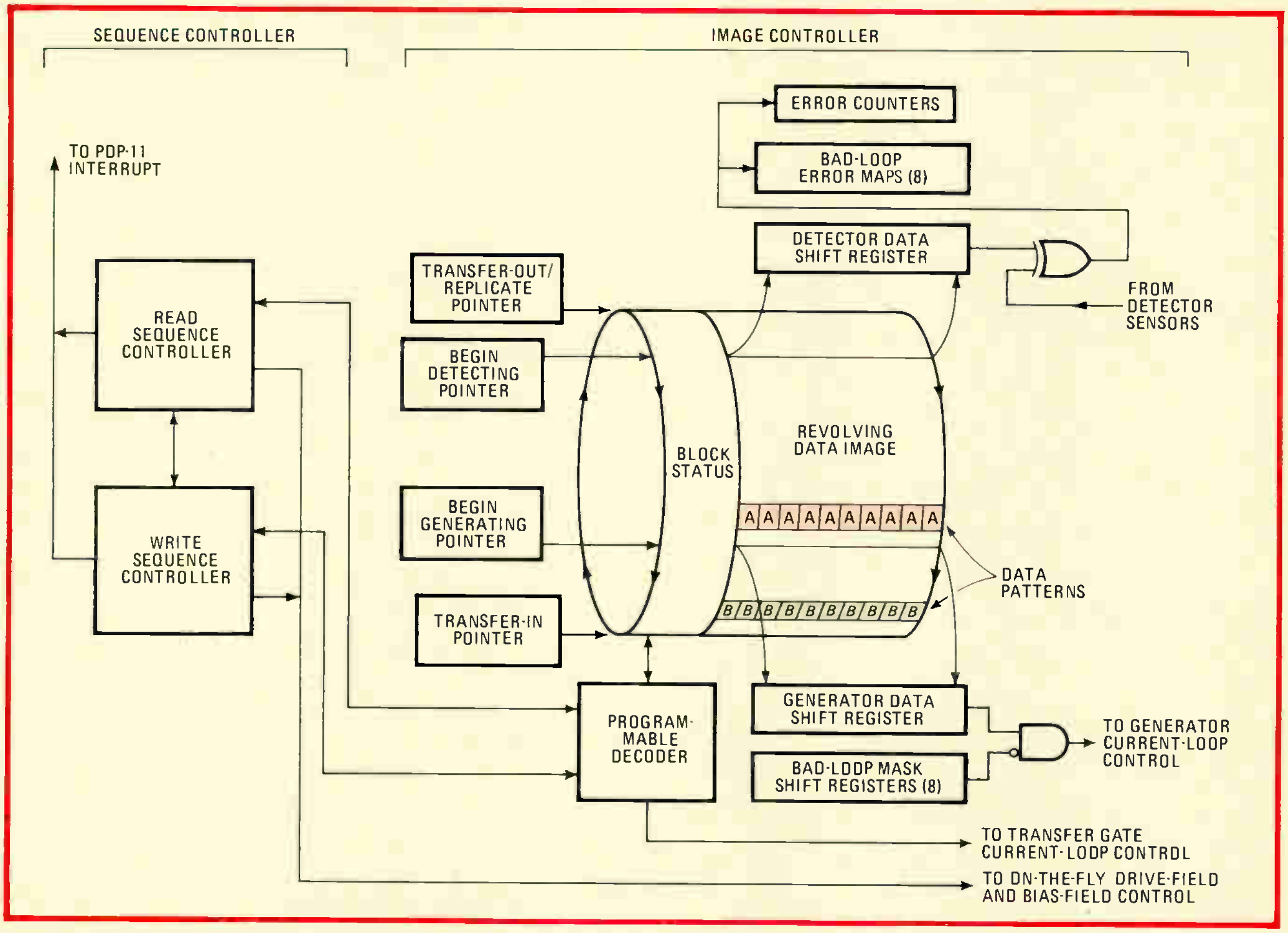
Since bubble devices may exceed megabit storage capacity in the not-too-distant future, it is impractical to specify each bit of data stored on the chip for each type of test performed. Fortunately, it is not necessary to do this. The image controller permits the programmer to specify a topological image of the data to be written into the device. He need only specify the pattern as a two-dimensional array of 1s and 0s.

The image controller also allows him to specify the status of each block location on the minor (storage) loops—e.g., full, empty, written, read, blank, etc. (A block is the string of locations, one on each storage loop, that are lined up such that they all reach the transfer-in or transfer-out gates at the same time.)

As there is negligible interaction between bubbles spaced more than a few periods apart, it makes sense to repeat the same test pattern after every few minor loops. The loops are divided into a series of equally sized groups (generally no larger than 16 loops wide) that store identical patterns.

It is usually unnecessary to fully load each loop with bubble patterns, since a pattern a few bubbles long is shifted around the entire loop, eventually passing through each site. It is, however, desirable to write in two or more patterns at locations widely spaced along the minor loops, to determine, for example, the extent to which bubbles passing on opposite sides of a loop will interact. Figure 5 portrays the data image as a cylinder that revolves as the bubbles propagate around the storage loops. The example has individual patterns A and B repeated across the chip's storage loops.

The architecture of a bubble memory requires that the test pattern as it ultimately appears topologically on the



5. Pattern processor. Data blocks are generated and monitored to test data-propagation pathways, bubble pattern sensitivity, and various gate operations—and to locate bad loops and mask them out. Extra loops compensate for defects, to keep yields high.

chip be written sequentially, block by block. The sequence can be looked at either as the order in which data blocks are written into their storage loop locations or in terms of the time delay between events, as measured in clock (drive field rotation) cycles.

Pattern sequencing

The test system's sequence controller provides cycle-by-cycle pulse control in addition to on-the-fly changes in bias and drive field. The sequence controller (a part of the pattern processor, which also contains the image controller and error map) does its job using software suited to high-speed manipulation of clock cycles. Program routines controlling the writing order of data blocks can be constructed as functions of clock cycle manipulation.

The delay between various events is determined by chip architecture. For instance, before transferring a block of data into the storage loops, the block must be generated one bit at a time and shifted along a "leader" track onto the generate track that runs along the transfer-in gates. With some architectures, the delay between the generation of the first bit of a block and the transfer-in pulse that moves the block into the storage loops may be given by $P(N+L)$, where P = the drive cycle period, N = the number of storage loops (block width), and L = the number of locations on the leader track. The delay between transfer-in and transfer-out is determined by the length of the storage loops; a block must travel halfway around the loop in order to reach the transfer-out gates.

The test system may use four image windows or pointers to keep track of data blocks during read and write operations. The windows shown in Fig. 5 are actually incrementing pointers that access a four-port memory containing the data image and block status. One window points to the block positioned at the transfer-out/replicate gates on the current cycle. If a block is transferred out, another window points to that block when its first bit approaches the detector. Another window monitors the block positioned at the transfer-in gates, and a fourth window indicates when the first bit of the block must be generated prior to transferring in.

Sequence control

To write a data block, the sequence controller produces an "access request." This essentially transfers the appropriate block of data into a shift register, from which it is shifted serially into the chip's bubble generator. The block status is set as "block generation initiated, but block not yet transferred." When the transfer-in window encounters this status the transfer-in pulse is generated. In this way the sequence controller program tracks events on a block-by-block basis, with the image

```
PHASE: = 0;
.
.
.
DO              40;                       (Begin outer loop)
$INT                                      (PDP11 interrupted here)
    DO              5;                    (Begin intermediate loop)
        AR,     TR;                       (Access request, Transfer request)
        DO              287;              (Begin inner loop)
        END:            NOP;              (Wait for block to be generated)
    END:            NOP;
$P                                        (Indicates PASCAL code executed when PDP11 is interrupted)

PHASE = PHASE + 2;

PULSETIME (XFERIN, EDGE1, BANK1, PHASE); (Sets pulse phase into programmable phase generator)

$S                                        (More Sequence Controller code)
END:            NOP                       (End outer loop)
.
.
.
```

6. Enter Pascal. The sequence controller is programmed with a block-structured language that uses nested loops to produce a serial data stream. This printout shows the PDP-11's Pascal coding mixed in to test the effects of varying transfer-in pulse phase.

controller completing block write and read operations as a function of chip architecture.

Sequence control is simplified somewhat by making the write and read functions simultaneous but independent. This is performed by a separate generator sequence controller and detector sequence controller. These controllers should be programmed in a simple but powerful block-structured language that expresses events as a series of nested loops.

The Megatest Bubble Memory Test System [*Electronics*, April 26, 1979, p. 167] incorporates a PDP-11 minicomputer using an extended version of the high-level language Pascal to control the complex operations of the pattern processor. Figure 6 shows how the programmer interleaves Pascal source code with the sequence controller's block-structured code in order to synchronize the simultaneous operation of the PDP-11 and the sequence controller. This program section writes 200 blocks of data, with the phase of the transfer-in pulse being incremented 2° for every 5 data blocks. It is then possible to see how a stream of data being written into bubble storage is affected by the phase shift of the transfer-in gate's waveform over an 80° test span with respect to the drive field. This is done to determine the optimum phasing of the transfer-in pulse.

To achieve reasonably high yields in the production of these dense devices, a certain percentage of the storage loops are allowed to be defective. The memory chip is made with extra loops to compensate for the defective loops. The test system locates the bad loops and stores the information in a map. It also keeps track of the overall error rates, the number of errors on each loop, and the total number of bad loops.

When a bubble memory is put into service, a mask register permits selective masking of bad loops, so that bubbles are not written into them. Some bubble chips have an extra loop with independent transfer gates that is used to store a map of the bad loops.

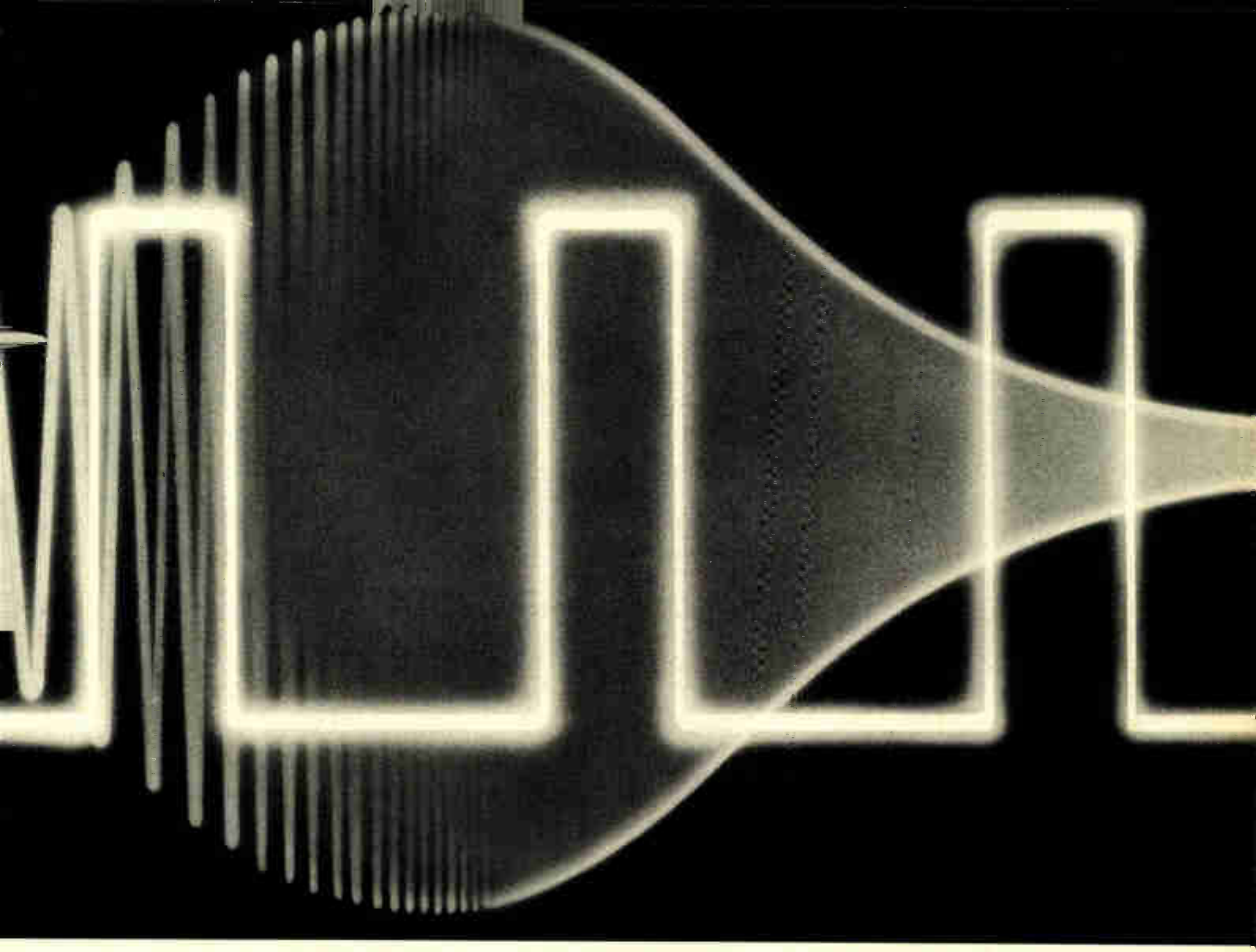
Economics

Final test times for quarter-megabit devices generally range from over a minute to several minutes. Since bubble devices are serial, the increase in test time as storage capacity rises will be more linear than exponential. Nevertheless, it is obvious that testing will be a significant manufacturing cost.

Tester accuracy and test sequence flexibility requirements make it impractical to create a production test system that is significantly less expensive than a system designed for device analysis. Therefore, other means of cost reduction must be used.

Bubble devices will be the first large-scale integrated devices for which parallel testing is truly cost-effective. This is so because the yield at final test should be very high, because of the rejection of most bad devices at the three previous testing stages. The test system must be able to support a large number of device interface circuits, and must simultaneously provide individual error mapping and bad loop masking for at least eight memory devices.

Throughput is further optimized if the tester has a flexible pattern processor that allows any required test sequence to be generated with minimum software overhead, simultaneous write and read capability, and a pattern processor that can be operated in parallel with the general-purpose computer. □



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Circle 123 on reader service card

Voltage-to-current converter handles bilateral signals

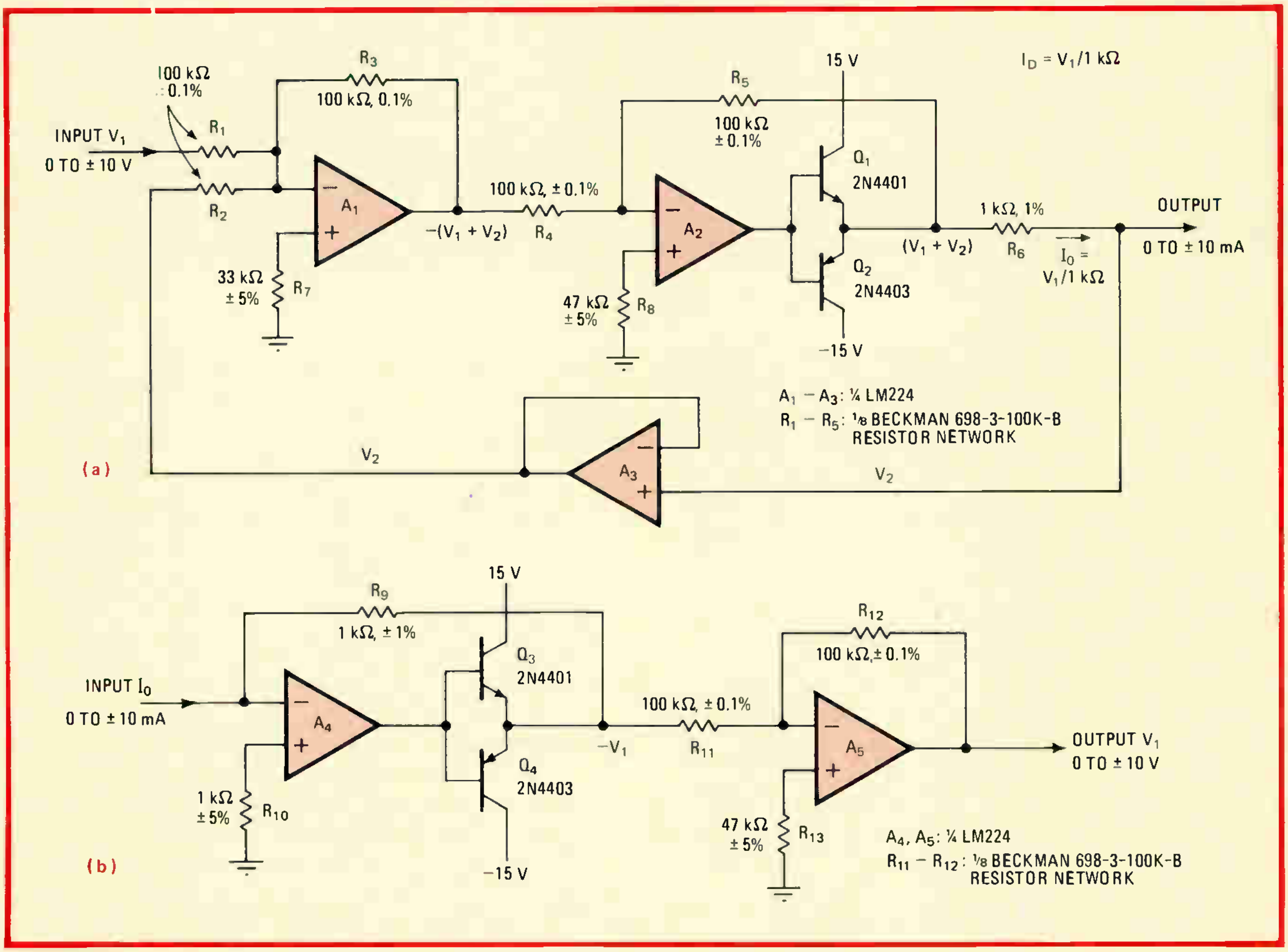
by Kelvin Shih
General Motors Proving Ground, Milford, Mich.

Sending an analog voltage from one point to another via a slip ring and brush assembly often causes disaster in instrumentation applications, because of the attendant voltage drops across the variable resistances encountered and also because of induced noise. By converting the voltage to a current before transmission (and back to a voltage at the receiving end), however, these circuits eliminate those problems. And unlike converters that generate a problem of their own—their inability to handle bilateral input signals—this one will transform a ±10-volt signal into a ±10 milliampere current at the transmitter and recover the ±10-V signal at the receiver.

At the transmitter, input voltage V_1 is applied to one branch of a summing-amplifier circuit consisting of A_1, R_1–R_3, and R_7. The other branch is driven by V_2, which is the transmitter's output voltage. As a consequence of this feedback arrangement, the voltage from inverting amplifier A_2 is $V_1 + V_2$.

Current booster Q_1–Q_2, which is part of A_2's feedback resistor network, provides a low-impedance source for generating a current, I_o, with Q_1 becoming active for positive input voltages and Q_2 active for negative input voltages. Thus, $I_o = [(V_1 + V_2) - V_2]/R_6 = V_1/R_6$, and therefore the output current is a function of input voltage V_1 only.

At the receiver, A_4, Q_3, and Q_4 detect input current I_o and convert it to a voltage, $-V_1$. Note that the two-transistor arrangement similar to that employed in the transmitter is again required to process the bilateral input currents encountered. A_5 acts as an inverting amplifier so that the output signal, V_1, is recovered. □



Communicating current. Converter (a) transforms bilateral analog voltages into corresponding currents for high-accuracy transmissions over high-resistance networks. Receiving converter (b) performs inverse operation to recover input voltage. Low-cost op-amps and transistors are used throughout. Beckman package in (a) and (b) provides low-cost source of matched resistors required for very precise conversions.

Cascaded C-MOS blocks form binary-to-BCD converters

by Haim Bitner
Seforad-Applied Radiation Ltd., Emek Hayarden, Israel

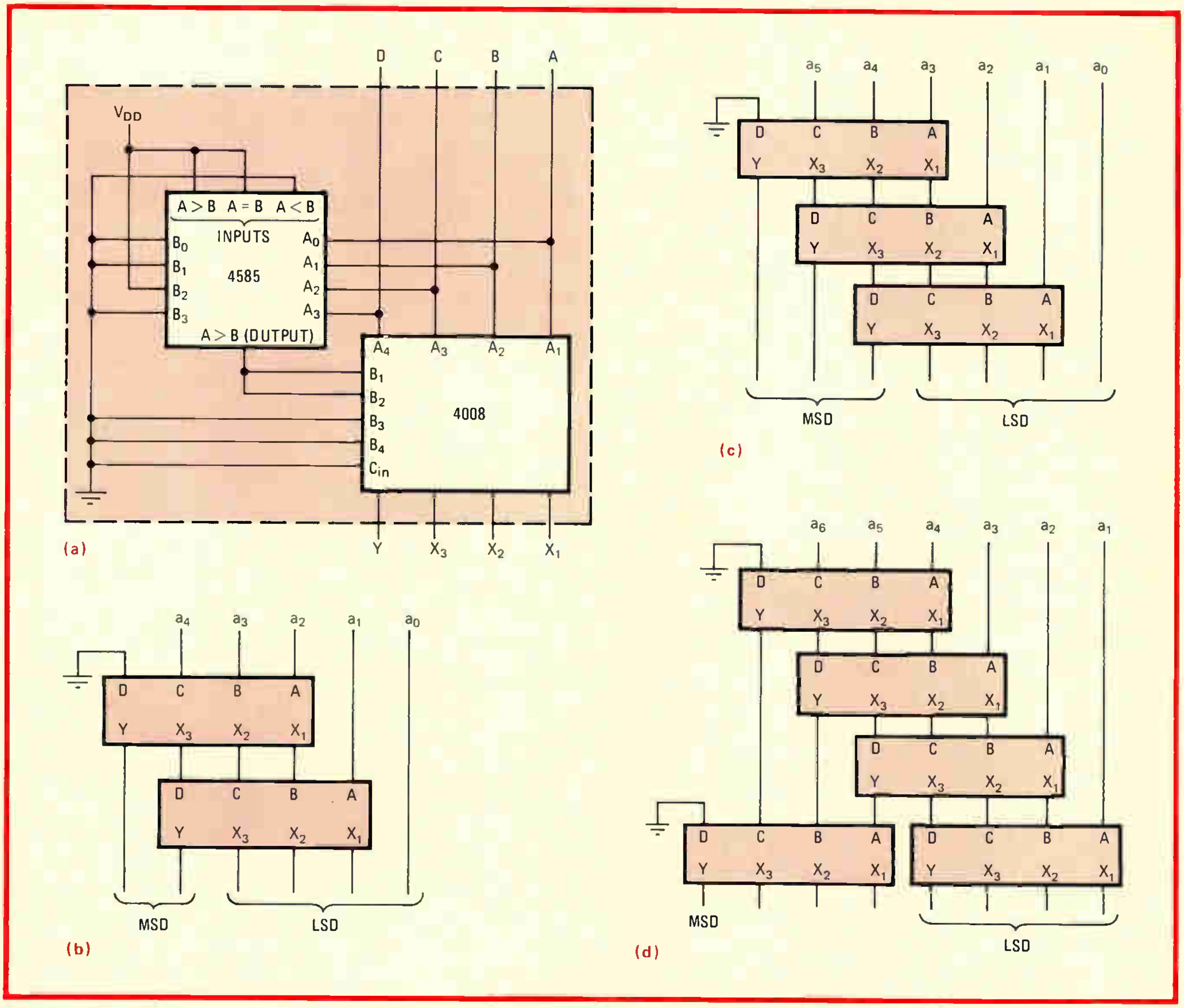
Low-power complementary-metal-oxide-semiconductor adders and comparators are easily combined to form this 4-bit binary-to-BCD converter. When the basic adder-comparator blocks are cascaded, the converter can be expanded to turn n binary input bits into a binary-coded-decimal output. The circuit is simpler than one using counters, and read-only memories are eliminated.

Comprising the basic 4-bit converter block (a) are the 4008 full adder and the 4585 comparator. The binary inputs are introduced at A–C, with A being the next to least significant bit, and D grounded. The BCD output appears at X_1–X_3 and Y of the 4008. The LSB input bypasses the unit and becomes the LSB output.

The 4585 compares the input bits to a binary number (0100) which is hard-wired to pins B_0–B_3. Thus the output of the 4585 is low if the number at A–D is less or equal to 4. The X_1–X_3 outputs of the 4008 are then identical to the input bits.

If the input number becomes greater than 4 (that is, greater than 0100), the 4585's output moves high, and so binary number 0011 is placed on the B_1 and B_2 inputs of the 4008 adder. Thus, 3 is added to the input number and the Y output of the 4008 goes high, indicating the most significant digit is active.

By cascading units, 5-bit (b), 6-bit (c) and 7-bit (d) converters can be built. The method can be used to extend indefinitely the number of bits processed. Note that the value of the least significant input bit (a_0) is numerically equal to its BCD-equivalent and so passes straight from input to output in all cases. □



Add infinitum. Low-power binary-to-BCD converter (a) requires only C-MOS adder and comparator for processing 4 bits. Unit is so configured that basic building blocks can be easily combined to form 5-bit (b), 6-bit (c), and 7-bit (d) converters.

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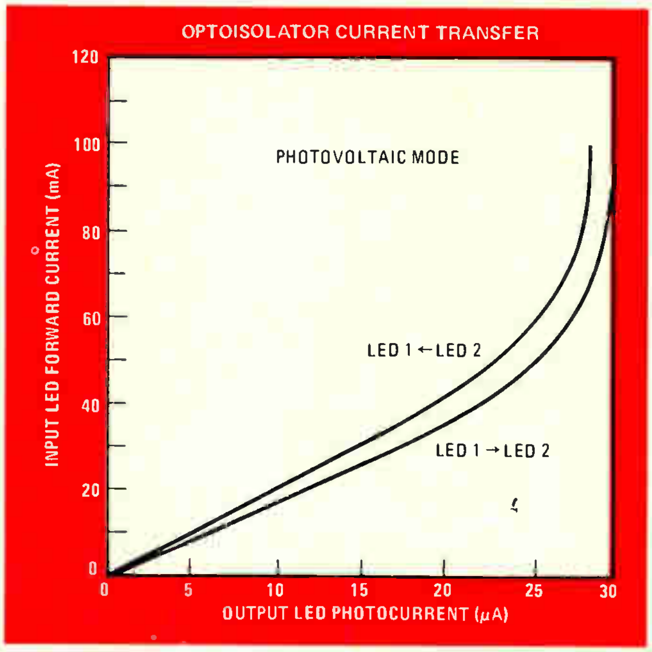
Circle 126 on reader service card

Bidirectional optoisolator puts two LEDs nose to nose

by Forrest M. Mims III
San Marcos, Texas



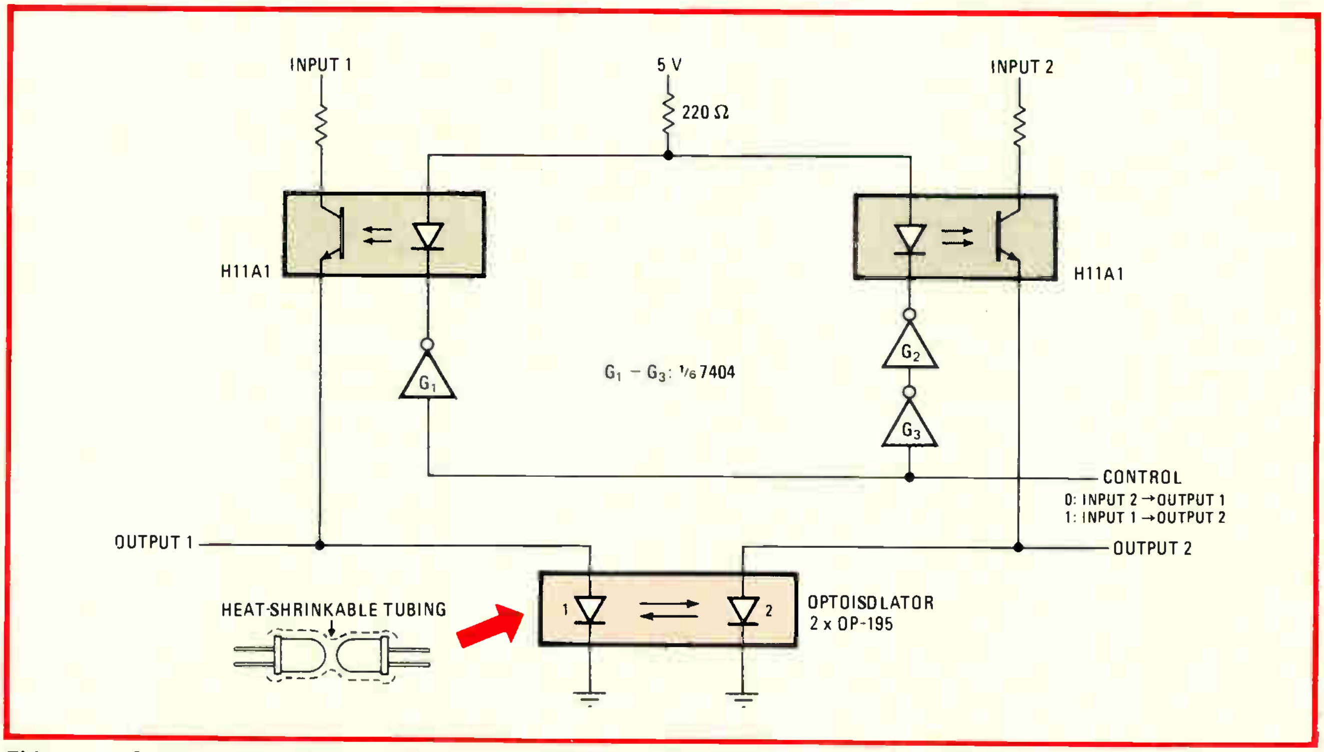
As conventional optoisolators employ a separate source and sensor, they can transfer current in only one direction. A few photodetectors and electroluminescent diodes can double as both a source and sensor, however, and when they are suitably connected they offer users a convenient way to build a low-cost bidirectional optoisolator, as shown here.

Two OP-195 LEDs, which have gallium-arsenide-silicon infrared emitters, can be made to transfer signals in either direction if they are placed nose to nose in a short length of heat-shrinkable tubing and secured in place by heating the tubing. Alternatively, the LEDs may be quite far apart if they are coupled by a plastic or glass-fiber waveguide.

In either case, the current transfer ratio (I_o/I_{in}) for the pair, with proper biasing, will be 0.06% for an input current of 20 milliamperes. This ratio is far too low for many applications but is good enough for some specialized roles where a bidirectional path is required. In any case, the output signal can be amplified or buffered, as necessary.

A logic-control voltage and two H11A1 optoisolators serve as the input/output port selector. Whichever of the OP-195 devices is designated the output diode may be connected in the reverse-biased photo-conductive mode or the unbiased photovoltaic mode. In the latter case, the output device is not biased. The response of the optocoupler operating in this mode for a given signal-input current is shown in the plot. Note the device linearity is completely adequate for duplex voice communication.

The photovoltaic current transfer ratio is virtually identical to that for photoconductive operation up to an input current of 20 milliamperes. The ratios begin to depart considerably above 40 mA. □



Either way. Standard light-emitting diodes encased in heat-shrink tubing can be made to function as a bidirectional transmission link. Alternatively, LEDs may be coupled through optical fibers. Control circuit for selecting input/output port arrangement is simple, using two optoisolators and three inverters. Circuit's current-transfer ratio suffices for many small-signal applications.

Electrically erasable memory behaves like a fast, nonvolatile RAM

It takes a processor only 300 nanoseconds to trigger a data modification in a 1,024-bit alterable read-only memory

by Chris Wallace, *SGS-ATES Componenti Elettronici SpA, Milan, Italy*

☐ In speed and size, semiconductor memories have kept pace with today's powerful microprocessors, so that both are finding their way into an ever-widening range of applications. From the system designer's viewpoint, however, the ideal semiconductor memory would be both flexible and easy to design with, as well as fast. But till now every device has had to sacrifice one of these characteristics to the exigencies of the other two.

The exception is the M 120, a 1,024-bit part that is the first of a new breed of memory chips descended from electrically erasable programmable read-only memories, or EE-PROMS. (EE-PROMS are also known as electrically alterable ROMs, or EAROMs.)

Like earlier EE-PROMS, the M 120 is flexible and simple to use, being a nonvolatile memory that can be reprogrammed by electrical signals while in place in a system. But unlike the others, the M 120 looks to a processor like a fast, nonvolatile, random-access memory. Whereas a processor typically takes 22 milliseconds to modify the data in other EE-PROMS, it need spend only 300 nanoseconds or one machine cycle on starting the data modification in the M 120. That period of time is much more in keeping with the 150-to-300-ns processor cycle times of bus-oriented mainframe systems.

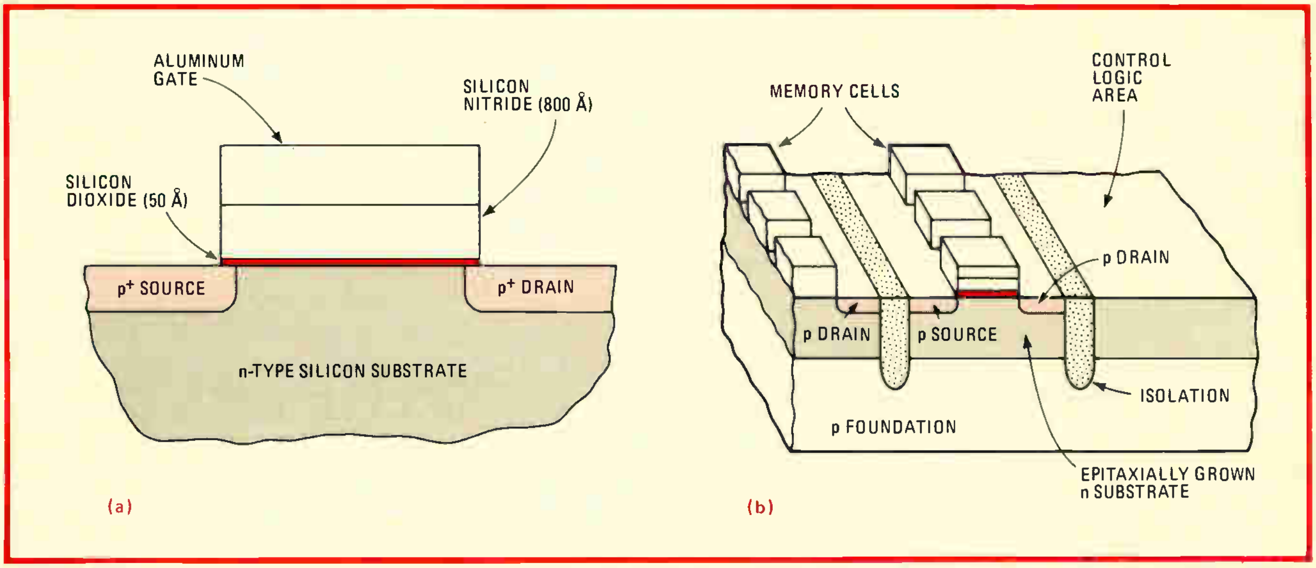
The M 120 has other advantages, too. It can be erased with a relatively low, single-polarity voltage, whereas many others can only be erased with potentially damaging large voltages. It is also bit-alterable, whereas currently available large-capacity EE-PROMS are only erasable in bulk or at best by the word.

The other semiconductor memory types available are also fast but lack either flexibility or design simplicity. By way of proof:

- Random-access memories (RAMs) have data that can be changed quickly and easily but require a dedicated backup power supply to preserve their volatile contents when power is removed from the system.
- Read-only memories (ROMs) and programmable ROMs are nonvolatile, but their contents cannot be changed once they are mask-programmed.
- Erasable PROMS (E-PROMS) are nonvolatile and alterable, but require removal from the system for reprogramming by ultraviolet light.

A change in process

The reason the M 120 is so much faster than its predecessors lies in its processing technology, which integrates fast, intelligent peripheral circuits with the memo-



1. Layered. Typical MNOS memory cell requires opposite-polarity gate voltages to write and erase data; thinness of oxide layer complicates fabrication (a). To protect the sensitive control logic from the high cell voltages, MNOS EE-PROMs require intervening epitaxial layers (b).

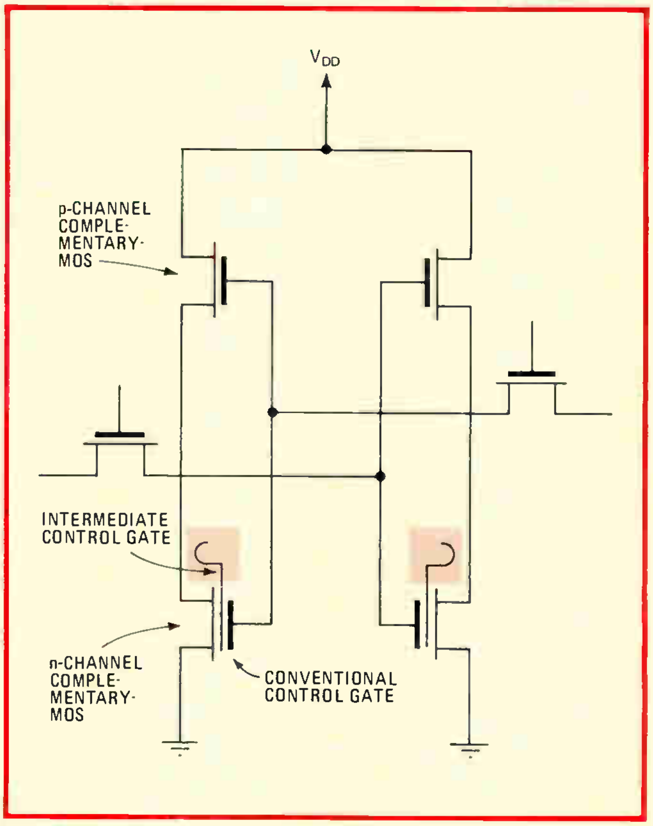
ry array. Earlier EE-PROMs employed either a double-dielectric, or metal-nitride-oxide-semiconductor (MNOS), process or a stacked polysilicon-gate approach. The M 120 uses an improved version of the latter.

MNOS devices rely on electrons' ability to cross a thin oxide barrier if given enough energy. In a typical MNOS memory cell (Fig. 1a), if a high enough voltage (25 to 30 volts) is applied to the gate, electrons in the substrate tunnel through the silicon-dioxide to its interface with the silicon-nitride layer. Since both layers are good insulators, the electrons remain trapped there for a very long time—as long as 10 years. To erase the cell, an equally high negative voltage is applied to the gate to drive the electrons back into the substrate.

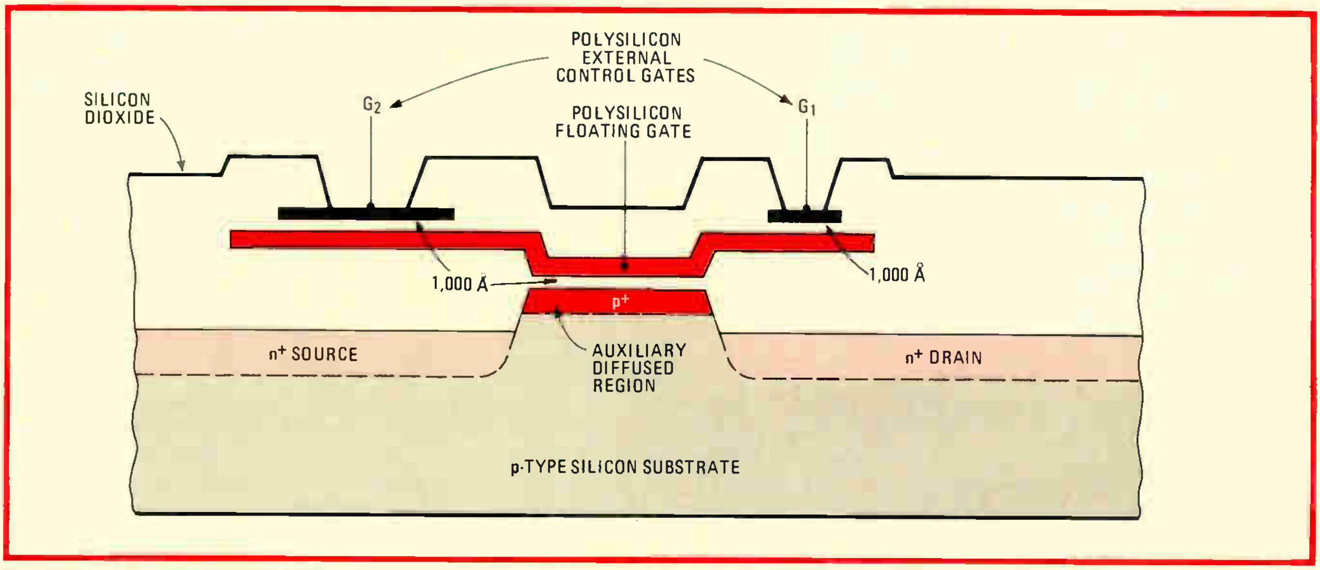
Two problems, in addition to production of a 50-angstrom oxide layer, plague MNOS memories. One is the tendency for electrons to recross the silicon-dioxide layer and cause a loss of data. The other relates to the need to reverse the polarity of the cell's gate-substrate voltage to erase it. Since the sensitive memory control logic is on the same substrate, several manufacturers have used an epitaxial construction like that shown in Fig. 1b to isolate the logic from the cells. While this arrangement helps prevent damage, the epitaxial layer and substrate constitute a high-leakage-current diode during erasure, which makes it necessary to use off-chip drivers with voltages as high as 40 V.

Compounding both problems is the time required for the complex modification sequence, which consists of applying the erase voltage, a delay, termination of erasure, applying the write voltage, another delay, and a final termination. Should either termination be omitted, the memory would be destroyed.

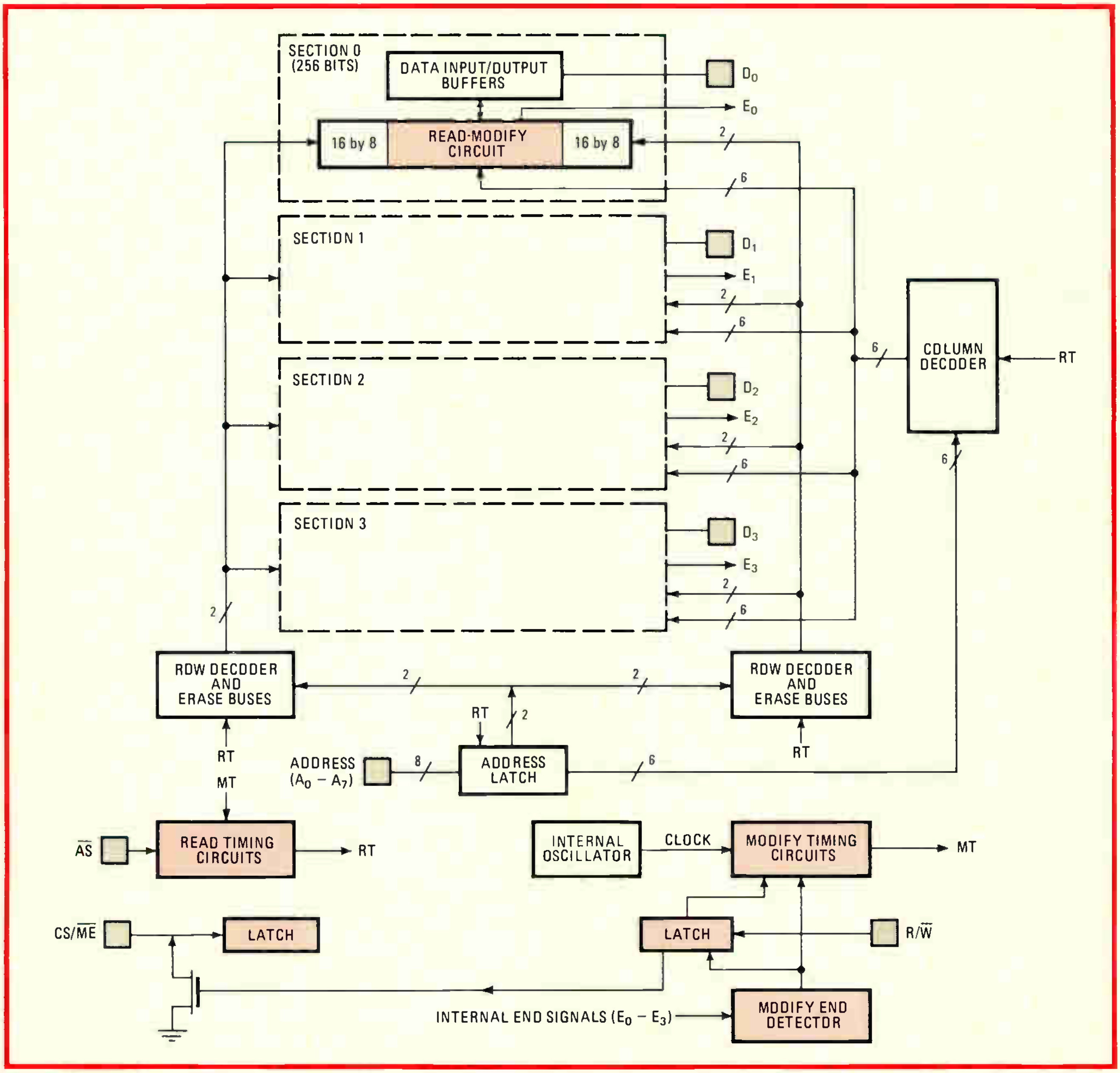
The second class of EE-PROMs is the polysilicon-gate type shown in Fig. 2. The cell configuration is that of a standard flip-flop, but the bottom two transistors have two control gates. At low supply voltages, this cell is volatile. But if V_{DD} is raised to a high level to "firm" the data, electrons on the conventional control gate with a positive potential migrate to the intermediate control gate and remain there when power is switched off. When power is reapplied, the difference in charge between the two intermediate gates toggles the flip-flop, reversing the cell's state predictably. That effect is conventionally overcome by large-scale integration of exclusive-OR logic on the chip, which complicates production. Another drawback to the use of polysilicon-gate parts as nonvola-



2. Extra gates. This flip-flop represents a typical polysilicon-gate EE-PROM cell. At low voltages, the cell is volatile. But raising V_{DD} to 20 V transfers charge from the drain to the intermediate control gate of the lower on-transistor, where it stays for up to 100 years.



3. Floating. In the M 120, application of 20 V to G_1 and G_2 raises the potential of the floating gate, which then attracts and traps electrons flowing between the source and drain. Note thickness of oxide layer, which makes it easy to manufacture.



4. Intelligent approach. Block diagram of M 120 electrically erasable PROM shows memory organization and relationships to the on-chip control circuits. Function of internal logic is to compare each stored bit to incoming bit before changing cell content, if necessary.

tile memories is the need to detect voltage failures via complex integrated circuitry.

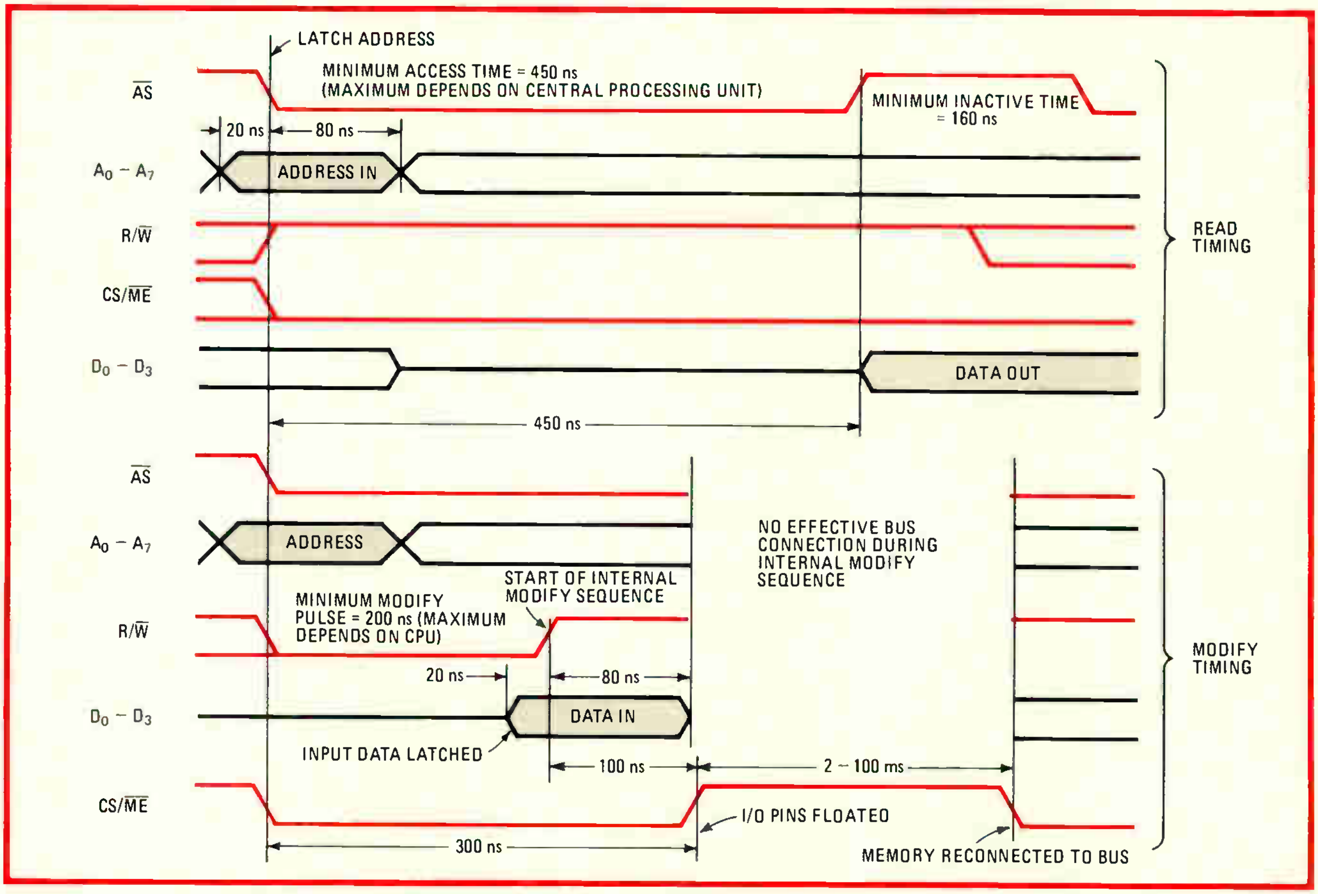
The M 120 solves the preceding problems—the need for very thin oxide layers in MNOS devices and for extra logic in stacked-gate parts—by adding an extra gate to the latter approach.

Adding a gate

Figure 3 shows the cell construction: two control gates G_1 and G_2, a floating gate, and a thick (greater than 1,000 angstroms) layer of silicon dioxide on a conventional n-channel transistor with an auxiliary p^-diffused region. Area of the cell is 3 by 2 mils, line width is 6 micrometers, and overall chip area is 216 by 131 mils.

To write data into the cell, 25 V is applied to both G_1 and G_2 with 15 V between the source and drain. With conduction between the source and drain, the high potential induced on the floating gate attracts electrons to it across the oxide layer. Once the electrons reach the floating gate, they are trapped in a deep potential well, where they can stay for as long as 100 years. To erase the cell, G_2 is grounded when G_1 is pulsed with a positive voltage, which creates an electric field that is of sufficient intensity to drive the electrons across the oxide layer to G_1.

Like other EE-PROMs, the M 120 has disadvantages. First, as the oxide layer between G_1 and G_2 captures ever more electrons with use, erasure time becomes longer, deteriorating to 100 milliseconds after 10,000 cycles. And since the transfer mechanism is a secondary effect, writing is slow compared with processor cycle times, even for new parts.



5. Otherwise engaged. Timing sequence for readout is conventional, yielding access time of 450 ns. Modification is a two-part procedure: 300 ns to latch the input word, followed by internal sequence of indeterminate length while the memory is off the bus.

But since EE-PROMs are normally used where data is changed only occasionally, rather than during every cycle, a solution to the modify-time dilemma is a design that allows a processor to present data to the memory when a change is required, and then remove the memory from the bus. The processor then can occupy itself elsewhere, while the memory completes the modification internally. The M 120 incorporates this feature in an on-chip intelligent modify system.

Figure 4 is a block diagram of the chip. It is arranged in four 256-bit sections, each of which is further divided into two 16-by-8-bit parts. Each section has a dedicated read-modify circuit and input/output buffers. Common to all sections are address and control latches, row and column decoders, and timing and control circuitry.

Read, modify

To read a 4-bit word from memory (Fig. 5, top), the processor applies the 8-bit address to address pins A_0–A_7 while keeping the read-write pin $R/\overline{W}$ high and the chip-select pin $\overline{CS}$ low. At the negative transition of the address-select pin $\overline{AS}$, the read timing circuits generate the RT signal, which latches the address and applies it to the row and column decoders. After 450 ns, the stored word appears at pins D_0–D_3. Total power consumption for a read cycle is 300 milliwatts.

During a modify sequence (Fig. 5, bottom), D_0–D_3 become input pins. Again, but now with $R/\overline{W}$ low, the negative transition of $\overline{AS}$ latches the address, but the input data is not applied to the internal latches until $R/\overline{W}$ goes high not less than 200 ns later. At this time, the internal modify sequence begins; 100 ns later, the memory removes itself from the bus by floating its I/O pins and holding the $CS/\overline{ME}$ pin low.

The modify sequence starts with a comparison of each bit in the new word with its stored counterpart. On the basis of this comparison, each section's modify circuit decides whether to write (write a 1), erase (write a 0), or do nothing (if the bits are equal). Those decisions are made during an initial 15-μs pulse. Longer pulses, to a maximum of 200 μs, and comparisons follow until each bit is modified. As each stored bit compares favorably with its corresponding input, that section's modify circuit raises an end signal (E_0–E_3) that goes to the chip's modify end detector. When all four end signals are high, the detector resets the internal read/write latch and floats the $CS/\overline{ME}$ pin, signifying that the memory is again ready to be read or written into. In this way, no cell is ever written into or erased unnecessarily. Power consumption for modification is a mere 400 mW.

Applications

Possible applications for the M 120 include storage of infrequently changed data like dimensions or production sequences in industrial control systems. SGS-ATES is at present working on a 4,096-bit part, and producing an integrated circuit that combines 272 bits of this type of memory with automatic tuning circuits for a TV set. □

Zero-insertion-force connector ousts conventional backplane

Structural connector opens up new packaging configurations like side entry and tandem stacking

by James Taylor, *AMP Inc., Harrisburg, Pa.*

□ Selecting a cost-effective and reliable package for microprocessor systems has become as vital as choosing the right microprocessor. With the change in circuit topologies brought about by the bus-structured microprocessors and the arrival of the zero-insertion-force (ZIF) connector, engineers are turning to some novel packaging schemes that have been able to dispense with the conventional backplane.

Composed of a motherboard with an array of printed-circuit connectors to receive the daughterboards, the backplane is still the predominant circuit-packaging structure today and is common to both digital and telecommunication systems. But traditional backplanes are increasingly unsuitable for several reasons:

- Microprocessor architecture, based on 40-pin-or-over integrated circuits, is driving the number of contacts required by the daughterboard to 100 or more.
- Backplane cooling problems have been aggravated by dense concentrations of large-scale integrated circuits that increase the amount of power that has to be dissipated per backplane.
- Gold contact systems, so prevalent in backplane architecture, have become prohibitively expensive.

The most significant component in every backplane system is the interconnection of backplane and daughterboards. This function has been performed most frequently by what are known as cantilever-beam, card-edge connectors, which have significant limitations.

Big-board problems

One drawback is that when the printed-circuit-board span approaches 17 inches along the board and connector interface, warping is likely. If a long board bows, it causes the contacts to deflect abnormally and they may take on a permanent set. Then, if the warped board is replaced by one that is not bowed, or is bowed in the opposite direction, some of the abnormally deflected contacts may fail to contact the fingers on the card.

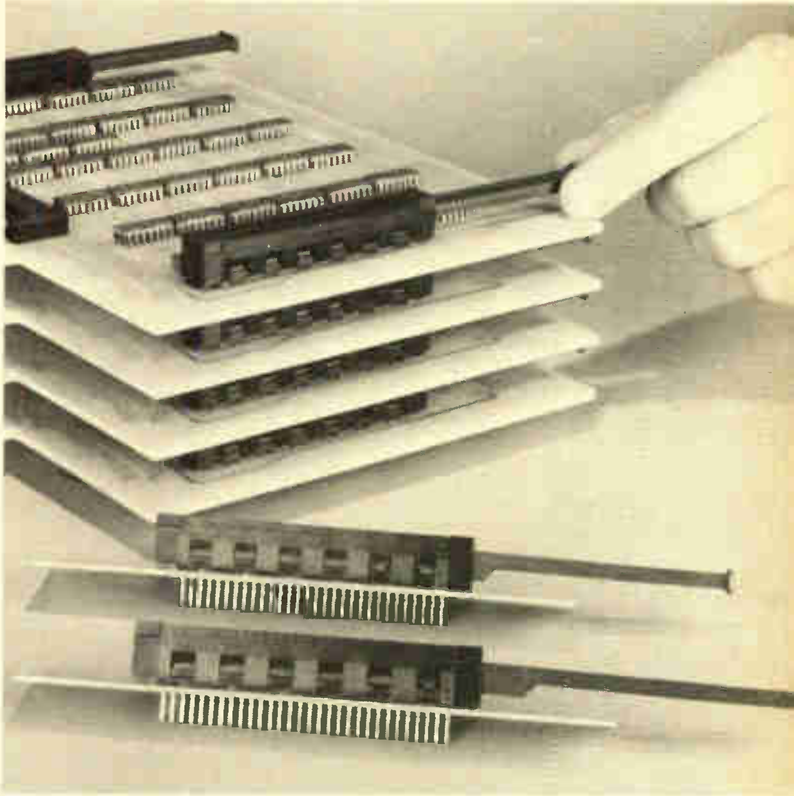
For example, when the number of contacts required at the interface between daughterboard and motherboard approaches 50, the performance of a conventional card-edge connector becomes marginal because of the physical length of the converter and the large insertion and withdrawal force required. This force is a linear function of the number of contacts. If each contact-pair (pin and socket) requires 1 pound of force to mate or unmate, then an interface that contains more than 50 contacts becomes generally impractical.

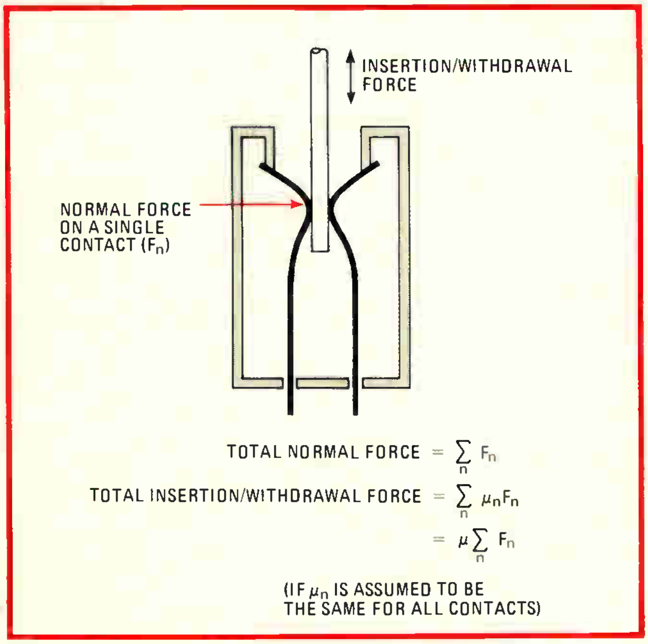
One solution seems to lie in reducing the contact force. But, ironically, designers want to raise contact force so that they can replace gold-to-gold contact interfaces with far less costly non-noble tin and tin-alloy systems.

Thus the challenge is to lower the insertion/withdrawal force while raising the contact force. Fortunately, there is an answer to this dilemma in the recently introduced zero-insertion-force (ZIF) connector.

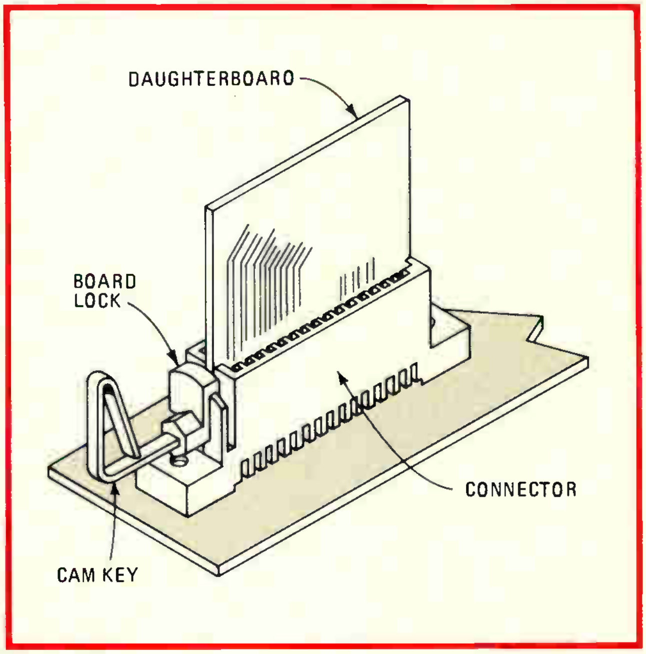
The term "zero insertion force" identifies a family of connectors in which the force of insertion or removal of the mating part is essentially zero (see "Getting

Stacking. Configuring daughterboards with stacking ZIF connectors eliminates the backplane and card cage entirely. This packaging architecture lends itself to large printed-circuit boards. Interfacing with flexible cable connectors is possible in this method.

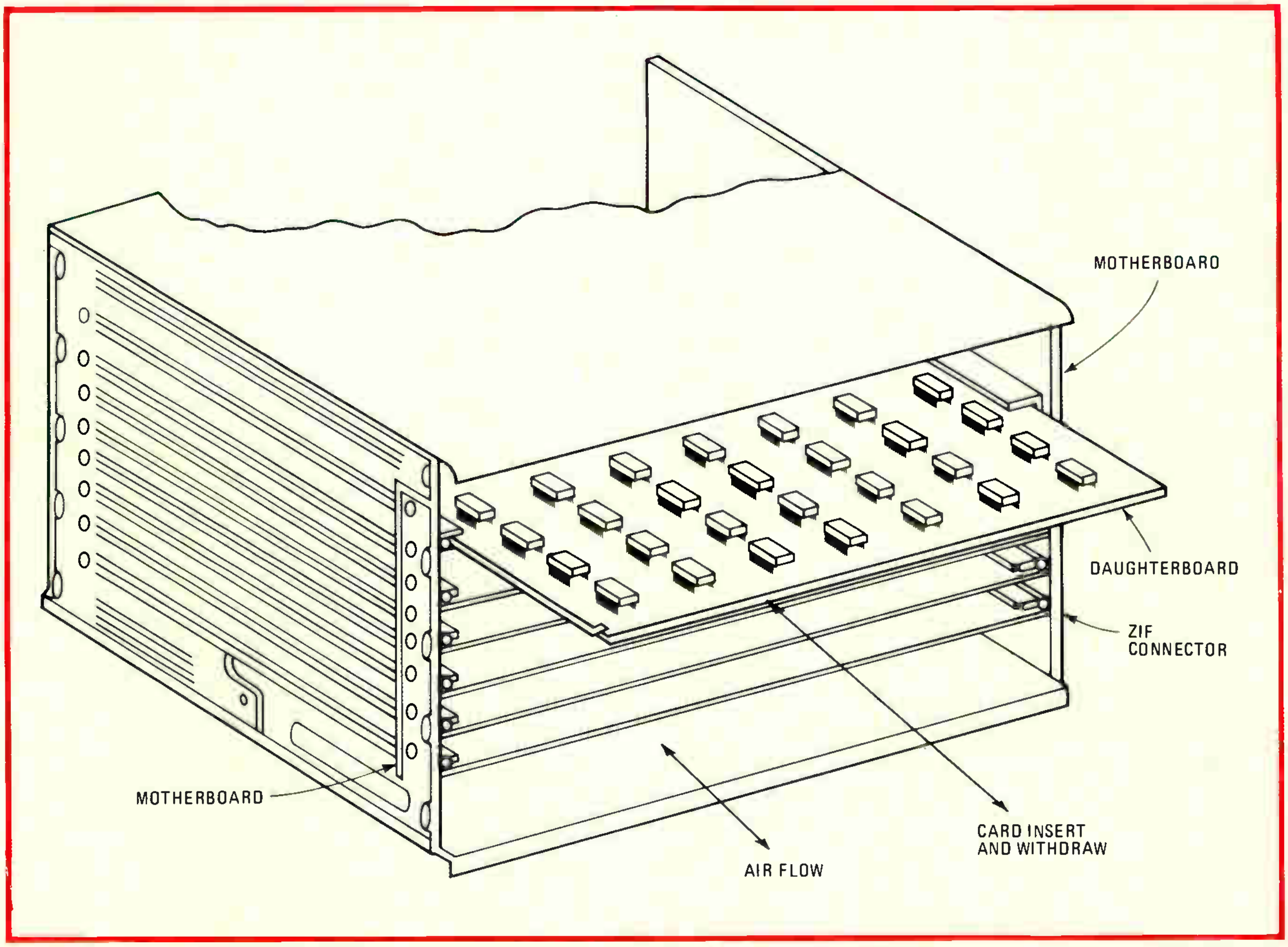




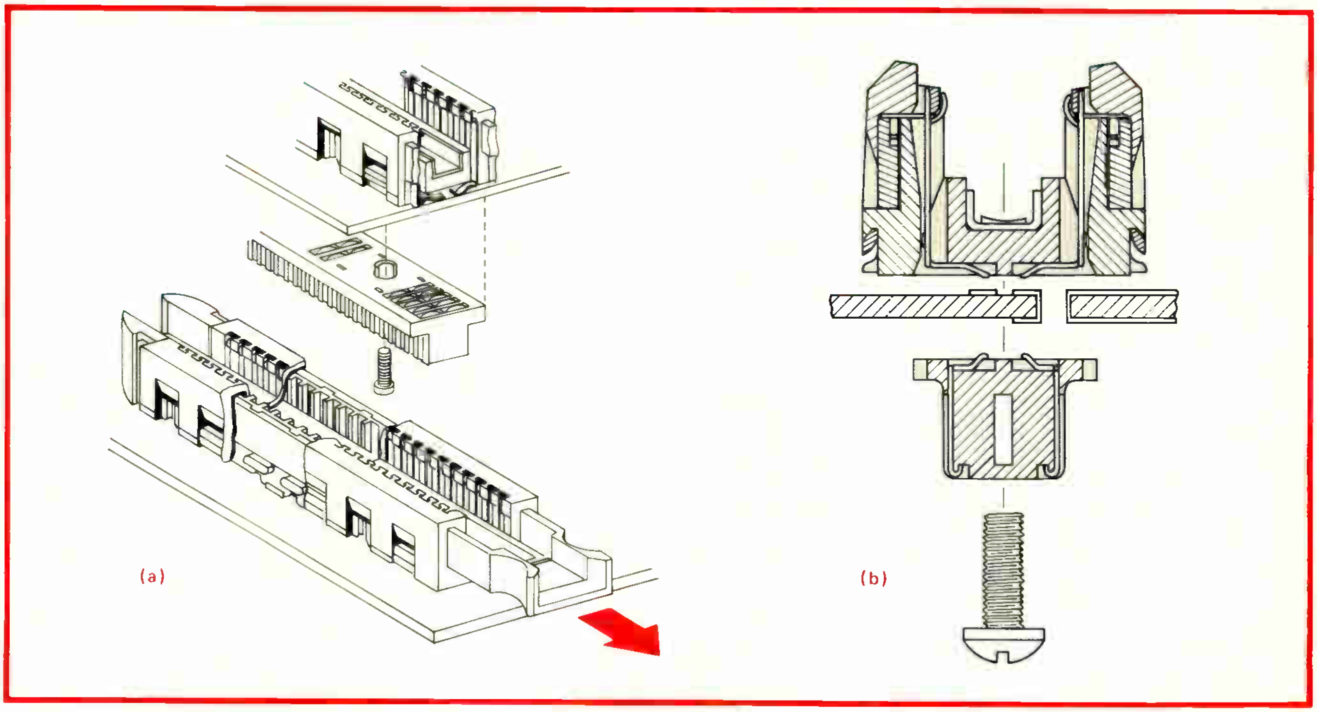
1. Sliding friction. In a card-edge connector, insertion or withdrawal force is due to the friction encountered as the circuit board enters or leaves the connector. The insertion-withdrawal axis is at right angles to the axis of force at each contact interface.



3. Key-operated. Rotating cam key on this ZIF connector counterclockwise opens contacts and board lock at near end. This enables easy withdrawal of the daughterboard. The key can be made removable to prevent tampering by unauthorized personnel.



2. Side entry. By using zero-insertion-force connectors, the designer can configure two backplanes with each, so that they perform both interconnection and structural support roles. This type of packaging is well-suited to bus-oriented circuitry.



4. Surface mount. Another version of tandem stacking uses surface-mounting ZIF connectors that require no soldering, shown in (a). In (b), protruding tabs contact the pc board. Male and female portions are bolted together, forcing the tabs against the pc traces.

acquainted with ZIF" on p. 136). The most common mating part is a printed-circuit board, which usually plugs into a card-edge connector.

When the board is inserted, each contact deflects and develops a force at the contact interface that depends on the amount of deflection. The force at each contact interface must be sufficient to ensure a reliable electrical interconnection.

What results from insertion or removal of a daughterboard is not the sum of these forces ($\sum_n F_n$ in Fig. 1), but the sum of the frictional forces that develop from the normal forces ($\mu \sum_n F_n$). The reason is simply that the insertion/withdrawal axis is at right angles to the axis of force developed at each contact interface.

This insertion/withdrawal force serves a second vital role. It acts to retain the board, keeping it securely seated in the connector.

The ZIF two-step

With a ZIF connector, insertion becomes a two-step process. First, the circuit board is mated, and since no force is required, it is seated effortlessly. Second, the engagement is performed mechanically. This may take the form of pushing a lever or rotating a shaft to engage the contacts. Removal is performed in the reverse order.

A major advantage of ZIF is that there is no limit to the number of contacts because insertion force is zero regardless of how many there are. These connectors can be finger-actuated (engaged or disengaged) for up to 120 contact pairs, or lever or bell-crank operated for up to 280 contact pairs. Equally important, ZIF connectors allow the designer to try out desirable packaging alternatives to the backplane configuration.

One such alternative is side-entry packaging, which eliminates the card guides common with traditional backplanes. With card guides, as with card-edge connectors, insertion and withdrawal forces develop because the daughterboard must fit snugly in the guides to stay securely in place.

The alternative configuration is shown in Fig. 2. Two ZIF connectors support each daughterboard, performing both structural and interface roles, one along each side. Moving the daughterboard interface from the rear to the sides of the board doubles the interconnection capacity. A natural circuit isolation also occurs because of the dual daughterboard structure. For example, signals and power buses can be distributed on alternate sides, or a designer might run certain signals and power along one side and confine other sensitive signals to the opposite.

A second advantage of this approach is that a clear air flow is created from front to rear. Hence an air plenum can easily be affixed to the rear to move the air in a laminar motion across the board surfaces.

ZIF connectors used in side-entry packaging can very easily provide 175 dual positions (350 contacts) with contacts on 0.100-inch centers. The connector housing is sufficiently narrow to allow adjoining circuit boards on centers as close as 0.6 in.

Key rotation

One manner of actuating a ZIF connector is shown in Fig. 3. Rotating the key causes all contacts to move approximately 0.030 in. along axes perpendicular to the daughterboard. The objective is to open each contact pair beyond the maximum board thickness, thereby ensuring that no force is encountered and no contact abrasion occurs during insertion/withdrawal cycles.

Variations of the cam-actuated connector, shown in Fig. 3, are available with a variety of actuating levers, rods, or a hex-shaped cam key. The cam key, which is

Getting acquainted with ZIF

The basic distinction between the traditional cantilever-beam, card-edge connector and the zero-insertion-force connector is shown in (a). With the cantilever-beam card-edge connector, the printed-circuit board itself deflects the beam contacts upon entrance. The insertion force it encounters upon entering is a result of the combined frictional and normal insertion force developed by the deflected contacts.

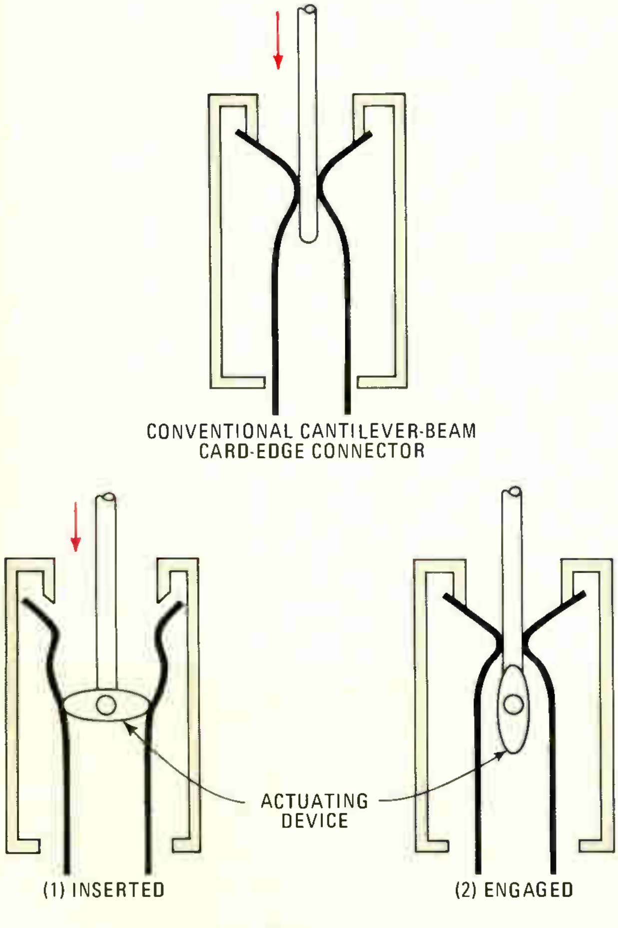
With the ZIF connector, the board is inserted into the connector housing, and because the contacts are held open (deflected) by an actuating device, it encounters no resistance and sets itself in the bottom of the connector body. Once the board is seated, the actuator (in this case, a rotary cam) is rotated 90°, allowing the contacts to engage the mating surfaces on the circuit-board fingers.

ZIF connectors can be configured in many ways. The objective is always to eliminate insertion/withdrawal force and at the same time to establish a sufficient normal force at each contact once the mating printed-circuit card or connector is put in place.

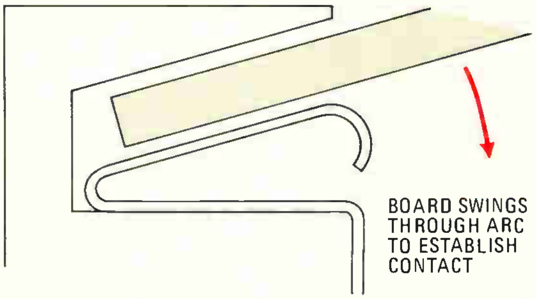
Shown in Fig. 3 on page 134 is a rotary, cam-actuated ZIF connector that may be operated by a key or a conventional nut driver. It is available with up to 65 dual positions (130 contacts) on 0.100-by-0.200-inch, 0.125-by-0.250-in., or 0.156-by-0.200-in. centers. Both sequential and nonsequential versions are manufactured.

A second type of ZIF connector, termed board-actuated, is shown in (b) and (c). In both cases, the board actuates the contact engagement. Not shown in either figure are latches or other devices to keep the board firmly mated with the contacts.

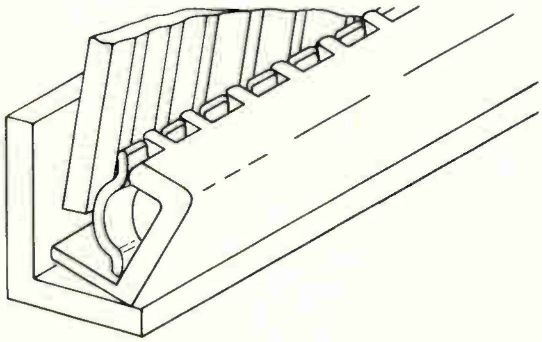
The sliding-ramp connector shown in (d) is yet another ZIF design, with a sliding bar configured as a sawtoothlike series of inclined ramps to engage and deflect the



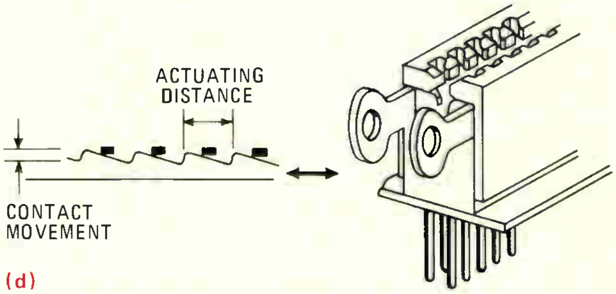
(a)



(b)



(c)



(d)

shown in Fig. 3, can be made removable, in order to prevent unauthorized personnel from removing printed-circuit boards.

A further advantage of side-entry architecture is that it enables a packaging designer to think in terms of sequentially operated ZIF connectors. For instance, sequential versions of the rotary, cam-action ZIF connector, shown in Fig. 3, execute a "2-4-remainder" contact sequence upon closing. This means that when the cam handle is actuated, first two, then four, and then the remaining contacts mate with the fingers on the board. Upon opening, the sequence is reversed. An appropriate circuit assignment would connect ground to the first two contacts, power to the next four, and signals and miscel-

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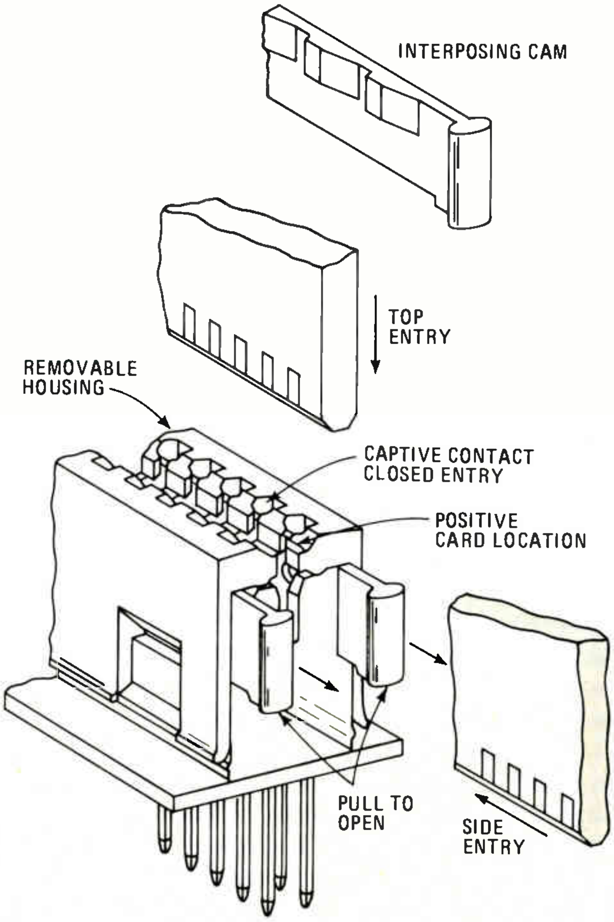
contacts. With contacts on 0.100-in. centers, though, the ramps cannot exceed that length. Thus a steep pitch is needed to develop momentum. This creates several design problems that discourage its use.

However, the interposer technique shown in (e) is a refinement of the sliding ramp technique and is satisfactory for gang-deflecting the contacts in a ZIF connector. Using this technique, a 175-position (350-contact) connector is entirely practical, even with contacts on 0.100-in. centers. The cam can generate a 0.030-in. contact movement connector. The role of the interposer is to lift the contacts off the printed-circuit board. Thus the contacts are stressed maximally when the connector is in its open position—a small portion of a connector's useful life. This arrangement contrasts with a card-edge connector where the contact stress is at the maximum with the board securely seated in the connector.



(e) OPEN POSITION

laneous circuits to the remaining contacts.

Though power-sequencing is attractive in many applications, it is particularly valuable in digital and communications systems where it is essential to remove or insert a daughterboard without draining power from the entire system. In these systems, the connectors serve as sequencing switches.

Another advantage of a two-sided backplane geometry is that signal and power routing on the daughterboard are eased. Paths become shorter and fewer dog-legs are necessary in the daughterboard circuit pattern, as the designer has added interfaces along the two opposite edges of the board.

Another alternative to the backplane is illustrated in the photograph on page 133. The outstanding feature of this novel design is the complete absence of any card-cage structure. In this packaging architecture, boards are stacked with a stacking ZIF connector, which mounts on 0.025-in. square posts on a standard 0.100-by-0.100-in. matrix. The posts extend 0.288 in. beyond a 0.0625-in. printed-circuit board. Organization of the buses, if so desired, is developed transverse to the boards through the mating connectors.

Tandem stacking

Stacking-type connectors of the type illustrated have contacts with square, 0.025-in. posts that have been press-fitted into a printed circuit board, like many card-edge connectors and other wrapped-wire post assemblies. The pins are, in addition, completely compatible with a variety of other connectors, including the popular flat-cable connector types.

With tandem stacking, the connectors can be located arbitrarily along the perimeter of the mating boards. In fact, the ZIF connectors need not be confined to the board perimeter so long as actuating levers are accessible for assembly and disassembly.

A further advantage is the ability to add boards when more options are needed, so long as the housing, or envelope, for the overall assembly is ample. The designer simply confines each option to one or more of the stacking circuit boards.

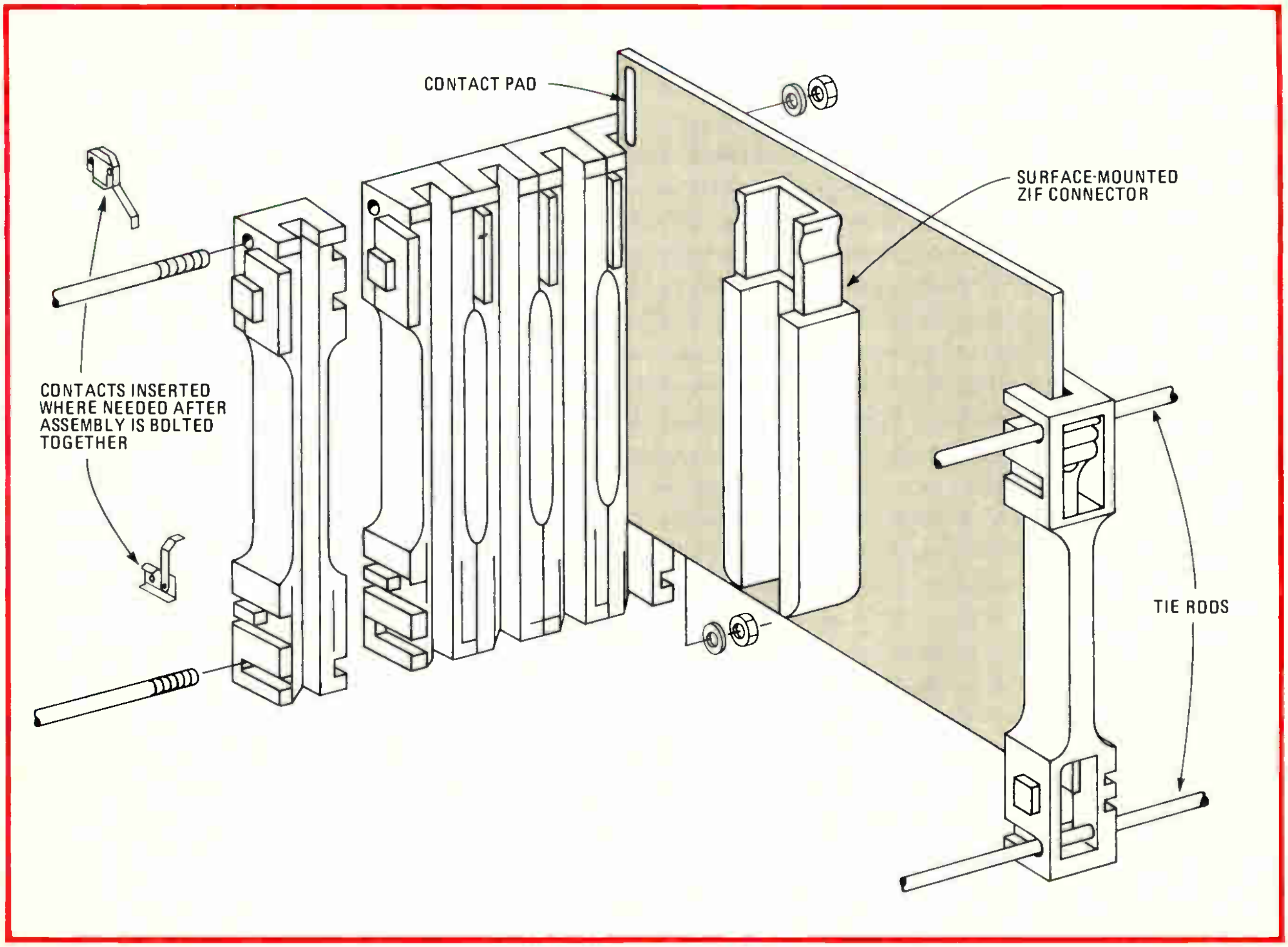
By spanning the connector near the center of the board, tandem stacking lends itself to the configuration of relatively large boards. In this case, the additional stacking connectors are located so as to stiffen an otherwise flimsy structure.

In addition to the ZIF stacking connector, there is a surface-mounted ZIF intercard connector, shown in Fig. 4. In this configuration the male and female portions are bolted to a printed-circuit board so that the spring-loaded, tin-alloy–plated ears of each connector are compressed against corresponding traces on the board. A normal force of 260 grams minimum at each contact will provide a highly reliable interface with tin-lead–plated pads. Stainless-steel support members are contained in each mating connector. By connecting them to a ground plane on the circuit board, a 90-ohm nominal-impedance connector system can be created.

Maintainability is another attractive feature of the tandem-stacking geometry. Once a defect is traced to a single board, the stack can be disassembled and reassembled with the suspected board at the top, giving a technician access to all components on its surface.

The system is bus-interruptible in two ways: first, a connector can be omitted from a series of boards; second, as in the case of the connector shown in Fig. 4b, the 0.25-in. posts can be cut off where desired.

Circuit-board connectors are seldom designed to carry



5. High-current stacking. Power-distribution card guides team with surface-mounted ZIF connectors to build an assembly able to handle both low-level signals and supply currents as high as 50 amperes. The tie rods distribute high currents with a negligible voltage drop.

more than 3 amperes. However, in many circumstances a much larger current is needed to drive a number of power-consuming circuit boards. One way to increase a connector's current-carrying capacity is illustrated in Fig. 5, where card guides (rods) at each end of the circuit board also serve as high-current connectors. The tie rods are each capable of distributing 50 amperes with negligible voltage drop.

Dividing signal and power

The ZIF connector in the middle of the board enables circuits to be interconnected on a card-to-card basis and provides a natural division between signal and power. Contacts can be inserted after assembly of the card guides to provide an electrical interface between the contact pad shown in Fig. 5 and the tie rods. By selecting the positions and lengths of the contact pads, power sequencing can be designed to ensure that a prescribed connecting and disconnecting sequence occurs at each card insertion or withdrawal.

Particularly attractive in the architecture shown in Fig. 5 are the short paths followed by signal and power traces to reach components on the board. The fact that signal traces from any component on each board are routed toward the center surface-mounted ZIF connector, whereas power traces fan out toward the periphery of the board, eases the designer's layout problems by a significant amount.

A crucial consideration in many products with digital circuitry is how to interconnect subsystems successfully via buses. Bus architecture has separate lines for data, addressing, and control, and enables a number of modules to communicate. In the traditional backplane there is virtually no isolation of the data signals. These must interface along the only surface available—the connector interface between daughterboard and motherboard. All the ZIF packaging schemes previously discussed are suitable for data buses, since they provide isolated alternatives to backplane routing.

Packing and bus architecture

In the side-entry geometry of Fig. 2, the bus may be routed along one side while power is distributed along the other. Tandem stacking offers the designer of bus architecture even more flexibility. Here the bus connector can be located virtually anywhere on the surface of the board. Also, in power distribution (Fig. 5), ZIF connectors can be anywhere on the board.

A noteworthy feature of both tandem-stacking and power-distribution techniques is the unusually direct transverse path of the bus. It must be routed to the board's circuitry from the intercard connectors. □

Notch filter and meter measure power-line harmonics

by Henno Normet
Diversified Electronics Inc., Leesburg, Fla.

Valid measurements of core loss in power-line transformers and various other magnetic devices require total harmonic distortion (THD) levels under specified limits—usually 3%. This inexpensive circuit determines the THD present in a 60-hertz waveform, over the range of 0 to 10%. Here, a notch filter is used to eliminate the voltage source's 60-Hz fundamental component, allowing an ac voltmeter to measure the remaining harmonic components.

The adjustable-Q Wien-bridge notch filter discussed in a previous article[1] proved to be best adapted for this application. Resistors R_{11} and R_{12} of the bridge (see shaded portion of figure) are selected to give the notch filter a Q of 10. The resulting null is sharp enough to pass a 180-Hz signal without attenuation, the lowest harmonic to appear as a component of distortion.

Component selection for the rest of the filter is also important to the achievement of good notch depth. C_1 and C_2 should be matched within 1%, and high-accuracy resistors used where indicated by asterisks. Metal-film resistors and polycarbonate capacitors help keep frequency drift and aging to a minimum.

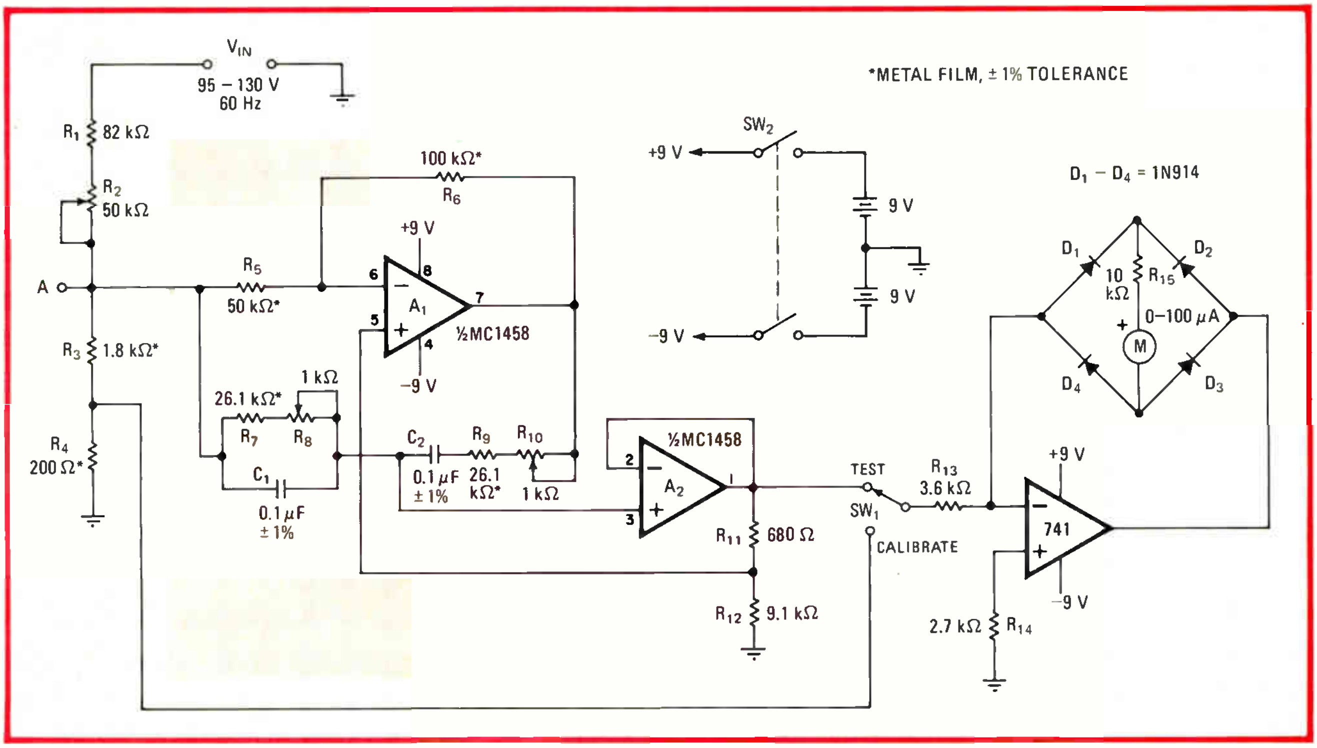
For initial balancing of the bridge, a low-distortion 2-V signal at 60 Hz is applied at point A. With SW_1 in the test position, R_8 and R_{10} are adjusted for a zero reading on the meter, M. If an audio oscillator is not available as a signal source, full line voltage may be applied to the input terminals, in which case R_8 and R_{10} are adjusted for a minimum reading on the meter.

In operation, SW_1 is first placed in the calibrate position and line voltage applied at the circuit input, V_{in}. R_2 is then adjusted for a maximum (full-scale) reading.

The switch is then placed in the test position, whereupon the input signal passes through the notch filter. Percent of THD may then be read directly. Note that the accuracy of the reading depends upon the accuracy of the 10:1 voltage divider, R_3 and R_4.

The definition of THD requires that both the calibration and measurement procedure be carried out with a root-mean-square-responding meter. However, in the 0–10% distortion range, a less costly average-responding meter will provide 10% accuracy, which is acceptable in most applications. □

References
1. "Wien bridge and op amp select notch filter's bandwidth", *Electronics*, Dec. 7, 1978, p. 124.



Handling harmonics. Wien-bridge notch filter rejects 60-Hz power-line fundamental frequency so that total harmonic distortion present in signal can be measured. Meter measures THD over 0-to-10% range. An rms-responding meter should be used, but an average-responding meter is acceptable. Results are displayed in percent, with an accuracy directly proportional to the tolerance of resistors in divider R_3–R_4.

Resistor snipping trims regulator voltage to within 1%

by Robert A. Pease
National Semiconductor Corp., Santa Clara, Calif.

Five low-cost resistors are used in this production-line technique for setting the output voltage of a three-terminal regulator to within ±1% of the desired output voltage. Thus, expensive and often unreliable potentiometers can be eliminated by this iterative trimming procedure, which removes up to three resistors until the output voltage is within tolerance.

In a typical three-terminal adjustable regulator such as the LM117 (a), the output voltage will be:

$$V_{out} = V_{REF}(R_2/R_1 + 1) + R_2 I_{ADJ}$$

where V_{REF} is nominally 1.25 volts, R_1 and R_2 are the regulator's external voltage-programming resistors, and I_{ADJ} is 100 microamperes maximum. Generally, V_{REF} will vary less than ±3% under normal operating conditions; if R_1 and R_2 each have a tolerance of ±1%, the regulator's overall accuracy then becomes ±5%.

The standard method for attaining a 1% tolerance is to substitute a trimming potentiometer, R_T, and some fixed resistor, R_F, for R_2, where in general $R_{Tmax} + R_F$ will exceed the value of R_2 previously used by a factor of 10% or so. But this scheme may be superceded with the circuit shown in (b) to avoid the disadvantages of using a trimming potentiometer, one of which is a tendency to misadjust it sooner or later.

In this particular case, a 22-V output voltage is sought for a 28-V source input. When first measured, V_{out} will be 4% to 6% higher than the 22V target no matter what conditions exist within the regulator, because the effective value of R_1 is lowered (see equation). R_3, R_4, and R_5 are selected so that one or more may be systematically removed to bring V_{out} within limits.

The method is as follows:

- If $V_{out} \geq 23.08$, cut out R_3.
- If V_{out} is or then becomes ≥ 22.47, cut out R_4.
- If V_{out} becomes ≥ 22.16, cut out R_5.

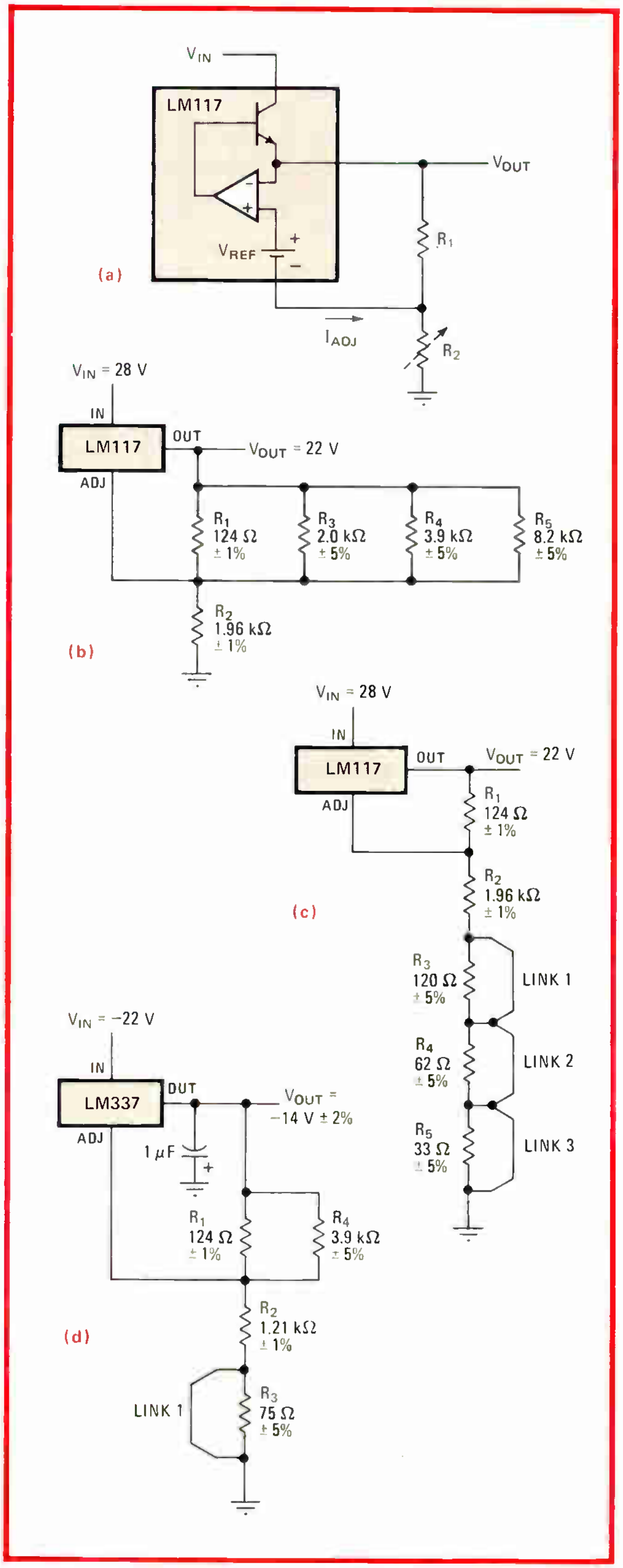
Note that the values of R_3, R_4, and R_5 are independent of the output voltage desired; it is only necessary to select a new value of R_2 so that $V_{REF}(R_2/R_1 + 1)$ is a few percent below the desired output voltage, assuming a V_{REF} of 1.25. In practice, this means selecting R_2 to be proportional to the output voltage desired.

An alternative trimming scheme is shown in (c), whereby R_3, R_4, and R_5, placed in the R_2 line, are initially shorted by jumpers. Here V_{out} is initially lower than the target value and never exceeds that voltage during trimming.

In this procedure:

- If $V_{out} \leq 20.90$, snip link 1.
- If V_{out} is or becomes ≤ 21.55, snip link 2.
- If V_{out} is or becomes ≤ 21.82, snip link 3.

When the output voltage is other than 22, R_3–R_5 need to be chosen in the same proportion to R_2. Thus if the



Tolerance. Programmable regulator's trimmer (a), which is costly and may drift, may be replaced with low-cost, fixed resistor network R_3–R_5 (b) for production-line trimming. Each resistor is systematically removed to bring V_{out} to within 1% of desired value. Alternate scheme uses resistors in series (c). If 2% tolerance is acceptable, one less resistor (d) and simplified procedure accomplishes task.

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scheme in (c) is used for $V_{out} = 12$, then $R_2 = 1.0$ kΩ, $R_3 = 62Ω$, $R_4 = 31Ω$, and $R_5 = 16Ω$. Note too that when approach (b) is used, some care must be taken that all the snipped resistors be removed without shorting anything out. If (c) is used, one end of the cut link should be curled back to prevent shorting.

If 2% tolerance is acceptable, the circuit in (d) will provide trimming with one less resistor and fewer iterations. In this instance, the configuration is shown for the LM337 negative-voltage regulator, where the desired $V_{out} = -14$ V. If the magnitude of $V_{out} \leq 13.75$ V, link 1 is snipped. Then if $V_{out} \geq 14.20$ V, R_4 is cut out.

In most cases, no trimming at all will be required, because most ±1% resistors are well within a tolerance of ±⅓%, and most often the LM337's V_{ref} term is within 1½% of its nominal value. □

8080 program computes 32-by-16-bit quotient

by G. W. Swift and J. P. Eisenstein
Department of Physics, University of California, Berkeley

It is sometimes necessary to perform a 32-bit-by-16-bit division in order to obtain two 16-bit numbers that may be multiplied by a third in the often used 16-bit-by-16-bit multiplication programs. This short subroutine does such a division, returning a 16-bit quotient and a 16-bit remainder. The execution time is about 2½ milliseconds.

The program works much like ordinary long division. It begins by trying to subtract the divisor from the most significant 16 bits of the dividend. The appropriate bit of the quotient will be set or cleared, depending on whether or not the subtraction process yields a 0 or 1 for that bit. The dividend is then shifted 1 bit with respect to the divisor, and the process is repeated. Sixteen such subtractions are necessary to generate the quotient and the remainder.

The dividend is introduced in register pairs HL–BC, with the high-order bytes in HL. The divisor is placed in register pair DE. If the quotient is greater than $2^{16}-1$, the routine will set the carry bit. Otherwise, it returns the quotient in register pair HL, the remainder in register pair BC, the 2's complement of the divisor in register pair DE, and then clears the carry bit. Intermediate results are stored on the stack, so that random-access memories are not required. □

8080 PROGRAM FOR 32-BY-16 DIVISION

Location	Op code	Source statement	Comments
5000		SP EQU 6	
5000	E5	DIVIDE PUSH H	initialize answer location on stack
5001	21 01 00	LXI H, 1	
5004	E3	XTHL	
5005	7A	MOV A, D	form 2's complement of divisor
5006	2F	CMA	
5007	57	MOV D, A	
5008	7B	MOV A, E	
5009	2F	CMA	
500A	5F	MOV E, A	
500B	13	INX D	
500C	E5	PUSH H	
500D	19	DAD D	
500E	DA 41 50	JC ERROR	jump if overflow
5011	E1	LOOP POP H	
5012	DA 3D 50	JC EXIT	jump if done
5015	79	MOV A, C	rotate HL-BC left 1 bit
5016	17	RAL	
5017	4F	MOV C, A	
5018	78	MOV A, B	
5019	17	RAL	
501A	47	MOV B, A	
501B	7D	MOV A, L	
501C	17	RAL	
501D	6F	MOV L, A	
501E	7C	MOV A, H	
501F	17	RAL	
5020	67	MOV H, A	
5021	DA 33 50	JC SURE	
5024	E5	PUSH H	
5025	19	DAD D	
5026	33	INX SP	
5027	33	INX SP	
5028	DA 34 50	JC ANSFIX	
502B	E1	POP H	append "0" to quotient
502C	29	DAD H	
502D	E5	CONT PUSH H	
502E	3B	DCX SP	
502F	3B	DCX SP	
5030	C3 11 50	JMP LOOP	
5033	19	SURE DAD D	
5034	E5	ANSFIX PUSH H	append "1" to quotient
5035	33	INX SP	
5036	33	INX SP	
5037	E1	POP H	
5038	29	DAD H	
5039	23	INX H	
503A	C3 2D 50	JMP CONT	
503D	E3	EXIT XTHL	return with quotient and remainder
503E	C1	POP B	
503F	AF	XRA A	
5040	C9	RET	
5041	E1	ERROR POP H	return with carry set
5042	33	INX SP	
5043	33	INX SP	
5044	C9	RET	

Engineer's newsletter

Making one bus troubleshoot another bus

Even without a bus analyzer for troubleshooting, users of general-purpose interface buses can locate errors in programming or data transmission **if a bus-responsive plotter such as the HP7225A or HP9872A is at hand.** The suggestion comes from James A. Rummell of the McDonnell Douglas Astronautics Co., Huntington Beach, Calif.

Just two steps are necessary, he says. First, command the plotter to go into the mode labeled LB. Then, add the plotter's listen address to the normal command string ("%" for the 7225A as shipped from the factory). The plotter will print out commands or data as they are transmitted, including such unwritten commands as line feed (LF). Notes Rummell, "The only limitation to this approach is that it slows down bus execution, since further commands wait until the commands are lettered."

Waste no more time— find out who's programming what

Desktop computer users who sweat out the writing of new programs always fear they are merely duplicating someone else's efforts. Now, at least for owners of the recently introduced Hewlett-Packard System 35 and System 45, there is a partial solution to the problem.

For these computers, which operate in an enhanced version of American National Standards Institute's Basic, H-P has established **a users' software club, which makes programs available on a three-for-one basis (submit one and get three in exchange).** And in case that's not enough, the club also sponsors information exchanges, area meetings, a software catalog, and a newsletter. Anyone interested in getting all these goodies is invited to contact the Basic User's Club, Hewlett-Packard Co., Desktop Computer division, 3404 East Harmony Rd., Fort Collins, Colo. 80525.

Find out about data access and protection

Both making the connection to a computer network and subsequent easy access to the net are inhibited by the variety of command languages and protocols required by different systems. This problem could be solved if all systems worked with the same commands. Of course this is not the case, but a first pass is described in the National Bureau of Standards' 32-page book, "Common Command Languages for File Manipulation and Network Job Execution: An Example." It is available as S. D. No. 003-003-01965-8 from the U. S. Government Printing Office in Washington, D. C. 20402, and costs $1.50.

At the same time, if you are worried about computer security, NBS's Institute for Computer Sciences and Technology has a list of Computer Security Publications that are available from the Printing Office. List 91 covers **techniques, practices, and policies for protecting computers and data from unauthorized modification, disclosure, or destruction.** Write the Institute at A200 Administration, NBS, Washington, D. C. 20234.

IEEE grants advances to advanced thinkers

Industrial specialists who want to review the state of the art in their area of expertise may compete for $5,500 grants sponsored by the Engineering Foundation. Their reports have to "provide an in-depth analysis of a specific field **including recommendations on engineering research needed to advance the state of the art** in that field" says Neil D. Pundit, the Institute of Electrical and Electronics Engineers' director of technical activities. Further details are available from him at 345 E. 47 St., New York, N. Y. 10017. Deadline for proposals is June 1. **-Harvey J. Hindin**


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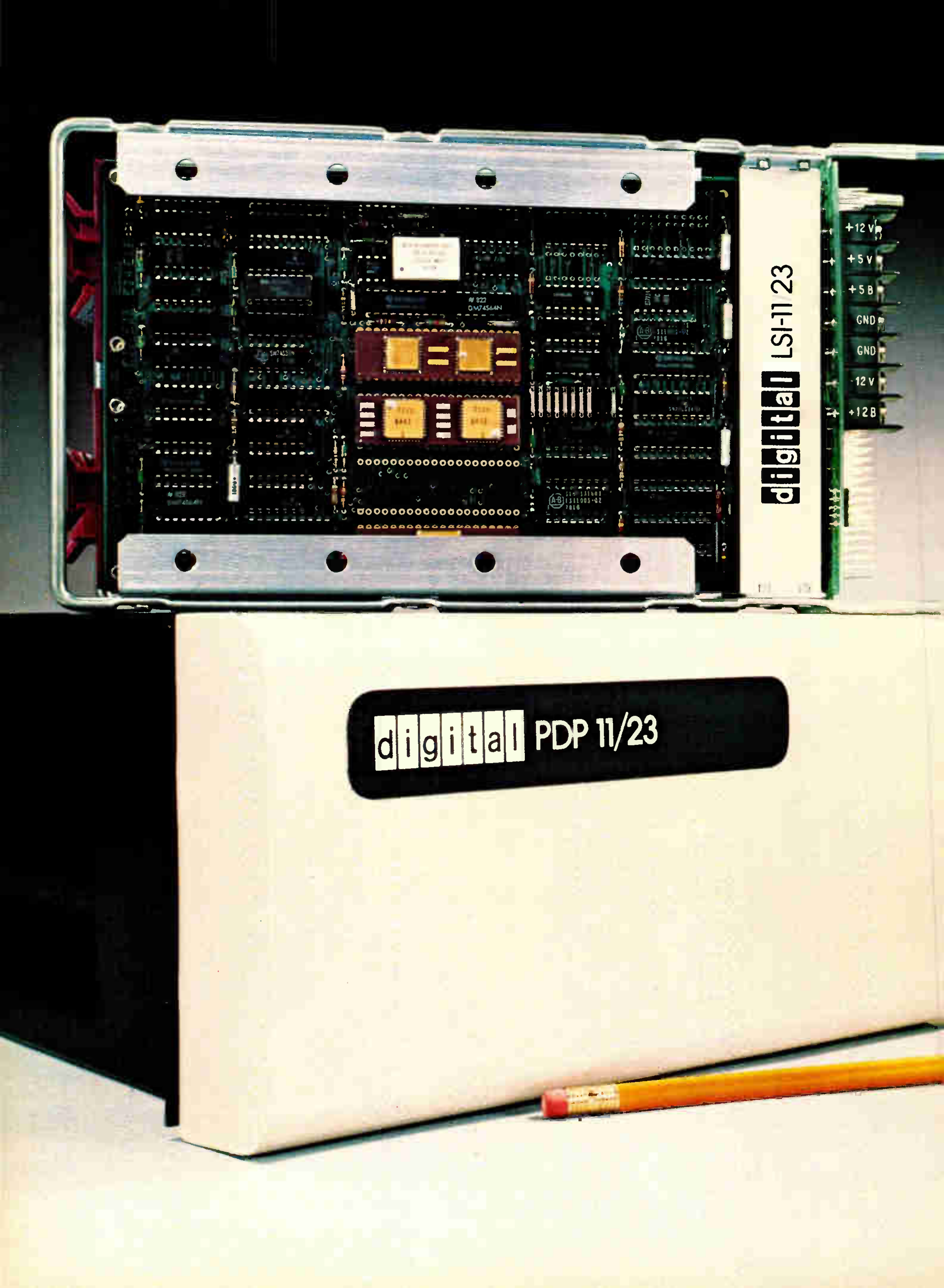

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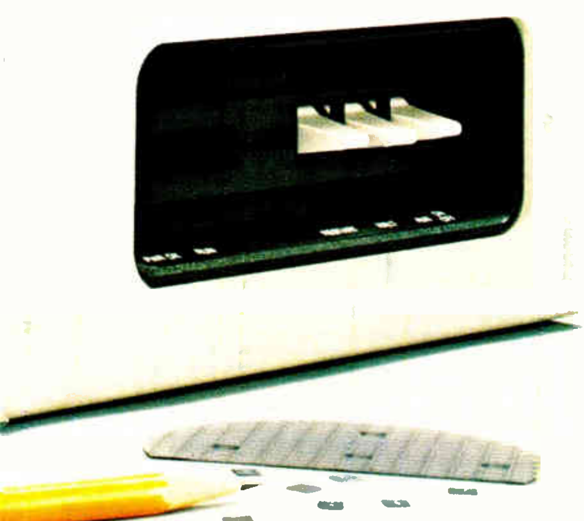

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During May, Digital is conducting half-day seminars on the LSI-11/23 and PDP-11/23 in 30 cities throughout the U.S. and Canada. To find out if a seminar is scheduled in your area, contact your local Digital sales office listed in the Yellow Pages.

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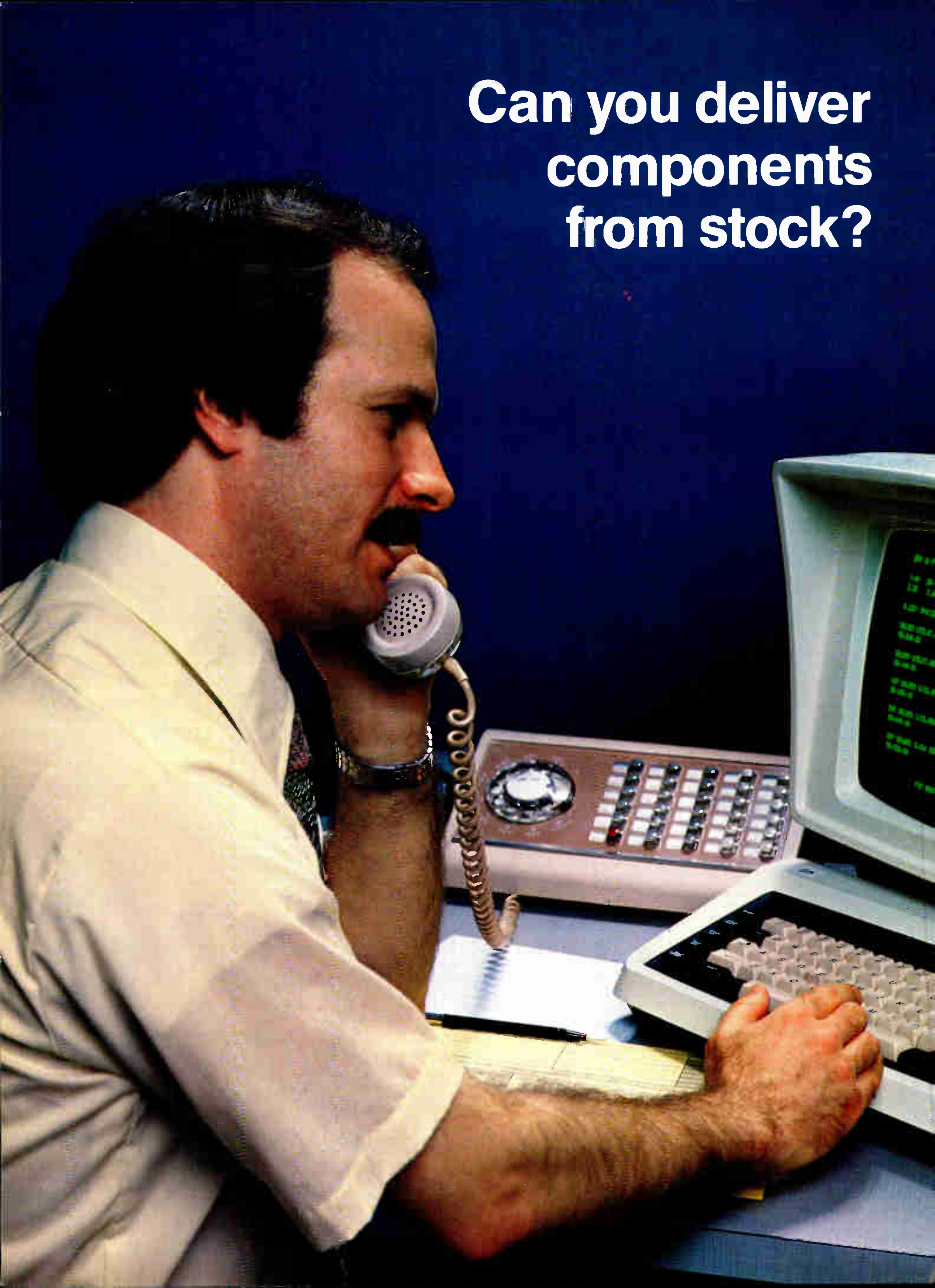
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A-d converter has 16-bit accuracy

Accurate to within 0.0015% of full scale, compact module with 10-μs conversion time is guaranteed to miss no codes from 0° to 70°C

by Nicolas Mokhoff, Components Editor

The demand for high-speed, high-resolution, exceptionally stable analog-to-digital converters is growing rapidly in fields where accurate data gathering in large quantities is required, such as in medical diagnostics, audio recording, automatic testing, general scientific research, and geophysical investigation.

The desired level of performance includes 16-bit resolution, 16-bit accuracy, conversion times as low as 10 μs, and linearity stability on the order of 0.4 ppm/°C. For the most part, converters so far available in the form of compact modules have missed these targets.

Now Zeltex Inc. is introducing its model ZAD7200 and ZAD7400 converters—a pair of 16-bit devices that are guaranteed to miss no codes over their 0° to 70°C operating temperature ranges, while also being virtually adjustment-free for life. The ZAD7200 and 7400 have conversion times of 20 μs and 10 μs, respectively. Other key features and specifications include a 0.4 ppm/°C temperature coefficient of differential nonlinearity, accuracy to within ±0.0015% of full-scale range, five-sided shielding against electromagnetic interference, low noise, low gain and offset drifts, and low sensitivity of code width to clock rate.

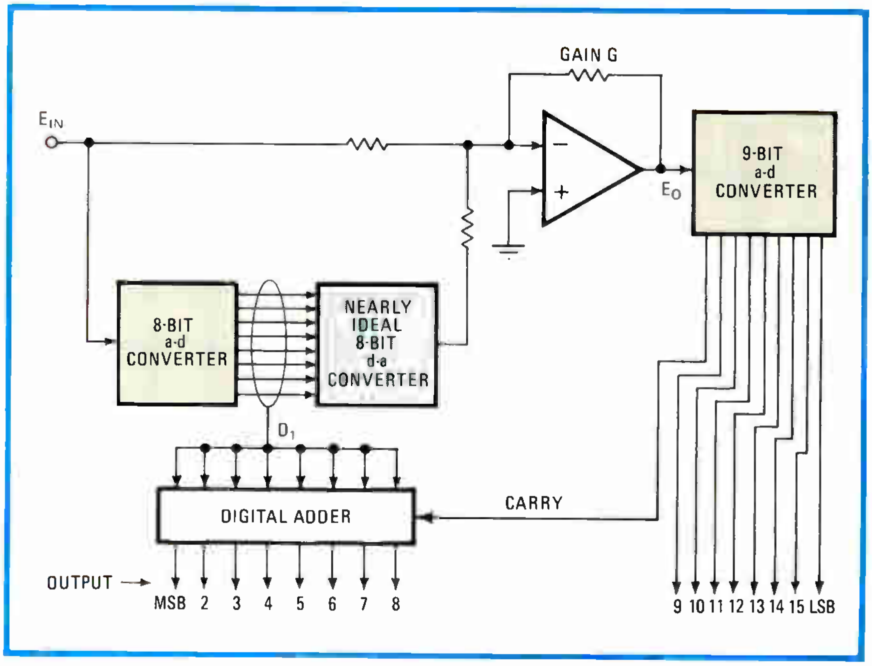
Monobit. In order to achieve these objectives, Zeltex design engineers abandoned most of the conventional approaches that impose state-of-the-art restrictions on critical components like resistors, switches, and comparators. Drift and accuracy problems, which are always associated with binary-weighted ladder networks, are overcome through the use of a so-called monobit ladder network of 15 identical resistors and a kind of successive-approximation configuration.

As the figure shows, an analog input, E_{IN}, is converted to an 8-bit digital word, D_1. This rough digital approximation of the input is then applied to a nearly ideal 8-bit digital-to-analog converter, which produces a precise analog measure of the crude digital approximation of the input. This intermediate analog signal is then subtracted from the actual analog input and the difference is amplified by a gain, G, which serves to generate the analog error voltage, E_O.

The analog error signal is next converted into a 9-bit digital word. The eight least significant bits of this word become the eight LSBs of the output. The most significant bit is carried over to D_1, where it is digitally added to that initial eight-bit approximation to yield the eight most significant bits of the output. Thus, if the 9-bit a-d converter were perfect, the nearly ideal d-a converter were truly perfect, and all offsets and gains were accurately known, the digital output would be a precise 16-bit representation of the input.

Seeking perfection. It is relatively easy to construct the 9-bit a-d converter so that its differential-linearity errors are less than 0.1 LSB. Keeping track of the gains and offsets is also not too difficult. The problem lies in the d-a converter.

To make the d-a converter as



Precise. The heart of this 16-bit a-d converter is an extremely accurate 8-bit d-a converter that is built around a monobit resistive ladder network. The output of the d-a converter is subtracted from the analog input, E_{IN}, at the input of the error amplifier.

nearly perfect as they could, its designers came up with a circuit whose errors refer back to the input on a one-to-one basis. That is, they made the converter less sensitive to errors in its resistor-ladder network, rather than attempt to make that network unrealistically accurate. Their innovative circuit is built around the monobit ladder network, which consists of 15 equal resistors. These resistors are used to add or subtract a single unit of current to the output as the input code changes incrementally. Thus no switch or resistor can affect a current that is more than a sixteenth of full scale. By contrast, in a conventional binary-weighted ladder network, the most significant bit is half of full scale. Assuming equal resistor errors, the monobit approach is eight times less sensitive to resistor errors—that is, it allows 16-bit performance while using the equivalent of 13-bit technology. This fact is the major technological contribution of the ZAD7200 series.

But it's not the only one. The converters are extremely fast for units of their resolution. Their speed is actually inherent in the conversion technique. About 25% of the conversion time is taken up by the initial, rough 8-bit a-d conversion, 25% by d-a conversion and amplifier settling, and the remaining 50% by the second a-d conversion. To attempt to achieve the speed and precision of this device with a standard successive-approximation technique would stretch present-day circuit technology to its limits.

The price of this performance is surprisingly low. The ZAD7200 sells for $750 each in lots of 100 or more pieces. It is contained in a 36-pin module with dimensions of 3 by 4 by 0.375 in. Delivery time is six weeks.

Zeltex plans to follow up the 16-bit a-d converters with both 14- and 18-bit units as well as with low-glitch, high-resolution d-a converters and other support devices aimed at designers of precision data-acquisition systems.

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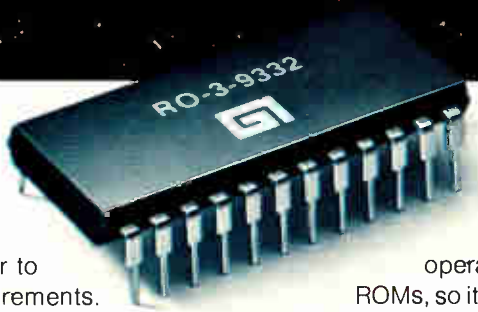

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Keyboard senses body capacitance

Contactless board contains ROM that provides up to four codes per key

A solid-state keyboard from Cherry Electrical Products Corp. senses body capacitance instead of an electrical contact closure, thus achieving a lifetime estimated by the manufacturer to be in excess of 300 million operations. Built around a custom LSI circuit from American Microsystems Inc. and a read-only memory from Cherry Semiconductor, the keyboard includes proprietary noise-rejecting circuitry that prevents false keying by invalid signals, according to Cherry officials.

The LSI processor scans the keys at a rate of one every 1.5 ms and, upon sensing a capacitive contact, sends the key's address to the ROM. There are actually four addresses per key for all but two of the keys. The address chosen is determined by the remaining two, which are referred to as the shift and control keys.

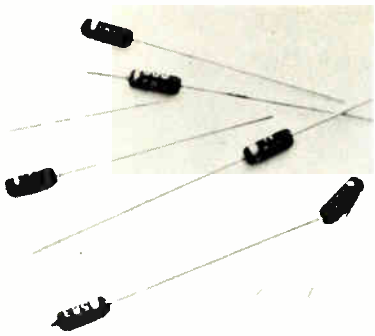
Paul Kollesar, keyboard product manager, notes that the unit is "designed to be altered by the user" and includes a variety of flexibility-enhancing features, such as the ability to accept additional ICs for connection to word-processing systems. Among the options custom programming of the ROM provides are repeat functions for any or all keys and key rollover or lockout.

The basic CB80-12AA keyboard sells for $135 in low-volume custom orders and has 95 keys. A version with an auxiliary 15-key numeric key pad and two additional user-labeled keys is also available under the designation CB80-07AA. Delivery time is 12 weeks.

Cherry Electrical Products Corp., 3600 Sunset Ave., Waukegan, Ill. 60085 [341]

High-Q varactor sports large tuning ratio

The ZC800 is a tuning diode, or varactor, that provides a large tuning ratio and a high Q. The tuning ratio is better than 5 to 1, with a nominal capacitance of 1.8 pF



at 10 V varying to 10 pF at 2 V. The high Q of the diode (300 measured at 50 MHz) assures good selectivity even at the upper end of the very high frequency band.

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A division of Honeywell

Circle 157 on reader service card

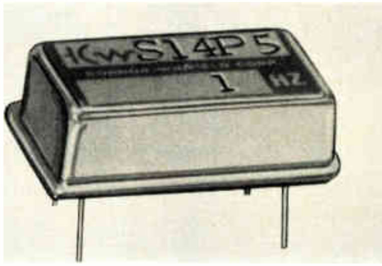
of greater than 25 V, the hyperabrupt-junction ZC800 can accommodate large rf signals. The varactor is useful in industrial and military communications systems as well as in applications using temperature-compensated or voltage-controlled crystal oscillators.

Housed in a DO-7 glass package, the ZC800 sells for $6.30 apiece in quantities from 1 to 99. Delivery time is two weeks.

MSI Electronics Inc., 34-32 57th St., Woodside, N.Y. 11377. Phone A. Lederman at (212) 672-6500 [343]

Crystal oscillator covers very low frequency range

Packaged in a metal case only 0.25 in. high, the model S14P5 crystal oscillator can drive up to 10 TTL loads at any fixed frequency chosen from the range of less than 1 Hz up to 32 kHz. Frequency tolerance is



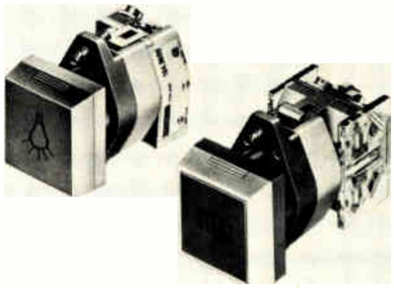
±0.005% across the temperature range from −25° to +75°C.

The device's output is a square wave with a minimum high of 2.4 V and a maximum low of 0.4 V. Units are available at prices of less than $65 with delivery times of four to five weeks.

Connor-Winfield Corp., West Chicago, Ill. 60185. Phone (312) 231-5270 [344]

Push-button switches resist oil invasion

Designed for use in harsh environments, the 04 series consists of oil-tight units. They are available as indicators or as both illuminated and unilluminated push-button switches



that have momentary or maintained action.

Upon operation, push-button switches in the series lock and the state of the switch is indicated. The square-faced switches consist of an actuator to which up to four contact blocks can be attached. The contact blocks snap into place without the use of tools. They may be of the quick-acting or slow-make type and have a mechanical life of three million operations.

The units conform to IEC 144/IP 65 and DIN 40050/P54 standards and come with red, blue, green, yellow, or clear lens caps that can be engraved with the switch's function. In quantities of 100, prices for the 04 series begin at $3.

EAO Switch Corp., 255 Cherry St., Milford, Conn. 06460. Phone Robert Maier at (203) 877-4577 [345]

Economical relays provide 10-A triac output

Using a single glass-passivated triac chip, a series of solid-state relays provide a 10-A output. The TD1210 sells for $11.10 each in quantities of 50 to 99 and the TD2410 sells for $11.70 each in similar quantities. Both devices are for loads with less stringent surge requirements than those requiring silicon-controlled rectifiers. The nonrepetitive peak surge rating for both is 100 A for one cycle. The TD1210 can handle a nonrepetitive maximum peak voltage of 300 V; the TD2410, 500 V.

International Rectifier Corp., Crydom Division, 1521 Grand Ave., El Segundo, Calif. 90245 [346]

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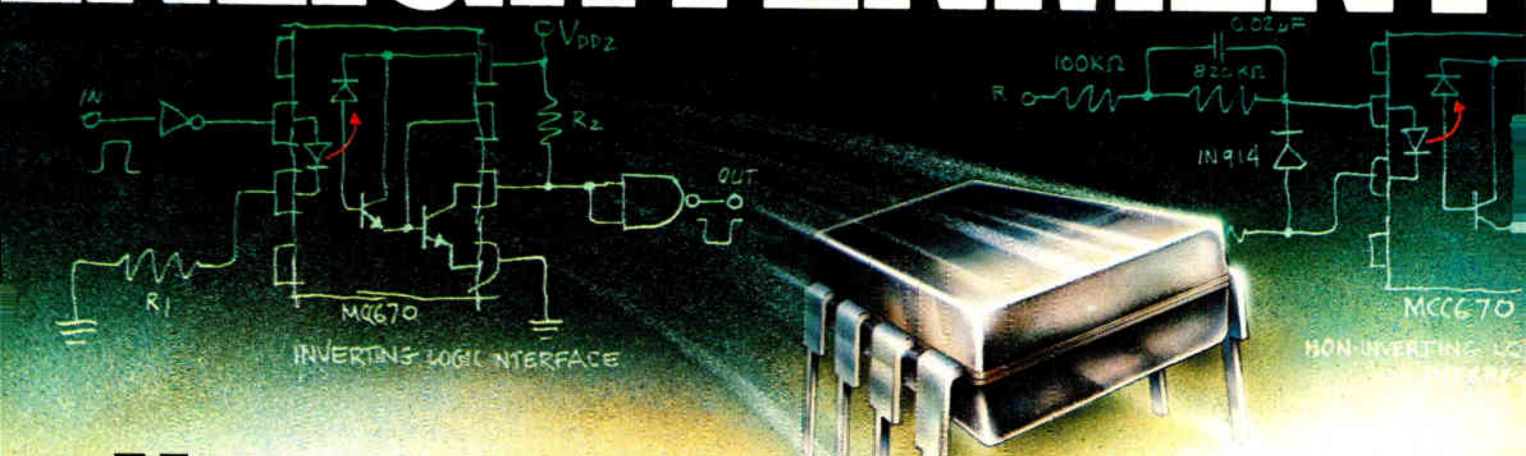

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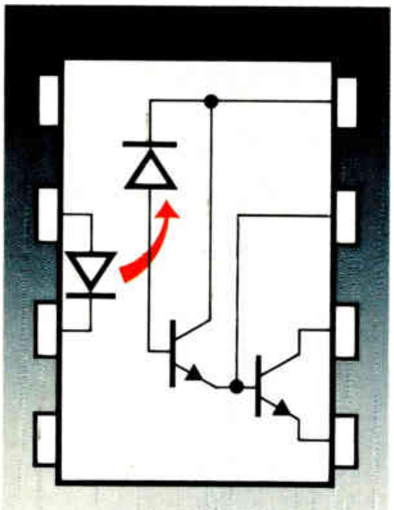
Typical response time is 1.5 microseconds. With the 6N138 Series you'll have fast switching capability at logic loads. Maximum turn-on/turn-off speeds range from 7 to 35 microseconds.



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Microcomputers & systems

DMA boards wait for LSI-11/23

Analog input and output subsystems will also work with LSI-11 and LSI-11/2

In data acquisition, as in just about every other aspect of the computer business, the name of the game is speed. Getting data into memory must often be done at rates the system bus is incapable of handling. Direct memory access (DMA) is obviously the solution, and when the LSI-11/23 microcomputer becomes available from Digital Equipment Corp. later this year, Data Translation Inc. will be waiting for it with a pair of analog input/output boards that include on-board DMA capability. The dual-height boards are the DT2782 analog-input subsystem and the DT2771 analog-output board, both of which will operate with the LSI-11 and LSI-11/2 as well as with the 11/23.

Fast in. The DT2782 is a 12-bit subsystem with a throughput rate of 35,000 samples per second. Extra-cost versions are available with throughput rates of 100 kHz and 125 kHz, with a 14-bit analog-to-digital converter, and with software-programmable gain. Even the fastest a-d converter can run at top speed because the data outputs are double buffered, allowing fast DMA transfer of converted data while a new conversion is being performed. The DT2782 can transfer data over the LSI-11/23's full 18-bit address space, using extended-address bits.

The subsystem can be configured with either 16 single-ended or eight differential input channels. Jumpers allow the user to select one of four input ranges: 0-to-5 V, 0-to-10 V, ±5 V, or ±10 V. The optional programmable-gain amplifier offers a choice of four fixed gains: 1, 2, 4, and 8.

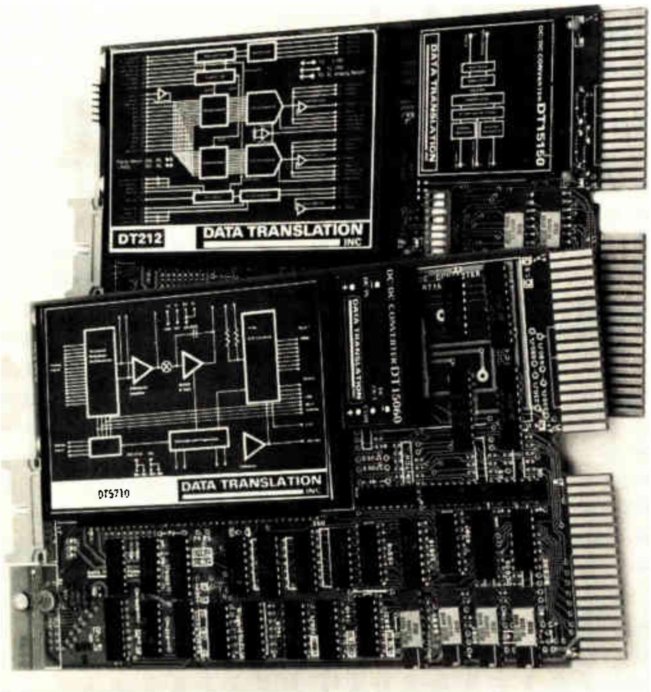
Three jumper-selectable output codes are provided: natural binary, offset binary, and two's complement. Both gain and offset errors are adjustable to zero. System nonlinearity is specified at less than half a least-significant bit, while the accuracy is within ±0.03% of full scale.

Fast out. The DT2771 dual digital-to-analog converter point plotter contains two independent 12-bit d-a converters, a Z-axis control output, and a pair of power amplifiers. Buffered by the amplifiers, the converters can be connected directly to X-Y displays. Operating under programmed input/output and external-interrupt control, the DT2771 can also control a light pen, providing interactive graphics capability. Moreover, the board's DMA capability allows the entire contents of a buffer of up to 16,384 16-bit words to be displayed without program or CPU intervention.

The d-a converters are accurate to within ±0.025% of full scale and linear to within half a least significant bit. Jumper-selectable ranges of 0-to-10 V, ±5 V, and ±10 V are provided. Minimum full-scale output current is 25 mA. Driving 50 feet of cable terminated by a 470-Ω resistor, the converter outputs will settle to within 0.1% of full scale in 1 μs and within 0.01% in 3 μs. Over the range from 0° to 70°C, each channel has an output temperature coefficient of ±25 ppm/°C.

The Z-axis output is a fast TTL-level pulse whose polarity and width can be adjusted.

Both DMA interface boards are priced at $995 each in quantities of one to nine. The DT2782 with a 100-kHz throughput rate goes for $1,295, whereas the 125-kHz version sells for $1,395. The basic 35-kHz board, when equipped with a 14-bit converter, carries a price tag of $1,495. When supplied with the programmable-gain option, its price is $1,170. Shipments will begin in June; delivery time is five days.



Data Translation Inc., 4 Strathmore Rd., Natick, Mass. 01760. Phone Fred Molinari at (617) 655-5300 [371]

Fast controller links peripherals and memory

Systems that require a fast, direct link between a microcomputer's memory and a high-speed peripheral can now be built using either of two direct-memory-access controllers, the 8237 or the 8237-2. The former is designed for use with the 3-MHz

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For more information, contact: ITT North Microsystems Division, 700 Hillsboro Plaza, Deerfield Beach, Florida 33441. Phone: (305) 421-8450, TELEX & TWX: 510-953-7523.

ITT North

Microsystems Division

Circle 163 on reader service card

8085A, whereas the latter operates with either the 8085A-2 or the 8088, both 5-MHz microprocessors.

The 40-pin devices are pin-compatible with earlier, slower units and they offer four independent DMA channels. By cascading the devices so that the output of one becomes the input to one channel of another, the total number of channels in a system can be expanded.

Without relying on the central processing unit, the controllers can perform block transfers from one set of memory locations to another, a desirable capability for word-processing applications. The 8237-2's data-transfer rate of up to 1.6 megabytes per second reduces idle time for the CPU, suggesting it for systems that require frequent DMA operations for, to give an example, refresh of video displays or dynamic read/write memories.

The controllers may be purchased in either plastic or ceramic dual in-line packages. In plastic and in quantities of 100 or more, the 8237 and the 8237-2 sell for $20 and $25 each, respectively. In like quantities, Cerdip units sell for $26.25 and $32.85, respectively. Sample quantities are available now.

Intel Corp., 3065 Bowers Ave., Santa Clara, Calif. 95051. Phone Mike Peak at (408) 987-8080 [373]

Finder frees 6800 programmer from fixed nomenclature

Finder, a general-purpose program for data-base management, lets users employ their own terminology to define and access items. It also allows them to customize file structures for their own requirements. The software is designed to run on 6800-based microcomputers with PerCom's LFD-400 minifloppy-disk systems.

The program requires 24 kilobytes of memory, is interpreted by the company's Super Basic, and uses disks for file storage. All functions ordinarily required for management can be accomplished by the five commands provided. In addition, up

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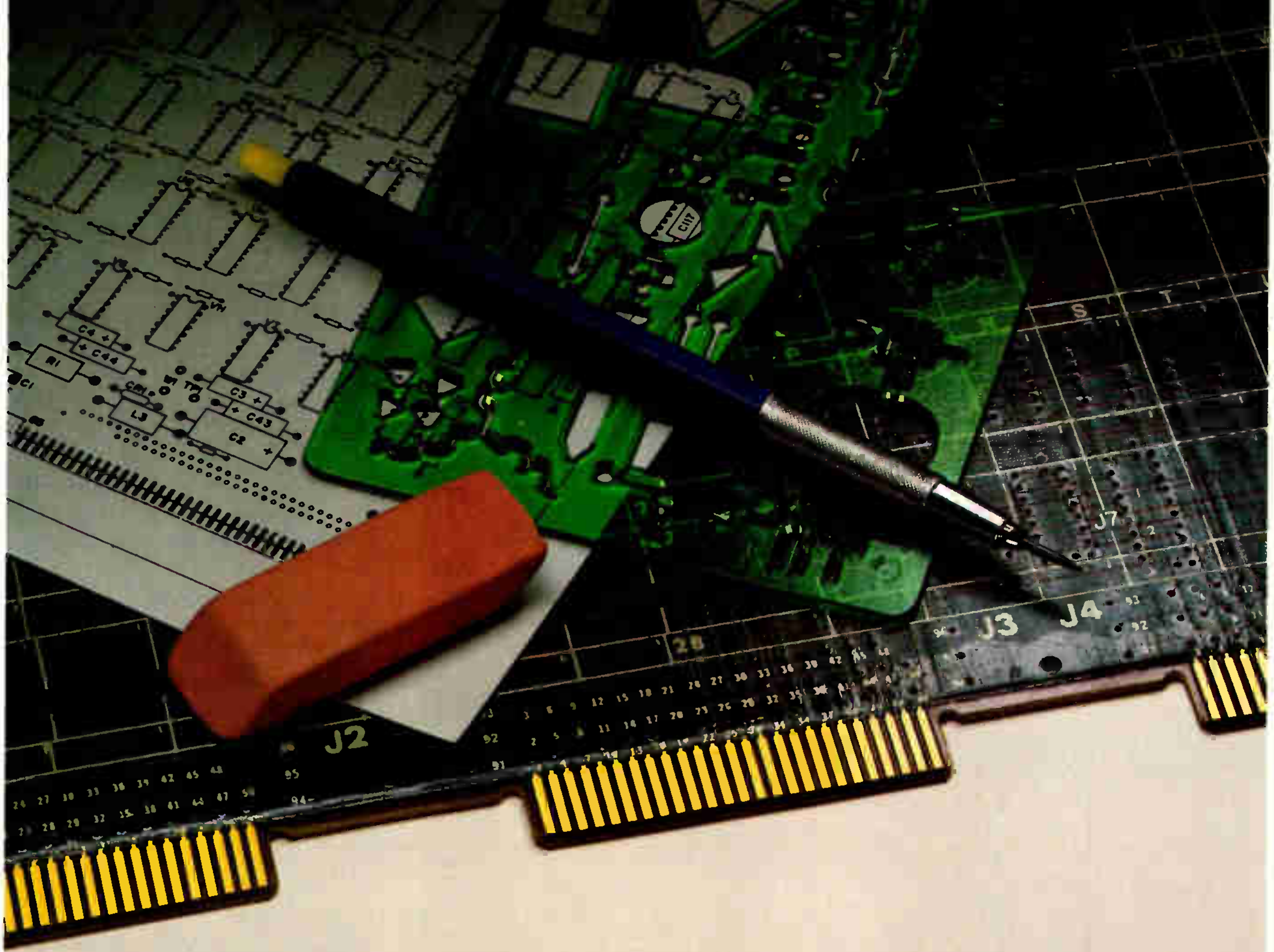

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to three user-defined commands may be added for special functions.

Finder is supplied on a minifloppy disk for $99.95. It comes with a user's manual.

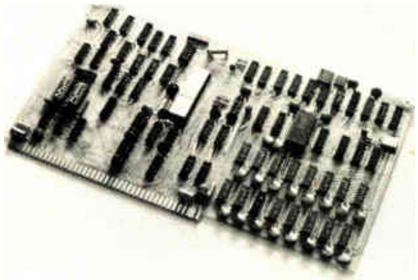
PerCom Data Co., 318 Barnes, Garland, Texas 75042. Phone (214) 272-3421 [375]

Video controller works with series 80, 86 computers

Compatible with both series 80 and 86 single-board computers, the VMC-186 is a video monitor board that permits 20-bit addressing. The board handles five-by-seven-dot or seven-by-nine-dot ASCII upper- and lower-case characters as well as graphics.

It features memory-mapped display, underlining, and blinking, as well as reverse, half-, and zero-intensity video. It provides a hardware clear-screen command and allows memory access at any time without display interference.

Also featured are an addressable cursor, scrolling, and 60-Hz real-time-clock interrupt. Both composite and separated data and sync outputs are available, and the board can



support Motorola's step-scan option. In hundreds, the VMC-186 is priced at $380.

Interphase Corp., 13667 Floyd Circle, Dallas, Texas 75243. Phone (214) 238-0971 [376]

Basic compiler serves machine instead of assembly language

A compiler called A/Basic lets designers produce machine-language programs for 6800 applications nor-

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mally performed by assembly-language software. It can run on either an EXORciser or a Tektronix 8002 with a 6800 emulator board.

Compiled outputs can be directly loaded without assembly or linking into read-only or read/write random-access memories in accordance with a user-defined map. Furthermore, such programs can run without a resident monitor program or run-time subroutine package. These attributes suggest that the compiler be used to generate programs for stand-alone systems such as single-board computers.

Extensions to standard Basic realized in the compiler can support Boolean and shifting operations, interrupt processing, extended string and character functions, and run-time memory allocation. The listing provides detailed memory assignments to simplify debugging. The program needs a 32-kilobyte slot in the development system's memory to run and a disk operating system for compilation.

Microware Systems Corp., 2035 East Ovid Ave., Des Moines, Iowa 50317 [377]

Microcomputers consume up to 35 times less power

Using its XMOS process, National Semiconductor has developed a family of 8-bit, single-chip microcomputers that includes the popular 8048 series and some proprietary designs as well. The technology results in chips that are not only 15 to 20% smaller than their competition, but consume 20 to 25% less power in operation and 12 to 35 times less during standby.

The INS8050 is one of the family's new designs. It contains 4 kilobytes of read-only memory and 256 bytes of read/write memory—more than twice the capacity of any similar device, the company says. The 40-pin devices will work with software generated for earlier 8048 systems.

National Semiconductor Corp., 2900 Semiconductor Dr., Santa Clara, Calif. 95051 [378]

Semiconductors

CRT controller avoids contention

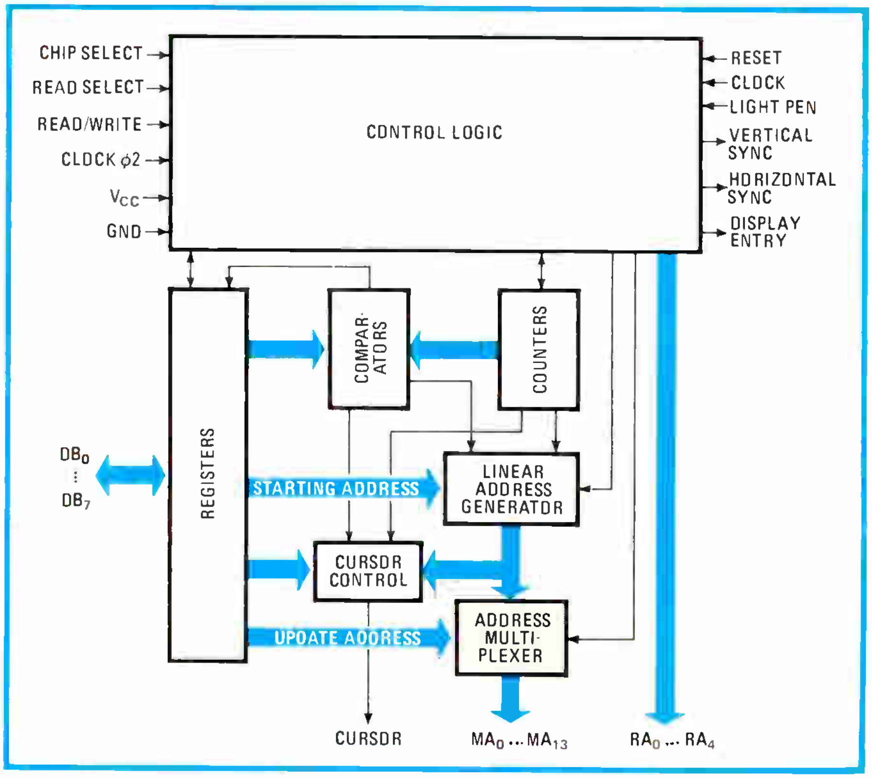
Monolithic unit also handles row-column addresses and detects light-pen strobes

Look behind the cathode-ray tube of many terminals these days and chances are pretty good that you will find a microprocessor. Some time ago, Motorola recognized the growing popularity of this combination and developed for it the MC6845 CRT controller, gaining an enviable position in the marketplace. Now, Synertek has taken a hard look at that part and decided it would do much more than just develop into a second source.

Starting with that controller's chip design, Synertek's engineers added some extra registers and an address multiplexer, thus developing a pin-compatible part with value-added features. Called the SY6545, it permits the refresh read/write random-access memory (RAM) to be isolated from the central processing unit's address and data lines, alleviating the need for external anti-contention circuitry.

"In using the 6845, both the CPU and the CRT controller must access the refresh RAM's address and data buses," says Conrad J. Boisvert, applications manager for Synertek's MPU group. "In order to prevent bus contention, you have to design in extra hardware." With the SY6545, the CPU communicates with memory through the controller, so a designer eliminates the need for that hardware. He must, of course, add some extra programming steps to accommodate the controller's new role.

The 6845 is set up for straight binary addressing only, so software routines are required to convert row-column addresses from a keyboard into sequential binary addresses. The SY6545, however, permits a designer to store characters by row and column locations, requiring less software. The price paid for this is in hardware: either the system will require more memory to store data directly in this form, or conversion



hardware will be required to change row-column into binary addresses to increase storage efficiency.

A third feature that sets the Synertek chip apart from the 6845 is its three-bit status register. "Instead of the CPU depending on external interrupt circuitry to know when a light-pen strobe has occurred, the light-pen bit on the 6545's status register is set when a strobe is detected on the light-pen input. The CPU then knows as soon as it examines the register that there's been a strobe," Boisvert explains.

A convenient time for the CPU to update the refresh memory without causing a glitch on the screen is during the roughly vertical retrace period; another status bit in the register tells the CPU when that retrace is in progress. When the memory has been updated, the register's "ready" status bit is set, informing the CPU that the RAM is prepared to accept more update data.

Plastic and ceramic versions of the SY6545 are being sampled now and production quantities are slated for June. The device is guaranteed to operate at any microprocessor clock rate from 1 MHz down to only 25 kHz and is priced at $21 (plastic) or $29.40 (ceramic) in quantities of 100 or more. A faster "A" version (maximum clock rate of 2 MHz) is being planned.

Synertek, P.O. Box 552, Santa Clara, Calif. 95052 [411]

Fast C-MOS gates crash into low-power applications

For fast analog switching at reasonably low leakage levels, designers have turned to hybrid circuits like the popular DG180 and DG190 families. Now by applying monolithic complementary-metal-oxide-semiconductor technology, Intersil Inc. product engineers are mounting some potentially strong competition to the hybrid devices with a family of analog gates that feature comparable speeds, but with lower power and leakage characteristics.

New products

The first hybrids to be challenged are the DG182 single-pole single-throw, DG188 single-pole double-throw, DG191 dual single-pole double-throw, and the DG185 dual double-pole single-throw circuits. Their pin and functional C-MOS equivalents are the IH5141, 5142, 5143, and 5145, respectively. But a DG191 hybrid, for example, contains five individual chips, whereas the IH5143 has only one. Thus, the monolithic chip should offer improved reliability along with C-MOS technology's low power dissipation.

"More and more designers are setting power limits on their systems designs—they are aiming at low rather than high milliwatts of power," asserts Skip Osgood, Intersil's data acquisition products marketing manager. In comparison with the DG191's 1.5-mA positive-supply and 5-mA negative-supply requirements, the IH5143 is a power miser that draws only 10 μA on each supply over the entire $-55°$ to $+125°$C military-temperature range, according to Osgood.

Current leaking through the drain-to-source "on" resistance of a field-effect transistor produces a voltage drop, hence is a major source of errors in solid-state analog switches. Whereas the on-resistances in both the hybrid and monolithic units are of the same order of magnitude (50 to 75 Ω), the C-MOS device's leakages are an order of magnitude lower. Source and drain leakages (in the "off" mode) are both 0.1 nA for the IH5143 versus 1 nA for the DG191. Drain leakage in the "on" mode is only 0.2 nA for the C-MOS device versus 2 nA for the hybrid.

It is important for the FET switches to turn on and off quickly, and both devices are fast, with the C-MOS product having an edge in turn-on time (175 versus 200 ns). Equally important is the switches' ability to turn off faster than they turn on so that two lines are not inadvertently tied together because one switch turned on before the other turned off. Both technologies provide turn-on times (125 ns for the IH5143 and 130 ns for the DG191) faster than the turn-off times. The

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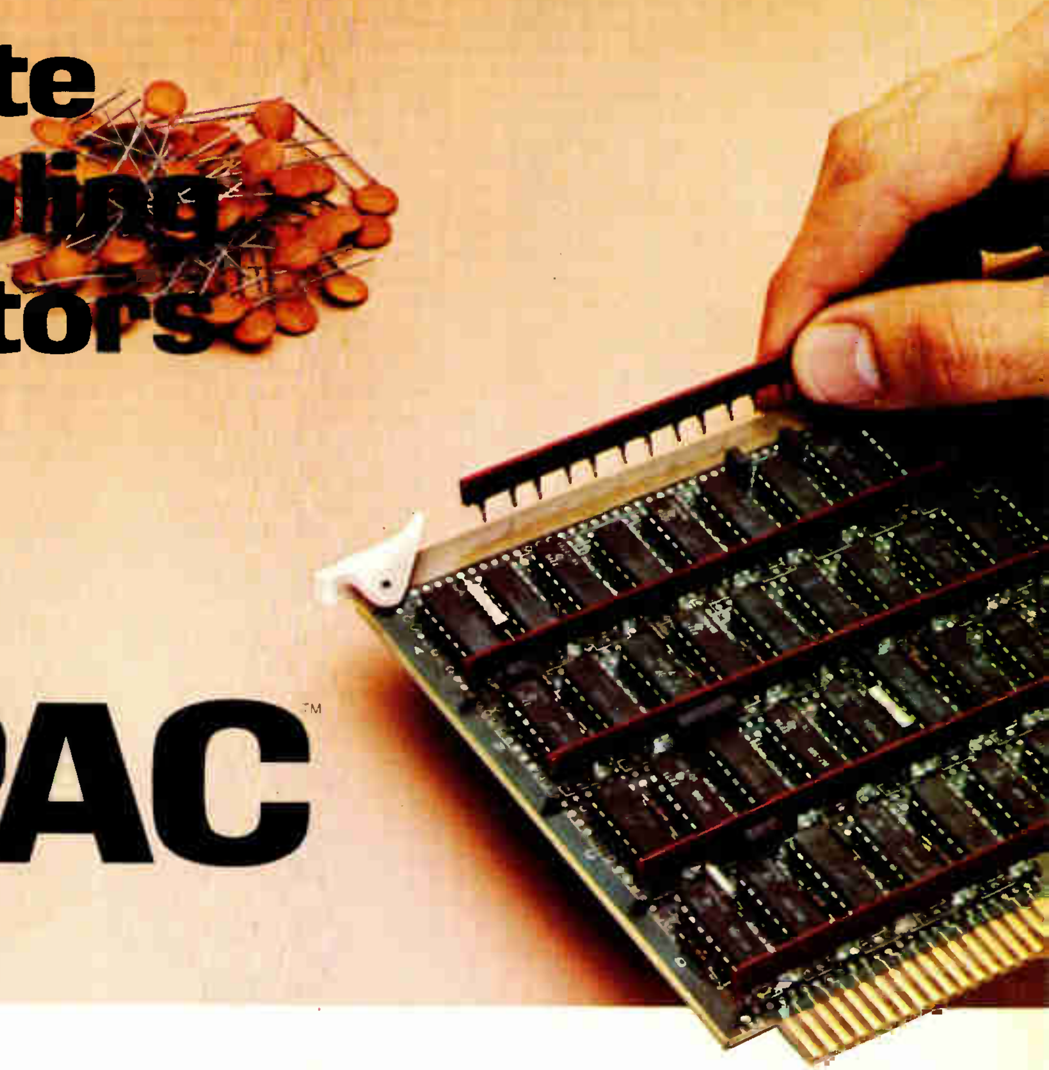

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test conditions, however, are not identical; the C-MOS part is switching ±10 V into a 1-kΩ, 10-pF load, whereas the hybrid's times are based on ±3-V swings into a 300-Ω, 30-pF load.

Although there are significant differences in characteristics between the C-MOS and hybrid families, that is not true of their prices. For example, in 100 and greater quantities the military version of the DG191 (DG191AP) sells for $27.75 and its C-MOS equivalent, the IH5143MDE, costs $25. However, each C-MOS device comes in a commercial temperature range plastic package at considerably lower prices. The IH5143CPE, for example, goes for only $5.40. Military versions of the IH5141, 5142, and 5144 are all $19.50; the IH5140 costs $17.55; and the IH5145 is $25. Plastic versions of each are $4.50, $4.05 and $5.40, respectively, and delivery is from stock.

Intersil, Inc., 10900 N. Tantau Ave., Cupertino, Calif. 95014 [412]

Booster lets op amps drive 50-Ω cables

Designed to boost the current output of operational amplifiers such as Teledyne Philbrick's 1435, the 2035 is a high-speed unit with a slew rate of 250 V/μs. Able to deliver ±5 V at ±100 mA, the booster makes it possible for those op amps to drive 50-Ω coaxial cables at high rates.

When used with a 1435, the 2035's output settles to within 0.025% of final value in 130 ns for a 10-V step. It has a typical gain-bandwidth product of 700 MHz and a full-power bandwidth of 8 MHz.

Packaged in a TO-3 case, the unit operates over the range from −55° to +125°C. All units are processed to MIL-STD-833 specifications. In single quantities, the 2035 can be purchased for $29 or, with additional burn-in and temperature cycling, for $44. Delivery is from stock.

Teledyne Philbrick, Allied Drive at Route 128, Dedham, Mass. 02026. Phone Wah Fea Ng (pronounced Eng) at (617) 329-1600 [414]

voltages in two ranges: 70 to 140 and 140 to 280 V ac from 47 to 440 Hz. They also accept inputs between 200 and 400 V dc. Overvoltage protection is standard, with shutdown occurring at 150 or 300 V ac or at 420 V dc. The units can sustain maximum input voltages of 170 V ac, 350 V ac, or 500 V dc, depending on range.

Also standard is a soft-start feature that limits the input peak current to 10 A at turn-on. Output current protection is not the usual current-limiting system, but power foldback instead. A crowbar circuit protects the output against overvoltage, and, in addition, unlike many competitive units, the S1 and S2 power supplies are also protected against reverse voltage.

The units also offer remote operation with shutdown and turn-on triggered by standard TTL signals. Carry-over time—the time that the supply meets its output specifications after a power-line dropout—is 30 ms. Since most such dropouts last for one power-line cycle (about 16 ms for a 60-Hz line), this is a comfortable safety margin in the majority of cases.

The two series offer a choice of 5, 12, 24, or 48-V dc outputs with combined line and load regulation of 0.2%. Temperature coefficient is typically 0.02%/°C. Rms ripple and noise are less than 0.1% of the output voltage, while the worst-case peak-to-peak noise is less than 0.5%.

In singles, the S1 supply sells for $249.95 and the S2 goes for $279.95. In lots of 10, the prices drop to $236 and $250, respectively. Small quantities are available from stock; large orders may take up to a month.

Semiconductor Circuits Inc., 218 River St., Haverhill, Mass. 01830. Phone (617) 373-9104 [381]

Switchers take inputs from 165 to 230 V ac

A line of fan-cooled switchers accepts a nominal input of 208 V ac at 47 to 63 Hz; operating range extends from 165 to 230 V ac. Efficiency is rated at up to 80%. The

New easy-to-use educational module. Your best ticket to the microprocessor world. Ideal for teaching. Yourself. Or others.

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TM990/519 power supply is available for $65.00.

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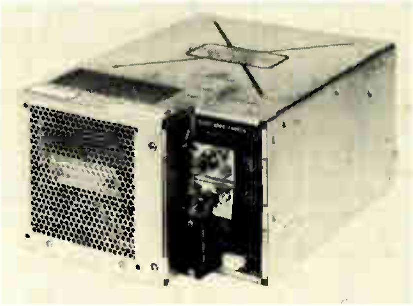


J75OP units deliver up to 840 W at voltages from 2 to 24 V dc, all of which can be adjusted over a range of ±10%. Operating at full power from 0° to 50°C, the switchers can be derated for operation at up to 70% of full power at 71°C. They are offered with current ratings from 35 A (at 24 V) to 180 A (at 2V).

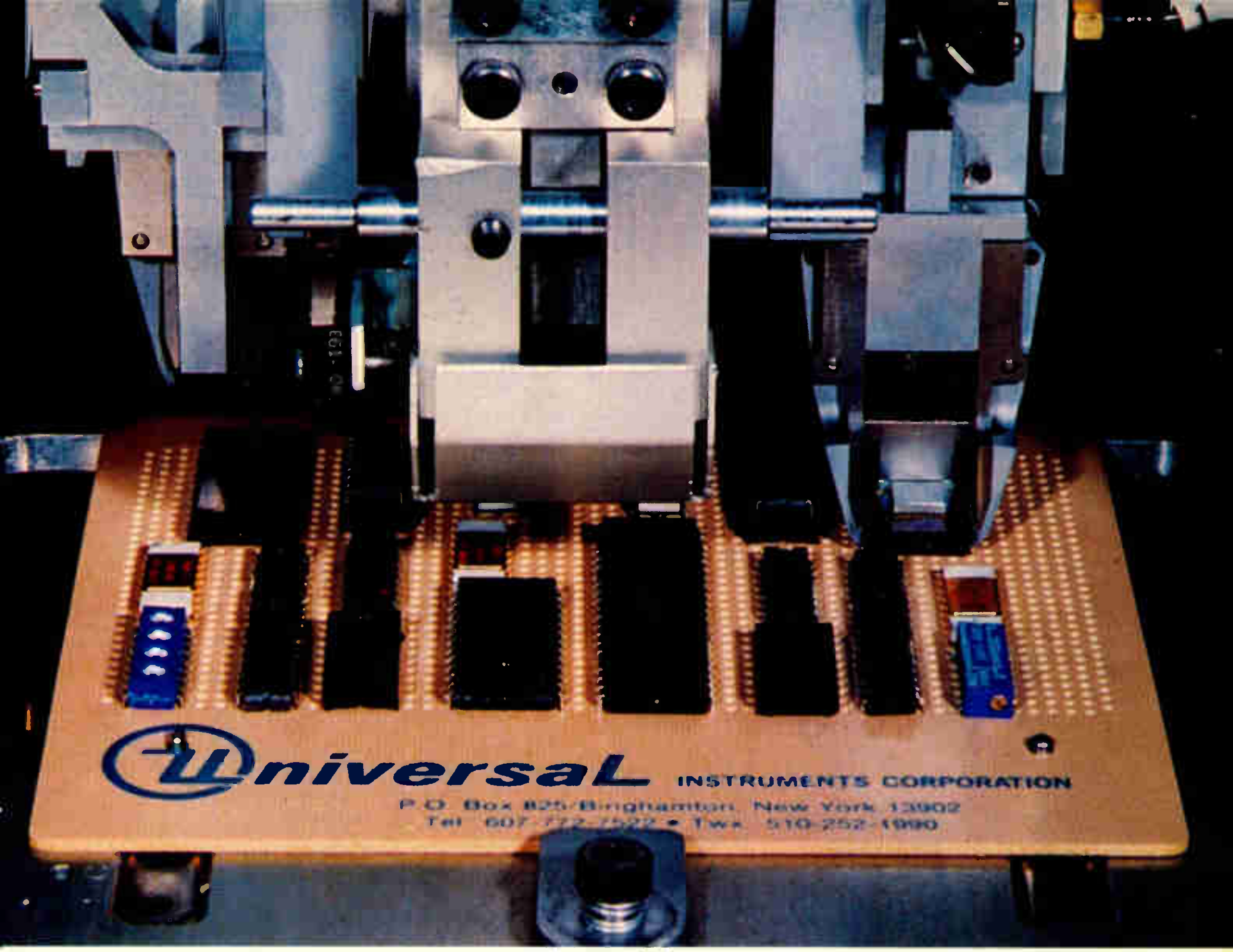
Features offered with the JF75OP series include short-circuit protection, reverse-voltage protection, and overvoltage protection. The units may also be connected in parallel. Other capabilities of the switchers are a turn-on delay time of approximately 400 ms after application of input power and a turn-off delay time of 60 ms after power shutdown. Among the available options are silicon-controlled-rectifier crowbar protection and remote programming.

General specifications include regulation to within 0.1% for any combination of line and load conditions, maximum ripple of 10 mV rms (50 mV peak to peak), and a 0.02%/°C temperature coefficient. In quantities of one to nine, the units sell for $650 each and delivery is from stock.

ACDC Electronics, Division of Emerson Electric Co., 401 Jones Rd., Oceanside, Calif. 92054. Phone (714) 757-1880 [383]

Externally controlled 30-kV supply delivers up to 400 μA

Particularly well suited for electron-beam lithography and similar applications, the 612-300 high-voltage power supply is available in both positive- and negative-voltage models. They provide outputs of from 0 to 30,000 V at 400 μA that can be controlled by an external potentio-



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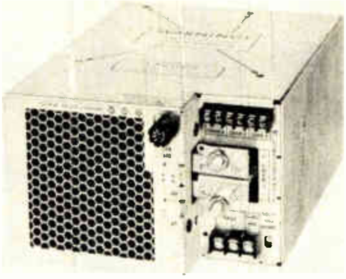
Bertan Associates Inc., 3 Aerial Way, Syosset, N.Y. 11791. Phone (516) 433-3110 [384]

Triple-output unit provides 2 V at 30 A for ECL circuitry

Designed for emitter-coupled-logic systems, the PM2675A and PM2676A multiple-output power supplies are intended for mainframe computer and high-speed data communications applications. The units have input-voltage ranges from 92 to 138 V rms or 184 to 250 V rms and provide an output voltage of 2 V dc with current ratings to 30 A in addition to two other outputs. Depending on the input-voltage range, the units can operate at inputs as low as 80 V ac or 140 V ac. The PM2675A and PM2676A have maximum power outputs of 375 W and 600 W, respectively. Regulation is to within ±2% regardless of line changes, static and dynamic load changes, ripple, noise spikes, and temperature variations. In the event of power loss, output voltage is maintained for 30 ms.

Standard features include over-



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load protection, short-circuit protection, overvoltage protection, and parallel-connection capability. Available options include a logic inhibit signal, input power-fail signal, and silicon-controlled-rectifier crowbar protection.

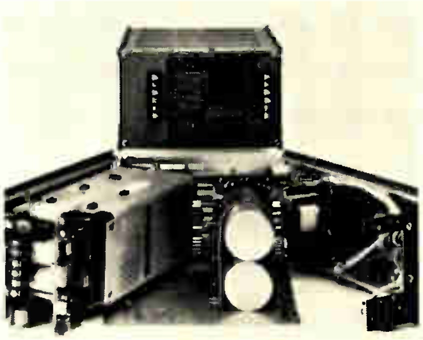
Pioneer Magnetics, 1745 Berkeley St., Santa Monica, Calif. 90404. Phone (213) 829-6751 [385]

Dual-output unit powers data-processing equipment

Intended to power electronic data-processing equipment, the HP 62615D dual-output power supply provides voltages of +11.4 to 15.75 V dc and −11.4 to −15.75 V dc at 17.5 A, with a maximum power output of 525 W. The unit's two output voltages are regulated to within 0.1% for full line and load variations with ripple and noise of less than 50 mV peak to peak. When the ac input is interrupted, the supply maintains the terminal voltage for a minimum carryover time of 10 ms under worst-case conditions of low line and full load. Both outputs are isolated from chassis ground and any output terminal may be grounded separately. Efficiency is rated at 67%.

Two versions, one with and one without output tracking, are available. Both types feature silicon-controlled rectifier crowbar protection, and overvoltage protection. In quantities of 100, the 62615 D sells for $636 each. Delivery time is two weeks after receipt of order.

Hewlett-Packard Co., 1507 Page Mill Rd., Palo Alto, Calif. 94304 [387]



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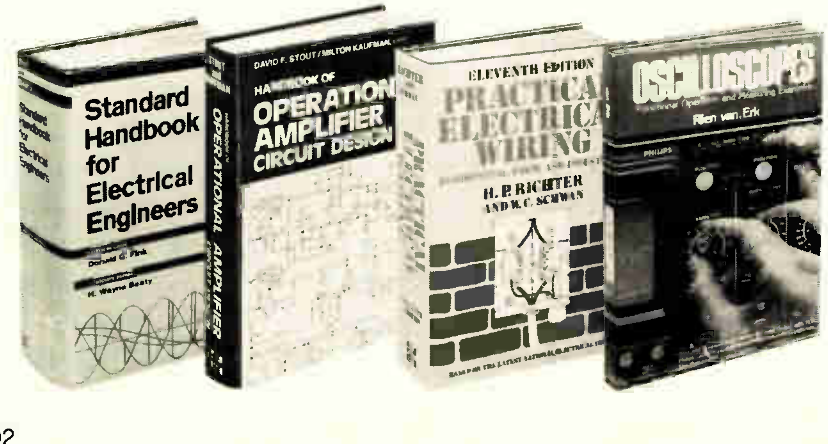

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Modular system adjusts batches of crystals to desired frequency tolerance

Precision quartz crystals are now standard components in wrist watches, clocks, microprocessors, and the like. Each crystal must be accurately adjusted to its nominal frequency—usually by depositing metal on it in a vacuum.

This metal-deposition process has been something of a bottleneck in crystal production, but the MPS-48 modular plating system from Transat Corp. is changing that. According to the company, the new system can produce the same number of trimmed crystals in one hour that present equipment makes in a day. The configuration in the photograph provides 2,000 crystals an hour at an accuracy of three parts per million.

The high production rate is obtained by combining several processing modules in a sort of parallel arrangement so that they can plate several crystals at the same time. The system shown in the photograph comprises a cryogenic pumping system; two alternately pumped vacuum chambers, each with a plating frame for 24 crystals; eight six-crystal plating masks; 12 plating-rate controllers (PRCs); a filament-current supply; and a control console. The plating frames contain the mechanisms required in the vacuum chambers: filaments, crystal sockets, and crystal oscillators. The PRCs control 12 crystals at a time, plating the 48 crystals in four sequential steps. The first unit of this type was recently delivered at a price of about $130,000. The size, cost, and throughput of the system may, of course, be scaled down by reducing the number of system modules.

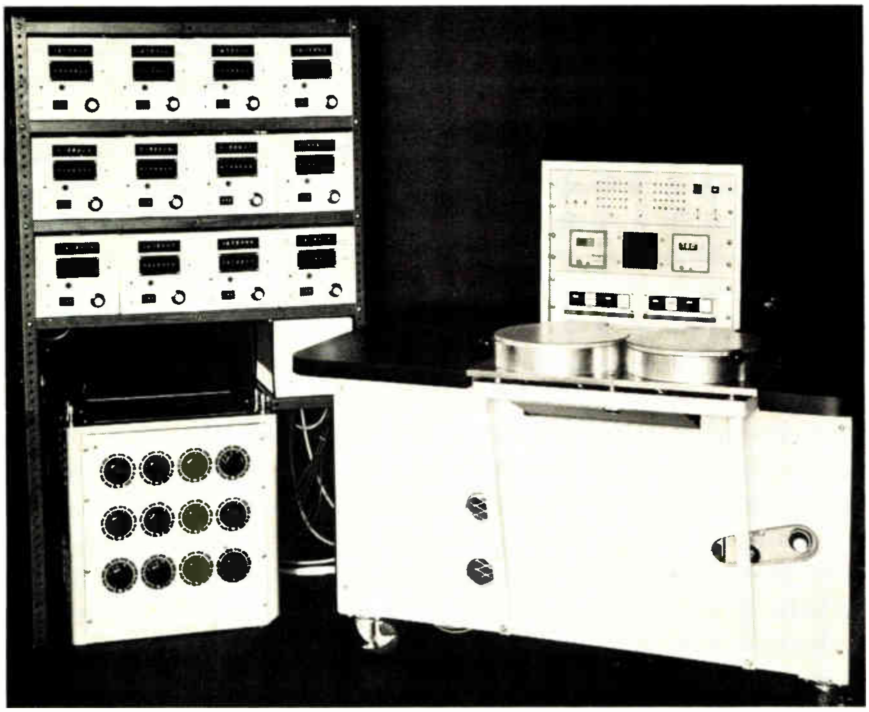
The primary attraction of this system is its high throughput. Since there are multiple crystals per vacuum chamber, the pumping speed per crystal is increased over one-crystal units. Simultaneous adjustment of several crystals increases the plating speed, while a fast load and unload mechanism reduces the time required for batch handling.

The PRCs adjust crystals to within 3 ppm in about 6 seconds. The time may be reduced at some loss in accuracy or increased to improve accuracy, which is directly proportional to plating time. The overall system accuracy is enhanced by keeping the leads between the crystals and the oscillators as short as possible.

Other features of this system are its versatility and ease of maintenance. Variables such as the number of PRCs, number of vacuum chambers, and number of crystals per vacuum chamber can be adapted to customer needs. With several PRCs, several different frequencies may be adjusted simultaneously.

Ease of maintenance has been designed into the modular plating system through the use of plug-in boards in the electronic circuitry and plug-in modules in the plating frames. The frames themselves are detachable and are connected to the external circuitry by means of sockets plugged into feed-through connectors in the walls of the vacuum chambers.

Transat Corp., 3713 Lee Rd., Shaker Heights, Ohio 44120 [391]



Graphics system breaks wiring software bottleneck

Preparing software for wire-wrapping a standard integrated-circuit socket panel can be a time-consuming operation. For instance, from the time an engineer generates a schematic to the actual creation of a punched paper tape to drive a wrapping machine more than two weeks may elapse. This time is consumed in generating to-from lists, key punching cards, delivering the cards to a computer facility, and checking and creating a wiring program.

Now Wire Graphics Ltd. has designed and produced a novel $20,790 graphics system that can do the same job in one to two days. The Wire Graphics Pen-Entry 2000 consists of a cathode-ray-tube display with a light pen, a 0.5-megabyte dual floppy-disk drive, a Z80-based central processor with 48 kilobytes of memory, a high-speed tape punch,

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Circle 197 on reader service card

and a high-speed bidirectional impact matrix printer.

In an actual wire-wrapping tape design, the wire-wrap pins of the sockets and of a portion of the wiring side of the IC socket panel are displayed on the CRT. The engineer working from the schematic "wires" this section of the board with the light pen. As he wires, he also assigns part numbers to each DIP socket and can even wire in discrete parts like decoupling capacitors.

Upon completion of wiring, data is entered into a diskette. This stored data is then used to create a paper tape for wire-wrapping and for printing out wire and parts lists on the system's printer.

The system has many other advantages besides low cost and high speed. It can also optimize wiring paths if desired. The system can be used to wire a 2,000-point board with 4,000-point capability available as an option. A Pen-Entry 2000 can also be applied to other automatic wiring systems such as Stitch Wiring, Solderwrap, and Termipoint. This unit should be ideal for prototype work since revisions that formerly took a week can be done in seconds. In addition, if a paper tape is destroyed or lost, its data will still reside on a diskette.

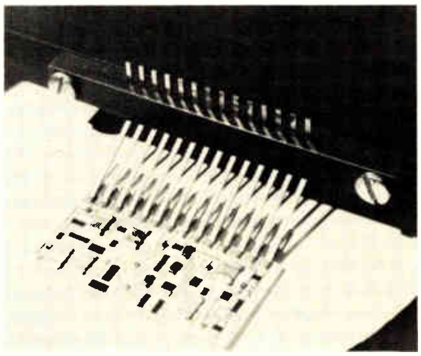
Wire Graphics Ltd., 555 Broad Hollow Rd., Melville, N. Y. 11746 [392]

Multiprobe assembly fits different circuits

The IC-1000 Multiprobe is an assembly of flat-ribbon probes housed in a single molded plastic retainer. This configuration eliminates the need for bulky individual probe retainers and allows a damaged probe to be easily replaced.

The assembly consists of up to 20 probes, making it particularly useful when testing hybrid circuits with multiple outer bonding pads. The flat edge of each probe maintains a continuous line of contact with the pad rather than the usual single point of contact. This extends the life of each probe. Also, the circuit that is being tested remains more visible than it is when bulky individual probes are used.

The IC-1000 is available with either 0.075-mil or 0.100-mil spacings, and other spacings can be made upon request. Each probe is 40 mils wide and 15 mils thick and has a



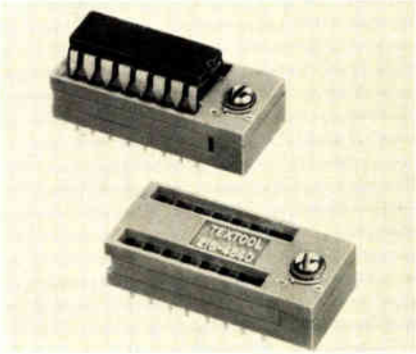
vertical travel of 0.100 in. The entire unit is priced at $60.75. Delivery is made from stock.

IC Industries Inc., P. O. Box 104, Altamonte Springs, Fla. 32701. Phone (305) 831-9797 [395]

Sockets hold ICs with 16, 24, and 40 pins

Designed for end-user production requirements, Econo Zip sockets will accommodate integrated circuits with 16, 24, or 40 pins. The three types of sockets can be mounted on printed-circuit boards with 0.100-mil centers. By simple mechanical rotation and counter-rotation of the cam on the socket, an IC may be inserted into and extracted from the socket with zero force. These sockets will accept crooked or distorted leads.

In quantities of 1,000, the 16-pin version sells for $1.45 each, the 24-pin device for $1.94 each, and the



40-pin type for $2.60 each. Delivery is from stock.

Textool Products Inc., 1410 W. Pioneer Dr., Irving, Texas 75061. Phone (214) 259-2676 [397]

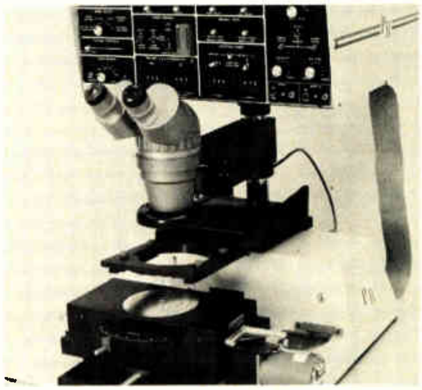
Versatile prober works on line and in lab

Because it is controlled by an 8085 microprocessor, the PS50 automatic wafer prober is able to operate in any of four modes. With this capability, it can serve both in the laboratory and on the production line.

For standard production-line work it uses an X-Y die indexing system, while for matrix probing digital front-panel switches are set.

The PS50 prober comes with a 4-in. wafer chuck, an inking control system with front-panel delay control, an edge-sensing system, and a wafer-orientation system. Prices for the unit vary from $7,000 to $16,000 depending on the particular configuration chosen. Delivery time is currently 10 weeks.

Probe-Rite Inc., 2725 Lafayette St., Santa Clara, Calif. 95050 [398]



Micro power

R6500 any way you like it. That's Rockwell Micropower!

Rockwell's R6500 microcomputer system consists of a family of ten software-compatible CPUs featuring 13 powerful addressing modes.

You get general-purpose I/O, communications interface, standard memory, and combination memory-I/O-timer circuits. Our intelligent peripheral controllers provide cost effective software/hardware tradeoffs. And there's even a single-chip R6500/1 microcomputer.

R6500 CPU Options

	40-Pin DIP		28-Pin DIP				
On chip clock	R6502		R6503	R6504	R6505	R6506	R6507
External Clock		R6512	R6513	R6514	R6515		
Memory Address Space	65K	65K	4K	8K	4K	4K	8K
Interrupts — Maskable	Yes	Yes	Yes	Yes	Yes	Yes	No
— Non-Maskable	Yes	Yes	Yes	No	No	No	No
SYNC — Output indicates op code fetch cycle	Yes	Yes	No	No	No	No	No
RDY — Single step and slow memory synchronization	Yes	Yes	No	No	Yes	No	Yes
$\emptyset_1$ Clock Output	Yes	Yes	No	No	No	Yes	No
DBE — Extended Data Bus Hold Time	No	Yes	No	No	No	No	No

To give you a headstart in microcomputing, AIM 65 (R6500 Advanced Interactive Microcomputer) puts a terminal style keyboard, 20-character alphanumeric printer and display, cassette interface, and more at your fingertips for only $375.

To put your design effort in high gear, Rockwell's SYSTEM 65 is a powerful, easy-to-use development system with two integral mini-floppy disk drives. High level PL/65 language designed to increase programming productivity is also available.

More to choose from in 1979 from the fastest selling microprocessor in 1978. That's Rockwell Micropower.

For more information, contact Department 727-F2, Microelectronic Devices, Rockwell International; P.O. Box 3669; Anaheim, CA 92803, or phone (714) 632-3729.

Rockwell International

...where science gets down to business

Products newsletter

64-kilobit static RAM consumes only 300 mW

It may not be a monolithic device, but the HM5-6564, which made its debut at Electro/79 in New York, is the first 64-kilobit complementary-MOS static read/write random-access memory. The unit, made by Harris Corp.'s Semiconductor Group, Melbourne, Fla., comprises 16 4-K C-MOS static RAMs arranged on 1.8 in.^{2} of area on a ceramic substrate. **The memory consumes less than 5 mW in standby, less than 300 mW when active, and has a maximum access time of 350 ns.** Prototypes are available now, with production quantities expected to be ready for delivery by September. In hundreds, the memory sells for $880 each.

Fairchild to spring development system at computer conference

The National Computer Conference in New York next month should see, among other things, the new microprocessor development system developed by Fairchild Camera and Instrument Corp., Mountain View, Calif. Based on the company's 16-bit Blaze general-purpose computer, **the system is designed for hardware and software development of the 16-bit Isoplanar integrated-injection logic 9440 microprocessor and a forthcoming faster version with built-in multiply and divide circuitry, the 9445.** The system features a cathode-ray-tube terminal, the Blaze central processing unit, a dual flexible-disk drive, a dot-matrix printer, and all required development software.

Printer for microcomputers to sell for below $1 K

Look for Centronics Corp., Nashua, N. H., to introduce a microprocessor-compatible dot-matrix printer that will sell for less than $1,000. **The lightweight machine, which is built around Centronics' free-flight head, can handle roll, cut, and Z-fold paper.** It prints at a rate of 50 characters per second.

Pascal compiler in works for VAX-11/780

A Pascal compiler is now being readied for Digital Equipment Corp.'s VAX-11/780 computer. Designed for instructional and industrial use, the **VAX-11/Pascal is a re-entrant native-mode compiler that supports standard Pascal language capabilities including scalar and structured data types and conditional statements.** The Maynard, Mass., company will license VAX-11/Pascal to non-profit institutions for $2,500 and to others for $5,000. Delivery is expected by the end of this year.

Logic analyzer handles 48 channels

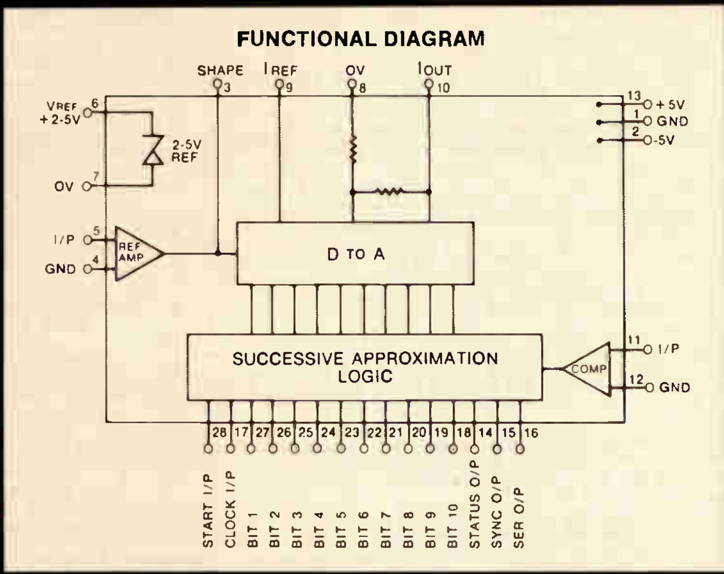
Structured as three independent 16-channel analyzers, the LAM 4850 logic analyzer is a 48-channel instrument in which each channel is backed up by 1,024 bits of data-recording memory and an additional layer of reference memory. **Aimed specifically at microprocessor-based logic systems, the 50-MHz unit can record synchronous logic-state information and asynchronous timing signals simultaneously.** Its four-level sequential triggering scheme allows the user to start or stop a multiclock recording process simply by defining a program sequence. Made in West Germany by Dolch Logic Instruments GmbH, the analyzer is distributed in the U. S. by Kontron Electronic Inc., San Mateo, Calif.

Fast, 10-Bit Monolithic A/D Converter

The Ferranti Model ZN432 is a truly complete successive approximation A/D system with 20 μs conversion time guaranteed.

Features:

- On-chip reference, reference amplifier, comparator, D/A converter and logic
- Bipolar or unipolar operation
- Parallel and serial binary outputs
- TTL/CMOS compatible
- Diffused resistor network, no trim required
- Guaranteed monotonic over operating temperature range
- Commercial and military temperature ranges available



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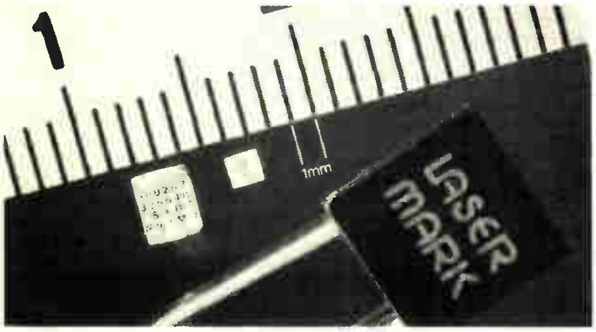
87 MODULAR AVENUE, COMMACK, NEW YORK 11725 / PHONE: (516) 543-0200

Circle 202 on reader service card

LASERMARK MEANS



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L119

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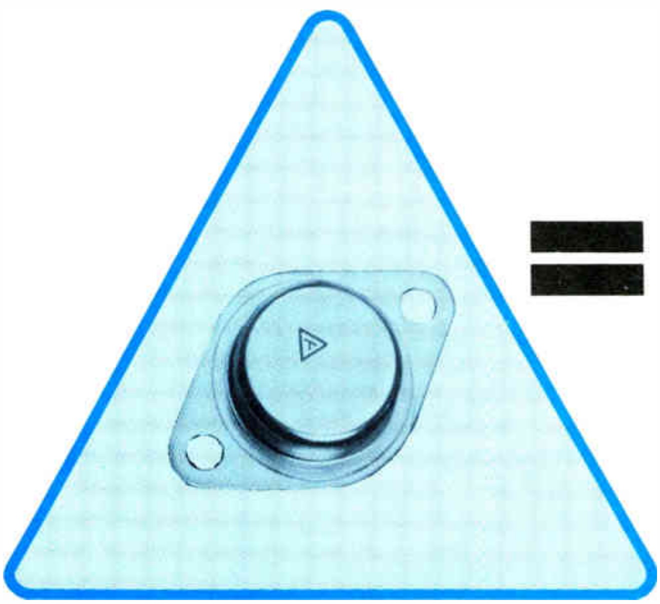

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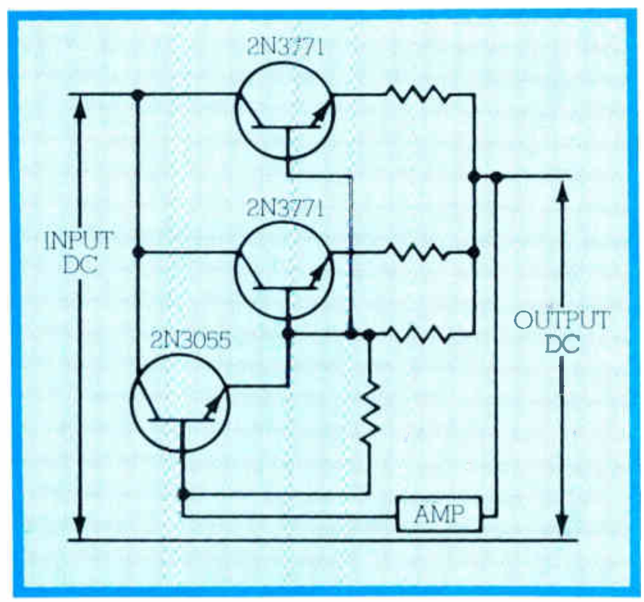

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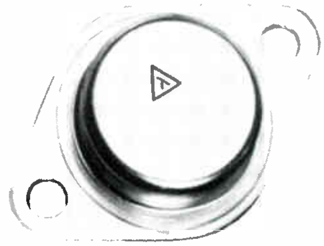


Compare these specifications!

PARAMETER	LAMBDA Darlingtons PMD-16K-60	LAMBDA Darlingtons PMD-12K-60	MOTOROLA* Darlingtons 2N6282	MOTOROLA* Darlingtons 2N6055	RCA* Darlington 2N6384
I_{CER} @ 200°C	7mA@40V	5mA@40V	Not Specified	Not Specified	Not Specified
Thermal Resistance $R_{\Theta JC}$	0.67°C/W	1.5°C/W	1.09	1.75	1.75
h_{FE} min	1000	1000	750	750	1000
Safe Operating Area $I_{s/b}$	7.5A@30V	3A@30V	5.3A@30V	3A@30V	2.8A@35V
Power Dissipation	225W	100W	160W	100W	100W
Derate Power Dissipation from	50°C	50°C	25°C	25°C	25°C

*From Published Specifications.

Now! With

Lambda Power Darlington Transistors

Power Circuit Designers can:

- Use fewer components
- Increase reliability
- Save 40% on material costs alone
- Reduce labor by 50%

OUTSTANDING FEATURES

- The only available 200°C operating junction temperature power Darlingtons in the industry.
- The only available hard glass passivated 200°C power Darlingtons in the industry.
- Guaranteed leakage current stability at 200°C—I_{CER} is equal to 5MA or less, up to 150 watts; I_{CER} is equal to 7MA or less, at 225 watts; I_{CER} is equal to 10 MA or less, at 240 watts.
- Guaranteed current gain vs collector current of greater than or equal to 1000 for NPN and 800 for PNP at 4, 6, 10, and 15 amps for power Darlingtons up to 240 watts.
- All power Darlingtons are guaranteed and 100% tested for $I_{s/b}$ (Secondary Breakdown Current) insuring maximum performance at high energy levels.
- Excellent thermal resistance ($R_{\theta JC}$) on all power Darlingtons providing for more usable power and lower operating temperatures.
- All power Darlingtons are hermetically sealed and are subject to leak testing.

LAMBDA PROCESS FLOW CHART

for Power Semiconductors

PROBED, PASSIVATED WAFERS	Each die is 100% high power visual class probed and electrically tested for all pertinent DC parameters. Rejects are inked.
SAW, BREAK, CLEAN DICE PRIOR TO ASSEMBLY	The 3" wafer is visually inspected prior to sawing. The wafer is grooved by use of a saw, and the dice are separated by fracture along the saw groove.
100% DIE VISUAL INSPECTIONS FOR METAL, CRACKS, OXIDE ALIGNMENT	Prior to package assembly, each die is subject to 100 power microscopic inspection to eliminate devices with visual defects that could cause failure in normal application.
DIE ATTACH AND 100% INSPECTION	Each die is attached to a JEDEC TO-3 package base using Sn/Pb/Ag soft solder. Each package and die is inspected for solder void and proper orientation.
WIRE BOND	Aluminum wires are ultrasonically bonded to both die and package terminals. Each bond is inspected and each wire pulled (Flick Test).
100% VISUAL INSPECTION	Prior to package sealing, each subassembly is subject to 50 power visual inspection to ensure device bond integrity, freedom from foreign material, and conformance to die visual standards. All devices are cleaned and baked for 14 hours.
CAP JEDEC TO-3 RESISTANCE WELD (STEEL) FURNACE SEAL (COPPER)	Lambda devices utilizing TO-3 packages are hermetically sealed in a JEDEC TO 3 package. Steel base packages are resistance welded. Copper base packages are furnace sealed. Cold welding is not used.
LEAK TEST (GROSS)	Each device is gross leak tested by use of fluorocarbon bubble testing
LEAK TEST (FINE)	A helium tracer gas leak test to $5X10^{-8}$ is used to eliminate devices with defective seals. Testing is done to a 1.5 AQL. If parts fail they are 100% tested. (Min 50 devices/lot)
100% DC PARAMETRIC TEST, + 25°C	All devices are electrically tested for conformance to +25°C DC parameters. Automatic test equipment assures proper testing.
100% SECOND BREAKDOWN TEST POWER DARLINGTONS	All power Darlingtons are 100% tested to conformance to the specified forward biased second breakdown current (Is/b). Non-destructive Is/b test techniques assure conformance to applicable safe operating area (SOA).
100% POWER CYCLE VOLTAGE REGULATORS	All devices are power cycled between case temperatures of 50°C and 100 C. Power dissipation during the heating cycle is approximately 5 watts resulting in approximately 10 cycles in 1 hour.
SAMPLE AC PARAMETERS 100% DC PARAMETRIC TEST, +25°C VOLTAGE REGULATORS	All devices are electrically retested for conformance to +25°C DC parameters.
SAMPLE AC PARAMETERS SAMPLE DC PARAMETRIC TEST AT +200°C POWER DARLINGTONS	Each production lot of power Darlingtons is sample tested for conformance to all specified device DC parameters at T_j = +200°C, including BVCER and ICER. Testing of product at +200°C assures the utmost in device stability in a power Darlington.
SELECT LIFE TEST SAMPLES CONDUCT LIFE TEST FINISHED GOODS STOCK	Periodic tests are performed upon randomly selected device samples to assure product quality. Tests performed include solderability, temperature cycling, seal, moisture resistance, terminal strength, mechanical shock, vibration, acceleration, radiographic inspection, and power burn in (thermal fatigue). Test results are available to qualified personnel upon request to Lambda.

GENERAL DESCRIPTION

The PMD-10K, 12K, 16K, 1600K, and 18K series of devices are three-terminal NPN Power Transistor Darlingtons. The PMD-11K, 13K, 17K, 1700K, and 19K series of devices are three-terminal PNP Power Transistor Darlingtons. These devices are monolithic epitaxial base structures with built-in base to emitter shunt resistors. The devices are CVD glass passivated to increase reliability and provide reduced high temperature reverse leakage current. This important feature helps to enable this series of Darlington devices to meet guaranteed junction operating temperatures of 200°C. Internal diode protection (D1) of the Darlington configuration is built into the structure to limit the device power dissipation during negative overshoot.

The five different series of NPN and five different series of PNP Power Transistor Darlington devices, are available in sustaining voltages ranging from +40 to +100 volts, and power dissipation levels from 100 to 240 watts. All Darlington devices are hermetically sealed steel or copper TO-3 packages, depending on power dissipation requirements, providing high reliability and low thermal resistance, when used with appropriate heat sinks.

ABSOLUTE MAXIMUM RATINGS

RATING	SYMBOL	12K 40 13K 40	12K 60 13K 60	12K 80 13K 80	12K 100 13K 100	10K 40 11K 40	10K 60 11K 60	10K 80 11K 80	10K 100 11K 100	1600K 1700K	1601K 1701K	1602K 1702K	1603K 1703K	UNITS
Collector Emitter Voltage	V_{CEO}	40	60	80	100	40	60	80	100	40	60	80	100	Vdc
Collector Base Voltage	V_{CBO}	40	60	80	100	40	60	80	100	40	60	80	100	Vdc
Emitter Base Voltage	V_{EBO}	5	5	5	5	5	5	5	5	5	5	5	5	Vdc
Collector Current Cont. Peak	I_C I_C	8 16	8 16	8 16	8 16	12 20	12 20	12 20	12 20	20 40	20 40	20 40	20 40	Adc
Base Current	I_B	0.12	0.12	0.12	0.12	0.2	0.2	0.2	0.2	0.5	0.5	0.5	0.5	Adc
Thermal Resistance	$R_{\theta JC}$	1.5	1.5	1.5	1.5	1.0	1.0	1.0	1.0	.83	.83	.83	.83	°C/W
Total Internal Dissipation	P_D @$T_c = 50°C$	100	100	100	100	150	150	150	150	180	180	180	180	Watts
	Derate	Derate at 0.667 W/°C, $T_A \geqslant 50°C$				Derate at 1 W/°C, $T_A \geqslant 50°C$				Derate at 1.2W/°C $T_A \geqslant 50°C$				
Temp. Range Operating Storage	T_j T_{STG}	-65° to +200°C				-65° to + 200°C				-65° to +200°C				°C

RATING	SYMBOL	16K 40 17K 40	16K 60 17K 60	16K 80 17K 80	16K 100 17K 100	18K 40 19K 40	18K 60 19K 60	18K 80 19K 80	18K 100 19K 100	UNITS
Collector Emitter Voltage	V_{CEO}	40	60	80	100	40	60	80	100	Vdc
Collector Base Voltage	V_{CBO}	40	60	80	100	40	60	80	100	Vdc
Emitter Base Voltage	V_{EBO}	5	5	5	5	5	5	5	5	Vdc
Collector Current Cont. Peak	I_C I_C	20 40	20 40	20 40	20 40	30 60	30 60	30 60	30 60	Adc
Base Current	I_B	0.5	0.5	0.5	0.5	.75	.75	.75	.75	Adc
Thermal Resistance	$R_{\theta JC}$	0.67	0.67	0.67	0.67	.625	.625	.625	.625	°C/W
Total Internal Power Dissipation	P_D @$T_c = 50°C$	225	225	225	225	240	240	240	240	Watts
	Derate	Derate at 1.5W/°C, $T_A \geqslant 50°C$				Derate at 1.6w/°C $T_A \geqslant 50°C$				
Temp. Range Operating Storage	T_j T_{STG}	-65° to +200°C				-65° to +200°C				°C

ORDERING INFORMATION

Type	Voltage Rating	Rated Power (watts)	Qty 1-99	Qty 100-999	Qty 1000-2499	Qty 2500-4999
PMD 10K 40	40V	150	$1.90	$1.55	$1.39	$1.33
PMD 10K 60	60V	150	2.10	1.68	1.50	1.44
PMD 10K 80	80V	150	2.32	1.86	1.67	1.60
PMD 10K 100	100V	150	2.70	2.16	1.94	1.86
PMD 12K 40	40V	100	1.10	.88	.81	.78
PMD 12K 60	60V	100	1.14	.91	.84	.81
PMD 12K 80	80V	100	1.20	.95	.87	.85
PMD 12K 100	100V	100	1.25	1.00	.92	.89
PMD 1600 K	40V	180	2.38	1.91	1.72	1.64
PMD 1601 K	60V	180	2.51	2.00	1.79	1.72
PMD 1602 K	80V	180	2.85	2.27	2.04	1.96
PMD 1603 K	100V	180	3.32	2.64	2.36	2.26
PMD 16K 40	40V	225	4.59	3.69	3.24	3.15
PMD 16K 60	60V	225	4.68	3.78	3.42	3.33
PMD 16K 80	80V	225	5.05	4.15	3.50	3.42
PMD 16K 100	100V	225	5.60	4.60	3.90	3.80
PMD 18K 40	40V	240	5.28	4.24	3.73	3.62
PMD 18K 60	60V	240	5.38	4.35	3.93	3.83
PMD 18K 80	80V	240	5.80	4.77	4.03	3.93
PMD 18K 100	100V	240	6.44	5.29	4.49	4.37

Type	Voltage Rating	Rated Power (watts)	Qty 1-99	Qty 100-999	Qty 1000-2499	Qty 2500-4999
PMD 11K 40	40V	150	$1.90	$1.55	$1.39	$1.33
PMD 11K 60	60V	150	2.10	1.68	1.50	1.44
PMD 11K 80	80V	150	2.32	1.86	1.67	1.60
PMD 11K 100	100V	150	2.70	2.16	1.94	1.86
PMD 13K 40	40V	100	1.10	.88	.81	.78
PMD 13K 60	60V	100	1.14	.91	.84	.81
PMD 13K 80	80V	100	1.20	.95	.87	.85
PMD 13K 100	100V	100	1.25	1.00	.92	.89
PMD 1700 K	40V	180	2.38	1.91	1.72	1.64
PMD 1701 K	60V	180	2.51	2.00	1.79	1.72
PMD 1702 K	80V	180	2.85	2.27	2.04	1.96
PMD 1703 K	100V	180	3.32	2.64	2.36	2.26
PMD 17K 40	40V	225	5.10	4.10	3.60	3.50
PMD 17K 60	60V	225	5.20	4.20	3.80	3.70
PMD 17K 80	80V	225	5.60	4.60	3.90	3.80
PMD 17K 100	100V	225	6.16	5.06	4.18	4.18
PMD 19K 40	40V	240	5.80	4.70	4.15	4.00
PMD 19K 60	60V	240	5.92	4.78	4.33	4.21
PMD 19K 80	80V	240	6.38	5.25	4.43	4.37
PMD 19K 100	100V	240	7.08	5.82	4.93	4.81

Contact The Factory For Higher Quantity Prices. Device Configurations, Specifications, And Prices Subject To Change Without Notice.

CROSS REFERENCE GUIDE FOR IMPROVED EQUIVALENTS*

MOTOROLA PART NUMBER	LAMBDA EQUIVALENT	LAMBDA IMPROVED REPLACEMENT
MJ-3000	LMJ-3000	PMD-10K-60
MJ-4033	LMJ-4033	PMD-10K-60
MJ-3001	LMJ 3001	PMD 10K-80
MJ-4034	LMJ-4034	PMD 10K-80
MJ-4035	LMJ-4035	PMD-10K-100
MJ 2500	LMJ 2500	PMD 11K-60
MJ-4030	LMJ-4030	PMD-11K-60
MJ-2501	LMJ-2501	PMD 11K-80
MJ 4031	LMJ-4031	PMD 11K-80
MJ-4032	LMJ 4032	PMD 11K 100
MJ 1000	LMJ 1000	PMD 12K 60
MJ 1001	LMJ 1001	PMD 12K 80
MJ-900	LMJ 900	PMD 13K 60
MJ-901	LMJ 901	PMD 13K-80
2N 6282	2N 6282	PMD 1601K
2N 6283	2N-6283	PMD 1602K
2N 6284	2N 6284	PMD 1603K
2N 6282	2N 6282	PMD-16K 60
2N 6283	2N 6283	PMD 16K 80
2N-6284	2N 6284	PMD-16K 100
2N 6285	2N 6285	PMD 1701K
2N-6286	2N 6286	PMD 1702K
2N 6287	2N 6287	PMD 1703K
2N-6285	2N 6285	PMD-17K 60
2N-6286	2N 6286	PMD 17K 80
2N-6287	2N 6287	PMD 17K-100

FAIRCHILD PART NUMBER	LAMBDA EQUIVALENT	LAMBDA IMPROVED REPLACEMENT
2N-6057	2N-6057	PMD-10K 60
SE 9303	LSE 9303	PMD-10K-60
SE 9304	LSE 9304	PMD-10K 80
SE 9305	LSE 9305	PMD 10K-100

FAIRCHILD PART NUMBER	LAMBDA EQUIVALENT	LAMBDA IMPROVED REPLACEMENT
2N-6050	2N-6050	PMD-11K-60
SE-9403	LSE-9403	PMD-11K-60
SE-9404	LSE 9404	PMD-11K-80
SE-9405	LSE-9405	PMD 11K-100
SE-9303	LSE-9303	PMD-12K 60
SE-9304	LSE 9304	PMD-12K-80
SE-9305	LSE 9305	PMD-12K 100
SE-9403	LSE-9403	PMD-13K-60
SE 9404	LSE-9404	PMD-13K-80
SE 9405	LSE 9405	PMD-13K 100
2N 6282	2N 6282	PMD 1601K
2N 6283	2N 6283	PMD 1602K
2N 6284	2N 6284	PMD 1603K
2N 6282	2N 6282	PMD 16K-60
2N 6283	2N 6283	PMD-16K-80
2N 6284	2N 6284	PMD 16K 100
2N 6285	2N 6285	PMD 1701K
2N 6286	2N 6286	PMD 1702K
2N 6287	2N 6287	PMD 1703K
2N 6285	2N 6285	PMD 17K 60
2N 6286	2N 6286	PMD 17K 80
2N 6287	2N 6287	PMD 17K 100

RCA PART NUMBER	LAMBDA EQUIVALENT	LAMBDA IMPROVED REPLACEMENT
RCA 8350	LCA-8350	PMD 11K-40
RCA-8350A	LCA-8350A	PMD 11K-60
RCA-8350B	LCA-8350B	PMD 11K-80
RCA-1000	LCA-1000	PMD-12K-60
RCA 1001	LCA-1001	PMD-12K 80
RCA 8350	LCA-8350	PMD 13K-40
RCA-8350A	LCA-8350A	PMD 13K-60
RCA-8350B	LCA-6350B	PMD 13K-80
2N-6282	2N 6282	PMD-1601K
2N-6283	2N-6283	PMD-1602K
2N 6284	2N-6284	PMD-1603K

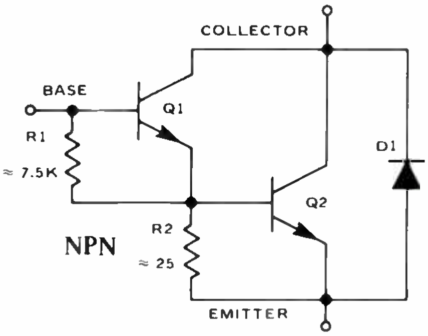
RCA PART NUMBER	LAMBDA EQUIVALENT	LAMBDA IMPROVED REPLACEMENT
2N-6282	2N-6282	PMD-16K-60
2N 6283	2N-6283	PMD-16K-80
2N-6284	2N-6284	PMD-16K-100
2N 6285	2N-6285	PMD-1701K
2N-6286	2N-6286	PMD-1702K
2N-6287	2N-6287	PMD-1703K
2N 6285	2N-6285	PMD-17K-60
2N-6286	2N-6286	PMD-17K-80
2N 6287	2N-6286	PMD 17K-100

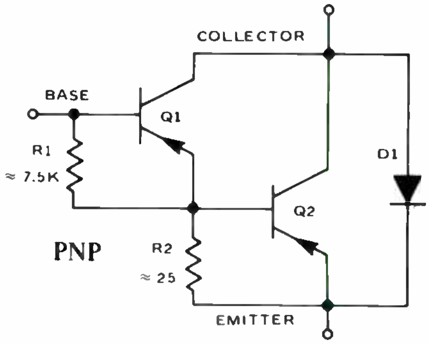
TEXAS INSTRUMENTS PART NUMBER	LAMBDA EQUIVALENT	LAMBDA IMPROVED REPLACEMENT
TIP-640	LTIP 640	PMD-10K-60
TIP 641	LTIP-641	PMD-10K-80
TIP-642	LTIP-642	PMD-10K-100
TIP-645	LTIP 645	PMD-11K-60
TIP 646	LTIP 646	PMD-11K-80
TIP 647	LTIP 647	PMD-11K-100

STANDARD COMMERCIAL PART NUMBER	LAMBDA EQUIVALENT	LAMBDA IMPROVED REPLACEMENT
2N-6057	2N 6057	PMD-10K-60
2N-6058	2N-6058	PMD-10K-80
2N 6059	2N 6059	PMD-10K-100
2N-6050	2N-6050	PMD-11K-60
2N-6051	2N-6051	PMD-11K-80
2N-6052	2N-6052	PMD-11K-100
2N 6055	2N 6055	PMD-12K-60
2N 6056	2N-6056	PMD 12K-80
2N-6053	2N 6053	PMD 13K-60
2N 6054	2N-6054	PMD-13K-80
2N 6383	2N-6383	PMD-12K-40
2N 6384	2N-6384	PMD-12K-60
2N 6385	2N 6385	PMD 12K-80

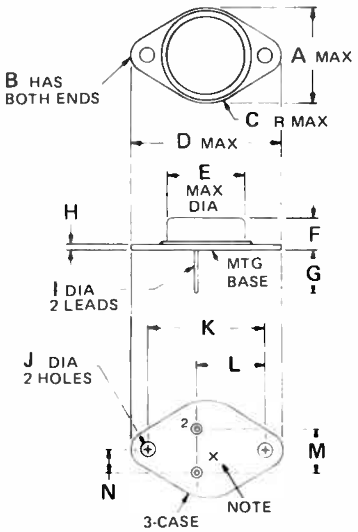
*ALL PMD DEVICES MEET 2N NUMBER SPECIFICATIONS AND HAVE GUARANTEED IMPROVED PERFORMANCE ON MANY SPECIFICATIONS.

⚠LAMBDA SCHEMATIC DIAGRAMS





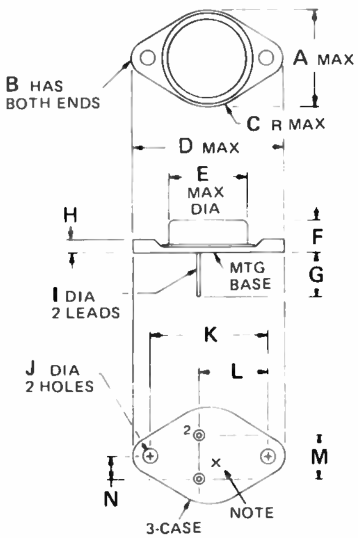
PACKAGE OUTLINE DRAWINGS AND PIN CONNECTIONS



PIN	FUNCTION
1	BASE
2	EMITTER
CASE	COLLECTOR

NOTE (X): CASE TEMPERATURE MEASURED AT THIS POINT

TO-3/3 TERMINAL STEEL PACKAGE				
	INCHES		MILLIMETERS	
DIM	MIN.	MAX.	MIN.	MAX.
A	–	1.050	–	26.67
B	–	0.188	–	4.77
C	–	0.525	–	13.33
D	–	1.575	–	40.00
E	–	0.875	–	22.22
F	0.250	0.450	6.35	11.43
G	0.433	0.480	10.99	12.19
H	0.053	0.066	1.34	1.67
I	0.036	0.043	0.91	1.09
J	0.151	0.160	3.83	4.14
K	1.177	1.197	29.89	30.40
L	0.655	0.675	16.63	17.14
M	0.418	0.440	10.61	11.17
N	0.205	0.225	5.20	5.71



PIN	FUNCTION
1	BASE
2	EMITTER
CASE	COLLECTOR

NOTE (X): CASE TEMPERATURE MEASURED AT THIS POINT

TO-3/3 TERMINAL COPPER PACKAGE*				
	INCHES		MILLIMETERS	
DIM	MIN.	MAX.	MIN.	MAX.
A	–	1.050	–	26.67
B	–	0.188	–	4.77
C	–	0.525	–	13.33
D	–	1.575	–	40.00
E	–	0.875	–	22.22
F	0.250	0.450	6.35	11.43
G	0.440	0.480	11.18	12.19
H	0.105	0.115	2.67	2.92
I	0.036	0.043	0.91	1.09
J	0.153	0.159	3.89	4.04
K	1.184	1.190	30.07	30.23
L	0.660	0.670	16.76	17.02
M	0.425	0.435	10.80	11.05
N	0.210	0.220	5.33	5.59

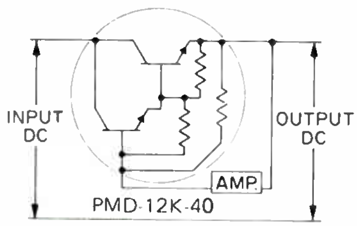
*FOR PMD 18K & 19K ONLY

ΛLAMBDA POWER

TYPICAL COST SAVINGS WITH LAMBDA DARLINGTONS

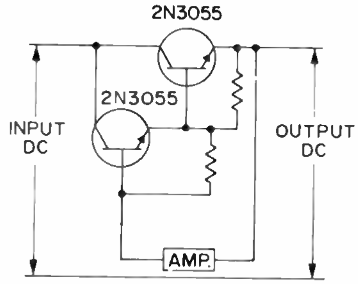
TYPICAL 4 AMP DC POWER SUPPLY CIRCUITS

Case 1:
1 PMD-12K-40 Darlington



Cost: **One Component $0.81**
No Assembly

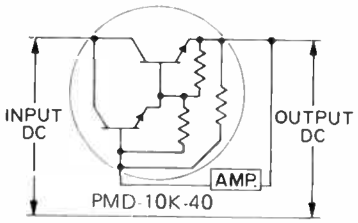
Case 2:
2-2N3055, 2 Resistors



Cost: **4 Components $1.02**
Plus Assembly

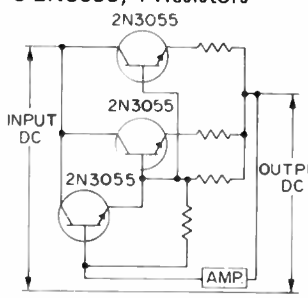
TYPICAL 6 AMP DC POWER SUPPLY CIRCUITS

Case 3:
1PMD-10-K-40 Darlington



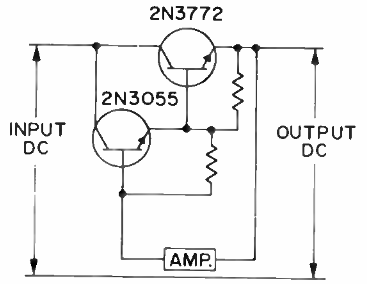
Cost: **One Component $1.39**

Case 4:
3-2N3055, 4 Resistors



Cost: **7 Components $2.33**
Plus Assembly

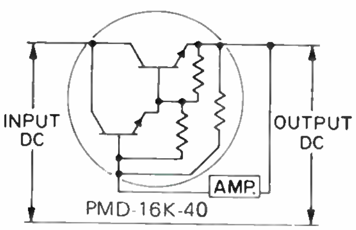
Case 5:
1-2N3772, 1-2N3055, 2 Resistors



Cost: **4 Components $2.36**
Plus Assembly

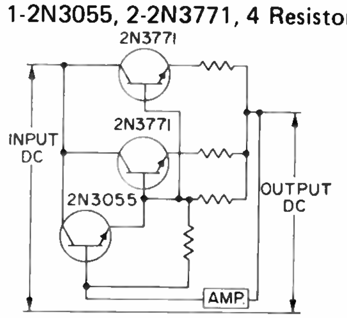
TYPICAL 10 AMP DC POWER SUPPLY CIRCUITS

Case 6:
1 PMD-16K-40 Darlington



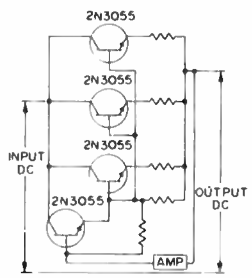
Cost: **One Component $3.24**
No Assembly

Case 7:
1-2N3055, 2-2N3771, 4 Resistors



Cost: **7 Components $4.73**
Plus Assembly

Case 8:
4-2N3055, 5 Resistors



Cost: **9 Components $3.64**
Plus Assembly

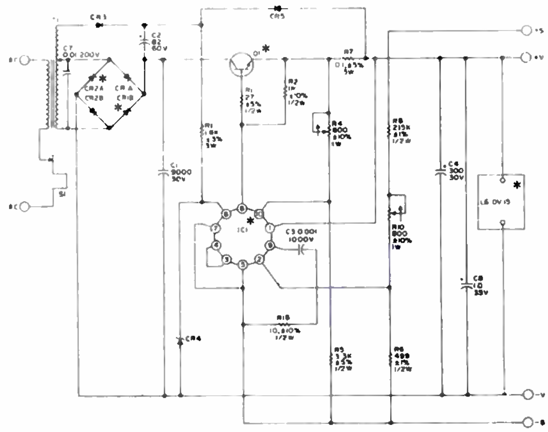
Estimated parts cost in quantities of 1000 at 2/79. Circuit conditions available on request. Component cost comparisons between ΛLAMBDA Darlingtons and discrete transistor designs using 2N3055 and 2N3771. Analysis based on 1000 piece price, similar savings apply for larger quantities.

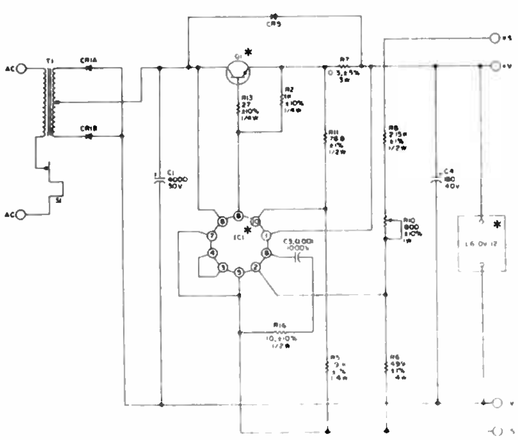
DARLINGTON TRANSISTORS

TYPICAL CIRCUIT APPLICATIONS

*LAMBDA MANUFACTURED PARTS
CR1A, B – PMR 27K 100
CR2A, B – PMR 31K 100
Q1 – PMD 10K 60
IC1 – LAS 1100
OV–L6 OV 15

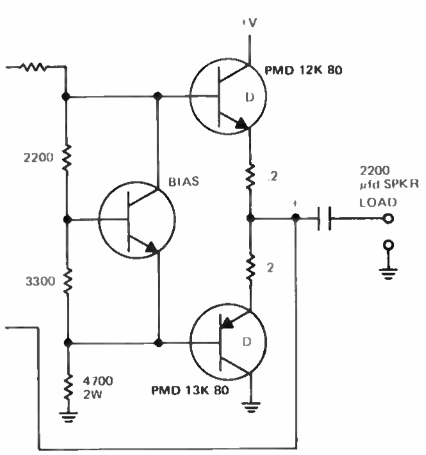
LNS-Y-15
15V @ 3.4A
(OV added)



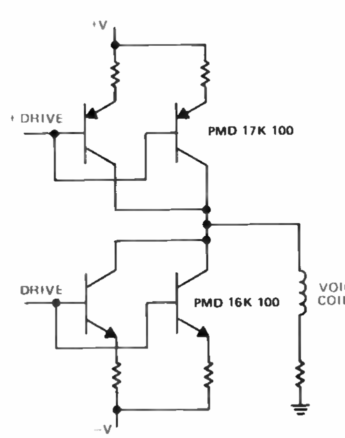


*LAMBDA MANUFACTURED PARTS
CR1A, B – PMR 31K 100
Q1 – PMD 12K 60
IC1 – LAS 1100
OV–L6 OV 12

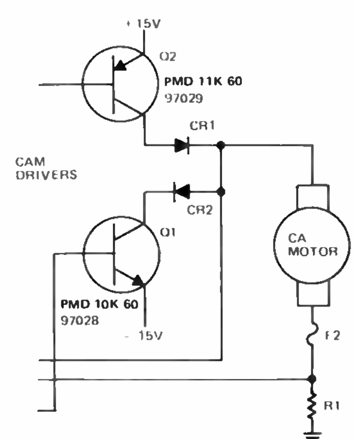
LNS-Z-12
12V @ 1.7A
(OV added)



CLASS AB AMPLIFIER



DISC DRIVE FOR COMPUTERS



MOTOR DRIVE

ΔLambda PMD 10K, 12K, 16K, 1600K, 18K Series of NPN Power Transistor Darlingtons

ELECTRICAL CHARACTERISTICS

ALL PARAMETERS ARE GUARANTEED AT T_J of 0°C to 200°C, UNLESS OTHERWISE SPECIFIED

DEVICE TYPE	TEST	SYMBOL		TEST CONDITIONS	MIN.	MAX.	UNITS	NOTE
PMD-10K SERIES PMD 12K SERIES PMD-16K SERIES PMD-1600K SERIES PMD-18K SERIES	Collector Emitter Saturation Voltage	V_{CE}(Sat)	ON Characteristics	I_c=6Adc, I_B=24MAdc I_c=4Adc, I_B=16MAdc I_c=10Adc, I_B=40MAdc I_c=10Adc, I_B=40MAdc I_c=15Adc, I_B=60MAdc		2.0	Vdc	1
PMD-10K SERIES PMD-12K SERIES PMD 16K SERIES PMD 1600K SERIES PMD-18K SERIES	Base Emitter Turn-on Voltage	V_{BE}(on)	ON Characteristics	Ic = 6Adc Ic = 4Adc Ic = 10Adc Ic = 10Adc Ic = 15Adc V_{CE} = 3Vdc		2.8	Vdc	1
PMD-10K SERIES PMD 12K SERIES PMD-16K SERIES PMD 1600K SERIES PMD-18K SERIES	Base Emitter Saturation Voltage	V_{BE}(Sat)	ON Characteristics	Ic=6Adc, I_B=24MAdc Ic=4Adc, I_B=16MAdc Ic=10Adc, I_B=40MAdc Ic=10Adc, I_B=40MAdc Ic=15Adc, I_B=60MAdc		2.8	Vdc	1
PMD-10K SERIES PMD-12K SERIES PMD-16K SERIES PMD-1600K SERIES PMD-18K SERIES	DC Current Gain	h_{FE}	ON Characteristics	Ic=6Adc Ic=4Adc Ic=10Adc Ic=10Adc Ic=15Adc V_{CE} = 3Vdc	1000 1000 1000 750 1000	20,000		1
PMD-10K SERIES PMD 12K SERIES PMD-16K SERIES PMD 1600K SERIES PMD-18K SERIES	Forward Bias Second Breakdown current	$I_{s/b}$	ON Characteristics	T_A 25°C V_{CE} 30Vdc 1 second nonrepetitive pulse	5.0 3.0 7.5 6.0 8.0		Adc	1
PMD-10K, 12K 16K, 18K-40 PMD 1600K PMD-10K, 12K 16K, 18K-60 PMD-1601K PMD-10K, 12K, 16K, 18K-80 PMD-1602 PMD 10K, 12K, 16K, 18K-100 PMD 1603K	Collector Emitter Breakdown Voltage (Base Open)	$V_{(BR)CEO}$	OFF Characteristics	I_{CE} 100MAdc T_J=25°C	40 60 80 100		Vdc	
PMD 10K, 12K, 16K, 18K-40 PMD-1600K PMD-10K, 12K, 16K, 18K-60 PMD-1601K PMD-10K, 12K 16K, 18K-80 PMD 1602K PMD 10K, 12K, 16K, 18K-100 PMD-1603K	Collector Emitter Sustaining Voltage	$V_{(BR)CER}$ (sus)	OFF Characteristics	I_{CE} 100MAdc R_{BE} 2.2K ohms	40 60 80 100		Vdc	
All NPN Series	Emitter Base Leakage Current	I_{EBO}	OFF Characteristics	V_{EB}=5Vdc I_C=0A		3.0	MAdc	
PMD-10K, 12K-40 PMD-10K, 12K 60 PMD-10K, 12K-80 PMD 10K, 12K-100	Collector Emitter Leakage Current	I_{CER}	OFF Characteristics	V_{CE}=20Vdc V_{CE}=40Vdc V_{CE}=54Vdc V_{CE}=67Vdc R_{BE} 2.2Kohms		5 0 5 0 5 0 5 0	MAdc	

continued on next page

ELECTRICAL CHARACTERISTICS (continued)

DEVICE TYPE	TEST	SYMBOL		TEST CONDITIONS		MIN.	MAX.	UNITS	NOTE
PMD-16K-40 PMD-1600K	Collector Emitter Leakage Current	I_{CER}	OFF Characteristics	$V_{CE}=20Vdc$	$R_{BE}=$ 2.2K ohms		7.0	MAdc	
PMD-16K-60 PMD 1601K				$V_{CE}=40Vdc$					
PMD-16K 80 PMD-1602K				$V_{CE}=54Vdc$					
PMD 16K 100 PMD-1603K				$V_{CE}=67Vdc$					
PMD 18K-40				$V_{CE}=20Vdc$			10.0		
PMD 18K-60				$V_{CE}=40Vdc$					
PMD 18K 80				$V_{CE}=54Vdc$					
PMD 18K 100				$V_{CE}=67Vdc$					
PMD-10K SERIES	Output Capacitance	C_{ob}	Dynamic Characteristics	$V_{CB}=10Vdc$, $I_E=0Adc$ $f=1$ MHz $T_J=25°C$			300	pf	
PMD-12K SERIES							200		
PMD-16K SERIES							400		
PMD 1600K SERIES							400		
PMD 18K SERIES							600		
PMD 10K SERIES	Small Signal Current Gain	h_{fe}		$I_C=5Adc$	$V_{CE}=3Vdc$ $f=1kHz$ $T_J=25°C$	300			
PMD-12K SERIES				$I_C=3Adc$					
PMD-16K SERIES				$I_C=7Adc$					
PMD-1600K SERIES				$I_C=7Adc$					
PMD-18K SERIES				$I_C=9Adc$					
PMD-10K SERIES	Common Emitter Short Circuit Forward Transfer Ratio	h_{fe}		$I_C=5Adc$	$V_{CE}=3Vdc$ $f=1MHz$ $T_J=25°C$	4			
PMD-12K SERIES				$I_C=3Adc$					
PMD 16K SERIES				$I_C=7Adc$					
PMD 1600K SERIES				$I_C=7Adc$					
PMD 18K SERIES				$I_C=9Adc$					

NOTES.

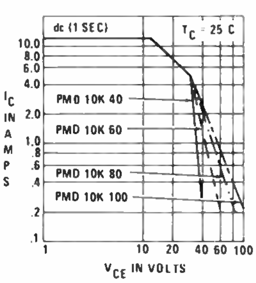
1. Pulse Tested: Pulse Width is less than or equal to 300 uSec. and the Duty Cycle is less than or equal to 2.0%.

DEVICE PRICES, SPECIFICATIONS, AND CONFIGURATIONS ARE SUBJECT TO CHANGE WITHOUT NOTICE

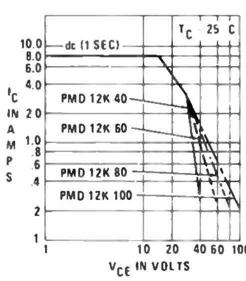
OPERATIONAL DATA

SAFE OPERATING AREA

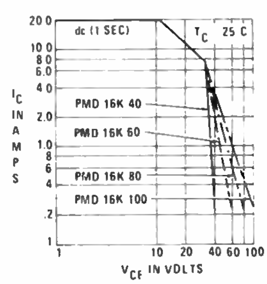
PMD 10K SERIES



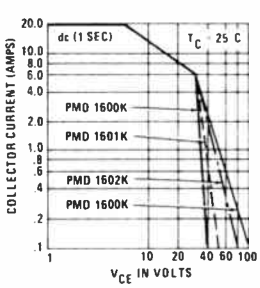
PMD 12K SERIES



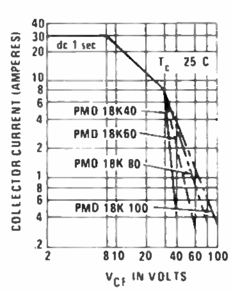
PMD 16K SERIES



PMD 1600K SERIES

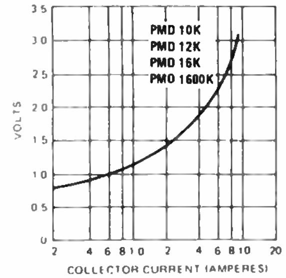


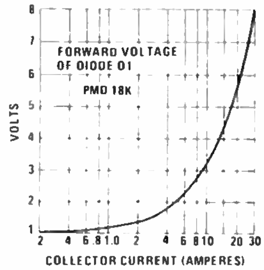
PMD 18K SERIES

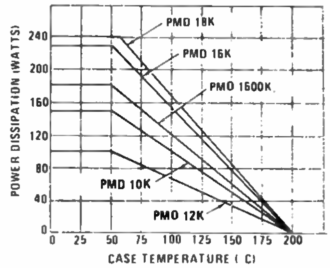


OPERATIONAL DATA (continued)

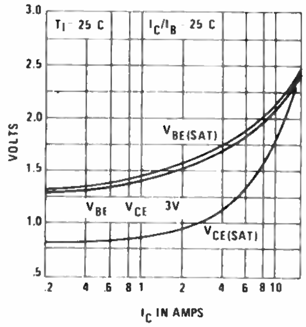
POWER DERATING



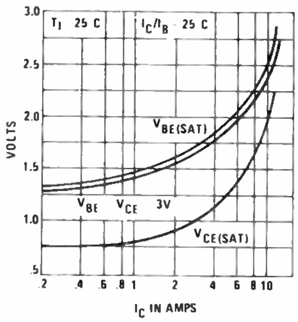




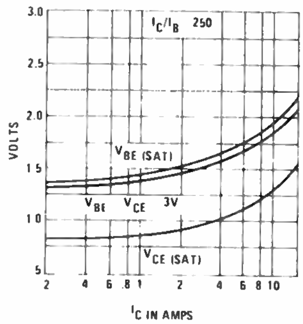
"ON" VOLTAGES VERSUS COLLECTOR CURRENT



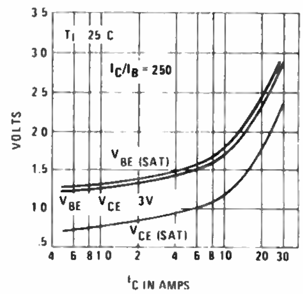
PMD 10K SERIES



PMD 12K SERIES

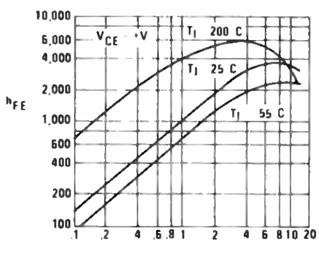


PMD 16K, 1600K SERIES

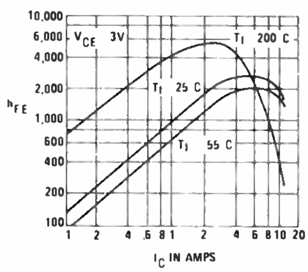


PMD 18K SERIES

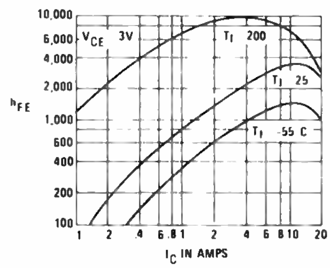
DC COLLECTOR CURRENT GAIN VERSUS COLLECTOR CURRENT



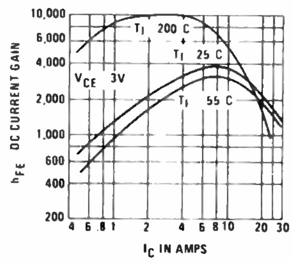
PMD 10K SERIES



PMD 12K SERIES

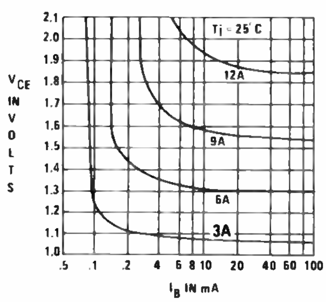


PMD 16K, 1600K SERIES

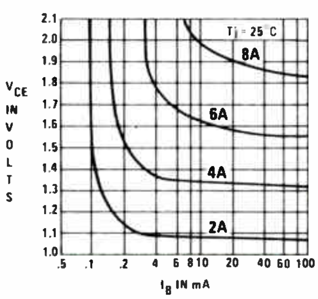


PMD 18K SERIES

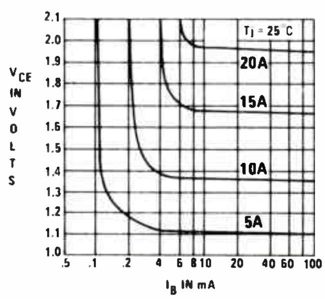
COLLECTOR SATURATION REGION



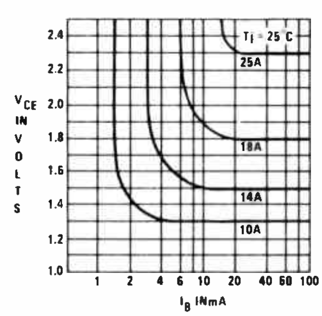
PMD 10K SERIES



PMD 12K SERIES



PMD 16K, 1600K SERIES



PMD 18K SERIES

△Lambda PMD 11K, 13K, 17K, 1700K, 19K Series of PNP Power Transistor Darlingtons

ELECTRICAL CHARACTERISTICS

ALL PARAMETERS ARE GUARANTEED AT T_J of 0°C to 200°C, UNLESS OTHERWISE SPECIFIED

DEVICE TYPE	TEST	SYMBOL		TEST CONDITIONS		MIN.	MAX.	UNITS	NOTE
PMD-11K SERIES PMD 13K SERIES PMD-17K SERIES PMD-1700K SERIES PMD-19K SERIES	Collector Emitter Saturation Voltage	V_{CE}(Sat)	ON Characteristics	I_C=6Adc; I_B=24MAdc I_C=4Adc, I_B=16MAdc I_C=10Adc, I_B=40MAdc I_C=10Adc; I_B=40MAdc I_C=15Adc, I_B=60MAdc			2.0	Vdc	1
PMD-11K SERIES PMD-13K SERIES PMD-17K SERIES PMD 1700K SERIES PMD-19K SERIES	Base Emitter Turn-on Voltage	V_{BE}(on)	ON Characteristics	I_C = 6Adc I_C = 4Adc I_C = 10Adc I_C = 10Adc I_C = 15Adc	V_{CE} = 3Vdc		2.8	Vdc	1
PMD-11K SERIES PMD-13K SERIES PMD-17K SERIES PMD 1700K SERIES PMD-19K SERIES	Base Emitter Saturation	V_{BE}(Sat)	ON Characteristics	I_C=6Adc, I_B=24MAdc I_C=4Adc; I_B=16MAdc I_C=10Adc, I_B=40MAdc I_C=10Adc; I_B=40MAdc I_C=15Adc; I_B=60MAdc			2.8	Vdc	1
PMD 11K SERIES PMD-13K SERIES PMD 17K SERIES PMD 1700K SERIES PMD 19K SERIES	DC Current Gain	h_{FE}	ON Characteristics	I_C=6Adc I_C=4Adc I_C=10Adc I_C=10Adc I_C=15Adc	V_{CE} = 3Vdc	800 800 800 750 800	20,000		1
PMD 11K SERIES PMD 13K SERIES PMD 17K SERIES PMD 1700K SERIES PMD-19K SERIES	Forward Bias Second Breakdown current	$I_{s/b}$		T_A=25°C V_{CE} 30Vdc 1 second nonrepetitive pulse		5.0 3.0 7.5 6.0 8.0		Adc	1
PMD 11K, 13K, 17K, 19K-40 PMD 1700K PMD 11K, 13K, 17K, 19K 60 PMD 1701K PMD 11K, 13K, 17K, 19K 80 PMD 1702 PMD 11K, 13K, 17K, 19K 100 PMD 1703K	Collector Emitter Breakdown Voltage (Base Open)	$V_{(BR)CEO}$	OFF Characteristics	I_{CE} 100MAdc T_J 25°C		40 60 80 100		Vdc	
PMD 11K, 13K, 17K, 19K-40 PMD 1700K PMD 11K, 13K, 17K, 19K 60 PMD 1701K PMD 11K, 13K, 17K, 19K 80 PMD 1702K PMD 11K, 13K, 17K, 19K 100 PMD 1703K	Collector Emitter Sustaining Voltage	$V_{(BR)CER}$ (sus)	OFF Characteristics	I_{CE}=100MAdc R_{BE} 2.2K ohms		40 60 80 100		Vdc	
All PNP Series	Emitter Base Leakage Current	I_{EBO}	OFF Characteristics	V_{EB} 5Vdc I_C 0A			3.0	MAdc	
PMD 11K, 13K 40 PMD 11K, 13K 60 PMD 11K, 13K-80 PMD 11K, 13K-100	Collector Emitter Leakage Current	I_{CER}	OFF Characteristics	V_{CE} 20Vdc V_{CE} 40Vdc V_{CE} 54Vdc V_{CE} 67Vdc	R_{BE} = 2.2 Kohms		5.0 5.0 5.0 5.0	MAdc	

continued on next page

ELECTRICAL CHARACTERISTICS (continued)

DEVICE TYPE	TEST	SYMBOL		TEST CONDITIONS		MIN.	MAX.	UNITS	NOTE
PMD 17K 40 PMD 1700K	Collector Emitter Leakage Current	I_{CER}	OFF Characteristics	$V_{CE}=20Vdc$	$R_{BE}=2.2K_{ohms}$		7.0	MAdc	
PMD 17K-60 PMD 1701K				$V_{CE}=40Vdc$					
PMD 17K-80 PMD 1702K				$V_{CE}=54Vdc$					
PMD 17K 100 PMD 1703K				$V_{CE}=67Vdc$					
PMD 19K 40				$V_{CE}=20Vdc$			10.0		
PMD 19K 60				$V_{CE}=40Vdc$					
PMD 19K 80				$V_{CE}=54Vdc$					
PMD 19K 100				$V_{CE}=67Vdc$					
PMD 11K SERIES	Output Capacitance	Cobo	Dynamic Characteristics	$V_{CB}=10Vdc$, $I_E=0Adc$ f=1 MHz $T_J=25^\circ C$			300	pf	
PMD 13K SERIES							200		
PMD 17K SERIES							400		
PMD 1700K SERIES							400		
PMD 19K SERIES							600		
PMD 11K SERIES	Small Signal Current Gain	h_{fe}		$I_C=5Adc$	$V_{CE}=3Vdc$ f=1kHz $T_J=25^\circ C$	300			
PMD 13K SERIES				$I_C=3Adc$					
PMD 17K SERIES				$I_C=7Adc$					
PMD 1700K SERIES				$I_C=7Adc$					
PMD 19K SERIES				$I_C=9Adc$					
PMD 11K SERIES	Common Emitter Short-Circuit Forward Transfer Ratio	h_{fe}		$I_C=5Adc$	$V_{CE}=3Vdc$ f=1MHz $T_J=25^\circ C$	4			
PMD 13K SERIES				$I_C=3Adc$					
PMD 17K SERIES				$I_C=7Adc$					
PMD 1700K SERIES				$I_C=7Adc$					
PMD 19K SERIES				$I_C=9Adc$					

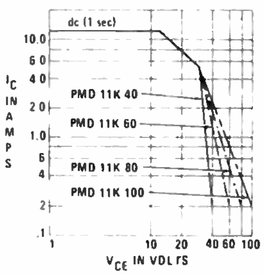
NOTES.
1. Pulse Tested Pulse Width is less than or equal to 300 uSec. and the Duty Cycle is less than or equal to 2.0%.

DEVICE PRICES, SPECIFICATIONS, AND CONFIGURATIONS ARE SUBJECT TO CHANGE WITHOUT NOTICE

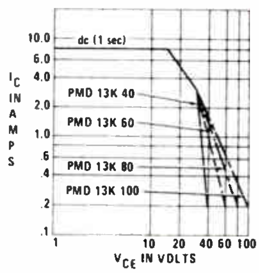
OPERATIONAL DATA

SAFE OPERATING AREA

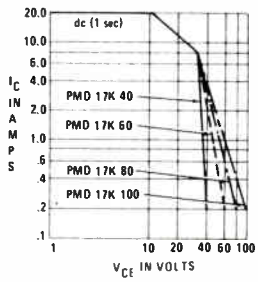
PMD 11K SERIES



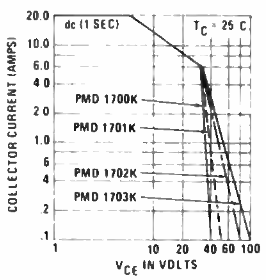
PMD 13K SERIES



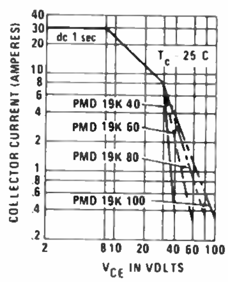
PMD 17K SERIES



PMD 1700K SERIES

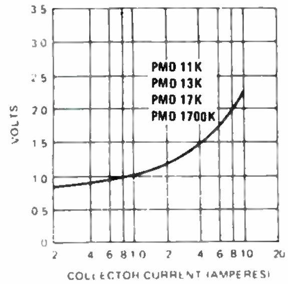


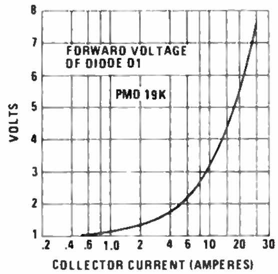
PMD 19K SERIES

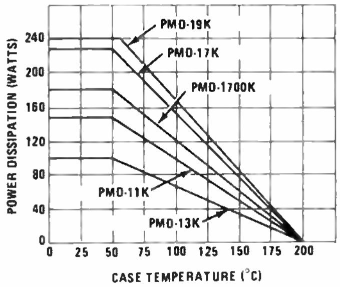


OPERATIONAL DATA (continued)

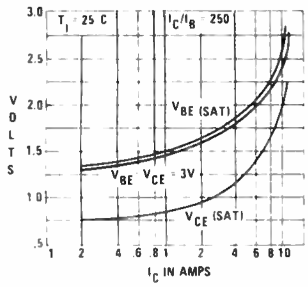
POWER DERATING



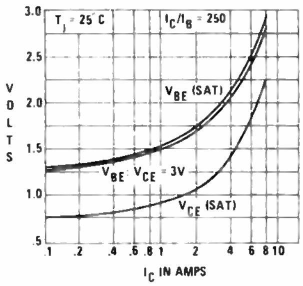




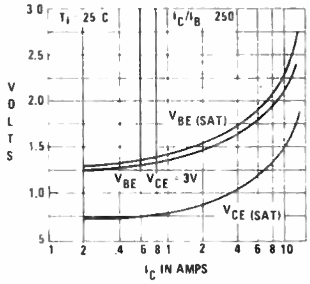
"ON" VOLTAGES VERSUS COLLECTOR CURRENT



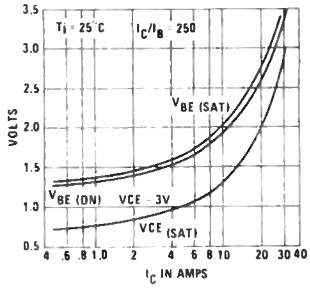
PMD 11K SERIES



PMD 13K SERIES

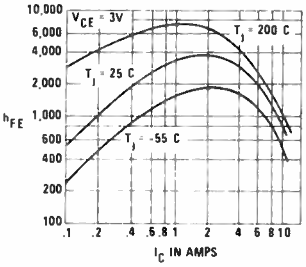


PMD 17K, 1700K SERIES



PMD 19K SERIES

DC COLLECTOR CURRENT GAIN VERSUS COLLECTOR CURRENT



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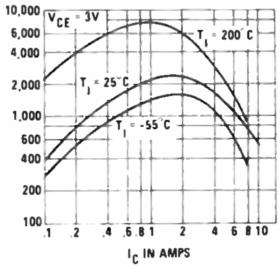
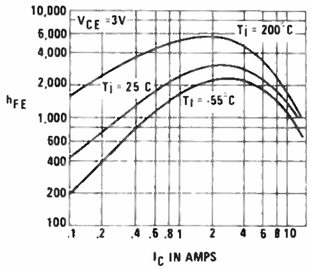
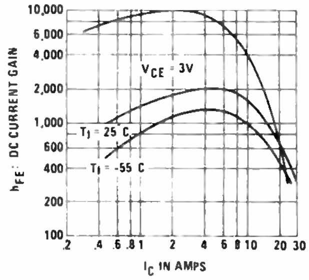


PMD 13K SERIES

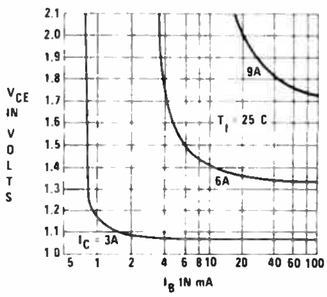


PMD 17K, 1700K SERIES

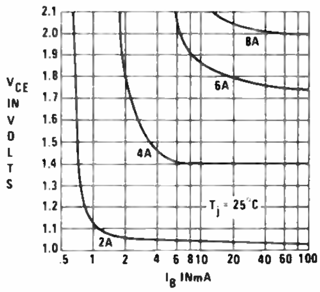


PMD 19K SERIES

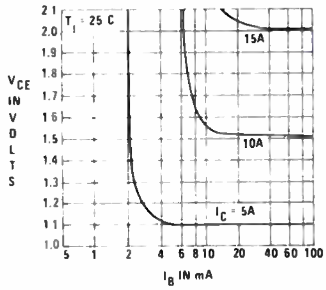
COLLECTOR SATURATION REGION



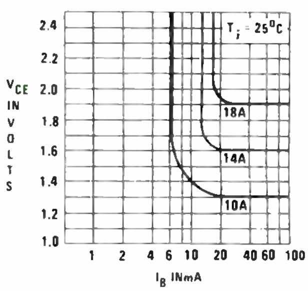
PMD 11K SERIES



PMD 13K SERIES



PMD 17K, 1700K SERIES



PMD 19K SERIES

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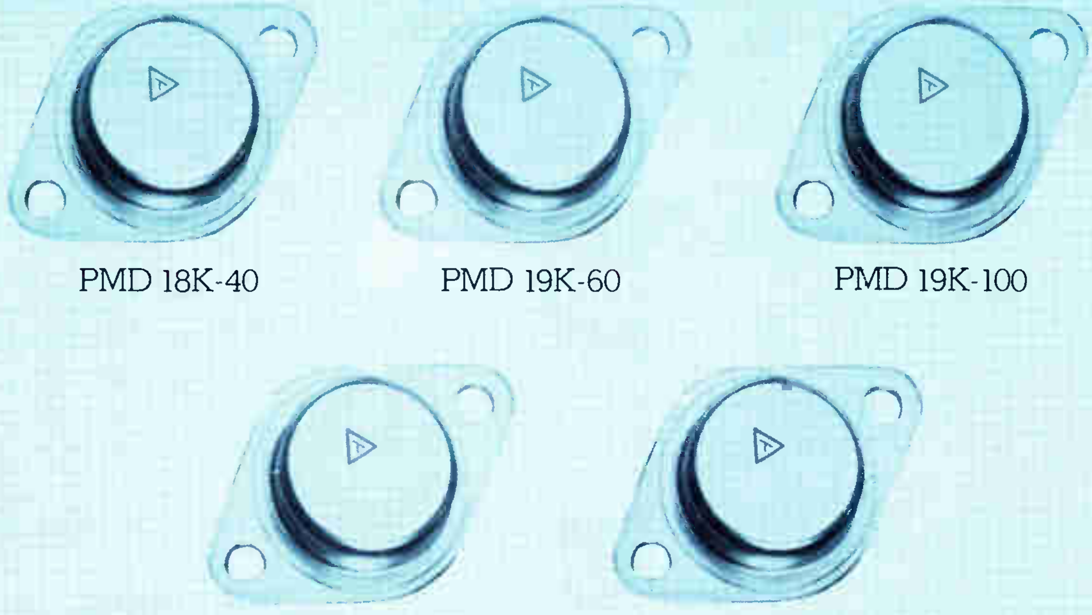

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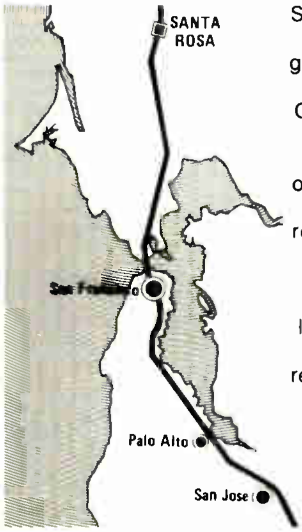

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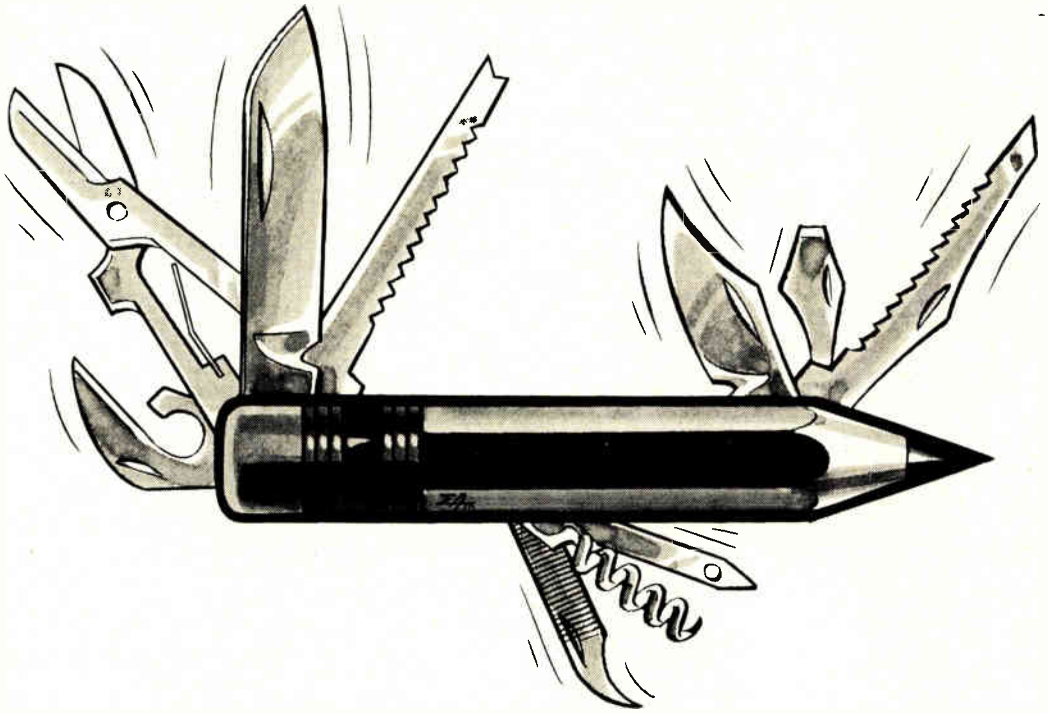

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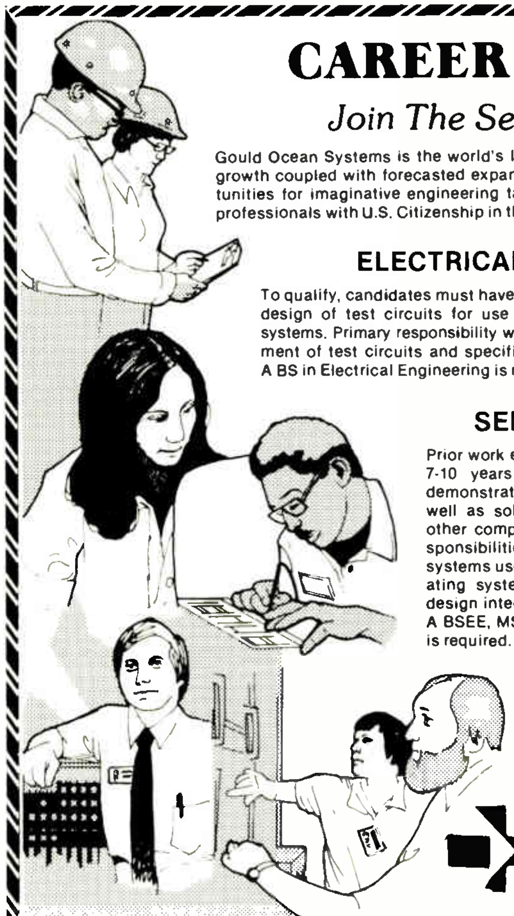

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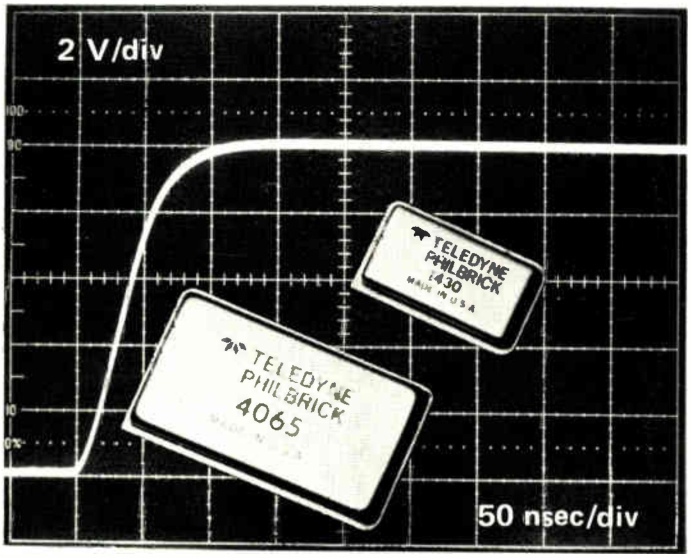

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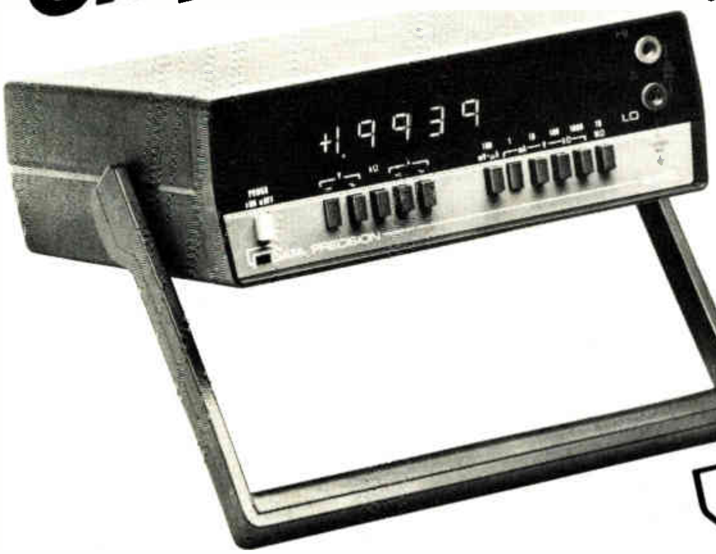

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3. Engineering services (evaluation, quality control, reliability, standards, test)
4. Basic research
5. Manufacturing and production
6. Engineering support (lab assistant, technician)
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4. ☐ Indicate your principal job responsibility (place applicable number in box)

1. Management 2. Engineering

5. ☐☐☐ **Your design function:** *(Insert each letter that applies)*

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B. I supervise electronic design or development engineering work
C. I set standards for, or evaluate electronic design components, systems and materials

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z ☐ I set standards for, or evaluate electronic components, systems and materials.

Your principal job responsibility (check one)

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