FEBRUARY 14, 1980

VLSI PACKS THEM IN AT ISSCC IN SAN FRANCISCO/138

Carter's budget: who will get the increases?/99

Serial communications processor simplifies data-acquisition system/127

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Electronics

The International Magazine of Electronic Technology

Vol. 53, No. 4 • February 14, 1980

Highlights

Cover: Chip reflects minicomputer's architecture and speed, 119

Matching the throughput of a high-end minicomputer built with TTL is no mean feat for an n-channel MOS microprocessor. The 16-bit microEclipse does just that, however, while executing a kernel of the Eclipse instruction set. The one-chip central processor and its associated hardware represent a new invasion by high-level integrated silicon of turf long occupied by large, power-hungry systems composed of thousands of discrete and lower-level integrated components.

Cover illustration is by Ron Chironna.

Microcomputer enslaved for serial remote data acquisition, 127

The general-purpose 3870's independence has been sacrificed so that it (and up to 254 others in a system) might perform remote data acquisition or control, responding to serial commands on a single half-duplex channel. The microcomputer's programmed supervisory and input/output commands are geared to a character-oriented data-communications protocol.

ISSCC offers initiation to VLSI future, 138

Mammoth chips, many of which will be some years in reaching commercial production, were unchained at this year's ISSCC. They include quarter- and half-megabit random-access memories and complete one-chip systems for telecommunications, signal processing, data acquisition, and more.

60-watt switching power supply meets tight budget, 154

The last bastion of linear power supplies—low-power, low-cost applications—has been breached by the efficient, lightweight switching approach. This example's ingredients (flyback transformer, control chip, nuts and bolts) can all be had for $37, when purchased in 1,000-unit lots.

Software arrives for adaptive data networks, 183

Data-communications networks capable of adaptive routing are by all accounts the wave of the future, but Digital Equipment Corp. is diving in head first right now. The minicomputer maker's Phase III DECnet is a packet-switching system that sends data via the least expensive functioning route.

. . . and in the next issue

An electrically erasable programmable read-only memory achieves high density . . . a functionally complete monolithic digital-to-analog converter operates on a single +5-volt supply . . . thermal processing with a production laser unit tightens chip parameters . . . a microprocessor development system paves the way to an integrated design center for very large-scale integrated circuits.

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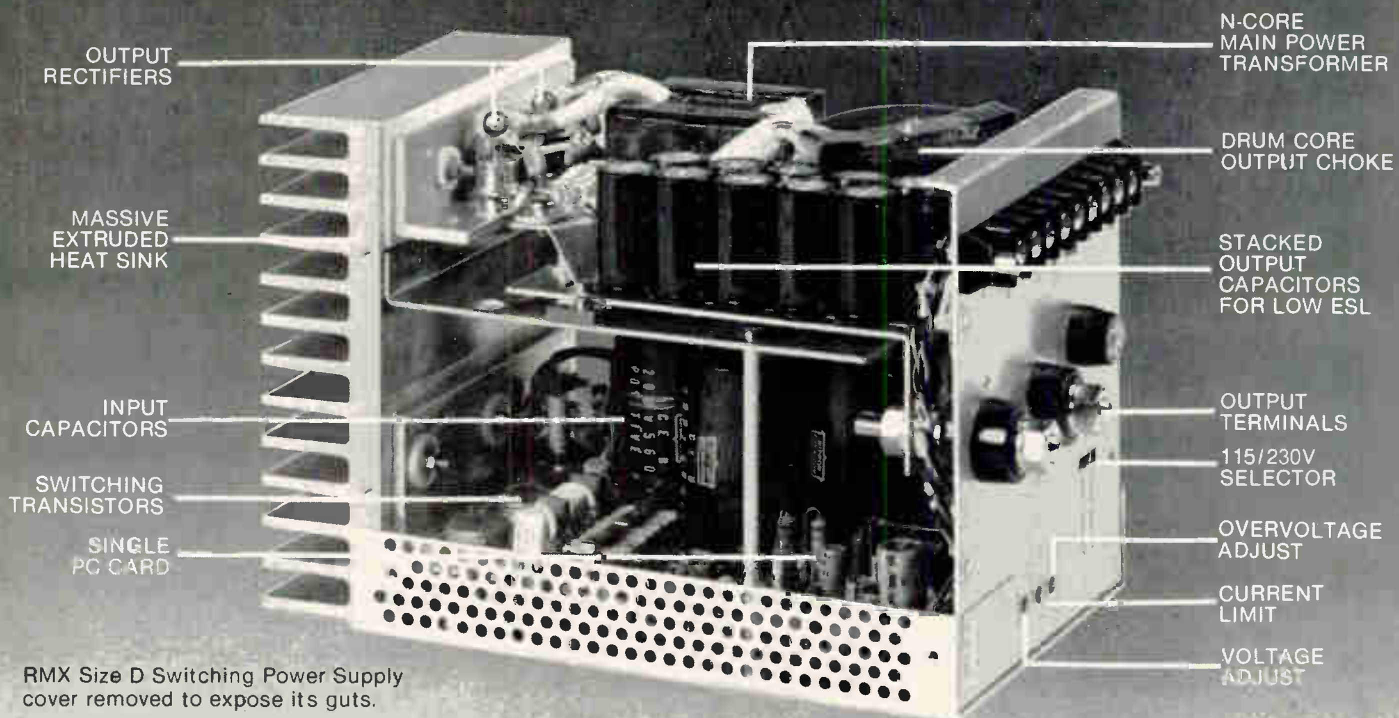

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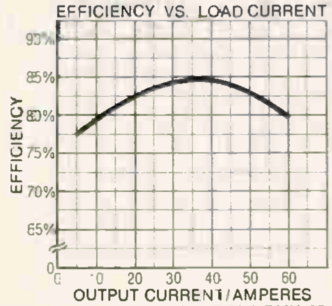
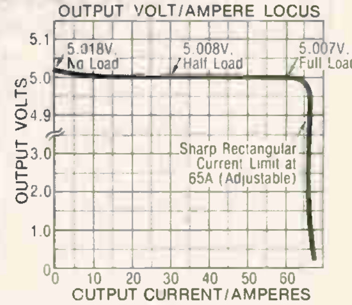
RMX 24-D	16.8–26.4	16A
RMX 28-D	19.6–30.8	13.7A





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VLSI at work. That's one of the themes to emerge from this year's International Solid State Circuits Conference, Feb. 13–15, in San Francisco. The comprehensive roundup (p. 138) put together by solid state editor John Posa and components editor Roger Allan took a couple of months of steady effort starting from the day the program became available.

To cover the 27th annual conference, John and Roger collected, read, and evaluated nearly 100 technical papers. In addition, each editor talked to dozens of authors. Because the program is international in scope, our overseas bureaus also got into the act. And, as John and Roger point out, the whole thing could not have come off without the cooperation of ISSCC organizer Lew Winner and program chairman James Plummer of Stanford Research International, Palo Alto, Calif.

"To me the program is impressive because it shows that VLSI is happening and viable," John observes. "The ISSCC presents papers on developments that are in working prototypes and as such provides a preview of the products to follow."

To Roger, the conference also marks the increased importance of analog design. "Some big names in solid-state design are represented by papers on analog developments. The whole field is catching up to digital chips," he reports.

Another trend on the program is the growing presence of Japanese papers, especially in the memory category. Among the dazzlers from engineering labs in Japan are descriptions of 256-K and larger random-access memories and a 64-K static RAM. John points out that the Japanese appear to be at home with the latest advanced processing such as electron-beam lithography and ion etching. Roger adds that the Japanese papers on telecommunications chips—codecs and filters—underscore the extent to which these devices are being applied in Japan.

It's Federal budget time, and once again Washington bureau manager Ray Connolly has lugged home the heavy volumes presenting President Carter's spending plans in order to analyze what electronics might get. The result (p. 95) looks pretty good if the Congress goes along with the Administration's budget. Defense spending is going up as expected.

As usual the DOD gets the lion's share of the R&D budget. At $16.6 billion the fiscal 1981 allotment would increase by $2.8 billion, or 20%, over fiscal 1980. The National Science Foundation's budget would go up 15.5% to over $1 billion.

But with the increase in spending will come the problem of finding and training more electrical engineers at a time when the defense industry is short of experienced EEs. Gearing up for what Ray refers to as Cold War II poses a difficult problem for the future. Let's not forget what happened in the 1960s when this country began turning out large numbers of engineers for aerospace and defense needs. Certainly the engineers who were laid off after that bubble burst in the 1970s will not forget.

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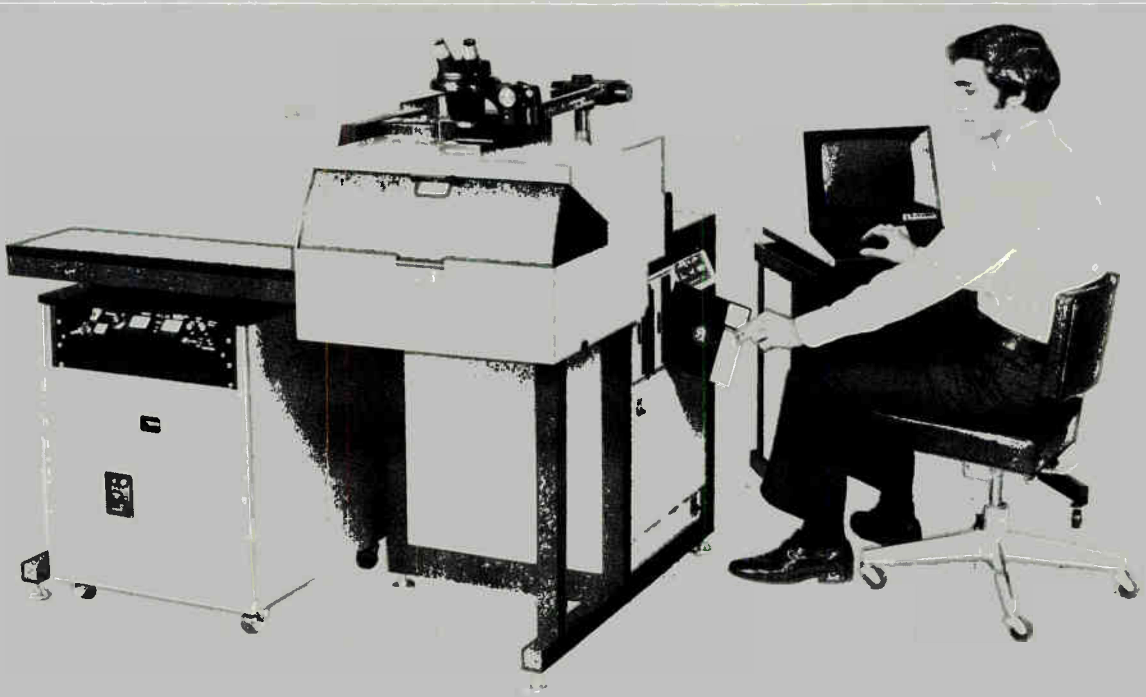
Just as the powerful software reduces programming time and personnel costs, the maintenance ease of the CLS-33 ensures low long-term costs. This system can be easily maintained by your maintenance staff. Training is quick and free to CLS customer personnel.

A variety of complementary parts handling mechanisms are available for the CLS-33. Fed by the recently introduced air-bearing Step-and Repeat Handler, the CLS-33 trims an incredible 100,000 resistors per hour. At the same time, the simple sophistication that has established Chicago Laser as a leader in the laser trim industry has been maintained. The handler is also available with stack load and unload to minimize operator support.

CLS 33



The Chicago Laser Systems CLS-33 is the smart way to solve your network or hybrid trimming problems. For the complete story and a frank appraisal of how the CL-33 can fulfill your needs, contact Chicago Laser Systems Inc.

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Circle 7 on reader service card

Readers' comments

Let it be

To the Editor: I want to reply to Robert Gaebler's letter on expression format in the Forth language [July 5, 1979, p. 6].

Gaebler notes, and I agree, that compilers can do the translation from infix to postfix notation and thus save the programmer both work and the risk of errors. Unfortunately, these advantages are not available without some penalty for extensible languages such as Forth. If the compiler is to translate, it must know how to parse expressions. The parsing rules for primitive operators are supplied with the compiler, but those for the added operators must be supplied by the programmer at compile time, which makes the basic parser much more complicated.

Examination of almost any program will reveal that the majority of program statements are nonalgebraic or can easily be converted to a nonalgebraic form. Thus the advantages of infix notation, when present, apply only to a fraction of the program statements. For most function definitions, the prefix notation of subroutine or macro calls is required, and this can be replaced by postfix notation with little or no loss of clarity.

Use of postfix notation leaves the parsing of all expressions in the hands of the programmer. It means that arguments for an operator may be prepared using the full power of the programming language, without any restrictions being imposed by the compiler. With this freedom comes the possibility of error, and argument preparation is one of the most error-prone portions of programming in a language such as Forth. If effort is to be spent on improving the ease of programming, it should be spent on simplifying argument preparation and stack manipulation. Postfix notation, with the applicative style of programming that it produces, has so many advantages that it should not be sacrificed to an algebraic notation that is not 'natural,' but only something we all learned in school.

Edward B. Rawson
Lincoln, Mass.

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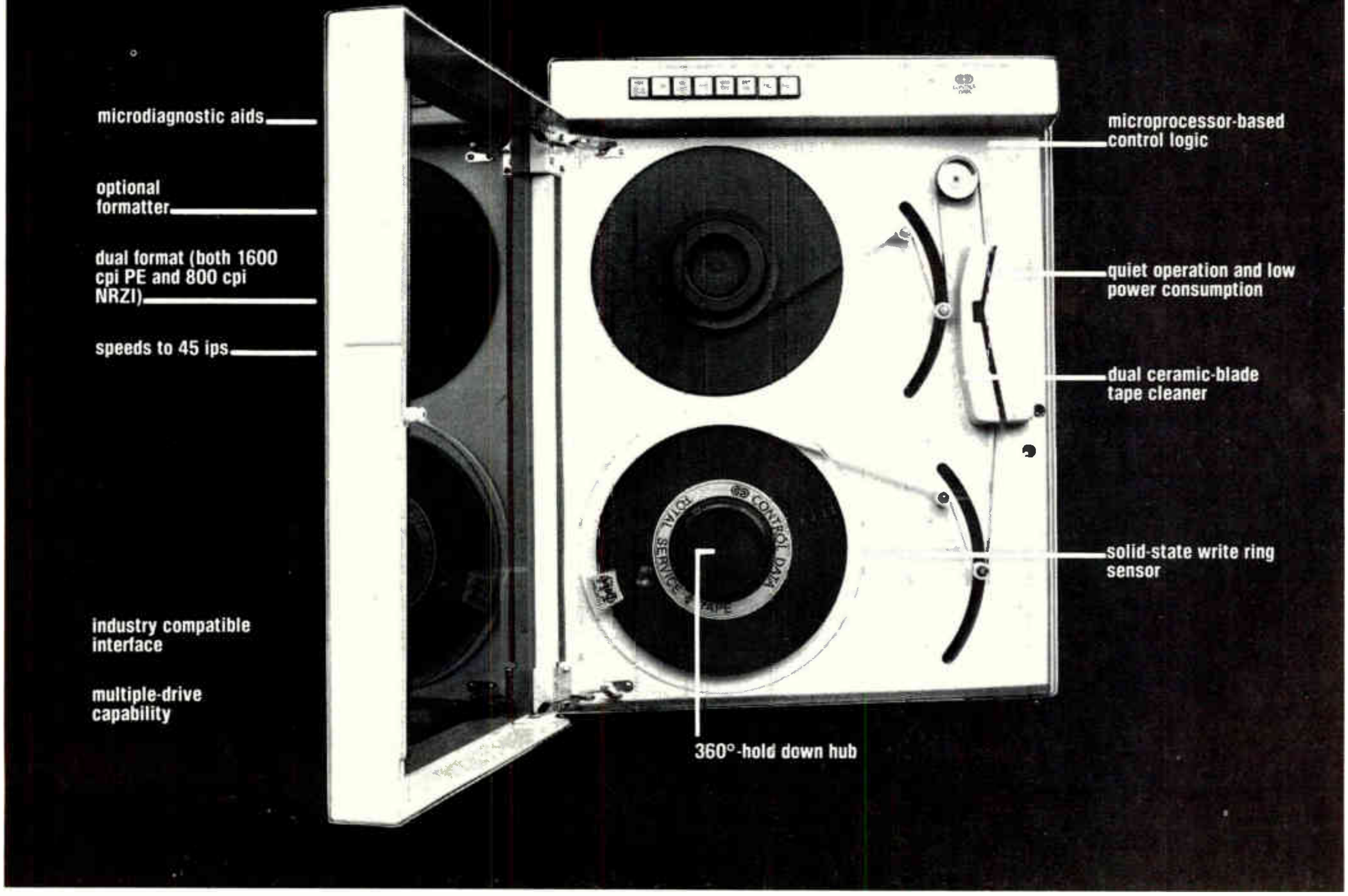

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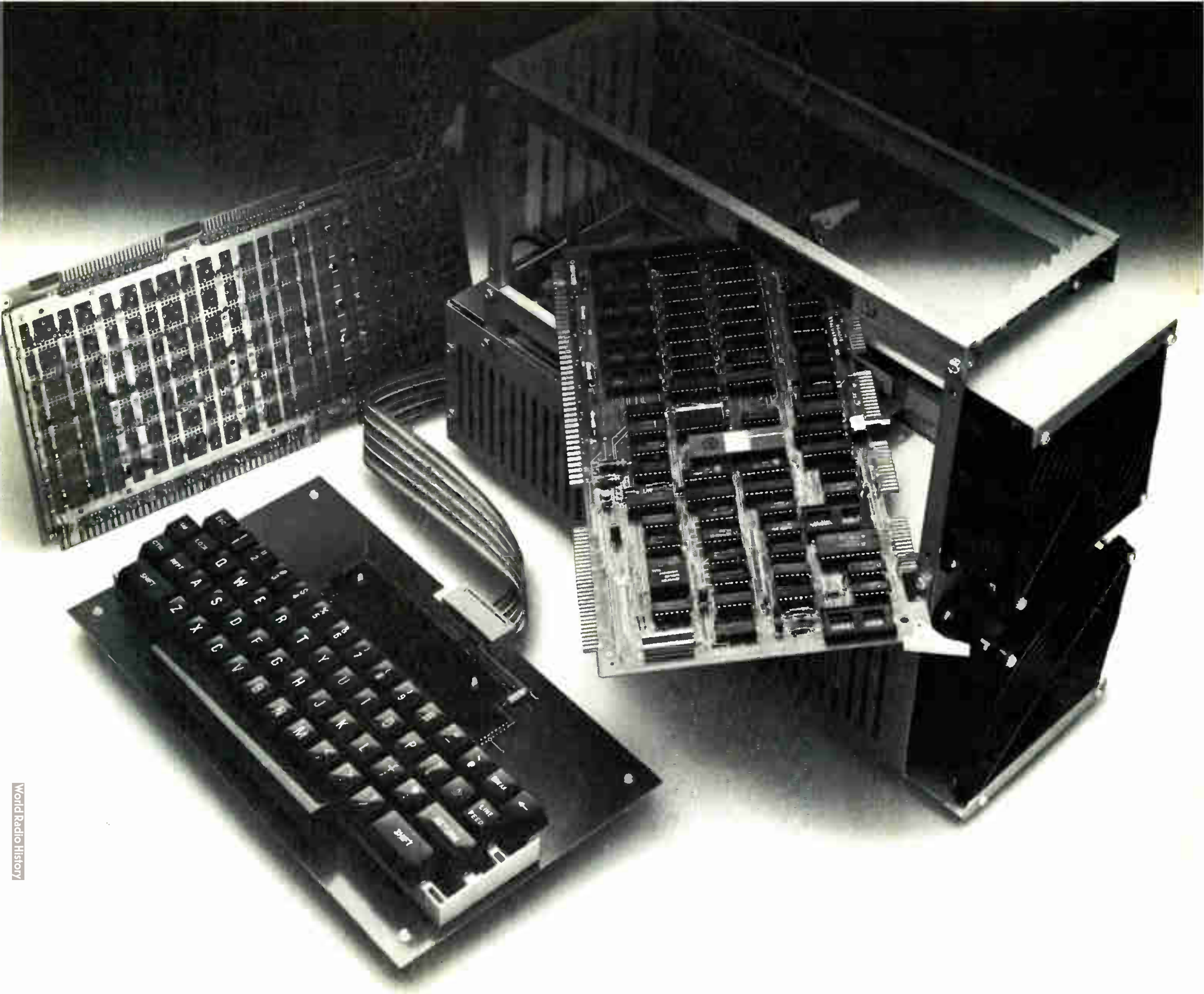

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News update

■ When Magnuson Computer Systems Inc. entered the IBM-compatible computer market almost two years ago, the company said the novel bus-oriented design of its microprogrammed M80 model 3 and 4 computers would ensure its ability to compete [*Electronics*, May 25, 1978, p. 93]. Now, a year after IBM stood the plug-compatible industry on its ear with the dramatic price-performance ratios of its model 4300 computers, [*Electronics*, Feb. 15, 1979, p. 85] Magnuson says it is still going strong—thanks to that design.

Company president Joseph L. Hitt says that some 50 M80 systems have already been installed and that as the books are closed on 1979 they show the company in the black, with about $10 million in revenue.

Hitt says the bus design was what sold so many systems during a period of market uncertainty. "The customer knows he doesn't have to replace his computer to upgrade later; we can just add to it," he says.

This is evident in the latest Magnuson machines, M80 models 32, 42, and 43, which were introduced last year to compete with the 4300 and will be delivered starting this April [*Electronics*, March 15, 1979, p. 44]. The model 32 is essentially an upgrade of the model 3 that is competitive with the IBM's smaller 4331. But the 42 and 43 take advantage of the bus design to swap a new, faster central processing unit for the old one, making the machine's price-performance ratio competitive with that of IBM's larger 4341.

The new CPU is based on MECL 10K emitter-coupled-logic chips instead of the TTL used on the earlier models. Because of this the CPU now operates twice as fast. A sophisticated micro-instruction pipeline was also added, further improving performance.

But as Carl Amdahl, Magnuson's executive vice president for engineering and the M80's designer, notes, the bus design lets the new CPU plug into the same cabinet and use the same main memory and input/output channels as previous models, making field upgrades possible.

-Anthony Durniak

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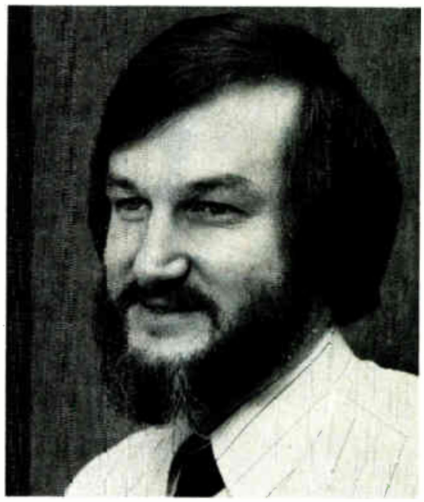
People

Bingham aims Two Pi at a place in the sun



Upward. Ronald Bingham plans to help Two Pi evolve into a smooth engineering firm

For someone who has directed a design effort that wins an award as one of the most significant technical advances of the year, what else is left? But Ronald H. Bingham, the new vice president of engineering at Two Pi Corp., faces a big challenge: to direct the engineering research and development that will enable the Santa Clara, Calif., manufacturer of IBM-compatible computers to become a major force in the industry.

Formerly Digital Equipment Corp.'s group engineering manager for the DECsystem 10 and 20, Bingham aims to lead the four-year-old Two Pi up out of the entrepreneurial stage to the level of a professional, well-organized engineering company. "That's difficult to do for a company Two Pi's size. But I'll have help from my experiences at DEC, where I was involved in a small-company, entrepreneurial-like venture," he says.

At DEC, Bingham took four people off into a corner and developed the DECsystem 2020—the eventual award winner—within one year, from start to prototype. "It took another year to integrate it into that large organization and get it into manufacturing," says Bingham, who holds a BS from Walla Walla College, Wash., with a double major in physics and mathematics.

The 40-year-old outdoorsman and avid photographer does not expect the transition at Two Pi to be as sudden. Rather, he intends it to evolve over the next few years in a smooth, efficient, and effective manner. A second objective, he says, is "to add a breath of predictability to engineering projects, which typically have a way of slipping. Over the next one to two years, we will focus on meeting budgets, goals and schedules. Because engineers respond to the feedback they get, I intend to put in place the control mechanisms and schedules that will ensure that they get it."

Bingham also plans to take advantage of modern architectural techniques, such as cache memories and pipelining, among others, that he can apply to Two Pi's V32 computer, a low-cost and powerful minicomputer that executes industry-standard IBM 370 software without any reprogramming. "In the near term, such enhancements will be the weapons we use to improve the performance and effectiveness of our product," he adds, suggesting that the next offering from Two Pi will be a product with higher performance than the V32, as well as a lower-cost system.

GenRad STI's Sear is building now for the future

For testing very large-scale integrated circuits, "architecture is everything," says Brian E. Sear. The relaxed, 43-year-old Briton has some strong ideas about that architecture, ideas that have made him president and general manager of "sort of an entrepreneurial venture," GenRad Semiconductor Test Inc. in Santa Clara, Calif. [*Electronics*, Jan. 17, p. 34].

"The architecture of the next few years must stress easy pattern generation; it must be extremely flexible and easy to modify; it must make it easy to keep track of the pattern; it must allow for parallel stimulation," says Sear. He notes that all the

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Circle 15 on reader service card

People

Builder. For GenRad STI's Sear, architecture is everything in testing VLSI devices.

system flexibility may not be needed for testing specific devices, so the overall system design must be easily modified to produce what he calls a "focused" tester—one that will provide a particular capacity for medium-volume testing. The result would be a class of testers ranging "from about $60,000 to $250,000."

Sear is right at home with building both systems and companies. It was he who set up Xincom Corp., where he remained as president until 1975 when Fairchild Camera and Instrument Corp. took it over. Later, as vice president and general manager of Fairchild's Sentry Systems division, he was architect of the strategy for Fairchild's takeover of Testline Inc. and Faultfinders Inc.

To Sear, it is an ideal time to be entering the market. "You don't want to invest a lot in refining an old generation," he states, noting that "multiple pattern processors will be needed for flexibility, to work with different types of scan techniques. Present testers can't handle them."

And not only is the timing right, but so is the partner, GenRad. "The architecture of the VLSI tester will look more like that for printed-circuit boards than today's semiconductors, but it will require more and faster test patterns per pin." GenRad's Concord, Mass., facility, he notes, is well versed in hybrid driver technology, sensor techniques, and arithmetic-and-logic unit design, as well as simulation software for pc board testing. □

hp MEASUREMENT COMPUTATION news

product advances from Hewlett-Packard

FEBRUARY 1980

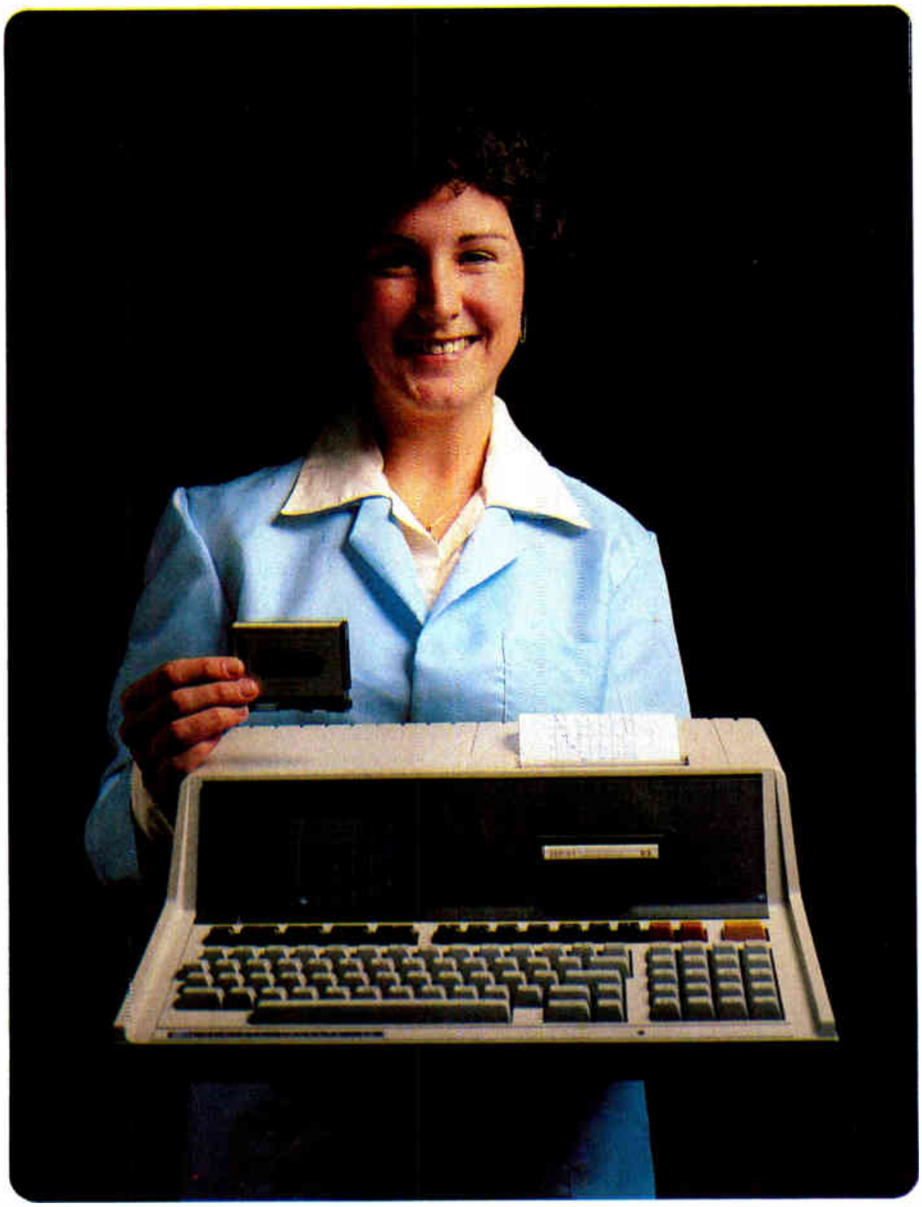
A very BASIC computer to give your personal productivity a lift

HP-IB

Basically, the new HP-85 is

- a fully integrated computer (keyboard, display, CPU, magnetic tape data storage, and thermal printer) in one package small enough to fit a corner of your desk or lab bench, or to take home.
- a computer that is easy to use because of HP's BASIC language, and that requires no computer expertise.
- a computer with 16K bytes of memory (expandable to 32K bytes, able to invert a 10 × 10 matrix). It will generate graphic designs on its CRT display interactively under your control, then transform the display to hard copy on its built-in printer.
- a computer that can interface with instruments and operate as a computing controller through HP-IB and other communication protocols available later this year.
- a computer whose versatility can be enhanced with optional peripherals through HP-IB interface: a high-speed, full-width line printer, a full-sized plotter, and flexible disc drives for data storage.
- a computer with a starting repertoire of 10 application pacs, including technical, graphics, statistics, and business.

To get full information on the HP-85, check **A** *on the HP Reply Card.*

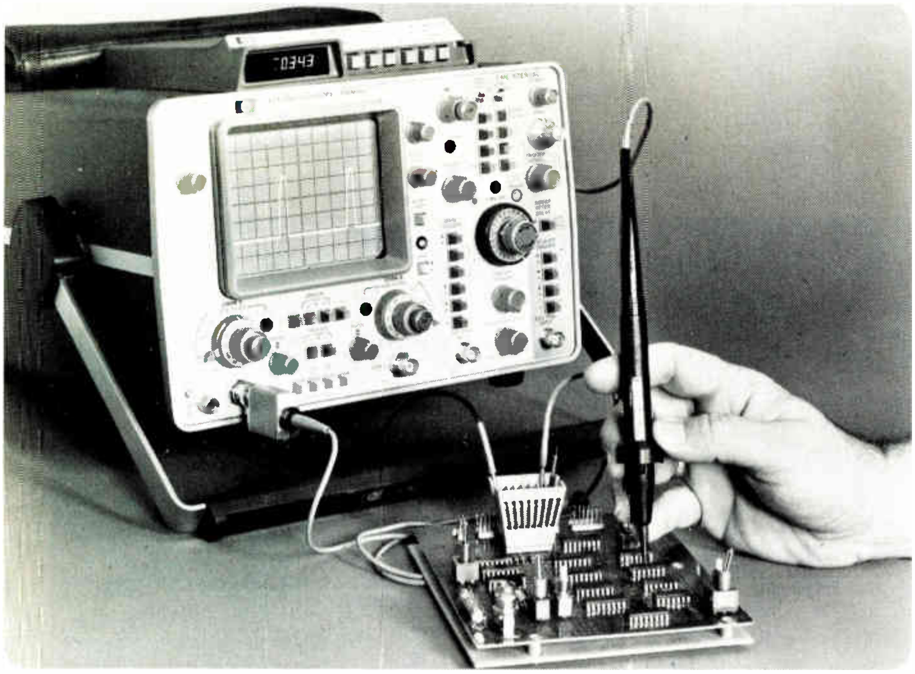


The HP-85 computer weighs a mere 20 pounds (9 kilograms). It's a very BASIC computer designed for individual use, with interactive graphics, expandable memory, optional peripherals, and interfacing potential disproportionate to its modest price.

IN THIS ISSUE

- First digital bar code wand
- Fast, accurate temperature probe

New temperature probe quickly, accurately locates circuit hot spots



HP's new temperature probe coupled with a 1700 series Option 034/035 oscilloscope gives you accurate temperature measurements while observing circuit operation.

HP's 10023A Temperature Probe provides the fast, accurate temperature measurements needed in a wide variety of thermal design, diagnostic and testing applications. Surface temperatures are read directly in degrees Celsius on any general purpose digital multimeter (DMM) with an input impedance of ⩾10 MΩ. Operation is simple with a convenient pencil-like probe tip and press-to-read switch. Just press the button, touch the surface to be measured, and read its temperature directly on the DMM.

The 10023A is a factory calibrated probe that does not require periodic recalibration. In fact, no internal adjustments are needed.

The calibrated linear output is 1 mV/°C, achieved by individually characterizing each diode in a precision thermal reference bath. An integrated circuit resistor network is then laser trimmed to match each diode to its electronic compensating network.

Measurement accuracy, which is traceable to the National Bureau of Standards, is ±2°C from 0°C to +100°C decreasing linearly to +2°C, −4°C at −55°C and to +4°C, −2°C at +150°C. For applications requiring relative rather than absolute measurements of similar temperatures, the probe has short-term repeatability of ±0.3°C. Fast temperature measurements are enabled by a temperature sensor with very low thermal mass positioned close to the measurement surface. This design also allows measurements with very low thermal gradient errors.

High thermal isolation reduces any tendency of the probe tip to act as a heat sink or cooling fin which may change the measured surface temperature. Minimum disturbance of the operating environment by the probe is particularly important when accurate measurements of small electronic components are needed. In addition, being electrically isolated, the probe tip can make measurements on non-grounded components such as power transistors with the collector common to the case.

The entire electronics assembly, including the battery, is packaged in the probe barrel. A standard dual banana plug output connector provides universal readout by most digital voltmeters including the built-in DMMs on HP's Option 034/035, 1700 series delta time oscilloscopes.

*Check **B** on the HP Reply Card for further information.*

HP's microprocessor lab teaches digital troubleshooting

Hewlett-Packard's 5036A Microprocessor Lab provides an aspect of microprocessor training not available in other products—microprocessor troubleshooting. What's more, it provides skill in this important area using HP's high-quality instruments and thorough documentation. The 5036A consists of a 20-lesson textbook/lab manual and a briefcase-contained operating microcomputer.

Included in the 450-page textbook are a troubleshooting tree for the lab, block diagrams, schematic, signature tables, and solutions for the lab's 12 moveable, practice fault jumpers. In short, all documentation needed to completely troubleshoot the lab.

Troubleshooting Lessons Build Skill on Microprocessors

The lab's textbook, "Practical Microprocessors" culminates in four highly practical troubleshooting lessons:

- **Handheld Troubleshooting Tools:** Hands-on troubleshooting using HP's 5024A IC Troubleshooters Kit: the 545A Logic Probe, 546A Pulser, and 547A Current Tracer.
- **Signature and Logic Analyzers:** Introduction to HP's 5004A Signature Analyzer and HP's Logic Analyzers.
- **Troubleshooting μP Systems:** Troubleshooting theories and useful tips.
- **Troubleshooting the Microprocessor Lab:** Detailed troubleshooting experiments on the lab using signature analysis.

*For details on HP's integrated system for learning microprocessors, check **C** on the HP Reply Card.*

The 5036A Microprocessor Lab with optional 5004 Signature Analyzer and 5024A IC Troubleshooters Kit provide actual hands-on microprocessor troubleshooting experience.

New Digital Bar Code Wand's 0.3 mm resolution enhances bar code readability

Hewlett-Packard's new HEDS-3000 Digital Bar Code Wand greatly enhances the readability of dot matrix printed bar codes thanks to its 0.3 mm (0.012 in.) resolution.

The world's first digital bar code wand, this handheld scanner is an effective alternative to the keyboard when used to collect information in self-contained blocks. In addition to the convenience advantages, bar code scanning is also faster than key entry and more accurate since most codes have check sums built-in to prevent incorrect readings from being entered.

Equipped with an integral push-to-read switch, the HEDS-3000 consumes power only when the switch is depressed. It is well suited to portable systems as well as those with line power. Housed in a rugged, stylized, molded plastic case with attached cord and connector, the wand can be manufactured in custom colors with desired logos.

Applications include remote data collection, ticket identification systems, security checkpoint verification, file folder tracking, inventory control, identifying assemblies in service, repair and manufacturing environments as well as programming of appliances, intelligent instruments and personal computers.

Check **D** *on the HP Reply Card for details.*

This new HEDS-3000 Digital Bart Code Wand is designed to scan black-and-white bar code and output TTL and CMOS-compatible signals. The heart of the wand is an advanced, high-resolution, high-speed, emitter/detector sensor in a sealed module near the removable tip.

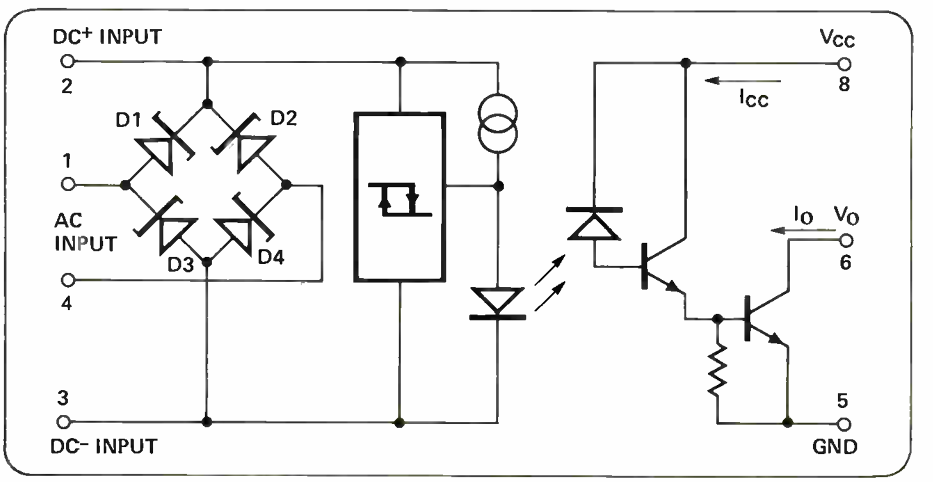
New AC/DC threshold sensing optocoupler

A new voltage/current threshold detection optocoupler with guaranteed input-threshold specifications and logic-compatible output is now available from HP. It is designed for industrial control computer input boards and other applications where a predetermined input threshold level is desirable.

The HCPL-3700 combines a threshold-sensing input buffer IC, an internal LED, and a high-gain photon detector to provide an optocoupler which features adjustable external threshold levels and logic-compatible output.

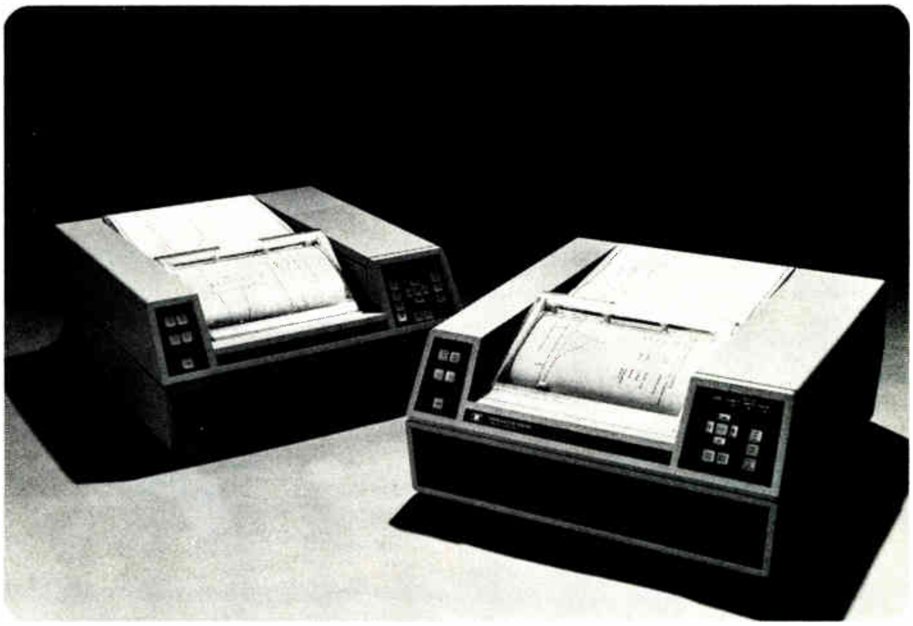
The input buffer IC contains a reference voltage circuit and a comparator that compares the input signal with the reference voltage. When the "threshold" is reached the comparator switches and turns on current to the LED. The nominal turn-on threshold is 2.5 mA and 3.8 V, but the addition of one or more external attenuation resistors permits the user to set the threshold switching point of the HCPL-3700 over a wide range of input voltages and currents. Additionally, a hysteresis circuit in the comparator minimizes false LED turn-on for electrically noisy input signals.

Obtain all details by checking **E** *on the HP Reply Card.*



Printer/plotter delivers high-quality graphics and an impressive range of capabilities

HP-IB



If your application calls for high quality graphics, a combination of vector plotting with extensive annotation, unattended operation, or long axis plotting, HP has a plotter/printer for your needs and your interface requirement. The Models 7245B land 7240A are HP-IB and RS-232-C versions of the same plotter/printer. They combine a state-of-the-art, thermal printhead and a newly developed Hewlett-Packard soft writing surface to provide high quality vector graphics and printing.

With a printing speed of 38 characters-per-second (CPS) and plotting speeds equal to or greater than that of many dedicated vector plotters, these HP desktop plotter/printers are outstanding general purpose devices. The Model 7245B HP-IB plotter/printer is an excellent companion for your desktop computer or computer system while the 7240A RS-232-C plotter/printer can be used either via telephone modem for remote applications or hardwired to your computer.

Some areas of application are engineering design, production testing, data acquisition, process monitoring, analytical plotting, long-term business forecasting, business reports, long-axis survey plotting, and project management.

Both models are microprocessor-based and use a bidirectional paper drive to advance a 61-metre (200 foot) roll of thermosensitive paper for unattended plotting and bidirectional long-axis plotting up to 5 metres (16.4 feet). A patented microstep sprocket paper drive gives them excellent line quality, and repeatability of 0.25 millimetres (0.010 inches) maximum from any point on the chart.

Blue printing and black printing thermosensitive paper is available for both units.

For full details, check **F** *on the HP Reply Card.*

East-4 Choke Cherry Road, Rockville, MD 20850, Ph. (301) 258-2000
South-P.O. Box 10505, 450 Interstate North Pkwy., Atlanta, GA 30348, Ph. (404) 434-4000.
Midwest-5201 Tollview Dr., Rolling Meadows, IL 60008, Ph. (312) 255-9800.
West-3939 Lankershim Blvd, North Hollywood, CA 91604, Ph. (213) 877-1282.
Europe-Central Mailing Depot., P.O. Box 529, Amstelveen-1134, Netherlands, Ph. (020) 47 20 21.
Japan-Yokogawa-Hewlett-Packard Ltd., Ohashi 29-21 Takaido-Higashi 3-chome Suginami-ku, Tokyo 168, Ph. 03-331-6111.

HEWLETT PACKARD

MEASUREMENT COMPUTATION news
product advances from Hewlett-Packard

January/February 1980

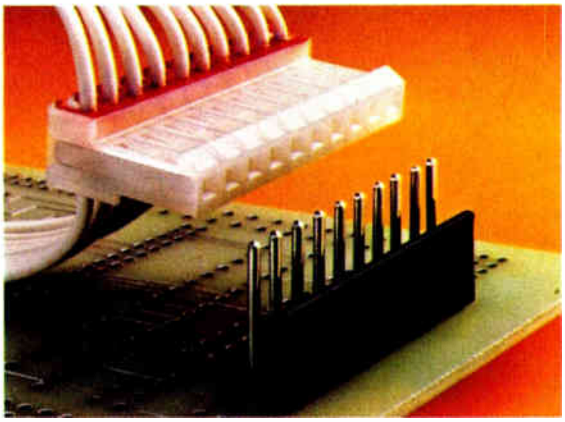
New product information from
HEWLETT-PACKARD

Editor:
Bojana Fazarinc

Editorial Offices:
1507 Page Mill Road
Palo Alto, California, 94304 U.S.A.

00081

"Every time I mass terminate discrete wire or cable, I save money. And total capability from AMP makes it happen."



The MTA interconnection system is the complete family of pre-loaded connectors, headers, and tooling that started a new era of mass termination. And since its introduction, it has proven to be a most reliable, cost effective termination method for hundreds of thousands of wire-to-post connections.

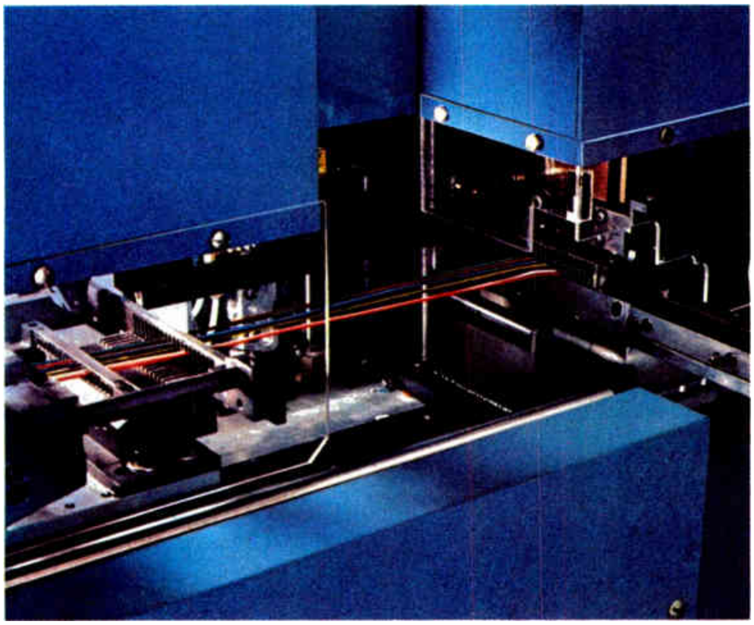
One of the many reasons for this success is the flexibility of MTA tooling, including everything from manually operated hand tools for low or intermediate volume, to automatic cable assembly machines for terminating up to 20 wires in a single stroke and double or single ended assemblies in any cable length. All this tooling is, of course, designed to lower your applied costs, and streamline your production.

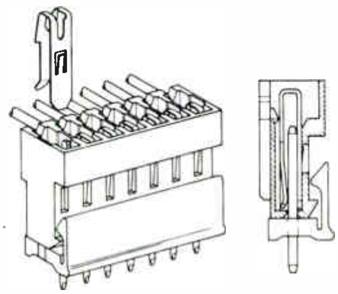
You can find this kind of versatility in our MTA connectors as well. They offer a choice of gold- or tin-plated contacts, .100" or .156" centerlines, card edge styles, and a wide variety of post header styles. Plus a complete range of positions, each of them pre-loaded with our dual insulation displacement contact. So there's no wire stripping, no crimping, and no damage to contacts. In addition, MTA allows you to mass terminate both discrete wire and ribbon cable, or even mix the two styles in the same connector.

One other advantage MTA gives you is the one you get with any AMP product. Service and engineering technical support to help keep your production error-free.

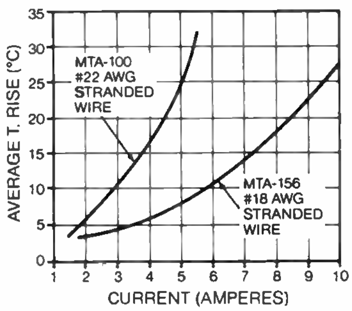
For more details about our total capability in mass termination and the savings that go with it, call or write us.

AMP has a better way.





CURRENT VERSUS TEMPERATURE RISE ABOVE AMBIENT



Some facts worth knowing about AMP MTA Connectors.

Description: A complete wire-to-post and card edge interconnection system for .100" or .156" centerlines, including headers and tooling.

	.100"	.156"
Sizes:	2-28 position	2-24 position
Wire Range:	28-22 AWG	26-18 AWG
Post Size:	.025" square or round	.045" square or round
Keying Capability:	Plug	Plug
UL Current Rating:	5 ampere	7 ampere
UL Voltage Rating:	250 VAC	250 VAC
UL Temperature Rating:	−55°C to +105°C	−55°C to +105°C

Where to telephone: Call AMP MTA Information Desk (717) 780-8400.
Where to write: AMP Incorporated, Harrisburg, PA 17105.

AMP

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Nowhere is the precision matching of memory components to function more important than in high speed cache, buffer, control store and main memory. At Intel, you'll find static RAMs to cover your full range of design goals.

*HMOS and HMOS II are patented processes of Intel Corporation.

SPEED (ns)	1K x 1*	4K x 1	1K x 4
20–40	2115H/25H (20-35ns)	2147H (35-55ns)	2149H* (45-55ns)
60	2115A/25A (45-70ns)	2147 (55-85ns)	2148H* (45-55ns)
80–100			2148 (55-85ns)
200		2141 (120-250ns)	2114A (120-250ns)
300			

*Available Q1, 1980

For highest speed and low power, no bipolar can touch our HMOS II 2115H/25H 1K static RAMs. One version gives you record access times of 20ns; three others let you choose speed/power combinations to 35ns. For designs requiring speeds from 45-70ns, our 16-pin industry standard HMOS 2115A/25A series covers the spectrum. All of these 1Ks are pin-compatible replacements for 93415/25 bipolars, and all give you dramatically lower power, too.

In a 4Kx1 format, our HMOS 2147 is the industry standard for low power and speeds to 55ns. Today, designers requiring even higher performance will find a winner in our new HMOS II 2147H—with versions as fast as 35ns and standby power dissipation of only 30mA.

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Intel gets you off and running now

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Circle 27 on reader service card

A cold shower for the optimists

Basking in the glow of a string of all-time record years, with orders showing little slackening, officials at electronics firms large and small alike may think they have it made, despite the gloomy outlook of President Carter's latest economic message. After all, the recessions feared for 1978 and 1979 did not happen on schedule, and stimulation from a sharp upswing in defense spending could pick up any commercial lag, from which auto and housing bellwethers already suffer. The question is: has the industry finally achieved its ideal—triumphing over the business cycle?

"Balderdash," scoffs a top adviser to U. S. and world firms, cautioning that complacency itself invites a tumble. With a hard-headed, fact-loaded presentation, A. Gary Shilling, a well-known economist who operates out of a New York company bearing his name, rocked the third annual Semiconductor Equipment Manufacturers Institute's information services seminar late last month in Newport Beach, Calif.

Warns Shilling: "Collapses never happen when everybody expects them, but during a state of euphoria as a result of excesses." That's why they never appeared in 1978–79, he says, when their widely forecast imminence damped speculation enough to stop a real downturn.

But "there's a serious recession coming, potentially very severe," according to Shilling. The consultant expects it to start in the last half of this year and linger into 1982, for a total of six quarters.

Do not look for much help from U. S. defense spending either, says Shilling, because even a 5% increase carries only a 2% procurement upswing. As for being counter-cyclical, "no chance," says Shilling, adding, "I've never met a guy who wasn't in an industry that is a trend-bucker." But the economist does see a bright side: the 1980s will be "a very attractive decade, except for the first two years."

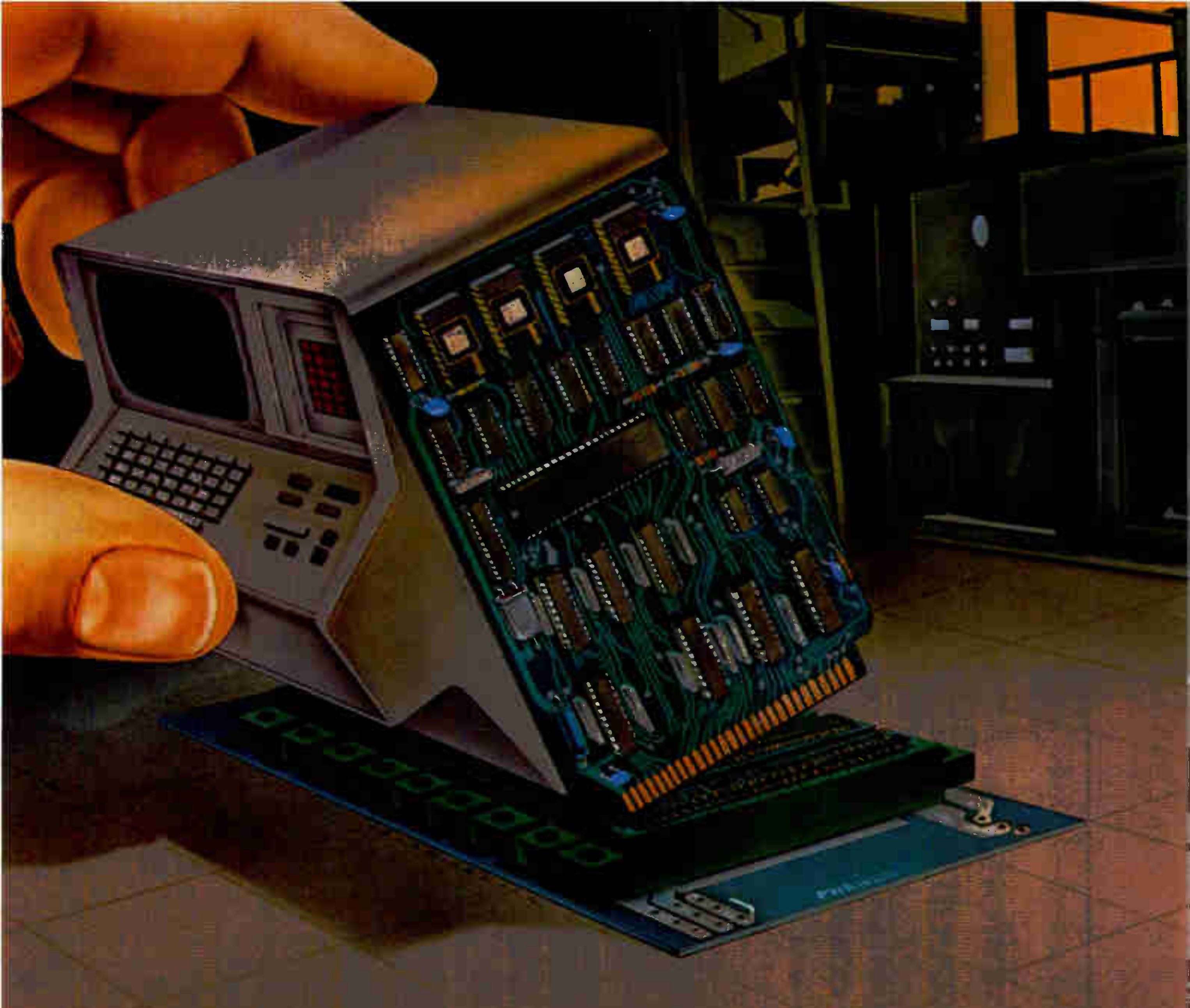
Is there anything to prevent a recession? No, says Shilling, since its causes are in place, with fiscal, monetary, and political factors forcing the inevitable. "But it's better to be prepared for the worst so you can plan," he says. Shilling's scenario could be a bracing shock to others with too rosy an outlook.

Looking beyond the EE boom

Judging from enlightened interpretation of the Carter budget (see p. 95), it looks as though another boom in the up-and-down life of the electronics engineer is in the offing.

Those old enough to remember the 1950s and 1960s also must still have vivid memories of how it felt to get to the other side of the mountain: the downhill side. The slide, particularly for aerospace and defense industry engineers, was precipitous and painful. The nation's ranks of cab drivers and gardeners, fast-food cooks and supermarket clerks were suddenly bolstered by an influx of well-educated newcomers. And they were the lucky ones.

Thus the eager EE might do worse than pause and think about what is going to happen when the contracts expire, and the young ones should not be dazzled by the recruiters. And the Government and its contractors could also do worse than plan now for the inevitable, the slump that follows the rise, the bad that sets in when the good goes away. With some intelligent forecasting and a little compassion, the next time the EEs get to the other side of the mountain they might find a gentler slope.



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PRO-LOG CORPORATION

Circle 29 on reader service card

Meetings

First International Conference on Bubble Memory Materials and Process Technology, American Vacuum Society (2030 Alameda Padre Serra, Santa Barbara, Calif. 93103), Santa Barbara Riviera campus, Feb. 20–22.

Office Computer and Peripheral Equipment Exhibition, Nippon Data Processing Association (1-8-4 Utsubo Hon-machi, Nishi-ku Osaka 550 Japan) *et al.*, Osaka International Trade Fairgrounds, Feb. 20–22.

Word/Text Processing, American Institute of Industrial Engineers, (P. O. Box 3727, Santa Monica, Calif. 90403), Ambassador West Hotel, Chicago, Feb. 20–22.

Software Quality Assurance and Configuration Management Seminar, American Institute of Aeronautics and Astronautics (P. O. Box 91295, Los Angeles, Calif. 90009) *et al.*, International Inn, Washington, D. C., Feb. 21–22.

Computers in Manufacturing Conference, American Institute of Industrial Engineers (P. O. Box 3727, Santa Monica, Calif. 90403), Airport Park Hotel, Inglewood, Calif., Feb. 25–27, Ambassador West Hotel, Chicago, March 19–21, and New York Statler, New York, April 30–May 1.

Compcon80, IEEE Computer Society (999 N. Sepulveda Blvd., Suite 410, El Segundo, Calif. 90245), Jack Tar Hotel, San Francisco, Feb. 25–28.

Diamond Jubilee Exhibition, Society of Automotive Engineers (400 Commonwealth Dr., Warrendale, Pa. 15096), Cobo Hall, Detroit, Feb. 25–28.

Conference on Industrial Investment Opportunities in Morocco, Moroccan Industrial Development Office (821 U. N. Plaza, Suite TM-606, New York, N. Y. 10017), Rabat, Morocco, Feb. 25–29.

13th International Instruments, Electronics and Automation Exhibition, Industrial and Trade Fairs Ltd. (Radcliffe House, Blenheim Court, Solihull, West Midlands B91 2BG, England), National Exhibition Centre, Birmingham, Feb. 25–29.

Conference on Laser and Electro-Optical Systems/Inertial Confinement Fusion, IEEE, Optical Society of America (200 L St. N. W., Washington, D. C. 20036) *et al.*, Town and Country Hotel, San Diego, Calif., Feb. 26–28.

1980 Engineers Public Affairs Forum, Public Affairs Forum (1155 15th St. N. W., Suite 713, Washington, D. C. 20005), Hyatt Regency Hotel, Washington, D. C., Feb. 26–28.

Ninth Annual Conference on Programmable Controllers, Engineering Society of Detroit (100 Farnsworth, Detroit, Mich. 48202), Omni International Hotel, Atlanta, Feb. 28–29.

Workshop on Computer Interface Standards, National Bureau of Standards (for information, write William A. Burr, B-212 Technology Building, Washington, D. C. 20234), NBS, Gaithersburg, Md., March 3–4.

Future Systems Forum II: Trends in the Information Systems Industry in the 1980s, Advanced Computer Techniques Corp. (222 N. Central Ave., Suite 101, Phoenix, Ariz. 85004), Registry Resort, Scottsdale, Ariz., March 3–5.

Short courses

Fundamentals and Applications of Lasers, Quality Inn, Anaheim, Calif., March 10–14. Write to the Laser Institute of America, Short Course Director, P. O. Box 9000, Waco, Texas 76710.

Digital Signal Processing and **Computer Communication Systems and Networks,** International Congress Center, Berlin, March 10–14. Write to the West German Convention Service, Congress Organization, Joachimstaler Str. 19, D-1000 Berlin 15, West Germany.

Facts from Fluke on low-cost DMM's

For a measurement like this, every millivolt matters.

In digital multimeters, accuracy and resolution go hand in hand. After all, an extra millivolt of resolution means nothing unless you can trust its accuracy. For critical measurements like checking avionics, calibrating medical systems, or simply verifying the performance of your circuit, it takes a precision DMM to fill the bill.

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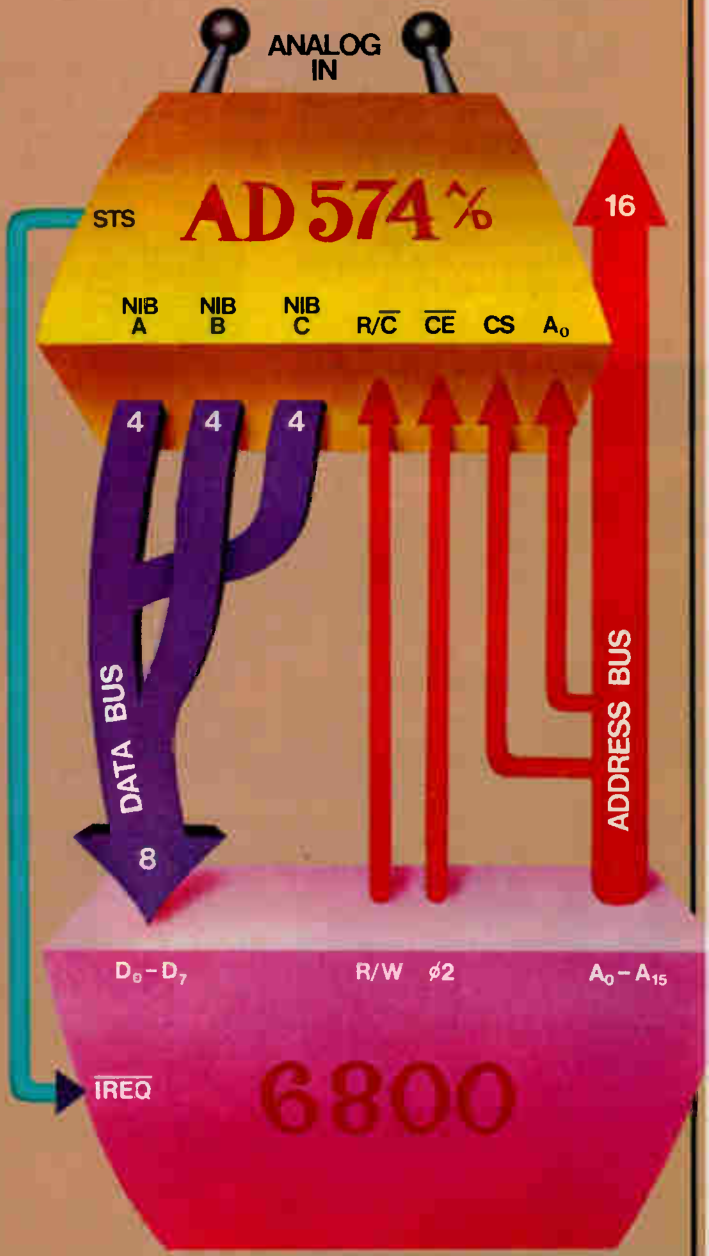

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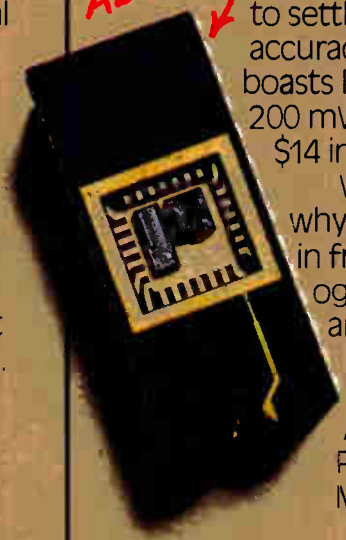

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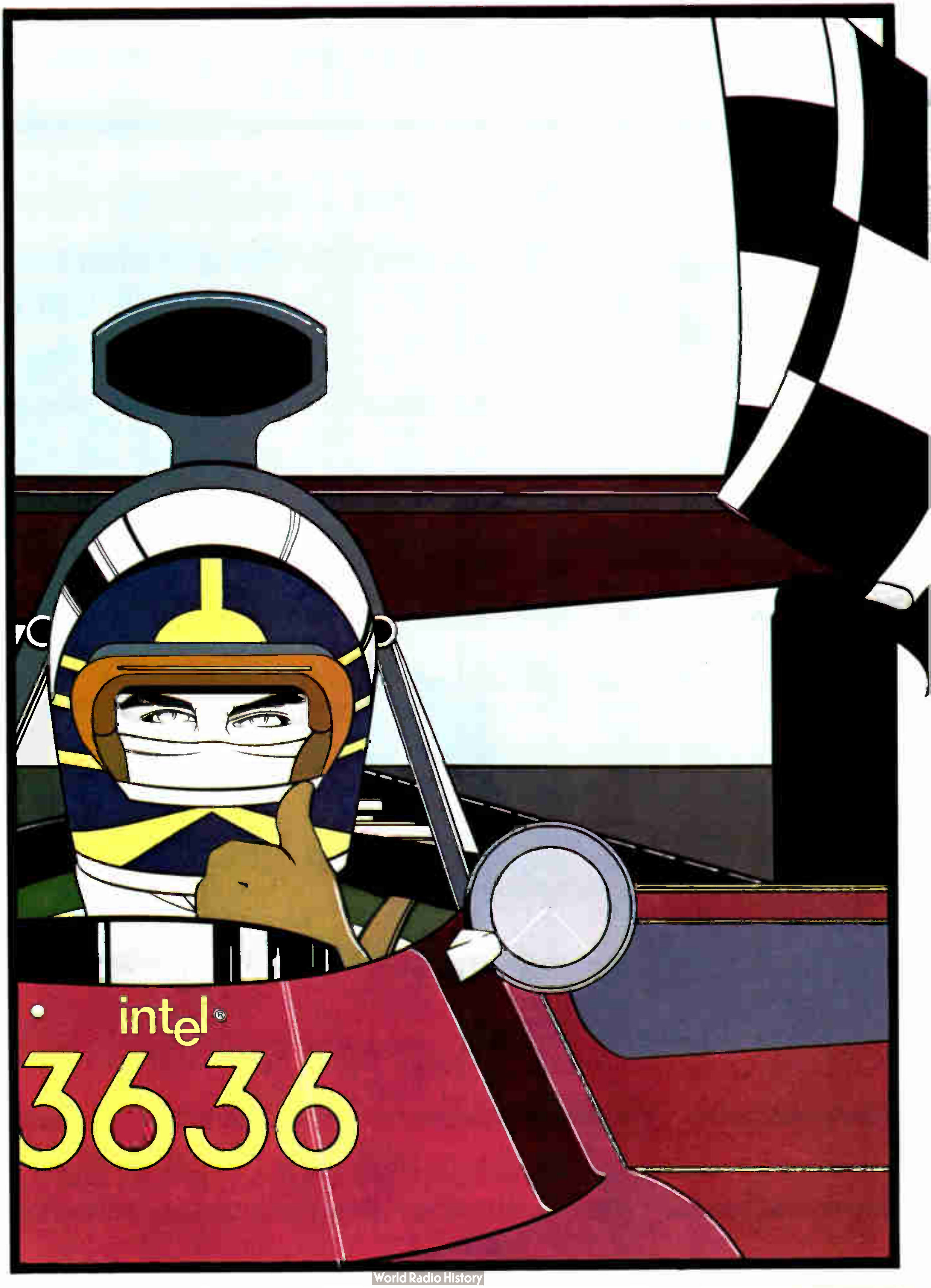
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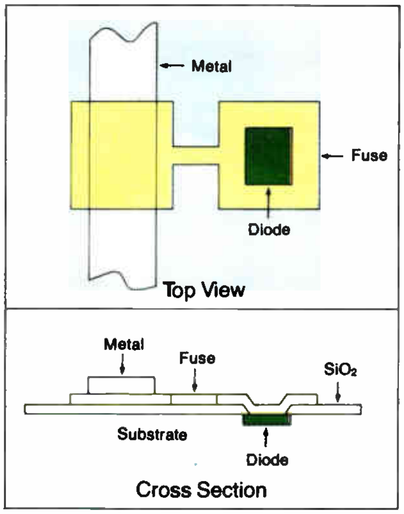

Intel's new Stacked Fuse Bipolar process allows a 30% reduction in the 16K cell size. This dramatic density improvement yields faster access speeds than ever before possible. The illustration shows the "stacking" of our polysilicon fuse over the diode instead of placing them side by side as in older designs.

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Maximum Access Time (ns)	65	80	80
Typical Power Per Bit (mW)	0.05	0.05	0.05

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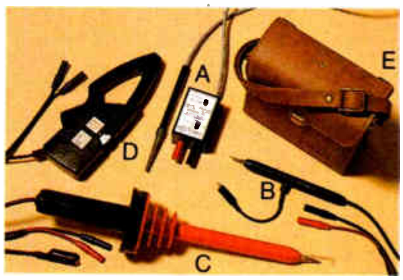

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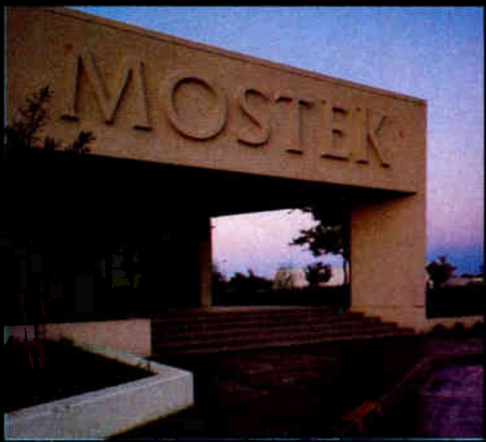

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Electronics newsletter

Lincoln Lab device called fastest yet

What is claimed to be the fastest three-terminal semiconductor yet was unveiled in Cambridge, Mass., at late January's Advanced Research in Integrated Circuits Conference. Developed at the MIT's Lincoln Laboratory in Lexington, Mass., it is called the permeable-base transistor and probably will be aimed initially at military uses. The gallium arsenide device should have applications both in logic ICs and in microwave and millimeter-wave low-noise amplifiers and power generators. The transistor's base is a tungsten grating embedded in its GaAs bulk structure; the grating creates a Schottky barrier that can be raised or lowered by varying gate bias. Performance, even at this early date, is spectacular: **maximum oscillation frequency is 17 GHz, with a remarkable 2,000 GHz forecast.** Early units already have achieved 9-dB gains with 3.5-dB noise figures at 4 GHz; 0.5-dB noise figures and 20-dB gains are said to be forthcoming. In logic ICs, the device promises gate delays in the 1-ps range.

SEC registration shows TI's share of markets . . .

Texas Instruments Inc.'s competitors, anxious to identify the world markets and products that the Dallas multinational corporation used last year to **boost its sales by 26% to $3.22 billion and profits by 23% to $179 million,** are burning up the copying machines at the Securities and Exchange Commission in Washington, D. C. The SEC form S-16 registers a $250 million upcoming offering of debentures due in 2005 and contains 1979 sales by markets. In millions of dollars (and profits) with changes from 1978, they are U. S.: $2,381 ($212), up from $1,922 ($170); Europe: $688 ($78), up from $510 ($40); other areas: $806 ($97), up from $617 ($79).

. . . plus breakout of sales, profits by product areas

The TI debenture registration also breaks out net sales and profits for 1979 and three prior years into five industry segments (with general product categories). The totals, in millions of dollars, with a 1978 comparison, include **components (semiconductors and electrical and electronic control devices): $1,527 ($216), up from $1,192 ($128);** digital products (minicomputers, data terminals, electronic calculators and watches): $887 ($53) up (and down) from $735 ($74); Government electronics (radar, infrared surveillance systems, and missile guidance and control systems): $572 ($53), up from $473 ($52); metallurgical materials (primarily clad metals): $208 ($31), up from $156 ($20); and services (primarily electronic collection and processing of seismic data used in petroleum exploration): $267 ($36), up from $223 ($31). **TI's 1979 research and development costs on commercial products totaled $134.3 million,** up 21% from $111 million in 1978, the registration statement says. Net sales billed to all Federal, state, and local governments in the U. S. totaled $376.5 million in 1979, an increase of nearly 14% from $330.7 million in the previous year.

Search, sort ROMs promise speed by log arithmetic

Most computers take longer to multiply and divide than to add and subtract. Now, two researchers at the computer systems laboratory of Stanford University in Palo Alto, Calif., hope to change this with **very large-scale integrated sorting and searching read-only memories they have developed containing log tables.** The approach, by Andreas Bechtolsheim and Thomas Gross, is faster than floating-point processing for multiplication, division, and roots; it is equally fast at addition and subtraction and can be used as an aid to pipelining, making successive arithmetic operations faster that the total time needed for each step. According to Bechtolsheim, the Xerox Corp.'s Palo Alto Research Center plans to develop the approach further. But there are no present plans to replace floating-point totally with log math, which is now limited to single-precision operations. Instead, log processing would be reserved for time-consuming operations like comparisons and fast Fourier transforms.

Optical switch, amplifier family aims at wide range

A new line of optically controlled V-groove MOS switches and amplifiers is due soon from the Theta-J Corp., Woburn, Mass. Aimed initially at reed-relay replacement in phone, instrumentation, data acquisition, and other areas, the devices, dubbed optoMOS should have far wider application. The first units will offer 1,000 MΩ of isolation but will switch either ac or dc five times faster than reeds and take less power. **Compared with optical couplers, optoMOS devices will accept about 10 times higher currents and voltages;** the earliest introductions will handle 50-W loads with as little as 100 μA of drive current—they are compatible with TTL and complementary-MOS. Because the units lack the offset characteristic of typical isolators, triacs, silicon controlled rectifiers, and bipolar transistors, they will be suited to low-distortion audio applications, either as amplifiers or as variable-ratio "transformers" or "potentiometers."

TI readies first standard product with megabit bubbles

The first standard product to use Texas Instruments Inc.'s megabit magnetic-bubble memory device is slated to roll out of the Dallas company this month. The TMS 990/211 module will employ up to six TIB 1000 bubble chips, providing 768 kilobytes of nonvolatile storage per card for use in TMS 990 microcomputer systems. The 211 board is **the first in a series of 990-compatible modules planned to utilize the TI family** of 256-K, 512-K, and 1-Mb bubble chips announced at Wescon last year [*Electronics*, Sept. 27, 1979, p. 37].

IBM adds 5120, at $9,340 its cheapest machine

IBM has introduced its lowest-priced computer—the 5120 desktop model, which starts at just $9,340. It is basically the same central processing unit as the 5110, but the corporation's Atlanta-based General Systems division has replaced that machine's small display **with a 9-in. cathode-ray-tube version that displays 16 lines of 64 characters each.** It also integrated two diskette drives, each storing 1.2 megabytes, into the computer's cabinet. Main memory ranges from 16 to 64 kilobytes, and an 80- or 120-character-per-second printer can be attached, along with Binary Synchronous or asynchronous communications adapters. Like its predecessors, the 5120 can be programmed in Basic or APL, but IBM is also making available six separately priced applications programs.

Addenda

Hewlett-Packard Co. of Palo Alto, Calif., has developed a **Pascal compiler that operates with its HP 1000 computer product line.** The compiler, priced at $4,000, runs only in the multiuser environment of HP's RTE-IVB disk-based operating system. Deliveries are to start in April. . . . **IBM will go shopping for about 28 million 16-K random-access memories** in 1980, to be used in a piggyback 32-K configuration, says an official of Dataquest Inc. of Menlo Park, Calif. Their value is in excess of $100 million.

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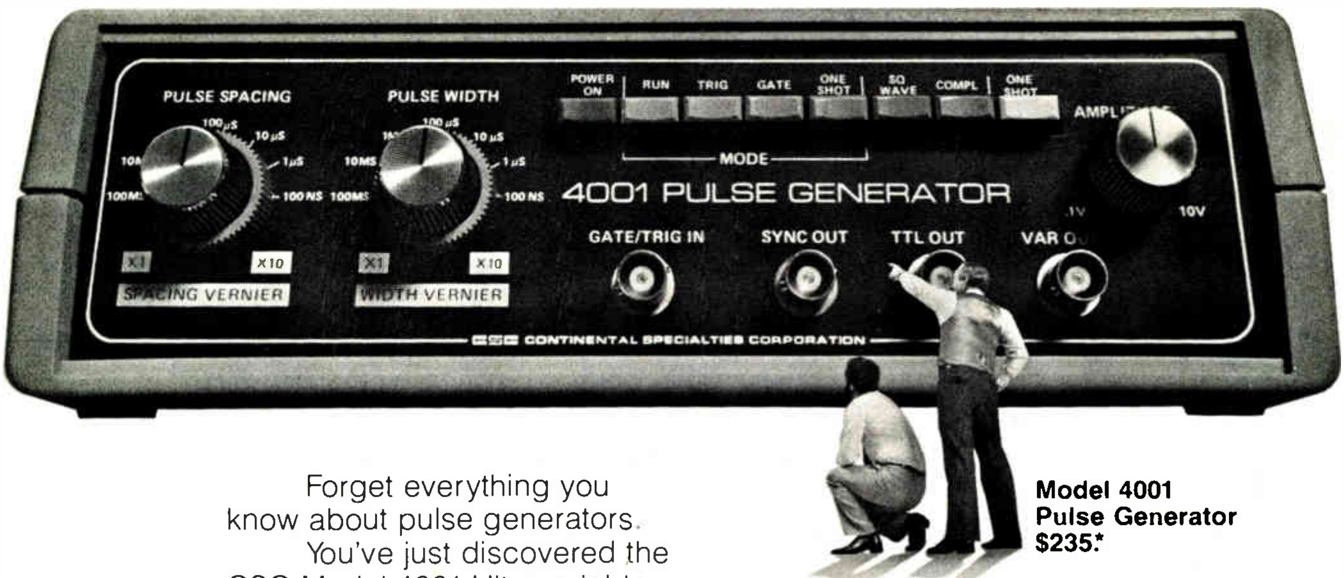
Raytheon	29625 65 ns	29641 60 ns	29631A 50 ns	
Harris	7641 50 ns	7643 50 ns	7681 60 ns	76161 60 ns
National	74S474 65 ns	74S573 60 ns		
Signetics	82S141 60 ns	82S137 60 ns	82S181 70 ns	82S191 80 ns
Intel	3624A 70 ns	3625A 60 ns	3628 80 ns	3636-1 65 ns
Texas Instruments	74S474 75 ns	74S476 70 ns	74S478 70 ns	74S452 75 ns
MMI	63S483 70 ns	63S441 60 ns	63S881 90 ns	63S1681 80 ns

(All figures taken directly from published source materials.)

Digital discovery.



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IC makers ponder polysilicon shortage predicted by year's end

by Larry Waller, Los Angeles bureau manager

Demand may exceed supply as early as August; some observers disagree, but supply is seen as tight

That oft-predicted shortage of polysilicon will materialize before the year is out, warns a top consultant on materials and processing to the semiconductor industry. The prediction, from Daniel J. Rose, president of Rose Associates, Los Altos, Calif., draws a mixed reaction from the industry—but, at the least, supplies will be tight, acknowledge makers and users of polysilicon.

Moreover, Rose is well-respected, with a reputation for accuracy. He is even ready to predict that an economic slowdown in the industry will only mitigate the shortfall between supply and demand.

Soon. Sometime between next August and December, in his worst-case scenario, the industry should run out of its basic material, he says (see figure). His detailed conclusions caused a stir at last month's Newport Beach, Calif., annual information services seminar of the Semiconductor Equipment and Materials Institute.

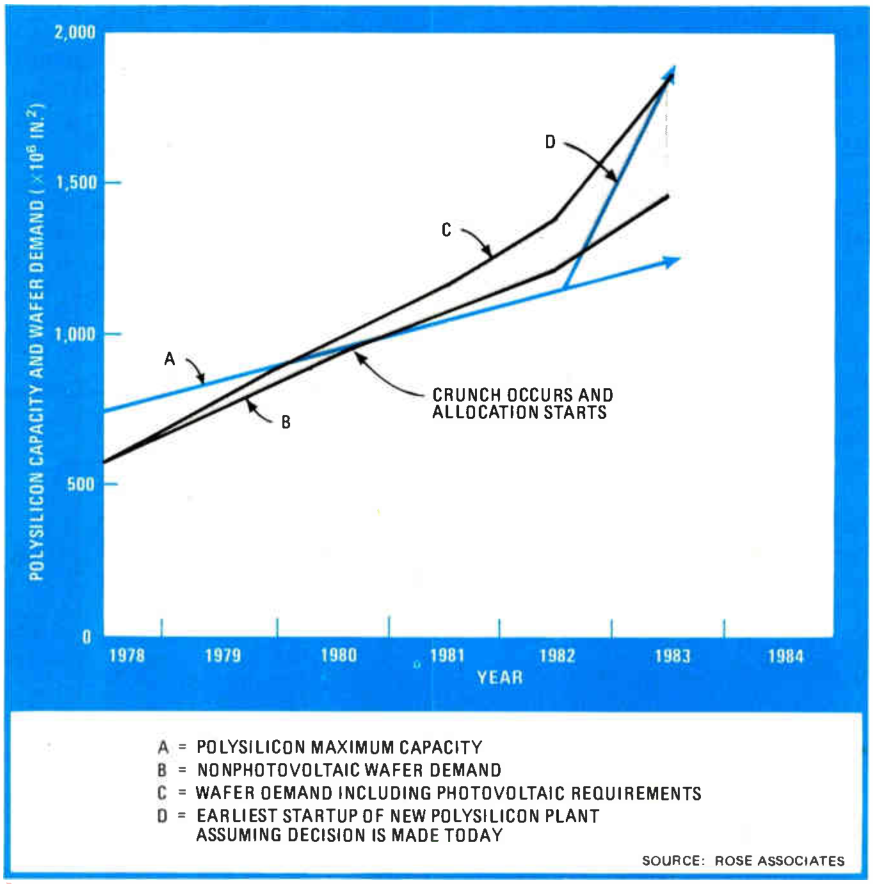
The specter of allocations by polysilicon makers, to say nothing of probable price increases from the present $65-a-kilogram level, hits semiconductor manufacturers already nervous about the spiraling cost of gold. Most industry hands agree that the present price level does not give the materials makers enough return on capital; one argues there will be no new investment until the price hits $100 a kilogram.

The shortage of polysilicon has long been anticipated, but until now no one has come up with a projection as firm as Rose's. The problem, he notes, is simple: the production capacity of the 10 or so polysilicon makers around the world is about to be outstripped by the ravenous needs of the chip makers.

The companies had a 1979 production capacity of about 2,675 metric tons, Rose says. This can be expanded about 10% a year through improved operating efficiencies.

High growth. However, the semiconductor industry has been growing at an annual rate of some 30% a year. If that continues in 1980, "I think we're in real trouble," Rose says. In fact, the industry consensus is that growth this year will total about 26% [*Electronics*, Jan. 3, p. 131].

Still, there is no consensus on the chances for a shortage among the



Crunch coming. By December, demand for bulk polysilicon will outstrip supply, says an industry consultant. Long-term increases in photovoltaic demand could aggravate shortage.

chip makers. Two who emphatically do not expect one are Motorola Semiconductor Group and Texas Instruments Inc.—but then Motorola makes about two thirds of the polysilicon it requires and TI produces all it needs.

In Silicon Valley, semiconductor makers are more uneasy. Charles E. Sporck, president of National Semiconductor Corp., for one, says the dearth of new polysilicon capacity "could lead to a real problem."

Big companies that buy polysilicon to make chips that will end up in their products would be hurt the worst by a shortage, says Rose. Among others, he mentions IBM Corp. and Western Electric, but neither company will admit to seeing a shortage on the horizon. IBM expects production capacity increases, and Western Electric points to long-term supply contracts.

Obviously, new plant capacity is one way to make up the shortfall. But Rose points out that such plants would take three years' incubation and a huge investment.

Some polysilicon suppliers do report expansion plans. The world's second biggest producer, Dow Corning's Hemlock Semiconductor Inc., makes about a quarter of the world's supply. It added 35% to its production capacity last year and will add another 25% this year.

Wacker Chemitronic GmbH, which supplies about a third of the world's needs, has a plant going on line in Portland, Ore. It will turn German polysilicon into wafers, but this does not entail an output hike.

Also, TI plans a new plant, but that is essentially to keep up with its own demands. On the other hand, SMIEL Montedison USA, an affiliate of Italy's SMIEL SpA, will be switching its output from polysilicon to more rewarding finished wafers.

Solar problem. Compounding the problem is the boom in solar cells. Though the photovoltaic demand for polysilicon has not grown at as high a rate as envisioned, it will still exacerbate the shortfall.

Moreover, the polysilicon producing community is reluctant to make large-scale new capital investment because of "seeds of hope in the technical development [of solar cells] of finding new ways to use cheaper silicon," Rose says. Such cheaper silicon processes would make the polysilicon makers' massive investments obsolete.

A wild card in any polysilicon crunch is held by the Department of Energy, which has talked about stepping into production in one way or another in order to assure materials for photovoltaics. At this point, however, it looks as though DOE will wait for cheaper manufacturing technology before moving—so the impact is a few years off.

Components

Denser V-MOS FETs strike at bipolars

By condensing the devices in a forthcoming new line of V-groove power transistors, Siliconix Inc. plans to overcome the two remaining advantages competing bipolar parts can boast: low on-state voltage drop and high breakdown voltage.

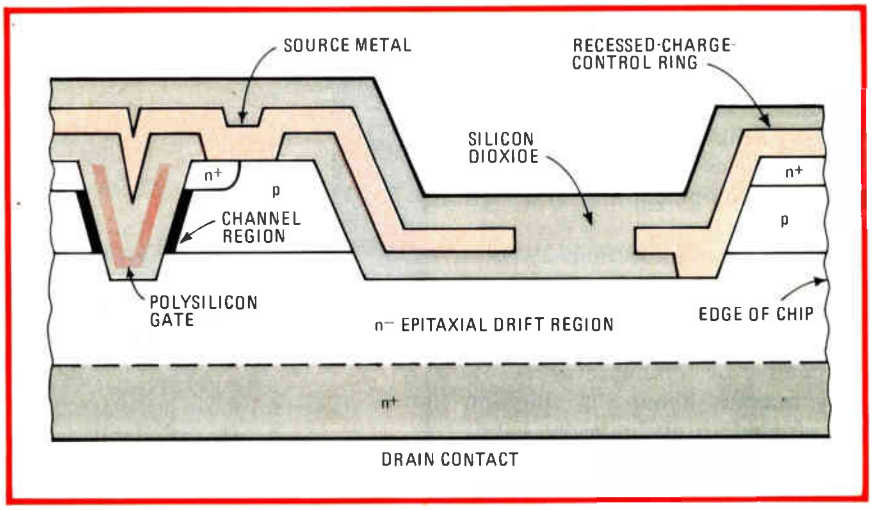
To do so, the Santa Clara, Calif., company is using what it calls triplanar conduction, with source, gate, and drain each in a different horizontal plane (see figure). The structure uses polysilicon gates buried under oxide, thereby allowing the source metalization to cover a great percentage of the IC surface.

This technique gives a threefold increase in V-MOS packing densities, says Gary Hess, marketing and applications manager. Simply achieving higher densities lowers channel resistance, a major factor in lowering the on-state voltage drop.

Second. The other major factor is lower resistance in the epitaxial drift region, and the company's engineers attacked this with two schemes. One, related to the push for higher density, is to arrange the V grooves to achieve the optimum use of the epitaxial area. The other is the choice of epitaxial material with inherent low resistivity and extremely thin doped layers—more than that, Siliconix will not say.

This ultrathin, low-resistivity epitaxial layer presented problems in achieving a high breakdown voltage. The company got around these by coming up with a novel edge-termination scheme.

These improvements will permit V-MOS power field-effect transistors "to aggressively compete with bipolar transistors both in performance and price," Hess maintains. The power V-FETs, originated by his company, already have advantages of speed and high input impedance, plus a positive temperature coefficient of saturated on-resistance, which inhibits secondary voltage breakdown and thermal runaway.



Denser V-MOS. To achieve more compact cells in its V-groove MOS power transistors, Siliconix stacks source, gate, and drain in three different horizontal planes.

While the triplanar setup itself improves density—other V-MOS transistors have the source and gate in the same plane—Siliconix has come up with a cell layout that further shrinks size. Viewed from above, the IC layout looks like a modified checkerboard, with V grooves grouped around source sites.

"No inactive silicon real estate is necessary for source bus bars," Hess says. Thus the V grooves may be arranged closer together than in prior V-MOS designs.

Using standard design rules (believed to be 5-micrometer dimensions), the IC has "an extremely high packing density because we no longer have surface-dimensional tolerances to maintain," he says. "The only tolerances that apply are chemical etch and diffusion tolerances, which are much tighter than metal tolerances" so cell size shrinks.

High breakdown. The company refuses to go into detail on its edge-termination scheme that achieves the high breakdown voltage. It involves a proprietary source field plate and the recessed charge-control ring to the right in the figure. The ring runs completely around the IC to control ion spreading from the doped epitaxial regions, thereby ensuring device stability and reliability.

According to Hess, practical triplanar V-MOS FETs achieve voltage breakdowns that are 80% of the theoretical ideal—a 10% to 20% improvement over earlier V-MOS transistors. "The on-state voltage drop is now comparable to bipolars of equivalent die area and breakdown voltage," he adds.

Figures. For example, one 23,300-square-mil IC had an on-resistance of 0.12 ohm and a breakdown of 200 volts. Another, 22,500 mil² in area, broke down at 420 to 450 V with an on-resistance of 0.9 to 1.4 ohms.

Soon to be introduced is a 400-V triplanar power FET that, Hess says, "will be about an order of magnitude less costly than currently available V-MOS parts with comparable breakdown voltages." The pricing, at around $6.50 in large quantities, will be almost on a par with comparable bipolar ICs, he adds. —**Bruce LeBoss**

Packaging & production

Two-layer resist technique produces submicrometer lines with standard optics

A team of researchers from Bell Laboratories and the Massachusetts Institute of Technology has developed a resist technique that routinely achieves submicrometer line widths using decade-old photolithographic equipment. While the team, from Bell Labs in Murray Hill, N. J., and from MIT in Cambridge has yet to make devices, it has reached line widths of 0.6 μm with ease and expects to get to 0.3 μm with state-of-the-art optical equipment.

Bell Labs' technical staff member King L. Tai unveiled the technique at late January's Conference on Advanced Research in Integrated Circuits. The method, using a two-layer resist of easily available materials and essentially familiar processing steps, might allow retooling of existing optical systems for operation in the submicrometer regions, where the much more costly X-ray and electron-beam systems have seemed to be the only choices.

Solutions. The Bell Labs–MIT team appears to have bested three of the four major obstacles to achieving silicon submicrometer geometries with optical exposure: surface roughness of the silicon, imprecise line widths, and insufficient resolution. The fourth obstacle is registration, and other researchers at the meeting at MIT reported lab systems capable of 0.1-to-0.2-μm registration accuracies, with at least one of these perhaps nearing production.

In the two-level resist method, a very thin, 1,500-to-2,000-angstrom amorphous upper layer of selenium

Sylvania to build 15,000-km fiber-optic net

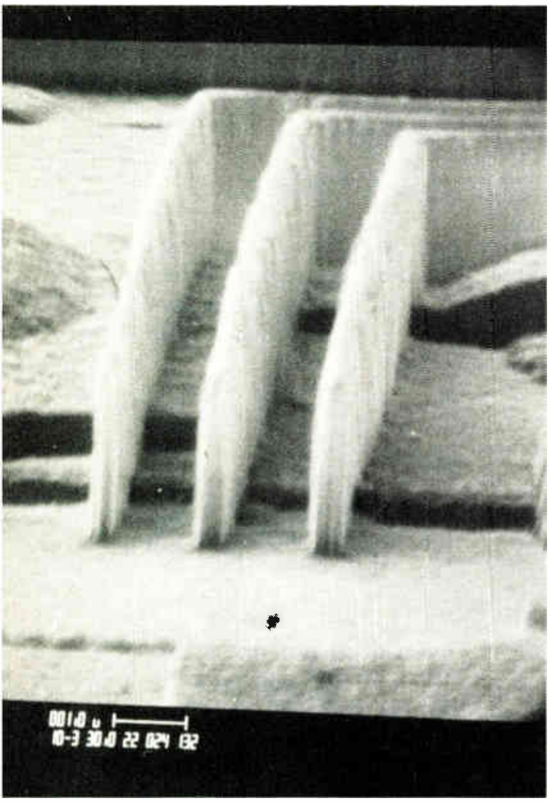
A 15,000-kilometer fiber-optic communications network, with some 5,000 communications and data-processing nodes and thousands of optical repeaters, is the centerpiece of an Air Force full-scale engineering development contract awarded to GTE Sylvania Inc.'s Systems Group. To serve the planned intercontinental ballistic missile, MX, the highly secure net will also include radio communications links.

The radios will use bands from very low to possibly superhigh frequencies for peacetime traffic, as well as medium-frequency links designed for a high-radiation post-attack environment. The missile complex will cover a large area in Nevada and Utah. Production funding in the long run could run as high as $3 billion.

For the Needham, Mass., group, the contract will mean an extensive recruiting effort, with 300 engineers needed now and another 300 within 18 months—and perhaps 3,000 production-line workers eventually. The company bested IBM and Rockwell's Autonetics division for the contract.

It bid from its strengths in communications and fiber optics, and a company spokesman says it also picked its subcontractors on the basis of readily available technology. Sharing in the award will be the Norwalk, Conn., United Technologies subsidiary, Norden Systems (computer hardware and software); Hayes International Corp., Birmingham, Ala. (airborne launch-control integration); and the Systems division of Computer Sciences Corp., Falls Church, Va. (analytic and systems engineering services).

GTE Sylvania faces some tight deadlines as the Air Force picks up the research and development pace for the missile, with a first contract review in five months. This year's $670 million MX R&D funding is up from $308 million last year, and the service is seeking $1,551 million in the proposed budget for fiscal year 1981 (see p. 95). If Congress approves the accelerated effort, Defense Secretary Harold Brown says, the fiscal 1982 budget plans call for a 40% hike to $2,180 million. —**James B. Brinton**



Fine lines. A two-layer resist enables a Bell Labs-MIT research team to achieve submicrometer lines with standard photolithography. The scale represents 1 μm.

and germanium is sputtered or evaporated onto a polymer layer. The latter, about 2 μm thick, may be made of any of the standard resist polymers without the silver that renders them photosensitive.

This beginning layer is thick enough to compensate for silicon's microscopic roughness, which often makes fine geometries impossible because of depth-of-field or optical-interference effects. Thus the SeGe layer is an almost perfectly flat optical surface—which also cuts the reflections and refractions that make for uncontrolled line widths.

Soak. To make the thin upper layer photosensitive, the team soaks the wafer in a room-temperature potassium silver selenide solution for 30 seconds. Then it exposes patterns with ultraviolet light, usually at a 4,300-Å wavelength, but sometimes as short as 3,250 Å.

Kai notes that the upper layer has more than twice the contrast of conventional resists and that the amorphous material is finely grained, thus reducing the optical-dispersion effects that can impair resolution. In fact, ultimate resolution is finer than the minimum spot or line sizes possible with available UV sources.

Also, the new resist technique could improve the benefits of retrofit kits that boost the performance of optical masking equipment. Such kits are under development [*Electronics*, Nov. 22, p. 46].

The processing steps following exposure do not depart much from present practice. To expose the lines, the team used a 10-year-old *f*1.4 lens in an aging camera and mask setup—and with contact printing rather than projection went to lines well below 0.5 μm without difficulty. With improved light sources and only slightly better optics, Kai says, 0.1-μm geometries are within the resist's capabilities.

The team has exposed submicrometer patterns as large as 1 square centimeter without dimensional variation or pinholes. Also, its method is compatible with all commonly used etching and deposition techniques, the team says. **-James B. Brinton**

Nature

Earthquakes can shake Silicon Valley, so electronics firms prepare for the worst

As earthquakes go, the Jan. 24 tremor near Livermore, Calif.—30 miles east of Silicon Valley—was not much. Still, at the Lawrence Livermore Laboratory, 29 trailers shook off their foundations; 50 gallons of slightly radioactive waste water leaked from a tank; Shiva, the world's largest laser, was thrown out of alignment. About $10 million worth of damage occurred.

Electronics plants in the area experienced only minor disruptions, but the incident does raise the question of the dangers earthquakes hold for Silicon Valley. After all, most of this semiconductor center is nestled between two of the world's most potentially dangerous fault systems.

Even mild jolts can disrupt some sensitive equipment, such as crystal-growing furnaces. At Siltec Corp, in Menlo Park, more than 30 miles from Livermore, three silicon ingots lost their crystal structures during the Jan. 24 quake and another fell back into the melt. That is far from major damage, though, notes Tony Bonora, vice president of research and development: "We lost a couple thousand dollars worth of crystals; that's hardly enough to worry about."

Were a moderate-strength earthquake to strike, wafer-fabrication equipment could suffer. For example, some of the hot xenon-quartz tubes in the diffusion furnaces at Intel's wafer-fabrication facility five miles from Livermore cracked—they might have imploded, but did not.

"Our first real concern, though, was with the arsine and phosphene that is piped into the wafer-fabrication equipment," notes Ed Sawicki, corporate safety officer. Intel detected no leaks of these lethal gases.

Survival. In fact, earthquake experts do expect a major quake to hit the San Francisco peninsula, although they cannot say when or where the epicenter will be. Most electronics plants would survive, but buildings and equipment would need repairs.

The impact is not lost on the Silicon Valley firms. They have fortified themselves against minor and moderate tremors and have taken steps to minimize damage coming from a major tremor.

Often, of course, minor vibrations can come from other sources, and manufacturers already have compensated for them. At Memorex Corp., the Santa Clara, Calif., magnetic-disk maker, test equipment floats on air pillows to isolate it from the vibrations caused by heavy trucks on adjacent Highway 101.

Feerst, IEEE joust over records disclosure

The legal maneuvering continues in the suit for a partial dues refund of $1.13 brought against the Institute of Electrical and Electronics Engineers by senior member and long-time critic Irwin Feerst. The suit centers around Feerst's contention that the IEEE, a not-for-profit corporation, acted improperly by failing to seek competitive bids in the selection of Ruder & Finn Inc., New York, as its public relations consultant.

During the first hearing, the judge in the Civil Court of the City of New York ordered that Feerst be allowed to examine the books and records pertaining to the public relations contract [*Electronics*, Jan. 3, p. 44]. The IEEE later put three stipulations on the examination:

☐That the review be for purposes of this suit only.

☐That no disclosure of the information in the records be made by Feerst to anyone other than the parties.

☐That the Court, upon request of the IEEE, seal the information discovered.

These stipulations are not unusual in civil cases involving business records.

Feerst, however, refuses to abide by the secrecy request, claiming that restricting disclosure is a violation of freedom of the press in his role as editor of a newsletter that he circulates among some IEEE members. The institute responded with a motion for a protective order from the Court, which is a request for the judge to approve the limits on the use of the records on the grounds that they contain confidential "financial data of competitive significance," according to the IEEE brief.

Feerst has countered with a motion to have the IEEE held in contempt of court and fined $1,000 a day until it provides the records. He is also requesting that an outside observer review all the records to make sure he receives the applicable documents and that the judge remove the secrecy stipulation. **-Gerald M. Walker**

Most of the major companies take such precautions as valve shutoffs activated by earth movement and the latest bolt-down techniques for equipment. Many of them have had their buildings designed or modified by a firm noted for its expertise in earthquake engineering: Rasmussen, Ingle, and Anderson, Architects and Engineers, of San Francisco.

The firm uses what one spokesman calls "conservative design principles" to exceed requirements of existing building codes. However, earthquake expertise is still as much an art as a science; only recently did experts agree that up-and-down motion in reaction to a tremor is not the problem that lateral shaking can be. This perception affects ways of bolting equipment down.

Of major concern are emergency services like firefighting. For them electronics firms are a low priority during earthquakes, notes Roger Anderson, vice president of the architectural firm. Thus many companies have readily mobilized emergency services in house.

Even if a plant is ready to resume operations right away, the loss of municipal support systems could prevent it. "A company must have water, power, and sewage lines in service in order to operate," Anderson points out. **-Martin Marshall**

Testing

Benchtop unit has flexible repertoire

That one-company product field of low-cost benchtop linear testers will soon pick up a new competitor. Analog Devices Inc. will join GenRad Inc., and it will do it with a unit that can test more types of devices more flexibly.

Known for its precision conversion products, the Norwood, Mass., company is entering the market for automated test equipment with its LTS 2000 benchtop tester [*Electronics*, Jan. 31, p. 33]. It is taking on ATE giant GenRad in an area it knows well, since it has long been testing its own linear integrated circuits.

The new benchtop tester uses a TMS 990/100A microprocessor, whereas GenRad's 1731 benchtop unit uses a Z80 [*Electronics*, March 29, 1979, p. 136]. The 16-bit processor, backed by 60 kilobytes of random-access memory into which the operating program is downloaded from a floppy disk, gives the LTS 2000 its capabilities.

More tests. For example, the unit can test analog-to-digital and d-a converters, something GenRad's tester cannot now do. By taking advantage of the 16-bit word of the TMS 990, it can test the converters to an accuracy of 12 bits (0.01%).

To configure the $25,900 tester for converter testing, the user slips out the linear test card that comes in its front drawer and replaces it with an optional $3,000 d-a card or $4,000 a-d card. Cards for logarithmic amplifiers, multipliers, and other components are on the drawing board now, and these too are parts the 1731 cannot test.

In effect, the LTS 2000 ups the ante in the low-cost benchtop tester field and has taken the industry by surprise. GenRad may be planning to upgrade the 1731, but it will not talk about its plans. Fairchild Camera and Instrument Corp. will neither confirm nor deny reports that it plans an entry.

Analog Devices uses the internal memory space, double that of the $22,800 1731, to ease system use through more flexible test sequences. The storage capacity also makes it possible to generate statistical analysis of the work performed.

The flexible test sequences are produced by stored programs that employ keys whose function is determined in software with appropriate labels displayed on a 40-character dot matrix. As the user works through the sequence-generation procedure, the keys' functions change, offering different choices of test operations at different steps.

What's more, the user can choose the order in which the LTS 2000 performs tests, thereby permitting early checking of what appear to be the failure-prone parameters. Limits for parameter values are typed in using a 30-character key pad when the program-generation procedure calls up the parameter name.

Once someone like a test-floor supervisor has generated a test program, it can then be stored on a 5½-inch single-sided floppy disk. Alternatively, Analog Devices can supply such programs from its growing library. In any case, an untrained user can run a go/no-go test by pushing a single button.

If the device fails, the test results can be printed on an integral thermal printer and attached to the failed part. Also, the tester can sort devices into eight bins.

Analysis. Another feature is an integral statistical analysis program. Failure trends for, say, a lot run through the tester can be spotted by using the program to generate tables, histograms, or curves. These plots can be printed out on an optional 132-column printer or displayed on an optional cathode-ray-tube terminal attached to the LTS 2000's two RS-232-C interfaces. Although it is intended primarily as a stand-alone tester, the new unit can work with a host computer, as well as with an automatic device handler. —**Richard M. Comerford**

I/O microprocessor aids mainframes

By providing a more sophisticated input/output organization, Burroughs Corp. hopes to facilitate attaching new B/6900 mainframes to communications-oriented distributed processing systems. Unlike previous schemes, data communications and other I/O are handled by a single subsystem based on a proprietary TTL microprocessor.

As many as 64 channels—three times more than before—are connected to this subsystem by new Data Link processors. To support its 15-month-old Burroughs Network Architecture, as many as four network support processors can be attached, each handling up to 64 communications links. By offloading many of the I/O housekeeping chores from the central processing unit, the new hardware organization equalizes the processing load, a spokesman explains.

Also new are two communications processors, the CP 9400 and 9500, which are designed to function as nodes in a BNA distributed processing system. Purchase prices for the B 6900, which will be delivered in the second quarter, start at $440,000. Typical prices for the CP 9400 and 9500 systems are about $26,500 and $36,029, respectively, and deliveries start this quarter. **-Anthony Durniak**

Telecommunications

High-speed modem grabs satellite data

The coming generation of fast data-communications satellites is stimulating rapid advances in the state of the art of ancillary equipment. A case in point is the modulator-demodulator for earth stations in the Advanced Westar satellite network, which must operate at 250 megabits per second, some four times faster than competitive ground-station modems.

Modem speed is critical to Westar because it will transmit data in the time-division multiple-access mode in order to beam four simultaneous 250-Mb/s signals to four U.S. geographic zones. The answer lies in a new modem design from TRW Inc.'s Defense and Space Systems Group in Redondo Beach, Calif.

"The problem is to acquire the signal reliably and in real time," says Zoltan A. Sarkozy, senior staff engineer. Each ground station has only 480 nanoseconds to acquire the TDMA signal burst from the satellite.

Speed. For sheer speed in signal acquisition, TRW chose what Sarkozy calls the fastest standard circuits available, Fairchild's 100K emitter-coupled-logic series. These integrated circuits operate at 1 ns, leaving ample margin for aligning and checking out the incoming bits, which have an 8-ns duration.

Other hardware developed for the modem includes wideband linear baseband amplifiers, fast analog-to-digital converters, and a direct KU-band modulator. The 18-month development cost about $1 million.

The payoff: tests show the modem has an approximate bit-error rate of 5×10^8 at a signal-to-noise ratio of 14 decibels, claims Sarkozy. TRW's next step is to deliver its prototype to Westar's parent, Western Union Telegraph Co., in Upper Saddle River, N. J. WU is still deciding overall performance specifications for the Advanced Westar, scheduled to go into operation in 1983.

The 250-Mb/s data-transmission rate is a big jump over the 64-Mb/s rate announced by prime competitor Satellite Business Systems. However, even higher data rates are on the horizon: the National Aeronautics and Space Administration wants a 500-Mb/s system, and American Telephone & Telegraph Co. is reportedly looking at the 600-Mb/s range.

TRW feels it has come up with a modem design that can meet these demands. In fact, says Sarkozy, the design can be pushed to about 800 Mb/s, although he will not go into detail. **-Larry Waller**

Solid state

Moisture-sensing IC may cut LSI failures

If a large-scale integrated circuit could indicate when it was about to fail, engineers would have fewer gray hairs. Just such an indication may be feasible with a new device type, the charge-flow transistor.

Developed at the Massachusetts Institute of Technology under the direction of Stephen D. Senturia, the CFT is a kind of field-effect transistor that senses humidity. Since it can be made by any MOS process, at the cost of an added masking step, it can easily be integrated into LSI chips.

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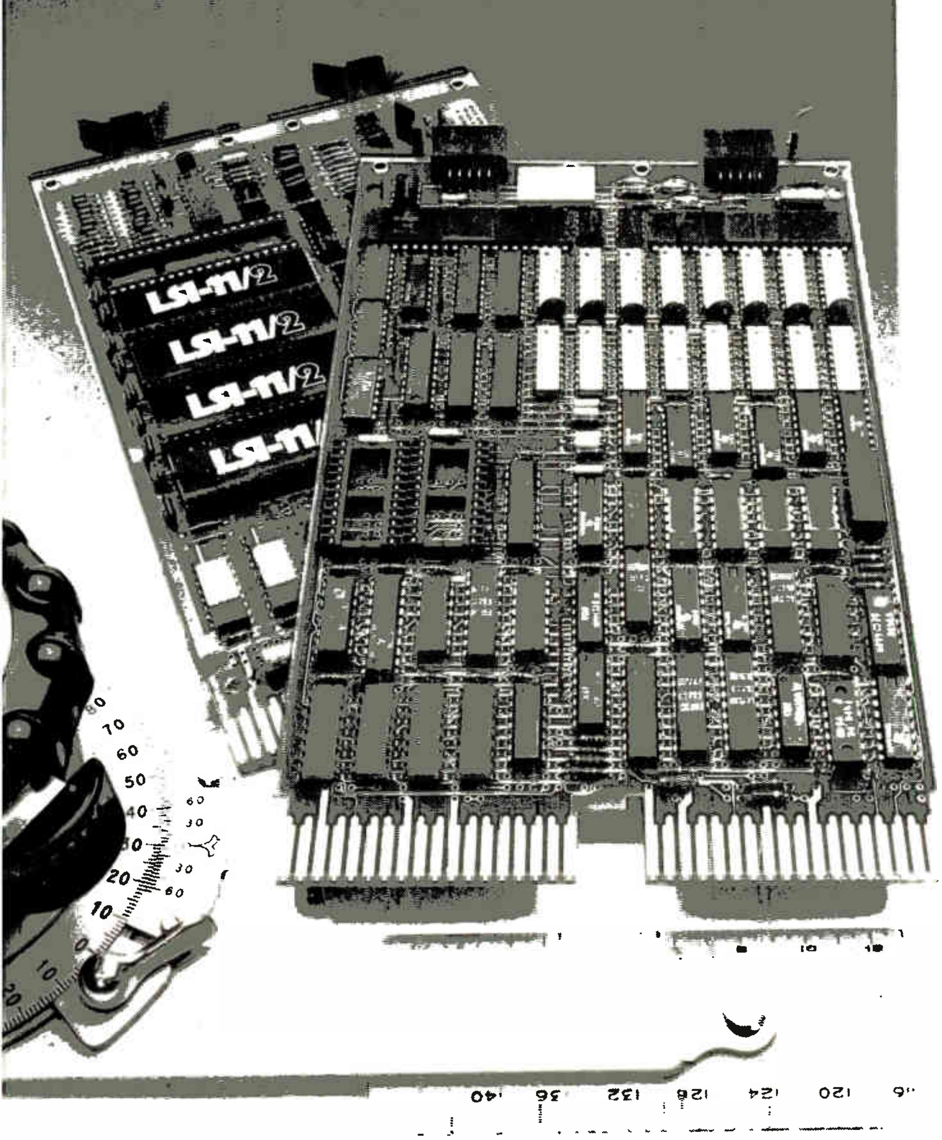

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ty within these packages causes up to 85% of post-delivery LSI failures, says Senturia.

"The rate of corrosion is just about an exponential function of relative humidity," he says. "Higher humidity means much lower reliability, so the key task becomes measuring in-package relative humidity"—and that's where the CFT comes in. He reported on the device at the Conference on Advanced Research in ICs, held in late January at MIT.

Polymer. The CFT resembles a conventional MOS FET, except that much of its gate metal is replaced by a polymer thin film of relatively high resistance. The Cambridge, Mass., research group used PAPA, polyaminophenyl-acetylene. The polymer is so viscous that the team nicknamed the CFT the "slime FET."

As PAPA absorbs moisture, its resistance declines. As relative humidity increases, therefore, the CFT's gate resistance drops and its turn-on time increases exponentially.

The research team used the CFT in a simple Schmitt trigger oscillator and found an 80% correlation between relative humidity and turn-on time or oscillation frequency. The response to a change in relative humidity takes seconds only.

Watchdog. As a reliability watchdog, Senturia foresees a tiny CFT circuit nestled in the corner of an LSI device, monitoring its own oscillation frequency or turn-on rate. If the period should become too short, the CFT would send a low-priority interrupt to a central processor or system-reliability monitor, which would print out a circuit-replacement message at the next convenient opportunity.

Because damaging corrosion takes time, the system's operators would have several hours to replace the offending IC. Replacement could prevent a crash, loss of time, and even loss of data and software.

Their application to LSI reliability may be the most important early use for CFTs. However, with other polymers than PAPA, they can sense combustion products like carbon monoxide, as well as a variety of chemical vapors. —**James B. Brinton**

Telecommunications

New crystal cut improves SAW parts

A new crystal orientation for the substrates for surface-acoustic-wave devices promises to eliminate the temperature sensitivity of orthogonal-propagation SAW filters in radar and communications systems. It is the first quartz crystal orientation having a zero temperature coefficient of delay in the two perpendicular directions of propagation.

Thus there is no need for bulky, power-hungry ovens to compensate for temperature-induced phase shift and attenuation. The most widely used device affected is the reflective array compressor, used to make dispersive delay lines with large time bandwidth products.

Next step. Devices built on substrates of the new orientation have yet to be built. One problem, of course, is the high insertion loss of quartz substrates [*Electronics*, July 5, 1979, p. 115].

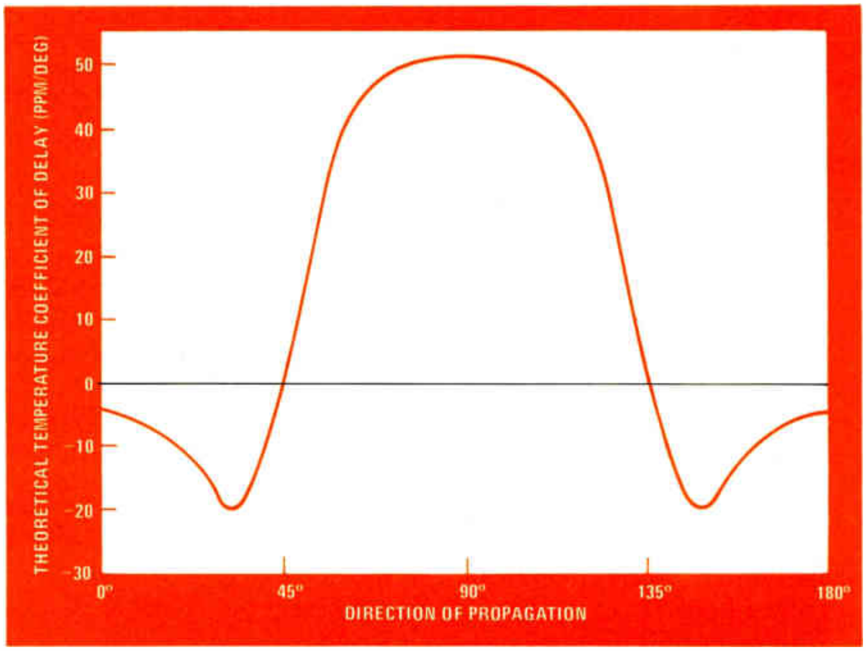
The new quartz crystal substrate is a member of the rotated Y-cut class—as is ST-cut quartz, a popular SAW material. It is produced by rotating the crystal 35.1° off its X axis, compared to ST quartz's 42.9°.

Since the anisotropic quartz material has as many different combinations or properties as it has axes and angles of operation, it is not easy to modify the substrate for a precise new operating mix. Each of the two research teams working independently on the problem used computer modeling techniques.

One of the teams is in the radio-frequency and SAW components group at the Rome Air Development Center, Hanscom Air Force Base, Bedford, Mass. Team member Robert M. O'Connell won the Air Force's 1979 research and development award for his theoretical identification of the quartz cut.

Reaching the same conclusion at about the same time was a team at Massachusetts Institute of Technology's Lincoln Laboratory in Lexington, Mass. It has verified the temperature characteristics experimentally and will soon begin building experimental SAW filters, says team member Daniel E. Oates.

Besides temperature stability, the new quartz cut offers several other advantages. For one, the acoustic waves propagated along the two



Handy. New quartz crystal orientation can be used in SAW reflective array compressors because it has a zero temperature coefficient of delay at ±45° from the cut.

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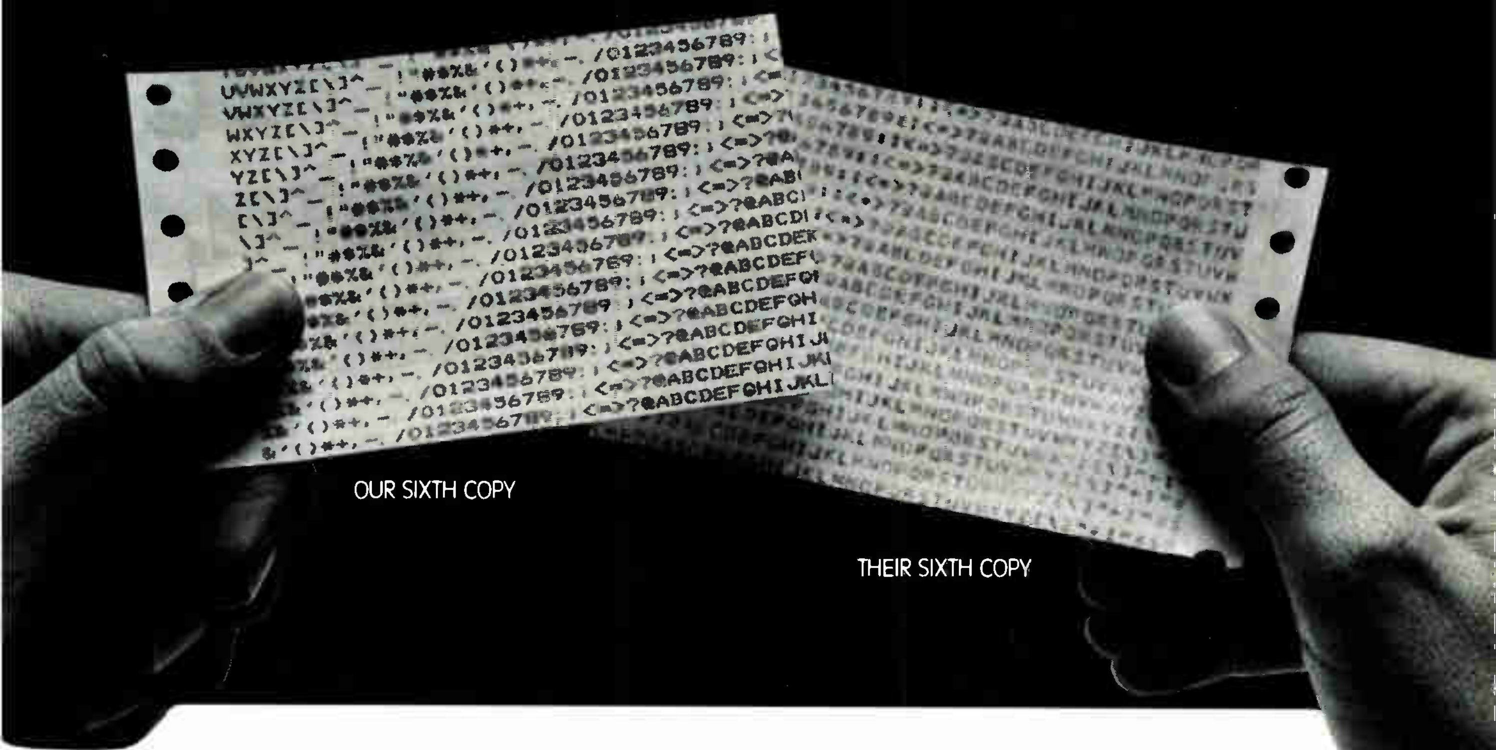

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Circle 53 on reader service card

perpendicular paths have equal velocities, so device design need not compensate for any variation.

Even more importantly, the value of the second-order temperature coefficient of delay is half that of ST-quartz, giving a wider temperature range over which the devices can operate for a given change in delay. This makes the new cut attractive for use in SAW filters that propagate in one direction.

On the other hand, quartz exhibits a relatively low efficiency in turning electrical signals into acoustic waves. Its low coupling coefficient means about a 12-decibel insertion loss for every doubling of every bandwidth past about 4%. For bandwiths of up to 50%, another popular substrate, lithium niobate, is used—but it is highly temperature-sensitive.

"You still can't have it all; you still have to decide which features you can afford to sacrifice for a given application," says Thomas A. Martin, vice president of Andersen Laboratories Inc., a Bloomfield, Conn., builder of custom SAW devices. Depending on design constraints, he says, RAC-cut components may find applications in pulse-compression radars; spread-spectrum, antijam digital applications; and compressive receivers used in electronic warfare. **-Linda Lowe**

News briefs

German IC makers plan foreign labs

Looking for greater inroads into the U. S. semiconductor market, AEG-Telefunken's Somerville, N. J., subsidiary is building an applications laboratory. Its research and development efforts will be aimed primarily at adapting the West German firm's semiconductor products to American markets. These products include a full line of linear integrated circuits, as well as optoelectronic devices.

Similarly, Siemens AG is planning a $7 million semiconductor design center in Villach, Austria, near the border with Yugoslavia. It will handle the development from initial conception to prototype of both bipolar and MOS large-scale integrated circuits. The company also plans to expand its semiconductor production plant in Villach. The semiconductor lab will be Siemens' first outside Germany and Austria's first.

See boom in data-management software

The continuing decline of the cost of computer hardware will dramatically improve the market for data-base management software, says a recent study by Creative Strategies International. Because systems software of this kind makes computers so much easier to use, practically all vendors of small-business computers, minicomputers and even microcomputer systems will offer one by the middle of the 1980s. The San Jose, Calif., market research firm predicts that, as a result, the market will grow at a rate of 82% a year from $503 million last year to $4,909 million in 1983. Although mainframes accounted for over 95% of data-base software shipments in past years, by 1983 small business systems will represent 52% of the installations, the study says. Reflecting its dominance of the industry and its bigger mainframes, IBM will account for about 56% of the software revenues. By 1983, a total of $6.2 billion will be spent on data-base management software for IBM mainframes, about half of that going to independent suppliers.

Software

VLSI could avert programmer crunch

The progression of large-scale integration into very large-scale integration will spawn whole new classes of microprocessors, but they will not prove to be the software-design burden that many foresee, says Andrew S. Grove, president and chief operating officer of Intel Corp. In fact, VLSI processors will be the solution to the coming shortage of applications software engineers.

In the 1980s, the microprocessor will grow into the solution to "the programmer catastrophe," he says, because VLSI will include more and more software on chip. Just as the microprocessor of the 1970s was a way of reducing the cost of electronic functions, its 1980s systems counterpart will be a way of reducing the cost of solutions.

The key watchword for the solid-state industry in the 1980s will be "evolution," he says. At first glance, the move from component integration to system integration that Grove foresees may seem revolutionary, but it is really a continuation of past trends, he says.

Starting point. The Santa Clara, Calif., company sees the 8-bit microprocessors with an integrated central processing unit as the starting point. Moving into the high-performance 8-bit and low-level 16-bit machines permits the integration of performance options like math-oriented coprocessors and input/output controllers, Grove says.

With high-performance 16-bit and low-level 32-bit processors, the industry will provide some level of operating system integration, Grove says. Then will come high-performance 32-bit microprocessors, featuring integration of operating system and high-level languages.

Such complex ICs will actually be the solution the programming crisis that some observers predict, Grove contends. Based on the growing number of microcomputer designs and the increasing amount of work needed to get them up and running in applications, it is possible to forecast a 1990 need for a million software engineers in the U. S. alone.

But something has to yield, and history shows that something will, Grove maintains. For instance, in 1970, the mounting use of random logic could have led to a prediction that millions of logic designers would be necessary by now. Forestalling that "circuit designer catastrophe," as Grove puts it, was the emergence of the microprocessor, a component that integrated much of the circuit-design task. There will be a similar trend with the integration of software, he says. ***-Electronics* staff**

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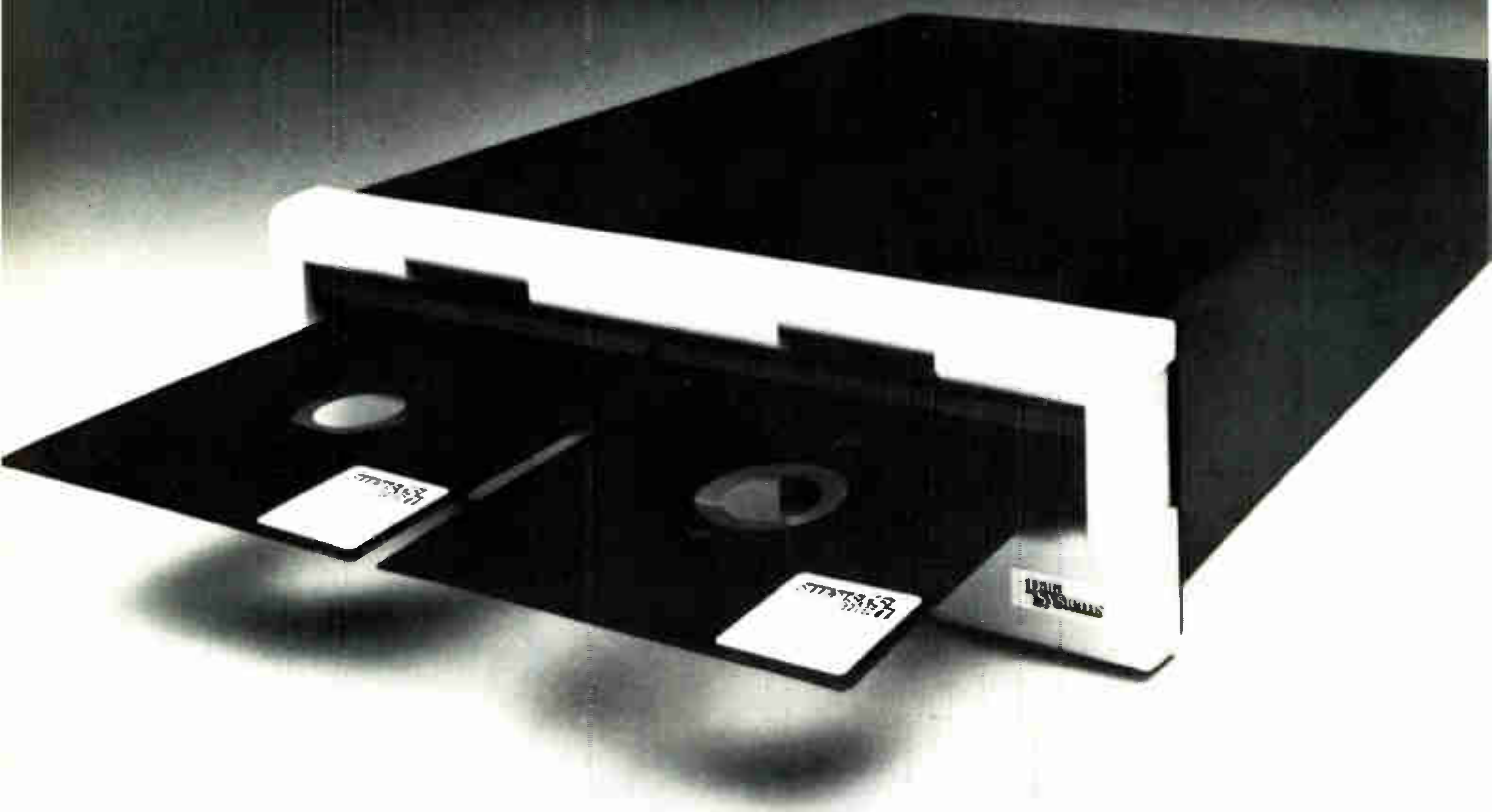

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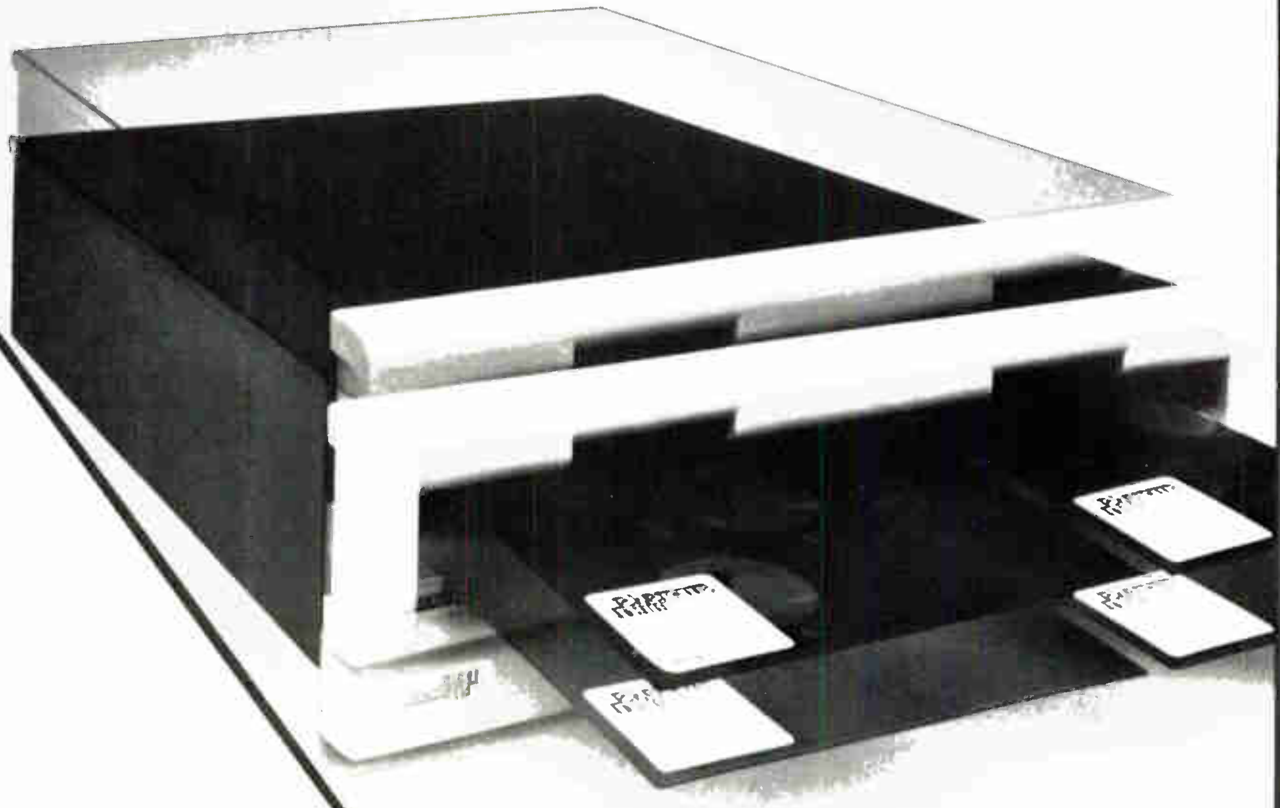

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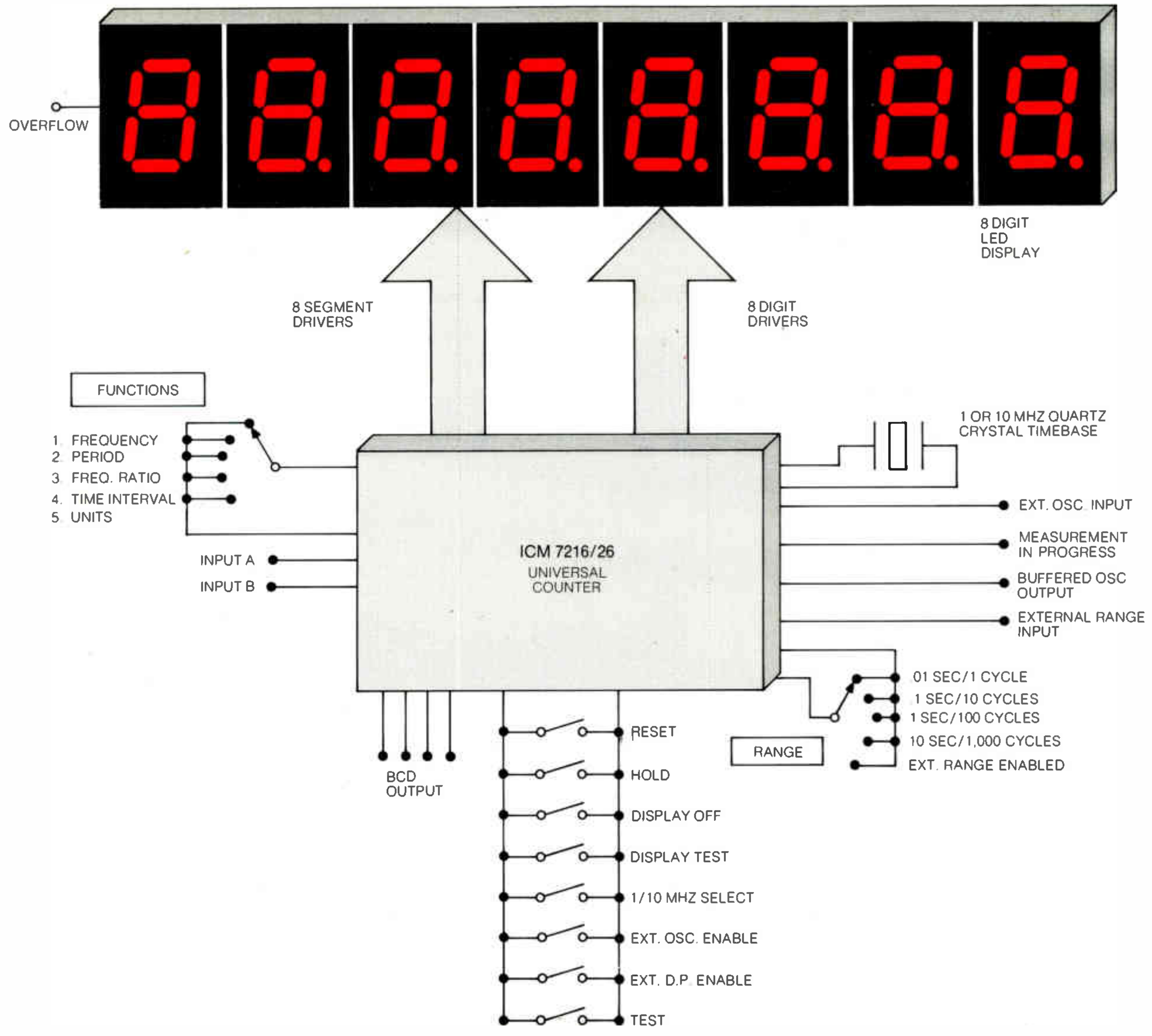

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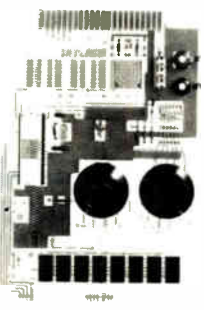

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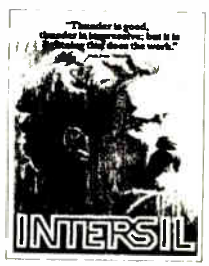

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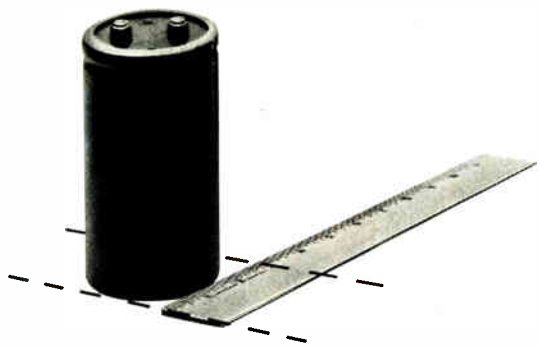

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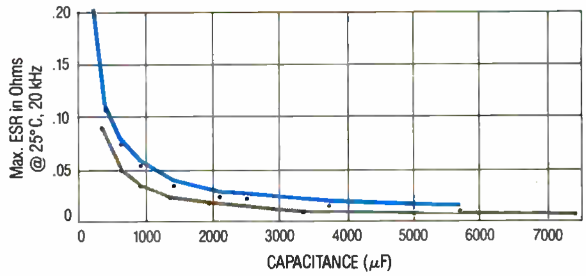
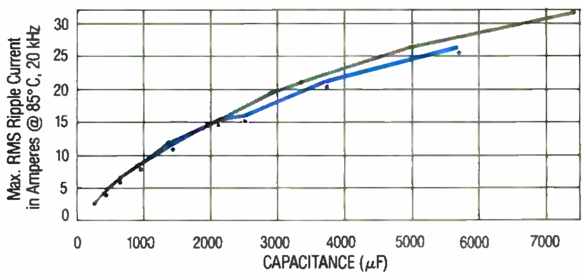


Curve plotted in gray represents capacitors rated at 200 VDC. Curve plotted in blue represents capacitors rated at 250 VDC.

HIGH RIPPLE CURRENT CAPABILITY



Curve plotted in gray shows ripple current capability for capacitors rated at 200 VDC while curve plotted in blue shows ripple current limits for capacitors rated at 250 VDC.

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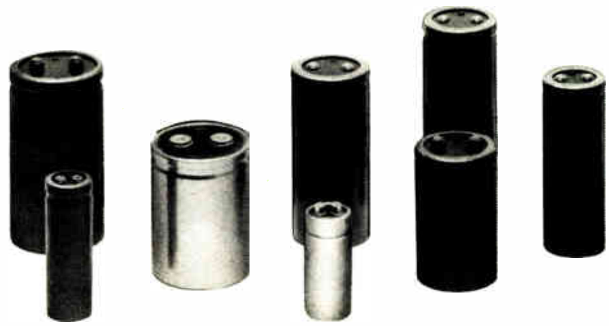

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Washington newsletter

AT&T opponents turn to Senate for protection

Telecommunications industry opponents of American Telephone & Telegraph Co. are looking toward the Senate and South Carolina Democrat Ernest Hollings' bill, S. 611, to tighten the competitive constraints on AT&T's entry into new deregulated markets. AT&T competitors also want the House Interstate and Foreign Commerce Committee headed by Rep. Harley Staggers (D., W. Va.) to hold full hearings on the amended H. R. 6121 rewrite of the 1934 Communications Act. It passed California Democrat Lionel Van Deerlin's communications subcommittee on a 13-to-1 vote at the end of January.

The H. R. 6121 substitute bill, hastily drafted by Rep. Timothy Wirth (D., Colo.) and four other subcommittee members, plugs many of the loopholes in the Van Deerlin proposal [*Electronics*, Jan. 31, p. 50]. **But it retains modifications to the 1956 antitrust consent decree to let AT&T and its Western Electric manufacturing arm enter new deregulated telecommunications markets through separate subsidiaries,** rather than requiring divestiture. The Senate bill, with stronger protective measures against AT&T subsidization of new services using telephone revenues, may be softened in a House and Senate compromise, AT&T competitors fear. Mid-April is now the timetable for House action on the Wirth substitute for H. R. 6121, with the Senate aiming at about the same date.

First VHSIC awards slip to March after Feb. 25 finals

The new deadline for soliciting best and final offers for the Pentagon's very high-speed integrated circuits program is Feb. 25, with award of the first nine contracts for VHSIC Phase Zero now set for about a week to 10 days later. Slippage of the $10 million to $12 million in nine contract awards from January [*Electronics*, Jan. 3, p. 81] is caused by **delays in obtaining triservice coordination on legal issues,** officials report. The $210 million six-year VHSIC program, in addition to its fiscal 1980 budget of $30.4 million, intends to spend $33.9 million in fiscal 1981, $40.6 million in 1982, and $41.5 million in each of 1983 and 1984 fiscal years before tapering off to $22.1 million in fiscal 1985.

Color TV sales rebound in January; monochrome weak

Color TV sales rebounded in January to 636,316 units, up 2.3% from a year earlier, following a steady downturn in the last five months of 1979 [*Electronics*, Dec. 20, 1979, p. 49]. But the latest Electronic Industries Association data puts January TV sales totals 0.6% below last year's as a result of a continuing drop in monochrome units to 325,376, off 5.9%. The high end of the consumer market remains unaffected, however, as **home video cassette recorder sales continued to surge ahead,** rising by 73.4% to 40,443 units in January.

Production seen for AQS-14 sonar after Navy approval

Westinghouse Electric Co. says it expects first Navy production funds in fiscal 1981 for its AQS-14 mine-hunting search sonar, now **approved for operational use following tests off the New England coast.** Developed by the Westinghouse Oceanic division at Annapolis, Md., for the Naval Air Systems Command, the AQS-14's active underwater vehicle is towed by a Sikorsky RH-53D helicopter using a coaxial tow cable and an on-board electronic console. The multibeam side-looking sonar has electronic beam-forming, all-range focusing, and an adaptive processor. A scan converter feeds two continuous moving-window TV pictures for real-time display.

Washington commentary

New approaches and new money for national R&D

President Jimmy Carter is now campaigning in his Commander-in-Chief's suit, according to the fiscal 1981 Federal budget that he sent to Congress last month, although he is keeping a university laboratory R&D smock hanging fresh in the closet in case the desert fighter's Cold War II uniform wears thin.

The fiscal 1981 Federal budget sent to Congress late in January (see p. 95) also shows that Carter has other new clothes ready to wear in this election year, including the incongruous outfit of a leader determined to train the nation's educationally deprived and unemployable young to enter an economy that Carter predicts will have increasing numbers of already employable persons competing for fewer jobs as a recession takes hold. Such paradoxes are not uncommon in presidential budgets, particularly in election years when the morass of numbers seems contrived to make them pictures of a never-never land.

For the short term, the job outlook for electronics engineers will prove an exception to the forecast recession. The principal budget conflict in Congress will dwell, for example, on how much more to enlarge upon an already expanded defense budget, not on the usual approach of how much to cut it.

NSF's interesting increases

More interesting, however, is the less controversial and longer-term program that would raise the National Science Foundation's budget by 15.5% to $1.15 billion. From that is woven Carter's university lab research and development smock, a garment he wears when discussing the need to increase cooperative industry and university research programs, shorten the lead time between research and development accomplishments in physical science and their engineering applications, and broaden the national science and engineering base by offering more programs in more colleges and upgrading their computer and laboratory instrumentation resources. The proposed result: more and better trained engineers and scientists, graduating from more schools, to maintain the U. S. lead in the world technological marketplace.

The fact that NSF's $154 million increase is not a very big one as long-term national programs go should guarantee it a relatively easy passage through Congress, too, although that growth might be enlarged as individual congressmen see an opportunity to tack on election year riders to fund their favorite educational constituency.

Director Richard Atkinson says NSF "is also moving aggressively to strengthen research directed at increasing opportunities for small business to make greater contributions to the national effort" in applications by raising this budget area to $13 million. Compared with this year's $3 million funding for small business applications, that is a major gain which finally recognizes that most new applications breakthroughs originate in small business.

The informal NSF response to those critics who contend that the increases are so long overdue that they should be even higher in light of past inflation and today's personnel shortages is this: NSF wants to avoid the accusation in Congress of "throwing money at the problem." Moreover, NSF sources make the point that a million dollars goes much further in the academic community than in the capital-oriented industrial complex. "We have to see how smaller schools handle the money—and determine who uses it most effectively—before we move any faster," says a staff member.

As for the assertion by some makers of semiconductors and other leading-edge electronics producers that they, not government, could more effectively fund university R&D if granted a tax cut for cooperative programs, NSF staff members respond that the issue is one for separate congressional consideration in tax legislation and note further that the calls for tax writeoffs for university R&D grants "is not necessarily in conflict with the NSF program." But, they add, it is important that the issues remain separated and not become involved in an either/or division between NSF funding and corporate programs for tax writeoffs.

The short and the long term

"Industry goals lean toward relatively short-term programs, as they should, to accomplish a given breakthrough in materials sciences or whatever for profitable applications," explains one budget official. "That can be very good for the companies and schools involved, and thus good for the country, too. But that does not mean NSF and other agencies can overlook or underfund longer-term, basic research that is not product-oriented. That would be a serious mistake. We must do both." **-Ray Connolly**

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First NEAX 61 ESS In Service

NEAX 61 ESS in service at the Manteca Central Office of Continental Telephone of California

The first NEAX 61 digital switching system was commissioned last year at the Manteca Central Office of Continental Telephone of California.

With the up-to-date digital switching system, the Manteca office has 4,320 subscriber lines and 1,134 trunks and operates as a combined toll and local exchange.

The NEAX 61 system has provided the Manteca exchange with such advantages as automatic charging systems – LAMA (local automatic message accounting) and CAMA (centralized automatic message accounting). In addition, its subscribers can expect new telephone services which were impossible with the old switching system.

The NEAX 61, developed for the purpose of covering a wide range of switching applications, offers a capacity range of up to 27,000 erlangs (972,000 CCS). For local switches, for example, the capacity is from 500 lines to 100,000 lines. This flexibility is primarily due to the system's digital switching network with a building-block configuration and to the introduction of a switch-block-oriented multiprocessor system. Each switch block consists of a switching network block and a local processor completely independent of other local processors and carries out call processing operations within the switch block.

NEC has already received dozens of orders for the NEAX 61 in the U.S., and now more than 15,000 lines are in operation.

Circle 121 on reader service card

New NEC 500 Series Microwave Transceivers Far Superior

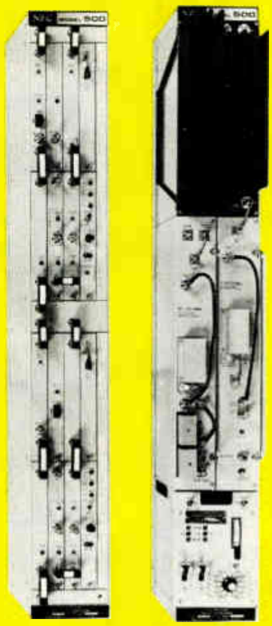
The NEC 500 series transmitter-receivers are the latest heterodyne IF repeating microwave transmitter-receivers operating in the frequency band of 2, 4, 6, 7 and 8 GHz in conjunction with an FM modulator-demodulator in the series.

The transmitter-receivers are in full compliance with CCIR recommendations. Each can transmit up to 1800/2400 telephone channels or one color television channel with a maximum of 4 sound programs.

The transmitter-receivers use microwave ICs throughout and are more economical and reliable than conventional all-solid-state equipment. The reliability is as high as over 300,000-hour MTBF (mean time between failures), thanks to highly sophisticated microwave and IF ICs used throughout. They are also four times more compact, lighter in weight and require less power than conventional equipment.

The 500 series FM modulator-demodulator provides a wide selection of transmission capacity ranging from 300 to 1800/2400 telephone channels or a color TV channel with sound programs.

The modulator, demodulator and baseband switchover circuits packed and plugged in one bay minimize the performance degradation resulting from interconnecting these components. The one-bay construction also simplifies installation and maintenance greatly.



Right: TR-6 GHz 1800/2400-500 transmitter-receiver measures 950 mm (h) x 130 mm (w) x 225 mm (d). Transmitting power is +37 dBm. Left: MD-1800V/2400V-500 FM modulator-demodulator is the same size.

The modulator-demodulator is equipped with a high-speed electronic baseband switch and the switching transfer time is as fast as 5 μs or less. It is also equipped with monolithic and hybrid ICs permitting compact, lightweight design and high reliability of over 200,000-hour MTBF.

Circle 64 on reader service card

Libyan Submarine Cable System Completed

A 708-kilometer submarine cable system linking Tripoli and Benghazi in Libya was recently handed over by NEC to the General Department of Posts and Telecommunications, Socialist People's Libyan Arab Jamahiriya. The project was completed on a full turn-key basis in cooperation with Fujitsu and OCC.

The system, constructed as a back-up link of the country's trunk microwave system running along the Mediterranean which was also completed by NEC in 1972, can handle 900 high-grade telephone channels and a two-way color television channel with good stability. It is the world's second submarine cable system capable of transmitting telephone and television simultaneously. The first such system is in service between two islands of Okinawa, Japan.

Circle 122 on reader service card

NEC Mobile Telephone Systems Ordered By Australia, Mexico

NEC will design, manufacture and deliver two 500MHz band mobile telephone systems to Telecom Australia for installation in Melbourne and Sydney. Each system is to have mobile control exchange (MCE), mobile base station (MBS) equipment, remote control and supervisory equipment and a number of mobile subscriber sets (MSSs).

The systems, to be put into service in 1981, will initially accommodate 1,000 subscribers each and will subsequently be expanded to 4,000 – 8,000 subscribers.

Thanks to SPC ESS techniques used for the MCE, the Australian systems will be fully automatic and will enable mobile subscribers to make calls both to other mobile subscribers and to ordinary telephone subscribers throughout the country at any time by automatic direct dialling (STD). The system will also permit international connection (ISD) by making the best use of LAMA techniques.

Each Australian system will consist of three to five large radio cells or zones, each one covering an area 20 to 30 kilometers in radius and able to accommodate a total of about 10,000 subscribers (as a system capacity).

Meanwhile, Telefonos de Mexico, S.A., Mexico, will also have a large radio cell mobile telephone system from NEC covering the entire area of Mexico City.

Operating in the 450MHz band, the system will initially accommodate 600 mobile subscribers and will subsequently be expanded to 4,000 subscribers.

Circle 123 on reader service card

Electronic Switching Systems At Greek Telex Exchanges

Four telex exchanges equipped with NEC's NEDIX 510A electronic switching systems are now providing excellent service in Greece.

The four NEDIX 510A electronic switching systems, accommodating a total of 14,000 telex circuits, were installed in Patras, Salonica (Thessaloniki), Athens and Piraeus by NEC for Hellenic Telecommunications, S.A. (OTE). In particular, the Athens exchange, the largest in the world with an equipped capacity of 9,000 circuits, is serving as Greece's gateway facility for international telex services.

The NEDIX 510A is a fully electronic time division stored program controlled telex and data switching system with many outstanding service features to meet both present and future telex needs. It can be used as a local, transit, international or combined exchange with a capacity of up to 30,720 telex circuits.

New High-Speed Modems

DATAX LSI 9600 modem

The DATAX LSI 4800 and 9600 are the two latest high-speed models developed using NEC's advanced carrier transmission technology. They fully comply with CCITT recommendations.

A custom LSI is incorporated, and DATAX LSI 4800 and 9600 are compact, lightweight and highly economical in power consumption. Yet, they are outstandingly stable.

These modems are also provided with many significant features to allow the construction of a variety of economical and easy-to-operate data networks in conjunction with the latest computer system network architecture using either a leased or the public switched telephone line.

In addition to the standard remote control and self-diagnostic functions, the two LSI modems can have important optional features such as voice adapters, an eye-pattern generator (DATAX LSI 4800), a multiplexer (DATAX LSI 9600), and others.

Being an all-round manufacturer of computers, communications equipment and highly sophisticated electronic components such as LSIs, NEC has facilities and expertise to meet fully the quickly changing demand both for higher speed, more efficient and better cost/performance modems and data systems.

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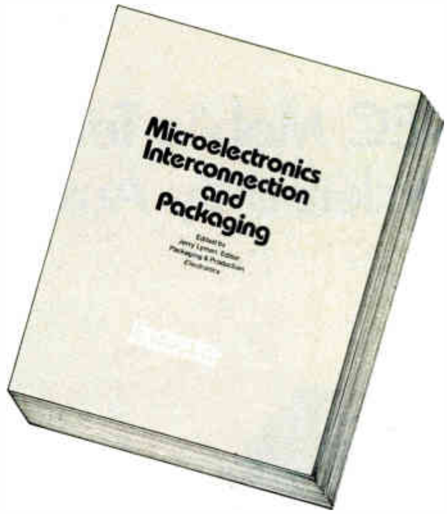

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Circle 67 on reader service card

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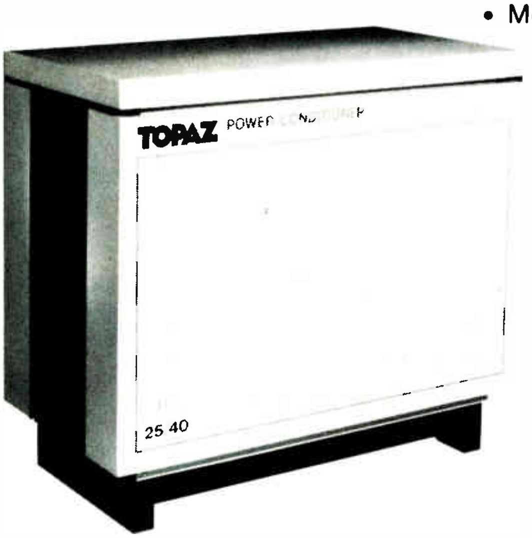

Because the computer has power requirements which can't always be met by existing facilities, the Olympic Committee decided to install a power conditioner. After a thorough review of available systems, the Committee selected the Topaz Power Conditioner because:

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THE OFFICIAL POWER CONDITIONER OF THE 1980 OLYMPIC WINTER GAMES

International newsletter

British develop 220,000-element CCD imager

A jumbo-sized, 220,000-element charge-coupled-device imager compatible with European PAL TV systems has been developed at General Electric Co. Ltd.'s Hirst Research Centre, Wembley, which will be offering limited samples over the next six months. **Fabricated using a three-level polysilicon-gate buried n-channel process,** the chip is 1 by 1.4 cm (394 by 552 mils). It consists of a matrix of 576 lines—the number operational in the PAL 625-line TV picture—of 385 elements each. Though the vertical resolution is comparable to that of a conventional plumbicon tube, the horizontal resolution is only 67%, the center says. Still, the imager should readily find applications in small audio-visual cameras, and significantly its specification was drawn up in collaboration with sister company GEC-Marconi Communications Ltd. (See also pp. 79 and 143.)

Japanese fax voices (synthetically) instructions to user

Synthesized speech is included in the latest facsimile transceiver from Matsushita Graphic Communication Systems Inc., to guide the user in the proper sequence of operations and in the proper method of recovering from errors in operation. The synthesizer uses Parcor techniques [*Electronics*, Oct. 25, 1979, p. 63] and is **currently implemented with standard chips and large-scale integrated circuits,** rather than with special-purpose chips. The $7,200 Voice Guide Panfax 7700 receives and transmits standard metric A-4–sized documents. It operates in nine modes, with transmission times ranging from 40 seconds to 6 minutes a page for a fine mode, including the 3 min./page standard of CCITT's Group II. Matsushita Graphic is a subsidiary of Matsushita Communication Industrial Co., and both companies cooperated in the product's design.

British array processor is bound for U. S.

Rather than attacking the U. S. mainframe market head on, Britain's **International Computers Ltd. is planning to market its advanced Distributed Array Processor there,** front-ended by a large, 2900 series mainframe. It has set up an Advanced Systems division in Falls Church, Va., as part of its American subsidiary, ICL Inc., to service business and government sectors, concentrating on unique products. Last month, ICL Inc. bolstered its U. S. effort in small-business systems.

Meanwhile in the UK, ICL **has received a letter of intent for a second DAP from the Science Research Council,** to be connected, funds permitting, to a new university network called Starlink. The network, linking super-minicomputers at six research centers, will be used for data and image processing. The first DAP, in which a 64-by-64 array of processors is embedded in the main memory [*Electronics*, Jan. 17, p. 44], is now scheduled for delivery this spring.

CII-HB announces two microcoded machines, turns first profit

CII-Honeywell Bull says that deliveries of its two latest medium-sized mainframes will be made before the end of the year. The DPS 7/60 and DPS 7/70 are bus-oriented and use current-mode logic in their central processing units. **The second pair of products in the company's Unisys merged line** [*Electronics*, Oct. 11, 1979, p. 78], both computers use microcodes to ensure compatibility with the three product lines inherited by the 1976 merger of Compagnie Internationale pour l'Informatique and Compagnie Honeywell Bull. Meanwhile, Paris-based CII-HB has also announced profits for 1979 of $25 million after deducting government subsidies, **the first time such net results have shown up in the black.**

Bosch's hot-wire meter measures car's air intake fast, accurately

Robert Bosch GmbH, the big West German automobile accessory maker, is developing a microcomputer-based fuel-injection system that is more accurate than the company's well-established analog version, the L-Jetronic. Unlike other systems, **the new LH-Jetronic system measures not the volume of the intake air but its mass,** which is independent of humidity and altitude. The current through a thin electrically heated platinum wire in the airstream measures the amount sucked in directly—the first time this fast, simple hot-wire metering method has been used in an auto engine application, according to Stuttgart-based Bosch.

Hitachi computers to control power net, railway in China

Hitachi Ltd. has received two major orders for computer-based control systems from China, bringing its total of such orders to 40 computers. One system, to be shipped in July, is a $2.1 million monitoring and statistical data-processing system for electric power networks. Built around two Hidic 80E control computers, it will be used to **monitor on line the power system serving the Peking area** and will also monitor power systems throughout the country and compute statistics on power transmission. The other system, which will cost $6.25 million and be shipped in December, is for train traffic control and consists of four Hidic 80Es and two small computers, the Hidic 08E. Its main task will be **to control traffic for the 137-km right-of-way, including 17 stations, between Peking and Tenshing.** The system will manage freight train traffic, route traffic onto the main line, and provide traffic information services in Peking.

Plessey turns SAW activity into joint venture with U. S. firm

The Plessey Co. is spinning off its surface-acoustic-wave activity into a new company, Signal Technology Ltd., owned equally with the Anderson Group Inc., Bloomfield, Conn. The Swindon-based firm, say its directors, **will have the size to dominate the emerging market for SAW devices in military and professional electronics markets. What's more,** there is a good fit of skills and products—which include bandpass filters, delay lines, convolvers, and spectrum analyzers—between the two companies. Both custom and standard parts will be made, the first of which will be video filters for TV transmitters and for community antenna television and a range of bandpass filters in the 70-to-160-MHz band for digital and fm communications. Signal Technology will cover the European market, and Anderson will sell the new company's products in the U. S.

Plessey is also regrouping its microelectronics and its optoelectronics and microwave activities into a new Solid State division with Melvin Larkin as managing director. Larkin was formerly chairman of Motorola (UK) Ltd. and managing director of its semiconductor division.

Addenda

Racal Electronics Ltd., whose $149 million in shares bid for Decca Ltd. [*Electronics*, Jan. 21, p. 55] was trumped by GEC's last-minute $190 million cash offer **has now countered with a bid of $210 million in cash or shares,** in what could be an expensive battle. . . . Intensifying their cooperation, **West Germany's Siemens AG and Japan's Fuji Electric Co. have set up a Tokyo-based 50/50 joint venture,** Fuji Electronic Components Ltd., to market both companies' components in Japan starting April 1. . . . **Israel increased the export of locally developed electronics items last year by over 20% to more than $100 million.**

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- Easy operation through built-in intelligence

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Circle 71 on reader service card

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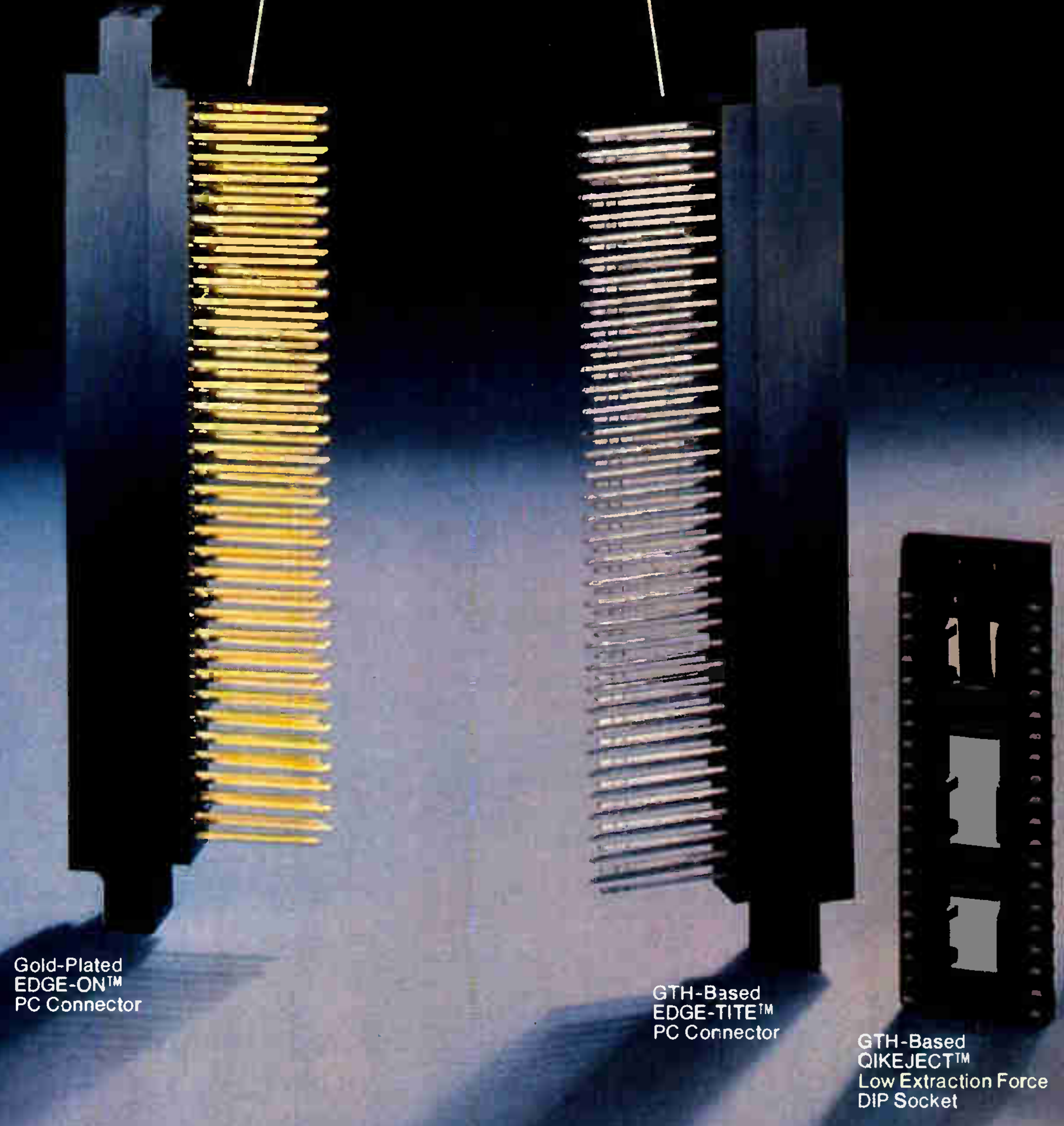

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Forget soaring gold prices. Stop worrying about gold "adders". Now you can enjoy good-as-gold connector performance . . . without gold. Without gold prices.

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After Environmental Test, at Dry Circuit Levels. (Range of Values Within 99.9% Confidence Level)

Environmental Test	GTH Contacts	Conventional Geometry Contacts			
	Tin-Alloy Plate	15 Microinch Gold Flash	30 Microinch Gold Plate	50-100 Microinch Gold Plate	Tin or Tin-Alloy Plate
Initial	4.0 - 6.0	4.5 - 13.3	4.5 - 8.6	4.4 - 8.3	4.1 - 12.0
Thermal Shock	4.0 - 8.6	6.0 - 15.0	5.0 - 8.0	5.2 - 7.2	6.0 15.0
Humidity	4.5 - 7.0	10.1 - 31.8	5.0 - 9.0	4.9 - 8.8	5.3 75.1
Industrial Atmosphere	4.0 - 6.0	10.9 - 20.3	5.0 - 20.0	5.0 - 13.0	28.7 Open Circuit
Gas Tightness	4.0 - 6.5	Not Applicable	Not Applicable	Not Applicable	4.0 Open Circuit
Thermal Cycling	4.0 - 7.0	8.5 - 15.5	5.0 - 10	4.6 - 9.0	4.0 Open Circuit
Durability	4.0 - 5.5 (100 cycles)	10.1 - 12.2 (100 cycles)	5.0 - 9.0 (100 cycles)	5.3 - 9.3 (500 cycles)	13.9 - 57.9 (100 cycles)
Vibration	4.0 - 5.5 (5-500-5 Hz)	9.0 - 15.0 (10-55-10 Hz)	4.0 - 8.0 (10-2000-10 Hz)	5.3 - 9.3 (10-2000-10 Hz)	4.0 - 15.0 (10-55-10 Hz)

Circle 254 on reader service card

Whose MCU does 8-bit jobs on a

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You can order S2000s now with built-in 1Kx8 ROM and 64 4-bit nibbles of RAM. And S2150s, with 1.5K bytes of ROM and 80 nibbles of RAM.

MIGHT

4-bit budget?

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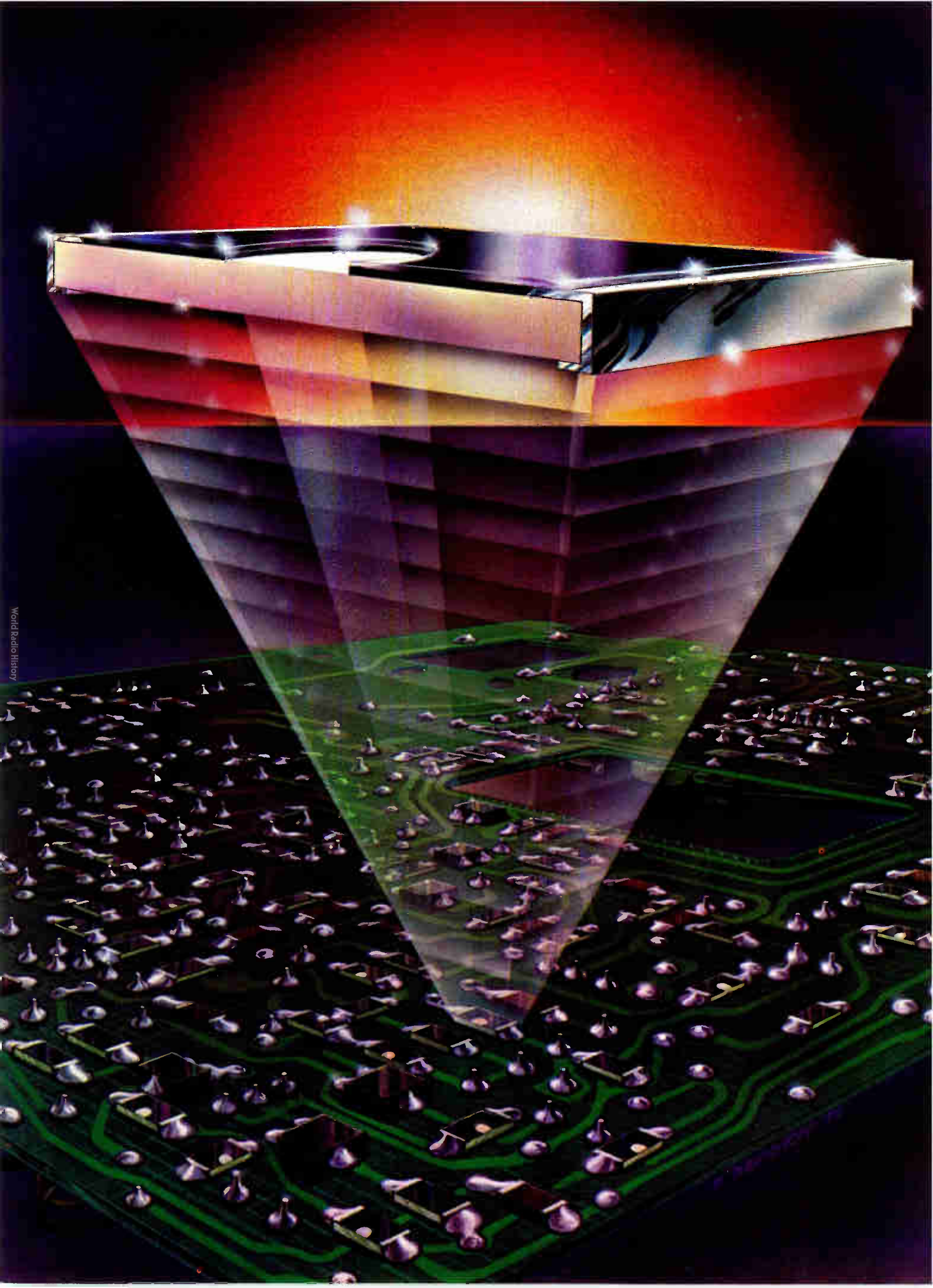

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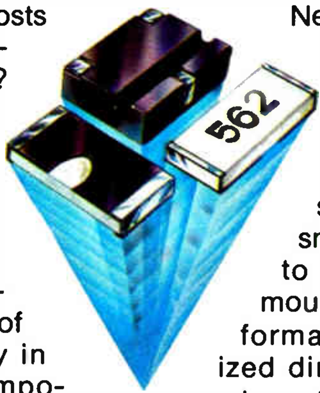
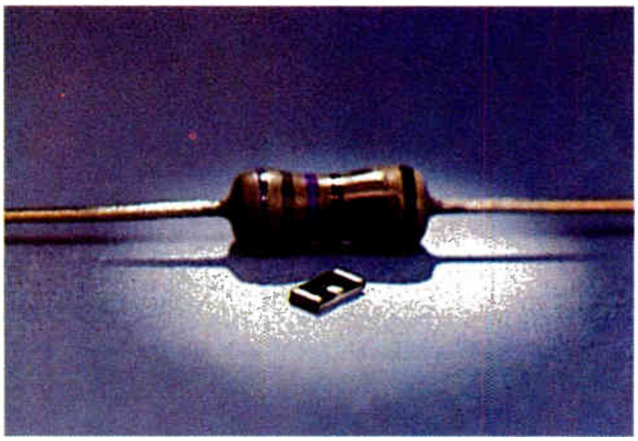
Now you can slash your assembly costs and create thinner, smaller, more reliable products at the same time. How? With our new flow-solderable resistor and semiconductor chips.



Start using both sides of your PC boards

Hundreds of these new chip components can be attached to either side of your PC boards in seconds. Already in widespread use in Japan, these components have fostered the development of high-speed magazine loading and tape and reel attachment methods. Once attached, the chips can be flow-soldered along with axial or radial-leaded components. Together, these developments are making dramatic reductions in assembly and labor costs possible.



Nearly 200 chip resistors (1/16W) can be mounted in just four square inches. This great density, coupled with the fact that the chips can be mounted on both sides, drastically reduces PC board size. The end result is thinner, smaller, lighter products that cost less to produce. In addition, the ability to mount chips opposite IC's provides performance improvements. And, standardized dimensions are making board layout and product design faster and more straightforward.

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Circle 256 on reader service card

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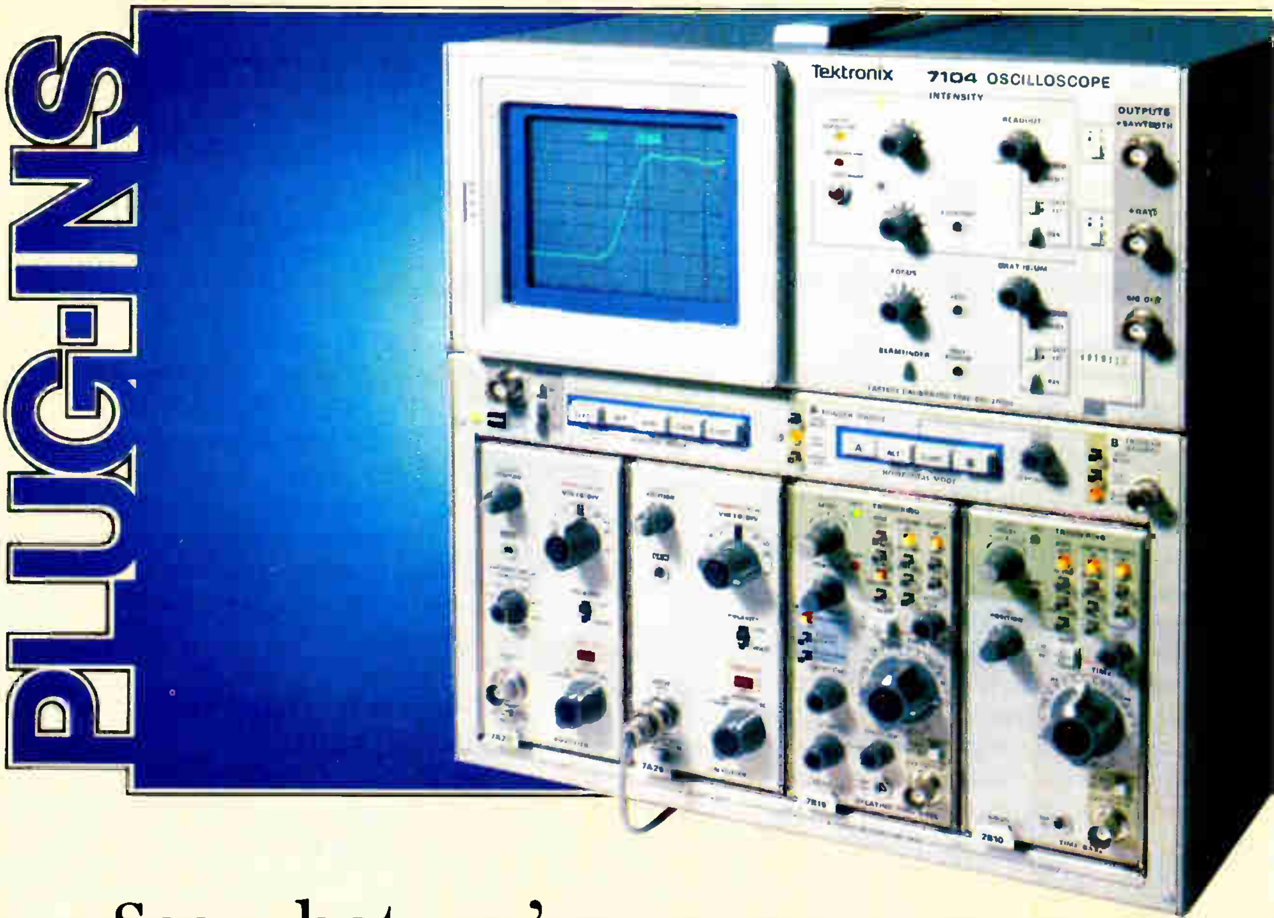

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Color TV camera using CCD imager chips gets first sale

by Charles Cohen, Tokyo bureau manager

Sony beats others to market with very small but costly two-chip commercial product; consumer unit is further off

The start of sales of the world's first commercial color TV camera using charge-coupled-device imager chips supports the frequent forecasts that these devices will soon supplant vidicons in small color cameras.

The initial sale of the cameras, made by Sony Corp., is to All Nippon Airways, which will install them in the cockpits of its 13 747s to allow passengers to view landings and takeoffs. Earlier, Sony supplied the airline with single-pickup vidicon cameras for installation in its Tristars, but the tube cameras are too large for the more crowded 747 cockpit.

Smaller. The new camera, including the control unit attached to its rear, is only 68 millimeters wide by 75 mm high by 198 mm deep (2.7 by 3.0 by 7.8 inches), excluding the lens. In contrast, its vidicon camera is 113 mm wide by 127 mm high by 256 mm deep and has an external camera control unit 191 by 173 by 345 mm.

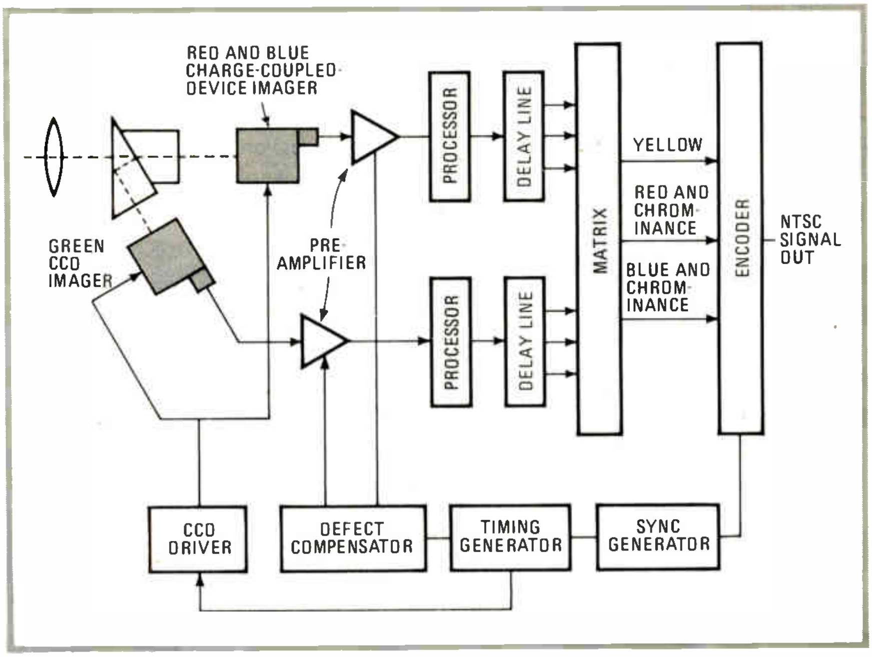
Although at $10,500 the new camera's price is high, it is about 7.4% less expensive than that of the vidicon camera. What's more, images up to 100 times brighter than those producing saturation output do not cause blooming, making it possible to include a sunset and the inside of the cockpit in the same scene. Further, extremely bright light cannot permanently burn the CCD chip, though there is a constant danger of vidicon targets being damaged in this manner.

Sony will sell the new camera to other customers for professional applications, but volume sales will have to wait until the company develops a low-priced camera for the consumer market. The key will be a moderately priced single-CCD imager with about double the pixel density of the present device.

For improved sensitivity and resolution, the new camera uses two imager chips, one to generate the green signal and the other to generate the red and blue signals (see figure). Sensitivity is high because an entire chip is used for green—a stripe filter is not required—and green light generally contains most of the energy in images.

The two chips are offset horizontally by one half the horizontal pixel pitch, and sophisticated signal-processing techniques are used to increase resolution to a value almost as high as what could be obtained with a single chip having twice as many pixels along each horizontal line. Thus a measured optical resolution of 280 test-pattern lines per picture height is obtained even though there are only 245 pixels across the width of each sensor. The measured vertical resolution is 350 lines from 492 pixels.

The CCD imager chips use an interlined geometry in which each cell includes both sensor and storage functions. The storage elements form CCD vertical shift registers at



Eye in the sky. Sony's cockpit-mounted color TV camera for passengers' viewing of takeoff and landing uses two CCD imagers and signal-processing circuits to improve resolution.

one end of the chip. The signal from all sensors is shifted into the vertical shift registers during the vertical blanking interval, and then repeated transfers of the signals in the vertical and horizontal shift registers provide each field of the TV signal.

There are 245 cells horizontally by 492 vertically, with each cell 36 micrometers horizontally by 14 μm vertically. This arrangement gives an optically effective area of 8.8 mm horizontally by 6.8 mm vertically (346 by 271 mils) on a chip 10.6 by 9.1 mm (417 by 358 mils)—which matches the $\frac{2}{3}$-inch optics.

Sensitive area. Because of the complexity of each cell, the size of the sensor is limited to about 17% of the cell area. Bias to provide a potential well under the blue area is provided by a transparent polysilicon layer overlying the sensor oxide, with the thickness of the polysilicon tailored to improve the blue sensitivity. Reflections at the air-polysilicon, polysilicon-oxide, and oxide-silicon interfaces cancel in the blue region.

Sony says that the signal-to-noise ratio is 43 decibels for a scene illumination of 500 lux and the lens opened to *f*2. At maximum sensitivity, the S/N is 33 dB for a scene illumination of 100 lux and a lens opening of *f*1.6.

By readying its camera, Sony has beaten out the competition. Of those working on video cameras using silicon imager chips, Nippon Electric Co. promises a CCD consumer unit by April 1, 1981 [*Electronics*, July 5, 1979, p. 67]. Also at work on CCD cameras are RCA [Jan. 19, 1978, p. 33] and Toshiba [July 20, 1978, p. 63]. On the other hand, Hitachi is well along with an MOS-sensor camera [Sept. 28, 1978, p. 68], and Matsushita has developed a small, light prototype camera based on a single sensor chip having a thin-film heterojunction as the photoconductive layer [Jan. 31, 1980, p. 62].

Great Britain

Personal computer looks to open up the market with an ultralow price

Acting on a belief that there's a big consumer market for a truly low-cost personal computer, British electronics innovator Clive Sinclair has come up with one of the lowest-priced units yet. A book-sized machine called the ZX80, it sells in England for under 100, or some $225.

The first product from Sinclair's new company, Sinclair Research Ltd., Cambridge [*Electronics*, Sept. 13 p. 72], it is based on a Z80 microprocessor. It looks like a programmable calculator without a display, is 9 by 2 by 7 inches, and weighs 12 ounces. A power-supply module, costing $20, is extra.

Others. This is not the first compact educational Z80-based microcomputer. SGS-ATES, for one, has a unit the size of a coffee-table book aimed at a more traditional instructional market. But "we reckon we are three to four times cheaper than anything else," says Sinclair, who has his eyes on household use, for people who want to get a grip on the elements of computing.

Therefore the ZX80 uses the Basic high-level language supported by a firmware interpreter and comes with a specially prepared Basic programming course. "I hope it will remove some of the mystique of computing for a great many people," Sinclair says.

Deliveries in the UK will be started next month and the machine will be introduced in the U. S. shortly thereafter. Kits are being sold, at about $170 (without the power-supply module), through another Sinclair company, Science of Cambridge Ltd.

Cutting costs. To bring the cost to a level that might prize open a consumer market, Sinclair has cut every corner—though, he adds, "not at the expense of reliability," a lesson he learned the hard way with his first pocket calculator. To start with, the ZX80 plugs into a TV aerial to display on a conventional television set 24 lines of up to 32 black characters each on a white background, thus eliminating the need for a display of its own.

Similarly, programs are stored on a conventional household cassette tape recorder. In addition, to keep costs down, Sinclair opted for a fully sealed touch-sensitive keyboard that is rugged and reliable but may take a little getting used to.

Internally, everything has been done to keep the component count low. The display generator circuitry, for example, has been eliminated and the task dumped onto the microprocessor, which therefore has to be

Opener? Sinclair Research hopes to open up the personal computer market with its ZX80: based on a Z80 microprocessor, it costs only $245 with power-supply module.

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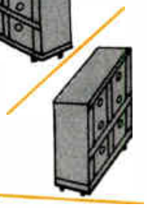

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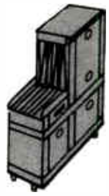

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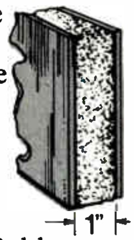

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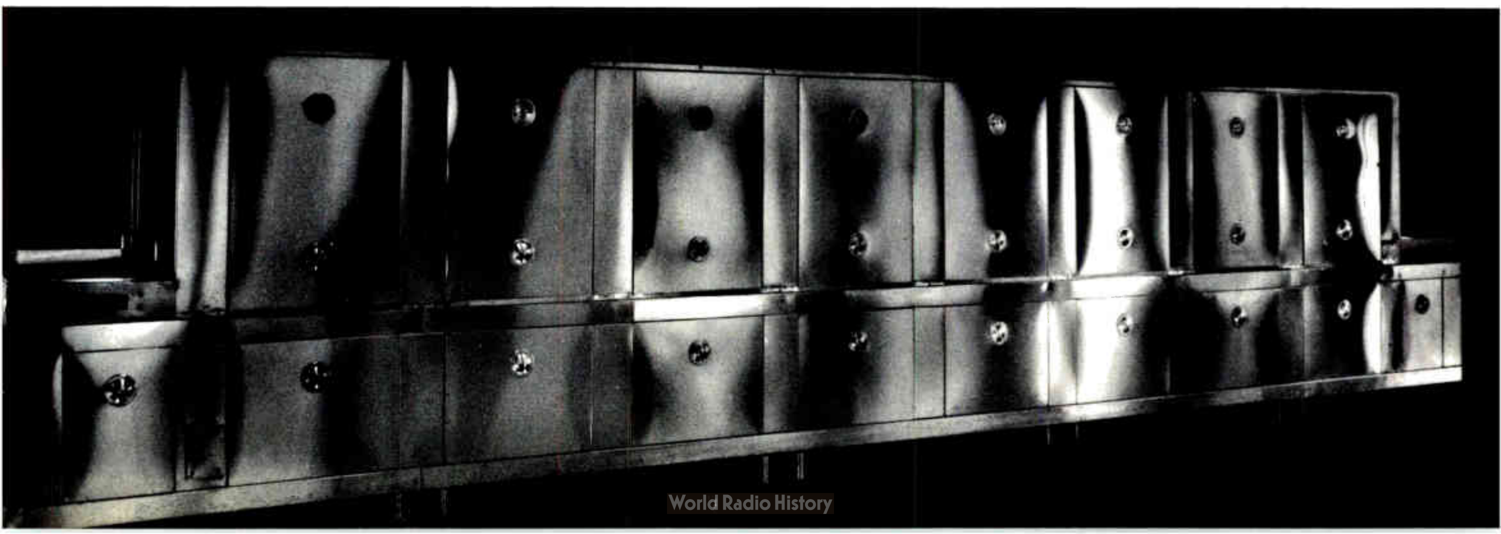

fast. Consequently, the company chose Nippon Electric Co.'s Z80A. Even so, the screen flickers every time a number is keyed in, but, says Sinclair, "that's a small price to pay" for the reduced cost.

Keywords. Like other microcomputer makers, the firm could have opted for Microsoft Basic. But it wanted to build certain features into its machinery—in particular the ability to enter an instruction, such as load or print, by a single keystroke, to speed program entry.

The compressed instruction coding has another advantage, as it occupies less space in the relatively small, 1-kilobyte random-access memory that comes as standard. As a result, Sinclair says, "it's equivalent to 4 kilobytes in a conventional computer." The memory can be expanded by up to 3 kilobytes.

The operating system also has powerful editing facilities, and every statement line is checked for syntax as it is entered at the bottom of the screen, so that only syntactically correct lines can be added to the program list at the top. A marker indentifies a syntax error.

Sinclair's design team, which worked with him on his programmable calculators, has managed to pack the Basic interpreter, character set, operating system, and monitor into a single 32-K read-only memory. Interpreters for other languages can thus be accommodated by changing the ROM and adding a new keyboard overlay to change key functions.

Still to come is a printer interface, a mathematics package with extended Basic, and an extensive range of applications programs. Sinclair is hoping that software houses will cash in on the market he is trying to open by offering already existing packages to run on his firm's hardware. **-Kevin Smith**

West Germany

Nixdorf introduces systems family for distributed data processing

As if to accentuate its strong position in the market for decentralized data-handling equipment, Nixdorf Computer AG is launching a family of distributed data-processing systems—a family with which the West German firm is competing head on with International Business Machines Corp.'s 8100 Information System. The result is a 600-man-year software and hardware development effort, the three models in the 8860 series draw heavily on the know-how the Paderborn-based company has gained with the more than 1,500 decentralized systems it has already installed.

Aimed primarily at medium-sized and large enterprises, the communications- and network-oriented 8860 rounds out Nixdorf's existing computer arsenal. The present lines consist of the 620 and 8850 data collector and preprocessing systems and the 8870 series of autonomous office computers.

These three established families, plus the new entry, give the company a decided edge over the competition, it says, in that they handle all essential tasks for decentralized data processing.

Strong points. For the user, the significance of the 8860 manifests itself in several ways. For one, communications between the various remote systems and work stations in a network need not occur by way of a host computer, which means that nonhierarchical organizations can be configured.

What's more, the remote systems and stations can each develop and compile programs. But the 8860 can also be programmed and controlled by means of down-line loading from a central computer; that way, a computer center can keep tabs on network operations.

Other positive features are the use of the widely employed Cobol language, an extensive package of licensed programs and applications software, and a broad range of peripheral equipment, says Reinhard Mix, who is responsible for 8860 product planning.

Of particular note is the remote diagnostic feature. With this capability, a remotely installed system automatically informs a service computer at a Nixdorf diagnostic center about any existing or impending defects in its subsystems. Using the diagnostic data, service personnel analyze the defect and phone in instructions on how to correct it to a technician. More than half of all possible malfunctions can be taken care of in that way, Mix says.

The family's three systems are software-compatible, and each model can operate either as an autonomous unit or in combination with the others. In a hierarchical network, the higher-ranking computer may be a host system or a member of the 8860 family.

Two-processor CPUs. The central processing units are based on a twin-processor architecture. One processor carries out the instructions; the other controls the data flow on the internal channel and sends the next command to the instruction processor while the latter is executing the previous command. Such overlapping considerably speeds up computer operations.

The three systems, in descending order of memory capacity, expandability, and performance, are the 8860/40, 8860/30, and 8850/5. The model 40 has a magnetic-disk storage capacity ranging from 26 to 264 megabytes and a main memory capacity of 256 to 1,024 kilobytes. It accommodates up to 16 communications lines.

The model 30 features a disk storage capacity of 26 to 132 megabytes and a main memory capacity of 256 to 512 kilobytes. It comes with up to 12 communications lines.

Processing power. The models 30 and 40 come in fixed- and removable-disk versions. In their basic configuration, they already contain a floppy-disk drive with dual-sided diskettes. As for processing power, the two are roughly equivalent to

SCIENCE/SCOPE

A new microwave sensor will allow military weather satellites for the first time to "see" through clouds to monitor meteorological conditions below. The instrument will scan a 1300-kilometer field of view every 1.9 seconds from an altitude of 450 nautical miles, sensing microwave radiation energy reflected from ice, land, and clouds. It will detect rainfall, ice masses, ocean wind speeds, soil moisture content, and other conditions, and relay compiled data within minutes nearly anywhere in the world. The information will help commanders of land, sea, and air forces in their planning of operations that depend on accurate weather forecasts. Hughes, under a U.S. Air Force contract, is to build one prototype and develop computer software for ground processing.

A unique "picture-taking" system comprising five separate sensors will help the U.S. Air Force evaluate which imaging methods may be most useful for advanced airborne applications. The Hughes-developed system consists of one sensor that sees only visible light, another that measures thermal radiation (heat), two active laser systems that detect the amount of reflected light, and a millimeter-wave radar. Variations in the gray tones of panoramas made by the sensors, particularly in those made at night and during inclement weather, reveal the advantages and disadvantages of each.

Military pilots may get help in locating ground targets from far away with a new electronic process that examines TV-like imagery and selects potential targets. The technique, called automatic target cueing, is designed to enhance the performance of such imaging devices as forward-looking infrared (FLIR) systems. It would free pilots from having to study imagery and allow them to concentrate on planning evasive action or performing other tasks. The Hughes approach checks full-frame pictures for likely targets and then further analyzes these highlights for classification. Automatic target cueing has been made feasible by advances in microcircuitry and pattern-recognition techniques.

"High technology" best describes the products, environment, and production processes of the manufacturing division of Hughes Electro-Optical and Data Systems Group. Our major programs include laser rangefinders and designators, thermal imaging systems, and missile launching systems. We have immediate openings for experienced or graduating engineers who seek the challenge and satisfaction of advanced production methods, including computer-aided manufacturing. Send your resume to Dan O'Daly, EDSMD Professional Employment, P.O. Box 92746, Dept. SE, Los Angeles, CA 90009. Or call (213) 641-5510 collect. Equal opportunity M/F/HC.

Saving money through energy management and preventive maintenance has been made easy by a hand-held infrared viewer, according to a leading zipper manufacturer. The Talon company reports that a Hughes Probeye® viewer helped save $96,000 in less than a year by pinpointing energy losses due to such problems as leaks in steam machines. The Probeye viewer creates pictures by sensing heat radiated by objects. An operator merely turns on the viewer and looks through the eyepiece. Warm areas appear much brighter than other objects in the surrounding scene. The device can distinguish temperature differences as small as 0.1°C.

Creating a new world with electronics

HUGHES

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Electronics International

IBM's top-end 8140, Mix says.

The 8860/5 features two diskette drives, each with a 600-kilobyte capacity, and a main memory of 192 kilobytes. It has one communications line to connect it to a larger system.

The key components in the main memories are 16-K MOS random-access memory chips supplied mainly by U. S. firms. Access times for these devices are typically about 360 nanoseconds.

Communication. Depending on the model, the communication lines can accommodate 2, 16, or 32 work stations. The data flow takes place at 9,600 bits per second, and the protocol may be bit- or byte-oriented. Communications processors help reduce the work load on the central processing units.

Purchase prices range from about $15,000 to roughly $300,000, depending on configuration. The family will eventually be offered in the U. S., and Nixdorf's American subsidiary contributed marketing needs to the 8860's development.

A broad range of peripherals is also available. For use at the work stations, the spectrum includes a 100-character-per-second bidirectional matrix printer, a 2,000-character display (25 lines of 80 characters each), and a 45-line-per-second letter-quality printer. For central applications, there are line printers with speeds of 300 to 1,200 lines per minute, magnetic-tape units with nine tracks and 800 or 1,600 bits per inch, and various punched-card readers. **-John Gosch**

Great Britain

Single chip realizes LC video filter using five gyrators and capacitors

One of the few remaining parts in the color television receiver to defy attempts at integration, the tuned-circuit section of the video amplifier, has now been reduced to a single bipolar integrated circuit. The IC, which has been three years in development at Philips Research Laboratories, Redhill, Surrey, replaces an LC filter comprising 20 discrete components—coils, capacitors, and resistors—that are bulky and relatively expensive and need to be individually screened and aligned.

Instead, the new chip, which comes in a 16-pin plastic package, requires no tuning or alignment, has a Q factor that is stable with temperature, and is suitable for mass production. Two versions, one for the European PAL television system and the other for the UK, have been made. However, no production decision has been made so far, says Gordon A. Wilson, who heads the development team.

Bypass. Attempts to integrate filter sections have been blocked till now by the problem of producing an integrated inductance. Wilson and his colleagues bypass this obstacle by using a gyrator connected to a capacitor. The gyrator makes the capacitor function as an inductor by reversing the roles of voltage and current. The complete video filter uses five gyrators terminated by junction capacitors, with the voltage dependence of the latter exploited for tuning.

The filter works on the composite sound and video signal produced after the very high- and ultrahigh-frequency tuning and detection stages. It therefore has to work only up to 6 megahertz, just about the practical limit for the gyrators.

Separating the signals. The filter strips off the intercarrier sound in a two-stage sound trap. The signal is then applied to a single-gyrator resonator to separate luminance and chrominance signals. In the sound channel, a bandpass gyrator pair provides the necessary selectivity.

The chip, described at this week's International Solid State Circuits Conference in San Francisco, is 11 square millimeters (17,050 square mils), uses standard bipolar technol-

ogy, incorporates 567 components, and dissipates 650 milliwatts. An earlier fully operational video gyrator filter was discussed two years ago at the European Solid State Circuits Conference but was not suitable for volume production, as its performance varied from batch to batch.

Tuning the gyrators. "Production spreads of resistors and capacitors can cause the resonant frequency to vary by up to 20%," Wilson says. Therefore his team has added an auxiliary gyrator that tunes itself and the other five gyrators on the chip using a crystal oscillator in the TV color decoder as a stable frequency reference. Since the crystal oscillator is normally used to restore the color subcarrier to the incoming video signal, the auxiliary gyrator, too, is set to nominal resonance at the color subcarrier frequency.

At resonance, a 90° phase shift occurs in the gyrator that is used to produce a control voltage by comparing its incoming and outgoing signals in a phase comparator. The phase-deviation signal is amplified and smoothed to give a capacitor bias potential that tunes the gyrator to the reference frequency. This bias can also be used to control the other gyrators because of the close matching of the components.

Temperature-induced frequency drifts are also compensated for automatically. The resulting temperature dependence is 0.006%.

Matching components. Even closer matching is called for in the sound trap section needed to remove the intercarrier sound signal from the video-recorder teletext output. "The sound trap needs to be accurate to about 0.5%, implying component matching to a similar accuracy," Wilson says. "Resistors are placed close together with the same orientation and are generously dimensioned with large contacts. This minimizes the effects of sheet resistance variations across the chip."

To avoid crosstalk between the various filter signals, the group made extensive use of computer simulations. As a result, says Wilson, "several problem areas were revealed and cured by rerouting." -K. S.

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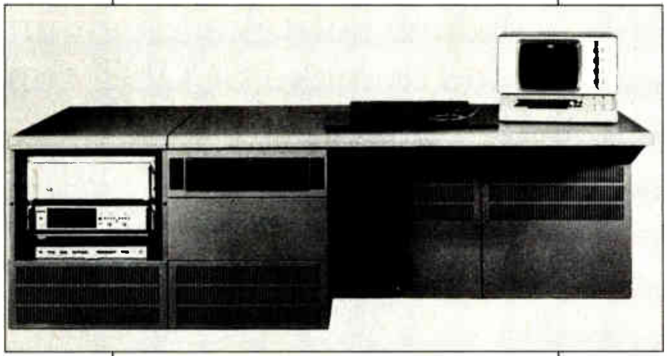

In addition to its super system speed, Series 70 offers faster, more accurate fault isolation. It features multiphase clocks, which let you program timing increments with 20 ns resolution. And its new dynamic current measurement technique lets you track bus-related faults at full system speed.

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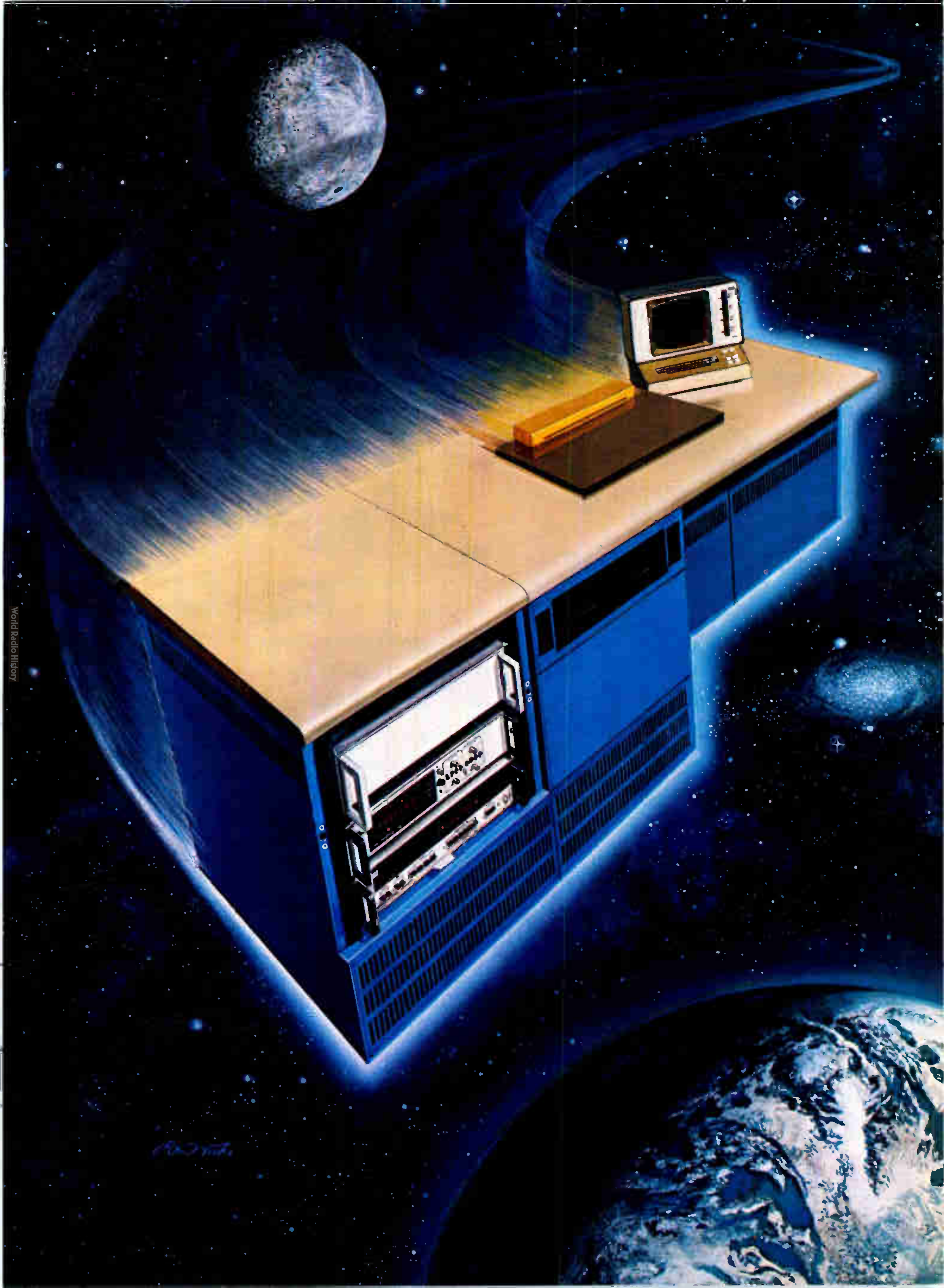


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Within seconds, Olympic officials at Lake Placid will be able to perform complex, computer-like calculations to audit results of competitive events.

They'll have at their fingertips the remarkable computational power of a TI Programmable 59 calculator. And, they'll be able to use it with ease because of a small, cube-shaped memory module that has been *specifically custom designed to do the job for them* — with little experience or training on their part.

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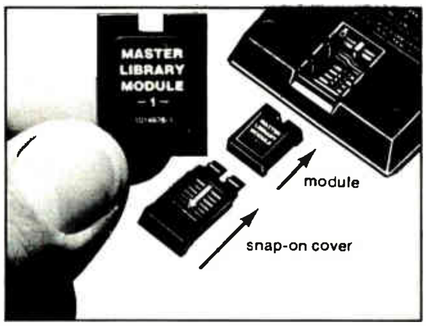
- A truck manufacturer has replaced the charts, graphs, and lengthy slide rule computations its dealers had been using with a TI programmable calculator and custom software module.

As different as these applications are, they represent only a few of the wide range of uses in which Texas Instruments custom Solid State Software™ modules are being used to tailor the powerful TI-58C and TI-59 calculators into easy-to-use, specific application machines.

Plug-in custom software simplifies complex tasks at low cost.

Custom modules for the TI-58C and TI-59 decentralize the analytical and computational power of the computer ... not only for Olympic scorers, combat pilots and petroleum engineers ... but also for many other Texas Instruments customers in business, government and industry. They allow the user to process data and handle complex calculations that would normally require access to a central computer system.



Designed for use with the TI-58C and TI-59 programmable calculators, custom plug-in modules contain pre-written programs developed to customer specifications. Each module contains up to 5,000 program steps, the equivalent of a multi-card library of magnetic cards. Even though the custom modules contain complex software, they are relatively inexpensive to produce and production runs of as few as 250 modules are feasible. In addition to module development, Texas Instruments offers equipment, training and advice to its custom Solid State Software customers.

Custom modules provide a low-cost, mass-producible protectable firmware medium because they are produced with the same advanced micromemory technology used in TI's standard Solid State Software library modules for non-specific applications, available through TI retailers nationwide.

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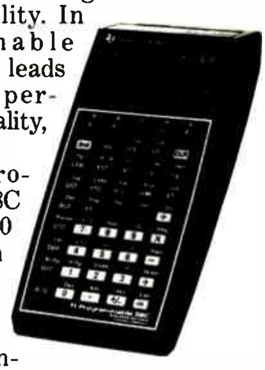

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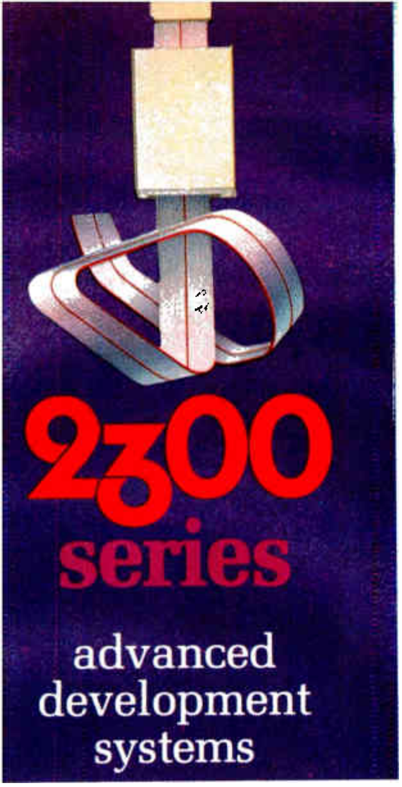

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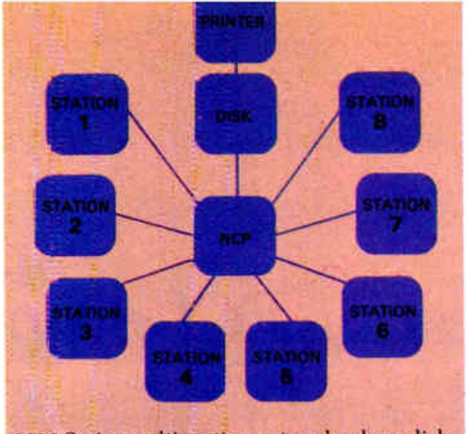

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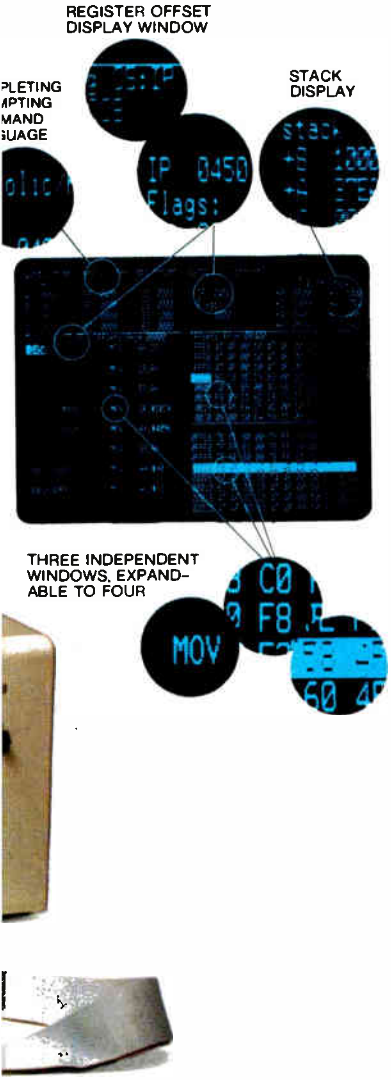

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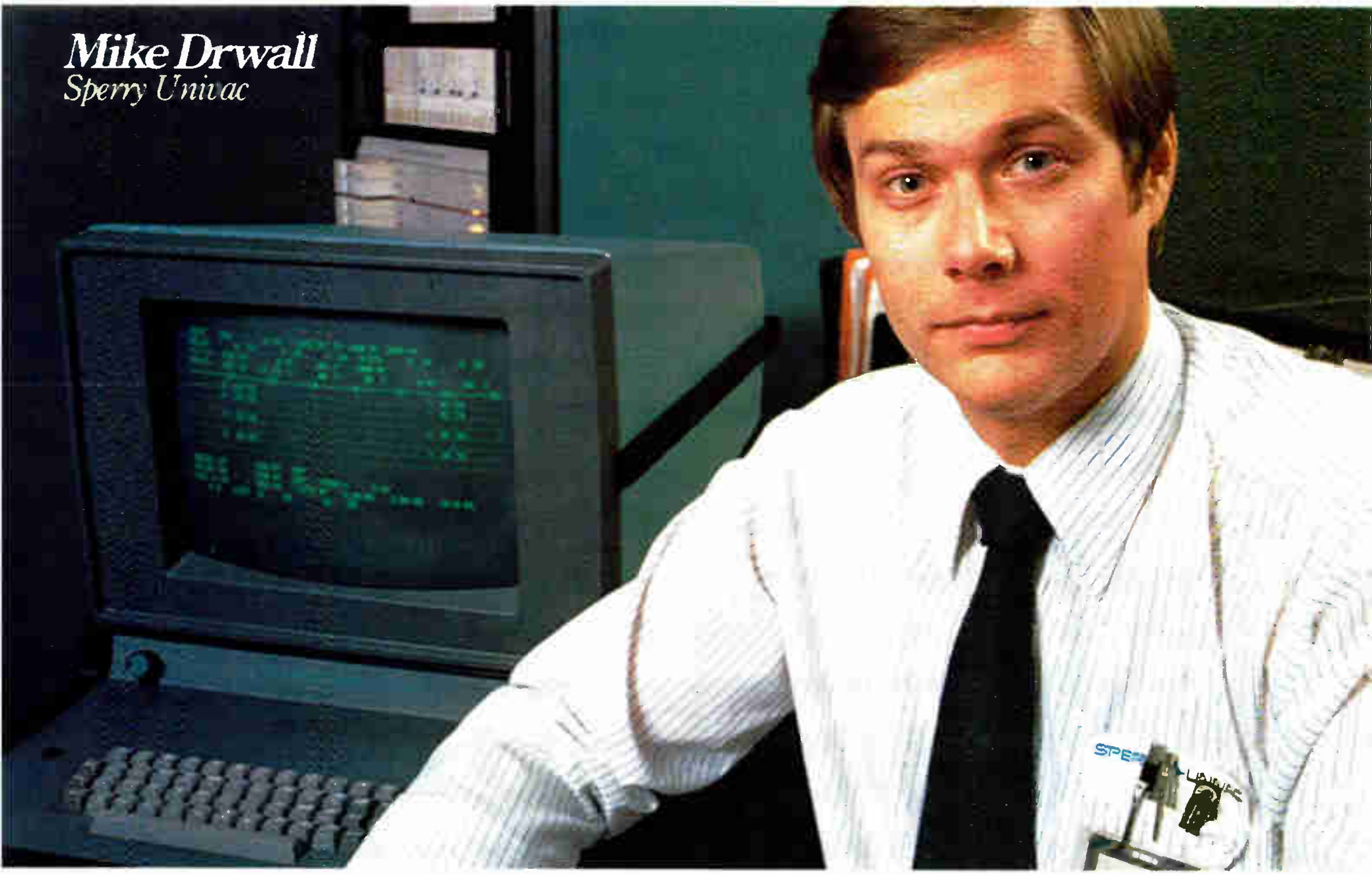
Circle 93 on reader service card

"With the kind of performance expected from Univac computers, testing ECL prop delays is just plain necessary."



Mike Drwall
Sperry Univac

A lot of ECL goes into every one of Univac's 1100 series computers. Mike Drwall knows that. As Quality Test Engineer for Sperry Univac's Semiconductor Control Facility at Minneapolis, Minnesota, he sees about a million ECL parts every month.

Univac tests every one of them for dc and functional performance on a Teradyne J325. But that's not enough.

"Our ECL parts are among the best devices we buy," Drwall says, *"but in a business where speed is the name of the game, we have to test prop delays as well as dc and functional performance."*

To handle the ac testing, Univac uses a Teradyne S357 Pulse Parametric Subsystem.

Why the S357?

"Right now, we're testing 10k series ECL, with prop delays of from 1 to 4 nanoseconds. Soon, we'll be getting 100k parts with subnanosecond delays. We chose the S357 because it will handle subnanosecond ECL just as well as it handles today's parts."

Performance is one reason why Sperry Univac chose the S357. Reliability is another.

"We use a lot of Teradyne gear here at SCF, and production test requirements demand high availability, because we work our systems around the clock."

High performance *and* high reliability. If you're testing ECL devices, you need both. You get both in Teradyne's S357 Pulse Parametric Subsystem, designed as a companion to the J325 Digital IC Test System.

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Budget opens seller's market for EEs

Increase in National Science Foundation outlay as well as record peacetime request for defense raises specter of shortage

by Ray Connolly, Washington bureau manager

Tucked away in the proposed 1980–81 Federal budget is good news for electronics engineers and educators, but disquieting news for employers.

The proposed 15.5% hike in the National Science Foundation's fiscal 1981 spending program to $1.15 billion recognizes at last that U.S. science and engineering education and research and development need a lot more Federal support. The plan to draw more students into engineering and the physical sciences, by providing new funds for cooperative industry-university programs and electronic and computer systems engineering and for upgrading university research laboratories with new computers and instrumentation, is good news for educators and equipment vendors alike. "We need a broader national base for engineering education," one deputy to NSF director Richard Atkinson emphasizes, "so this money will not be concentrated on places like Caltech or MIT, but will help build up smaller schools, too."

The bad news for Government and corporate employees of EEs is that President Carter's push to raise defense procurement and research and development spending by 15.6% to more than $57 billion is sure to add to the already existing shortage of engineers and technicians. And it will give an inflationary boost to both salaries and benefit programs as well.

"NSF's program sounds great for 1985," says one project manager at the Naval Air Rework Facilities in Alameda, Calif., "but that's not going to help us find bodies now" to install, test, and debug improved

MAJOR REQUESTS FOR WEAPONS PROCUREMENT
(in millions of dollars; quantities in parentheses)

	FY 1980	FY 1981	Contractor
ARMY AIRCRAFT			
Advanced Attack Helicopter (AAH)	$176.0	$222.0	Hughes
RC-12 Guardrail modifications	4.3	52.9	Beech, ESL
UH-60A Blackhawk utility helicopter	379.2 (94)	338.6 (80)	—
NAVY AIRCRAFT			
E-2C Hawkeye	209.2 (6)	259.5 (6)	Grumman
EA-6B Prowler	178.4 (6)	148.3 (3)	Grumman
EC-1300 Hercules	98.8 (3)	46.3 (1)	Lockheed
F-14A Tomcat	792.1 (30)	804.0 (24)	Grumman
F/A-18 Hornet	1,434.0 (28)	1,752.5 (48)	McDonnell
P-3C Orion	351.7 (12)	276.9 (8)	Lockheed
SH-60B LAMPS	177.7	220.8	IBM
AIR FORCE AIRCRAFT			
A-10	912.6 (144)	506.8 (60)	Fairchild
B-52G/H avionics modernization	394.4 (31)	323.1 (64)	Boeing
B-52G Cruise missile modification	94.8 (22)	122.4 (40)	Boeing
E-3A Awacs	378.9 (3)	326.2 (2)	Boeing
EF-111A modifications	109.8 (3)	276.9 (12)	Grumman
F-15 Eagle	1,053.2 (60)	869.7 (30)	McDonnell
F-16 Multimission fighter	1,684.3 (175)	1,919.6 (180)	General Dynamics
NATO Awacs (U.S. share)	243.1	377.7	—
ARMY MISSILES			
GSRS General Support Rocket System	131.5 (1,764)	181.2 (2,340)	—
Hellfire Heliborne missile	61.0	75.6	Rockwell/Martin
Patriot, air defense	543.2 (155)	541.6 (183)	Raytheon
U.S. Roland, air defense	308.2 (410)	424.6 (600)	Hughes/Boeing
Tow, antitank (2)	54.9 (6,260)	101.1 (12,000)	Hughes
NAVY MISSILES			
Harm, air-surface	48.0	150.8 (80)	TI
Harpoon, antiship	147.5 (240)	180.1 (240)	McDonnell
Phoenix, air-air	144.2 (60)	142.7 (60)	Hughes
Sparrow, air-air (3)	65.8 (240)	127.5 (770)	Raytheon/GD
Standard ER/MR, air defense (2)	179.5 (535)	242.2 (535)	GD
Tomahawk, cruise weapon system	133.4 (6)	205.6 (20)	GD
AIR FORCE MISSILES			
ALCM Air Launched Cruise Missile	475.4 (225)	745.8 (480)	Lockheed
GLCM Ground Launched Cruise Missile	69.1	187.8 (11)	GD
Sidewinder (3)	87.3 (2,050)	46.1 (260)	Raytheon/Ford
Sparrow	125.3 (1,320)	121.6 (910)	Raytheon/GD
NAVY VESSELS			
CG-47 Aegis cruiser	827.1 (1)	1,631 (2)	not selected
CV SLEP, carrier modernization	50.1	530.6 (1)	not selected
FFG, guided missile frigate	1,260.0 (6)	1,109.3 (4)	not selected
Trident, ballistic missile sub	1,482.8 (1)	1,239.8 (1)	GD
T-AGOS, ocean surveillance ship	35.9 (1)	184.3 (5)	not selected
OTHER PROCUREMENT			
DIVAD Division Air Defense Gun	25.5	260.0 (12)	not selected
MK-15 Phalanx close-in weapon system	132.6 (59)	154.3 (62)	GD
AFSATCOM, Air Force satellite communications system	55.1	102.1	GE
DSCS, Defense satellite communications system	41.0	121.1	GE

(1) includes Marine Corps Procurement (2) includes Navy/Marine Corps Procurement
(3) includes Army/Navy requirements

Source: DOD

navigation, infrared, and sonobuoy detection and to work on missile launch systems on the Lockheed P-3 antisubmarine warfare system. Fiscal 1981 money sought for the P-3 modifications rises 44% to more than $92 million, bringing the program money back up to the fiscal 1979 level.

Workers needed. Defense Secretary Harold Brown's request for record peacetime outlays of $142.7 billion heralds a need for 167,000 more workers in all defense industries next year for a total of nearly 2.2 million jobs. That 8.2% increase comes on top of a 5.2% rise this year.

Congress, with its growing contingent of hawks, is threatening to push those job numbers even higher by adding more billions to fund Cold War II. The resultant swelling demand for EEs "has to severely strain the credibility" of the President's 9.5% guideline for salary increases, says the American Electronics Association's Kenneth C. O. Hagerty. "We hear that a lot of companies are already ignoring it."

The Aerospace Industries Association's personnel specialists note that "there are already two jobs for every person on the market" in the defense industries. They cite special problems of companies like Martin Marietta Aerospace, which reportedly will need more than 1,600 new workers for its Air Force program to begin full-scale development of a new intercontinental missile, the MX, whose fiscal 1981 funding request has soared 88% to $1,568 million.

Beginning salaries for new BSEE graduates now exceed $20,000—often more than their professors earn—according to the Scientific Manpower Commission, even though the number of 1979 graduates rose 14% to 12,213 after four essentially flat years. "But the number is rising quite rapidly and will continue to rise," says Elizabeth Vetter, a member of the private commission. "There is a massive crop of new engineers coming out," she notes, "but this is and always has been a highly cyclical business—with supply usually not synchronized with demand. At present, younger engineers are happy and employers are not." Neither are older engineers, she says, as they press for higher salaries to maintain the separation in pay scales between themselves and the new graduates.

R&D money. The NSF's billion-dollar budget to stimulate research and development may not match the single Air Force MX program, but it is expected to encourage university efforts where new basic research can begin with relatively small outlays. By nearly tripling to $20 million the funds to encourage cooperative programs between industry and universities, and then adding another $20 million to more than double money available for upgrading instrumentation in school laboratories, NSF director Atkinson expects "further interaction between basic and applied programs," as well as help for U. S. industries to "maintain a technical edge in the worldwide competitive environment."

Overall R&D funding in other nonmilitary programs remains essentially flat as dollar increases fail to cover inflation costs. For example:

- National Aeronautics and Space Administration R&D money gets the biggest percentage increase—nearly 10% to $5.6 billion—after the NSF and the Pentagon (up 22% to $16.5 billion), but a significant share of that will be needed to cover increased costs to fix problems with the Space Shuttle, whose launch has been postponed to late 1981. New starts are limited to beginning work on a Gamma Ray Observatory (GRO) satellite for 1985 launch at Maryland's Goddard Space Flight Center, plus money to start development of the National Oceanic Satellite System (NOSS), a joint effort with the Navy and the Commerce Department's National Oceanic and Atmospheric Administration.

The GRO "will improve our knowl-

CHANGES IN FEDERAL RESEARCH AND DEVELOPMENT REQUESTS
(in millions of dollars per fiscal year)

NONMILITARY PROGRAMS	1980	1981
National Science Foundation, total	993.8	1,148
Computer research	18.2	23.3
Physics	63.4	73.5
Materials research	68.5	78.6
Electronics, data processing, and systems engineering	17.6	22.5
Small business/industrial	7.4	18.2
Industry and university cooperative	7.0	20.0
Research facilities and institutions	8.1	20.2
NASA	5,114	5,617
Energy	4,919	5,106
Transportation	353	379
Commerce	371	379
All other	6,424	6,942
Total	18,175	19,571

MILITARY PROGRAMS	Air Force		Army		Navy		Defense agencies	
	1980	1981	1980	1981	1980	1981	1980	1981
Technology base	552	634	459	558	613	773	632	759
Advanced technology base	279	291	141	158	219	162	–	–
Strategic programs	1,582	2,716	242	266	369	383	7	8
Tactical programs	957	1,391	1,490	1,593	2,778	2,774	–	–
Intelligence and communications	669	919	31	44	101	136	361	473
Programwide management and support	987	1,135	482	612	482	608	79	91
Military RDT&E, total	5,026	7,085	2,845	3,233	4,566	4,836	1,080	1,332

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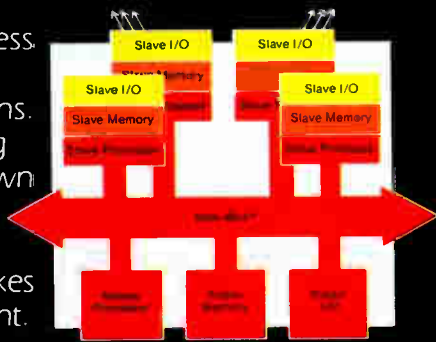

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Circle 97 on reader service card

edge of gamma ray source positions by a factor of 50 to 100," says NASA chief Robert A. Frosch. The NOSS polar-orbiting monitoring system is proposed as a limited operational demonstration of the feasibility of continuously monitoring in near real time such aspects of the earth's oceans as the surface winds, sea state, wave height, surface water temperature, and ice.

- Transportation Department R&D money includes $85 million—roughly 22% of the total—for the Federal Aviation Administration, which has the department's largest electronics component, plus much smaller shares for the Coast Guard and the Urban Mass Transportation Administration. Included in the FAA funds is $5 million to develop an independent Beacon Collision Avoidance System (BCAS) to reduce the threat of midair collisions. On the operations side, the FAA wants $85 million to begin procurement, installation, and testing of the Flight Service Station Automation program in order to speed handling with a computerized system of the increasing demand for such flight services as weather data and routing. Another $52 million is needed, the FAA says, to complete replacement of vacuum-tube VOR/ Vortac air navigation equipment with solid-state hardware. As for the Discrete Address Beacon System (DABS), the FAA wants $20 million in the first year of a multiyear program for replacement of the old air traffic control radar beacon system with the highly automated DABS.
- Department of Energy R&D monies, up only slightly, are discouraging to advocates of photovoltaics and other solar technologies. The Carter Administration's orientation to near-term solutions for U. S. energy problems has produced a cut in funds for photovoltaics R&D to $140 million in fiscal 1981 from this year's $147 million. Moreover, the proportion of the budget request to be spent in the new fiscal year—$118.5 million—is down even further from the fiscal 1980 spending level of $131.5 million. Energy Secretary Charles W. Duncan Jr. says the new photovoltaics budget will stress development of thin films, novel concentrators, and advanced materials.

Military increase. Carter's election year budget forecasts steadily rising military spending programs for electronics and other high technologies for the next five fiscal years. While future political events could alter those estimates, "those are the best numbers we can go by now," says one Washington-based military electronics industry executive, who admits his company "is scrambling just like everyone else to recruit engineers and scientists" in an already tight labor market. Defense Secretary Harold Brown has already told Congress that military spending is projected to rise steadily by about 12% per year until reaching a $225 billion level by fiscal 1985.

Beyond the major weapons systems with high electronics content (see weapons system table), Brown's post-budget briefing for the Congress disclosed that many existing aircraft, ships, and other weapons already in inventory will be upgraded with improved electronics. The Navy fleet rebuilding program calls for adding 97 new ships over the next five years—including one nuclear attack sub each year.

But Brown also disclosed that 46 Knox-class frigates will be retrofitted with the SQR-18A long-range tactical towed-array sonar (Tactas), an antisubmarine warfare a technology that Brown calls "the most important surface ship ASW development in a generation." In addition to the $10 million sought for four more SQR-18A sets next fiscal year, Brown wants nearly $23 million to continue development of the more advanced Surtass—Surveillance Towed-Array Sensor System—labeled the SQR-19A. It is proposed for later production and installation on the more expensive DD-963 destroyer and its DDG-963 guided-missile variation, as well as the CG-47 Aegis cruisers and the FFG-7 Perry-class frigates.

Brown also disclosed that the 25% increase to $221 million in fiscal 1981 for the Navy's SH-60B light airborne multipurpose system—the Lamps Mk III helicopter to be carried on the Aegis cruisers—includes $120 million to buy long-lead-time items for the first 18 production models in fiscal 1982. IBM Corp. is prime contractor for Lamps, which uses the Sikorsky Aircraft Blackhawk helicopter. An Army cutback in the number of Blackhawks it purchases, Brown said, "will increase the Navy's unit cost of the Lamps Mk III"—a program plagued by cost escalation.

Renewed emphasis on tactical ground and air forces also produces some major funding increases in the fiscal 1981 budget requests. The Army, for example, plans to pick a contractor next year to produce the first dozen Division Air Defense gun systems, known as Divad. Each consists of twin 35- or 40-millimeter automated guns and surveillance and automatic tracking radars mounted on a modified M48 tank chassis. The first 12 Divads are budgeted for $183 million, plus nearly $65 million more for RDT&E. Brown says the Army proposes equipping 12 divisions with Divad systems in years to come.

Growing programs. Examples of expanding tactical programs cited by Brown to enhance defense suppression and command/control/communications and C³ countermeasures include:

- More than doubling fiscal 1980 funds of $13.2 million to develop the joint Navy–Air Force Airborne Self-Protection Jamming system (ASPJ to $29 million in fiscal 1981 with another $24 million for fiscal 1982. In addition to proposed Air Force purchases for its 860 General Dynamics F-16 fighters [*Electronics*, Jan. 31, p. 43], Brown says the Army is looking at the ASPJ system to provide countermeasures against radar-controlled weapons for some of its aircraft.
- A 50% jump to $108 million to develop the Joint Tactical Information Distribution System (JTIDS), with a rise projected in fiscal 1982 to $129 million for the jam-resistant digital information distribution system to coordinate ground and air forces in forward combat areas.
- Tripling funds to $63 million for continued development of the Precision Location Strike System (PLSS) after a sharp cutback this year to $15 million from the fiscal 1979 level of $87 million. □

Solid state

Signal processors spur changes

Now simplifying communications problems, the single-chip digital devices will move into other areas of application

by John G. Posa, Solid State Editor

The general-purpose microprocessor, nearing its 10th birthday, has clearly dignified the design of digital electronics—but in an analog universe. However, the analog-to-digital gap could be bridged by a specialized microprocessor with an architecture dedicated to analog applications.

The device is the single-chip digital signal processor, and it is starting its own miniature revolution. Though it evolved out of a need for a single component to fill a variety of telecommunications roles, its sphere of influence will expand and also affect instrumentation, industrial control, and probably even consumer electronics.

Indeed, where there is analog circuitry, there could be a digital signal processor. Programmed with the right equations, these devices replace inductors, capacitors, and operational amplifiers yet oscillate, modulate, mix, filter, code, and decode in real time. And they do so with crystal-controlled accuracy and with a circuit-to-circuit consistency previously unknown to the analog circuit designer. Recognition and synthesis of human speech, fast Fourier transforms, spectral analysis, and other arithmetic-intensive functions fill out this device's list of talents.

Singles club. Four units are being classified as single-chip digital signal processors. Joining the earlier announced Intel Corp. 2920 analog microcomputer [*Electronics*, March 1, 1979, p. 105] and American Microsystems Inc. S2811 signal-processing peripheral [*Electronics*, Aug. 30, 1979, p. 133] are voiceband processors from Nippon Electric Co. and Bell Laboratories, Holmdel, N. J. The last two devices are being announced at this week's International Solid State Circuits Conference (see p. 138).

There are other ICs capable of limited forms of signal processing. In the widest category, these might include Advanced Micro Devices' 9511 arithmetic processor (but not the 9512), Signetics' 8X300 bipolar microcontroller, and Intel's new 8087 mathematics coprocessor, another ISSCC entry. Also, single-chip microcomputers with internal analog-to-digital conversion might suffice. Typical here are AMI's 4-bit S2200, Intel's 8022, and Motorola's upcoming 6805R2. This class of device would either be slow or require a master microprocessor.

The mark of a genuine digital signal processor is its raw number-crunching capability. It has to add and multiply furiously, even to the extent of giving up luxuries like interrupts and branches if necessary. After the analog signal is converted into digital form, it is processed in real time and sent back out into the real world, usually through a digital-to-analog converter. According to Nyquist's theorem, sampling must be done at twice the highest frequency of interest. At 8 kilohertz, the frequency chosen for pulse-code modulation of voiceband signals, that leaves just 125 microseconds for intersample processing. And real time means the device must be fully prepared for each sample.

An often-used benchmark for conventional microprocessors is the time

COMPARISON OF SINGLE-CHIP DIGITAL SIGNAL PROCESSORS

Feature		AMI (S2811)	Intel (2920)	Nippon Electric	Bell Labs (DSP)
Technology		V-MOS	n-MOS/E-PROM	n-MOS	n-MOS
Die size (mil^2)		40,401	47,089	44,088	106,175
Package pins		28	28	28	40
Supplies (V)		+5	+5, −5	+5	+5
Power dissipation (W)		1	0.8	0.9	1.5
Program memory		250 17-bit words of ROM	192 24-bit words of E-PROM	512 23-bit words of ROM	1,024 16-bit words of ROM
Data memory	RAM	128 16-bit words	40 25-bit words	128 16-bit words	128 20-bit words
	ROM	128 16-bit words	—	512 13-bit words	—
Instruction time (ns)		300 (multiply, add, store)	400 (shift, add, store)	250 (multiply)	800 (multiply and accumulate)
Second-order filter sections at 8-kHz sample rate		50	19	55	39
Unique hardware		FIFO input, scratchpad RAM	a-d and d-a converters	stack	parallel bus to access real-time program ROM
Development support		real-time in-circuit emulator	software simulator, assembler	n.a.	assembler

Source: *ELECTRONICS*

required to sort a list of numbers. For the digital signal processor, it is the number of second-order recursive filter sections that can be computed at 8 kHz. This second-order section is a basic building block from which complex higher-order filters can be built by cascading. Four additions, four multiplications, and two move operations might have to be carried out on 16-bit or wider data for each second-order section.

Second orders. As the table shows, these machines are nonetheless capable of performing from 19 to 55 second-order sections if they are programmed for that function alone. For this kind of performance, they must be built differently. "Whereas with normal processing you are performing arithmetic operations only a small percentage of the time and multiplications very rarely, in the signal processor you are predominantly doing arithmetic operations and multiplications, with jumps and conditional branches occurring less often, on a relative scale," says Richard Blasco, a principal designer of AMI's chip.

The table also shows that performance is strongly related to the ability to multiply. In general, the faster the multiplications, the higher the number of filter sections and the more the device is able to stand up to sophisticated algorithms. AMI's, Bell's, and NEC's devices, for example, have on-chip Booth's algorithm multipliers, and their throughput benefits accordingly.

More methods. Besides on-chip multipliers, other architectural arrangements are used to further increase performance. In all four designs, the user has access to microcode because time cannot even be spared for macro-instruction decoding. A lot of pipelining and overlapping of instructions is also evident.

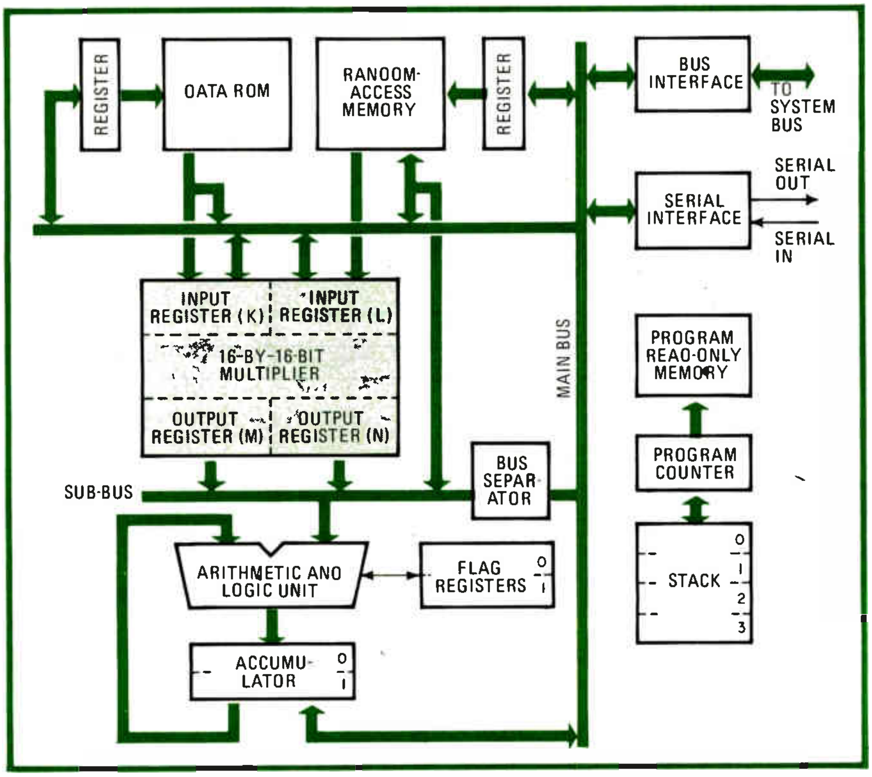
The anatomy of NEC's device, shown in the figure, illustrates some of the other tricks that might be used for more speed. Separate data paths from the data read-only and random-access memories are provided so that the two values can be loaded concurrently. The main bus can be detached from a sub-bus that connects the multiplier to the arithmetic and logic unit. This technique allows accumulator operations and system-bus transfers to occur simultaneously.

Marcian E. Hoff, the Intel employee credited with having designed the general-purpose microprocessor, is now manager of applications research for the Santa Clara, Calif., company and largely responsible for Intel's analog microcomputer. He is enthusiastic about the digital signal processor's accuracy and ability to make one circuit always act like that same circuit. "Once you've built that filter [with a digital signal processor], you know the next one will be identical," he explains. In contrast, "with an op amp and capacitors you have to worry about 1% and 2% tolerances, and when you build a multistage filter, what happens when all the components run through their distributions? How good is that filter going to be?"

Multiplications. The digital signal processor is an excellent use of large-scale and very large-scale integration because one device can serve many markets. This helps to keep volume up and prices down. As for improvements to the signal processors, one might be to make them even more versatile. As mentioned, to meet the number-crunching requirements, the devices trade off some general-purpose features. "Future architectures will tend to get more of that flexibility back," predicts Jim Boddie, a member of Bell Labs' Holmdel technical staff and co-author of its ISSCC paper.

For instance, context switching in the digital signal processor can be awkward and time-consuming because the pipelines must be flushed and refilled with new values for jumps and branches. Not only is Bell Labs' chip better able to switch gears for a new processing environment, but also, it "can do practically anything that a general-purpose microprocessor can do, including bit manipulation," boasts Boddie.

Although the concept and techniques for digital signal processing have been around for decades, "in the past it was limited to special-purpose applications or it was non-real-time," says Intel's Hoff. He feels that now single-chip units "will take over analog processing to the same extent that microprocessors did for digital." But he also notes that "there's still a lot of TTL sold. There will still be a lot of op amps—and capacitors and . . . " □



Construction secrets. NEC's signal processor gains speed with some design tricks. For one, it can separate the main bus from a sub-bus for concurrent operations.

Instrumentation

Signature analysis wins new acclaim

Discovery that the 'field service technique of the '80s' can be retrofitted erases early disappointment

by Martin Marshall, West Coast Computers & Instruments Editor

Back in 1977, signature analysis was introduced as a digital servicing technique that must be designed into a product from its earliest engineering stages. Though it looked promising for the microprocessor-based products of the 1980s, field service managers regretted its inapplicability to their existing product base.

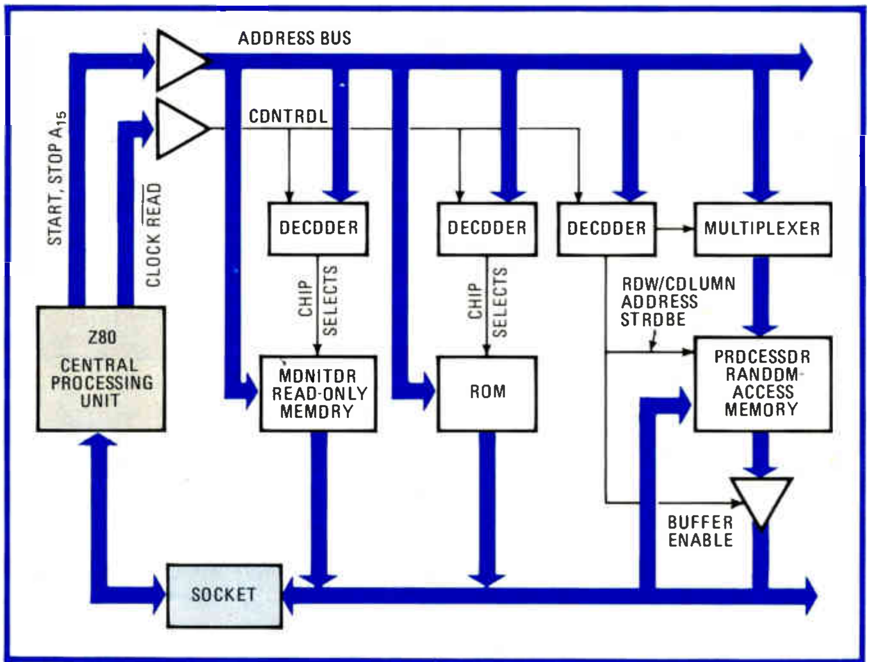
But those regrets have given way to a pleased surprise: familiarity with the technique has led a number of field service organizations to the discovery that, under the right circumstances, signature analysis can indeed be retrofitted.

"We knew about its potential for retrofitting when we introduced the model 5004A signature analyzer, but we didn't want to push retrofitting until people had become familiar with the basic concepts of signature analysis," says Ed White, product manager for signature analysis at Hewlett-Packard Co.'s Santa Clara (Calif.) division. He points out that any existing product that contains a microprocessor as well as some read-only memory, random-access memory, and input/output is a likely candidate for retrofitting.

It may be done very easily, as was the case with the Sorcerer II computer from Exidy Data Systems Inc. of Sunnyvale, Calif. "After three or four man-days of effort, we had a signature analysis program on programmable ROM that we just dropped into a slot in the computer reserved for user programs," notes software engineer David J. Straugas. "No hardware was involved at all."

The effectiveness of signature analysis stems from its origin in the cyclical redundancy check of the computer world. It is far more effective than transition count measurement because its four-digit hexadecimal display encodes timing elements along with data elements to form signatures that can boast a figure of 99.998% nonrepeatability.

The net effect of using signature analysis can be a tremendous reduction in the number of spare boards that a company must keep at its



SIGNATURE ANALYZER		Z80	
Input	Edge	Signal	Pin
Start	falling	A_{15}	5
Stop	falling	A_{15}	5
Clock	falling	$\overline{RD}$	21

ADDRESS BUS SIGNATURE TABLE

Address	Pin	Signature	Address	Pin	Signature
A_{15}	5	755P	A_7	37	52F8
A_{14}	4	3827	A_6	36	UPFH
A_{13}	3	3C96	A_5	35	OAFA
A_{12}	2	HAP7	A_4	34	5H21
A_{11}	1	1293	A_3	33	7F7F
A_{10}	40	HPPD	A_2	32	CCCC
A_9	39	2H70	A_1	31	5555
A_8	38	HC89	A_0	30	UUUU

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repair depots to maintain a "board-swap" repair program. Take Lanier Business Products Inc. of Atlanta. It found retrofitting signature analysis to be a good alternative to maintaining a large number of spare boards for its No-Problem typewriter. "Before we retrofitted signature analysis, we had to keep about 25% to 30% of our boards in a 'float' status. They were all repaired at the factory," recalls national field service manager Herschel McCroan. "Now we have signature analysis at 25 service centers, and in a few months we will have another 25 or so. In the time that we have been using signature analysis, we find that almost 100% of our boards can be repaired using it. Only an extremely small percentage of our boards now come back."

Because of the microprocessor orientation of its No-Problem typewriter, Lanier found retrofitting an easy task. "We have one signature analysis PROM that we substitute for the bootstrap PROM to check that the system can load a program successfully," McCroan says. "Then we use another signature analysis program on floppy diskette to check the rest." Together, the PROM and diskette required about three man-months of development to accomplish the retrofit. Equally important, McCroan noted, is the fact that only one week was required to teach field technicians the technique.

Eastman Kodak Co. of Rochester, N.Y., which designed signature analysis into a microprocessor-controlled photoprinter, has had even more impressive results. "In the 15 months that we have used signature analysis, only four or five boards out of hundreds could not be debugged using it," reports a company spokesman. "It has almost eliminated board float at our 36 stocking locations in the U.S."

The signature analysis bandwagon has also captured the imagination of Hewlett-Packard's fellow instrument makers. It is used in several new products coming from Racal-Dana Instruments Inc. of Irvine, Calif., John Fluke Manufacturing Co. of Mountlake Terrace, Wash., and Tektronix Inc. of Beaverton, Ore. "Signature analysis is not mandated as a company policy, because not all products are suited for it, but we do encourage its use in our designs," observes a Tektronix spokesman.

The competitive bandwagon has also grown, with a logic analyzer–signature analyzer offered by Tektronix, an in-circuit emulator–signature analyzer offered by Millennium Systems Inc. of Cupertino, Calif., and a series of half-priced competitors of the HP 5004A produced by Phoenix Digital Corp. of Phoenix and by Kurz-Kasch Inc. of Dayton, Ohio.

No panacea. Still, not everyone is sold on the prospects of signature analysis. Bill Schwartz, service manager for Hugin Cash Register Inc. of Hawthorne, N.Y., for one, asserts: "I can find a problem on our model H51B cash register with a scope faster than it takes me to set up a signature analyzer." The H51B was retrofitted for signature analysis after its design was completed. Schwartz objects to the fact that to troubleshoot with signature analysis he must "cut cladding" at six points on the board. The actual retrofit, he reports, was also more complicated than the simple dropping of a PROM into a socket reported by other users. It entailed the development of a board with a PROM and a resistor network IC, along with a switch and a DIP clip, one that fits over dual in-line packages, in order to track down signatures on the bus lines.

This last task, the cutting of bus lines, or putting them in a high-impedance state in order to track signatures through a bus loop, has become the central question in determining the feasibility of signature analysis for a given product retrofit. The problem is that, unless there is a way to break a bus loop, a bug contained in any member of the loop will propagate bad signatures all the way around the loop. HP's answer is to put the bus in a high-impedance state in the design stage or to install a socketed DIP jumper across the bus lines. This allows the technique of "free running" the microprocessor—having it execute no-operation codes while it is incrementing its addresses—in order to verify the bus-connected circuitry. □

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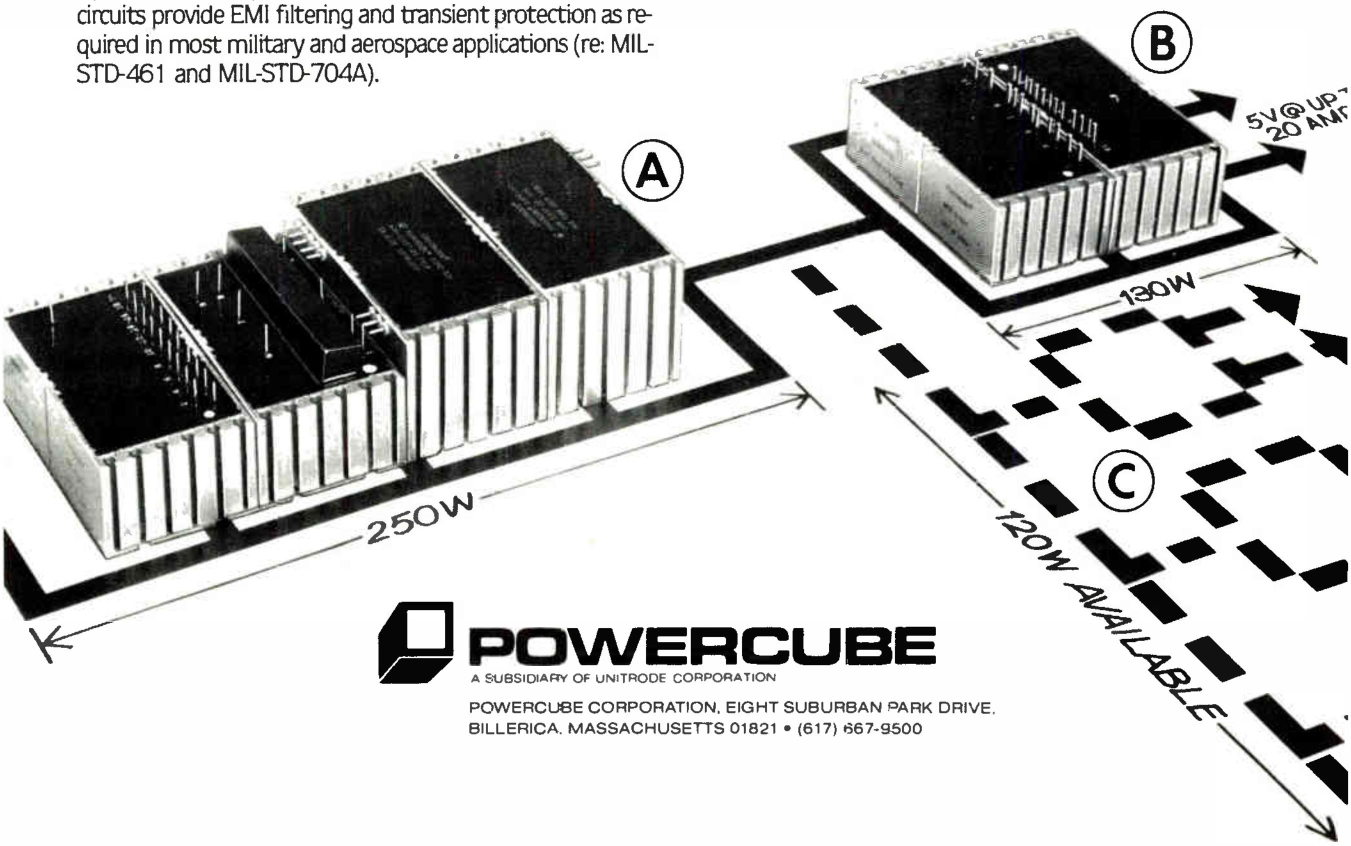

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Packaging & production

Bells, whistles haunt chip houses

IC firms tell semiconductor equipment makers they prefer basic machines with CRTs, microprocessors as options

by Bruce LeBoss, San Francisco regional bureau manager

Does semiconductor equipment design reflect the needs of the industry, or have equipment suppliers burdened users with too much in the way of microprocessors and other advanced technology? Those questions were the subject of a panel discussion late last month at the Advanced Semiconductor Equipment Exposition in San Jose, Calif.

With the exception of high-vacuum systems and equipment for depositing thin film, small users of semiconductor equipment are not getting a fair shake from suppliers, especially of masking and ancillary equipment, says James Gable, vice president of operations at Micro Power Systems Inc., Santa Clara, Calif. As a user interested primarily in basic equipment, Gable contends that "the ancillary equipment people are too involved in adding bells and whistles not needed to perform the basic function."

Though nice adjuncts, says Gable, such features increase complexity, cost, and maintenance requirements. Yet the basic unit made by many U. S. manufacturers today incorporates such adjuncts as standard, and "you take it, or else," he says. He would prefer to see features like microprocessors and cathode-ray-tube readouts kept as optional extras. Meantime, he believes that, as a result, overseas manfacturers who concentrate more on building basic units are coming to the U. S. and selling them at about half the price of domestic equipment.

However, equipment suppliers "have to look at where the bulk of the market is," one that requires more complexity by its very volume, points out Larry D. Hartsough, senior staff scientist in the advanced development department at Perkin-Elmer Corp.'s Ultek division in Palo Alto, Calif. As processes become more complex, the chances for human error become greater. What's more, he says, "the industry tells us: 'We need the bells and whistles to ensure that equipment gives us the product that we want time after time, reliably, with high throughput, and more efficiency.' "

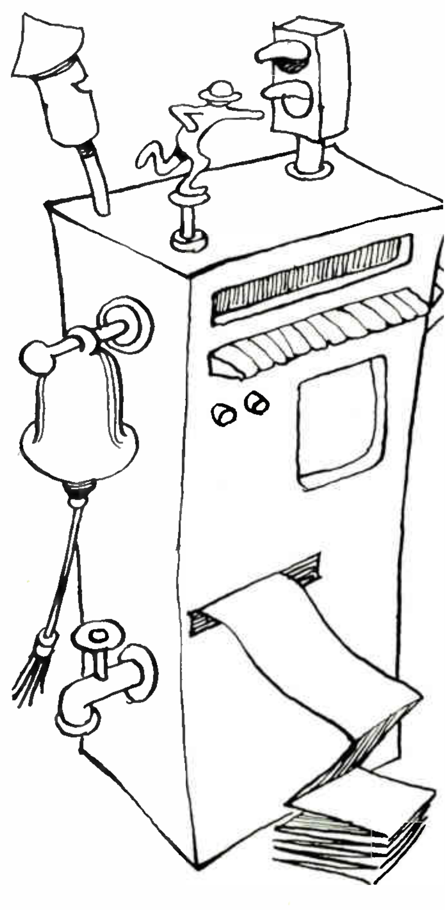
A fairly large firm, Hartsough says, "cannot respond to the needs of all the users. It has to evaluate where the biggest payback comes from— standardized equipment with very few specials or with none at all."

Too much. But the needs of large users may not be met, either. Ron Schoenholzer, manager of equipment engineering at National Semiconductor Corp., Santa Clara, Calif., wonders why he has to pay out the same $200,000 for a small wafer startup line as for a large one. "I'm buying a Cadillac, and I only need a Volkswagen," he states.

Schoenholzer contends that equipment vendors have jumped on the microprocessor bandwagon too soon. "Everything has to be microprocessor-controlled," he complains. Half the original-equipment manufacturers who supply such capability cannot repair it themselves, he claims.

"The world is locked into the microprocessor," says the National manager, who further notes that he has sent three major microprocessor-based systems back "because the manufacturer couldn't even get them to run. There are no manual overrides, and everybody says: 'It's solid-state, it has got to work forever.' Well, it doesn't work if you can't turn it on."

According to Rick Heim, vice president of product planning at Computervision Corp.'s Cobilt division, Santa Clara, it is the users that "have forced the equipment manufacturers to go into microprocessor-controlled systems. Some users want a very simple piece of equipment, while others want that same piece of equipment to do far more and are willing to pay those extra dollars. "Without the microprocessor we could not meet the simultaneous



demands for simple and for sophisticated equipment."

Hartsough suggests a user with specific needs might look to a smaller equipment manufacturer. National's Schoenholzer agrees that such manufacturers, unlike the big ones, are generally willing to meet customers' requirements. But often, because they have built few systems that meet those needs, the user is reluctant to buy from them, says Robert Blackwood, vice president of marketing and engineering at Fluoroware Systems Corp., Chaska, Minn. Blackwood asks such users to be "willing to take a shot" with the small equipment manufacturer, rather than say to him: " 'Well, you haven't sold 200 of them and you haven't been doing it for the last 15 years. Therefore, we obviously can't do business with you.' "

Yet another problem area is field service support, according to Micro Power Systems' Gable. "Equipment builders don't have the support team they should have." What's more, he adds, "trying to get repair parts out of them is difficult. They say they have repair parts stores, but when you try to get a part, they don't have it and they don't recognize the fact that they've got a user who is down."

No match. National's Schoenholzer, however, claims that sets of spare parts often include "four fuses, light bulbs—not what keeps equipment running." He tells of buying two major pieces of capital equipment with sequential serial numbers. "The whole idea was if one went down, the unit sitting next to it was an ideal spare parts bank—but not one pc card was interchangeable," he states.

In the wake of such experiences, Schoenholzer says his group of semiconductor production equipment users at National has opted against the microprocessor-control route in many areas "because we don't feel the microprocessor application people are mature enough. It's like buying a refrigerator from Sears," he says. "You really don't know who built the equipment until you open it up and look in the back." □

Electronics abroad

For Scandinavia, vagaries fill 1980

With export-oriented economies, Sweden's growth rate should dip, Denmark looks at a no-growth year, and Norway should come back

by Arthur Erikson, Managing Editor, International

Like cross-country skiers who have trekked over the same course several times, Nordic businessmen this year see little chance they will round a corner and find themselves in terrain they simply cannot handle. Yet they know as well that 1980 will not bring 12 months of easy gliding.

Much depends on the ups and downs of world trade. Sweden, Denmark, and Norway all have export-oriented economies, and any serious general setback in global business would turn the year into a hard slog. And a downturn in export business would worsen the already high balance-of-trade deficits of Sweden and Denmark, which have large bills to pay for energy imports.

Even with world trade holding at reasonable levels, the Swedish economy, dominant in Scandinavia, figures to slip back a little this year in growth rate. For the Danish economy, second largest in the region, it looks even bleaker—a no-growth year. In contrast, Norway should be on the comeback after its year of austerity in 1979.

The arithmetic of growth, then, produces a sum that marks a slowdown in the expansion of electronics markets in Scandinavia. As usual, computer and communications gear makers expect to register adequate advances. But the malaise that comes with saturation lingers on in entertainment electronics markets. All told, equipment markets this year in the three countries should run some $2.691 billion, according to a survey made by *Electronics* last fall (see chart). The rise here is 6.5%, well below the 11% logged last year, when equipment sales totaled an estimated $2.461 billion.

Components markets figure to suffer much the same sort of slowdown. They are forecast to total $661 million, up 3.8% over an estimated $637 million for 1979. Last year's rise was 6.7%

Sweden. The Swedes managed to turn in one of the best growth records in Western Europe last year, boosting their output of goods and services by 4.2%. So they went into 1980 with a lot of momentum—and some problems as well.

For one thing, the unions insist that workers got short shrift last year, holding the line on wage demands while the companies made high profits. So there is a drive now for double-digit wage boosts. For another, a lot of the country's attention has been diverted in recent months by its upcoming referendum on nuclear power.

Because the solutions to these problems are still far from clear, there is an understandable spread in current forecasts for economic growth. They range between 2.5% and 3.5%. But despite the slight slowdown that forecasters say is in the offing, the economy looks strong enough to ensure a solid year for electronic equipment suppliers. *Electronics'* survey suggests 1980 equipment markets of $1.313 billion, a gain of 9.8% over the $1.196 billion estimate for 1979.

Swedish entertainment electronics producers were the first in Western Europe to bask in a color TV boom and, inevitably, also the first to suffer the stagnation that comes with saturation. The logical sequel would make them the first to benefit from a burgeoning replacement market, and some dealers now think that

SCANDINAVIAN ELECTRONICS MARKETS FORECAST
(IN MILLIONS OF DOLLARS)

	1978	1979	1980
Total assembled equipment	2,217	2,461	2,691
Consumer electronics	833	865	903
Communications equipment	469	559	620
Computers and related hardware	584	673	778
Industrial electronics	157	176	192
Medical electronics	87	91	90
Test and measurement equipment	57	64	71
Power supplies	30	33	37
Total components	596	637	661
Passive and electromechanical	359	380	388
Discrete semiconductors	64	66	69
Integrated circuits	81	105	121
Tubes	92	86	83

(Exchange rates: Denmark, $1 = 5.3 kroner; Norway, $1 = 5.0 kroner; Sweden, $1 = 4.25 krona)

Note: Estimates in this chart are consensus estimates of consumption of electronic equipment obtained from an *Electronics* survey made in September and October 1979. Domestic hardware is valued at factory sales, prices and imports at landed costs.

has started. After the usual post-Christmas lull, late January brought a spurt in sales as Swedes—many of them owners of old sets—made sure that they would have a good view of the Winter Olympics.

No matter how well the color market holds up, set makers cannot expect to match the communications gear producers in market gains. Their domestic sales of electronics hardware will rise a solid 11.2% to $263 million this year.

But for all the strong growth in sight for communications gear producers, they cannot count on matching strides with the computer people. Their markets will run some $381 million this year, the survey predicts. That works out to a 14.9% hike over last year's $332 million.

Denmark. One characteristic that Danes feel sets them apart from their Nordic neighbors is their buoyant spirit. But there are few jolly Danes at the moment among the ranks of economic forecasters. After turning in a respectable 2.5% rise last year, the Danish economy now seems mired in a no-growth mix—double-digit inflation, a crushing payments deficit, a low level of capital investment, and a minority government that cannot force tough economic programs through.

It is not the kind of climate that makes for buoyant electronic hardware markets. *Electronics'* survey projects equipment sales of $752 million in Denmark for 1980. That works out to a nominal gain of 7%, whose luster tarnishes badly when exposed alongside the expected inflation rate of about 10%. The leader and the laggard are exactly what one would expect. Computers, the survey suggests, are set for a rise of 14.3% to $256 million, whereas consumer electronics markets will edge up less than 2% to $257 million.

Norway. North Sea oil puts Norway in a class of its own—it ranks both as an industrial country and also as a net energy exporter. After a spate of spending oil revenues before they actually came in, the Norwegian government last year cooled the country's overheated economy in an icy bath of austerity, freezing wages and prices. That slowed growth but at the same time shrank the inflation rate to 5% and drastically improved the balance of payments.

Now, the austerity measures have expired and the economy is on the thaw. As a result, the gross domestic product should rebound to something like 3.75% growth this year, compared with last year's 3.0%. But, warns a government economist, "without oil and shipping, the figure would be only 1.75%."

So Norway seems set to regain its rank, relinquished during the year of austerity, as the fastest-growing electronics market in Western Europe, albeit the smallest of those surveyed. *Electronics'* charts equipment markets in the country for 1980 at $634 million, 19.2% over the estimated $532 million for 1979. □

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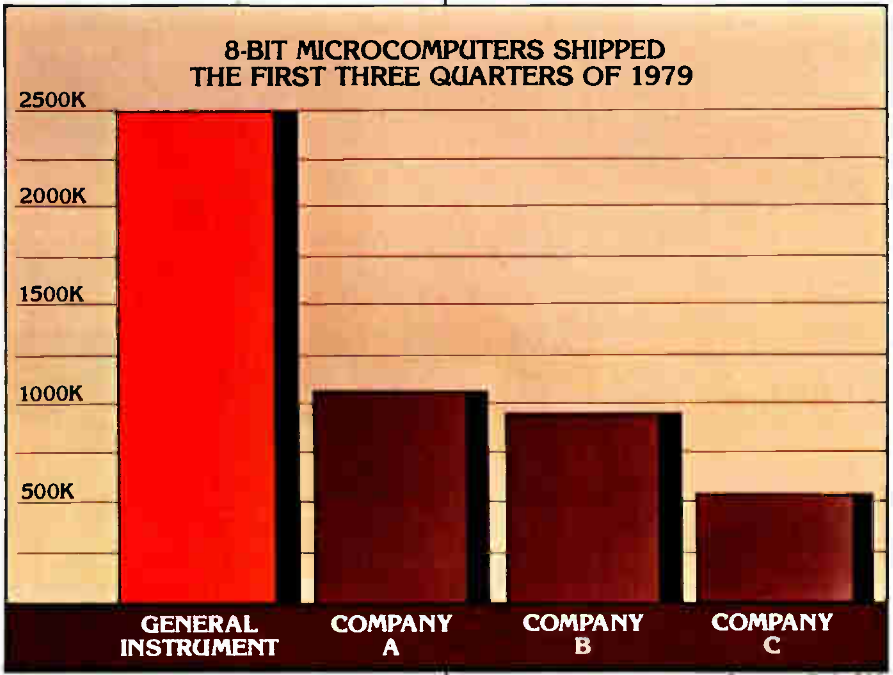

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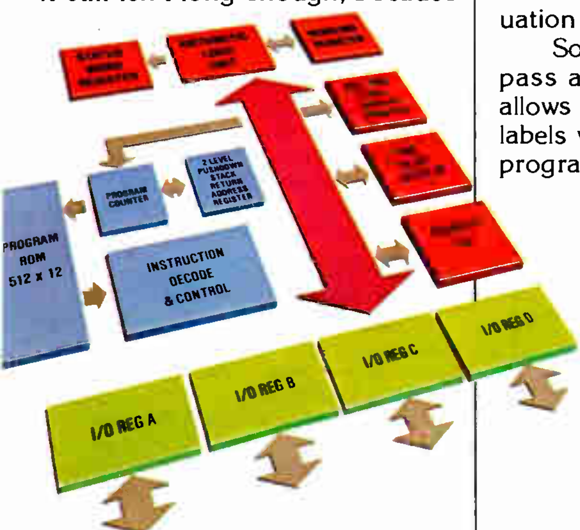

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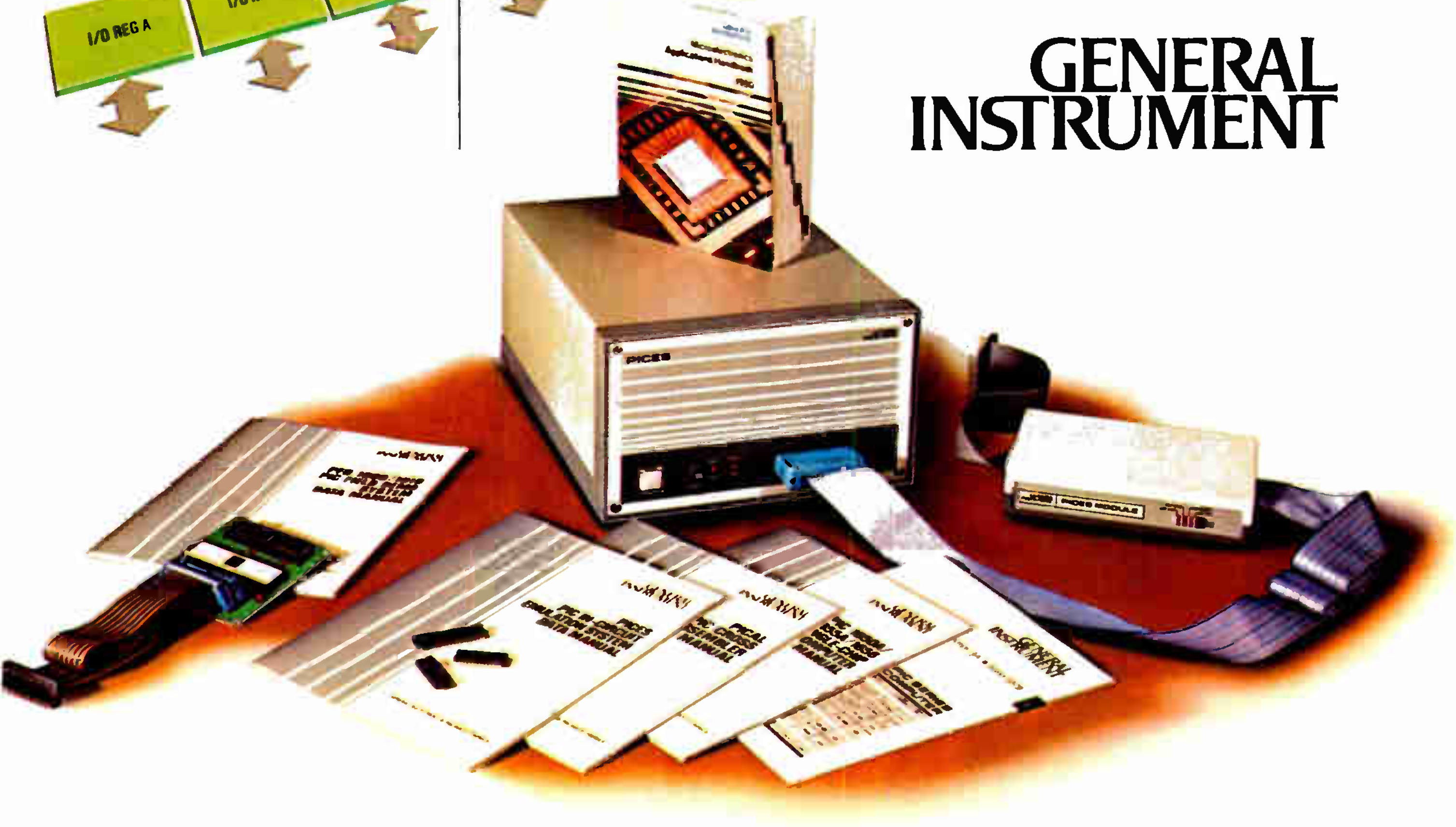

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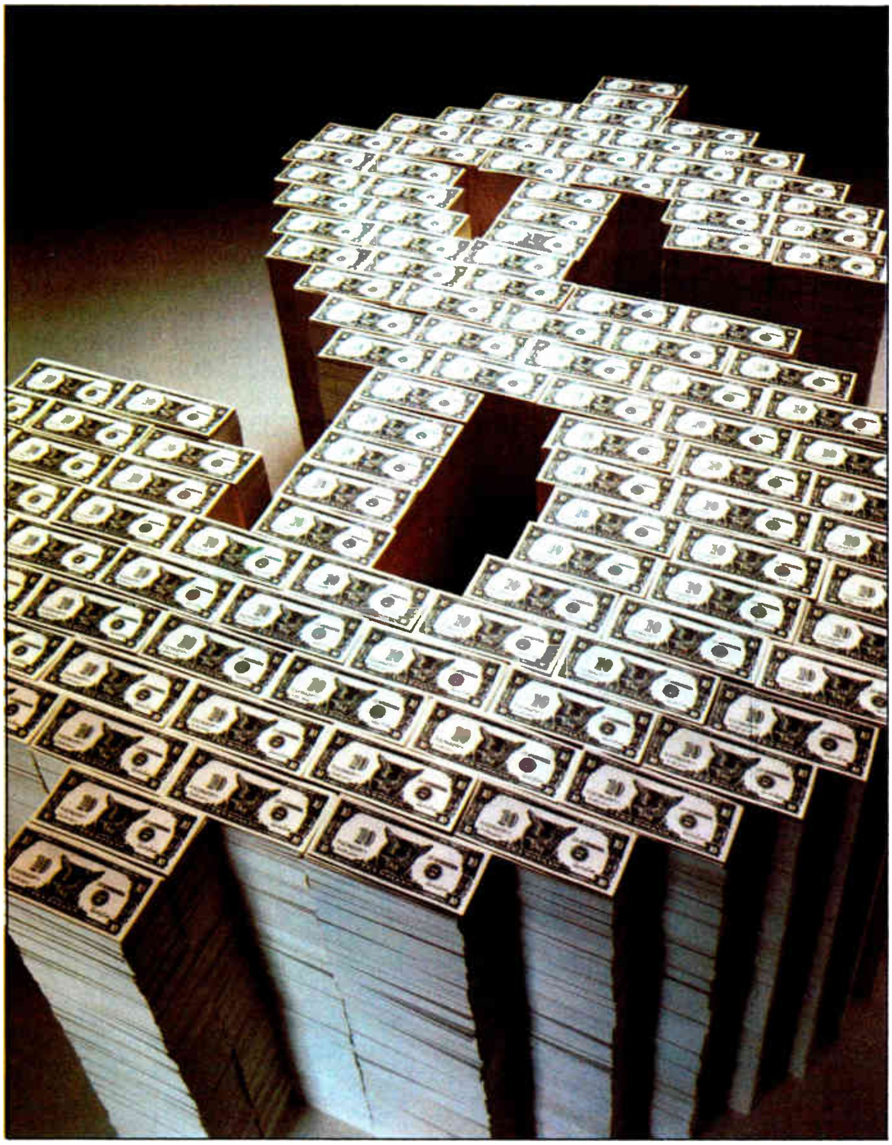

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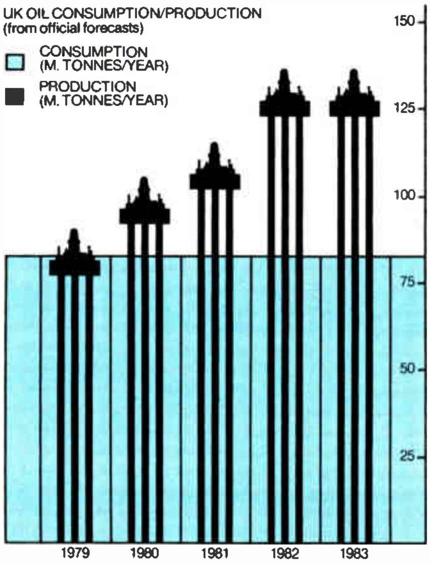

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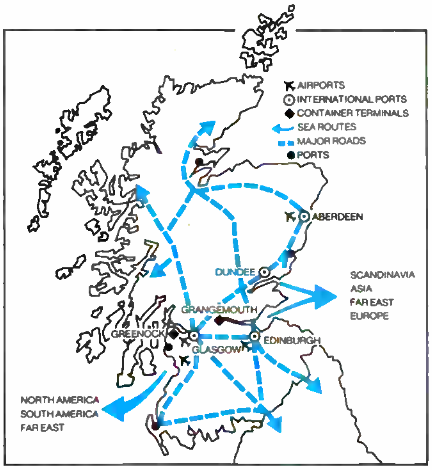

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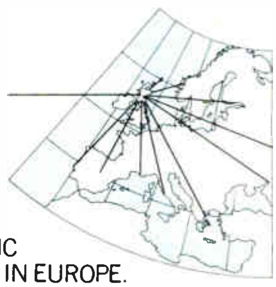

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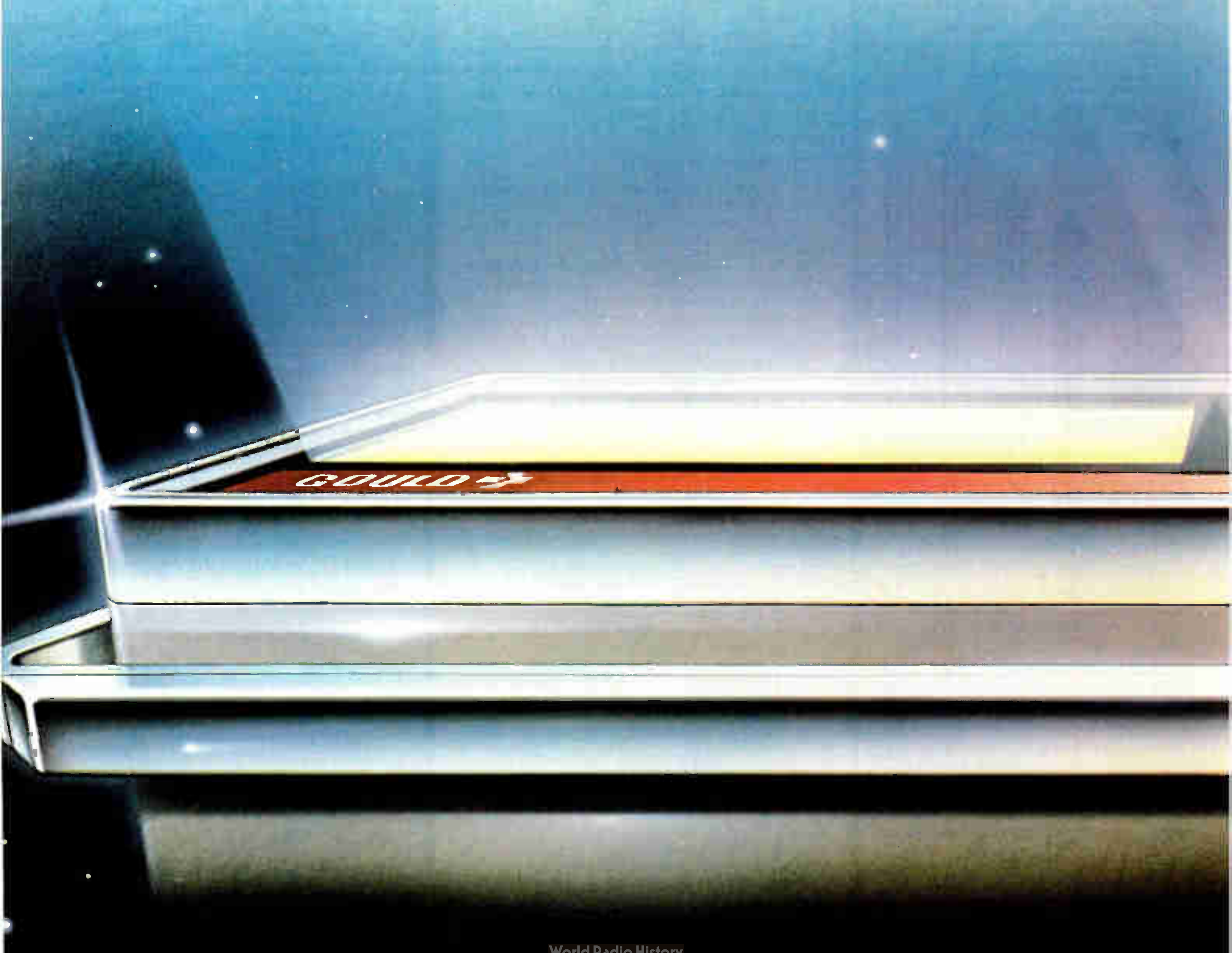

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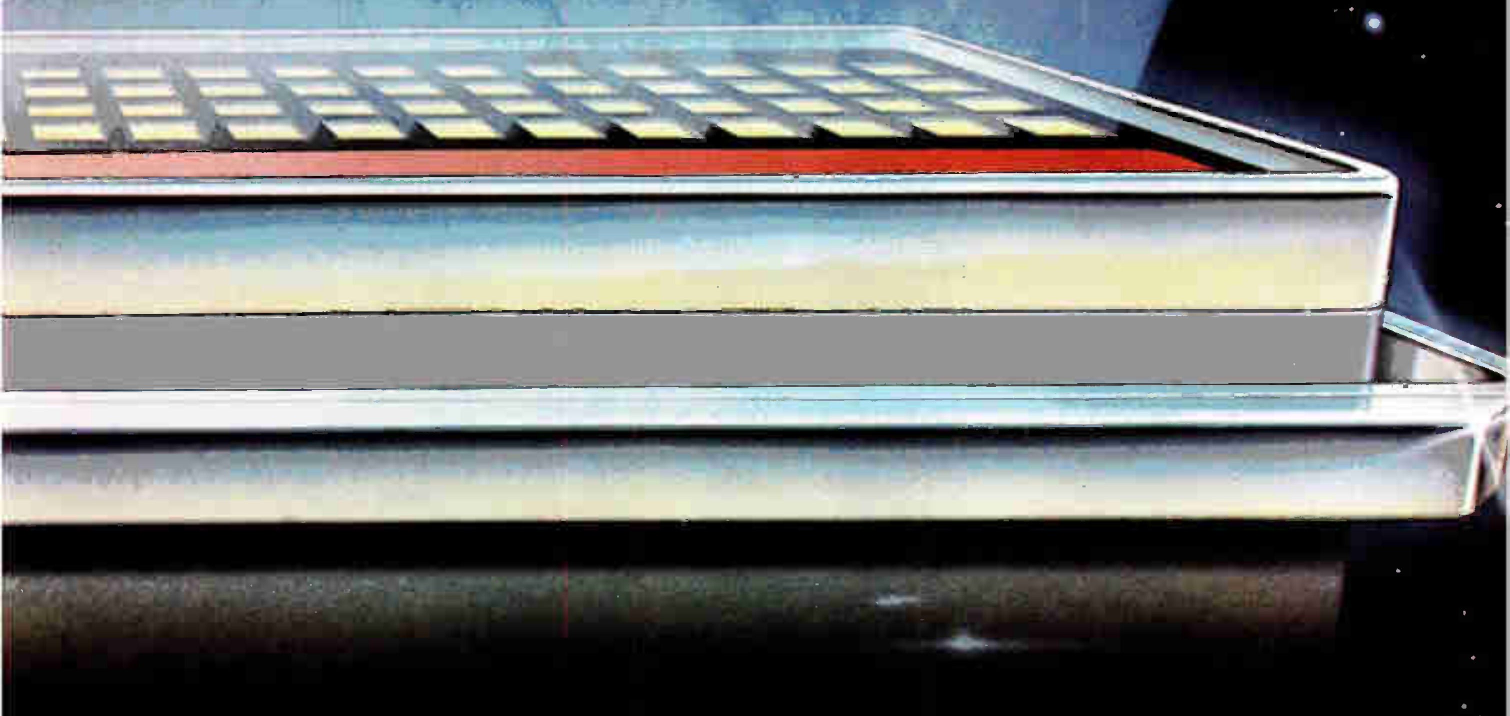

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LSI processor mirrors high-performance minicomputer

Parallel-pipelined MOS chip machine matches Eclipse C/350's throughput; two optional ICs support floating-point and commercial extensions

by Michael Druke, Ronald Gusowski, and Edward Buckley, *Data General Corp., Westboro, Mass.*
and Dean Carberry, Roger March, and Richard Feaver, *Data General MOS Engineering, Sunnyvale, Calif.*

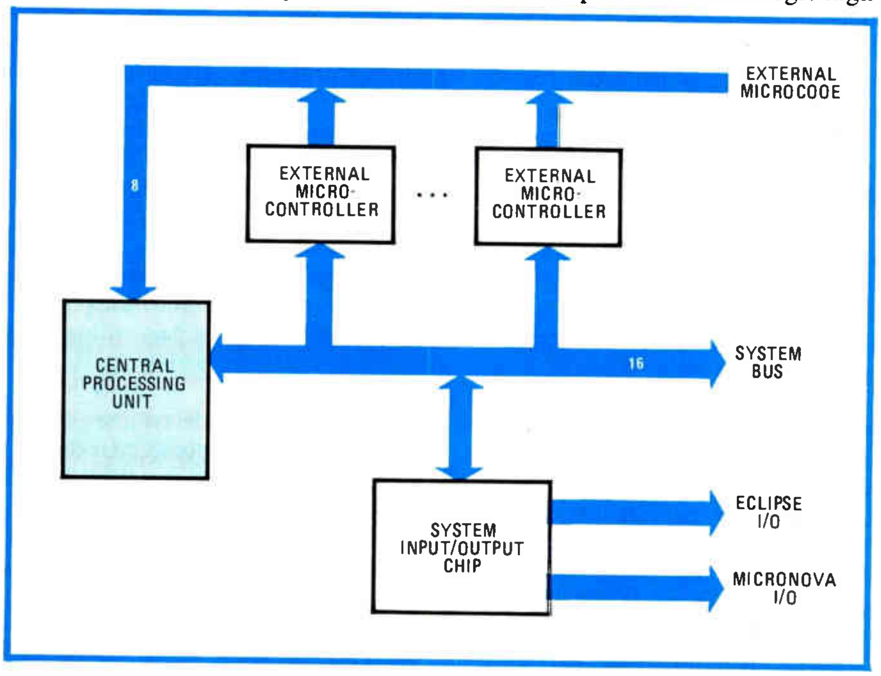
☐ A new family of n-channel MOS integrated circuits emulates the architecture of the high-end Eclipse minicomputer. The chip set, called the microEclipse, forms the basis of an entire spectrum of system configurations ranging from compact single-board computers to high-performance minicomputers. The new architecture was planned and subdivided to be as fast as the existing TTL implementations of the Eclipse.

These implementations include the S140, a small general-purpose minicomputer; the S250, a larger machine capable of array and floating-point processing; and the C/350, a high-end minicomputer with floating-point and instruction set extensions aimed at the large data-processing applications of banks, insurance companies, etc. At the top of the line is the M600, a multiple-function mainframe-sized computer.

The microEclipse family is based on a central-processing-unit chip that executes a kernel of the Eclipse C/350 instruction set and, like the three smaller Eclipse minicomputers, supports up to 2 megabytes of memory. The microEclipse CPU executes 16-bit register-to-register operations in a single 400-nanosecond microcycle and memory-to-register moves in two microcycles. It can accept external microcode from one or more optional external microcontroller chips (XMCs) to accommodate the floating-point and commercial extensions.

A system input/output chip (SIO) generates both the Eclipse and the microNova I/O buses, at the same time providing several internal peripheral functions. The CPU, XMC, and SIO devices are interconnected by a 16-bit parallel system bus as shown in Fig. 1. A dedicated 8-bit bus enables the XMCs to transmit microcode to the CPU.

The family is fabricated with an n-MOS silicon-gate process with 4.5-micrometer channel lengths, 5.5-μm metal width and spacing, and a 700-angstrom gate-oxide thickness. Single-depletion and single-enhancement threshold voltages are used. The CPU chip (Fig. 2) is 270 by 270 mils, the SIO chip is 270 by 270 mils, and the XMC is 210 by 210 mils. Their respective power dissipations are 1.2, 1.2, and 0.5 watt. The chips use a single +5-volt supply with TTL-compatible levels on all signals except for the clocks, which require 4.5 V for a logic high



1. CPU chip set. The microEclipse family is based on a CPU that runs a kernel of the Eclipse C/350 instruction set. This device can accept external microcode from one or more microcontroller chips. A system input/output device generates both Eclipse and microNova input/output buses.

level. The −2.5-V substrate bias voltage is generated on chip, but uses a pin for an external capacitor.

Two-phase logic is used throughout, with both clocks externally generated. Each microcycle is split between an initial phase 1 and a final phase 2. The entire system is synchronized to these two clocks.

The CPU chip realizes three primary design goals: compatibility, expandability, and speed. An enormous amount of software has been written for the Eclipse architecture, so a microprocessor compatible with it is very attractive, given increasing software costs.

The architecture has three optional instruction set extensions, adding character-string manipulation, floating-point arithmetic, and commercial instructions. The Eclipse C/350 model includes all three options and is comparable to a mainframe in the complexity of its instruction set. The CPU chip allows easy and efficient expansion of the on-chip microcode to accommodate these and future options.

It was hoped that the CPU chip could also perform as fast as the existing medium-scale integrated TTL implementations. This high-performance goal was met because of three factors that permit several concurrent operations within a single microcycle. They are a macro-instruction prefetch unit, a four-bus internal data path, and self-modifying temporary registers.

CPU on a chip

The CPU chip's data paths are all 16 bits wide and parallel. They connect a bus transceiver, a register file, and an arithmetic and logic unit with an internal busing system as shown in Fig. 3. This structure allows register-to-register operations in a single microcycle.

Two dynamic buses, the A bus and the B bus, are used to transmit two source operands from the register file during phase 1. A third bus, C, writes data into the register file; this bus can be driven either with the ALU result or with external data during system-bus read operations. This third bus allows the source buses to be precharged during phase 2 without any loss of speed. A fourth bus, called the M bus, is used to transfer addresses directly from the register file or the program counter to the system bus.

The time-multiplexed system bus interfaces with the internal buses through the transceiver. Addresses are driven onto the system bus from the M bus during phase 1 of a bus cycle. Write data is driven from the A bus through an output register for the duration of the cycle. Read data is placed onto the C bus during a bus read operation. A macro-instruction on the system bus can be read into the IR pipeline independently of the status of the C bus.

The register file consists of four program-accessible accumulators defined by the Eclipse architecture, plus four temporary registers accessible by the microcode. The four accumulators provide the source and destination for many Eclipse instructions. The microcode can indirectly address the register file using the source and destination fields of the macro-instructions to specify which accumulators to place on the A bus and B bus and which accumulator is to be written from the C bus. This common technique of substituting fields from the macro-instruction for control fields in the microcode is referred to as macromodification, which will be discussed later.

Each of the four temporary registers in the file can perform a specific transformation independently of the ALU. These four functions are increment, decrement, shift left, and shift right. By coordinating a combination of these "in place" functions with the ALU operation, only one microcycle is required for a multiply or divide iteration step. By incrementing or decrementing the stack pointer in place, context switching requires only one microcycle per register.

The least significant 4 bits of one of the temporary registers drive a bit decoder that can be placed on the A bus under microcode control. This bit decoder serves to improve the performance of the Eclipse bit-manipulation instructions.

The arithmetic and logic unit

The ALU can perform the following operations on 16-bit operands: add, subtract, AND, negate, increment, decrement, and complement. The result of the operation can be shifted left or right 1 bit position or its bytes can be swapped by the shifter matrix.

The output of the shifter is driven onto the C bus. While the C bus is writing into the destination register, the ALU is monitored by test-condition logic that detects a zero result, signed and unsigned carry, arithmetic overflow, and single-digit decimal carry.

The ALU contains logic that selects single-microcycle multiply and divide iteration steps. In using a 1-bit Booth algorithm, signed multiplication is performed as fast as unsigned multiplication.

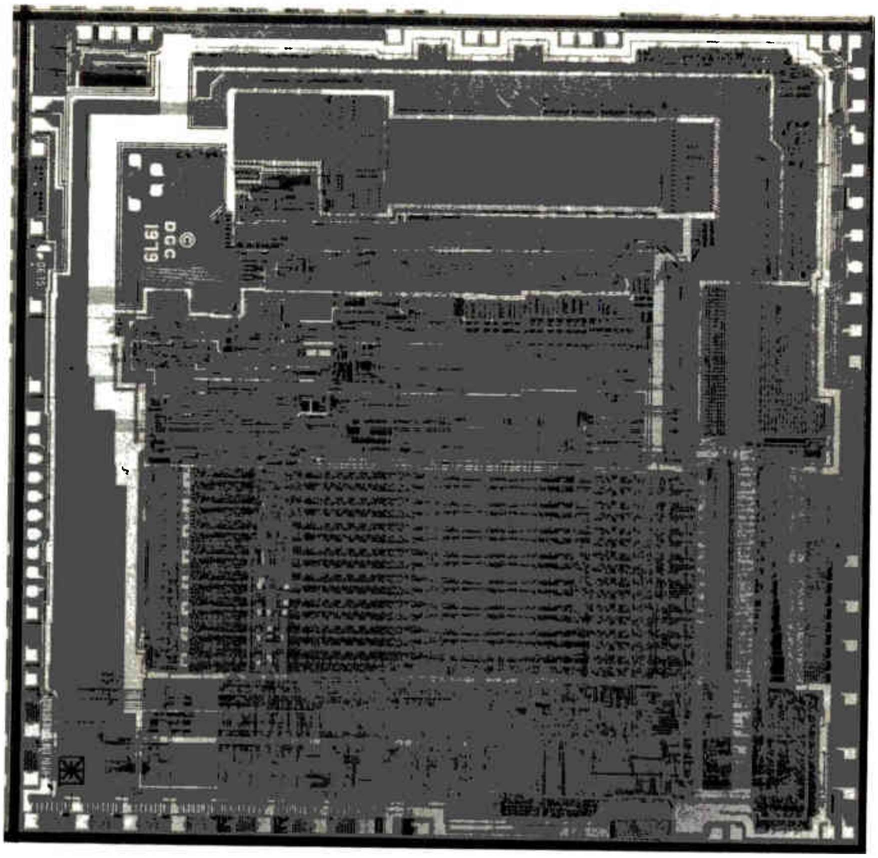
System bus

As mentioned, the microEclipse CPU communicates with other system components over a single time-multiplexed system bus. Every bus cycle comprises two distinct parts, a cycle-specifier segment and a data-transfer segment. The CPU is normally responsible for controlling the system bus, but control may be transferred to any device requiring direct high-speed access to it. When the CPU receives a bus request, all of the system bus interface pins are placed into a high impedance state. The CPU continues to execute instructions during periods when it has relinquished control of the bus, unless access to it is required.

The minimum length of a bus cycle is one microcycle (the duration of a system phase-1, phase-2 pair), but the data-transfer portion of the cycle may be extended indefinitely, allowing the use of memory and peripherals of widely varying cycle times.

A ready pin is used by the microEclipse CPU to determine whether a given bus operation has been completed during the current processor microcycle or if it needs to be extended for another microcycle period. The ready pin is sampled by the microEclipse CPU at the end of every system phase-2 period during bus cycles, and if this pin is found inactive, the data-transfer portion of the bus cycle is extended until the ready pin is asserted at the end of a system phase 2.

Whenever the CPU initiates a memory transaction, the



2. Eclipse chip. This is a photomicrograph of the CPU chip. It is uses n-channel silicon gate technology and 4.5-μm channel widths. The die measures 270 by 270 mils and consumes 1.2 watts. It can support as much as 2 megabytes of memory.

logical memory address is placed on the system bus along with read/write and address translation information during the bus-specification phase of the bus cycle. The data segment of the cycle then transfers data to or from memory, depending on the type of transfer that has been specified.

During I/O instruction execution, the CPU places an encoded version of the instruction on the system bus during the cycle-specification portion of the bus cycle. It then transfers data to or from the selected peripheral device during the data portion of the bus cycle.

Memory cycles are distinguished from I/O operations by the memory cycle pin. When asserted, the specified bus cycle is a memory cycle. When this pin is not asserted during bus specification, the cycle is for I/O. Additionally, bit 0 of the memory address is used with the pin to specify further the target of a bus cycle. The combination of memory cycle and specifier bit 0 are used as listed in Table 1. In the table, program memory is the standard Eclipse 32-K logical address space for program execution. This is the only address space for which memory management is supported. Console memory is used for the virtual console program (about which more will be said later) and data. This address space is entered at startup and whenever a nonmaskable interrupt (NMI) is received.

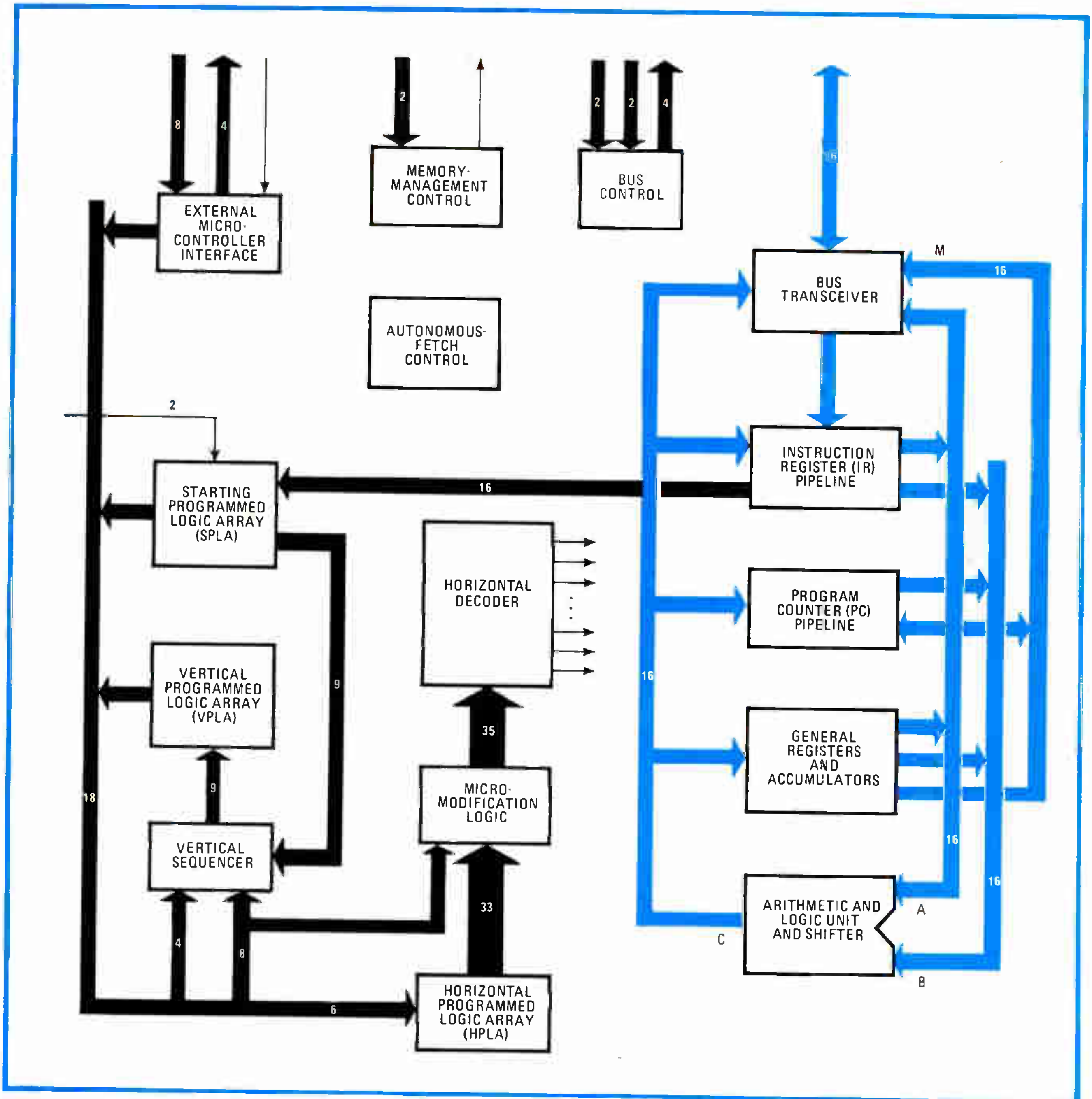
The address space for I/O operations is selected whenever it is necessary for an I/O instruction to be executed. A re-encoded version is placed on the bus during the cycle-specification portion of the segment. The re-encoding facilitates the integration of microEclipse systems and I/O devices (see Fig. 4).

The last entry in Table 1, the local communications address space, is reserved for data communications between system components. Such communications might include microcode-directed transfers of internal microEclipse registers to other system components requiring access to CPU registers.

During bus cycles, cycle-specifier information is presented only during the initial phase of the cycle, even if the bus cycle is extended. The address-enable pin is asserted by the microEclipse CPU to identify this phase 1 as the first in a bus cycle. This requires that cycle-specifier information be latched by target devices on the falling edge of every system phase 1 when address enable is asserted.

The data-enable pin is activated during the data-transfer portion of a bus cycle by the device that is entering data onto the system bus. During write operations, the microEclipse CPU asserts the data-enable pin to indicate that it is actively driving the bus with data. During read operations, the microEclipse CPU samples this pin to determine when the system bus is being driven with valid data.

The address- and data-enable signals also coordinate operation of the microEclipse and other system components. An interlock prevents address enable (and the internal address drivers) from being driven whenever the data-enable pin is asserted. A similar mechanism prevents data from being driven onto the bus whenever address enable is asserted. Without these, the microEclipse (or another system component) might attempt to drive the system bus while it is still being driven from a previous bus cycle. An overlap of this type may arise



3. CPU architecture. Primary data paths in the CPU are 16 bits wide. Two dynamic buses, A and B, carry source operands from the register file, while the C bus writes data into the register file from the ALU or the system bus. The M bus transfers addresses to the system bus.

from the slow disable time of bus drivers or from system timing skews. The interlocks allow rapid pin-driver and receiver turnaround, thereby eliminating the need for a period of bus inactivity to insure safe pin-driver and receiver switching.

A set of 16 pins (MB_0–MB_{15}) on the CPU communicates addresses and data between the microEclipse and other system components. The pins supply cycle-specification information whenever address enable is asserted and pass data in or out of the microEclipse whenever data enable is asserted.

Read cycles are distinguished from write cycles by the state of the write high (WH) and the write low (WL) pins. These pins are asserted during the cycle specification portion of all CPU-initated bus operations as indicated in detail in Table 2.

Multiprocessor operation is facilitated by the inclusion of a bus lock (BLOCK) pin. When asserted, this pin indicates that the microEclipse is reserving exclusive use of the system bus and will not relinquish control even if requested to. This pin is asserted during the instructions to increment and skip on 0, decrement and skip on 0, and skip on 0 bit and set to 1 (ISZ, DSZ, and SZBO). These three instructions may be used as interprocessor semaphore instructions because of their indivisible read/modify/write bus accesses.

The CPU chip contains a prefetch unit that operates independently of the microcode. This logic endeavors to fetch words from the instruction stream beyond the currently executing macro-instruction. If the microcode needs the next word in the instruction stream and the prefetch unit has not yet succeeded in obtaining the desired word, it will suspend the execution of micro-instructions until the word can be fetched. The instructions are stored in a structure called the instruction register, or IR, pipeline (Fig. 5).

Instruction register pipeline

The IR pipeline contains three registers, which were found sufficient to support most expected instruction sequences without degrading performance by requiring separate fetch cycles. The data paths necessary for all IR pipeline transfers are independent of the register file and ALU, so a complete micro-instruction can be executed in parallel during any IR pipeline operation. Jump instructions alter the program counter and invalidate all entries in the pipeline.

The first register in the IR pipeline is called IRF because instructions are fetched into it. Whenever the pipeline is not full and the system bus is not being used by microcode or by external devices, a fetch state is entered and a word fetched into the IRF.

Instructions are decoded from the second register, or IRD. IRD is loaded from IRF whenever IRD is not valid and IRF is. When the microcode routine interpreting the current macro-instruction is complete, it will issue a decode-microsequence order, transferring control to the next macro-instruction. The first word of a macro-instruction contains the op code and will be in the IRD.

The IRD is invalidated after a decoding cycle; therefore, in multiword instructions, the IRD will contain the second instruction word, and this can be either an immediate operand or an address displacement. The microcode will request IRD to be placed on the A bus, where it is then invalidated. Therefore a subsequent decoding will use the instruction stream word following the immediate operand or the address displacement. The result is a very simple mechanism for handling multiple-word macro-instructions.

The third register, the IRE, always contains the first word of the currently executing macro-instruction. IRE is loaded from IRD whenever a decode occurs. Its primary use is to provide fields for macromodification, which occurs most frequently when the source and/or destination register of a microcode operation is specified with fields from the microinstruction.

In certain memory reference instructions IRE contains a short 8-bit address displacement. These 8 bits can be sign-extended and placed on the A bus under microcode control. The address placed on the system bus during an I/O instruction is a simple permutation of some of the fields in the actual macro-instruction word and can be placed on the B bus under microcode control. There is also a data path to load IRE from the C bus under microcode control.

A separate program-counter (PC) pipeline is maintained in parallel to establish a correlation between prefetched instructions and their addresses. The pipeline contains a self-incrementing program-counter and three other registers—PCF, PCD, and PCE, which contain the memory addresses of the instruction stream word in IRF, IRD, and IRE, respectively. A block diagram of the PC pipeline is shown in Fig. 6.

TABLE 1: BUS-CYCLE DESTINATIONS

Memory-cycle (MEMCYC) pin	Address bit 0	Cycle type
1	0	program memory
1	1	console memory
0	0	input/output operations
0	1	local communications

During a fetch, the program counter is placed on the address bus. It is incremented independently of the ALU after every fetch, and the unincremented value is saved in PCF. The transfers from PCF to PCD and from PCD to PCE occur at the same time as the corresponding IR pipeline transfers. Both PCD and PCE can be placed on the B bus under microcode control and are useful in computing program-counter-relative addresses and in saving return addresses.

PCF and PCD are compared with every write address to detect attempts to store a new value at a prefetched address. These impure code sequences must be found in order to maintain compatibility with the Eclipse architecture. To ensure that the updated instruction word is processed instead of the prefetched word, the CPU will execute an "impure trap," which flushes or invalidates the IR pipeline.

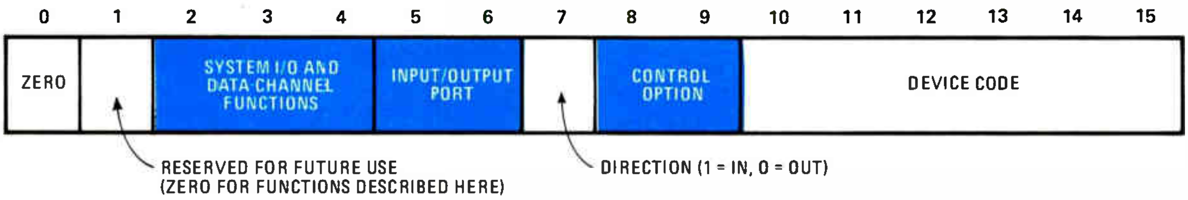
The micro-architecture

One goal of the micro-architecture design was to fit enough microcode on the CPU chip to implement a kernel of the C/350 instruction set. Another was to allow for expansion through externally generated microcode to implement the complete C/350 instruction set. A two-level micro-architecture offers the bit efficiency needed for the on-chip instruction set, as well as significantly reducing the width of the control word that must be transferred between chips for the complete set.

The classical method of two-level microprogramming is vastly improved through the use of a technique called micromodification. The first or vertical level of micro-instructions is 18 bits wide. Six bits are used to select one of 64 35-bit, second-level horizontal micro-instructions. Two 4-bit fields supplied by the vertical can be substituted for two fields in the selected horizontal microcode. The remaining 4 bits control the sequencing of vertical micro-instructions.

Thus micromodification—the technique of substituting vertical fields for horizontal fields—multiplies the power of each horizontal micro-instruction. The result is an orthogonal, horizontal micro-instruction set having a general yet bit-efficient set of control primitives.

The microEclipse CPU provides support for Eclipse C/350-compatible memory management and protection;



SYSTEM I/O AND DATA-CHANNEL FUNCTIONS

Bit 2	Bit 3	Bit 4	Function
0	0	0	no operation (NOP)
0	0	1	interrupt acknowledge (INTA)
0	1	0	mask out (MASKO)
0	1	1	I/O RESET (IORST)
1	0	0	data-channel address (DCHA)*
1	0	1	data-channel input (DCHI)*
1	1	0	data-channel output (DCHO)*
1	1	1	reserved

*produced by the system I/O (SIO) chip

I/O PORT

Bit 5	Bit 6	Port
0	0	status
0	1	A
1	0	B
1	1	C

CONTROL OPTION

Bit 8	Bit 9	Function
0	0	none
0	1	start
1	0	clear
1	1	pulse

4. I/O encode. The I/O address space of Table 1 is selected whenever an I/O instruction is executed. A re-encoded version of the I/O instructions, shown above, is placed on the bus during cycle specification. This facilitates interfacing the microEclipse with the I/O devices.

indirect protection, I/O protection, and the load effective address (LEF) instruction are all available without any external logic being needed.

When enabled by a supervisor program, the indirect protection feature restricts to 15 the number of levels of consecutive indirection. Should a program violate this restriction, the microEclipse initiates a map fault trap sequence for intervention by the supervisor program. Without such protection any program might inadvertently initiate an infinite indirect chain that would adversely affect system integrity.

I/O protection

The I/O protection feature of the internal map hardware lets supervisory software restrict I/O device accesses to privileged programs. If a violation of this protection occurs, it causes a map fault trap and returns control to the supervisor.

When a program is running in an I/O-protected environment, an additional instruction is available if the LEF enable bit is set in the map status word. The LEF instruction allows direct loading of a register, with the result of an effective address calculation.

With the addition of external translation RAMs and some control logic, a physical address space of up to 2 megabytes is supported by the memory management and protection logic. Additionally, these external components provide a mechanism for either individual write or validity-protection of pages in the logical address space.

A set of seven bonding pads has been added to the microEclipse CPU to enhance testability. These pads, which are not normally brought out to package pins, are used for logic debugging and to minimize the time required for wafer testing.

Testability features

Assertion of a pad by test equipment inhibits the execution of on-chip microcode, thus allowing entry of test microcode sequences through the XMC interface and rapid verification of the internal data paths and register-file control logic.

Five other pads enable test apparatus to observe the sequencing of the microprogram counter during the execution of micro- and macro-instruction test sequences. The 9-bit microprogram counter is multiplexed onto these pads, with 5 bits available during processor phase 1 and the other 4 bits during phase 2.

A single pad was added to bit 0 of the left-shifting register to enable microprogram test sequences to enter internal data without requiring full integrity of the memory interface logic.

Although not essential to the operation of the microEclipse CPU, the SIO chip's rationale is that it allows flexible and efficient system configurations. It enables the microEclipse CPU to communicate through both the Eclipse I/O bus and the microNova I/O bus and it contains several specialized I/O components.

The SIO chip generates timing signals conforming to Eclipse I/O bus specifications for programmed I/O and data-channel transfers. The microNova I/O bus produced by the SIO is functionally identical to that of the microNova CPU chips (the mN601 and mN602).

SIO functions

The SIO monitors the system bus for I/O instructions from the CPU. When one is recognized, the current cycle is extended and the operation is performed. Devices selected by programmed I/O instructions are either internal to the SIO or they exist on the Eclipse or microNova I/O buses. Proper routing is determined on the basis of the instruction's device code.

At power-up, the microNova I/O bus is polled for device codes residing on that bus. The SIO chip then generates and maintains a microNova device code map. During programmed I/O instructions, the SIO uses this map to determine which of the two I/O bus the selected device is interfaced to.

Data-channel transfers are initiated through the use of separate data-channel request pins for the Eclipse and microNova I/O buses. After a data-channel request is made, the SIO asserts the bus-request signal to become the new bus master on the next available cycle. While acting as master, the SIO controls all aspects of the transfers between memory and the peripheral device, with Eclipse data-channel transfers having priority over microNova transfers.

To synchronize all internal and external device service requests, the SIO generates a request-enable signal. All peripheral devices use this signal to enable interrupt requests and data-channel transfer requests.

Internal devices

The SIO contains several common peripheral devices useful in designing a microprocessor-based system. These include: power monitor, programmable interval timer (PIT), real-time clock (RTC), and an asynchronous serial port (TTI/TTO). The PIT, RTC, and TTI/TTO are all fully compatible Data General peripheral devices, including busy/done networks, mask bits, interrupt logic, device codes, and instructions.

The power monitor responds to the power-fail signal sourced by the power supply. An interrupt is generated whenever a change occurs in the power-fail line except at initial power-up, when a nonmaskable interrupt (NMI) is generated. The NMI signal is used to inform the CPU that the SIO is initialized.

The PIT is a 16-bit counter with a clock rate selectable through external system jumpers. It is preset with the desired count and an interrupt is generated on overflow. The PIT continues to count on overflow, and since the counter is double-buffered, it may be read at any time. This simplifies interrupt latency measurement.

The RTC section generates an interrupt at one of the four program-selectable frequencies: ac-line frequency, 1 kilohertz, 100 hertz, or 10 Hz.

The TTI/TTO section provides a standard asynchronous serial I/O protocol. Both the input and output sections are double-buffered and controlled by their own finite

TABLE 2: READ- AND WRITE-CYCLE SPECIFICATION

Write high	Write low	Operation
1	1	word read
0	0	word write
1	0	byte write (bits 8 – 15)
0	1	byte write (bits 0 – 7)

Note: the WH and WL pins are driven using negative logic conventions

state machines. Sixteen baud rates are selectable via system jumpers. Additionally, the input section contains logic to detect the depression of the break key, which causes an NMI to be generated.

Interrupt request priority is maintained by the SIO. There are three separate sources of interrupt requests: internal, Eclipse, and microNova I/O devices. Internal devices have the highest priority. Each external bus maintains its own priority chain with the Eclipse I/O bus having priority over the microNova I/O bus.

Virtual console support

Most microEclipse systems will be operated with a virtual console: a small program to duplicate all of the functions of front panel switches. The SIO provides virtual console support in three ways:

- TTI logic detects the depression of the break key.
- 30 words of static RAM for use by the virtual console program as scratch pad memory are resident on the SIO.
- Special logic detects the halt instruction and initiates the jump to the virtual console program.

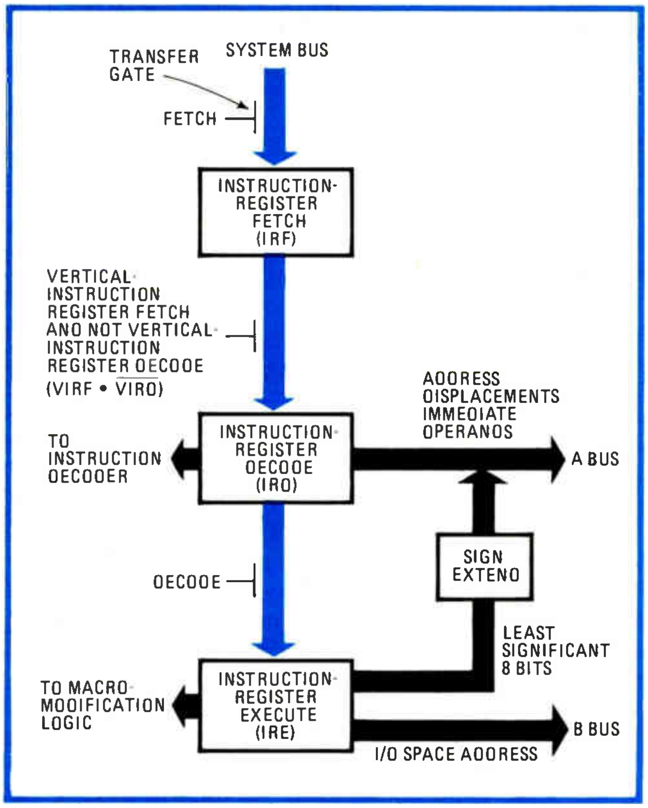
For maximum system flexibility, a fixed system clock frequency is not assumed. Instead, the microEclipse system has been designed to operate with eight predetermined cycle periods ranging from 300 to 600 ns. The SIO's internal devices (the PIT, RTC, TTI, and TTO) need a fixed frequency, however.

The frequency-synthesis section generates two pseudoconstant clocks for the internal devices. These frequencies (1 megahertz for the PIT and RTC and 614 kHz for the master baud rate) are produced using a binary rate multiplier technique. The circuit performs variable-rate frequency division of the system clock to produce the required frequencies.

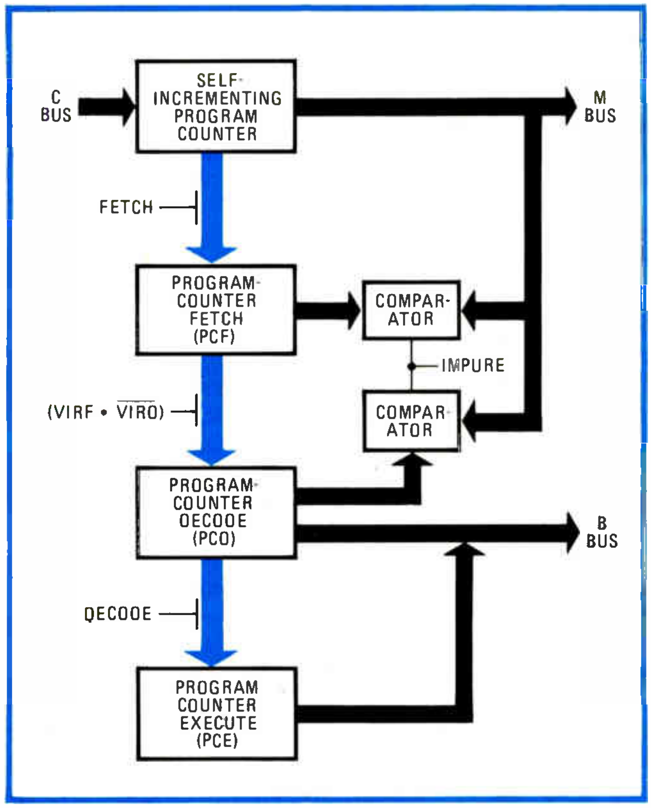
The 1-MHz frequency is pseudoconstant, producing a noncumulative short-term error that is never greater than one system clock period. The master baud rate does show a small cumulative error because of the irrational fractional count required to produce the 614-kHz frequency. However, the error is less than 0.16% and is cumulative during only one character time, since each new character must be resynchronized to the baud rate.

System flexibility is further provided by external selection of various SIO functions and speeds. The SIO maintains 14 system configuration bits that are set by external jumpers and loaded on the rising edge of reset. The following eight conditions are externally selectable:

- System clock rate—informs the frequency synthesis section of the operating clock rate.



5. Instruction pipe. The microEclipse pipelines enable the microprocessor as fast as TTL versions of the Eclipse. The instructions first go to the IRF when the pipeline is not full. They are decoded in the IRD and subsequently loaded into IRE for execution.



6. PC pipe. A separate program counter pipeline is maintained along with the IR pipeline to track prefetched instructions and their addresses. It contains a self-incrementing program counter and three other registers that correspond to those in the IR pipeline.

- Baud rate—selects the desired baud rate.
- PIT rate—selects the desired PIT counter rate.
- Eclipse I/O bus enable—informs the SIO that the Eclipse functions will be enabled.
- MicroNova I/O bus enable—enables the microNova section.
- Virtual console RAM enable—may be disabled to allow for external expansion.
- Break-key enable—may be disabled when the virtual console is not being used.
- Halt dispatch—allows the halt instruction to cause either a jump to the virtual console program or a hard halt. The latter suspends CPU operation until an NMI.

External microcontroller

The microcontroller chip (XMC) contains 1,024 vertical micro-instructions, a decode programmable logic array capable of recognizing 64 macro-instruction op codes, and an internal vertical sequencing mechanism. The microcode and decode PLAs are mask-programmable and several XMCs are needed to implement all the optional instruction sets.

The XMC can send 16 bits of microcode to the CPU chip using an 8-bit time-multiplexed bus. The XMC and the CPU chips use five control signals for a microcode transfer protocol.

Each XMC monitors the system bus to maintain a duplicate of the CPU's macro-instruction pipeline. This allows the CPU and multiple XMCs to decode macro-instructions simultaneously. Therefore, only one unused microcycle follows a decode where the microcode is applied by an XMC.

When the decode PLA recognizes a resident macro-instruction, it provides the first vertical micro-instruction necessary to execute it. The XMC then transfers control to the vertical sequence, which provides the remaining micro-instructions.

Vertical sequencing

The XMC contains a sophisticated internal sequencing mechanism. Two of its features enable sharing of microcode space; four-deep microsubroutine capability is implemented, and three internal mode flags are maintained. Testing these flags and modifying them is transparent to the CPU.

On each microcycle the CPU transmits the result of a test performed by the previous micro-instructions. When no microcode branch that is conditional on this external test is encountered, the XMC transmits the next micro-instruction to the CPU as it executes the current one. When an external conditional branch is encountered, a two-microcycle time penalty may be incurred because the choice of which micro-instruction to transmit must wait for receipt of the external test result.

This penalty can be avoided if useful micro-instructions can be inserted between the micro-instruction performing the test and the conditional branch that reacts to the test. In this case, the inserted useful micro-instructions are executed while the test result is transmitted to the XMC. □

Microcomputer brings flexibility and power to communications control

Up to 255 remote serial control units, employing 19 preprogrammed commands, can be tied to a single host processor

by Robert A. Burckle, *Mostek Corp., Carrollton, Texas*

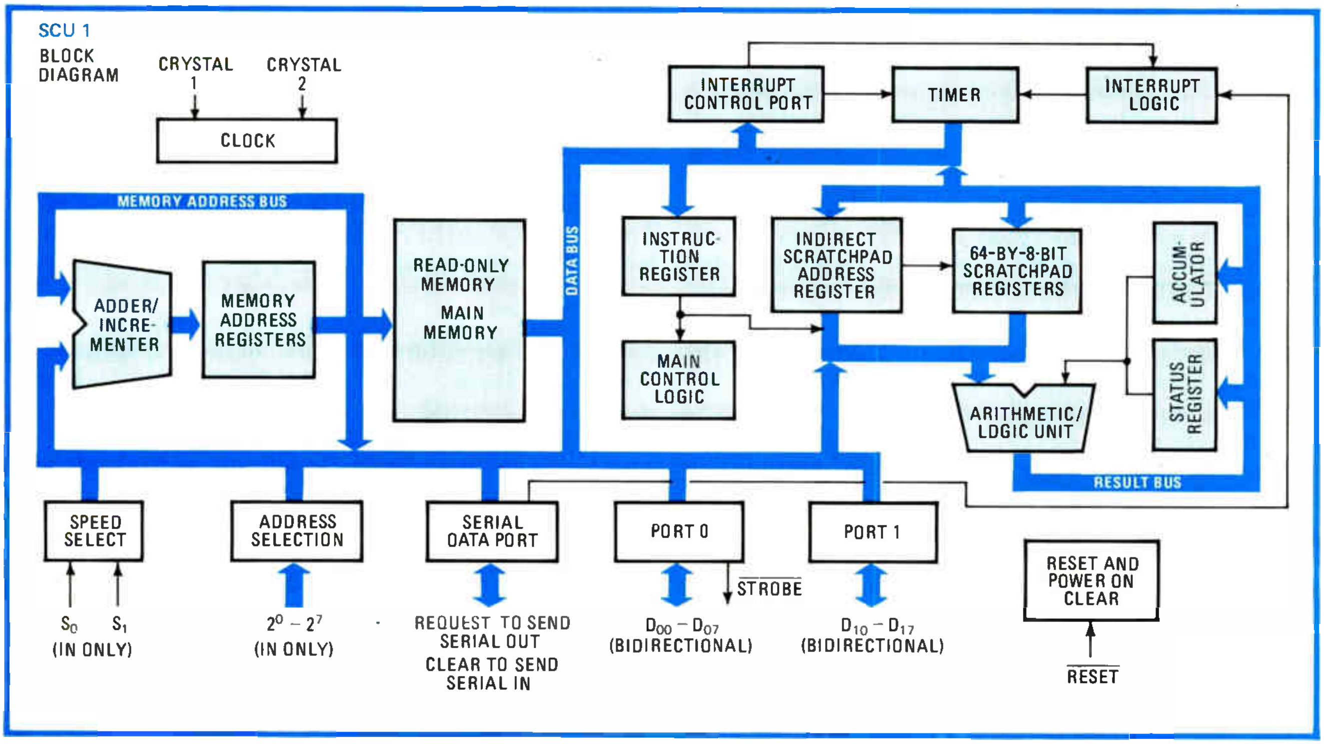
☐ Remote data acquisition and control is becoming the byword for many microcomputer-based systems, where the objective is to carry out operations at various locations under control of a central processor. Such applications are cropping up virtually everywhere, from factories, for, say, checking inventories, to gas stations, for monitoring gas pumps.

The trouble is that setting up the serially linked communications system, including the protocols, turns out to be no mean feat—and almost prohibitively expensive—since it often requires lots of random logic chips. Large-scale integration has changed the picture, adding some flexibility to the communication formats through programmability. But still it is difficult to attain from the available communications controllers the power, simplicity, and flexibility of a serial control unit, the SCU-1, developed by Mostek.

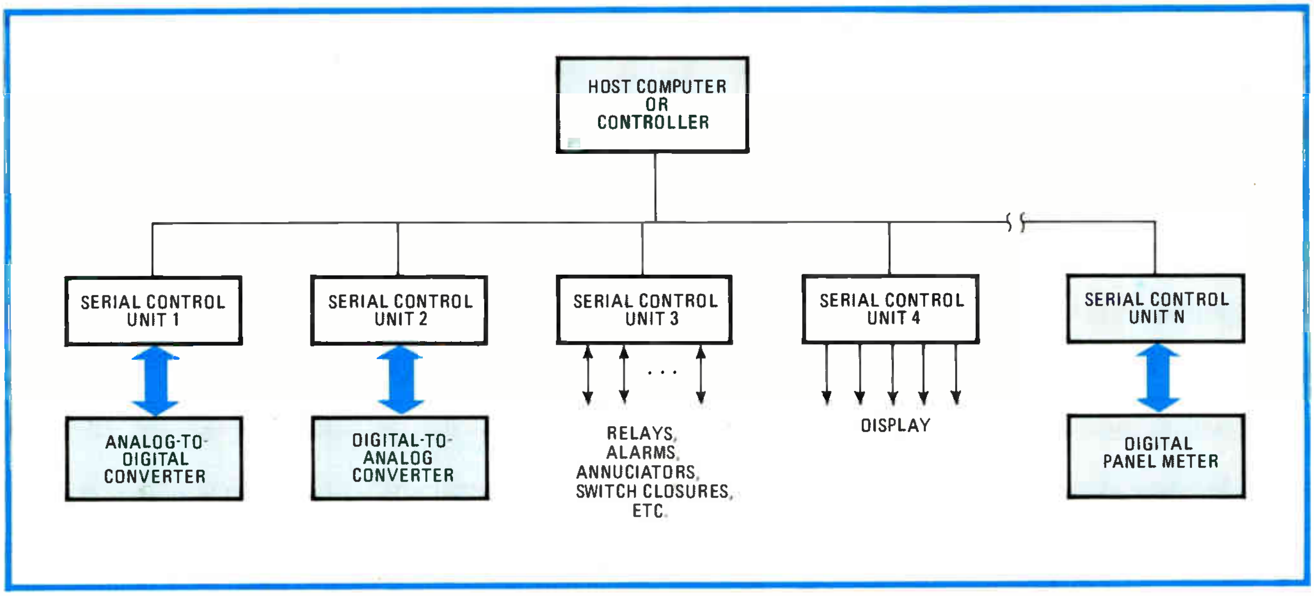
The SCU-1 takes much of the worry out of serial communication between processors. Up to 255 of them can be used as front-end controllers operating under direction from one central processing unit, and simple commands can initiate up to 19 different preprogrammed procedures each. Moreover, the network communication protocol for the SCU-1 derives from the attributes of multidrop communications systems developed in the minicomputer world; simple and reliable, it specifies asynchronous operation in a half-duplex mode at a rate of up to 1,200 bits per second.

The power of the SCU lies in the fact that it is a single-chip microcomputer (Fig. 1). Housed in a 40-pin dual in-line package, it is able to change its mode of operation by interpreting commands received in a newly defined network communication protocol.

The preprogrammed tasks include single-bit input and output, byte input and output, monitor or control input for selected patterns, and handshaking with analog-to-



1. Processor-peripheral. Mostek's SCU-1 serial control unit is housed in a 40-pin DIP and implemented using ion-implanted n-channel silicon-gate technology, which yields a typical power requirement of 275 mW. All eight port 0 and all eight port 1 I/O lines are bidirectional.



2. Party line. Up to 255 serial control units can be placed in a one-data-link system under control of a host processor. A positive-true transistor-transistor-logic-convention is observed for selectable address strapping using eight dedicated chip pins.

digital converters and digital panel meters. This functional flexibility means that the part can actually be used for both monitoring and control.

Even more useful to the cost-minded system designer is the fact that multiple units can be hooked up on a single half-duplex communication channel (Fig. 2). Connected thus, all the units share the same "party line" communications link and are controlled by a central computer or controller. Orderly system operation is maintained by a user-defined polling sequence, as the SCUs cannot initiate a transmission—they can only respond after being polled.

Within the SCU is a communications controller, a task monitor, a command library, and an I/O interface (Fig. 3). With the communications controller, a complete communications line can be set up for sending and receiving messages, checking errors, and synchronizing the unit. It also interfaces with the task monitor to allow specified tasks to be executed and reported on.

The task monitor interprets received commands and controls their execution. It also compiles results from I/O operations and passes them back through the communications controller.

The preprogrammed functions are stored within the command library. These functions are grouped into two categories: supervisory and timing (supervisory/timer) and memory and I/O (memory/input-output) commands. They give the user a great deal of flexibility in revising the software dynamically.

Applications

The SCU has 16 I/O lines that can be addressed individually or together, depending on configuration. They are used to interface products such as analog-to-digital and digital-to-analog converters, 3½-digit panel meters, relays, and switches.

The chip generates and receives asynchronous serial data composed of 1 start bit, 8 data bits, 1 even parity bit, and 1 stop bit. Therefore, communications can be initiated by ASCII-compatible devices, from cathode-ray-tube terminals to mainframe computers.

The SCU is designed to work in locations far from the central controller, with the distance a function of the communications link, not the SCU. A minimum link configuration requires a half-duplex serial channel with a signaling capacity of 300 bits per second, but the 5-volt chip has pins for selecting 300 or 1,200 b/s.

The SCU transmits and receives a TTL-compatible serial asynchronous bit stream. No modulation or demodulation capability is provided. Handshaking and control signals allow the SCU to be interfaced with single-ended and differential line drivers and receivers, TTL-compatible radio-frequency modems, or fiber-optic transceivers. Since the data transmission is asynchronous, there are no critical timing or signaling parameters.

As mentioned earlier, up to 255 serial control units may be on one data link. Control is provided by a selectable address on the SCU using the appropriate pins. The 256th address, FF_{16}, is not allowed, since it is used internally by the SCU itself.

New protocol

Mostek has defined a new data-communications protocol for the SCU. This protocol provides easy access to the units, as well as good data throughput and data integrity. As with all protocols, it was designed to be easy to use and implement, flexible, and expandable and to have a low data-bit overhead. In addition, it had to be error-resistant and computer- or controller-independent, operate in a factory environment, and provide as much intelligence as possible at the remote site.

These considerations led to the choice of a character-oriented protocol, which means that even though messages are sent in a bit-serial format, they are reconstructed and processed in 8-bit characters. In this protocol, five characters constitute a message. The characters are address, command, data address, data, and LRC (the error-check character, literally, "longitudinal redundancy check"). Before they can be understood, the message structure itself must be analyzed in some detail.

Messages to and from the serial control unit are sent in an asynchronous bit-serial format identical to ASCII transmission. For each character, first a start bit, followed by 8 data bits (least significant bit first) is sent, then an even parity bit and a stop bit. A total of five characters is transmitted for each message, yielding a total of 55 bits per message. A communication sequence consists of a message sent to an SCU and a corresponding acknowledgment.

Within the bit stream are two parity checksums. The first checks for the integrity of the previous 8-bit data word. The second, the LRC, checks the integrity of the four data words that make up the actual message. By using these two checks, any odd number of bit errors, as well as 2 bit errors, can be detected.

The individual characters specified by the protocol can be grouped to provide a normal or a special short message sequence. The latter is made up of only the address and command elements and is used during a fast polling operation. It trades some error-detection capability for an increased total-message throughput.

Address and command

Eight bits are needed to represent the address of any serial control unit in a data link. These range in base 10 notation from 0 to 254. All inputs use positive-true logic and are coded in binary format. Therefore, if an SCU is to be defined as unit 100, for example, address-select pins 2^2, 2^5, and 2^6 should be signaled.

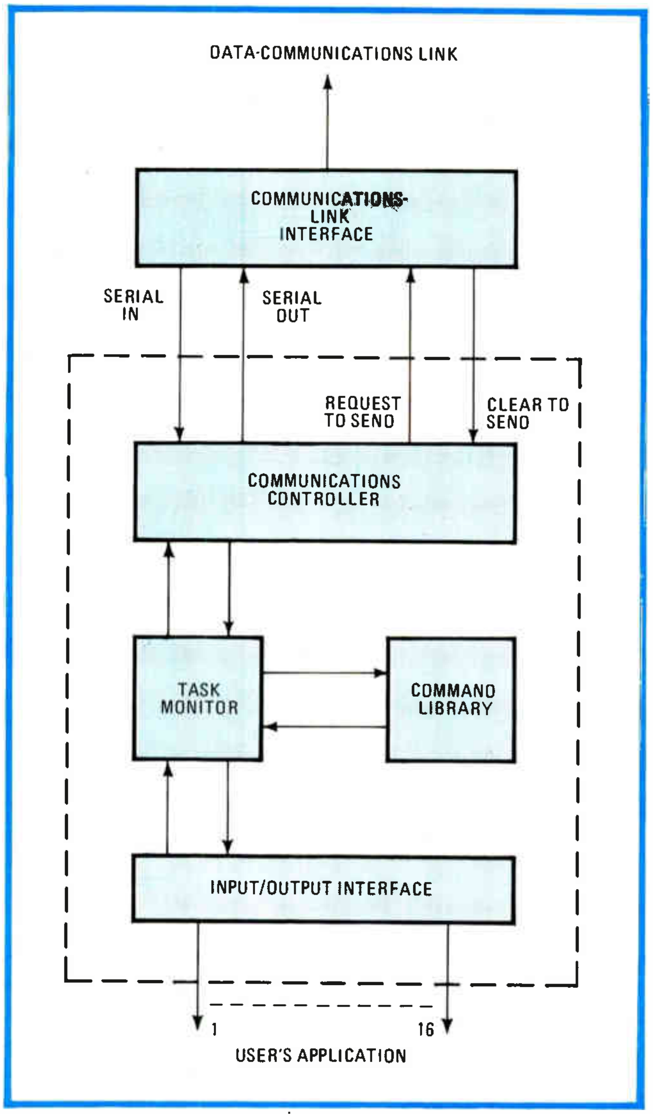
A bit-oriented command structure has been specified to ensure that the system is flexible and expandable. In this approach, 128 commands are reserved for use by the SCU and 128 commands left undefined for the user.

Even though the undefined commands cannot be executed by the SCU, the user can integrate other I/O controllers, in addition to the SCUs, into a single network. Bit C7—the most significant bit in the command word—controls such units. If it is set, one of Mostek's reserved commands will be accessed; if it is cleared, the SCU will ignore the command and send a loop command.

The command structure is subdivided further. Bit C6 differentiates between the two different kinds of tasks. If it is set, the supervisory and timer commands are accessed; if it is cleared, the memory and input/output commands are accessed.

The six bits C5 through C0 are used within the Mostek command word to select one of 64 possible tasks in the groups specified by bit C6. The command assignment within the SCU is: $00_{16}-7F_{16}$ (128 user-defined commands); $80_{16}-BF_{16}$ (64 memory and I/O commands) and $C0_{16}-FF_{16}$ (64 supervisory and timer commands). Any command that is not defined within the SCU but is nevertheless received by it will cause a loop supervisory command to be issued in response.

The 8-bit word of the data address serves two purposes. It is used to specify either the address of a port or memory or up to 8 bits of data. The actual determination is defined within the command word. The 8-bit word of the data character forms a byte and can be information from either a memory or an I/O port.



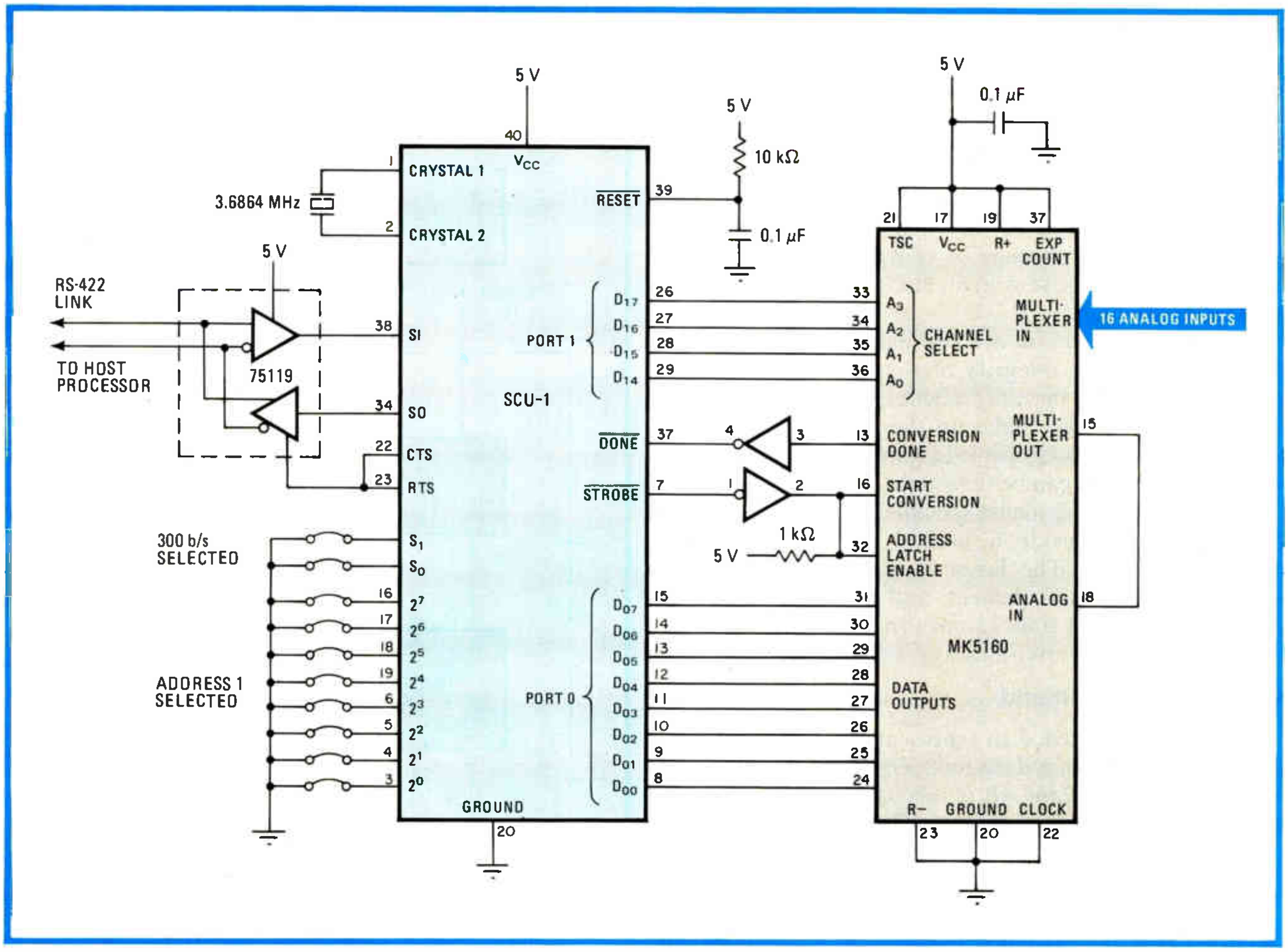
3. Flexible. The SCU-1's architecture is designed for flexibility—up to 19 commonly used supervisory or memory-oriented functions may be accessed by a single command from a remote host processor. They permit system software to be reconfigured dynamically.

The final element in the protocol is the longitudinal redundancy check, or horizontal error-detection character. It is created by generating a parity check on each of the four previous elements of the protocol. Combined with the vertical parity check provided in each element, the LRC provides a high margin of error detection and a virtually error-free message interchange between the SCU and the host processor.

Synchronizing messages

The SCU uses a special procedure to synchronize network messages. Bit and word synchronization, on the other hand, are no problem, since they are provided by the asynchronous format. Network-message synchronization is needed when an SCU is initialized or whenever an individual SCU or the network is restarted.

There are three responses an SCU can generate to a host message. They are: address, command, data



4. Conversions. The SCU-1 is ideal for controlling analog-to-digital or digital-to-analog converters. In this case, an 8-bit a-d chip with 16 analog inputs sends its data to a host processor over an RS-422 transmission line, which provides good noise immunity and drive capability.

address, data, LRC; address, loop, data address, data, LRC; and no response.

The first response is the normal reply to a host message. The address and command characters are identical to those generated by the host, and the data-address and data characters are modified to reflect the response requested in the command field. The LRC is generated to ensure that correct parity is maintained for the four previous characters.

The second response is generated if the host processor issues a loop command or a memory address.

The third, literally no response, occurs if a message is sent to the SCU and an error is detected. The unit simply remains in synchronization and the message must be retransmitted.

Short-poll responses

As mentioned earlier, the short-poll format is especially useful in speeding up message throughput, as, for example, when the SCUs are performing monitoring functions only. Three SCU responses are possible in this mode: address, poll; address, command, data address, data, LRC; or no response.

If a short poll is issued and there has been no change since the previous poll, the address and poll command is sent back to the host. If an activity has occurred since the previous poll, the SCU will issue the second response to the host. This reply indicates the SCU's designated task and the new condition that caused the reply to be generated. The unit will continue to generate this response until it is reset by a host command.

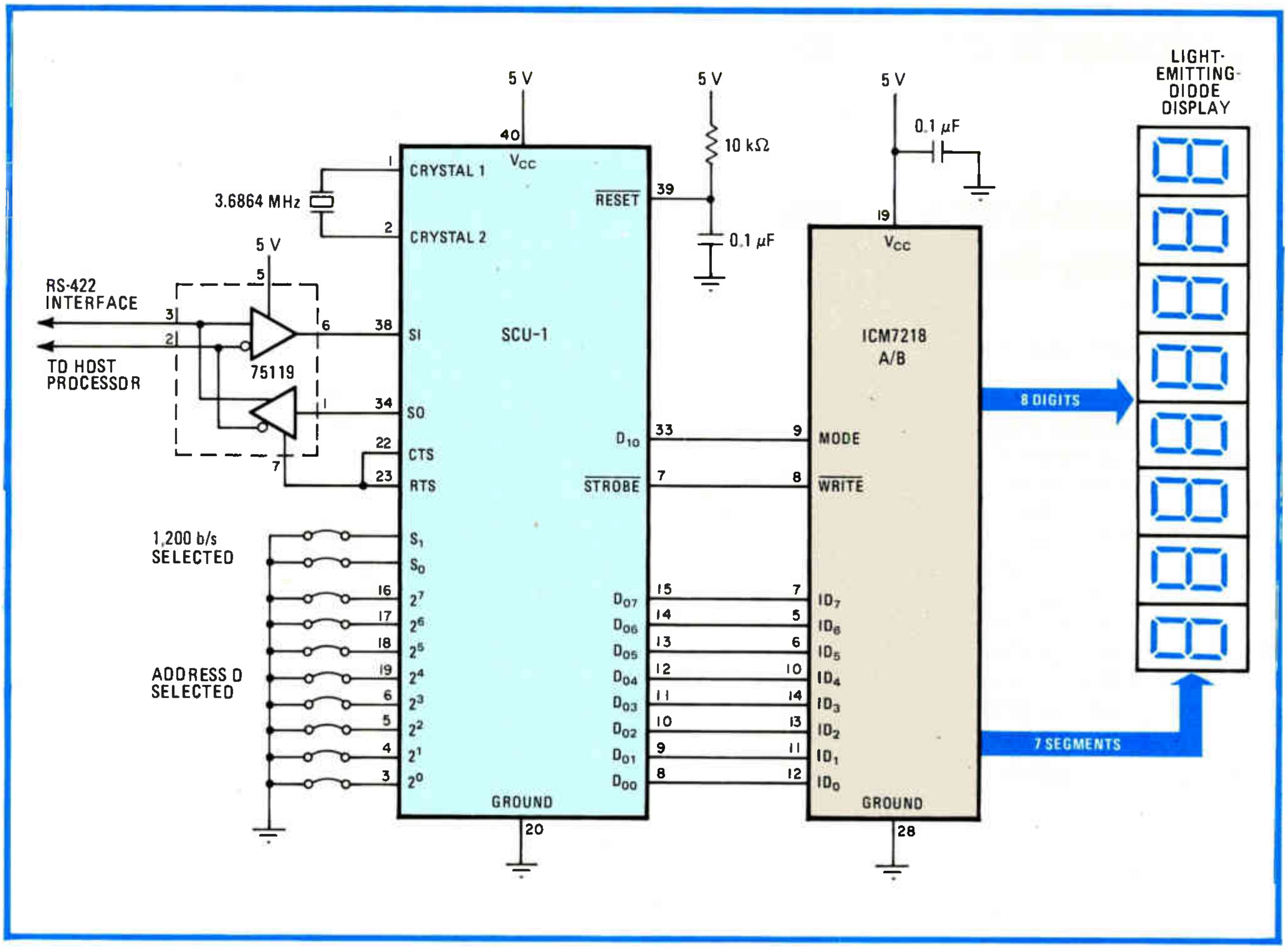
If a parity error has been detected by an SCU, no response will be generated in answer to the short poll. At the same time, all regular command formats are fully functional and will be acknowledged when the short-poll mode is activated.

Implementation

The logic flow within the SCU to implement the protocol is an interrupt-driven routine. In the receiving mode, the message is always checked for synchronization, errors, unit address, and message completeness. If all is well, a new task is then placed in the executive routine for further processing.

In the transmitting mode, a message is assembled in the output buffers and then sent in a bit-serial format to the host processor. Here, the executive routine acts on command placed in its buffer by the protocol handler. It also manages the task library and reports the results of requested operations into an output buffer for transmission by the protocol routine.

The executive routine continually scans for a new task.



5. Display. Mostek's SCU-1 peripheral microcomputer can both provide data to and control the operation of a light-emitting-diode display driver. Here, it is connected to the host processor by an RS-422 link. Only 5 volts is needed for the complete system.

When an error-free message is received and a new task requested, the executive searches for the task in the task library. The task is then executed and if required an appropriate response is made.

When this task is completed, the routine tests to see whether a previous task was suspended. If so, it restores that task. When all tasks are completed, the executive returns and once again scans for additional tasks.

One special feature implemented in the software is request-to-send (RTS) and clear-to-send (CTS) commands. These signals permit the SCU to be used over a variety of communication media by synchronizing the data with the channel direction. The two can be tied together or be used in conjunction with an external control; data synchronization can thus be maintained on channels with radio links and modems that have slow turnaround times.

Synchronizing the data

With this feature, when a message is ready to be sent, the RTS signal is activated. Data will then be transmitted only when the CTS signal becomes active.

Note that only the SCU issues an RTS. After a interval selected by the user, a CTS command is received and data appears on the serial-out pin. If a CTS is not received within two seconds, the RTS becomes inactive and the output-message request is cancelled.

The SCU can be made to work with virtually any analog-to-digital converter. For example, it can control a 16-channel multiplexer while accepting the value from a 12-bit a-d unit.

Remote data acquisition

In one application (Fig. 4), a Mostek 50816N 8-bit, 16-channel single-ended a-d converter is interfaced with a serial control unit. Port 0 (D_{00}–D_{07}) of the SCU is used to pass data, and D_{14}–D_{17} of port 1 select the input multiplexer channel.

A conversion is begun when a request is commanded by the strobe line. Upon completion, the conversion-done flag is sent to the SCU and the digitized voltage is sent via the unit to the host processor.

In this application, an RS-422 communications link is used. This channel provides high noise immunity and good drive capability and allows the whole system to use a single 5-V supply.

The SCU can also be used to interface with display circuits such as the Intersil 7218 series eight-digit light-emitting-diode driver (Fig. 5). This chip, which includes digit and segment drivers, all mutliplex scan circuitry, and an on-board 8-by-8-bit static memory, is interfaced with the SCU. □

Sample-and-hold modules shrink delay-line cost

by T. G. Barnett
London Hospital Medical College, Department of Physiology, England

Providing a selectable time lag while faithfully reconstituting an analog signal, this circuit, which uses a 555 timer and three one-shots to clock two sample-and-hold modules, serves as a low-cost substitute for the conventional analog delay line in some applications. Although its spectral response is not nearly so great as that found in commercial charge-coupled-device–type delay lines, the circuit is suitable for use in the analysis of low-frequency physiological data.

Components R_a, R_b, and C_t of the 555 (wired in the astable mode) set the desired sampling frequency $f = 1.44/(R_a+2R_b)C_t$. In line with the sampling theorem, this frequency should be equal to or greater than twice the highest analog frequency to be processed.

The output of the 555 drives one-shot A_1, which provides a sampling pulse for the first LF398 sample-and-hold module. Similarly, the 555 drives A_2, which (through A_3) drives the second sample-and-hold device.

Timing components R_{t1} and C_{t1} should be set to provide an output pulse of a minimum of 10 microseconds from A_1. Components R_{t2} and C_{t2} surrounding one-shot A_2 should be set so that its output pulse width is less than $t = t_i - t_3$, where t_i is the sample-interval time and t_3 is the width of the pulses emanating from one-shot A_3, which is set to give a minimum width of 10 μs.

Thus, assuming A_1 and A_3 are set for the minimum width possible, analog signals appearing at the input will be sampled and transferred to the output of the second sample-and-hold device after a delay time approximately equal to t, the time set by A_2. □

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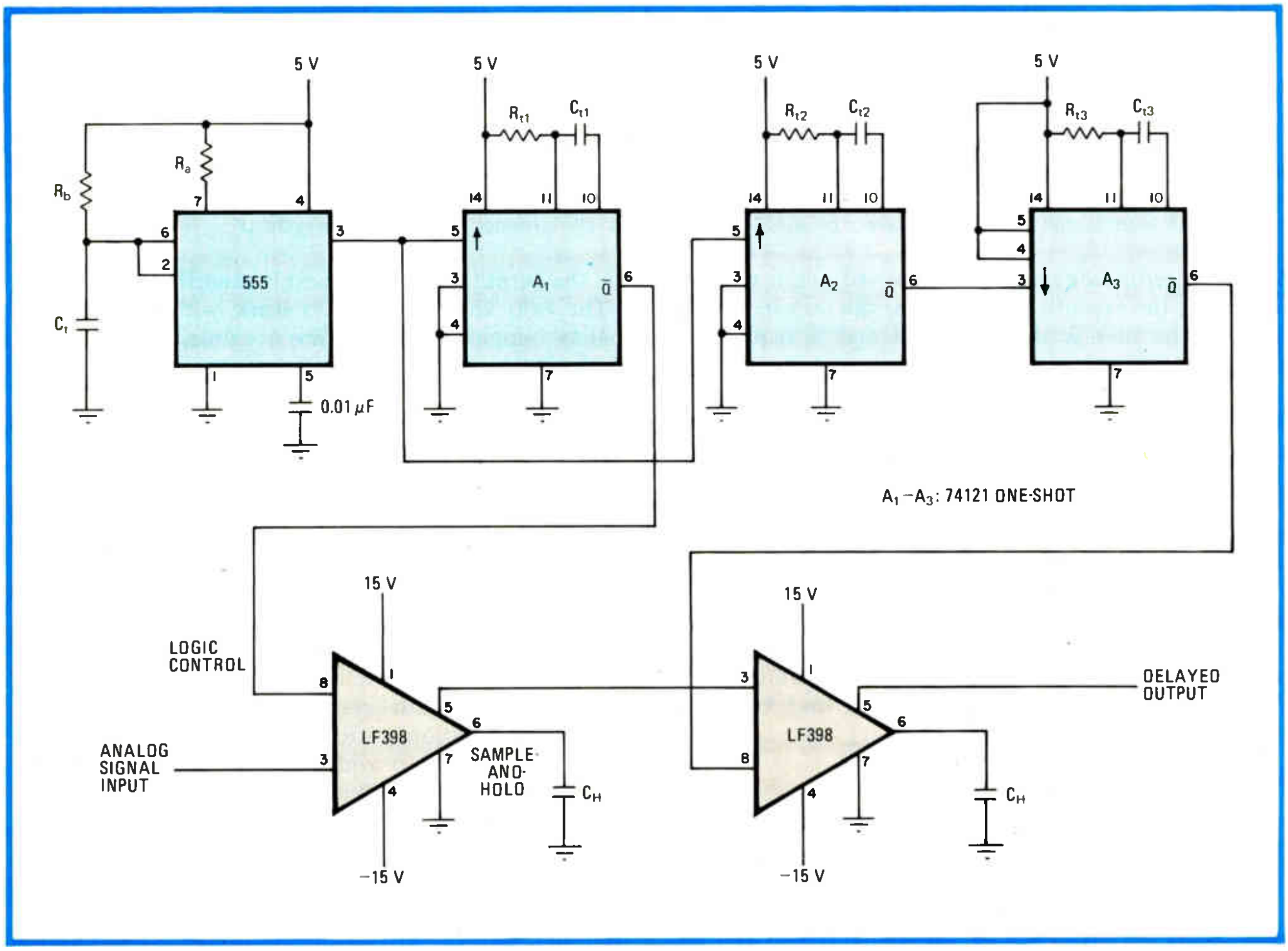


Discrete delay. Stand-alone sample-and-hold modules, suitably clocked, will serve to delay analog signals. Sampling frequency set by 555 should be at least twice the highest analog frequency to be processed. One-shot multivibrator A_2 sets delay time.

Bipolar current mirror scales, inverts signals

by Henry E. Santana
Hewlett Packard Co., Loveland, Colo.

A pair of operational amplifiers and a few resistors build this precision current mirror. Though simple and low in cost, the circuit excels the usual designs because it not only offers true bipolar operation but also can scale and/or invert any ac or dc input signal.

Input currents are applied to op amp A_1, which is biased by V_{ref}. If I_{in} is generated by a constant current source, V_{ref} may be brought to zero. Otherwise, it should be set to some arbitrary value to maintain circuit bias.

A current-to-voltage converter at the input and a voltage-to-current converter at the output comprise the current mirror. As a consequence of the configuration, the voltage appearing at the output of A will thus be:

$$V_{A1} = V_{ref} + I_{in}R_1$$

for $R_1 >> R_2$ and R_L. The voltage applied to the output circuit is therefore:

$$V_2 - V_1 = I_{in}R_1$$

Writing the nodal equations for V_L, V_3, and V_4 yields these results:

$$I_L = -V_L(1/R_2 + 1/bR_2) + V_3(1/bR_2) + V_2(1/R_2)$$
$$V_3 = A_2(s)\,(V_L - V_4) = (GB/s)(V_L - V_4)$$
$$V_4 = V_1[a/(1+a)] + V_3[1/(1+a)]$$

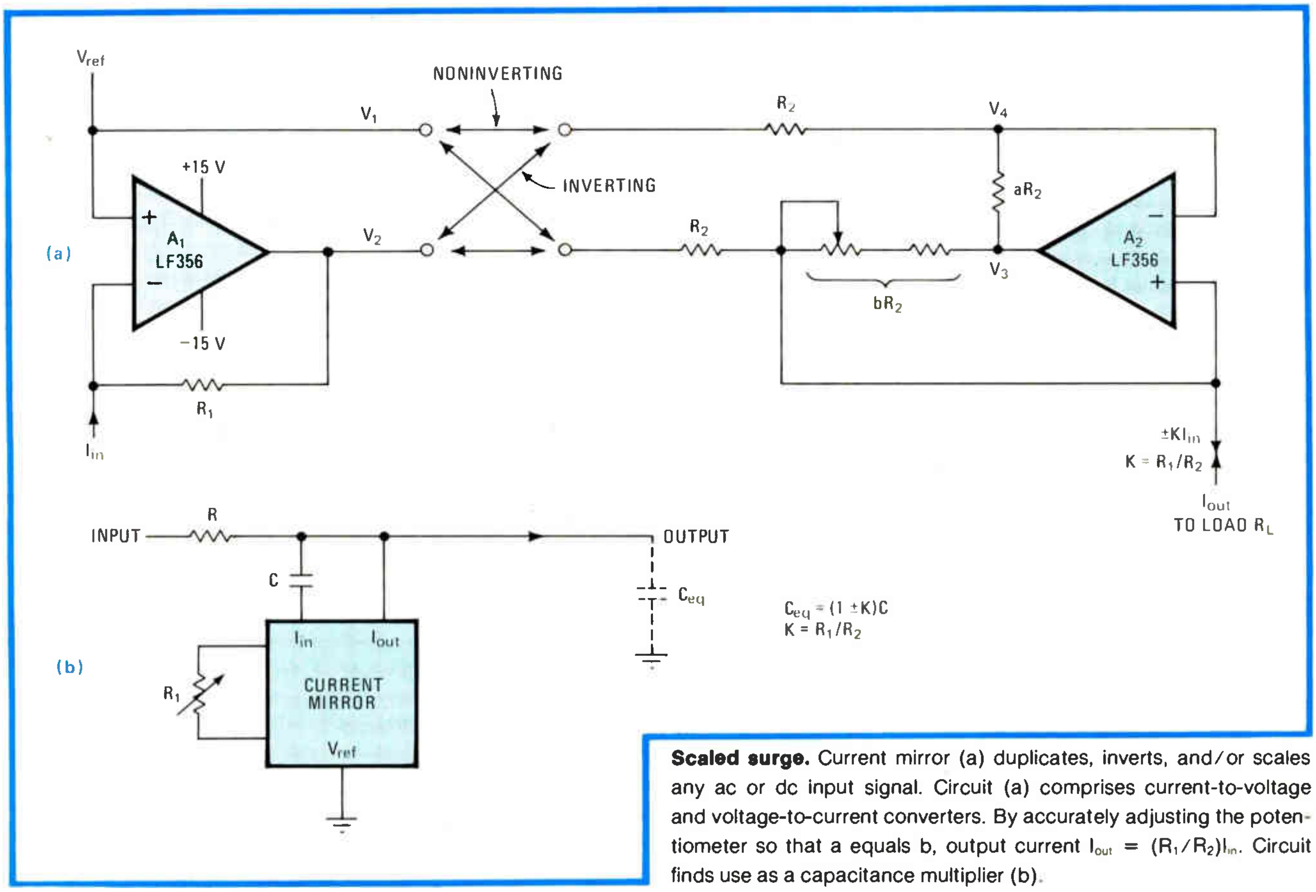
where GB is A_2's gain-bandwidth product. Substituting V_3 and V_4 into the equation for I_L, it is seen that $I_L = (R_1/R_2)I_{in}$, given that $a = b$ and $s << GB/(1+b)$.

The output impedance can be set, within limits, by selection of aR_2 and bR_2. The output impedance is:

$$Z_o(s) = \left[\left(\frac{a}{1+a}\right)\left(S+\frac{GB}{1+b}\right)R_2\right] \div \left[S+\left(\frac{a-b}{1+a}\right)\left(\frac{GB}{1+b}\right)\right]$$

Since a must equal b for the circuit to work, this equation simplifies to $Z_o(s) = [1/(1+a)]\{1 + [1/1+a)]GB/s\}\ R_2$, and no other assumptions about resistor ratios are made.

In addition to its use as a scaled current mirror, the circuit will find other not-so-obvious applications. Such an example is its use as a capacitance multiplier (b). □



Scaled surge. Current mirror (a) duplicates, inverts, and/or scales any ac or dc input signal. Circuit (a) comprises current-to-voltage and voltage-to-current converters. By accurately adjusting the potentiometer so that a equals b, output current $I_{out} = (R_1/R_2)I_{in}$. Circuit finds use as a capacitance multiplier (b).

Digital phase shifter covers 0° to 360° range

by J. W. V. Storey
Dept. of Physics, University of California, Berkeley

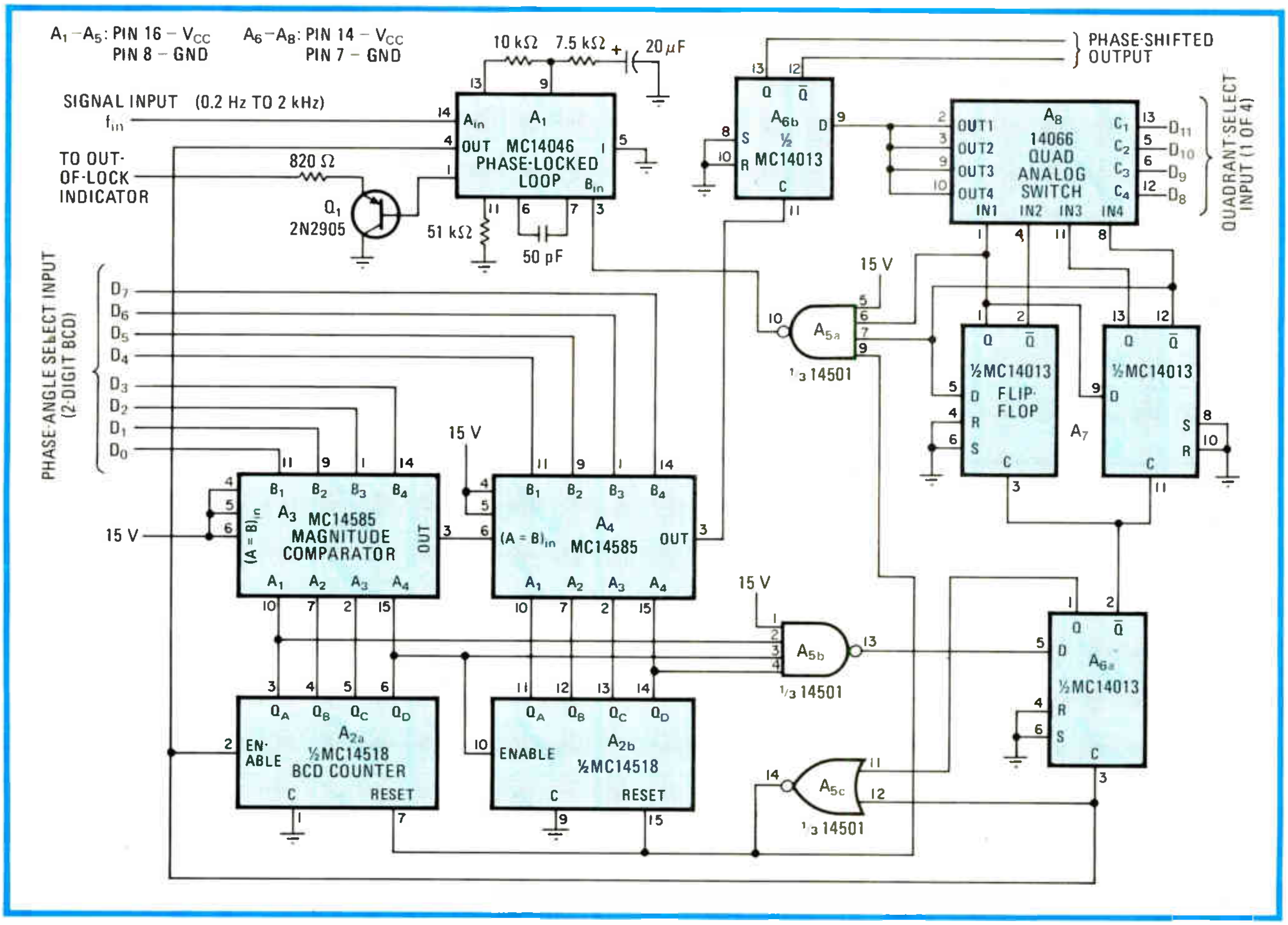
Offsetting the phase of a signal by digital means over the range of 0° to 89° in any quadrant, this low-power circuit is particularly useful in data-recovery systems that employ synchronous detectors. Unlike most RC phase shifters, the value set is independent of the input frequency.

The input reference signal is first introduced to the 14046 phase-locked loop. Its output, which is set to generate a frequency 360 times that of f_{in}, is then applied to the 14518 binary-coded decimal counter, where it is divided by 10. A second, cascaded counter, A_2, divides A_{2a}'s output by 9, the 89th count of a 90-step cycle being detected by A_{5b}. A_2 is then reset to zero on the 90th count by A_{6a} and A_{5c}.

The signal at the output of A_{6a} is thus at a frequency equal to $4f_{in}$. Flip-flop A_7 performs a divide-by-four operation on this signal, at the same time generating four quadrature outputs. Meanwhile, A_{5a}, which generates one pulse per cycle of f_{in}, locks the PLL in phase with the zero count of A_2. Note that the operation of this divider chain is unaffected by the setting of the digital input lines.

The desired phase is selected by applying the appropriate digital signals D_0–D_7 in binary-coded decimal form. Thus, the output from A_3 and A_4 moves high when A_2 counts to that number and clocks flip-flop A_{6b}. This action occurs four times per each cycle of f_{in}. The appropriate quadrant, available at A_7, is selected by digital inputs D_8–D_{11}, the active quadrant corresponding to which one of the lines is high. Flip-flop A_{6b} thus produces a symmetrical square wave at f_{in} having a phase shift equal to the number of degrees specified plus 0°, 90°, 180°, or 270°. There is an additional phase shift of 0.5° at all settings because of the way the PLL is operated to achieve lock. The error can be eliminated by adding an inverter between the output of A_{5a} and the B input of A_1.

With the component values shown and a 15-volt supply, the circuit will operate over the range of 0.2 hertz to 2 kilohertz. Thumbwheel switches with 1-megohm pull-down resistors are used to set the phase-angle input lines. A four-position switch can be used to select the quadrant. With slight modification, the circuit will find application as a digitally controlled ignition timing system for internal-combustion engines. □



Discrete degrees. Circuit sets 0° to 360° phase shift of reference signal by digital means. Digital inputs D_0–D_7 determine displacement over 0° to 89° range, D_8–D_{11} set quadrant. Output is thus 0° to 89° signal shifted by an additional 0°, 90°, 180°, or 270°.

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8085A	✓		✓		✓		✓		✓		✓	
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8039	✓		✓		✓		✓		✓		✓	
8039-6	✓		✓		✓		✓		✓		✓	
8035	✓		✓		✓		✓		✓		✓	
8021	✓		✓		✓		✓		✓		✓	
8048	✓		✓		✓		✓		✓		✓	
6802	✓		✓		✓		✓		✓		✓	
6800	✓		✓		✓		✓		✓		✓	
F8	✓		✓		✓		✓		✓		✓	
3870	✓		✓		✓		✓		✓		✓	
3872	✓		✓		✓		✓		✓		✓	
Z80A	✓		✓		✓		✓		✓		✓	
TMS9900	✓		✓		✓		✓		✓		✓	
SBP9900*	✓		✓		✓		✓		✓		✓	
1802	✓		✓		✓		✓		✓		✓	

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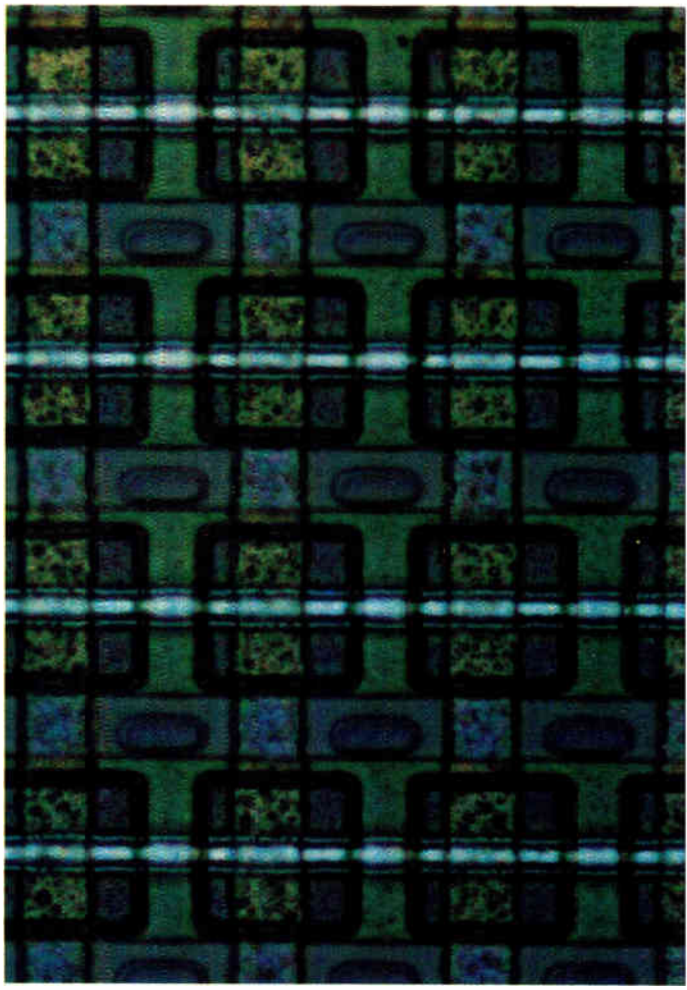
ISSCC: a gallery of gigantic memories,

by John G. Posa, *Solid State Editor*, and Roger Allan, *Components Editor*



Other dominant themes are the use of switched-capacitor technology for telecommunications and monolithic converter systems complete with data latches and voltage references

☐ *More than any other gathering, the International Solid State Circuits Conference assesses the state of semiconductor technology. This year's meeting of the minds behind leading-edge integrated circuits attests to no slowdown in device ingenuity. It marks the debut of the quarter-megabit dynamic memory and the 64-K static random-access memories, as well as a look into the makings of 0.5- and 1-megabit dynamic RAMs. So remarkable are these advances that they almost overshadow the two totally complementary-MOS 16-K static memories—significant developments in their own right.*

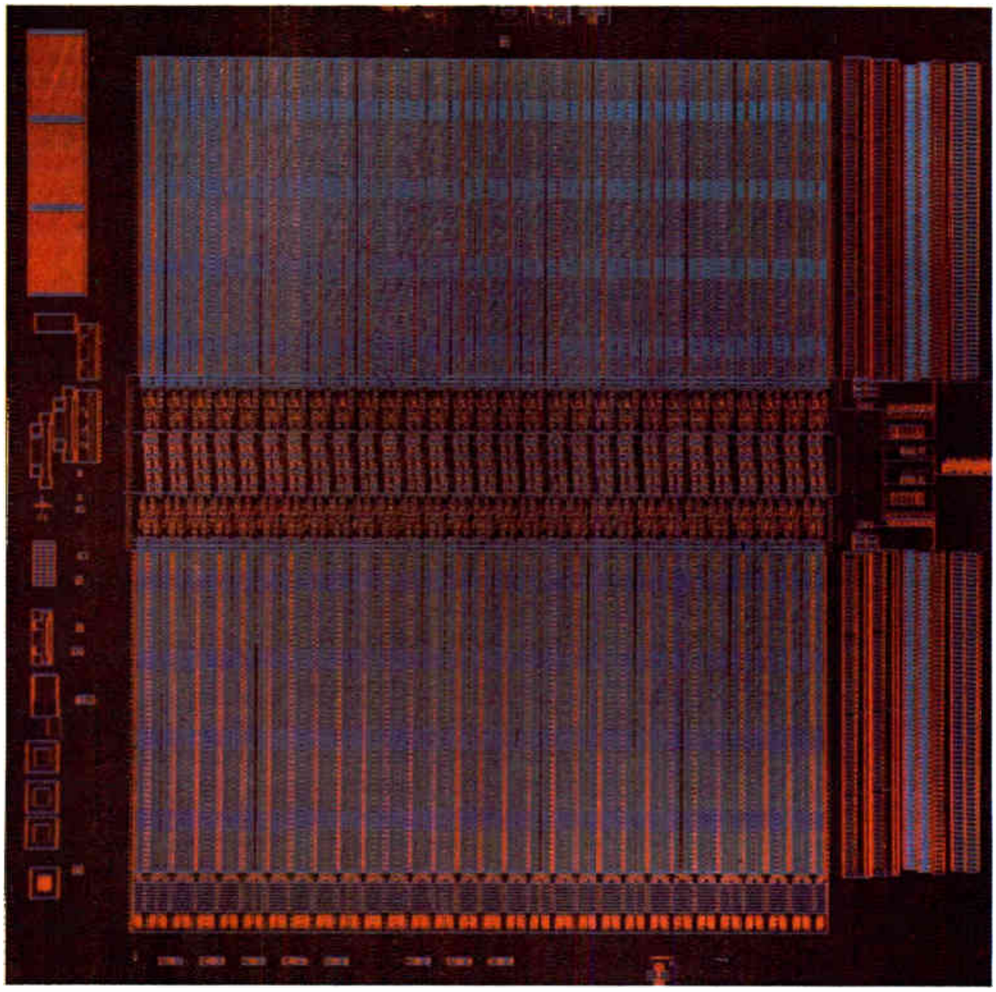
Aside from the biggest memories yet, the conference chairpeople say that the theme for the 27th annual meeting in San Francisco is "systems on chips." And so it is; signal-processing systems on silicon, monolithic telecommunications systems, single-chip data-acquisition systems, minicomputers on chips—they are all here.

The presentations also submit proof that with this new decade the era of very large-scale integration emerges. There is no standard of VLSI, but it is hard to deny that chips measuring in excess of 100,000 square mils, or packed with over a quarter million devices, do represent integration on a scale grander than just large. Even if geometry is the yardstick, 1-micrometer features are soon becoming the rule rather than the exception.

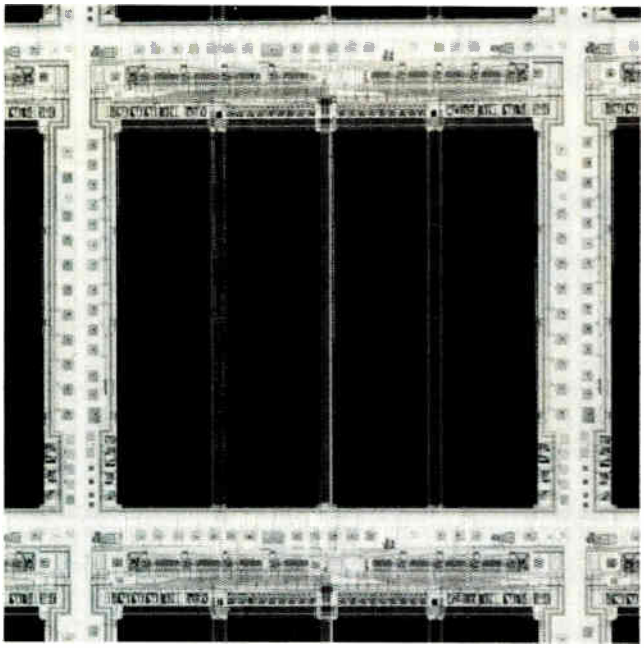
Besides the level of integration, speed is also of the essence. Now apparent are techniques for coercing MOS logic to run at gigahertz speeds. Fabricating, modeling, and predicting the behaviour of tomorrow's integrated circuits are also on the bill.

NEC-Toshiba Information Systems Inc. and NTT-Musashino Electrical Communication Laboratory, both of Tokyo, each present 256-K-by-1-bit dynamic RAMs in late papers. The NEC-Toshiba chip has a 160-nanosecond access time and a 350-ns cycle time, while the NTT device, which uses molybdenum to speed signal propagation, accesses in just 100 ns and cycles in double that. NEC-Toshiba's chip consumes 225 milliwatts of active power and 25 mW on standby, while NTT's device uses

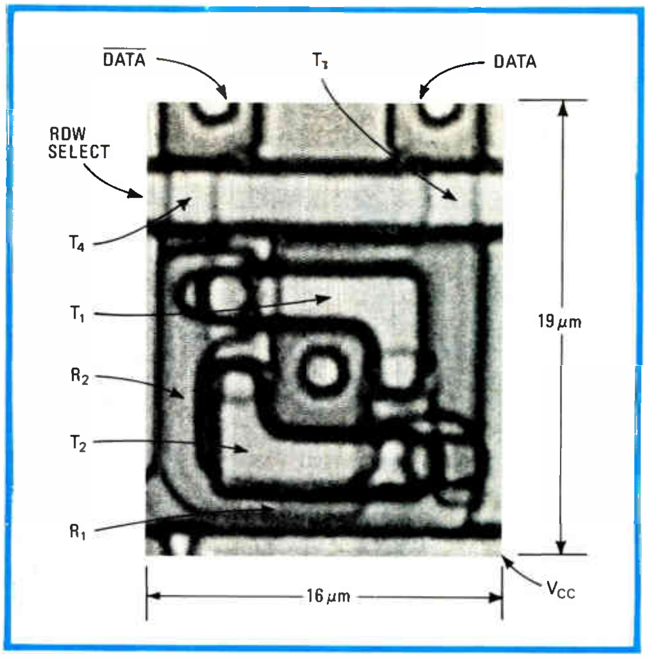
gigabit logic, and single-chip systems



Chip parade. At left is a close-up of the elements in a charge-injection-device image sensor from General Electric Corporate Research and Development. It features high speed and low noise. At the upper right is 64-K bipolar random-access memory from International Business Machines Corp. that has a 50-ns access time. The television picture is made possible by an image sensor described in a late paper from Matsushita Electric Industrial Co.



1. Quarter megabit. Two 256-K dynamic RAMs are introduced at ISSCC. One is from NEC-Toshiba Information Systems, and the other, shown above, is from the NTT-Musashino Lab. NTT's chip employs redundant cells and molybdenum for a 100-ns access time.



2. 64-K static. Matsushita appears to be the first to announce the truly static 64-K RAM. Each 16-by-19-μm^2 cell incorporates four transistors (the Ts) and two polysilicon load resistors (the Rs). The array is n-channel; the peripheral circuits, C-MOS.

230 mW but only 15 mW on standby. Both designs require a 256-cycle/4-millisecond refresh.

NEC-Toshiba uses two levels of polysilicon, 1.5-μm direct-step-on-wafer photolithography, and all-dry processing to build its RAM. The device is already being shown in a 16-pin package, the pinout of which meets the Joint Electron Device Engineering Council's standard with the eighth address line on pin 1. The oblong die, measuring 191 by 338 mils, contains two 128-K arrays. Each array is further split into two 128-by-512-bit sections, separated by 512 sense amplifiers that run the length of the chip. Various techniques, including silicone coating, are used to keep the mean time between failure due to alpha radiation below 30,000 device hours.

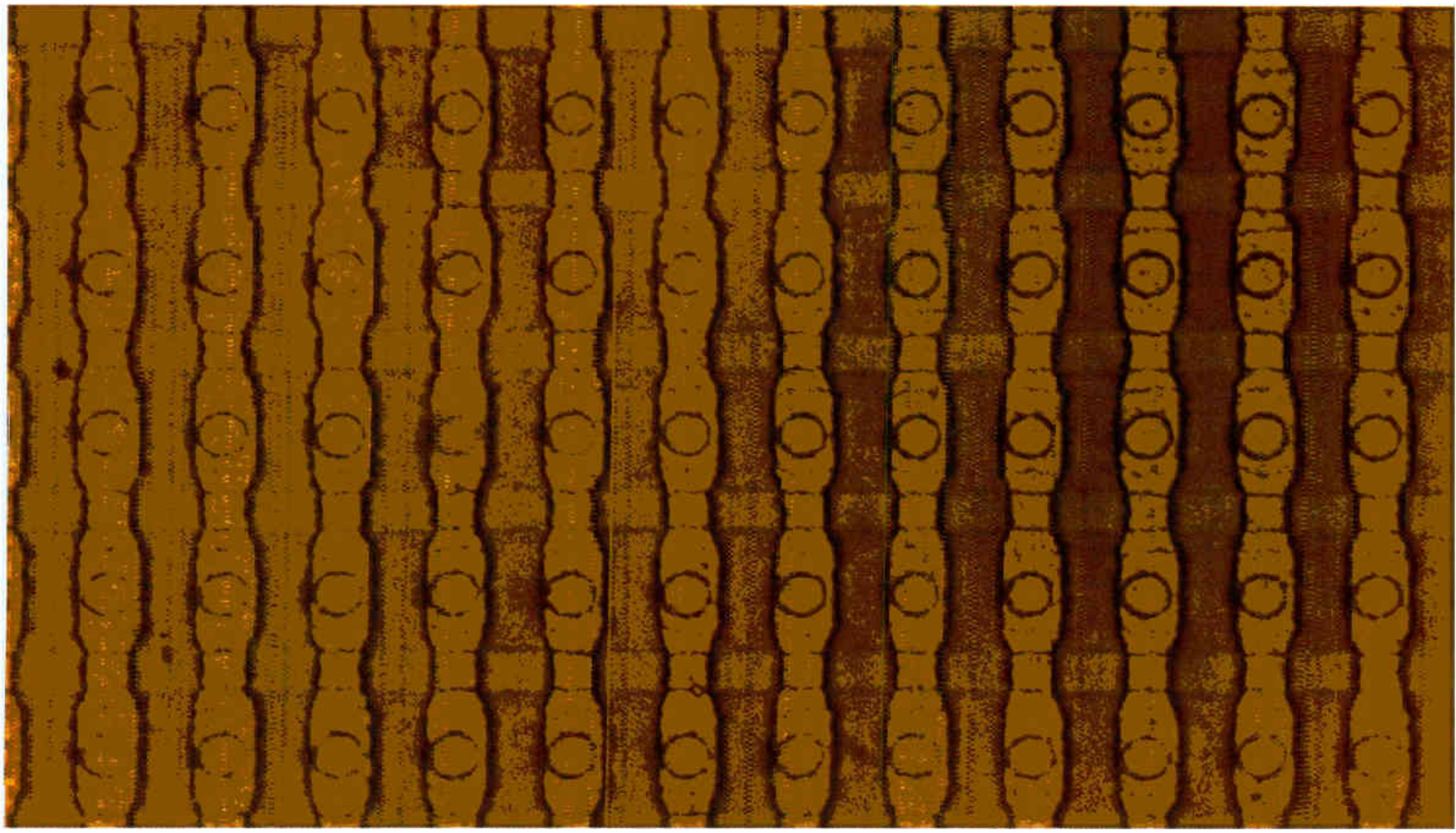
NTT-Musashino's RAM is built with electron-beam direct writing, dry processing, and three interconnection levels: molybdenum word lines, aluminum bit lines, and polysilicon for storage capacitor electrodes and gates of non-array devices. NTT's die is organized just like NEC-Toshiba's but with one interesting difference: each 128-K array has attached to it a 2-K block of redundant cells and a dummy sense circuit. The extra cells, connected via four pairs of spare bit lines and two spare word lines, are replaced by electrically programming on-chip polysilicon resistors during wafer probing. The additional circuits take up no more than 10% of NTT's nearly square 230-by-232-mil die, shown in Fig. 1.

Even more dynamic RAMs may be the product of another late paper, this one authored by Japan's Cooperative Laboratory of Kawasaki. Using a variant of its quadruply self-aligned MOS structure [*Electronics*, Dec. 6, 1979, p. 124] called the stacked-high capacitor RAM, it has built experimental 512-K and monolithic megabit chips measuring 70,680 and 131,192 mils, respectively. The cells are so small (52 μm^2) that tantalum oxide (Ta_2O_5) is employed for its higher dielectric constant in the storage capacitors. These devices are based on a 256-cycle refresh and a simulated 170-ns access time.

Clearly the most ambitious static RAM is the 64-K device from the semiconductor research lab of the Matsushita Electric Industrial Co. of Osaka. The device exemplifies the construction of future static parts; they will use polysilicon load resistors, of course, and although the array will be n-channel, the peripheral circuitry will be complementary-MOS for low power. Such is Matsushita's RAM: organized as 8 K by 8 bits, the device dissipates 300 mW and 75 mW in active and standby modes, respectively. Double-level polysilicon and 2-μm design rules result in a chip size of 48,906 mil^2 and a cell size of 304 μm^2 (see Fig. 2).

Three 64-K dynamic RAMs are described in session 17: two MOS types, plus a very creative 8-K-by-8-bit bipolar memory called the 1/N fractional device from International Business Machines Corp. A paper by workers from several IBM groups says the 1/N cell is the bipolar equivalent of the single-transistor MOS memory cell, only twice as fast: the 1/N 64-K RAM has a 50-ns access time and a 100-ns cycle time.

Word lines in this IBM memory connect to the bases of npn transistors that have eight emitters. Each emitter connects to a storage capacitor located directly above it; the other side of the capacitor connects to a bit line.



3. 64-K bipolar. Not only did IBM Corp. build another 64-K RAM, but this time it also uses bipolar technology for a remarkable 50-ns access time. It is called the 1/N fractional device, and it has an 8-K-by-8-bit organization. Aluminum bit lines run vertically in this photo.

Doped polysilicon makes contact with an emitter and simultaneously forms the bottom plate of a capacitor, while aluminum is used for the bit lines. The device draws half a watt from a single +5-V supply and needs a 257-cycle refresh every 3 ms. It is built with 2.5-μm lithography, and IBM says the structure is conducive to scaling. A close-up of the chip's array is shown in Fig. 3.

The other two 64-K RAMs are from the Hitachi Central Research Laboratory, Tokyo, and Texas Instruments Inc.'s MOS memory division in Houston, Texas [*Electronics*, Sept. 28, 1978, p. 109]. Hitachi incorporates a substrate-bias generator for 5-volt only operation—a requirement for the U. S. market. The device is divided into eight 128-by-64-bit arrays, giving a highly rectangular shape of 125 mils by 296 mils. A combination of circuit-design, packaging, and chip-coating techniques protect it from alpha particles.

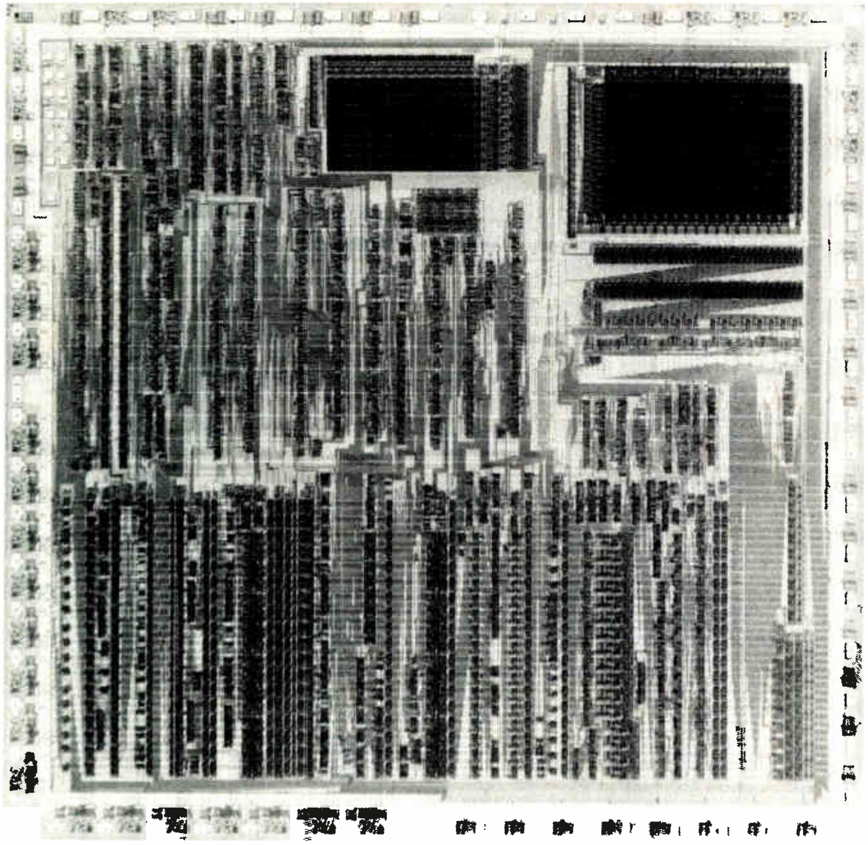
Unlike in Hitachi's RAM and in fact all others, the substrate of TI's 64-K device is grounded and thus needs no charge pump. Here the secret is explained: a novel sense amplifier design pumps up each logic 1 in the memory to a full V_{DD} level. Also employed is an interlocked clock scheme to eliminate race conditions.

Two 16-K fully C-MOS static RAMs are detailed in session 17, one from Hitachi Ltd. and one from Toshiba Corp. of Kawasaki. The Toshiba chip, which was unveiled at the International Electron Devices Meeting [*Electronics*, Dec. 6, 1979, p. 124] uses only 1 microwatt for standby retention; Hitachi's consumes only 5 μW on standby. Hitachi goes to the trouble of putting the chip in two 24-pin packages: one is compatible with the Jedec standard for erasable programmable read-only memories; the other replaces the output-disable pin with a supplementary active-high chip select for easy battery-backup design.

Low power

Speaking of battery backup, by using some novel circuit configurations, Mostek Corp. of Carrollton, Texas, has dramatically lessened the standby power requirements of the popular 4-K-by-1-bit 2147 and 1-K-by-4-bit 2148 high-speed static RAMs—without the need for extra pins. Mostek's versions, to be called the MK 4147 and MK 4148, both have 55-ns access times.

The technique is outlined in a session 6 paper. When the user supplies a 5-V level to the write-enable pin ($\overline{WE}$), V_{CC} can be turned off. In this condition, peripheral circuits dissipate no power and the array on standby draws only 30 microamperes. When to override the chip-select buffer and to switch internal power sources is



4. C-MOS CPU. Fujitsu Ltd. built this C-MOS processor for a business computer. It uses C-MOS for low power consumption, double-level metal for speed, and a computer-aided standard cell layout scheme. The chip measures a whopping 172,484 mil².

decided automatically when V_{CC} is lower than $\overline{WE}$ by at least a volt. An auxiliary substrate charge pump also kicks in during backup to keep subthreshold conduction sufficiently low for data retention.

IBM Laboratories, Boeblingen, West Germany, discusses in session 17 an interesting 16-K-by-1-bit bipolar static RAM having a 45-ns access and a 100-ns cycle time. (One of the authors is S. K. Wiedmann, a pioneer of integrated injection logic.) The device is called an MTL/I^2L memory because it borrows from merged transistor logic and I^2L. The cells are small—comprising just four devices, they measure only 640 μm^2—and they also have extremely low standby power, in the subnanowatt range. In fact, this bipolar RAM dissipates less than 100 μW in what IBM calls quasi-nonvolatile operation.

Read-only session

Session 12, "ROMs, PROMs, and EROMs," is dominated by Intel Corp. It supplies one of the three 64-K E-PROM papers (the other two belong to Mostek and Motorola Inc. of Phoenix), it has a paper on a 16-K electrically erasable PROM, or EE-PROM, and a third on a 35-ns bipolar PROM. The remaining paper in the session concerns a unique 4-megabit full-wafer ROM from NTT Musashino. There is also a late E-PROM paper from Texas Instruments.

To keep pace with today's high-speed microprocessors, E-PROMs have gotten much faster. Not only have densities quadrupled recently, but access times have been more than halved. The 64-K devices from Intel and Motorola, for example, both have 200-ns access times compared to the 450 ns of the standard 16-K 2716. Intel scaled way down for a cell size of just 0.24 mil² and a die size of 32,400 mil². Motorola offers its device in a 24-pin package for compatibility with the 64-K ROM and it also plans a 28-pin version, which will be compatible with the other maker's devices [*Electronics*, Sept. 27, 1979, p. 40].

TI's X series of E-PROMs and Mostek's 64-K device both incorporate cell structures that, when viewed from above, look like crosses. Mostek's memory is most unusual in that it uses redundant circuitry to improve yield. The 8-K-by-8-bit memory has four 2-K-by-8-bit arrays and two 2-K-by-4-bit spares. The redundant circuitry comes complete with column-decode and -select logic, sense amps, and a data-in buffer. If a failed bit is uncovered during testing, a so-called repair buffer blows a polysilicon fuse that routes a redundant matrix to the input and output multiplexers instead of the bad area.

Although TI recently unveiled a 64-K E-PROM, it is using its new X series approach for dense (41,500-mil²) 128-K and fast (100-ns) 32-K memories. The larger memory is edge-activated and features a pipeline precharge technique that allows the cycle time to equal the chip's 200-ns access time. The memory also has a standby mode that reduces power consumption to a matter of only 15 mW.

Intel springs the details of its EE-PROM replacement for the 16-K 2716 E-PROM in session 12. The device uses a new technology called Flotox, for floating-gate tunnel oxide. The floating gates are both programmed and erased by electron tunneling. Just 25 V persuades the electrons to jump the gap of less than 200 angstroms from the substrate to the gate to write the cell.

Electrically erasable

A complete cell in the Intel EE-PROM consists of two transistors: one for cell selection and one for storage. The device is word- and chip-erasable; either process takes 10 ms. (That compares very favorably with the 2716's half-hour under the ultraviolet lamp.) Power dissipation is very nearly that of the 2716 (500 mW active, 100 mW standby), but access time is as fast as in Intel's new 64-K E-PROM.

Intel's 35-ns bipolar fuse-link PROM represents another breakthrough, in view of the fact that the few other 16-K PROMs in existence take twice as long as its 25-ns (typical) specification to relinquish data. The fuse material is Intel's usual polysilicon, and double-level metalization is employed. But a new process brings die size down to 19,600 mil^2. Diffused isolation, Schottky base contacts, and 3-μm feature sizes are other characteristics. Power consumption is 600 mW.

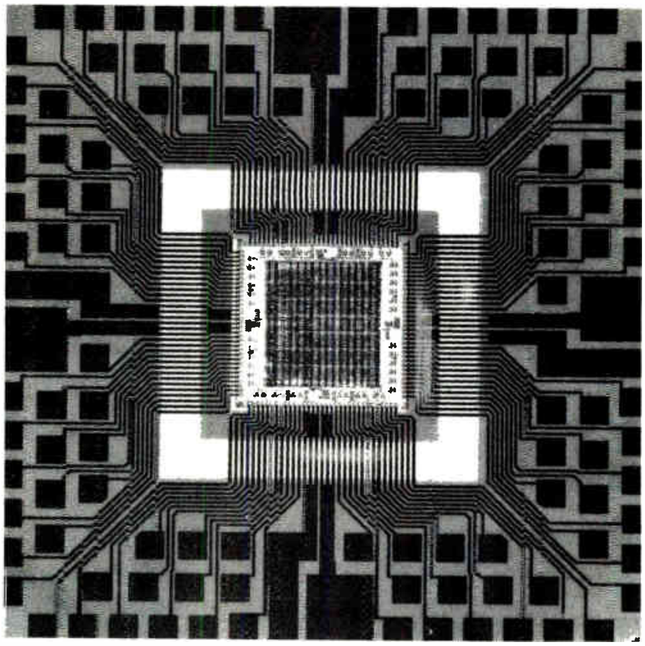
NTT-Musashino's full-wafer ROM is designed for a Chinese ideograph character generator. The memory uses a charge-coupled-device–like multigate MOS structure and duplicate cell blocks to circumvent otherwise devastating yield problems. The 3-inch wafer holds four 1-megabit modules that together store 15,040 16-by-18-dot characters. Access time for a character is a rather long 12 μs, but NTT says this will do for printers and cathode-ray tubes.

Good image

Session 2, on charge-coupled devices and imaging, signals a proliferation of low-cost portable color video cameras in the 1980s. Matsushita, NEC, and Hitachi each present color sensors, but they are vastly different. Matsushita's 413-by-506-element chip employs a $ZnSe$-$Zn_{1-x}Cd_xTe$ heterojunction thin-film photoconductor to sense incoming light; NEC uses CCDs in its 384-by-490-element matrix; and Hitachi employs an array of 485-by-384 MOS elements. Matsushita and Hitachi have also both put color filters on chip.

Black-and-white CCD sensors come from Fairchild Camera and Instruments Corp.'s MOS/CCD division in Palo Alto, Calif., and from General Electric Corporate Research and Development in Schenectady, N. Y. Fairchild's 1,030-by-128-element sensor was developed for applications at low light levels like starlight. It has a floating-gate structure optimized for image sensing as well as two floating-gate amplifiers that increase input dynamic range.

GE's sensor, of the row readout variety, emphasizes high-speed, low-noise operation, and high spectral sensitivity. Readout rates as high as 8 megahertz are possible with 128-by-128-element test arrays. To extend sensitivity into the blue region of the spectrum, a thin 1,000-Å layer of polysilicon is used as the bottom level of the electrodes. Over this is deposited a fine 2-μm aluminum-line to lower resistance.

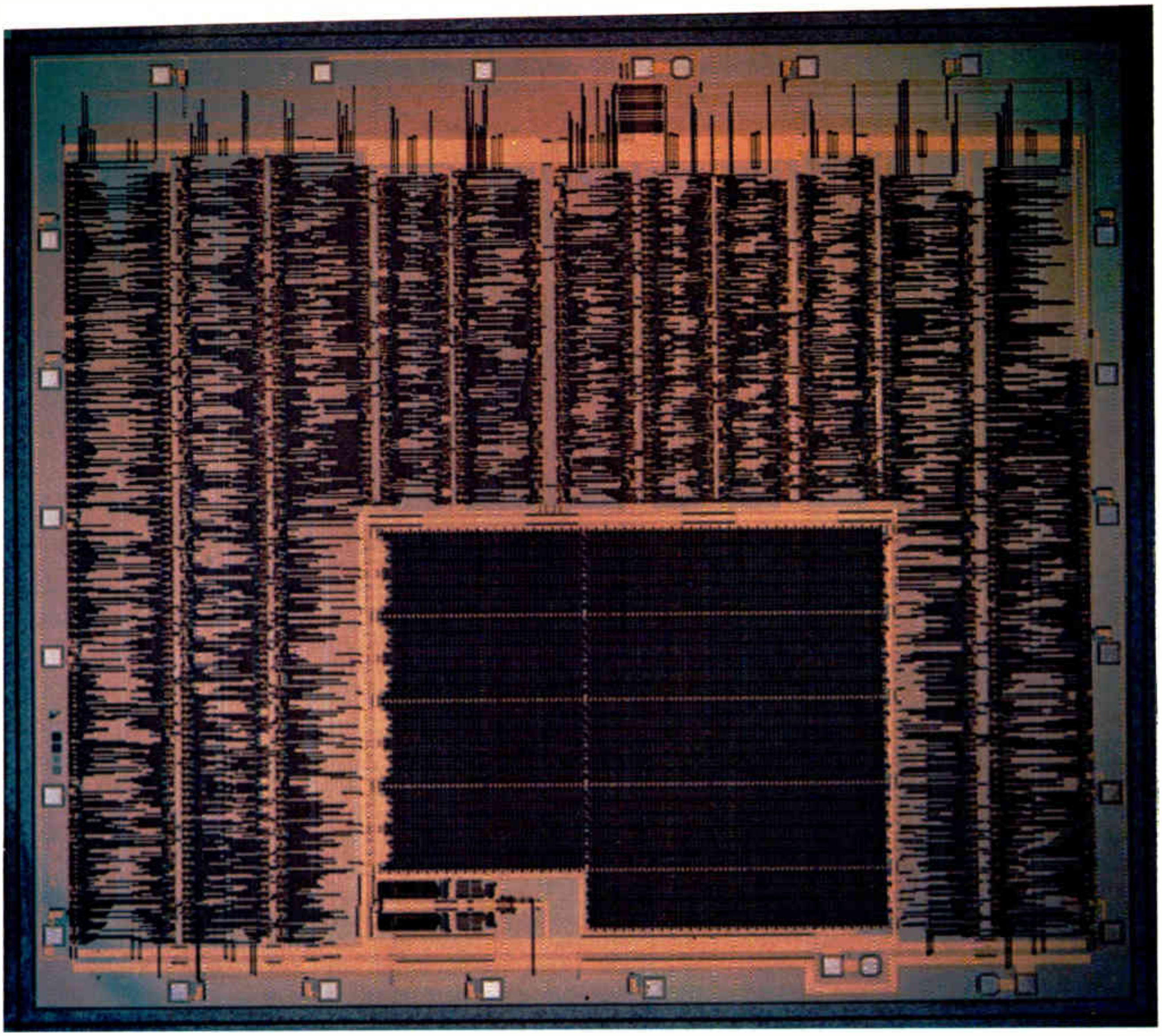


5. Bipolar ALU. This 18-bit register and arithmetic and logic unit comes from NEC-Toshiba Information Systems. It sports three metal levels and effective base widths of just 0.2 μm. This machine can exercise a read-modify-write cycle in 7 nanoseconds.

Also in session 2, GE describes charge-domain recursive filters that "represent about an order of magnitude increase in the speed or bandwidth capabilities of CCD signal-processing circuits," says Jerome J. Tiemann, who presents a late paper. Only passive operations—charge packet division and/or merging—are needed to build high-pass, low-pass (and hence, bandpass) filters with Butterworth, Chebyshev, and even elliptic response characteristics. This is all done without on-chip amplification, so that it is physically impossible for these filters to become unstable.

Systems on chips

Adding validity to the idea that systems on chips are forthcoming is session 9 where four sophisticated processor chips are announced. One is from Data General Corp. (see p. 119). Another is built with C-MOS by the IC division of Fujitsu Ltd., Kawasaki, for a business data-processing application. The approach addresses some of the physical limitations inherent in moving to very large-scale integration. For example, straight MOS would consume too much power, so C-MOS was used; double-level metalization was chosen in lieu of doped polysilicon because the latter's resistance is too high; to make use of computer-aided design facilities, a standard cell layout



6. Echo . . . echo . . . Bell Labs is responsible for this 111,428-mil² echo canceler IC. The single-chip system subtracts an echo replica from the return signal after a delay. The dense block contains a 2,704-bit shift register; the rest is 3,300 random-logic gates.

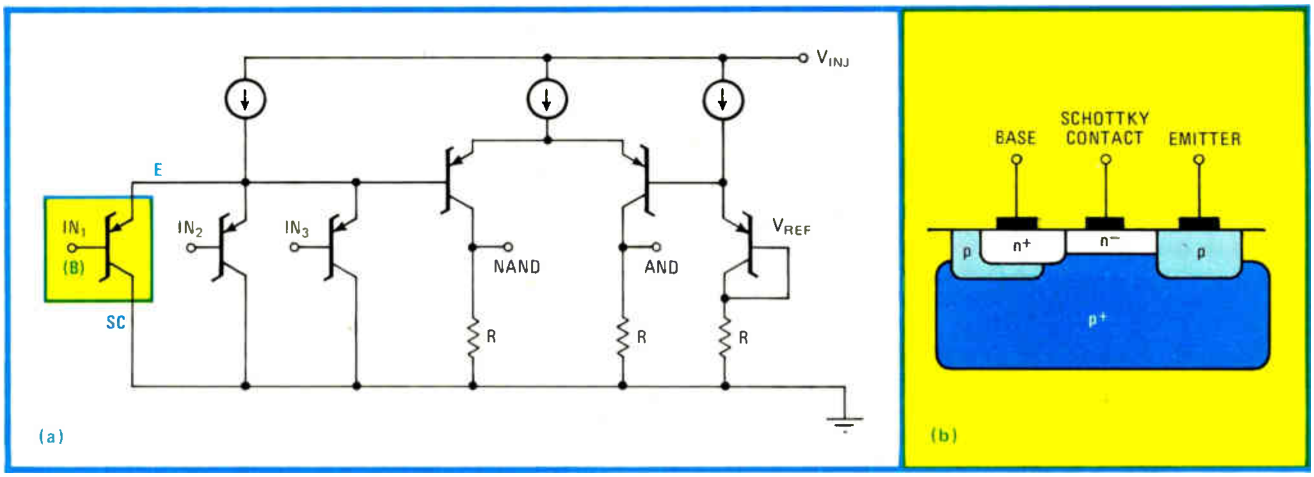
scheme was adopted. There is no free lunch, however; the chip's area is 172,484 mil². That's right—172,484 mil² (see Fig. 4).

The C-MOS processor has 40,000 transistors or about 10,000 gates. It operates on 16 megabytes of memory. Power dissipation is only 130 mW with a 2.5-MHz system clock.

Intel finally lets the 8087 math processor out of the bag in this session [*Electronics*, April 26, 1979, p. 33]. Its clever design was carried out by Intel Israel Ltd. in Haifa. It also seems that the 8087 must have been planned at the same time as the 8086. Not a peripheral chip, it scrutinizes the same instruction stream as the 8086 (or 8088) and, when it encounters an escape instruction, reads its own operand from memory instead of letting the general-purpose microprocessor do the work. Intel calls this by the name of coprocessing.

The 8087 operates on 16-bit data, 32- and 64-bit 2's complement integers, 32- and 64-bit real numbers, 80-bit binary floating-point numbers, and 18-digit (80-bit) signed, packed binary-coded decimal integers. The list of operations, too, is comprehensive; the 8087 will add, subtract, multiply, and divide; find remainders, square roots, logarithms, and trigonometric functions,; and convert to and from BCD. These functions are performed by over 65,000 H-MOS transistors on a 78,000-mil² die. With a 5-MHz clock, execution times range from about 4 μs for a comparison to 16 μs for a multiplication and 35 μs for division and finding square roots.

Also meant for higher-speed computation is the 18-bit bipolar register and arithmetic and logic unit described



7. ECL + I²L = ECIL. In an emitter-coupled injection-logic gate (a), emitter followers drive a differential stage for AND and NAND outputs. A device cross section is shown in (b). Transistors are built in an n-type epitaxial layer, and a p-type injector rail is situated near by.

by NEC-Toshiba. The circuit employs some fancy bipolar processing for brilliant performance. All electrodes except the emitter and a first level of interconnection are formed in polysilicon before the transistor. A second polysilicon electrode serves as the emitter electrode, and the tolerance is so tight as to yield a 0.2-μm base width. The structure also incorporates three-level metalization: polysilicon alloyed with platinum, then aluminum, and finally gold. A basic gate winds up with a 400-picosecond delay time, making the ALU capable of a 7-ns read-modify-write cycle (Fig. 5 shows the chip and its elaborate pad ensemble).

Applied LSI

"LSI Applications," the title of session 3, contains four single-chip systems dedicated to signal processing as well as two radio tuning circuits from General Instrument Corp., Hicksville, N. Y. Bell Laboratories shines in this session with a signal processor, a code converter, and an echo canceler, none of them trivial. NEC also shows a digital signal processor.

Bell's code converter paper is coauthored by Hewlett-Packard Co.'s Laboratories in Palo Alto. In it, a bipolar IC converts analog telephone signals that have been digitized using the A-law encoding scheme to those in μ-law format, and vice versa. Since North American pulse-code modulation complies with μ-law and European digital networks use A-law, this chip forms the go-between for future digital transatlantic telephone communications.

The echo canceler takes a huge chunk of circuitry and reduces it to the 111,428-mil² die shown in Fig. 6. Primarily intended for satellite telephone communications, the system attenuates echos by creating an echo replica and subtracting it from the return signal after the proper time delay. Either A-law or μ-law inputs and outputs can be selected. The chip is fabricated from 5-μm n-MOS using five masks, and it dissipates 750 mW from +5-V and +12-V supplies.

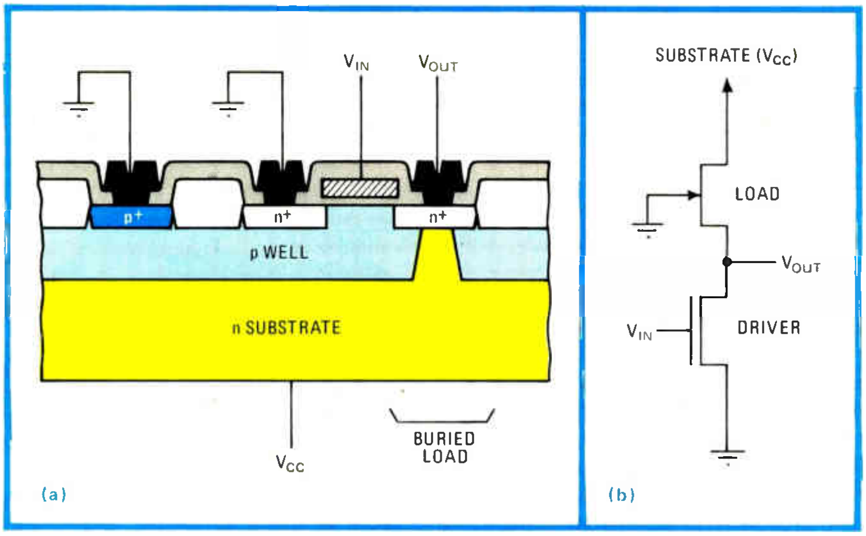
Speed and more speed is the subject of session 6, "Digital Circuit Techniques," whose methods are applied both to MOS ICs and to bipolar. Emitter-coupled injection logic is a high-speed merged bipolar technology from the Technische Hochschule in Aachen, West Germany. It is compatible with I²L. In an ECIL gate, pnp emitter-follower inputs drive a differential stage that supplies both AND and NAND outputs as shown in Fig. 7. As in I²L, individual transistors are arranged along an injector rail. The basic ECIL cell is larger than an I²L's, but the technology does have the complementary outputs and it is faster. With identical starting materials and design rules, an ECIL gate's delay is 4.2 ns; that of an I²L gate would be about 40 ns.

Mitsubishi Electric Corp. of Itami, Japan, has a logic form that is even faster than ECIL. The paper is entitled "Static Induction Transistor Logic Compatible with 1-GHz ECL Circuits." In ordinary static induction structures a buried n⁺ layer acts as the source for vertical junction FETs. During the doping of the drain, done from above, impurities diffuse up from the source and reduce the quality of the channel. Mitsubishi's trick is to compensate for these impurities with a p-type ion implantation. This lowers the effective channel length to only 0.2 μm and allows gigahertz speeds.

Speed demons

The buried-channel junction-FET gates from Fujitsu Laboratories Ltd. of Kawasaki reach 72.5-ps switching delays for 1.64-GHz toggle frequencies. The key here is scaling down. Masks are made with electron-beam lithography and reactive sputter etching brings out the device's 1-μm dimensions. It is said to have buried channels because ion implantation forms the channels of both the enhancement-mode drivers and the depletion loads.

The other fast MOS technology, buried-load logic, comes from Hitachi's Central Research Laboratories in Tokyo. Conventional drivers are formed in p wells, and buried under them are load devices, vertical JFETs. It is a



8. Merged MOS. Buried-load logic gates from Hitachi are formed in p-type wells (a). The load devices are vertical devices, buried under the drivers. When drivers are built with 3-μm channel lengths, power-delay products of only 0.17 picojoule result.

merged technology; the driver's drain is the source of the buried FET and the n substrate forms the common (grounded) source of all the load devices (see Fig. 8). Drivers with 3-μm channel lengths exhibit 0.34-ns gate delays and a power-delay product of just 0.17 picojoule.

Sessions 7 and 16 focus on design aids, IC processing, and technology limits. Included in the list of contributors to session 7 is Fujitsu Labs with a method for thermally growing 70-Å-thick gate oxides for VLSI. Stanford University, Palo Alto, supplies two papers. One presents a model for predicting the behavior of downward-scaled enhancement- and depletion-mode MOS FETs; it states that fundamental limits will be reached with channel lengths of 0.3 μm, supply voltages of 0.5 V, and power-delay products of 0.5 femtojoule. The other paper describes a 14,756-mil² capacitive replacement for the piezoelectric pressure sensor. Its current drain is only 20 μA with a 2.5-to-20-V supply.

In session 16, IBM's Poughkeepsie, N. Y., center tells of a focused, pulsed-dye laser that can actually add and delete interconnections in existing ICs to reroute lines and to bring out test pads. Photoresist is used for superficial modifications. To subtract a line, the exposed resist serves as a mask for etching; to add a line, it acts as a mask for a metal lift-off step. Furthermore, the beam energy can be adjusted to burn holes through silicon dioxide so as to contact underlying diffused regions. Who said bad chips cannot be fixed?

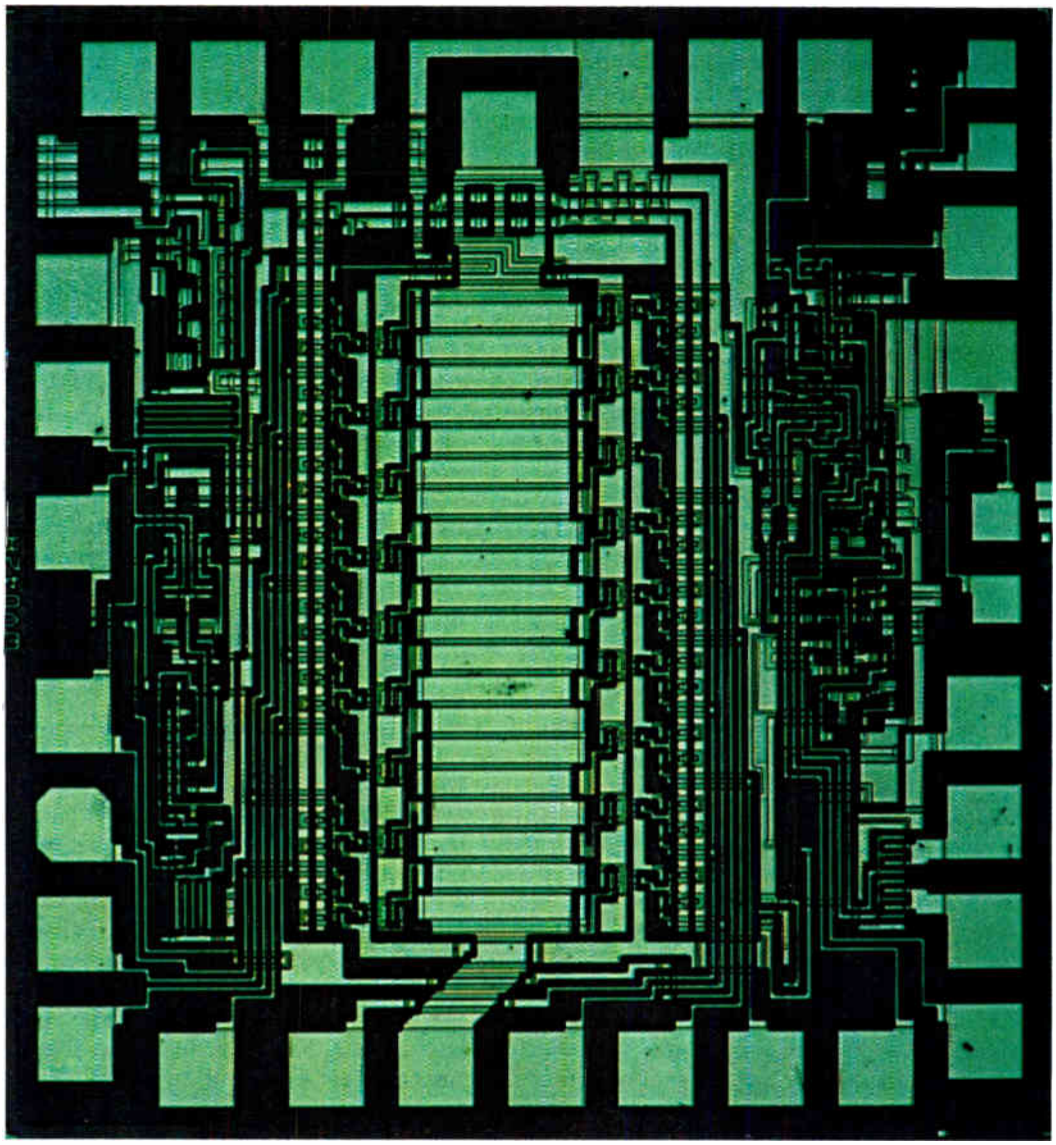
Data acquisition and conversion

A number of exciting products surface for the first time in session 1, "A-d and D-a Converters." Noteworthy for sheer speed is an 8-bit digital-to-analog converter from Plessey Research (Caswell) Ltd., Towcester, England. It has an incredible settling time of 5 ns (see Fig. 9). Intended as a building-block component for a monolithic successive-approximation 8-bit a-d 15-MHz converter, it departs from previous designs in that it contains all of the analog components needed for a video-speed feedback a-d converter: it includes not only the d-a converter, but also a precision reference, a reference amplifier, and a latched high-speed comparator with an extremely short 1.3-ns propagation delay. The d-a converter has complementary outputs and can be driven in a current-multiplying mode with a 3-decibel bandwidth of 40 MHz.

The first paper from National Semiconductor Corp., Santa Clara, Calif., concerns a monolithic 12-bit (plus sign) successive-approximation analog-to-digital converter. All monolithic 12-bit a-d converters to date have been of the slower integrating types because the successive-approximation type is limited by the comparator's poor performance—its low accuracy, slow response, and noise. National's designers, however, made their a-d converter a practical successive-approximation unit by the use of a multiple-input comparator that allows an arbitrary number of differential input voltages. Their C-MOS device has a conversion speed of 50 microseconds and power dissipation of just 25 mW. Unique to the National design is its trimming: an on-chip PROM is laser-programmed. Also, the device has processor input and output capabilities approaching and sometimes in excess of those for board-level data-acquisition systems (Fig. 10).

Researchers at the University of California at Berkeley present a paper on a 7-bit monolithic a-d converter that uses the time-interleaved-array technique to achieve 400-ns conversion. The technique allows for high-speed a-d conversion on a smaller die and at lower power dissipation than would normally be needed for a flash type converter circuit. Fabricated with a 10-μm-guard-banded C-MOS process, the chip packs four time-interleaved 7-bit a-d converters, timing and control logic, and an implanted MOS voltage reference into just 208 by 278 mil².

From Analog Devices Inc., Wilmington, Mass., comes a report on a monolithic bipolar d-a converter with a calibrated voltage output that eliminates the need for



9. Superfast. This tiny digital-to-analog subsystem converter chip achieves a full-scale settling time in 5 nanoseconds. The 8-bit device has a d-a converter, reference source and amplifier and a latched 1.3-ns comparator. Its dimensions are 67 by 71 mils.

conventional power-supply voltage trimming. The 8-bit unit uses I^2L data latches and is microprocessor-bus–compatible while operating from a single 5-V supply. Logic, reference, and output amplifier are all included. A pin-selection scheme even allows operation from a single 15-V supply if desired.

Session 1 also contains a paper from Catholic University, Heverlee, Belgium, on an 8-bit d-a converter with programmable ranges. The n-MOS converter chip contains an 8-bit capacitor array, an operational amplifier, and an eight-channel analog demultiplexer. Its ranges and end points are programmable, and it interfaces with microprocessor-based control systems.

Session 11 on "Data Acquisition" reports on several new integrated circuits for data-conversion circuitry. Two such components are from Harris Semiconductor Corp., Melbourne, Fla. One is a sample-and-hold IC that automatically zeroes dc errors to provide accuracies high enough for 12-bit data-acquisition systems. The IC includes all digital control circuitry and requires no external components. The other new component from Harris is a monolithic 5-V reference for use in an a-d converter. It is accurate to within ±1 least significant bit over the temperature range of −55° to +125° C. Designed for 12-bit a-d converters, the trimmed temperature-regulated reference features a temperature coefficient of 0.3 parts per million/°C, and a power-supply rejection ratio of 100 dB.

Precision Monolithics Inc. describes a latching comparator IC for 12-bit a-d applications. The Santa Clara, Calif.–based firm's device features 0.1-LSB error and 50-ns response time with 0.5-LSB overdrive. Designed for use in 12-bit successive-approximation a-d converters, the junction-isolated device is made with a standard process supplemented by two extra ion-implantation steps. Its high performance and expected low price will aid in the design of multichip hybrid a-d converters.

National Semiconductor Corp. unveils details about an instrumentation amplifier that offers 0.01% linearity error. The design eliminates most of the amplifier's secondary dc errors and significantly reduces its primary dc error sources. The absence of all the normal external components, like gain-setting resistors and trimmers, will make for a low-cost device. Input and output offset voltages and gain are trimmed internally. Performance is typified by input-voltage noise of 8 nanovolts/$Hz^{1/2}$, 2-nanoampere input bias current, 20 microvolts of input offset voltage, and 0.2 μV/°C of drift.

On a system level, engineers from Analog Devices' facility in Limerick, Ireland, talk about an 8-channel data-acquisition system that includes an eight-word dual-ported memory and direct memory access on the same chip. The C-MOS system's memory provides a microcomputer with a totally transparent a-d conversion.

More advances in linear ICs

Additional developments in analog circuit techniques are unveiled in session 15, which hosts two of the electronics community's more notable inventors, Barrie Gilbert of Analog Devices Inc., Forest Grove, Ore., and Robert Widlar, formerly with National Semiconductor Corp., Santa Clara, Calif., and now a consultant in Puerto Vallarta, Jalisco, Mexico. Gilbert explains how he achieved ±0.25% accuracy error and a 100-MHz signal bandwidth in a two-quadrant analog multiplier. Despite the fact that his design operates in a current mode, its virtual-ground inputs permit it to operate from low-level voltages. Nonlinearities caused by base-emitter voltage mismatches are eliminated by the use of laser trimming.

One of the strong advantages of FET operational amplifiers—low input bias current—is now being challenged by a new bipolar operational amplifier designed by Widlar. His design provides 100 μV of offset voltage, 1 μV/°C of drift, and only 20 picoamperes of bias current, a figure that rivals bias-current levels of FET amps. The device is called the LM-11 [*Electronics*, Nov. 8, 1979, p. 44].

Two other session 15 papers are from Japan. One is from the Toshiba Corp.'s R-D Center in Kanagawa, whose researchers talk about a volume- and frequency-response control IC for audio applications. The 16-pin dual in-line package requires no external components and contains a dual-volume channel and tone and balance controls. The device features total harmonic distortion of less than 0.2% and a signal-to-noise ratio greater than 57 dB (at a 300-V root-mean-square input level). The IC also contains a voltage-controlled filter that uses a time-constant control technique (Fig. 11).

The other Japanese report is from the Sony Corp. of Tokyo. Its researchers describe an LSI IC for servo control of video tape recorders. The device contains 3,000 I^2L gates and 350 linear elements on the same chip. Included on the chip are a pulse-width-modulated d-a converter, steady-state error-compensation circuitry, and interface circuitry for playback speed control and editing-point adjustment.

The pace of digital filter development has been nothing short of spectacular, particularly as telecommunications applications expand. Session 8, on monolithic filters, has several papers attesting to this.

Digital filters of all kinds

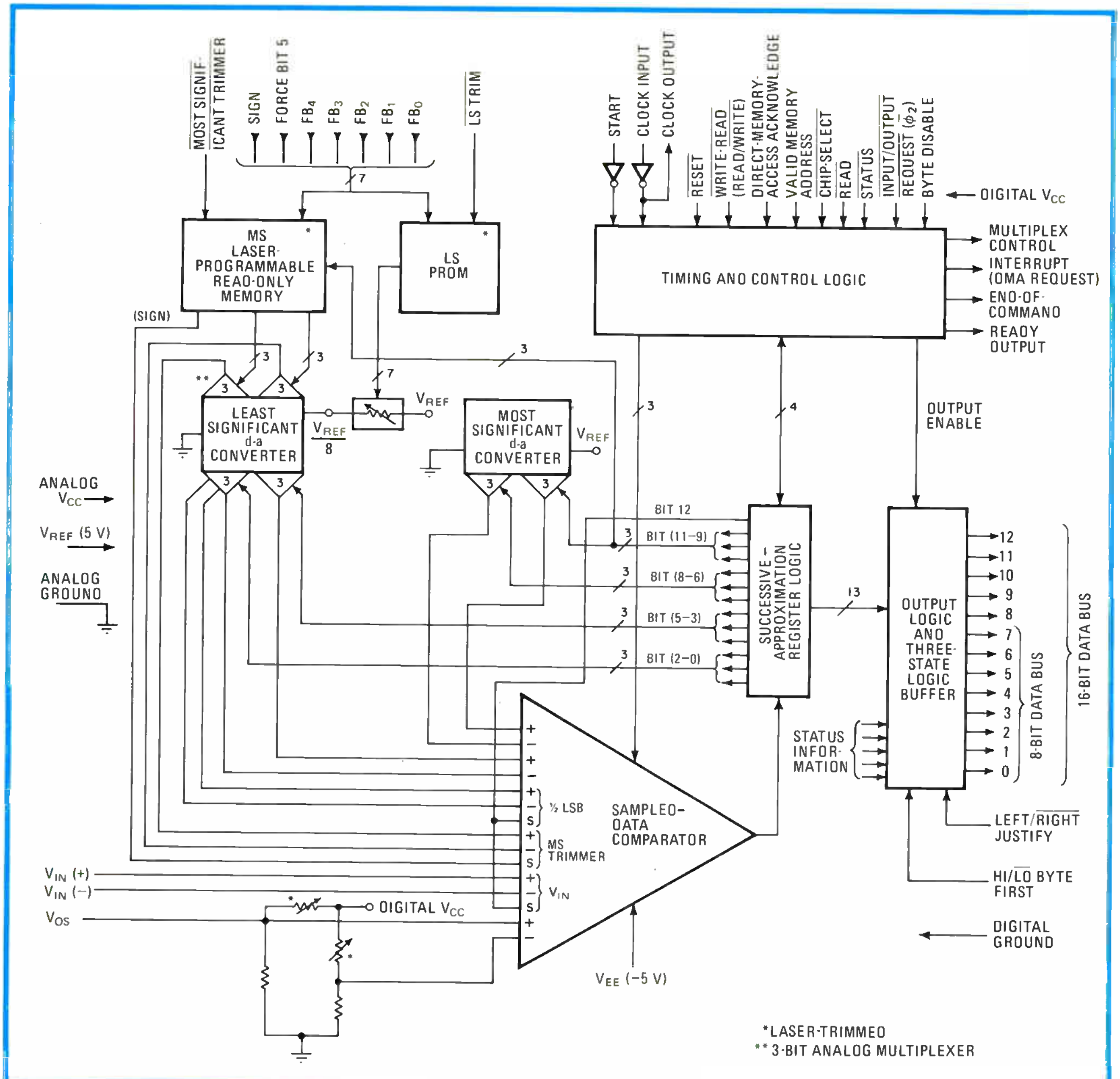
The University of California at Berkeley and National Semiconductor Corp. together present a paper on a C-MOS channel filter chip that contains transmitting and receiving functions, 50/60-Hz rejection filters, and two 600-ohm output drivers. The filters are of the switched-capacitor type. The IC was designed to operate from either a single 5-V or a 12-V power supply line. It dissipates less than 40 mW of power and overcomes two of the least desirable monolithic filter characteristics—high power dissipation and noise.

Another switched-capacitor filter comes from Texas Instruments Inc. Twenty of these multiplexed switched-capacitor filters are used in a bank configuration. The second-order filters together with two operational amplifiers fit into one 3,875-mil^2 chip.

A paper from Mitel Semiconductor, Kanata, Canada, describes a switched-capacitor bandsplit filter made with a double-polysilicon oxide-isolated C-MOS process (see Fig. 12). The single chip contains two bandpass filters, Schmitt-input comparators, and the necessary clock logic for front-end functions of a dual-tone multifrequency receiver. The process employed offers the advantages of both high speed and high density due to its C-MOS density and analog-component compatibility.

By combining state-of-the-art switched-capacitor circuits with bucket-brigade structures, researchers at EG&G Reticon, Sunnyvale, Calif., came up with an integrated real-time programmable transversal filter. The 296-by-328-mil chip contains n-MOS RAMs and multiplying d-a converters for tap-weight programming, as well as bucket-brigade-device registers for signal delay and summing. The transversal filters have one of two configurations, having either 32 symmetrical function weights or 16 asymmetrical weights. In the 32-tap symmetrical version, 32 bucket-brigade devices are pipelined in pairs with 16 multiplying d-a converters.

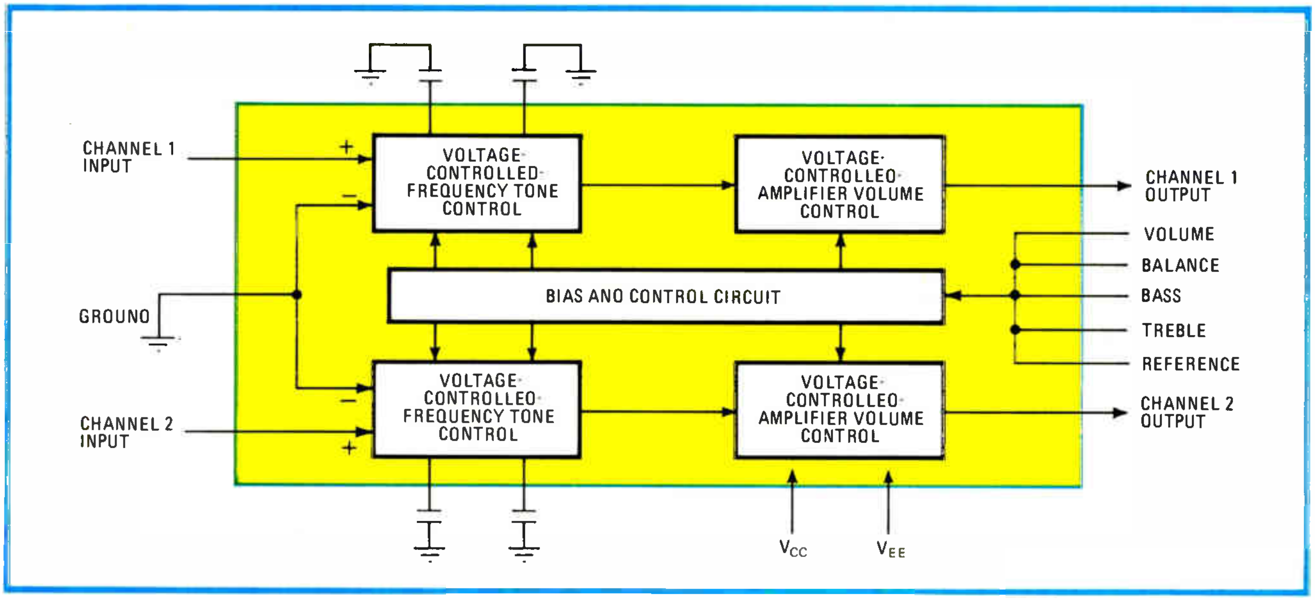
Not all filter developments are of the MOS variety. Philips Research Laboratories, Redhill, Surrey, England, has designed a bipolar gyrator video IC filter that automatically tunes a TV receiver. The 17,000-mil^2 filter chip operates up to 6 MHz, requires no tuning or alignment, has Q factors that are stable under temperature changes, and is suitable for mass production with a standard bipolar process. Resonators on the chip are simulated with gyrators terminated by junction capacitors whose voltage dependence allows for automatic tuning. The filter reportedly can be used to separate the luminance, chrominance, teletext, and sound signals in a TV receiver.



10. Successive approximation. The use of a multiple-input comparator allows the design of a monolithic 12-bit (plus sign) successive-approximation analog-to-digital converter. Two programmable read-only memories are laser-trimmed for the converter's required linearity.

Session 10 on microwave circuits includes several papers on gallium arsenide FETs. One from Hewlett-Packard Co.'s Santa Rosa, Calif., division describes a monolithic GaAs FET IC that combines several system functions on one chip. The 25.6-by-23.6-mil chip whose active area is 217 mil² and dc power dissipation is 330 mW includes an integrated oscillator, a double-balanced mixer, a phase-splitting radio frequency amplifier, and a broadband intermediate-frequency amplifier. All of these single-chip components are combined for a large part of a heterodyne signal-generation system. The chip's local oscillator frequency is 2.5 GHz and is tuned with on-chip varactors. The i-f amplifier's bandwidth is 1.5 GHz (Fig. 13).

Rockwell International Corp., Thousand Oaks, Calif., reports on how Schottky-diode FET logic was used to make multiple-level GaAs logic gates. Up to three levels of logic can be manipulated in a single gate from high-speed and low-power planar GaAs digital ICs. This work is an extension of work reported on at last year's ISSCC, in which single-logic-level GaAs logic gates with propagation delays of 75 to 150 ps and power-dissipation levels



11. Audio control. This monolithic circuit has dual-channel volume, tone, and balance controls. Housed in a 16-pin dual in-line package, it needs few external parts to operate. Its total harmonic distortion is under 0.2% and signal-to-noise ratio is over 57 decibels.

of about 100 μW were reported.

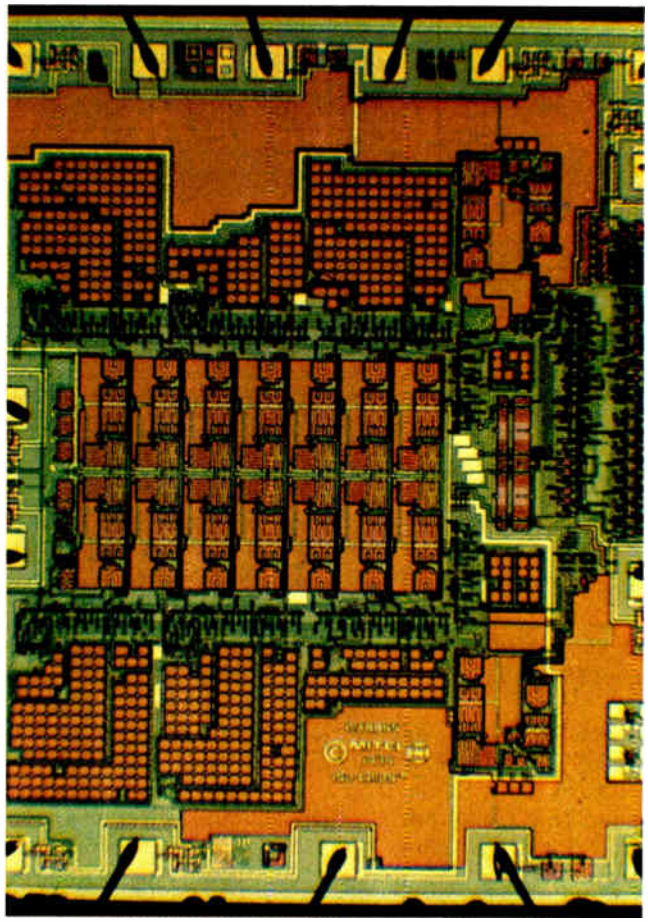
The processing side of GaAs is the subject of a paper from Westinghouse Electric Corp., Baltimore, Md. It reports on the application of direct ion implantation to unbuffered GaAs substrates for FETs and monolithic power amplifiers. The effects or processing tolerances and compensating trim adjustments on the performance of a two-stage, 1-W octave-bandwidth amplifier is analyzed.

In session 13, on GaAs FET amplifiers, the papers report on microwave system developments. Microwave Semiconductor Corp., Somerset, N. J., shows how high output power is developed from a GaAs FET amplifier at X band, through pulsed operation at high voltages. Peak output power of 10 W is managed at 8 GHz, from a device capable of providing 5 W of continuous-wave output power at a frequency of 6 GHz.

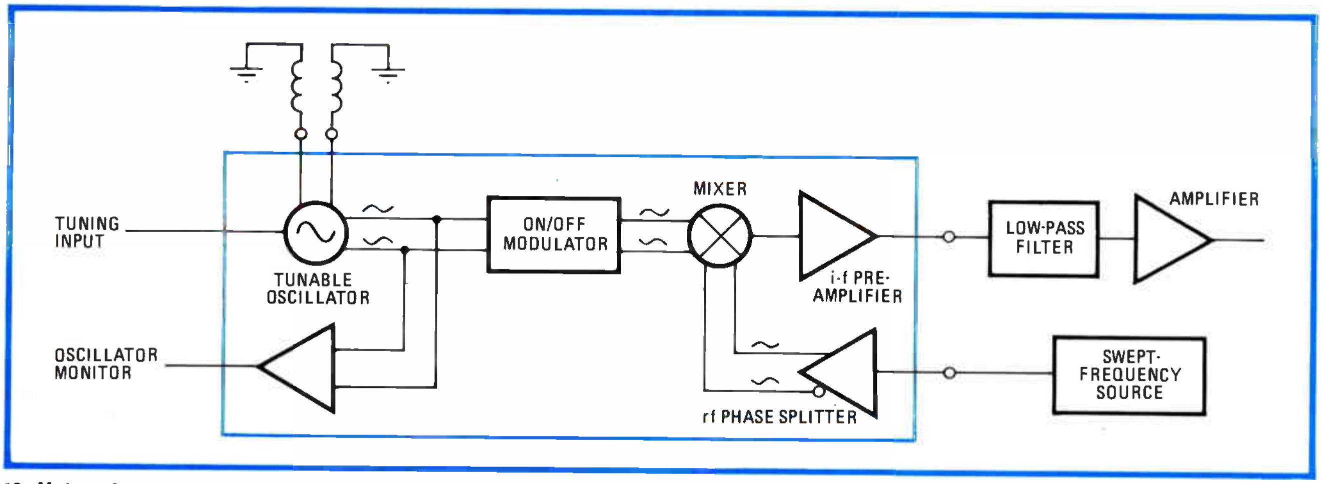
Improvement of GaAs FET gate structures has made it possible to minimize S-parameter variations from small- to large-signal operation for such devices. So reports Fujitsu Laboratories Ltd. in a paper about the large-signal dynamic behaviour of power GaAs FETs at X band. It discusses how to design a 12-GHz, 3.5-W amplifier by applying small-signal level measurements.

Another paper on a GaAs FET amplifier comes from RCA Laboratories, Princeton, N. J., and RCA Astroelectonics, Hightstown, N. J. The device is a 300-MHz instantaneous-bandwidth GaAs FET power amplifier for satellite transponders. The amplifier has 54 dB of power gain, is 38% efficient, and has 10 W of output power in the 3.7-to-4.2-GHz frequency band.

The principle of negative feedback has been recently applied successfully to a GaAs metal-semiconductor FET amplifier for ultra-broadband and low-voltage-standing-wave-ratio amplification. Now Watkins-Johnson Co.,



12. Switched capacitor. Designed to perform the front-end functions of a dual-tone multifrequency receiver, this bandsplit monolithic filter makes use of switched-capacitor techniques. It is made by Mitel's double polysilicon complementary-MOS process.



13. Heterodyne. Thanks to gallium arsenide technology, a large part of a heterodyne signal-generation system is contained on a single monolithic chip. Included are an integrated oscillator, double-balanced mixer, and phase-splitting and broadband radio-frequency amplifiers.

Palo Alto, Calif., uses both positive and negative feedback to design a single-ended GaAs MES FET amplifier that covers the frequency range of 350 MHz to 14 GHz, a 5⅓ octave band. Gain across this band is 5.2 ±1.2 dB, at an output power level of 13 dBm.

Texas Instruments Inc. of Dallas, has developed ultra-wideband medium-power GaAs MES FET amplifiers. Its designers talk about single-stage and multistage GaAs MES FET amplifiers that span the frequency range of 5 to 18 GHz. Output powers of 100 to 300 mW are reported.

Telecommuncations spawns devices

Encoder/decoder (codec), subscriber-line interface circuits (SLICs), and a variety of other components are nowadays familiar devices, thanks to the way in which telecommunications technology is opening up new areas of electronic applications. Session 14 on telecommunication circuits covers some of these new devices developments with six papers. The first, from Bell Laboratories, Murray Hill, N. J., and Naperville, Ill., reports on a 500-V monolithic bidirectional two-by-two-crosspoint array [Electronics, Jan. 31, 1980 p. 41]. The IC employs a novel gated-diode switch developed to replace the electromechanical switch normally used for the concentrator function in telephone circuits. The new IC has potential cost, size, and reliability advantages over its forerunner. It is also said to reduce the high cost of providing telephone lines with battery power, ringing, codec, and other line-interface functions.

Other researchers at the Bell Naperville facility bring out a new SLIC that offers space and energy consumption savings in telephone systems. The SLIC uses a floating power-conversion technique and provides 1,000-V isolation for low-level analog switching telephone networks.

Another line-interface circuit, this time from Bell Northern Research Inc., Palo Alto, Calif., and Ottawa, Canada, is a digital C-MOS IC that serves a number of telephone line functions. These include clock recovery, speed conversion, multiplexing of pulse-code-modulated signals, signaling, synchronization, encoding/decoding, and microprocessor interfacing.

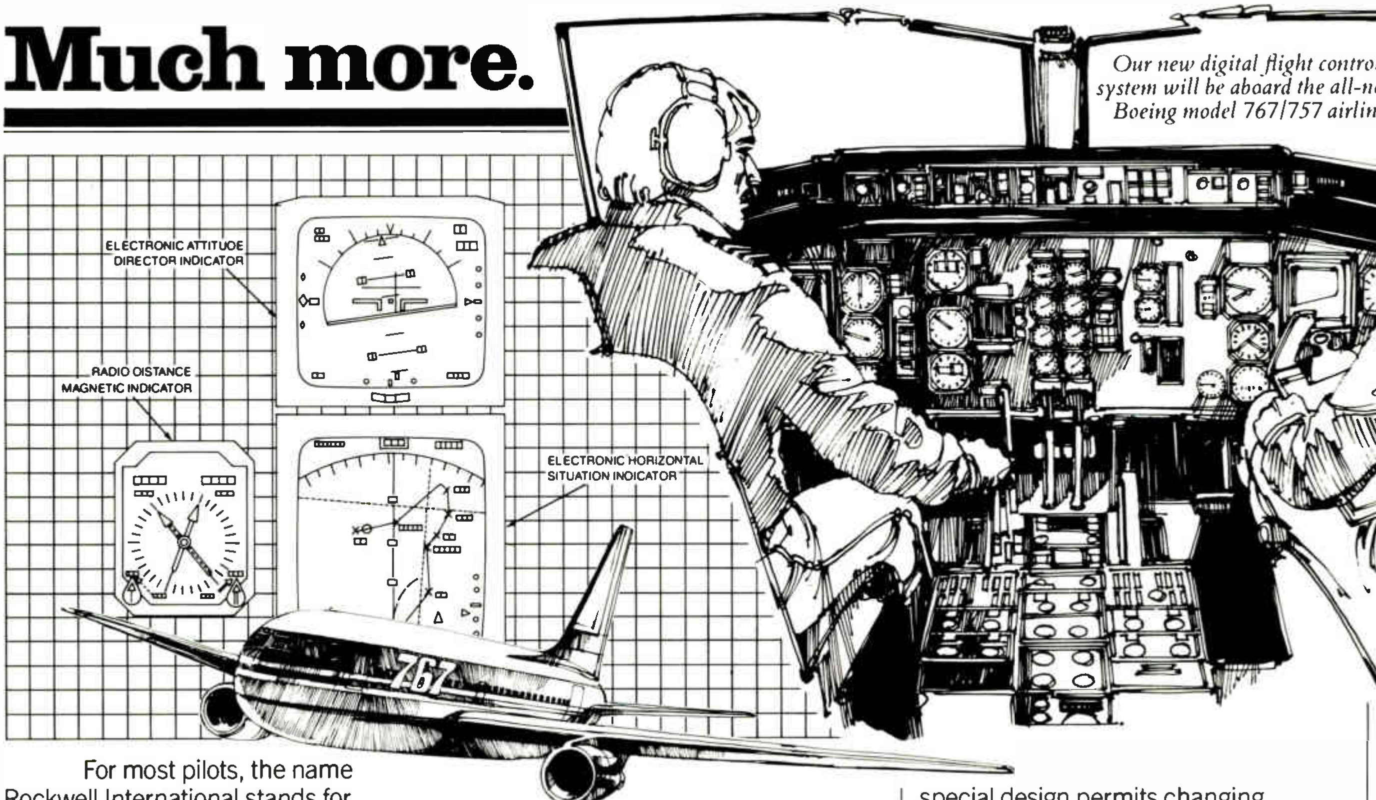
Three of session 16's papers are from Japanese organizations, an indication of the tremendous strides Japan has made in telecommunications technology developments. For example, researchers from Hitachi's Central Research Laboratory in Tokyo unveil the PCM codecs that are used with fully timed I^2L digital multiplexed filters. The single-chip codec (217.3 by 218.9 mil) is made by a phosphorus buried-emitter I^2L process and operates from 22 V and at 4 MHz. A 212.6-by-232.3-mil digital filter chip was developed through the use of conventional n-MOS technology. The chip is shared between four of the aforementioned codecs; it has an 88-dB dynamic range and operates at 12-MHz with 16-bit word lengths. A 12-bit digital compander chip, also of standard n-MOS, operates at 2.048 MHz and combines with the codec and digital filter chips to make possible a three-chip interpolative PCM codec with multiplexed digital filters for telephone-line switching.

Nippon Electric Co. of Kanagawa and the NTT Musashino Electrical Communication Laboratory have collaborated to produce a PCM codec and switched-capacitor filter system using a silicon-gate C-MOS process. Power dissipation of the codec/filter system is just 68 mW. A key factor was the reduction of the number of amplifiers, which consume most of the codec's power.

Some of the same NTT researchers and others from Fujitsu Ltd. also report on a different PCM codec. The two-chip/channel companded codec with an on-chip switched-capacitor filter includes a transmitter chip and a receiver chip and was manufactured through the use of a metal-gate C-MOS process. The two-chip approach was undertaken to minimize crosstalk where both transmission and reception functions are on one chip. The codec features typical power dissipation of 130 mW in the active mode of operation. Standby-mode power dissipation is but 15 mW. □

Rockwell International is more than a builder of avionics for most of America's airliners.

Much more.



Our new digital flight control system will be aboard the all-ne[w] Boeing model 767/757 airlin[ers.]

For most pilots, the name Rockwell International stands for aviation electronics. Understandably so: Our Collins avionics systems are not only on board nearly every U.S.-built airliner, but on many general aviation and military aircraft as well. And our Collins Air Transport Division has a contract — scheduled to extend into the next century — to build avionics for all Boeing model 767/757 airliners. But avionics is only one of our strengths.

Rockwell International is a major multi-industry company applying advanced technology to a wide range of products — in automotive, aerospace, electronics and general industries. Following are some examples of our balanced diversification.

Electronics.

(Sales, fiscal 1979: $1.5 billion.)

Our position as one of the world's leading suppliers of avionics — communications, navigation and flight control equipment — reflects only one of our electronic businesses.

We also make microelectronic systems and devices, broadcast equipment, and missile guidance and control systems. And we manufacture and install telecommunications systems, including both digital and analog microwave systems, for businesses and governments worldwide.

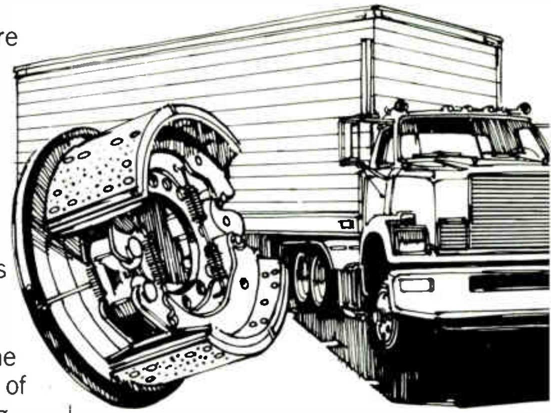
Automotive.

(Sales, fiscal 1979: $1.8 billion.)

One-half of the highway tandem tractors in North America are equipped with Rockwell axles — and more than half of the heavy-duty trucks stop with Rockwell brakes. We're also a major supplier of drivelines, steel and styled aluminum wheels, mechanical devices, castings, stainless steel wheel covers and other components for trucks, trailers, buses, vans and passenger cars.

Our Cam-Master® "Q"™ is the latest in the most widely used series of heavy-duty air brakes in the trucking industry. The "Q" is known as "the no-sweat, no-tools brake," because its special design permits changing brake shoes without tools, in less than two minutes.

Rockwell's extensive product line of mechanical, hydraulic, cam and wedge brakes is the result of over a half-century of design, engineering and manufacturing experience. Our most popular brake designs have been proved on and off the highway in literally billions of miles on the job.



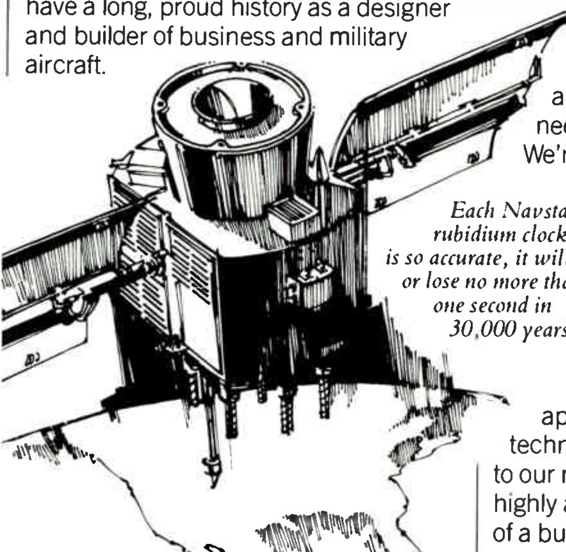
The brake shoes in this Cam-Master "Q" brake can be changed in less than two minutes – without using tools.

Also aboard is our new Electronic Flight Instrument System which displays attitude and navigation data.

Aerospace.

(Sales, fiscal 1979: $1.6 billion.)

We're prime contractor to NASA for its Space Shuttle orbiters and their main engines, and for integrating the entire Space Shuttle system including selected payloads. We build rocket engines for many other applications, too, and several types of Earth-orbiting satellites. We also have a long, proud history as a designer and builder of business and military aircraft.



Electrical power for the Navstar Global Positioning System satellites is provided by solar arrays which swivel to track and capture the sun's light.

Each Navstar's rubidium clock is so accurate, it will gain or lose no more than one second in 30,000 years.

Our current satellite projects include a new $86.1 million contract for "the brightest star in navigation history" — Navstar — designed and built by Rockwell for the U.S. Defense Department's Global Positioning System (GPS). When fully operational in the mid-1980s, GPS will utilize 24 Navstar satellites orbiting 11,000 miles above the Earth. Beaming a continuous stream of signals, the system will enable land, sea, air and space navigators to determine their positions to within 30 feet, their speed to within a fraction of a mile per hour — and the correct time to within a millionth of a second.

General Industries.

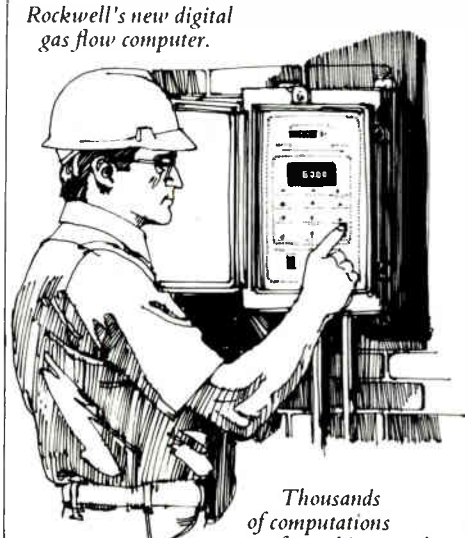
(Sales, fiscal 1979: $1.2 billion.)

Rockwell is one of the world's largest suppliers of high-technology valves for the energy market and for general industry. We also make printing presses, textile equipment, power tools, industrial sewing machines, and products for utilities, including over one-fourth of all the meters purchased by America's municipal water departments.

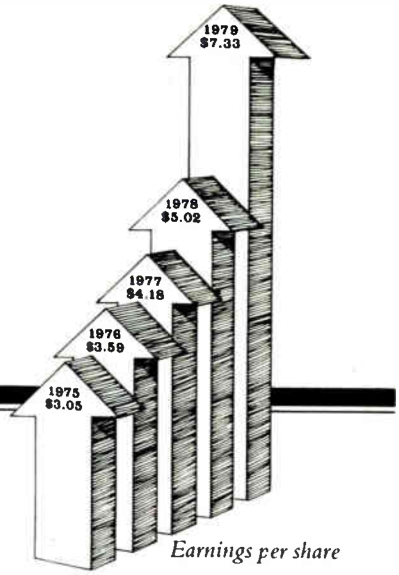
Our extensive technology is also applied to the world's growing need for alternate sources of energy. We're involved in projects for nuclear energy, coal gasification, flue gas desulfurization, and solar, wind and geothermal power.

We also manufacture gas meters for industrial applications. And our new MPG Gas Flow Computer, an application of our microelectronics technology, can be connected directly to our meters to provide extensive, highly accurate flow data at the push of a button.

Rockwell's new digital gas flow computer.



Thousands of computations are performed in seconds – continuously calculated to ten places.

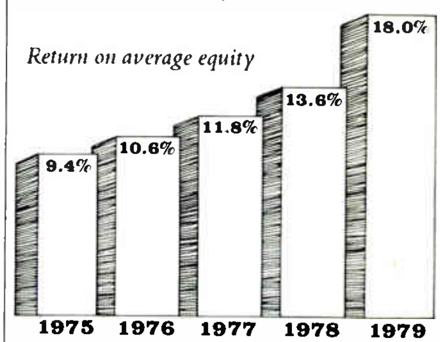


Earnings per share

Earnings up in '79 4th consecutive year.

Rockwell International's total sales for fiscal 1979 were $6.2 billion, up 16 percent over $5.3 billion in the prior year. Net income totaled $261.1 million, or $7.33 per share, an increase of 48 percent over 1978 net income of $176.6 million, or $5.02 per share. Return on average equity has increased to 18 percent, which is a substantial improvement over

Return on average equity



the previous year and nearly twice that of 1975. This should place the company among the top one-third of the 100 largest companies in the 1979 *FORTUNE 500 Directory*.

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Circle 153 on reader service card

60-watt switching power supply comes together for just $37

Off-line unit uses a single integrated control circuit in a flyback-regulator design for a minimal parts count

by R. J. Haver, *Motorola Inc., Semiconductor Group, Phoenix, Ariz.*

☐ Though more efficient, smaller, and lighter than linear power supplies, switching-regulator supplies have also cost more except for outputs of more than 100 to 200 watts. But within the last two years or so their price per output watt has dropped far enough to make them attractive even under 100 W.

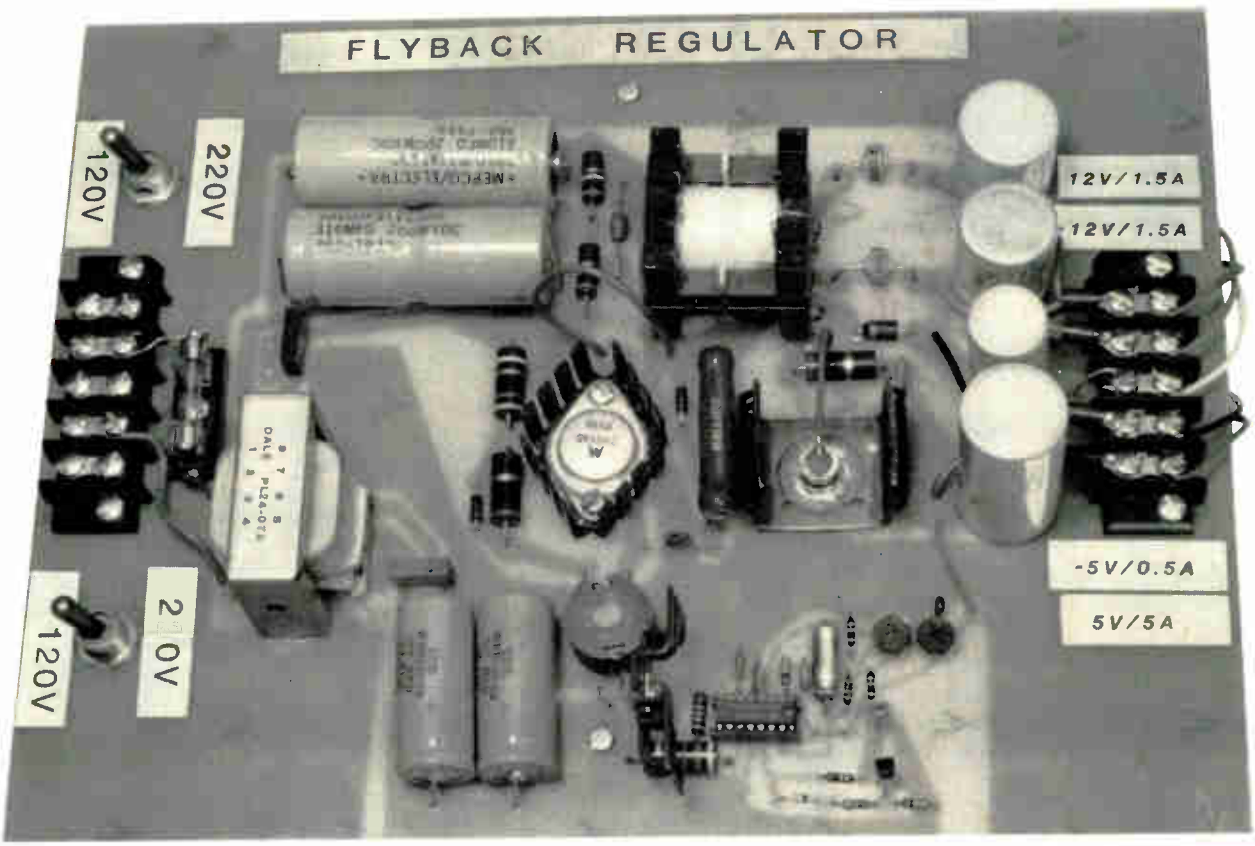
Control and protection integrated circuits as well as transformer designs have advanced so rapidly that, for instance, a 60-W switching supply, operating off line from 120 or 220 volts ac and providing outputs of ±5 and ±12 V, can be constructed with parts worth a mere $37. Yet it performs admirably (Fig. 1).

A flyback-regulator circuit (Figs. 2 and 3) with a single drive transistor needs only a few main parts:

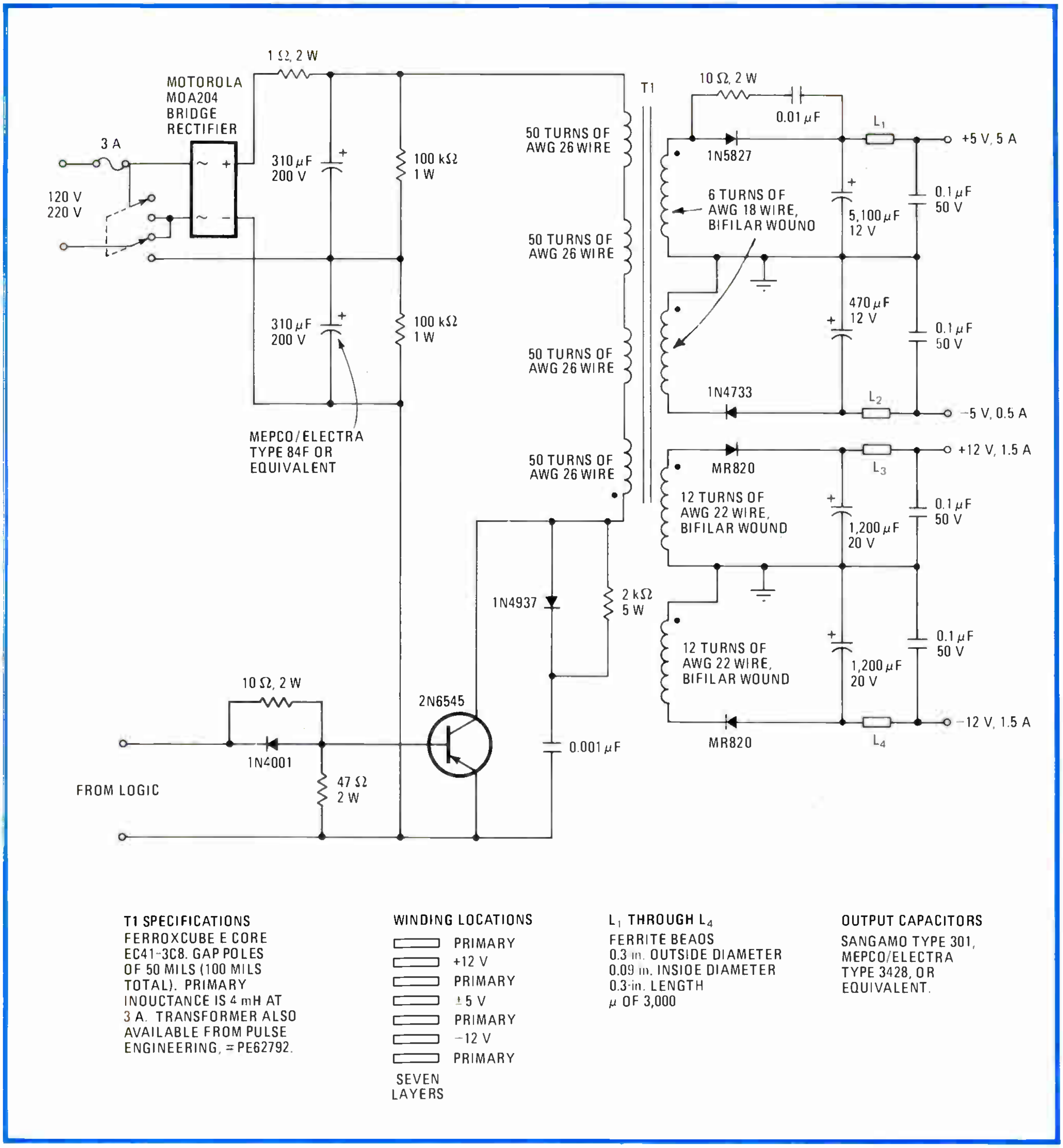
- A unique flyback transformer.
- A single control IC.
- A rapid-switching high-voltage transistor.
- Single output filters in each of the four outputs.
- The flyback base-drive circuit.
- Ac-line input voltage doublers.

Sandwiching the windings

The flyback transformer uses an EC-41 ferrite core made by the Ferroxcube Corp., Saugerties, N. Y. It has a 40:1 turns ratio and is wound by a sandwich technique that improves the coupling between its primary and secondary windings. It can also be purchased from Pulse Engineering Inc., San Diego, Calif. (part no. PE62792).



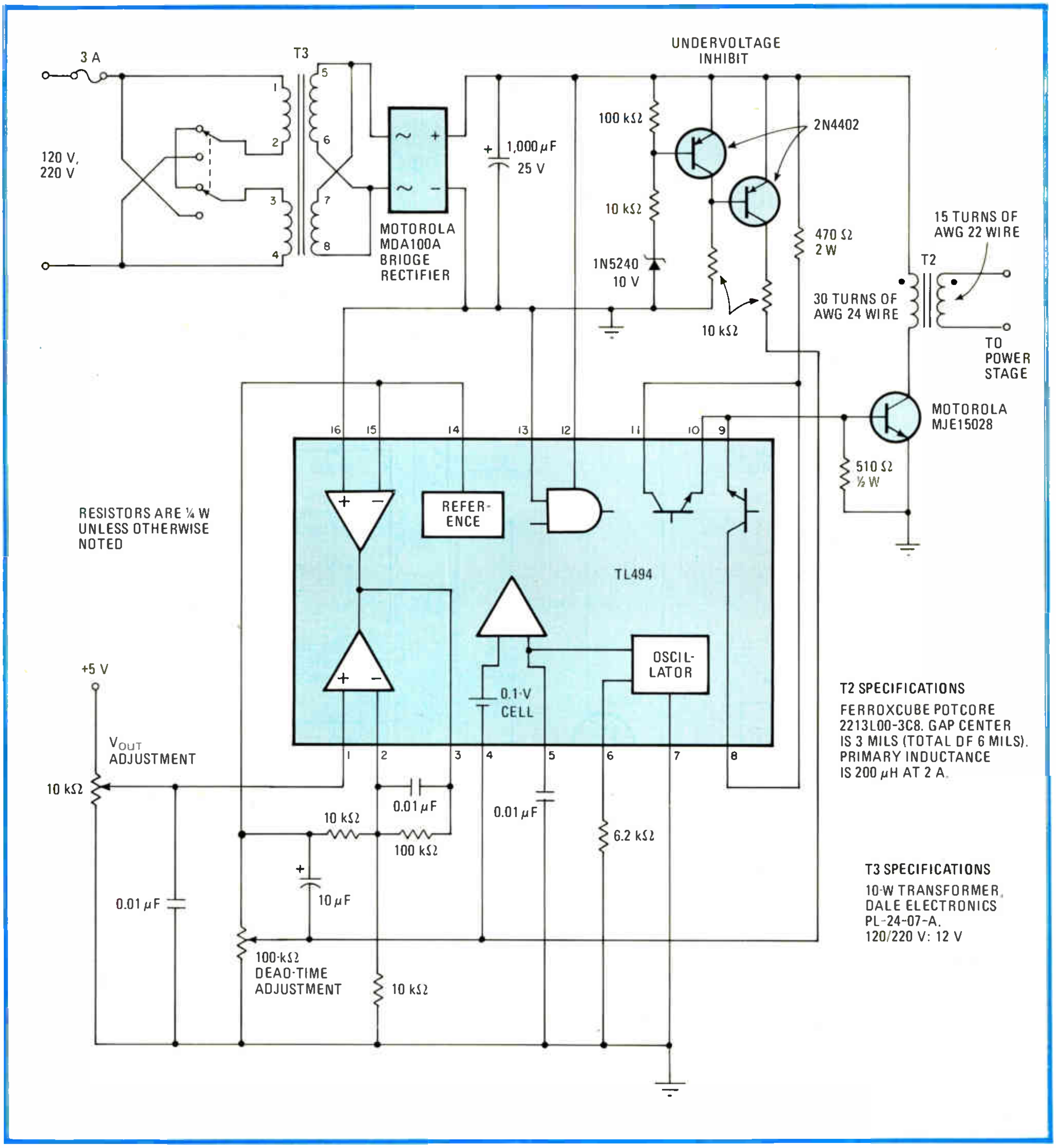
1. Compact switcher. This tiny 60-watt switching power supply is built from a design that requires only $36.99 worth of assorted components (in 1,000-unit lots). The off-line unit makes use of a single control integrated circuit and a flyback-regulator switching scheme.



2. Power stage. A flyback regulator transformer employing a single drive transistor is used for switching. The transistor, Motorola type 2N6545, is capable of switching 1 ampere of current in 40 nanoseconds and of blocking voltages of up to 800 volts.

The primary winding consists of four split windings in series with each other. The four windings of the secondary alternate in a sandwich construction with the four primary windings. Total core gap is 100 mils, and primary-winding inductance is 4.5 millihenries at 2.5 amperes. Transformer performance can be gauged from the fact that although the output current ratings for the secondary transformer windings are specified as 5, 1.5, and 0.5 A for 5, ±12, and −5 V, respectively, actual respective current values are 8, 3 and 4 A (Fig. 4).

All of the power-supply control functions reside in a single IC, the TL494. Available from both Texas Instruments Inc. and Motorola Inc., it requires a minimum of external resistor and capacitor components. It includes a 20-kilohertz oscillator, a dead-time adjustment (50% maximum) for preventing transformer saturation, two error amplifiers to process both current and voltage feedback signals, and an output stage that produces 400-milliampere pulses to drive the power transistor. An undervoltage-inhibiting circuit is added externally to the



3. Control stage. All of the power supply's control functions are obtained from the Texas Instruments' TL494 IC, which is also available from Motorola. Besides minimizing the number of control components, the IC also minimizes the number of external parts.

control IC. Consisting of two transistors and a zener diode, it inhibits output pulses when the drive voltage is less than 10 V.

For rapid switching, a Motorola type 2N6545 transistor is used. It is capable of switching 2 A in just 40 nanoseconds and can block up to 800 V under worst-case conditions. Because of the transistor's high speed, losses due to the snubber (the RC network in the collector circuit) are low—typically 2 W, or less than 2% of the total delivered power.

Each of the four output stages employs one filter capacitor and one diode. The capacitors (series 301 from Sangamo, 3428 from Mepco/Electra, or UPT from Cornell-Dubilier), exhibit low equivalent series resistance, typically 10 to 100 milliohms. Noise spikes are reduced dramatically (by as much as a factor of four) by the addition of a ferrite bead and ceramic capacitor across each of the output filter capacitors. Ripple test data for various types of capacitors is shown in Table 1.

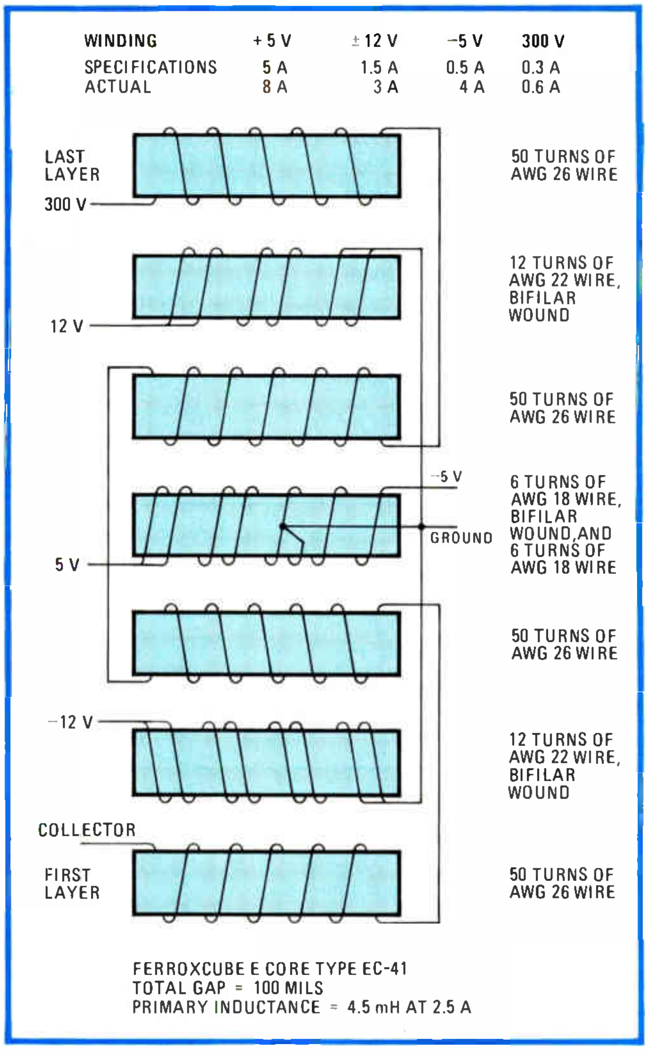
The use of a flyback transformer for base drive greatly simplifies the drive circuit. Besides the transformer, only three other components are employed: a drive transistor capable of handling 2 A, a resistor, and a diode. The flyback transformer turns on the transistor with a 5-V drive pulse while simultaneously storing the energy from the 2-A current drawn by the transistor. This stored energy becomes the reverse bias drive when the pulse from the transformer is terminated. The reverse bias drive removes stored charge quickly—within 2 microseconds—and then causes the transistor's base to avalanche for the short while it takes to reset the transformer. Typically, if the transistor was initially turned on for 20 μs with a 5-V pulse, a 10-μs 10-V pulse is needed to reset it after it has been turned off.

At the ac line input, two axial-lead 310-microfarad 200-V capacitors (Mepco/Electra series 84F) are connected in series with each other across the bridge rectifier output, thus acting as a voltage doubler when operating from 200 to 400 V. A nominal 320-V bus is thus provided across the transformer's primary winding, regardless of whether it operates from a 120-V or a 220-V ac line input.

Why flyback

One of the most popular switching-regulator power supply circuits for low-wattage supplies is the forward converter. Its transformer, having only a 15:1 ratio of primary to secondary turns, is simpler than the flyback type approach, but requires four expensive filtering chokes. In addition, its secondary windings are unregulated, so its output voltages vary with line and load variations more than they need do in the case of a flyback transformer.

A flyback transformer with a control IC placed at the secondary windings (as is done here) has a number of advantages. Feedback signals can be coupled directly to the transformer. Also, current-limiting protection on any or all of the output windings is simplified. Since the control IC has an extra amplifier, the addition of a single sense resistor to the high-current 5-V output makes it



4. Transformer. The flyback transformer can be hand-wound over an EC-41 ferrite core obtainable from Ferroxcube Corp. The four secondary windings alternate in a sandwich construction with four split primary windings that are connected in series with each other.

TABLE 1: RIPPLE TEST DATA FOR VARIOUS CAPACITORS

Output	Test	Sangamo 301	Mepco/Electra 3428	CDE UPT	Mallory VPR	Sprague 432D
+5 V	Capacitance/volts	5,100 μF, 12 V	800 μF, 7.5 V	5,000 μF, 12 V	5,300 μF, 20 V	5,600 μF, 10 V
	Ripple (P-P)	200 mV	360 mV	170 mV	250 mV	200 mV
	Spikes (P-P)	660 mV	640 mV	980 mV	880 mV	580 mV
	Cost	$1.70	$1.58	$1.95	$1.70	$4.69
+12 V	Capacitance/volts	1,200 μF, 20 V	1,400 μF, 20 V	1,000 μF, 20 V	1,200 μF, 12 V	1,200 μF, 20 V
	Ripple	210 mV	260 mV	200 mV	200 mV	n.a.
	Spikes	740 mV	1,100 mV	1,800 mV	1,440 mV	n.a.
	Cost	$1.43	$1.41	$1.95	$0.45	$4.24
−5 V	Capacitance/volts	470 μF, 12 V	2,100 μF, 10 V	680 μF, 12 V	1,200 μF, 12 V	560 μF, 40 V
	Ripple	160 mV	160 mV	180 mV	140 mV	180 mV
	Spikes	540 mV	1,300 mV	680 mV	360 mV	440 mV
	Cost	$1.27	$1.41	$0.53	$0.45	$4.24

TABLE 2: PARTS LIST FOR $37 SWITCHING-REGULATOR POWER SUPPLY			
Semiconductors (all Motorola)			Cost ($)*
Transistors	2N6545		2.50
	MJE15028		0.98
Rectifiers	MDA100A		0.78
	MDA204		0.96
	1N5827		3.58
	MR820(2)		2.50
	1N4933		0.19
Control IC	TL494		2.00
Other	2N4402(2)		0.36
	1N5240		0.27
	1N4001		0.10
	1N4937		0.30
		subtotal =	14.52
Capacitors			
Sangamo Series 301			
	5,100 μF, 12 V		1.71
	1,200 μF, 20 V (2)		2.86
	470 μF, 12 V		1.27
Mepco/Electra Series 84F			
	300 μF, 200 V (2)		2.56
		subtotal =	8.40
Transformers			
Ferroxcube type EC41-3C8			5.55
Ferroxcube type 2213L00-3C8			2.35
(Core plus bobbin equal 20% of cost)			
Dale type PL-24-07-A			3.17
		subtotal =	11.07
Miscellaneous			
Beads, resistors and fuses			
		subtotal =	3.00
		Total =	36.99

*based on 1,000-unit prices of September 1979

easy to protect that output against short circuits. The addition of three more sense resistors and a quad operational amplifier makes it a simple matter to protect all four outputs against short circuits.

This approach breaks with convention. Other switching-regulator schemes place the control IC at the primary side of the transformer, where the transistor emitter current is sensed for overcurrent protection. Optocouplers then have to be inserted in the feedback loop for proper isolation, but even so do not fully protect the supply against short circuits. Moreover, optocouplers drift with increasing temperatures.

The bottom line

The final determining factor is the bottom-line cost. In quantities of 1,000, the semiconductor parts for this flyback regulator power supply cost $15; the capacitors, $8; the transformers, $1; and miscellaneous parts, $2; for a total cost of $37. (see Table 2).

The power supply's design, which consumed about three man-months of labor, was done in three phases—first the output power stage, then the control logic, and finally the input ac power stage.

The output power stage was checked out by using a pulse generator to energize the drive transistor and transformer and subsequently calculating the snubber values. To improve coupling and reduce the 13-by-14-V nominal output to 12 V, the 5-V secondary winding was increased from an initial five turns to six.

Adding control logic involved designing the base drive transformer and finding values for the feedback network that would provide optimum performance without creating instability. An operational amplifier gain of 20 with a rolloff at 1 millisecond proved sufficient. A dead-time limit of 50% keeps the drive transformer from saturation without interfering with low-line-voltage performance. An undervoltage-inhibiting circuit was added to keep the control circuit from misbehaving at voltages under 10 V (6 to 9 V). Otherwise, the control circuit became incapable of providing adequate drive voltages and excessive output pulse widths resulted.

The first power transformer selected was a 7-W unit, which provided regulation so poor that it confused the undervoltage circuit. Substituting a 10-W version solved that problem. Later on, it was discovered that the 3-A input fuse was failing because of inrush currents. The problem was traced to the 470-μF, 300-V input filter capacitors. These were changed to 300-μF, 200-V units and a 1-ohm inrush-current–limiting resistor was added. The ac ripple voltage rose as a result, but not intolerably, being only 10 V peak to peak at full load.

Impressive results

Despite the power supply's low parts count and simplicity of design, it has an impressive level of performance. For a nominal input of 120 V, it maintains regulation over an input range of 90 to 140 V and load range of 2:1 (half load to full load). For example, line and load regulation for the 5-V output are 2.5% and 1%, respectively. At an input of 90 V ac, full-load output voltages are 4.848, −4.930, −12.78 and 12.68 V, respectively, for the 5, −5, −12 and 12-V outputs. At 120 V ac, full-load output voltages are 5.001, −4.977, −12.98 and 12.94 V. At 140 V, full-load voltages are 5.983, −5.061, −13.16 and 13.10 V.

Half-load regulation is equally impressive. At a 90-V ac input, output voltages are 5.040, −5.075, −13.13 and 13.07 V. At a 120-V input, they are 5.098, −5.162, −13.30 and 13.20 V. At a 140-V input, they are 5.114, −5.191, −13.35, and 13.28 V.

Should it become necessary to work over a wider load range, such as from full to no load, the power transformer would have to be redesigned to protect the drive transistor from load dump conditions. This can be done by increasing the transformer's core size from the present EC-41 to EC-52 and by adding a primary bifilar winding coupled through a diode to the dc bus.

The power supply is also very efficient. At 120 V ac in and a full-load condition, its efficiency was an impressive 89%. The only noticeable heat rise is in the small components like the snubber resistor and Schottky diode. All other components remain cool to the touch. □

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		55°C		25°C	25°C	25°C		INCHES
	VOLTS	MA Air	MA Oil	AMPS	μA	MA	VOLTS	
SCHC5000	5000	500	1000	50	2	500	6	1.13
SCHC10000	10000	300	600	35	2	300	12	1.13
SCHC20000	20000	250	500	35	2	250	24	2.01
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SCFC5000	5000	500	1000	50	2	500	6	1.13
SCFC10000	10000	300	600	35	2	300	12	1.18
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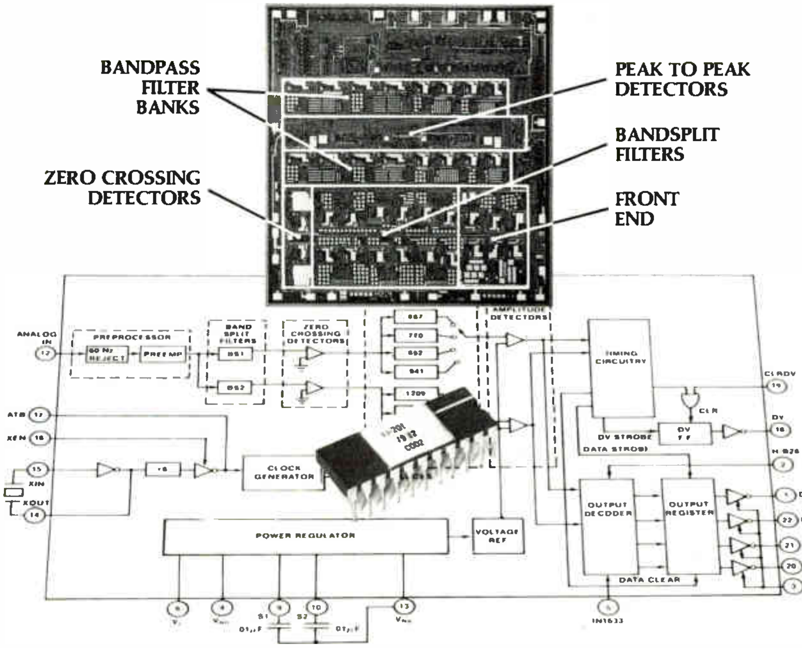

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Taking the heat off semiconductor temperature testing

Probes make measurements easy, but for accuracy the user must understand the thermal characteristics of sensors and devices

by William Mark, *Tektronix Inc., Beaverton, Ore.*

☐ As electronic products grow smaller and are therefore less able to dissipate heat, design engineers and service people grow more concerned about operating temperatures. They realize that proper thermal performance improves reliability and increases customer satisfaction.

As a result, the inexpensive, easy-to-use hand-held temperature probe for use with digital multimeters is fast becoming a common sight in the field and at the test bench. But in the hands of the uninformed user, the ease and convenience of this tool can lead to typical errors of 25°C or more. To reduce these errors to acceptable levels requires an understanding of probe design and use.

Temperature measurements of electronic components are typically made for one of two reasons: to determine the temperature rise where thermal calculations would be very cumbersome and complicated or to confirm thermal design calculations already made. Before convenient temperature probes became available, temperature measurements were usually taken with thermocouples, heat sensitive stick-on tabs, or—as some might admit—the thumb or finger.

The introduction by Tektronix of hand-held probes that could be used with digital meters made it easier to measure temperature. For one thing, digital readout provided more resolution than was available from the heat-sensitive paper of thermal tabs. Further, it was no longer necessary to wait for the glue to dry to hold the thermocouples in place, so that temperature measurements could be taken at a moment's notice wherever the probe could reach.

Unfortunately, because the temperature probes appear similar to electrical ones, many users made assumptions that led to frustrating results. Whereas taking a dc voltage measurement with a test probe is a "goof-proof" procedure in most applications, a seemingly similar temperature measurement can produce gross errors unless the probe's characteristics and capabilities are considered.

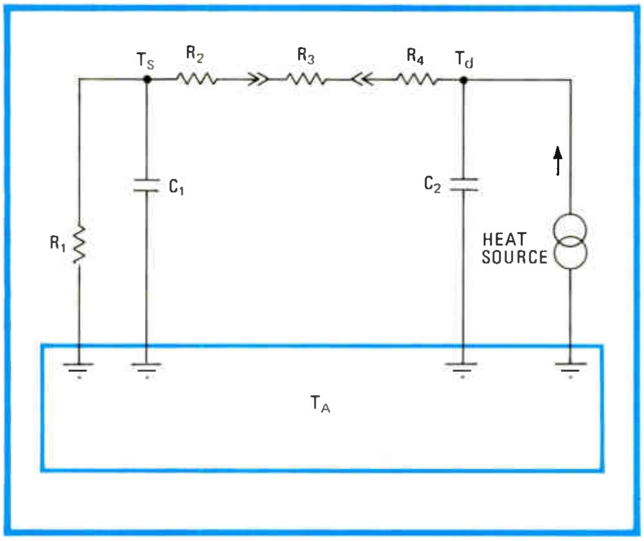
Error sources

Sources of temperature measurement error can be sorted into two groups: those associated with the intrinsic characteristics of the probe and those associated with its dynamic thermal characteristics. The intrinsic errors depend upon the nature of the heat sensor and the signal-conditioning circuitry and are usually the only factors taken into account in the published accuracy of the probe. However, the published accuracy is achieved only when there are no thermal gradients within the probe—that is, when it is totally immersed in the measured medium, be it liquid or gas. For contact measurement of solids, such as with electronics, that second error source must be considered, too.

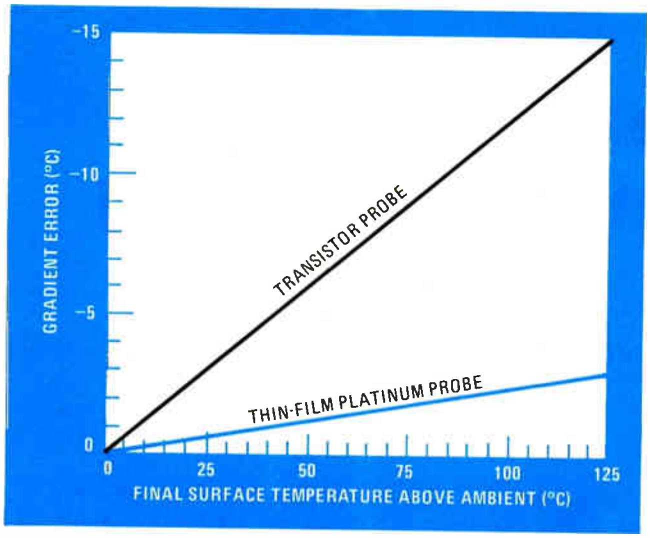
Thermal characteristics

Three basic temperature sensor characteristics become apparent when errors of contact temperature measurements are analyzed. These are the thermal resistance, the thermal mass, and the thermal time constant of the total sensor and the device being measured. Though the thermal characteristics of the device being measured cannot be changed, their effects can be minimized by selecting a proper sensor and by knowing the characteristics of that sensor.

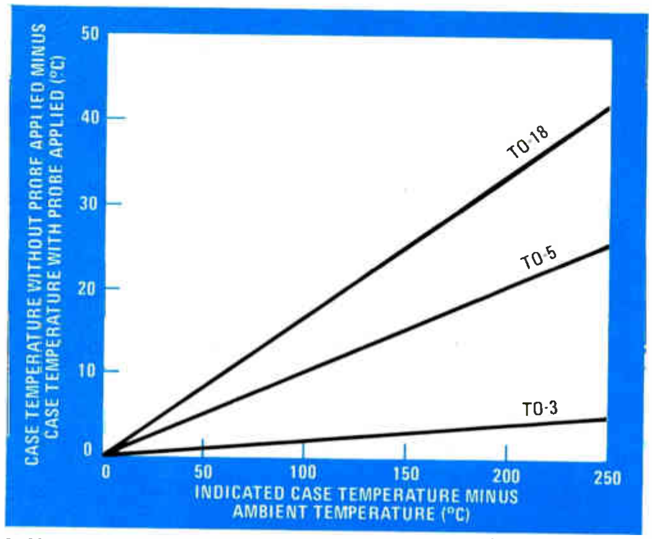
These three characteristics are common to all temperature probes. Unfortunately, information describing them is not handled very well, if at all, by most vendors. Advertisements, data sheets, and manuals seldom describe adequately the nature and magnitude of these



1. Heat à la Thévenin. An electrical equivalent for the heat flow during a temperature measurement, the circuit is divided in two by R_3, the thermal resistance from the contact between the probe (represented on the left) and the device under test (right).



2. Gradient error. To keep the thermal gradient error low, heat must remain at the sensor during measurement. To do this, the thermal resistance of the sensor tip must be low with respect to that of the probe, as is the case with thin-film platinum probes.



3. Heat sink. Charts like the one above that show the temperature probe's heat-sinking effect on various-sized transistor cases give some idea of the probe's thermal mass. That parameter depends on probe size, shape, and composition and is hard to quantify.

effects. Improvements are needed not only in sensor characteristics but also in the way they are described.

The first of these characteristics, thermal resistance, leads to what can be called the thermal gradient error. Thermal resistance causes the temperature of the sensor itself to be somewhere between the temperature of the device being measured and the ambient temperature. And all any instrument ever really displays is the temperature of the sensor itself.

Figure 1 shows an electrical analog of thermal effects for a temperature probe and a device being measured. Thermal resistors R_1, R_2, R_3, and R_4 form a temperature attenuator. The displayed temperature, T_S, is therefore equal to:

$$[R_1(T_D - T_A)/(R_1 + R_2 + R_3 + R_4)] + T_A$$

where T_D is the internal temperature of the device being measured and T_A is the ambient temperature. R_4 is the thermal resistance of the device being measured and thus cannot be changed. R_3 is the thermal resistance at the contact point between the sensor and device, R_2 is that of the sensor and probe tip, and R_1 is that between the sensor and the ambient temperature.

A spherical tip on the sensor helps make contact resistance R_3 less than when a flat tip is used. That is because no surface is perfectly flat. There will always be an air gap between the two parts, but when a flat tip must be used, contact resistance can sometimes be reduced by the use of a thermally conductive grease. The probe manufacturer can minimize the thermal resistance of the sensor tip, R_2, by proper construction.

The thermal resistance from the sensor to ambient air, R_1, is generally due to the probe material behind the sensor tip, and therefore it must have as high a thermal resistance as possible. This error component also includes the contribution of leads running from the signal-conditioning circuitry to the sensor. Since electrical conductors also tend to be thermal conductors, leads can be a dominant part of R_1.

Thermal-gradient errors of up to 25% of the difference between ambient temperature and device temperature have been measured on some types of sensors. Figure 2 shows typical thermal gradient errors for a transistor sensor and for a thin-film platinum sensor. The difference in these errors is due both to the material of which the sensors are made and to their packaging. Very few vendors give this information.

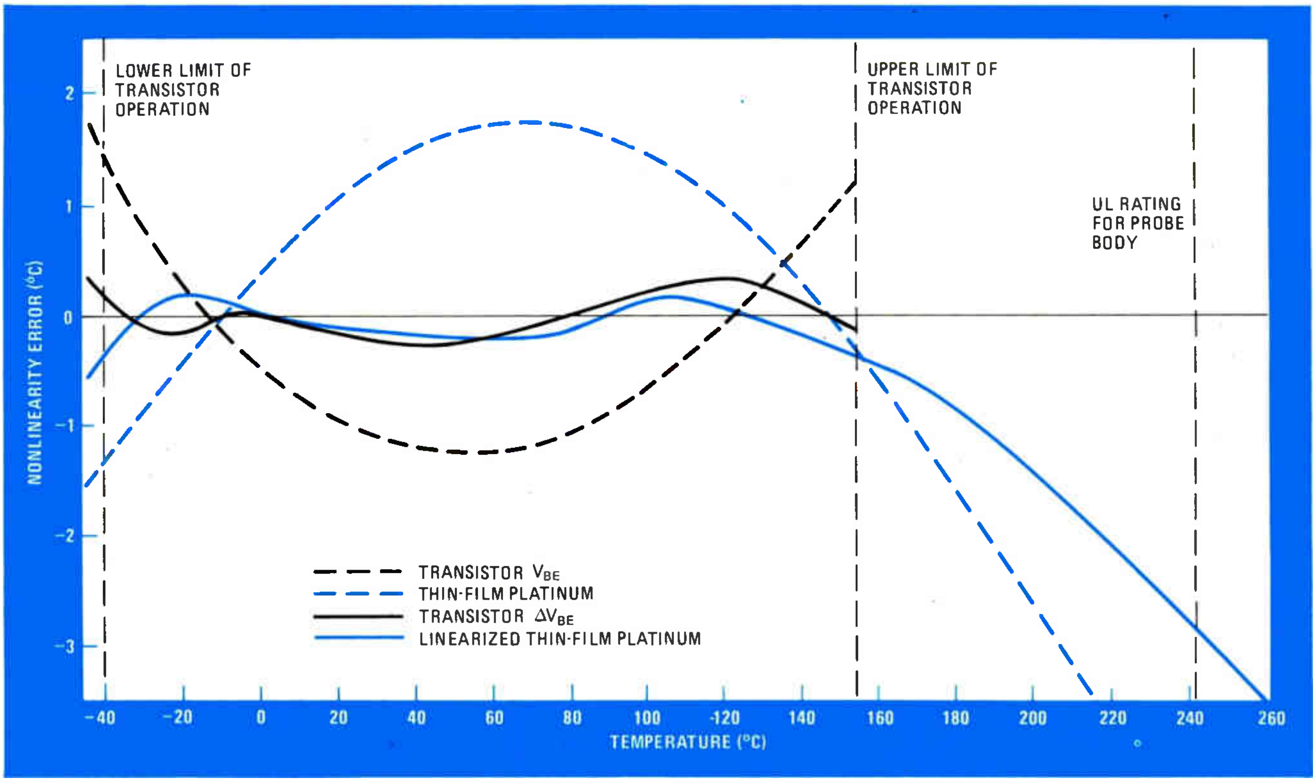
Thermal mass

The loading due to thermal mass, or simply the heat-sinking error, must also be considered for component measurements. If the thermal mass of the probe approaches that of the device being measured (C_1 and C_2, respectively, in Fig. 1), a large error is generated. This error is much more difficult to specify in a quantitative sense. Figure 3 gives a good indication of the relative heat-sinking error when the temperature of known components such as common transistor cases is measured. Although these curves vary from one temperature probe type to another and, to a lesser extent, from one device to another, they are much better than no information. A reduction in the mass of the sensor tip and probe body will reduce the heat-sinking errors but must be traded off against the need for probe ruggedness.

The thermal time constant of the material used to fabricate the probe may be anywhere from milliseconds to tens of seconds or greater. The amount of time the probe is held in position determines the magnitude of this error component. Besides reducing steady-state error, a low thermal time constant also improves the ability to follow rapidly changing temperature.

Other characteristics needing attention in selecting temperature probes fall mainly in the areas of safety, convenience, and type of use. Questions that have to be answered are:

- What is the maximum allowable voltage on the device whose temperature is being measured, and does the probe tip or body conduct current? No one wants to use



4. Useful range. Whereas the useful range of a transistor probe is limited by the sensor itself, the platinum film-sensor can measure temperatures way above the failure point of ordinary semiconductors. The DM502A plug-in DMM has a platinum-probe linearizing network.

a probe as a shorting bar or a welding rod while measuring temperatures in high-powered circuitry.

- Will the maximum temperature limits of the probe tip body and cable be sufficient for the needs at hand? The tip may measure temperatures up to as much as 200°C, but if the cable and handle will go only to 70°C, the probe's use is limited.
- Can the probe tip be immersed in liquids? A stirred ice bath is the most convenient and easily obtained temperature reference for checking probe accuracy.

Thermocouple, semiconductor junction, and resistance temperature sensors make up the majority of hand-held probes. Thermocouples, probably the most common of all temperature detectors in use today, have the widest temperature-measuring range available.

Thermocouples

Temperatures ranging from −250° to over +2,400°C can be measured, depending on the type of thermocouple used. Iron-Constantan, the most popular kind, is the least expensive.

But though they cover a broad range, thermocouples are the least sensitive of temperature detectors. Their outputs are low, ranging from approximately 2 microvolts/°C (platinum-rhodium) to 60 μV/°C (Chromel-Constantan) and therefore require good (low-noise, low-drift) amplification. Furthermore, the probe must include an analog or digital linearizing network to correct for the thermocouple's nonlinear output, as well as a reference (or cold) junction at the terminating ends of the thermocouple to maintain the correct output voltage. The wires used in thermocouples vary in size from less than 0.0005 inch in diameter to over 0.16 in. and are usually mounted in stainless-steel probes for protection from damaging environments such as corrosive liquids.

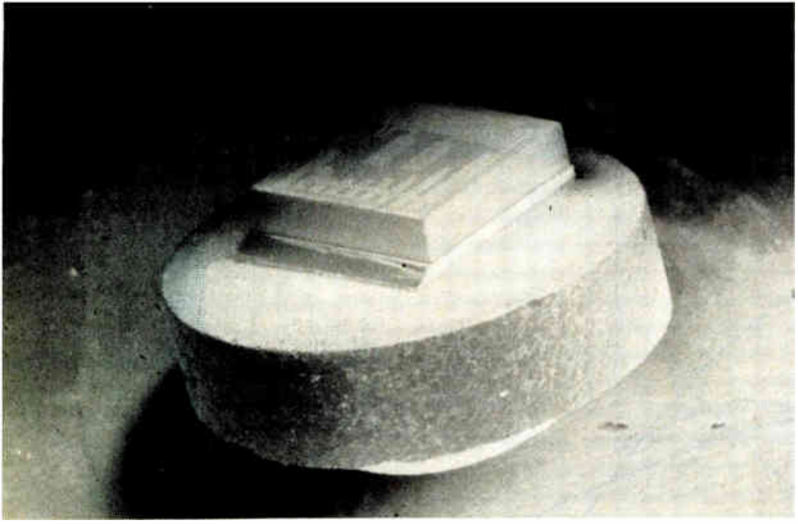
Thermocouple temperature probes are mostly used for immersive measurements and, in most cases, are difficult to use when measuring small components because they can cause large heat-sinking or thermal gradient errors. Furthermore, the wires and stainless-steel probes can be a safety hazard in the attempt to measure temperatures in operating circuits with large voltages present.

Semiconductor sensors

The design of semiconductor temperature probes, on the other hand, better suits them for checking electrical component temperatures. They generally have a nonconducting probe body; thus they can make measurements on components at elevated voltages. However, their measurement and operational temperature range is limited to approximately −50° to +150°C. The upper temperature limit is due to the leakage currents and the low-end limit is imposed by transistor gain degradation.

The transistor can be used in two different ways to measure temperature. First, the transistor may be connected as a diode (base shorted to collector). In this configuration, measurement depends on the variation of V_{BE} with temperature. The output sensitivity varies from −2 to −2.5 mV/°C. The signal conditioning required is minimal for these detectors. The diode-configured transistor is somewhat nonlinear over the temperature range given, as seen in Fig. 4.

The second way a transistor may be used as a temperature detector is by monitoring the difference in V_{BE} at



5. Tip-top. To reduce thermal resistance, the thin-film platinum sensor die is eutectically bonded to the top of a beryllium disk whose rounded bottom comes in contact with the device to be tested. This scanning micrograph shows the tip 50 times its actual size.

two different collector currents; that is, V_{BE} at I_{C1} minus V_{BE} at I_{C2}. Then $\Delta V_{BE} = (KT/q)\ln(I_{C1}/I_{C2})$. This method yields a more linear output, and interchangeability between different sensors is much improved. It needs a little more circuitry than the previous version, and it reduces sensitivity to about 0.4 mV/°C.

Probes built with thermistors and bulk-metal resistance temperature detectors rely on the variation of resistance with temperature. Unlike thermocouples, RTDs are highly sensitive to small temperature changes, do not need reference junction compensation, and produce highly accurate and repeatable measurements. Thermistors are the most sensitive of all temperature detectors—a 3% to 5% in resistance per °C is not unusual—and can therefore provide the best resolution. Specially calibrated to 0.01°C resolution over a narrow temperature span, they have been used in biomedical and chemical research. The maximum temperature range of thermistors is also from about −50° to +150°C.

However, thermistors are generally composed of a bulk-semiconductor material with nonlinear temperature characteristics and their long-term stability under temperature cycling is worse than most well-made, bulk-metal RTDs. The sensing element is generally a rather fragile, glass-encapsulated device.

Thermistor detector packaging

Most thermistor detectors are mounted in either a glass rod or a stainless-steel probe tip. The glass-rod packaging gives adequate performance with average heat-sinking errors but poor ruggedness; their thermal gradient error depends greatly on the tip design and the size of the electrical conductors leading to the thermistor itself. The stainless-steel probe body is very rugged but not at all suited for minimizing heat-sinking and thermal gradient errors.

Bulk-metal RTDs are usually constructed of pure platinum wire, although less expensive copper and nickel have been used in applications in which platinum's wider temperature range and greater stability is not needed. All RTDs have a wide temperature range, with platinum being the most sensitive and the least linear. Platinum's high sensitivity and stability, coupled with rigorous calibration procedures, have made it the most accurate of all temperature-measuring materials.

In spite of all this, bulk-metal RTDs do not make very good contact temperature probes. Their relatively large thermal mass—due to the coil of platinum wire and the protective stainless-steel, glass, or quartz sheath—produces high thermal-loading and high thermal gradient errors. The desire to reduce the errors due to the packaging of a temperature sensor and to improve its range has led to a new technology in resistance temperature sensors—the thin-film platinum resistor.

Thin-film platinum sensor

A probe developed by Tektronix uses a thin-film platinum resistance deposited on a silicon die. The die, in turn, is eutectically bonded to the top of a beryllium oxide disk whose bottom comes in contact with the surface being measured. The small mass of this configuration (Fig. 5) minimizes heat-sinking errors. Beryllium oxide, chosen for its very low thermal resistance, reduces the thermal time constant by a factor of 5 to 10 compared with available transistor probes.

A transistor could also have been used in place of the thin platinum film, but the use of platinum permits the limits of the probe's operating range to be increased to that of the packaging materials rather than of the sensor. Thus semiconductors can be measured at their temperature limits without worry that the probe will fail before the device under test.

To package the sensing tip, it is glued to an epoxy lead-frame carrier. Rather than bond the lead frame directly to the resistor, small-diameter wires are used to join the two to increase thermal resistance. This decreases the thermal gradient error by a factor of about four when compared with transistor probes.

After the sensor has been glued to the epoxy lead-frame carrier and once wire bonds are in place, the assembly undergoes a final molding operation to produce a completely immersible probe tip. The immersion characteristic allows the tip to be immersed in any liquid that does not attack the BeO tip or the epoxy probe body, and therefore it can be easily calibrated in an ice bath.

The variation with temperature of thin-film platinum resistors takes the same form as bulk-metal platinum or any pure metal, namely, $R = R_0(1+\alpha T+\beta T^2)$. The thin-film platinum coefficients α and β are somewhat different than for bulk platinum; this results in a temperature coefficient of resistance of 3,650 parts per million per/°C, versus the European standard (DIN 43 760) of 3,850 ppm/°C for pure platinum or the international practical standard of temperature of 3,925 ppm/°C. This measured difference may be caused by the strain-gage effect of the platinum resistor on the silicon die or by the little-understood effects of thin-film processing on material. Figure 4 shows the intrinsic linearity of the platinum sensor and the result with a simple, two-diode breakpoint linearization network.

Practical and effective temperature measurements can only be made with a knowledge of the error sources and magnitudes. Thin-film technology, combined with careful packaging, shows much promise in reducing errors while broadening the range of temperatures measured. □

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Interrupts call the shots in scheme using two microprocessors

Two single-board computers and five other Multibus boards divvy up control of a real-time airborne data-acquisition system

by Thomas A. Harr Jr. and Robert Phillips,
U. S. Department of Commerce,
*National Telecommunications and Information Administration,**
Institute for Telecommunication Sciences, Boulder, Colo.

☐ When a system must collect, analyze, decode, and record multichannel information at differing throughput rates, a multiple-processor approach is desirable. It allows the measurement and input/output tasks to be divided into separate functions with a resulting higher system performance.

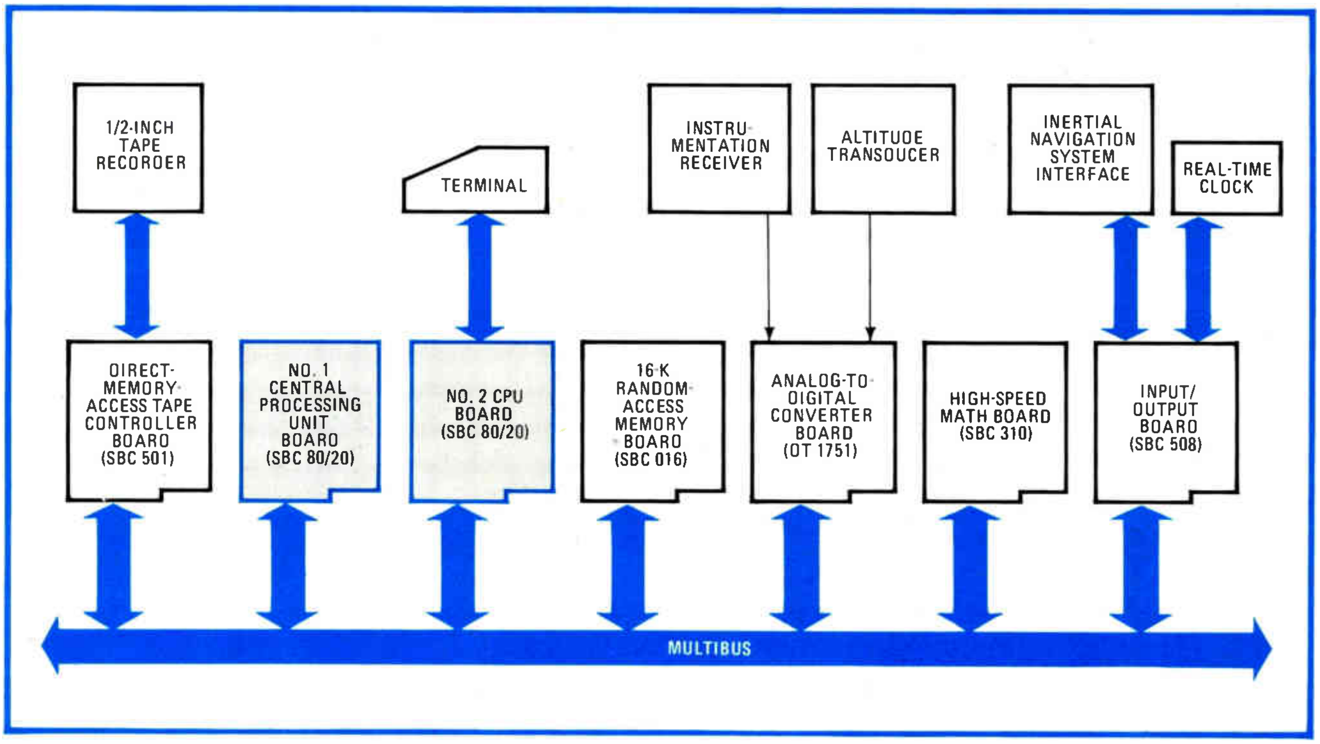
Along with this concept of task allocation comes the more important problem of communication between the processors, which can present challenging hardware and software design problems. The system examined here—an airborne measurement system—uses the microcomputer's interrupt mechanisms to advantage.

System considerations

The major constraint in any real-time processing system is that the computer must always be ready to detect and acknowledge the asynchronous events presented to it by the outside world. The requirements of the particular application may present the central processing unit with too many tasks to handle within the time available between the real-world events to be processed. Assuming that the system's task load cannot be reduced, there are two general ways to alleviate the time crunch.

The first method is to perform more of the tasks in hardware where possible—for instance, perform time delays with a programmable interval timer rather than using the CPU to decrement a set of registers. Secondly, the tasks should be partitioned in such a way as to allow multiple processors to perform them in parallel. The multiprocessor approach offers speed and flexibility, but

*Thomas Harr is now with Integrated Sciences Inc., Longmont, Colo.; Robert Phillips is an independent consultant in Boulder, Colo. The identification of commercial products in this article does not constitute a recommendation or endorsement by the Department of Commerce or the National Telecommunications and Information Administration.



Shared resources. The measurement system uses seven microcomputer boards. The 16-K RAM board is treated as a public memory area, and it is shared between the two CPU boards (the 80/20s) and the DMA/tape controller board (the 501). These three can be masters.

TABLE 1: SYSTEM TASK PARTITIONING		
Direct memory access tasks	No. 1 central processing unit tasks	No. 2 central processing unit tasks
• perform the transfer of data to tape.	• control the DMA/tape interface. • control the sampling of the receiver's analog-to-digital converter data. • control the sampling of the altitude transducer a-d converter. • input the position data (latitude, longitude, ground speed, heading) from the navigation interface. • read the real-time clock. • set up and control the math board for hardware math calculations. • provide checking for the tape, system status, and math board routines.	• perform console input and output (using Intel 80/20 system monitor). • prompt the operator for pertinent measurement and system control information, enter it, and store it in memory. • print statistics and status message on the console, providing code conversion and output formatting when necessary. • perform error checking on operator input data. • provide access to system test routines.

introduces the complex problems of data and control integrity when the processors must communicate with each other or share system facilities such as the system bus or common memory or I/O.

The response time and throughput of the system is also dependent upon the method used to respond to requests for service. The commonest methods used in microprocessor systems are polling and interrupts.

In the polled mode the CPU periodically checks the status of a control line or latch or the value of a memory or input byte to determine if an event has occurred that must be acknowledged. This mode of operation ensures that the event will be detected and serviced in synchronism with the computer's internal timing and program requirements. Provisions usually must be made, however, to ensure that the computer will see the service request even when the request is made at a time it is not polling. It is also necessary to prevent multiple responses to events that span more than one polling cycle.

Interrupt asset

The interrupt concept provides a more asynchronous interface to the service requests, with the further benefit of requiring little software overhead until an event actually captures the CPU's attention. Upon receipt of an interrupt request, the CPU finishes execution of the current instruction, then transfers control to a predetermined interrupt service routine address.

Many systems provide so-called vectored interrupts that automatically supply a different call address, depending upon the relative priority of the interrupt request about to be serviced. The service routine performs the functions needed to respond to the interrupt, such as activating a peripheral or performing data transfers or manipulations. Control is then returned to the interrupted program.

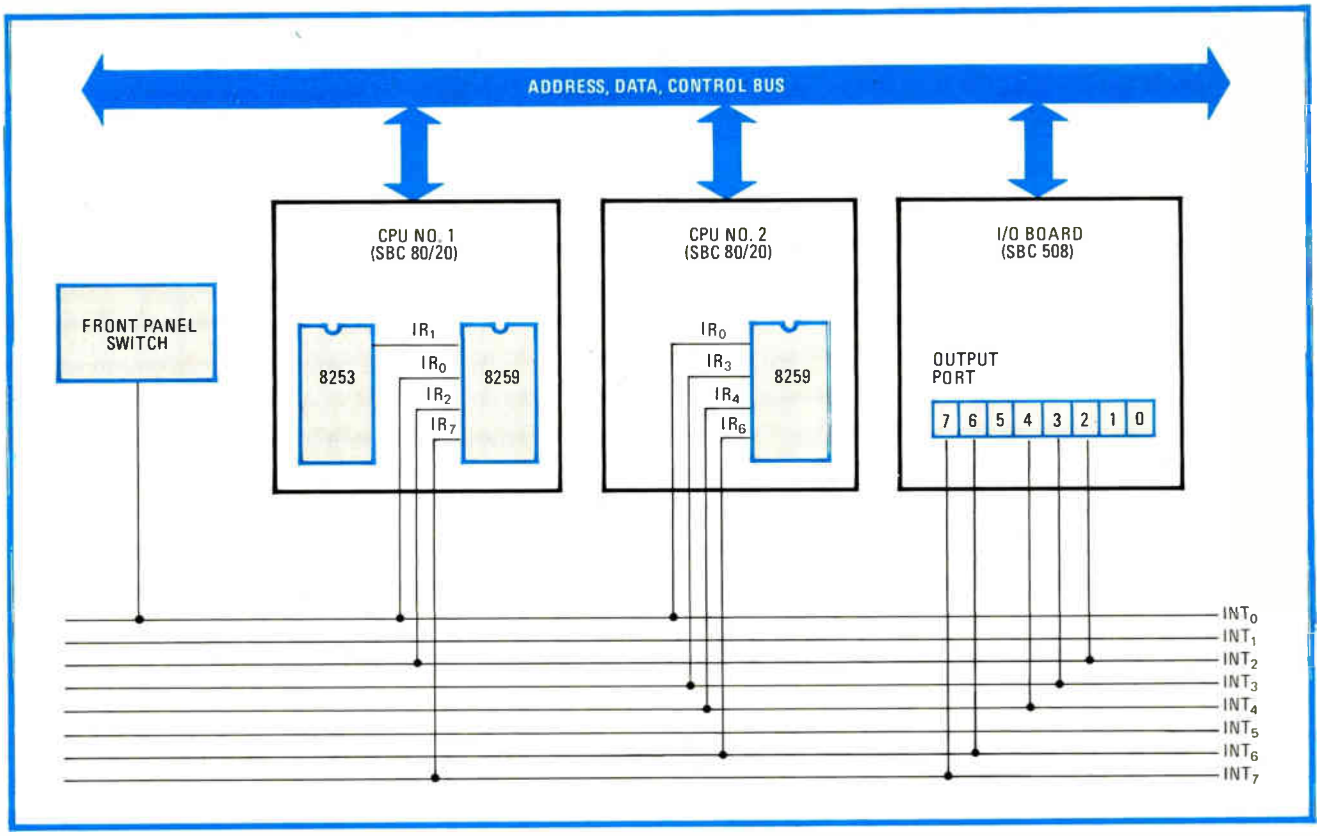
The tradeoffs presented by these two techniques depend upon the details and requirements of the application. These tradeoffs will be discussed in terms of a particular measurement application—an automated data collection, analysis, and recording system, whose block diagram is presented in Fig. 1.

Design goals

This measurement system was designed to be installed in an aircraft and flown in a grid pattern over radio-frequency signal sources on the ground. The key measurement parameter was the received signal level at the aircraft, the characteristics of which were unknown and possibly subject to Rayleigh signal fading. To get a true estimate of the statistical distribution from the time samples, a sufficient number of samples must be taken. For the conditions of aircraft speed and desired confidence level, a sample rate of 100 to 400 hertz was determined to be adequate. Also, since some of the follow-on data analysis and reduction were to calculate a statistical distribution of the signal in space plus a quasi-antenna pattern of the signal sources, it was decided that this receiver sampling process could not be interrupted—that is, it could tolerate no time intervals longer than one sample between samples.

The rest of the system requirements are overhead functions such as reading the location of the aircraft when the signal is sampled, writing data to a tape, etc. Briefly, the system's tasks are:

■ Sample the receiver analog-to-digital converter at a



2. Interrupt bus. The eight lines at the bottom of the figure are a representation of the measurement system's interrupt bus. The various interrupt levels were made accessible to the three bus masters, but only those lines that applied were connected to the modules.

synchronous rate of 100 to 400 samples per second.

- Enter position data from the navigation system.
- Sort measured data into amplitude bins as it is collected.
- Periodically print distributions of signal-level data.
- Print system error and status messages as required.
- Record the sampled data on standard magnetic tape, along with aircraft position and time of day.

It soon became apparent that meeting these requirements would require a high-speed system. The alternative hardware implementations were first explored, and these resulted in the following design decisions:

- Let the sample rate be controlled by a programmable interval timer.
- Perform tape operations via direct memory access.
- Do data reduction with a high-speed math board.

Although these implementations greatly decreased the task load on the CPU, the console I/O remained a stumbling block. With that in mind, the decision to use an additional processor for I/O was made. This would enable one processor to take care of the high-speed tasks while the other processor took care of the slower tasks plus housekeeping functions.

System implementation

The dual-processor system was built from the Intel SBC series of single-board computers and their attendant Multibus, which provides common address, data, and control lines for the system. The bus goes a long way to solving the problems of interfacing several master modules on a common system bus and provides bus arbitration for both serial and parallel priority schemes.

The Multibus was used to interface three master modules: a DMA board and two CPU boards in serial priority. The tasks were partitioned so that one CPU performed all of the data sampling, analysis, and statistics generation, and the other performed console-I/O and system-control functions. Table 1 details the tasks performed by the three bus masters in this system.

Each CPU board has its own on-board bus over which the CPU communicates with its own memory, I/O, interrupt lines, and so on. Most of the control and signal lines of this bus are made available to the Multibus via bus interface logic, whereas certain features remain accessible only to the resident CPU. In the measurement system, each CPU communicates privately through memory addresses 0 to 800_{16} and their interrupt controllers.

To keep the a-d sample rate as constant as possible, a programmable interval timer controls the sample delay periods. The end of the timer delay cycle provides a sample command to the converter by letting the timer initiate an interrupt request. The service routine initiates a new sample delay, reads in the a-d sample, stores it in the tape buffer area, and analyzes and checks the data for errors.

A dual buffer memory scheme increases data throughput. The first CPU fills one of the buffers while the DMA controller empties the other to tape. Similarly, half a dual buffer provides the second CPU with statistical data while the first stores another set of data in the other half of the dual buffer.

So far, the system described illustrates the use of

TABLE 2: INTERRUPT OPERATIONS

Interrupt level	Interrupt	Description
0	front-panel interrupt switch	CPU No. 1 halts its data collection activities, and completes programs in progress; CPU No. 2 prints status message to the console.
1	interval timer on CPU No. 1	The programmable interval timer provides the sample delay for the a-d converter.
2	from CPU No. 2	General control: signals CPU No. 1 to start or resume operation after a system startup or interrupt 0 sequence.
3	from CPU No. 1	General control: signals CPU No. 2 to start or resume operation after system startup or interrupt 0 sequence.
4	from CPU No. 1	CPU No. 1 places error or status message text into memory, then uses the interrupt to signal CPU No. 2 to print message.
6	from CPU No. 1	CPU No. 1 places statistical data into memory, then uses the interrupt to signal CPU No. 2 to print statistics.
7	from CPU No. 2	Signal from CPU No. 2 to CPU No. 1 indicating the beginning of a system test sequence.

special-purpose hardware, multiprocessing, and interrupts to provide the desired system throughput capabilities. The description is not complete without detailing the methods used by the system components for communication and control.

Interrupt processing

The SBC 80/20 computer accepts up to eight interrupt requests and automatically determines their relative priorities. The CPU can be forced to ignore all interrupt requests by executing an instruction to disable interrupts (DI). In addition, interrupts are disabled automatically while an interrupt is being processed and, if desired, the CPU can disable interrupts on an individual basis.

In the measurement system, both CPU boards are capable of responding independently to interrupt requests issued on the Multibus. The key word here is independently. An interrupt request on a particular Multibus line may cause both CPUs to be interrupted; however, the services performed by each at that point may be completely different. An example is the response to a front-panel interrupt (INT_0 on the Multibus). The first CPU performs some tape operations and other assorted tasks, while the second one prints out status messages and waits for the arrival of further instructions from the operator.

The Multibus interrupt requests also function as a means of communication between the two CPU boards. In addition, they provide a ready interface with the outside world. Figure 2 diagrams the interrupt structure of the measurement system, showing the sources and destinations of the requests, as well as their interface with the Multibus.

Figure 2 oversimplifies the CPU-to-Multibus interface with respect to the ability of the CPU board to generate a Multibus interrupt request. The configuration of the hardware did not allow the CPU board to accomplish that directly, but the problem was overcome in a way that provides extreme flexibility for the generation of interrupt requests.

Each level of interrupt request is wired to a single bit of an I/O port on an SBC-508 I/O expansion board as shown in the figure. The port is addressable by either CPU board, thus allowing either CPU to initiate an interrupt request on any level by merely loading the appropriate value to the interrupt-generation port.

To request an interrupt on level 2, for example, a pulse must be applied to that bit in the port by a 00_{16}, then a 04_{16} (a 1 in bit 2), followed by a 00_{16}. The pulse will appear on the Multibus INT_2 line, which is connected to the first CPU's interrupt controller so that appropriate actions are taken. Thus, with this configuration, a CPU board can issue an interrupt request to itself, the other CPU, or both, depending upon the configurations of their prospective interrupt controllers. Table 2 details the responses made to the interrupt requests used in the measurement system.

When several asynchronous processes attempt to share common memory resources, the data accessed by each unit may change, depending upon the order in which each device accesses the memory. This problem was circumvented in two ways. One was to assign control of the access of public memory to the first CPU. With this method, the first CPU either performs the transfers with that portion of memory or dictates when the other devices are allowed to make access. The second way was to ensure that the timing relationships were such that the second CPU and DMA operations were finished with their data before the first CPU could overwrite it.

Software

The system software can be subdivided into four parts The first part is the hardware initialization software that brings the system to a known desired state. Most of these functions are automatically done on the SBC 80/20, as these functions are implemented by the system monitor. The second part, the driver software routines, are called to control the tape recorder, navigation interface, clock interface, math board, a-d converter, console, and so on. These drivers are usually small (one page of code or less)

```
         THIS ROUTINE IS CALLED UPON RECEIPT OF A
         FRONT-PANEL INTERRUPT (ON LEVEL 0). IT WRITES
         THE LAST SAMPLE BUFFER TO TAPE ALONG WITH
         AN EOF, STORES POINTERS AND TIME FOR CPU # 2,
         THEN SIGNALS CPU # 2 TO PRINT STATUS. WHEN
         CPU # 2 IS DONE, IT SIGNALS # 1 WHICH THEN
         RE-INITIALIZES ITSELF.

INH01:   SHLD     CSBPT        ;SAVE CURRENT RCVR BUFFER POINTER
         LXI      D, TPBUF     ;POINT TO TIME BUFFER LOCATION
         CALL     TIME         ;STORE THE TIME THERE

         LXI      B, BUFFL     ;SET BUFFER LENGTH
         LHLD     BUFFT        ;AND START ADDRESS
         CALL     PDW          ;AND WRITE THE BUFFER TO TAPE
         CALL     PEOF         ;ALONG WITH AN EOF

         POP      PSW          ;POP RETURN ADDRESS PUSHED BY INTO
         MVI      A, NSEOI     ;RESET THE INTERRUPT CONTROLLER
         OUT      ICCP
         MVI      A, IMSK1     ;GET COMMAND TO MASK LEVEL 1
         OUT      MSKPT        ;TO DISABLE SAMPLE TIMER
         MVI      A, ENSMM     ;GET COMMAND TO ENABLE SPECIAL
         OUT      ICCP         ;MASK MODE SO THAT THE MASKED
                               ;LEVEL 01 WILL NOT PREVENT LEVEL 02
                               ;FROM GETTING THROUGH

         CALL     GPIN3        ;SIGNAL CPU # 2 THAT THE STATUS
                               ;INFO IS READY FOR PRINTING
                               ;BY ACTIVATING INT3/
         HALT HERE AND WAIT FOR INTERRUPT # 2 TO
         RETURN US TO THE STATEMENT AFTER THE HALT. THIS
         IS DONE SO THAT CPU # 2 HAS TIME TO PRINT ITS
         STATUS BEFORE THE RE-INITIALIZATION WHEN
         THINGS GET DESTROYED.

         EI                    ;ENABLE INTERRUPTS SO WE CAN
         HLT                   ;WAIT HERE FOR INTERRUPT # 2

         RE-ENTER HERE AFTER INT 2 RECEIVED.
         INTERRUPTS ARE DISABLED AND THE CONTROLLER WILL
         BE RESET DURING RESTART.
         JMP      RST1         ;AND THEN RESTART
```

3. Interrupt handler. CPU No. 1 executes this routine when it receives a level-0 interrupt from the front panel. Among other actions, a special mask mode operation is performed that allows a user to disable interrupts on a particular level and not the others.

and modular and called from the applications software when required.

The third part of the software is the interrupt-handler software. These handlers (eight in this system) each perform specific tasks (see Table 2). Interrupt level 0 causes both CPUs to perform some function. Interrupt level 1 is used by the first CPU only, and interrupts 2 through 7 are used for inter-CPU communication of some sort. Inter-CPU interrupts use one CPU as the interrupt source, with the other responding appropriately. Figure 3 lists the interrupt handler used by the first CPU to respond to a front-panel level-0 interrupt.

The routine illustrates some of the typical actions taken by such a routine, like register preservation, calling of general service routines, and resetting of the interrupt controller. It also illustrates the use of one of the features of the interrupt controller—the special mask mode of operation. This mode allows the user to disable interrupts on a particular level while still letting other interrupts through. In this example, it was desired to ignore all further timer (sample command) interrupts on level 1 while still allowing the signaling interrupt on level 2 to be received from the second CPU. The special mask mode is invoked by issuing the proper command value to the interrupt controller command port.

The last part of the software is the applications software. It contains the function of the particular measurement being made and ties the previously mentioned routines together.

Advantages

Using the multiple-processor approach for a data system such as this has some benefits that would not be realized otherwise. Many data channels can feed the measurement system, and mathematical calculations can be performed in real time. Using the Multibus as the interface enabled standard circuit boards to be used, eliminating special hardware design. And most important, the use of interrupts allowed the software and hardware to interact in a straightforward manner. □

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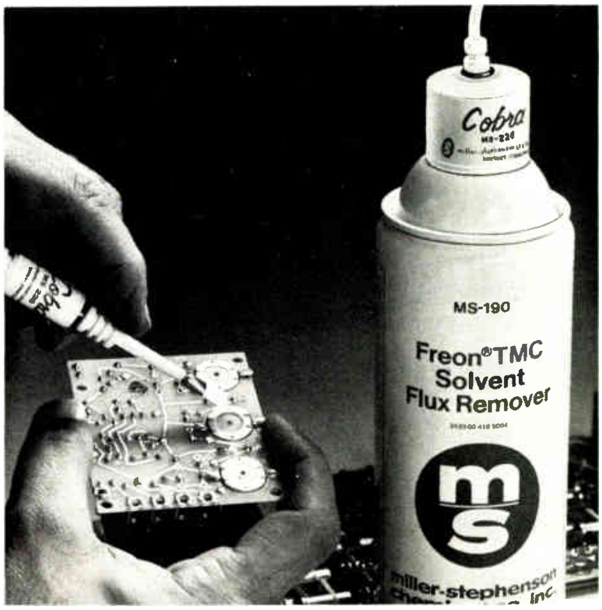

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Logic-analyzer displays eight-variable Karnaugh map

by Dennis Crunkilton
Four Point Technology, Albuquerque, N. M.

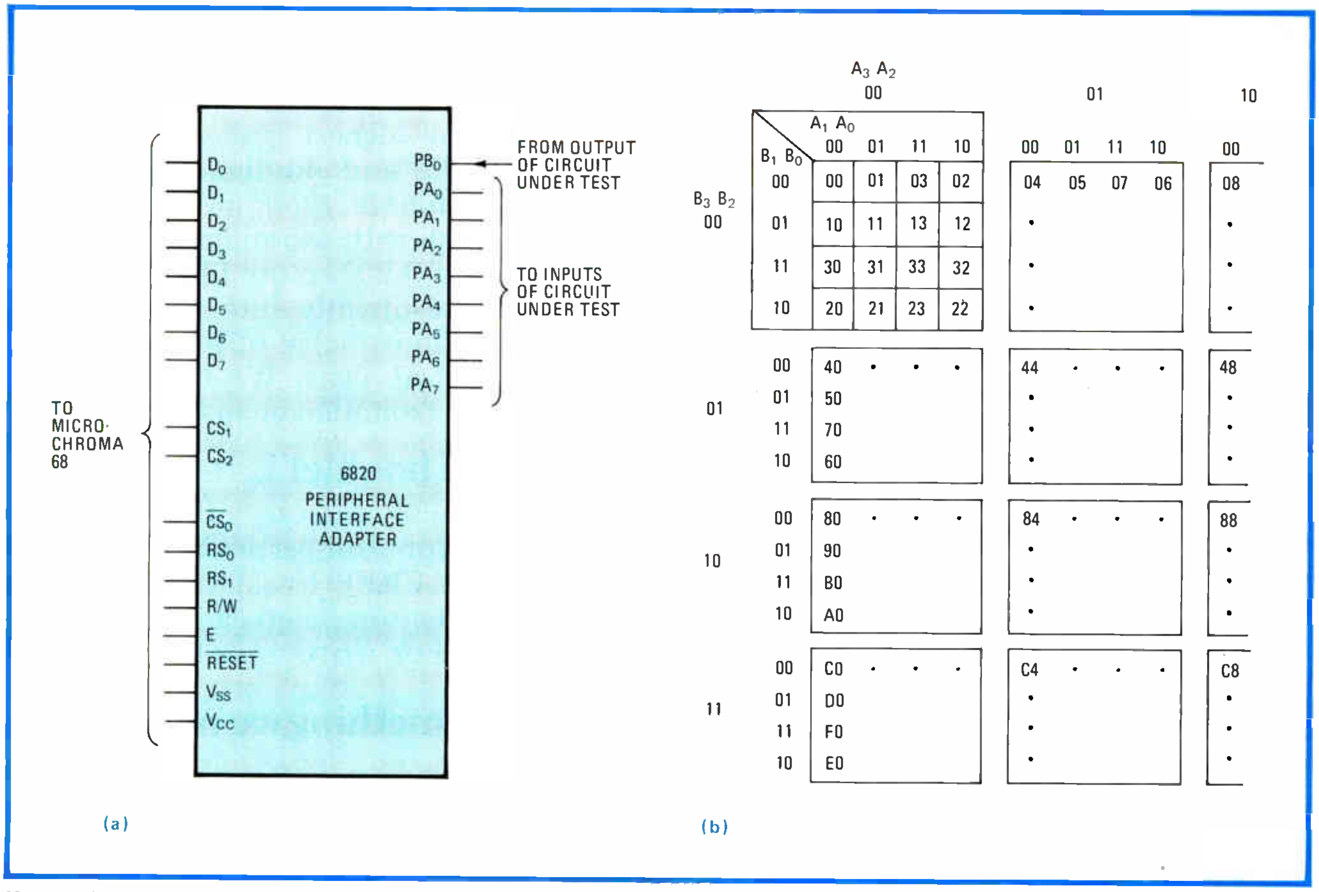
This program and a one-chip interface equip Motorola's popular Microchroma 68 evaluation kit for duties as an eight-variable logic analyzer. Use of the MEK 68 makes it possible to display the corresponding Karnaugh map on large TV-type screens—an asset in educational applications. The software can be readily adapted to any of the developmental systems associated with Motorola's 6800 microprocessor simply by modifying the externally referenced subroutines as required.

This analyzer was developed from Jiraphasra's four-variable circuit for oscilloscopes.[1] In using the MEK 68, however, interfacing hardware for the circuit under test is minimal, in this case requiring only the 6820 peripheral interface adapter (PIA), which is decoded for system address $F450_{16}$(a). An interconnected keyboard monitor to allow user interaction, complete with large screen display, comprises the rest of the system.

In this setup, the eight outputs of the PIA (lines PA_0 through PA_7) are automatically instructed to exercise the circuit under test. Line PB_0 is configured as an input to monitor the response of the circuit for logic values of the given variable field A_0–A_3, B_0–B_3.

To accomplish the monitoring, the program generates a binary count sequence of 0 through 255, where one count corresponds to each of the 256 positions of a 16-by-16-element array (truth table) on the large screen. The Karnaugh-map-address subroutine (location 0063_{16}) is generated by passing the binary count to the KM subroutine (location 0025_{16}), which returns a semi-gray-code equivalent.

The 4 least significant bits are converted to gray code, and the 4 most significant bits remain in binary. In this way, PA_0–PA_7 excite the circuit under test with eight signals and line PB_0 receives the corresponding response as a logic 1 or a logic 0. This response signal, under program control starting at location 0089_{16}, is transferred to the screen of the television monitor through the



Karnaugh mapper. The 6820 peripheral interface adapter is the only hardware required to interface the software-based MEK-68 logic analyzer to a circuit under test (a). The analyzer can display 16-by-16-element Karnaugh maps (b) on a large-screen TV monitor system in two formats: one showing the logic values of all locations in the matrix, the other displaying the addresses of the values in the matrix.

6800 PROGRAM LISTING: 8-VARIABLE KARNAUGH MAP

Address	Op code	Mnemonic	Comment
0010	B6 F404	LDAA	Read keyboard
13	2B FB	BMI	Check for any key pressed
15	81 41	CMPA	If A, go to address subroutine
17	26 03	BNE	
19	BD 0063	JSR	
1C	81 4B	CMPA	If K, go to map subroutine
1E	26 03	BNE	
20	BD 0089	JSR	
23	20 ED	BRA	End of driver. Loop back
0025	B6 F351	LDAA	Get binary count
28	16	TAB	Save in B
29	84 03	ANDA	Look at first 2 LSB of 2nd byte
2B	81 02	CMPA	If it equals 2 . . .
2D	26 02	BNE	
2F	CB 01	ADDB	Make it 3
31	81 03	CMP	If it equals 3 . . .
33	26 02	BNE	
35	C0 01	SUBB	Make it 2
37	17	TBA	Fetch original bin number
38	84 30	ANDA	Look at first 2 LSB of 1st byte
3A	81 20	CMPA	If it equals 2 ... .
3C	26 02	BNE	
3E	CB 10	ADDB	Make it 3
40	81 30	CMPA	If it equals 3 . . .
42	26 02	BNE	
44	C0 10	SUBB	Make it 2
46	F7 F352	STAB	Save KM address here
49	39	RTS	
4A	C6 00	LDAB	Initialize PIA subroutine
4C	F7 F451	STAB	CRA = 00; grant access to DRA
4F	F7 F453	STAB	CRB = 00; grant access to DRB
52	F7 F452	STAB	DRB = 00; set PB as inputs
55	C6 FF	LDAB	
57	F7 F450	STAB	DRA = FF; set PA as inputs
5A	C6 04	LDAB	B = 04
5C	F7 F451	STAB	CRA = 04; enable ORA
5F	F7 F453	STAB	CRB = 04; enable ORB
62	39	RTS	
0063	CE 0000	LDX	X = 0000; initialize binary sequence
66	FF F353	STX	Save X
69	FF F350	STX	Pass bin to KM subroutine
6C	BD 0025	JSR	Get KM address
6F	CE F352	LDX	KM address from subroutine
72	BD F9A7	JSR	Output 2_{16} for monitor
75	FE F353	LDX	Restore X
78	08	INX	Increment binary count
79	8C 0100	CPX	Increment done?
7C	29 E8	BNE	If not, do again
7E	39	RTS	
007F	B6 F352	LDAA	Pass KM address from KM subroutine
82	B7 F450	STAA	PA accumulator A: write to device under test
85	B6 F452	LDAA	Accumulator A PA: read from device under test
88	39	RTS	
89	CE 0000	LDX	Set up binary count
8C	FF F353	STX	Save X
8F	FF F350	STX	Send bin to KM subroutine
92	BD 004A	JSR	Call PIA subroutine
95	BD 0025	JSR	Call KM (address) subroutine
98	BD 007F	JSR	Send address, read response
9B	84 01	ANDA	Mask unused input bits
9D	8B 30	ADDA	Convert to ASCII
9F	BD F803	JSR	Print (monitor)
A2	86 20	LDAA	Load code for space desired
A4	BD F803	JSR	Print space (monitor)
A7	FE F353	LDX	Restore X
AA	08	INX	Increment binary count
AB	8C 0100	CPX	Increment done?
AE	26 DC	BNE	If not, do again
B0	39	RTS	

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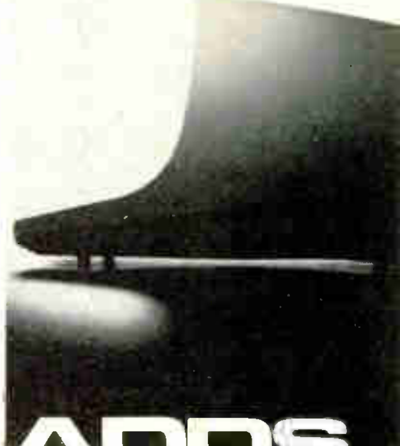

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peripheral interface adapter's data bus.

The map may be displayed in two formats, one showing the logic values for all locations in the matrix, the other containing the locations (addresses) of the logic variables. Keying in the letter "K" will generate a 16-by-16 array of 1s and 0s corresponding to the truth table of the circuit under test. Pressing A will generate an array that shows the actual location of the binary addresses (b), shown in segmented cells for clarity. In the actual case, the screen would be filled with a contiguous block of numbers 32 rows long and 16 columns deep. □

References

1. Prasert Jiraphasra, "Low-cost logic analyzer displays Karnaugh map," *Electronics* Dec 8, 1977, p. 118.

Low-cost tester checks DIP switches

by Stephen Strom

Motorola Inc., Semiconductor Group, Phoenix, Ariz.

Detecting all the possible failure mechanisms in dual-in-line package (DIP) switches of the multiple single-pole, single-throw and the double-pole, single-throw variety, this circuit is simple and inexpensive and will therefore be invaluable for production-line testing. The basic circuit is useful for uncovering defects in 16-pin switches: it is easily expanded so that 8- and 14-pin switches can be checked.

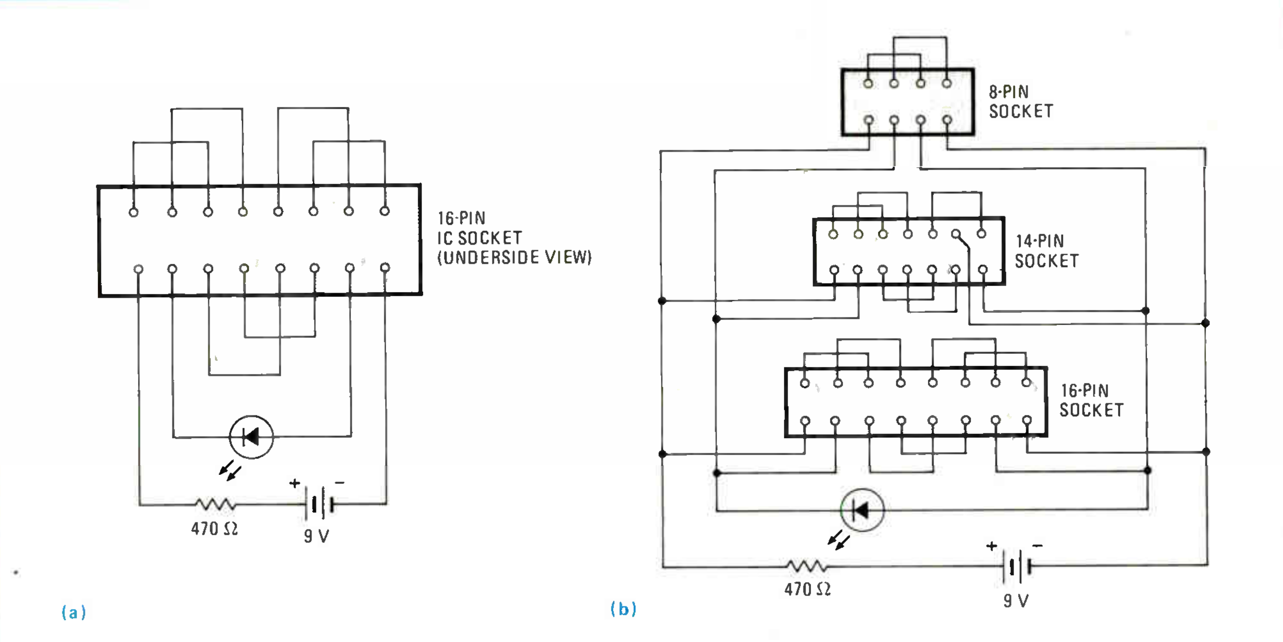
The basic DIP assembly can exhibit three types of failure mechanisms—two adjacent switches can be shorted together, a switch in the closed position may not be touching its respective terminal, or a switch in the open position may be touching its respective terminal. The switch tester shown in (a) can test for the first two failure mechanisms simultaneously in 16-pin devices as well as detect complex combinations of the two.

To initiate the test, the DIP assembly is inserted into the socket with all of the switches in the closed position. Because the tester daisy-chains all of the switches, the light-emitting diode will be illuminated if each switch is making proper contact with its respective terminal and if there are no shorts between adjacent terminals. Any fault encountered will keep the LED off.

To test the third failure mechanism, when a switch in the open position is still making contact with its terminal, the technician must open and close each of the switches within the assembly. Initially, the LED will be on; however, it must go off and on each time each switch is opened and closed, or the assembly is faulty.

The arrangement in (b) will accommodate all popular switch sizes. That includes the 8-, 14-, and 16-pin single-pole, single-throw switch types, as well as the 8- and 16-pin dip switches of the double-pole, single-throw variety, which have virtually the same electrical configuration as their spst counterparts.

The circuit will operate from a 9-volt transistor battery and thus is suitable for portable use. Maximum current drain is approximately 15 milliamperes. □



Line test. Circuit daisy-chains multiple spst or dpst switch contacts of 16-pin DIP assembly in order to check for all types of open circuits and shorts (a). Illuminated LED indicates good assembly. Circuit is easily expanded to handle the popular 8- and 14-pin types (b).

Full-wave bridges tie dc power supplies together

Many high-reliability electronic installations require redundant or uninterruptible power supplies to guarantee system integrity, but most of the methods used to tie dc power supplies directly to a common bus are complex and expensive. D. F. Hines of the Algome Steel Corp., Sault Ste. Marie, Ontario, has come up with a dc-dc interconnection that is also **immune to incorrect supply connection yet costs only a few dollars.**

Hines's circuit is built around two identical bridge rectifiers—he suggests Varo VM108s. One dc voltage, V_{1in}, is fed to what would normally be the ac input to one of the bridges, while a second isolated dc voltage, V_{2in} is fed to the identical points on a second bridge rectifier. Output voltage, V_{out}, is taken across the paralleled floating outputs of the dual bridges and is equal to V_{in} minus 2 V_d, where V_{in} is the value of the higher supply voltage and V_d is a diode drop.

The higher voltage back-biases the diodes holding the lower voltage off. When the two supplies are equal, load current is shared. A short or open circuit on either input causes a smooth voltage transfer. A battery 2 V_d lower than the normal bus voltage can act as a backup supply, in which case it replaces the lower supply.

Novel chip-carrier fits in game and calculator cartridges

For its foreign language memory cartridge, the Craig language translator uses a custom memory package specially designed by Molex Inc. The package could also be used in programmable calculators, TV games and any **other applications that require specialized read-only memories to be easily removed from and plugged into microcomputer boards.**

The package consists of a low-cost molded nylon and glass integrated-circuit holder, plus a special socket. The ROM's 24-pin dual in-line package is inserted upside down into the holder and its leads are folded to secure it. The holder is then inverted and inserted by means of a small molded handle into the special socket, which in turn is wave-soldered to a printed-circuit board. The socket and holder are keyed to each other to prevent misalignments. The insertion and withdrawal force is less than 5 lb. For additional information, contact Don Siebold, Molex Inc., 2222 Wellington Ct., Lisle, Ill. 60532.

Dig into Pascal, Modula, and Portal

If you want to keep up with the latest programming languages—Pascal, Modula, and Portal—there is some good literature around that may be of help. An excellent discussion of Pascal is given in a 29-page article in Acta Informatica (1971), reprints of which can be obtained from the inventor of that language, Niklaus Wirth, if you write to him at the Computer Sciences Department of the Swiss Federal Institute of Technology (CH-8092 Zurich, Switzerland).

Wirth will also supply reprints of articles (from "Software—Practice and Experience," Vol. 7, pp. 3–35, 1977) dealing with **Modula, the language for modular multiprogramming** intended mainly for dedicated computer systems. Finally, anyone interested in Portal, the programming language for real-time systems, should ask for the Landisand Gyr Review 2-78, obtainable from the Swiss firm Landis and Gyr Zug Corp., CH-6031 Zug, Switzerland. It contains one introductory and one survey article on that high-level language. **-Jerry Lyman**

STRATHCLYDE

the right environment for electronics.

There is already a thriving electronics industry in Strathclyde. Many international companies have established large plants in the region as a base for their European operations. Firms like IBM, Honeywell, Digital, National Semiconductor and Motorola.

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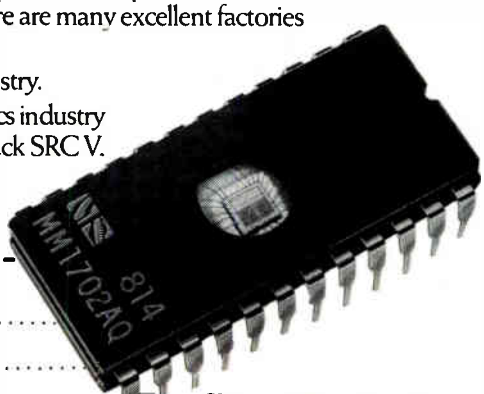

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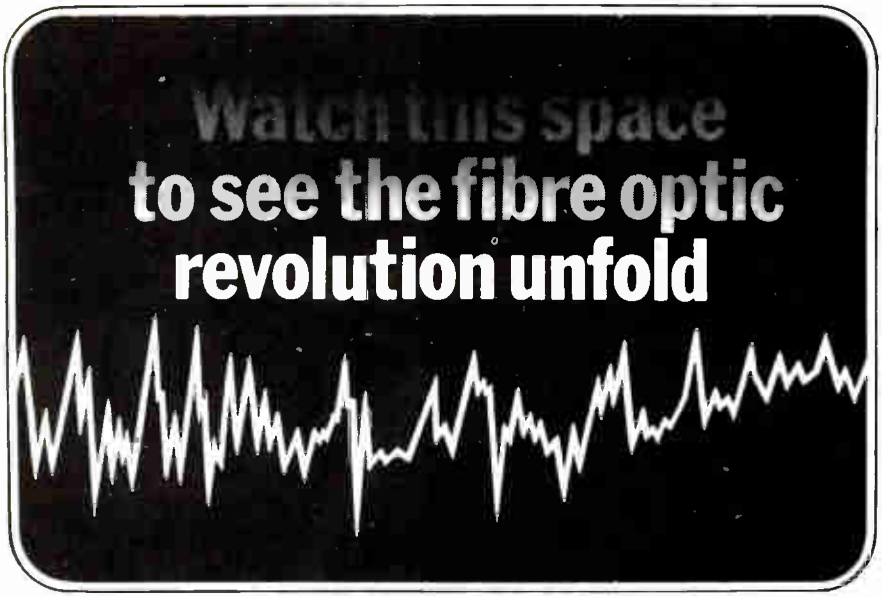
The silicon chip illustrated (type MM 1702 AQ) is manufactured in the Strathclyde Region by National Semiconductor (UK) Ltd.



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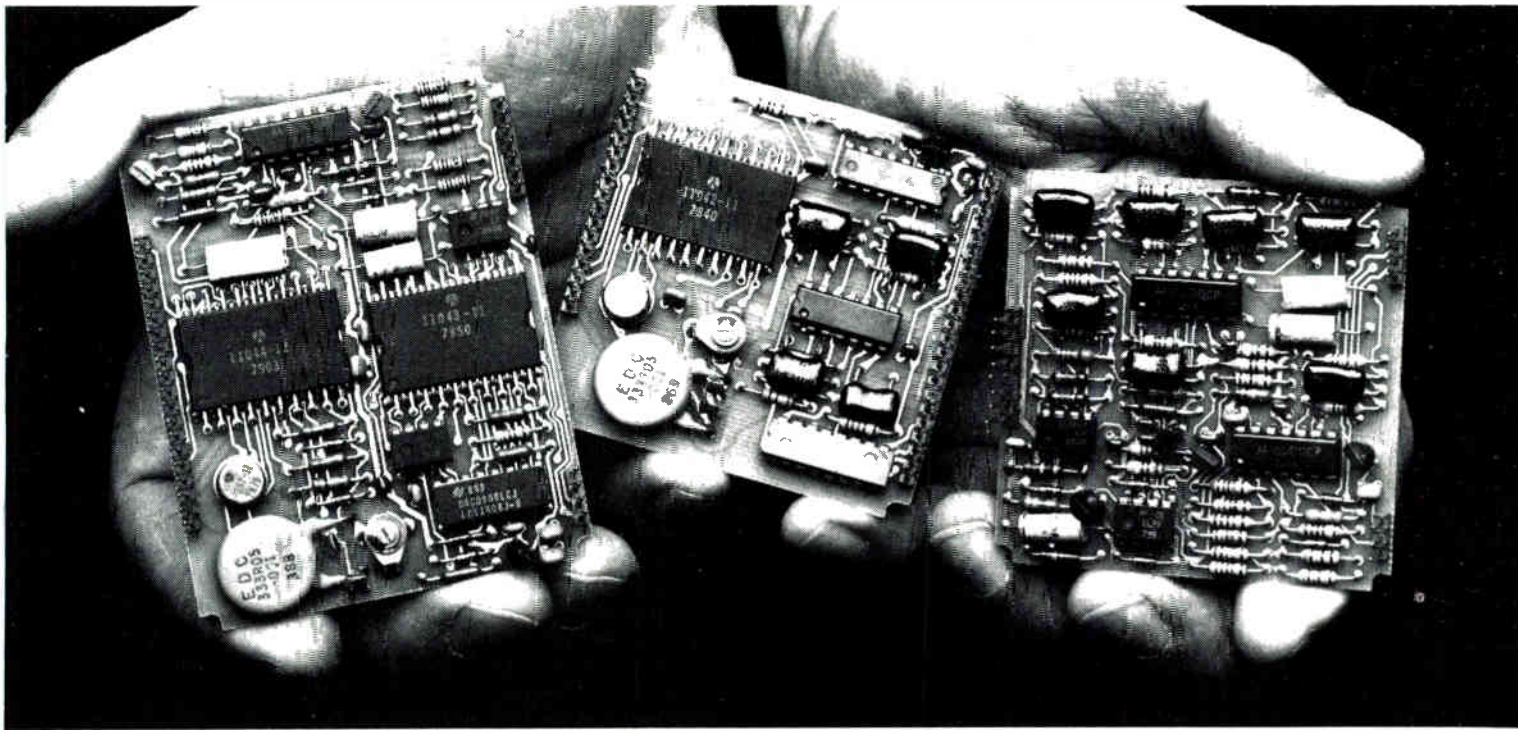

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Data network switches packets

Networking system supports multipoint networks with up to 100 nodes and automatically reconfigures itself around faults

by James B. Brinton, Boston bureau manager

Almost all minicomputer firms offer some form of networking and almost all have severe limitations. But the Digital Equipment Corp., Maynard, Mass., got an earlier start than most, introducing its DECnet Phase I networking system into the market over a two-year period, between 1974 and 1976. Phase II was announced in 1978, and now the firm has unveiled DECnet Phase III, a system capable of handling widely varying interconnection topologies within adaptively controlled nets of 20 to more than 100 nodes.

The announcement is especially interesting in light of IBM Corp.'s late-January statement that it is considering adaptive routing for its future network systems. IBM is thought to be about three years away from any implementation, say industry sources.

So DEC probably is not exaggerating when it claims that DECnet Phase III combines almost all the features of other available computer networking systems, plus many heretofore unavailable ones (see "DEC emulator goes after IBM market").

Phases I and II had direct node-to-node, modem-and-cable connections between every communicating computer pair. The result was much like that of a telephone system before the central office's advent. And because of the large amount of dedicated interconnection hardware needed it was costly. Phase I in particular failed to get a foothold in the market.

Partly because of the cost of earlier interconnection schemes, "of the approximately 500 networks now using DEC equipment, the average size is only four nodes," says Stephan W. Johnson, product manager, distributed systems. The reason is simple enough, he says: interconnection costs tended to rise almost as the power of the number of nodes in a network.

DEC's Phase III DECnet addresses this problem directly while preserving the best features of its Phase I and II systems such as multi-operating system compatibility. Although the system is being made available first to users of the RSX-11M, -11M-Plus, and -11S operating systems, plus appropriate computers, over the next 18 to 24 months, DEC plans to make it available to users of all DEC operating systems except the aging IAS.

The Phase III system is packet-based. A typical packet is 290 bytes long: 256 bytes of data, plus the necessary protocol bytes needed to move through the multiple layers of DECnet software.

The DECnet features the company is proudest of include:

- Adaptive path routing.
- Multipoint operation.
- Network-command-terminal operation.
- Network-management functions.

Rerouting. Through adaptive path routing, nodes communicate with each other via each other, acting as store-and-forward intermediaries between communicants. Where more than one path exists between nodes, network software automatically selects the highest-speed, least-cost route by consulting a routing table in memory. This table is continually updated with link status information so that if a link fails or encounters

DEC emulator goes after IBM market

Simultaneously with DECnet Phase III, Digital Equipment Corp. is offering its RSX-11M, which emulates the protocol of IBM's Systems Network Architecture. SNA employs a large central-control computer surrounded by cluster controllers to service distributed processors and peripherals. On paper, its topology resembles an octopus with smaller octopi attached to the end of each tentacle.

Now, through the SNA protocol emulator, DEC can make one of its PDP-11 class machines seem to an IBM host to be identical to a cluster controller. Through the emulator package, up to four 9,600-bit/s lines can support as many as 61 concurrent logical connections—seeming overkill for a single PDP-11. But there are some obvious market implications here.

If a user can get what he needs from a digital machine at less cost than for a cluster controller and its associated equipment, DEC could begin eating into IBM's heretofore almost captive network market—and the company expects to do just that.

Further, as soon as DEC develops the software allowing the SNA emulator to run concurrently with Phase III DECnet—and that will be "in the near future," according to the company's Internet product manager, Allan C. McGuire—users will be able to graft large DECnet networks onto IBM-based systems with "near-total transparency." Thus a user will not have to give up features of one firm's products when buying from the other. **-J. B. B.**

too high an error rate, it is ignored for communications purposes and an outage notice is generated. Meanwhile, communication continues over the next-least-costly route.

Johnson points out that adaptive path routing saves a bundle of money. In a sample four-node network, only half as many modems and cable links are needed as in Phases I and II, and the savings increase as the size of the network expands.

Multipoint lines. A multipoint system is either a small network or a building block for larger nets. This feature allows up to eight tributary computers to communicate over a single duplex line while a host computer controls communications, polling each machine in turn. Tributary computers communicate with each other via the host. In larger nets, computers in a multipoint configuration would all be able to participate in message routing, file transfer, and resource access with other computers via their host.

Again, because only a single duplex connection—much like a bus system—connects each computer, interconnection cost is minimized. Thus multipoint systems fit well into low-cost, small network applications.

Network management. Finally, there is Phase III's network-management function. It can be either centralized or distributed among nodes to monitor communication loads, error rates, line conditions, and net-wide node status. The decision to centralize or decentralize this function will probably be based on two factors: the organization using the net (if it is highly centralized, it will most likely opt for centralized control) and memory availability or cost. Lower-cost networks would use only enough node memory for normal operation plus store-and-forward activities, while a central node would be equipped to handle the management function.

Phase III software allows the human managers of the net to evaluate its overall efficiency and optimize traffic flow by altering the path-selection routine's routing table. Managers also can make full-system, interface, and line tests without impairing the operation of the network.

Notably, Phase III includes fault location and isolation. Its network management system can isolate problems to the modem level through looped test messages transmitted, returned, and compared with the original. Phase III can isolate faults down to the buffer level, but not within modems. There are just too many different ones, says Johnson, for there to be a common modem test algorithm.

Written agreement. Customer support will be an important aspect of the Phase III marketing push, he says. DEC's customer support plan will involve a written understanding between DEC and the customer—end user or original-equipment manufacturer—spelling out exactly what the capabilities of the system are to be, and the responsibilities of DEC and the customer in network operation and upkeep.

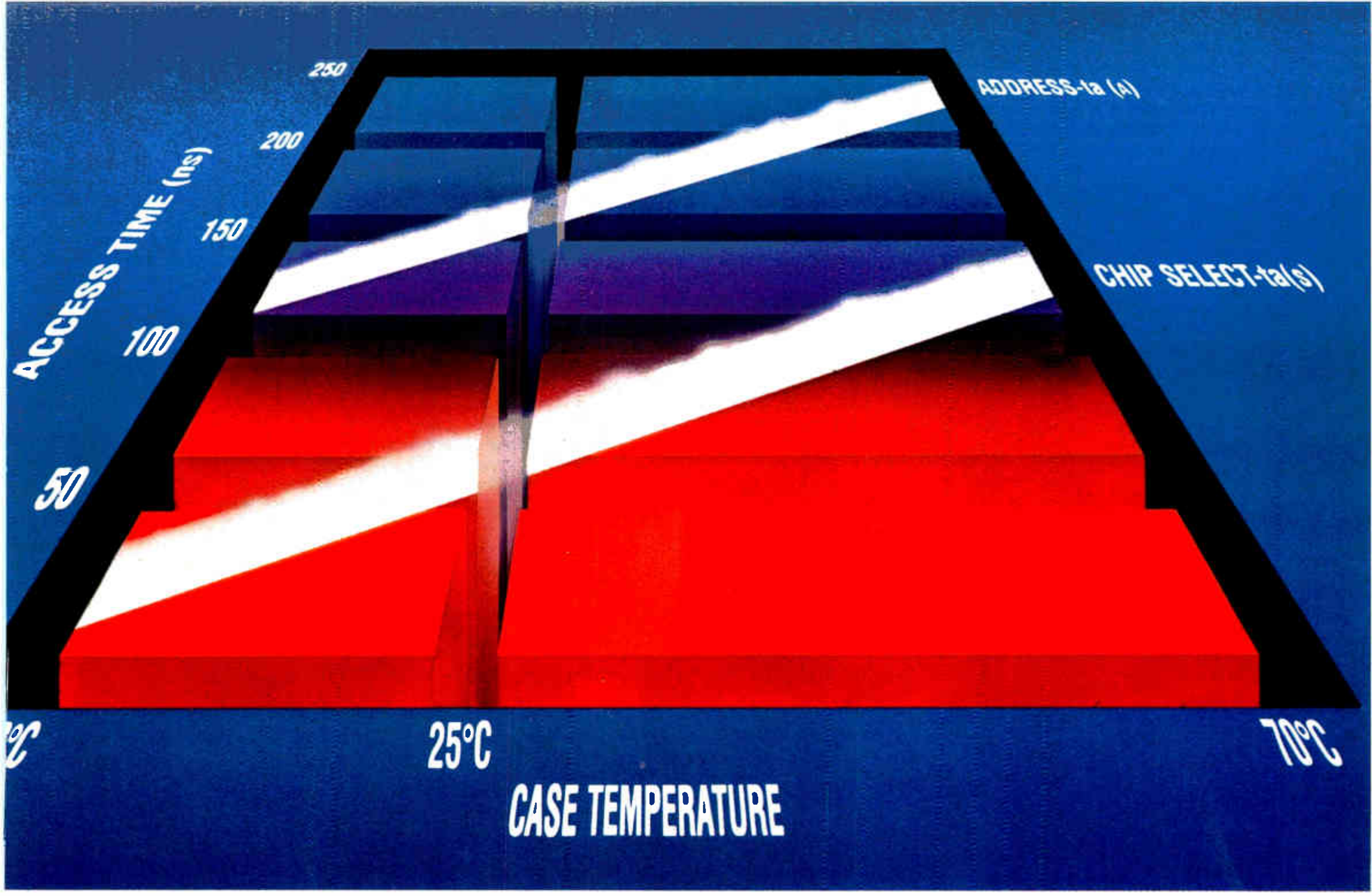
DEC is not offering an X.25 capability as part of Phase III. The firm has decided to wait a bit before offering X.25 compatibility; it may come sometime this year, however.

But in two years, DEC expects Phase IV. Aimed at networks of 100 nodes or more, it will have expanded routing and management capabilities and will be implemented in microcode for greater speed and more economical memory management.

It should also have improved automatic fault location capabilities, if for no other reason than that DEC is now deciding whether to go into the modem business or standardize on a single modem type. Thus it would be able to construct fault location routines usable down to the modem subsystem level.

License fees for Phase III are $5,000 for DECnet-11M-Plus, $3,500 for DECnet-11M and $1,500 for DECnet-11S. These are per-node prices, and OEM and end-user discounts will apply. Deliveries are to begin this month.

Digital Equipment Corp., 146 Main St., Maynard, Mass. 01754. Phone (617) 897-5111 [338]



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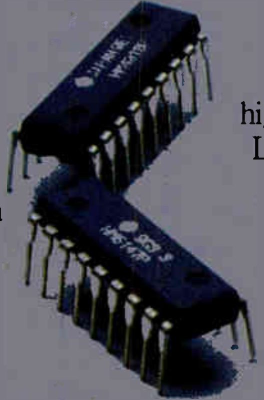

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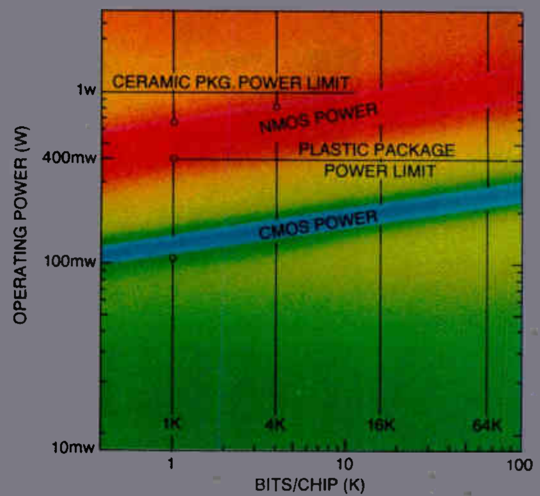
CMOS PLASTIC VS. NMOS POWER LIMITS

Hitachi CMOS plastic technology allows plastic packaging of high-speed static RAMs to densities of 64K and beyond, whereas NMOS reaches the limit at 16K.



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This advanced CMOS plastic technology means you'll need only 200mw to operate our 16K devices compared to the 700mw operating power required by standard 16K NMOS cerdip RAMs.

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Part No.	Organization	Speed	Operating Power	Availability
6147	4K x 1	55/70	75mw	Now
6148	1K x 4	55/70	150mw	Samples
6116	2K x 8	120/150/200	200mw	Samples
4334	1K x 4	300/450	20mw	Now
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Fairchild's LSI know-how adds a new dimension to in-circuit testing.

LSI test know-how.
Fairchild knows about testing LSI. Virtually every LSI device devised by man has been tested on Fairchild's Xincom, Sentry® or Sentinel™ systems. That know-how has been applied to in-circuit testing with the development of the FF303's LSI Testing Module (LTM), to bring a new dimension to LSI testing.

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You need tests that are ready to run, or easily altered, so you can use your time for testing, not programming. The special tests you may need can be quickly and easily generated by using CHIPS, our unique LSI test language compiler. That's the kind of software support you get with the FF303 – along with our commitment to maintain the industry's largest LSI testing library for in-circuit testing.

The complete in-circuit tester.
Your PCBs do not live by LSI alone. So the FF303 is designed to test SSI, MSI, and the whole gamut of analog components. Faultfinder systems pioneered the analog in-circuit test method and the FF303 brings you the advanced component and circuit path inspection techniques you need for precise fault identification and diagnosis.

And you can choose from two different system analog and digital test point capacities with modular expansion as you need it.

With this powerful in-circuit digital/analog testing system, you can count on yields of 95% or better at final test.

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Your FF303 will do more than test. Its computer control lets you selectively run tests, file failure data, use the FAULTS automatic program generator and call, sort and file data quickly and easily. With real-time data logging, you can generate histograms to track PCB assembly failures by shift, day or week. And you can do more.

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Fairchild's Thinline® vacuum fixture system lets you choose from a wide variety of fixtures, fixture kits and universal personalizers. Build your own fixtures with Thinline kits or get turnkey testing with ready-to-test fixtures and programs. No other in-circuit test system manufacturer offers single-source fixturing and contract programming support.

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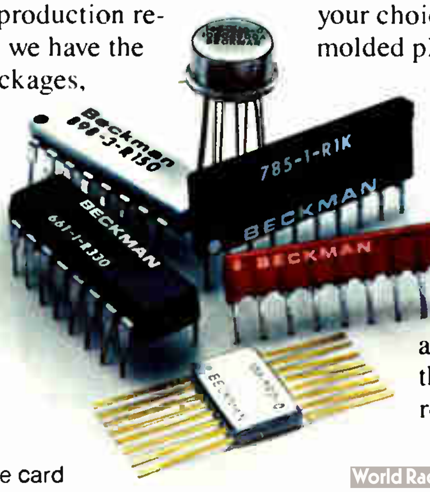

Our technical capabilities include precision, semi-precision and general purpose thick and thin films. We offer four packages: SIPs, DIPs, flat packs, and discrete transistor metal cans. Take your choice of ceramic, molded plastic, or conformal coating. Select from components including resistors, diodes, capacitors, and conductors. Besides large production and technical capability, we offer you the utmost in reliability. And our resistor networks are designed to meet military specifications.

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Design Beckman in.
Design problems out.

BECKMAN

Circle 190 on reader service card

Thick-film heads print 8 dots/mm

Thermal units from Japan incorporate all enabling electronics and have printing times of 2 ms per line

by Larry Waller, Los Angeles bureau manager

Thermal print heads of the thick-film variety, although rugged and relatively inexpensive, have typically not been able to offer the printing resolution of thin-film and semiconductor types. Now a one-piece unit being marketed in the U. S. by R-Ohm Corp. takes advantage of an improved thick-film paste and process to provide up to eight dots per millimeter. Furthermore, all of the head's enabling electronics—driver circuits, shift registers, and diodes—are mounted on the head itself.

The result of a seven-year research program by R-Ohm's parent company, Toyo Electronics Industry Corp., Kyoto, Japan, the new print heads represent a "different physical approach" that overcomes the limitations previously associated with thick films, according to R-Ohm president Kozo Sato. In addition to improved resolution, Sato refers to "better thermal characteristics" that allow an upgrade of performance.

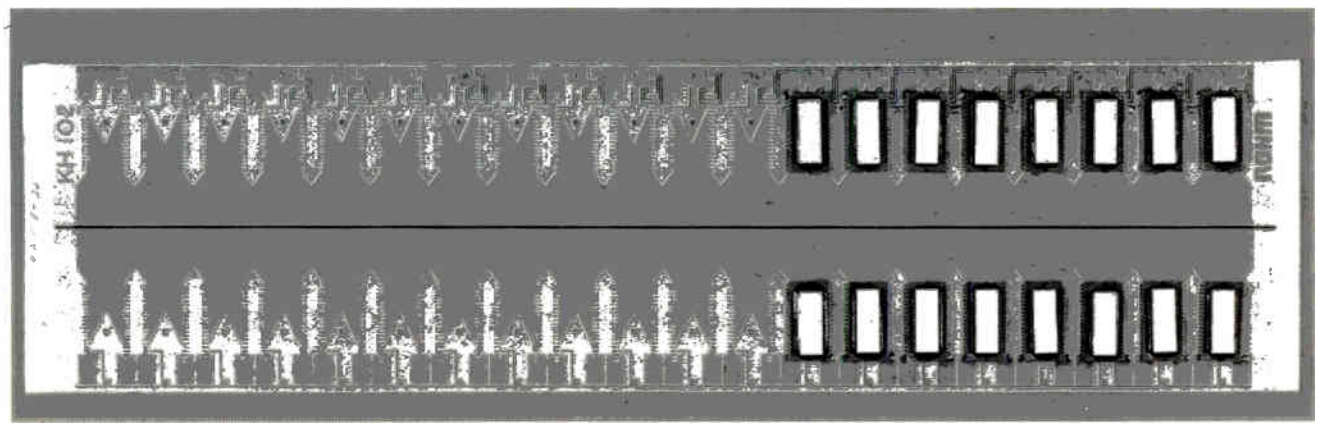
Big. Sato is more informative about the user advantages of the new heads. The most important of these, he says, is that the heads can be built in large sizes, as single units, for such applications as facsimile printing. R-Ohm's first thermal head, the KH102, has an 8.614-in. printing element. To match that size, other approaches must resort to butting several smaller blocks together, creating quality and reliability problems. The printing-quality problem is caused by imperfect matching of the blocks that are butted together: if they are not identical, the optical density of the printing may vary from point to point across the printed copy, depending on which block printed each point. The reliability problems are linked to the number of connections needed by the different approaches. Sato estimates that an array of smaller heads might need some 150 terminations; the KH102 needs only seven.

Printing time for the new heads can be as fast as 2 ms per line, compared with 5 ms per line for semiconductor heads and 8 to 9 ms per line for other thick-film heads. The new devices operate at a maximum temperature of 60°C.

Custom. Because applications differ so much from customer to customer, R-Ohm is developing different designs for each user. So far, parent Toyo Electronics is turning out just enough model KH102s for demonstration purposes, and John Goldman, R-Ohm marketing vice president, reports U. S. customers are snapping up all he can get. For this reason, prices are hard to nail down, but for a $5,000 to $10,000 outlay, a customer gets five sample heads tailored to his needs.

Goldman points out that quantity pricing, while not announced, should be much lower than the $1,000-per-unit sample range, depending more on the total number of dots on the head than on resolution. The KH102 has six dots/mm because the full eight per millimeter possible with the new process is not needed for most facsimile jobs. The part has a total of 1,279 dots, each measuring 0.105 by 0.35 mm. Toyo makes all its own parts, including bipolar ICs, and is phasing the new units into manufacturing lines still turning out earlier thick- and thin-film heads. Delivery time is 90 days.

R-Ohm Corp., 16931 Milliken Ave., P. O. Box 4455, Irvine, Calif. 92716. Phone John Goldman at (714) 546-7750 [339]



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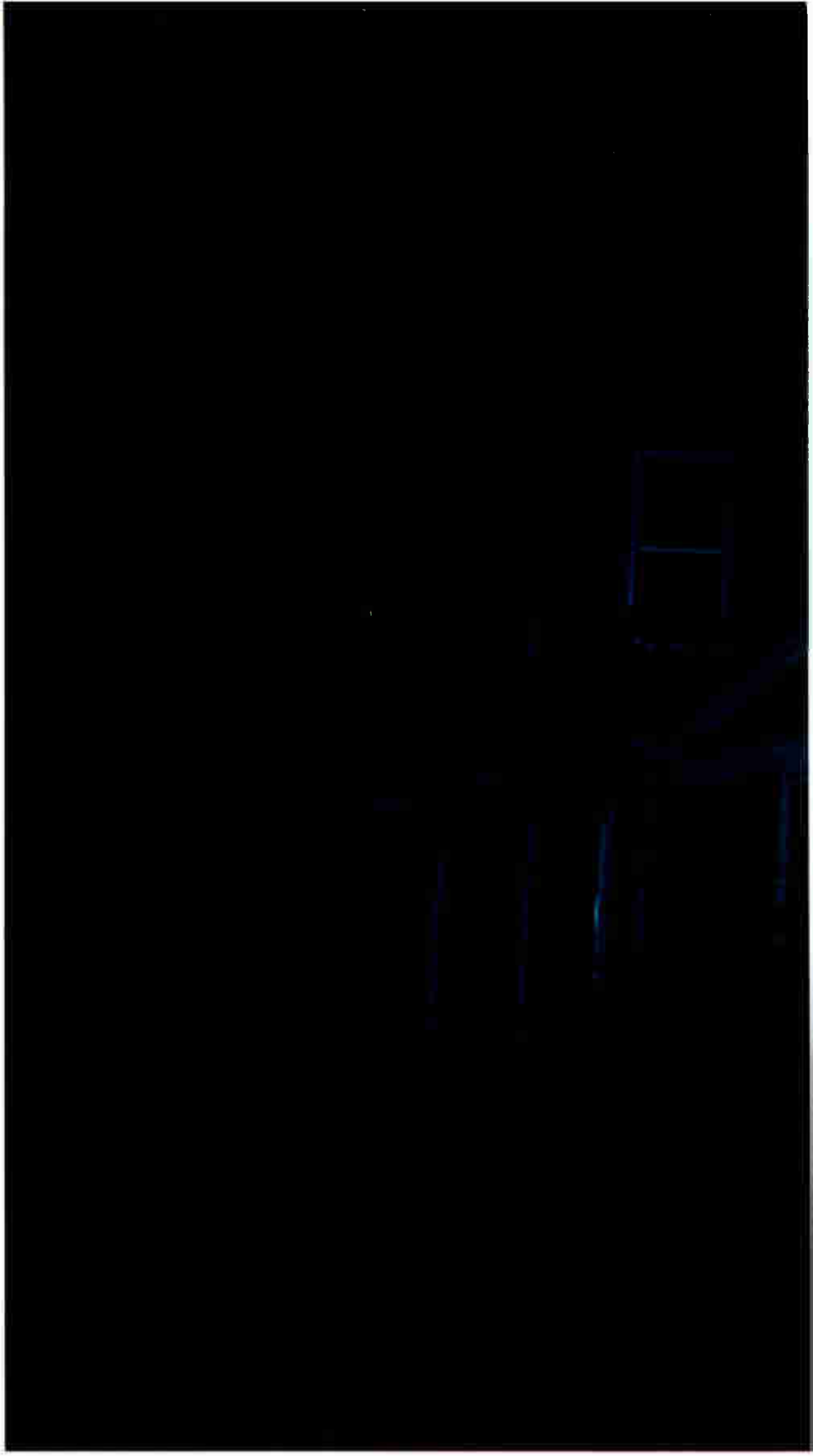


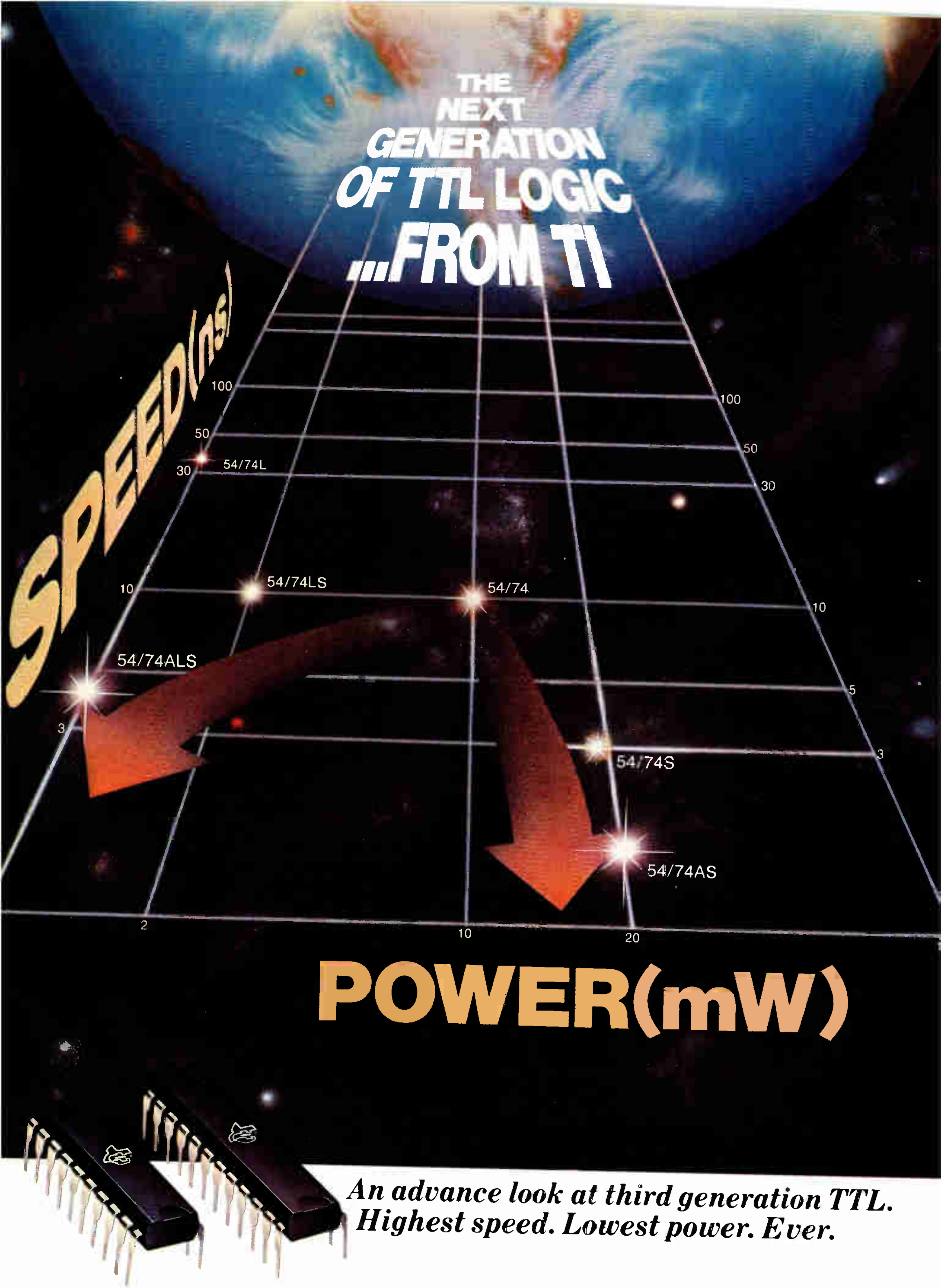
In linear LSI test systems, like anything else, you only get what you pay for. And if you don't look before you leap, that "entirely new approach" to linear LSI testing could turn out to be the very same old computerized tester hiding behind some new metal, complete with all of yesterday's bottlenecks.

With today's LSI devices, you need a sophisticated, accessible and powerful computer to execute the complex test algorithms.

What you need is the LTX Spacesaver LLSI Test System. It's a unique modular integration of hardware and software that's easy to use and easy to program. Our Spacesaver puts computer power where you need it. All with an eye towards speeding up payback by increasing throughput and yield.

Your test engineers can be just that, test engineers, and quickly program, debug and update job plans in a high level language that doesn't require a Computer Science degree to use or understand. They can mix forced or measured variables and obtain rational results without scaling. They can debug and edit online anytime without interruption of production testing. All at a quarter of the cost of competitive systems that may be nothing more than the same old tester hooked to a host computer that does nothing for your testing capability.


You looked at the 11/34 and loved the price.
You looked at the 11/70 and loved the features.
Now look at the PDP 11/44.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30
10
3
54/74L
54/74LS
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54/74ALS
54/74S
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100
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10
5
3
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20
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Featuring a typical 1.5-ns gate delay and a 20-mW gate power dissipation, the new Advanced Schottky (AS) Series is twice as fast as any Schottky device available before.

PROJECTED SAMPLE AVAILABILITY

Part Number	Description	Available
Advanced Schottky		
SN54/74AS804, 05, 08, 32	Hex 2-Input Gates	Now
SN54/74AS882	ALU Look-Ahead	Now
SN54/74AS857	Universal MUX	1Q80
SN54/74AS881	4-Bit ALU	1Q80
SN54/74AS873	Octal Latch	1Q80
SN54/74AS894	Shifter/Scaler	2Q80
SN54/74AS870	Dual 48x16W File	2Q80
Advanced Low-Power Schottky		
SN54/74ALS74	Dual D Flip-Flops	Now
SN54/74ALS109, 112, 113, 114	Dual J-K Flip-Flops	Now
SN54/74ALS00, 01, 02, 03, 04, 05, 08, 09, 10, 11, 12, 15, 20, 21, 22, 27, 30, 32, 133	Gates	Now
SN54/74ALS28, 33, 37, 38, 40	Buffer Gates	Now
SN54/74ALS573, 873	Octal Latches	1Q80
SN54/74ALS574, 874	Octal D Flip-Flops	1Q80
SN54/74ALS160, 161, 162, 163, 168, 169, 568, 569	Synchronous 4-bit Counters	1Q80

Internal gate delay for MSI functions is typically 1 ns, while power consumption is only 12 mW.

The AS Series, a combination of new high-performance 20 and 24-pin functions designed specifically for high-speed applications, will encompass the MSI arithmetic operators and supporting gate and flip-flop functions required to implement high-speed CPUs, controllers, processors, and more.

Advanced Low-Power Schottky

Featuring a typical 4-ns gate delay and 1-mW gate power dissipation, the new Advanced Low-Power Schottky (ALS) Series will consist initially of 75 popular device types currently in the LS Series, including gates, dual D and J-K flip-flops, and MSI functions.

In addition, the new ALS Series, with the same drive as today's popular LS Series, allows immediate plug-in to existing logic systems.

The ALS Series, offered initially in familar socket-compatible packages, will ultimately encompass more complex MSI products in the new 300-mil wide 24-pin DIPs.

Fully compatible

Both the new AS and ALS Series will be fully compatible with the 54/74, 54/74LS and 54/74S TTL Series, in both military and commercial temperature ranges.

The logical choice

Never before have designers had such a wide range of choices. Choices of compatible catalog functions that offer effective TTL solutions to state-of-the-art systems design.

Imagine...two new advanced Schottky TTL families...both offering twice the performance... one, half the power.

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Microcomputers & systems

Control system fits on chip

Preprogrammed version of Intel UPI-41A aims at industrial applications

The demand for speed and accuracy in modern industrial processing is generating a need for complex electronic components to do monitoring and control. These electronic components have been offered in a variety of configurations ranging from complete systems to single-board computers. Now an entire industrial control subsystem is available on a single integrated circuit.

The 40-pin iSBC 941 is called an industrial digital processor, or IDP. It is a preprogrammed version of the versatile UPI-41A universal peripheral-interface single-chip microcomputer having canned routines specifically tailored for industrial applications. The IDP is an 8-bit machine with 1 kilobyte of read-only memory, 64 bytes of random-access memory, and a pair of 8-bit programmable I/O ports.

The two ports give the user 16 independently programmable I/O lines that can serve as inputs for sensing and monitoring and as outputs for control. Thus, closed-loop systems can be realized with one or more IDPs. Some of the 16 lines may even be used as inputs and outputs in simplex serial communications to other stations. The table lists the nine industrial I/O functions that the IDP can perform in addition to those available through its general-purpose instruction repertoire.

When used as inputs, the lines will sense events through pulse, period, or frequency counting. This makes the IC ideal for limit-alarm detection, pulse counting for turbine control, and monitoring photodetectors on conveyer lines. As outputs, the lines can be programmed to be at a constant dc level or they can be pulsed to control such equipment as stepper motors.

The iSBC 941 IDP can also be used as a slave processor to perform these I/O operations via commands from a master. Up to three of the chips may be installed in the slave processor sockets provided on the iSBC 569 intelligent digital controller board [*Electronics*, June 7, 1979, p. 183]. The IDP can likewise be plugged into the iSBC 80/30 single-board computer or in fact any other 8080-, 8085-, 8086-, or 8048-based product that conforms to the UPI-41A's signals and control protocol.

The iSBC 941 industrial digital processor is available from stock at a single-unit domestic price of $150.

Intel Corp., 3065 Bowers Ave., Santa Clara, Calif. 95051. Phone (408) 987-8080 [371]

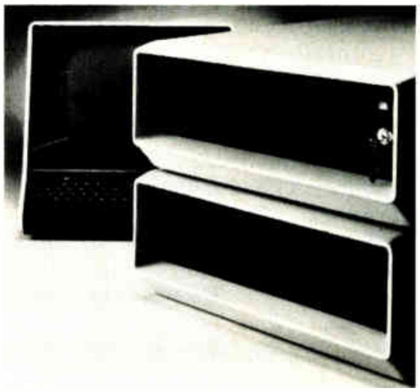
FUNCTIONS OF THE iSBC 941 INDUSTRIAL DIGITAL PROCESSOR

Mnemonic	Function
EVENT	Monitors up to eight input lines for event counting or for comparison with a preset count for each line.
FCOUNT	Measures frequencies up to 18 kHz on one of eight digital inputs over a programmable period.
FREQ	Generates up to eight gated-frequency outputs with separately programmable pulse width and period.
PERIOD	Measures the period of up to four inputs.
SCAN	Monitors up to 16 input lines for change-of-state and direction of change.
SERIN	Enables simplex reception of asynchronous serial data at rates up to 1,200 baud for communications applications.
SEROUT	Enables simplex transmission of asynchronous serial data at rates up to 1,200 baud.
SHOTI	Emulates a gated one-shot pulse generator.
STEPPER	Generates up to eight programmable outputs that may be used for the control of stepper motors.

8-bit microcomputer can process data at 7-MHz rate

The Centurion system is an 8-bit microcomputer that can process data at a rate of 7 MHz. Built around Intel's 8085A-2 microprocessor, it is to be used in small-business applications. It increases the 8085A-2's 5-MHz speed by using a floating-point math chip to handle numerous simple computations. The system has 16 kilobytes of internal programmable read-only memory, 64 kilobytes of random-access memory, a floppy-disk controller, and Digital Research Inc.'s CP/M operating system, all of them built on a shielded motherboard. The unit is compatible with any printer having an RS-232 interface.

The microcomputer is available in three configurations. The Centurion I comes with a 16-slot motherboard in a custom enclosure and includes a Hazeltine 1500 cathode-ray tube terminal (a 1420 is also available). In a separate housing, it has two Shugart 8-in. disk drives and a power supply. It sells for $10,825.



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Getting down to specifics.

"But advanced technology means little unless the instrument does the job for you. So both feature a basic bandwidth of 125 MHz with options to 1300 MHz. Each with manual or autoranging through all measurement modes.

Model	Resolution	Max. Sensitivity	Price
7260A	100 ns	10 mV	*$850
7261A	10 ns	10 mV	*$995

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EL 2/80

New products

The Centurion II has an 8-slot motherboard and two 8-in. disk drives, all housed in a single enclosure. It is priced at $9,500. The Centurion III, which sells for $8,025, has the 8-slot board and two 5.25-in. disk drives. Two more 8-in. drives with a power supply can be purchased for $2,500 total. The system is available from stock.

Artec Electronics Inc., 605 Old County Rd., San Carlos, Calif. 94070. Phone Robert Jones at (415) 592-2740 [374]

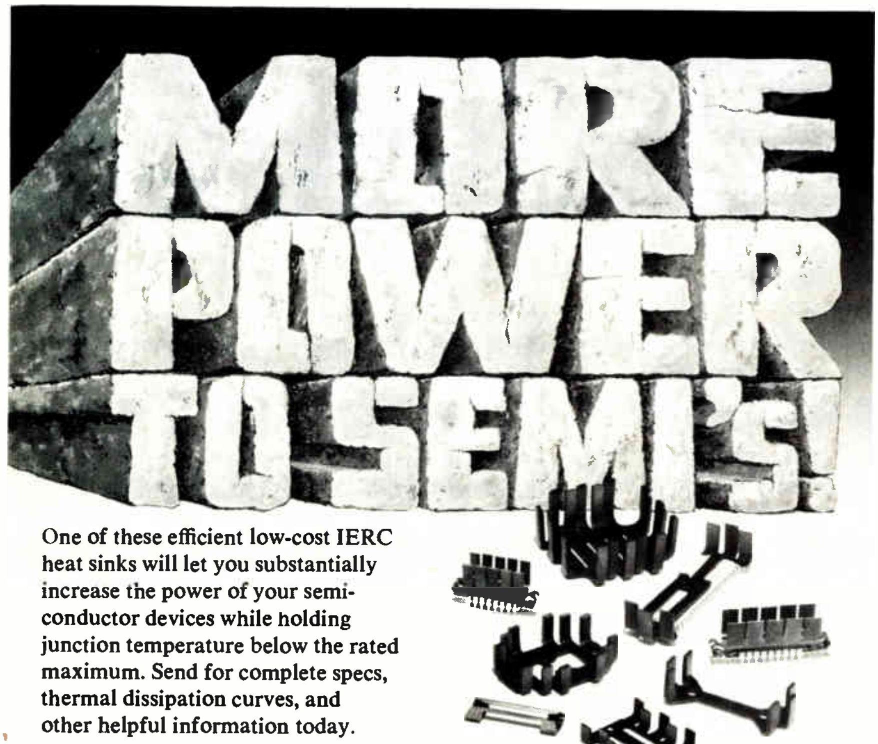
Development system made for Cosmac DOS

The CDP18S007 is a software-development system for Cosmac disk operating systems (CDOS) that uses the soon-to-be-announced CDP1804 microprocessor to operate at a 2.5-MHz clock rate. It contains 28 kilobytes of random-access memory, a dual-drive floppy-disk system, and a disk operating system. Additional software includes an editor, a Level II macro-assembler, and various diskette utility programs. The system comes with a 19-in. rack-mountable chassis with printed-circuit backplane; internal power supplies with a clock and controls; a front panel with controls and display; and plug-in modules such as a central processing unit, address latch and bank selector, control universal asynchronous receiver-transmitter terminal interface, disk interface, input/output decoder, and read-only or random-access memory. Standard 20-mA current loop and RS-232-C interfaces are provided. In single quantities, the system is priced at $9,500.

RCA Solid State Division, Box 3200, Somerville, N. J. 08876 [375]

Interface allows DMA block transfers among 255 LSI-11s

The model 11-0011 is a Q-bus–compatible interface that permits direct-memory-access block transfers between as many as 255 LSI-11 microprocessors at a 1-megabaud rate



over a single coaxial cable. It allows point-to-point and multidrop networks containing PDP-11/03s, LSI-11/2s, and LSI-11/23s to be set up.

The unit is packaged on two standard-sized half-quad boards that plug into all LSI-11 backplanes. Implemented in the hardware is a synchronous data-link control that serves as the interface's communications protocol. A coaxial cable modem incorporated on one of the half-quad boards functions as the data transmitter and receiver. The interface's wide dynamic range permits operation on coaxial cables up to 32,000 ft long.

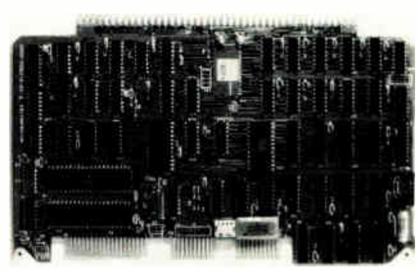
The 11-0011 sells for $970 each in quantities of 100. Delivery time is 30 to 60 days.

Computrol Corp., 15 Ethan Allen Hwy., Ridgefield, Conn. 06877. Phone (203) 544-9371 [376]

Single-card CRT controller is compatible with EXORcisor

The MCG 6800 is a single-card controller for color or black-and-white cathode-ray tubes that is bus-compatible with the EXORcisor. Fully compatible with the M6800, 6801E, and 6809E microcomputers, it operates at a 1-MHz rate. The unit provides 128 characters (upper- and lower-case) in a basic 80-character-by-24-line screen format. It has a 25th line for special command formats. It also contains an independent static random-access memory for display, control code, and graphics. Prices for the MCG 6800 controller start at $595.

Phoenix Digital Corp., 3027 N. 33rd Dr., Phoenix, Ariz. 85017. Phone (602) 278-3591 [377]



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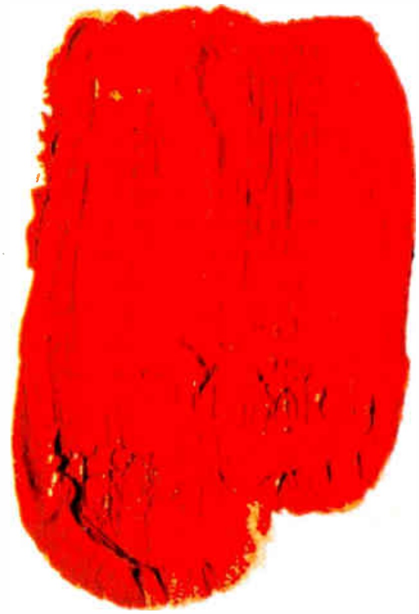

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Circle 203 on reader service card

Components

Drivers link logic to displays

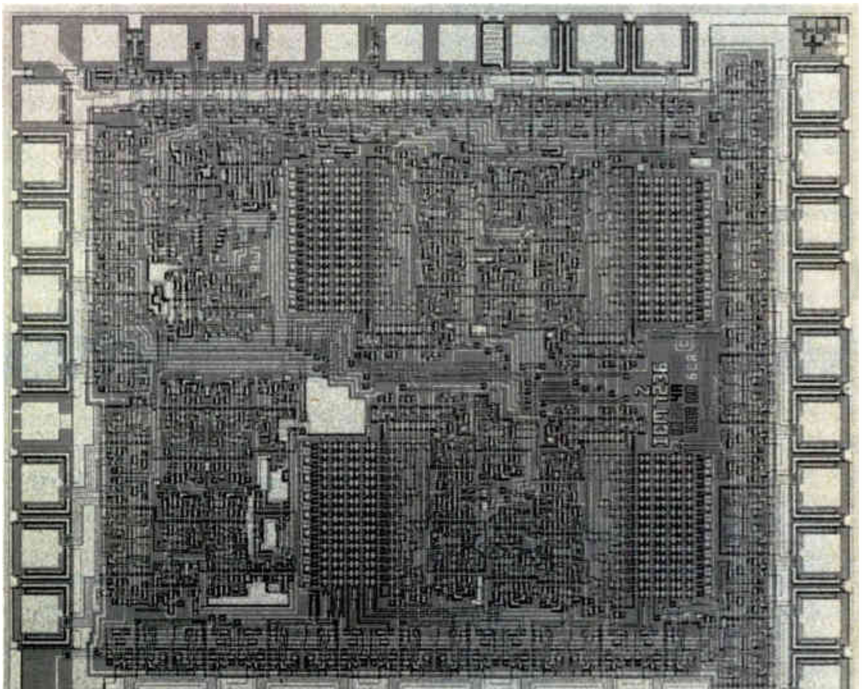
IC family for nonmultiplexed vacuum-fluorescent displays includes counting units

What with microprocessors and vacuum-fluorescent displays gaining popularity in a rapidly expanding number of industrial and commercial systems applications, equipment designers searching for a simple means of interfacing the two technologies need no longer look beyond Cupertino, Calif. That is where Intersil Inc. has developed a new family of display driver circuits that provide the user with a single-chip interface between digital logic or microprocessors and nonmultiplexed seven-segment vacuum-fluorescent displays.

Designated the ICM7235 family, the new complementary-MOS devices are available with multiplexed binary-coded decimal inputs or high-speed processor interfaces. There is also a choice of hexadecimal outputs or popular code B outputs—0–9, dash, E, H, L, P and blank. The new family, according to Murray Siegel, director, low-power products, "allows the designer to eliminate up to six TTL or C-MOS integrated circuits required with conventional vacuum-fluorescent display-driver circuits."

Each of the four chips in the family has 28 high-voltage open-drain p-channel transistor outputs organized as four seven-segment digits. The basic devices have four data-bit inputs and four digit-select inputs, a configuration that is suitable for interfacing with multiplexed BCD or binary output devices, Siegel notes. The microprocessor interface devices (suffix M) provide data input latches and digit-select-code latches under control of high-speed chip-select inputs. These devices "simplify the task of implementing a cost-effective alphanumeric seven-segment display for microprocessor systems, "without requiring extensive read-only memory or CPU time for decoding and display updating," Siegel says.

All devices in the ICM7235 family dissipate a maximum of 0.5 W at 70° C and are available in standard plastic 40-pin dual in-line packages at rated temperature ranges of −20° to +70° C. Their inputs feature display blanking and protection against static discharge. The nonmultiplexed driver design prevents the generation of interference. Targeted for applications such as microprocessor and analog-to-digital converter readouts, general digital systems, instrument display driving, and automobile information displays, the units are priced at $3.75 each in 100-unit quantities and are available from stock.



Meanwhile, Intersil is extending its single-chip display-driver expertise into counting systems applications with two C-MOS counter-driver chips that have 4½-digit capability and direct interface to nonmultiplexed vacuum-fluorescent displays. The ICM7236 decade counter provides a maximum count of 19,999, while the ICM7236A has a maximum count of 15,959 and is intended for timing purposes. Both chips include on-chip decoders, output latches, count inhibit, reset, and leading-zero blanking circuitry, as well as 29 high-voltage open-drain p-channel transistor outputs.

The counter section of the two devices provides direct static counting from dc to 15 MHz guaranteed (with a 5-V ±10% supply) over the operating temperature range of −20° to +70°C. At room temperature the devices will typically count up to 25 MHz. According to Siegel, count input is provided by a Schmitt trigger for operation in noisy environments or for correct counting with slowly changing inputs. What's more, the devices incorporate features that are intended to simplify cascading in four-digit blocks. For example, the carry output allows the counter to be cascaded, while the leading-zero-blanking input and output allow correct leading-zero blanking between four-decade blocks.

Both the ICM7236 and 7236A dissipate a maximum of 0.5 W at 70° C and are packaged in standard 40-pin plastic DIPs. Priced at $4.25 each, in 100-unit quantities, they are

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2. Choose synchronous or asynchronous sampling. Use the clock of the system under test or the 308's own internal clock. In either case, sampling rates up to 20 MHz are possible.

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4. Press "start" and you're done. Now, you can view the acquired data in the format you want. Or, store the data in the reference memory by pressing the "store" key. Other function keys allow you to acquire new data and compare it with the reference memory.

In each data acquisition mode, all measurement parameters are displayed for your convenience.

Minimum keystroking with the new 308 Data Analyzer from Tektronix.

Of course, the 308 Data Analyzer can do a lot more than we've shown here. For example, there's a self-test routine at power-up, plus seven diagnostics, to ensure accurate results. And the 308 weighs only 8 pounds (3.6 kg), for easy portability.

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designed for applications such as counting instrumentation, automobile tachometers and speedometers, and laboratory timers.

Intersil Inc., 10710 N. Tantau Ave., Cupertino, Calif. 95014. Phone (404) 996-5000 [341]

400-V, 6-to-30-A rectifiers recover in 100 ns

The 1N3879 through 1N3913 diffused-junction silicon rectifier diodes for motor controls, dc-to-ac inverters, and high-frequency rectifiers have a typical reverse recovery time of 100 ns. Encapsulated in DO-4 or DO-5 stud-type hermetic packages, they have voltage ratings of up to 400 V and average current ratings of 6, 12, 20, or 30 A.

Prices vary with specifications. For example, a model 1N3883, which has a 6-A average forward current, goes for $2.14 each in lots of 100. In the same quantities, a 30-A version—the model 1N3913—is priced at $4.32 each. Delivery is from stock to six weeks after receipt of order.

Ferranti Electric Inc., Semiconductor Products, 87 Modular Ave., Commack, N.Y. 11725. Phone (516) 543-0200 [344]

LED bar modules radiate 160 cd/m² at 20 mA dc

The HLMP-2600, -2700, and -2800 series of light-bar devices are composed of four or eight light-emitting diodes whose light is optically scattered to evenly backlight annunciator messages that have large surface areas. Because the anode and cathode of each LED are brought out to

Extend your storage capabilities beyond the conventional.

Now Gould offers a range of digital storage oscilloscopes that offer a world of advantages over conventional tube storage technology, beginning with being able to capture transient of "one-time" events and store them indefinitely for display or hardcopy printout. This makes them ideal for electronic, electromechanical, educational, and biophysical applications.

Both the OS4000 and the new OS4100 combine the capabilities of semi-conductor memory with a bright, stable, flicker-free display. This technique allows analysis of signal build-up and decay characteristics through pre- and post-trigger viewing. Expansion of the display after storage permits detailed study of specific areas of the trace.

The new model—OS4100—also offers you stored X-Y displays, channel sum or difference and a maximum of 100 V per cm sensitivity with noise suppression. A unique trigger window circuit assures capture of transients of unknown polarity.

Other outstanding features include automatic operation, display of stored and real time traces simultaneously and hard copy memory output in digital or analog form. And IEEE488 is available for compatible interfacing.

And, remember that Gould scopes are backed by a two-year warranty of parts and labor, exclusive of fuses, minor maintenance and calibration. For further information, contact Gould Inc., Instruments Division, 3631 Perkins Ave., Cleveland, Ohio 44114. Or Call (216) 361-3315, Ext. 395, for a demonstration.

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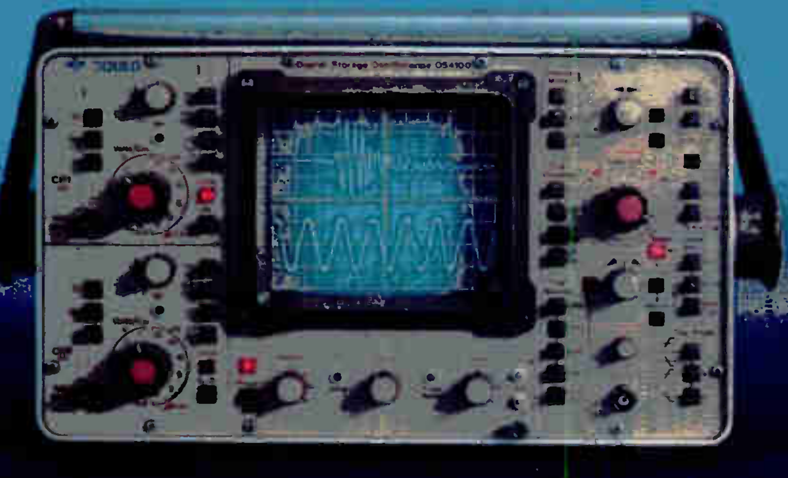

Circle 207 on reader service card

Circle 208 on reader service card

separate pins, the LEDs within a device can be wired in parallel, series, or a combination of the two. Typical luminance is 160 cd/m² at an average dc forward current of 20 mA under pulsed conditions. The radiation pattern is approximately Lambertian. Six different package fonts are available, with multiple or continuous rectangular surfaces. Square units measure 8.89 mm a side, and rectangular units measure 8.89 by 19.05 mm; both have a profile of 6.096 mm.

The HLMP-2600 series are red modules, the -2700 are yellow, and the -2800 are green. They come in dual in-line packages that can be stacked in an X-Y form and are compatible with integrated circuits. In quantities of 1,000, the square modules are priced at $1.75 each and the rectangular packages at $2.56 each. The devices all are available from stock.

Hewlett-Packard Co., 1507 Page Mill Rd., Palo Alto, Calif. 94304 [343]

$365 CRT display does 50,000 horizontal scans/s

The VR-800 raster-scan display module performs 50,000 horizontal scans per second to display a full page of typewritten text with 66 lines of up to 96 characters each. The open-frame module uses a 15-in. (diagonal) cathode-ray tube in a vertical position and contains all its circuitry on a single board. The entire module measures less than a cubic foot and displays five-by-seven-dot black characters on a white background. The raster consists of 800 noninterlaced scan lines: 600,000 dots, each less than 8 mils in diameter.

The unit has rise and fall times of less than 4 ns; linearity distortion is less than 3%. In 100-unit quantities, the display sells for $365 each and will be delivered in 30 to 40 days. Each unit has a power requirement of 42 to 48 V dc.

Moniterm Corp., 250 North Central Ave., Wayzata, Minn 55391. Phone (612) 475-1106 [345]

When the Doctor heard we were famous for our custom work, he wanted to order a bride for Frankie.

Sorry Doc. It's custom MOS/LSI.

Match-making is a little out of our line. But we *have* come up with quite a few original creations. For custom MOS/LSI circuits.

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Standard Microsystems provides a total capability. We design, develop, process, assemble and test state-of-the-art MOS/LSI circuits. That means we can design from scratch, or enter the custom cycle at any point you want. And assisting us at every step is the latest computer-aided design and diagnostic equipment.

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Level measuring range	−120 to +30dBm
Level measuring accuracy	±0.1dB (10kHz to 13MHz, −80 to 0dBm)
Frequency stability	$\leqq 1\times10^{-5}$ (0 to 45°C)
Input impedance	75Ω, 135Ω, 150Ω, 600Ω (High)
Bandwidth	40Hz, 1.74kHz
Dimension/Weight	195(H)×426(W)×350(D)mm/ $\leqq$16kg

For comprehensive literature on the Selective Level Meter ML422A, contact—

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Circle 210 on reader service card

ATEC Points the Way

A simple solution to shorts and opens inspection of loaded boards.

The Series 55: Improves throughput at in-circuit and functional test levels

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Inspects populated boards in seconds, relieving congestion and increasing throughput at in-circuit and functional test—without tying up expensive personnel and high cost equipment.

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Circle 211 on reader service card

Communications

Coaxial cable takes a beating

Armored assemblies resist crushing, survive pull loads in excess of 150 lb

No one taking television pictures from a helicopter wants to drop his camera and retrieve it by pulling on its electrical cable. But it's nice to know that it would be possible—as it could be if the cable was Trompeter Electronics' new stainless steel armored coax.

Designed to survive such calamities as cameramen slamming car doors on them or having cars run over them—not uncommon occurrences in the broadcast industry—the new coaxial cable assemblies have been informally tested under tension loads of up to 300 lb and are formally rated at half that—150 lb.

Being run over by a cement truck does not affect the cables' electrical characteristics although it may demolish their easily replaced connectors. These electrical characteristics include nominal impedances of 50 Ω and 75 Ω and attenuations (at 10 MHz) of 1.6 dB per 100 ft for the 50-Ω cable and 1.8 dB per 100 ft for the 75 Ω one. At 100 MHz, the 50-Ω cable has an attenuation of 6.9 dB per 100 ft and the 75-Ω cable is rated at 5.7 dB/100 ft. A 10-ft assembly of 75-Ω cable weighs only 13 oz.

Pricing on the armored cable, which is typically supplied with wrench-crimped BNC connectors, depends upon length, impedance, and cable size. A typical 10-ft section sells for $99.50 and can be delivered in four to six weeks.

Trompeter Electronics Inc., 8936 Comanche Ave., Chatsworth, Calif. 91311. Phone (213) 882-1020 [401]

Devices encrypt stored and communicated data

Two data-encryption devices that meet the National Bureau of Standards' data encryption standard ensure the security and privacy of both stored and communicated data. The DataLock units use the standard RS-232-C interface, so no software or hardware modifications are

needed to place one in the communications path between a user's terminal and the computer. The DataLock 150 is controlled by the user through his computer terminal, whereas the DataLock 250 can accept commands from both the terminal and the computer and may be shared by different users and systems utilities.

When not in the security mode, the DataLock units have no effect on system operation. They may be used with any asynchronous protocol. A version that can be used with IBM's Binary Synchronous Communications protocol (Bisync) will be available April 1. The DataLock's baud rate is switch-selectable, from 110 to 9,600 bauds. In single quantities, each DataLock 150 sells for $2,390, and each 250 sells for $2,950. Delivery takes four weeks.

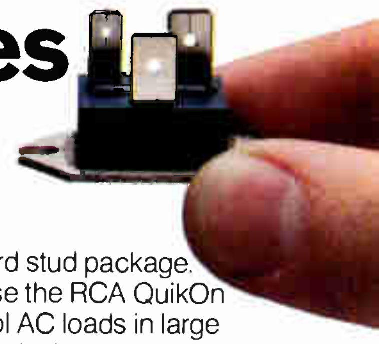
SPI Data Systems Inc., 488 Cowper St., Palo Alto, Calif. 94301. Phone (415) 328-5183 [403]

LSI frequency synthesizers sell for $4.95 to $8.15

The manufacturer of two frequency-synthesizer integrated circuits hopes that the devices and five more ICs to be introduced this year will foster the implementation of phase-locked-loop circuitry in equipment that still relies on tuned circuits and multiple crystals. Motorola Semiconductor Products feels that the lower price and off-the-shelf availability of the devices may encourage a change in the architecture of much of the equipment currently used for radio-frequency communications.

The new silicon-gate complementary-MOS ICs have a typical frequen-

Easy to mount. Easy to connect. The RCA 25 amp triac comes in a rugged new package.



Our new QuikOn triac package is designed for high-speed assembly line installation.

Top side terminals let you do all your mounting from one side, with fast self-tapping sheet metal screws. The device can handle 300 amps surge current. 2500 volts isolation from any terminal to flange makes isolation hardware unnecessary.

Plus, we used quick-connect terminals that let you use solderless snap-on connectors.

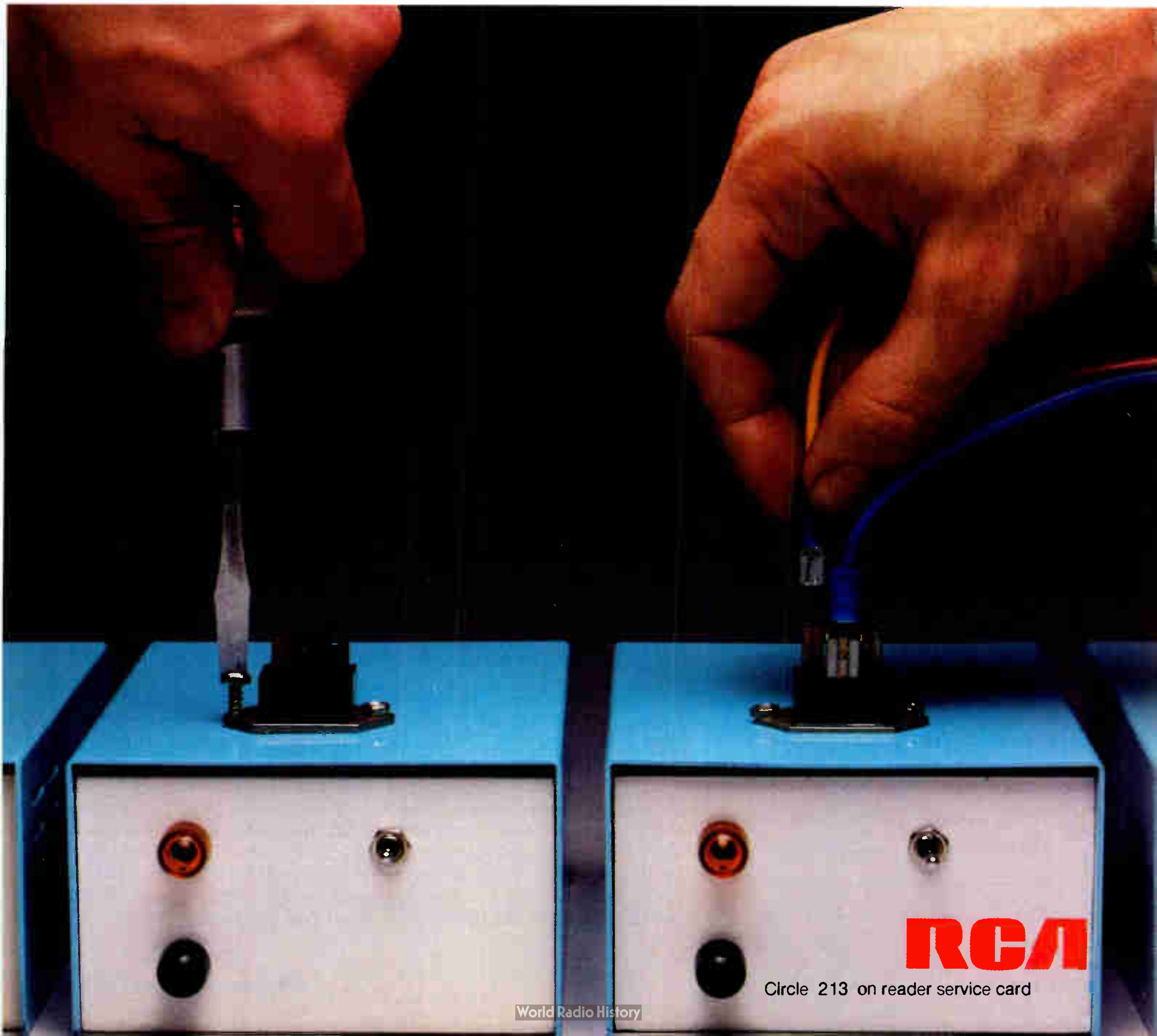
All of which can add up to lower assembly costs than with conventional stud packages.

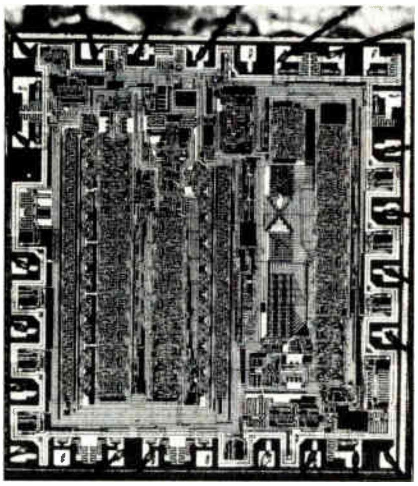
We've kept the price down too, by using a glass passivated chip in a molded plastic package. And there's no loss of reliability compared to the standard stud package.

You can use the RCA QuikOn triac to control AC loads in large appliances and other types of high current equipment.

For more information, contact your local RCA Solid State Distributor.

Or RCA Solid State headquarters in Somerville, N.J. Brussels, Belgium. Tokyo, Japan.





cy range that extends beyond 25 MHz. The models MC145155 and MC145156 are programmed by a clocked, serial-input bit stream. Like other ICs in the family, these devices feature a crystal reference oscillator, a reference divider, a digital phase detector, and lock-detection circuitry. The MC145155 contains a 14-bit programmable divide-by-N counter. The MC145156 contains a 10-bit and a 7-bit counter for the programmable divide-by-N counter and on-chip control logic that works with external dual-modulus prescaling ICs to expand this device's frequency range to 500 MHz.

The MC145155, in a plastic dual in-line package, sells for $4.95 each; in ceramic, it is $7.43. The MC145156 in plastic is $5.43; in ceramic, it is $8.15.

Motorola Semiconductor Products Inc., P. O. Box 20912, Phoenix, Ariz. 85036. Phone Doug Tashiro at (512) 928-6899 [404]

Pair of optical data links for microprocessors is $455

The model 5010-series Optodata is a complete infrared optical communication system for microprocessors and microcomputers. A pair of the units placed between computer terminals will provide two-way transmission of data for other serial binary devices, controls, and instruments.

A light-emitting diode serves as the source of a 9,000-Å modulated beam that carries digital information at rates of up to 2,400 b/s for a distance of 100 m. A patented gain control automatically compensates for ambient light changes, whether indoors or out. Available versions have 25-pin EIA connectors, switch selection of sending and receiving lines, power switches, plugs, and 20-mA current-loop operation. The system operates on 117 or 230 V ac, but battery operation (at 12 or 24 V dc) is available as an option.

Optodata is priced at $455 per transceiver pair for the ac version and at $395 a pair for the 12-V dc version. Delivery takes two weeks.

Scientific Radiation Corp., 1201 San Antonio Rd., Mountain View, Calif. 94043. Phone Mark Evans at (415) 965-0910 [405]

Slow and fast facsimile machines are compatible

The various members of a family of digital facsimile transceivers transmits documents over ordinary voice-grade telephone lines at different rates, yet all are compatible. The Rapicom 1500, 1000, and 800 join the Rapicom 1850 in the Rapinet family of machines that automatically answer incoming telephone calls and receive messages as well as feed and send 50 documents at a time. The 1850, which has been available for about six months, transmits at a rate of 9,600 bits per second. Like the 1850, the 1500 and 1000 imprint the date, the time, and the sender's address on each transmitted document.

The 1500 will handle legal-sized documents; it transmits a normal business letter in 30 seconds with a resolution of 67 by 200 lines/in. The unit may be switched to operate at speeds compatible with the 1000—which sends a letter in either 45 or 90 seconds—and with the 800, which operates at even slower speeds but with higher resolution.

In single-unit quantities, the Rapicom models are $6,500 for the 800, $7,350 for the 1000, $9,600 for the 1500, and $13,350 for the 1850.

Rapicom Inc., 2475 Augustine Dr., Santa Clara, Calif. 95050 [406]

MOSTEK MILITARY UPDATE

WORLD'S LEADING 16K DYNAMIC RAM RECEIVES QPL CERTIFICATION.

Now you can order a fully JAN qualified 200ns dynamic RAM from the world's leading supplier of dynamic RAMs. It's from Mostek, of course. Designated M38510/24001BEC, this 16K x 1 device is JAN specified over a −55°C to 110°C operating case temperature range and is available in a high density 16-pin hermetic dual-in-line package. Order now for June delivery from your authorized Mostek distributor.

The M38510/24001BEC is just one of the memory components from a full line of the densest and most advanced military memories available today—memories screened to MIL-STD 883B, methods 5004.4 and 5005.5. Besides dual-in-line packaging, Mostek Military offers high density, hermetic leadless chip carriers and flat packages as well.

It's all part of a long-range commitment from Mostek's Military Products Department. Their charter: To create state-of-the-art high density memory products exclusively for the military marketplace.

For more information, write: Mostek, 1215 West Crosby Road, Carrollton, Texas 75006. Or call (214) 323-6000. In Europe, contact Mostek Brussels; phone 660.69.24.

	Mostek Military Products	Organi-zation	Temperature Range	Access Time	Active Power	Standby Power
JAN DYNAMIC RAMS	M38510/24001BEC	16K x 1	−55°C to 110°C*	200ns	462mW	30mW
	M38510/24002BEC	16K x 1	−55°C to 110°C*	250ns	462mW	30mW
DYNAMIC RAMS	MKB 4116-93	16K x 1	−55°C to 93°C	200ns	462mW	30mW
	MKB 4116-83	16K x 1	−55°C to 85°C	200ns	462mW	30mW
	MKB 4116-84	16K x 1	−55°C to 85°C	250ns	462mW	30mW
	MKB 4027-83	4K x 1	−55°C to 85°C	200ns	467mW	40mW
	MKB 4027-84	4K x 1	−55°C to 85°C	250ns	467mW	40mW
STATIC RAMS	MKB 4104-84	4K x 1	−55°C to 125°C	250ns	150mW	53mW
	MKB 4104-85	4K x 1	−55°C to 125°C	300ns	150mW	53mW
	MKB 4104-86	4K x 1	−55°C to 125°C	350ns	150mW	53mW
ROMS	MKB 36000-83	8K x 8	−55°C to 125°C	250ns	220mW	55mW
	MKB 36000-84	8K x 8	−55°C to 125°C	300ns	220mW	55mW
EPROMS	MKB 2716-78	2K x 8	−40°C to 85°C	450ns	633mW	165mW

*Case operating temperature range

MOSTEK.

Circle 142 on reader service card

There's no body like our new ZOOM BODY

The new AO STEREOSTAR¾ Zoom "T" microscope features the "T" zoom body with coaxial illumination and photo capabilities. It may be just what you need to boost output in your production, assembly or inspection department.

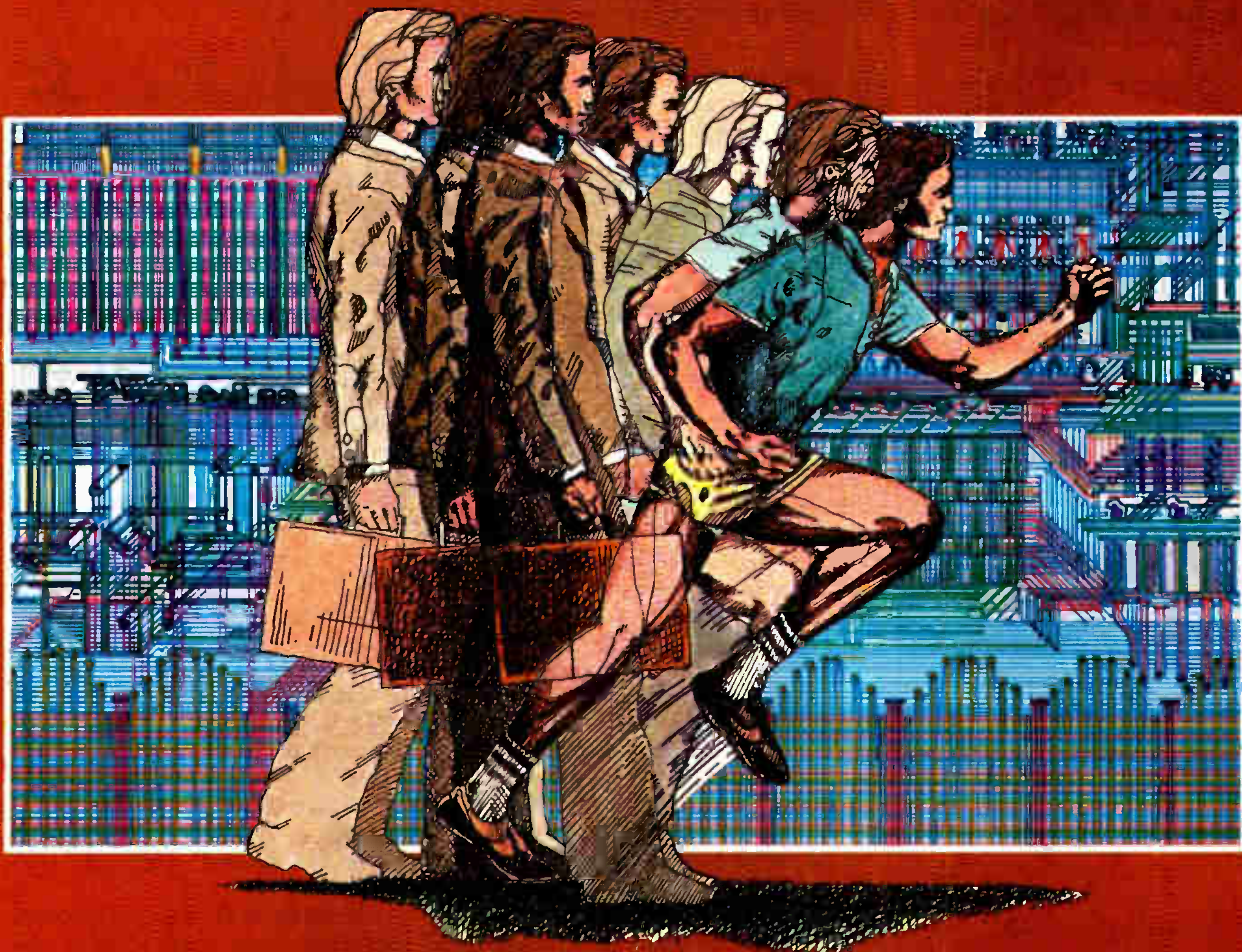
The Zoom "T" gives you a constant 4" of working room. It has a 1x - 6x magnification range, and with auxiliary lenses and eyepieces it offers a total range of 5x - 300x. Magnification can be conveniently changed with controls on both sides of the body. No matter what magnification you're working with, you get crisp, sharp image definition.

Modular in construction, the Zoom "T" can be ordered with or without the coaxial illuminator. In fact, any accessory can be simply added at any time. However, if you're working with highly reflective opaque surfaces, coaxial illumination is invaluable because it gives contrast without hot spots, glare, reflections or shadows.

We invite you to compare the new AO STEREOSTAR Zoom "T" microscope, feature by feature, with any other competitive microscope.

We're confident you'll immediately see that it offers the outstanding value in its field. See your AO dealer or representative for a demonstration. Or write for a detailed brochure. American Optical, Scientific Instrument Division, Buffalo, NY 14215.

AO® American Optical



Instruments

Power analyzer tests for years

Portable analyzer measures average power consumption over long periods of time

Since both buyers and sellers of electrical goods are more energy-conscious than ever before, some manufacturers are beginning to provide figures on how much power their products normally consume. Magtrol Inc. of Buffalo, N. Y., has decided to address this potentially lucrative market with an instrument that can measure average power consumption for long periods.

The company's model 4612 portable power analyzer is a volt-ampere-wattmeter that lets the operator integrate those parameters for hours, weeks, months, or even years if need be. After connecting the power lines to the appropriate connectors on the rear panel and setting the range on the front, the user presses the display-hold button on the front panel. This freezes the display and prepares the meter for averaging. Then, when he wants the averaging period to start, he or she need only press an averaging start/stop button. The instrument then takes samples at intervals of approximately 400 ms until the averaging button is again pushed.

Pushing the button causes the five-digit watt display to show first the number of samples taken for about 1½ seconds and then the integration time, in seconds, for approximately 5 seconds. Display resolution limits the validity of these figures to integration times of 11 and 28 hr, respectively, but does not affect the integration results. Those results come up last, with the average voltage and current on separate four-digit displays and the average power on the five-digit display.

The analyzer will perform either dc or true rms ac averaged, as well as unaveraged, measurements. Voltage ranges of 15, 30, 150, 300, and 600 V and current ranges of 2, 5, 10, 20, and 50 A are selectable. Accuracy varies with range, but it is within approximately ±(0.25% of reading + 0.25% of full scale) ±1 digit for ac readings from 40 to 100 Hz. Ac readings from 100 to 500 Hz or dc readings add ±5 digits to that figure.

According to Dick Traise, product marketing manager for Magtrol, this averaging feature is unique. "You'd have to gimmick up some Rube Goldberg arrangement at maybe $15,000 to do what this compact instrument does for about $2,200," he claims. To provide that feature,

Why pay 81¢ for a Hall effect sensor when you can get one for $2.21?

It all depends on your application.

For 81¢,* you can get a solid state Hall effect sensor from the people who invented it. Us.

And that may be all you need.

But, if your application requires precision, our fully engineered $2.21* position sensor may be a better deal.

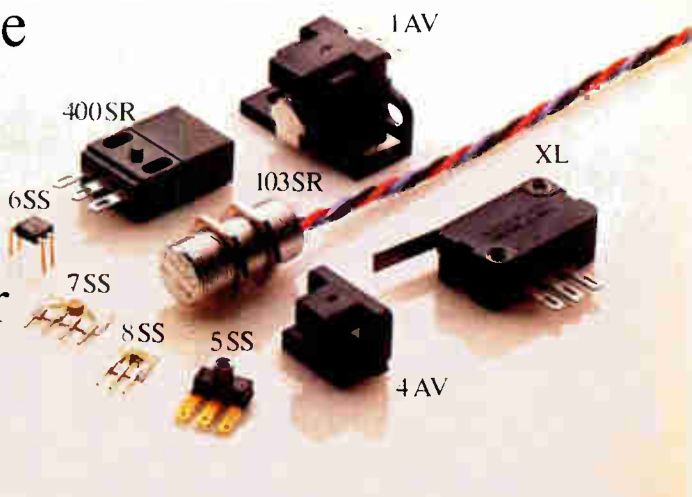
The Hall effect sensor and magnet are matched and adjusted to get operate and release points that are specified to tight tolerances.

All this can add up to a lot if you start out with the wrong sensor.

When you come to MICRO SWITCH, you're dealing with people who have made over 100 million Hall effect sensors. So you get experts to help fit each sensor to your application. And you always get the right sensor for the job.

Which means a $2.21 sensor can turn out to be a lot better deal than one that costs 81¢.

For details, and the location of our sales offices and distributors around the world, write MICRO SWITCH, The Sensor Consultants. Freeport, Illinois 61032. Or call 815/235-6600.



MICRO SWITCH
a Honeywell Division

*One thousand piece pricing for 7SS and XL Series devices, respectively.

Circle 219 for Data

Magtrol engineers turned to a National MM57109 number cruncher, "which gives us extensive math capability with minimum software design," Traise explains.

Part of the COPS family, the MM57109 is a MOS digit-oriented microprocessor, built by National with scientific calculators primarily in mind. In the power analyzer, it is used in a stand-alone configuration with two program counters and a UV-light–erasable PROM. The processor accepts instructions in reverse Polish notation, so that it is an easy matter to change the meter's operating program and burn a new PROM.

Magtrol will investigate such alterations at the purchaser's request, and will also provide a binary-coded decimal or analog interface for external data logging. Delivery time on standard units is eight weeks.

Magtrol Inc., 70 Gardenville Pkwy W., Buffalo, N.Y. 14224. Phone (716) 668-5555 [351]

Selective level meter covers 50 Hz to 32.5 MHz

Essentially a microprocessor-controlled synthesizer-based receiver, the model 3586C selective level meter measures signal levels from −120 dBm to ±20 dBm with 0.01-dB resolution from 50Hz to 32.5 MHz. The instrument is accurate to within 0.2 dB over the range from 10 kHz to 18 MHz and down to −80 dBm. The measurement bandwidth is user-selectable to be 20, 400, or 3,100 Hz.

The unit can be operated from the keyboard or remotely, using an IEEE-488 interface bus. Selective measurements with 50-dB rejection on signals as close as 80 Hz may be obtained using the standard 20-Hz

THE MULTIPLE CHOICE TESTER

THE NEW PRODIGY PT900 SYSTEM FROM 3H INDUSTRIES TESTS:

- ☐ Power Supplies
- ☐ Relays
- ☐ Transformers
- ☒ All of the above

Our PRODIGY PT900 Power Supply Test System provides multiple answers to your test requirements in Production Testing, Incoming Inspection and Engineering Evaluation.

The complete turn-key system provides a PDP 11/3 computer with two floppy disks, a video terminal with keyboard, and programmable modules for testing power supplies, relays, transformers, regulators or batteries.

Proven software packages in PASCAL allow complete software control, using your choice of three programming methods: existing 3H proven test programs, primitive commands, or your own new test procedures written in simple testing language. You won't require a staff programmer as the system features operator prompting, making it very easy to use.

The PRODIGY is not only the fastest power supply tester available, it is also the most versatile. The modular design of the PRODIGY makes it simple for you to expand your system to meet specific individual requirements.

The PRODIGY Multiple Choice Tester is the answer to your testing requirements. It's built with the same reliability that makes our linear test systems the most accepted in the world. For further information, contact one of our offices listed below.

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32129 Lindero Canyon Road
Suite 210
Westlake Village, CA 93161

3H ELECTRONICS INC

Circle 221 on reader service card

filter. A 3,100-Hz filter that provides 75 dB adjacent-channel rejection is available.

The meter can store nine front-panel settings for fast repetitive testing. It sells for $9,100.

Hewlett-Packard Co., 1507 Page Mill Rd., Palo Alto, Calif. 94304 [353]

No-frills digital VOM sells for $89.95

Intended to replace the traditional volt-ohm-milliammeter, the LX 304 is a 3½-digit multimeter that measures ac and dc voltage, dc current, and resistance. It also has diode and transistor testing capability and a built-in low-battery indicator. The rugged hand-held unit has a basic dc-voltage uncertainty of 0.5%.

The meter's half-inch liquid-crystal display draws little power, giving the instrument a typical battery life of six months in normal operation. The LX 304 sells for $89.95.

The Hickok Electrical Instrument Co., 10514 Dupont Ave., Cleveland, Ohio 44108. Phone (216) 541-8060 [355]

Automatic analyzer measures distortion down to 0.005%

Capable of measuring total harmonic distortion down to 0.005% (0.003% typical), the model 6801 automatic distortion analyzer oper-

NORPLEX® POLYIMIDE-BASE LAMINATES

help you achieve high performance and greater yield.

Norplex G-30 laminates and prepregs are premium grade high-temperature base materials using polyimide resin with glass fabric reinforcements.

Developed for use in high-performance printed wiring boards and multilayer circuitry, G-30 polyimide laminates make possible design concepts that cannot be attained with epoxy-base materials. Because of their stability during fabrication and higher operating temperatures, these Norplex laminates are especially suited for microelectronics and guidance systems, computer logics and communications equipment.

Norplex G-30 laminates and prepregs have been approved and listed as qualified products for the military specifications MIL-P-13949E, MIL-P-55617B and MIL-G-55636B.

Other advantages of G-30 laminates and prepregs are their excellent X- and Y-axis dimensional stability, low Z-axis expansion, moisture resistance and outstanding electrical characteristics.

Technical information and assistance is available on these and other laminates from the Norplex Technical Service Department.

Norplex Division, UOP Inc., 1300 Norplex Drive, La Crosse, WI 54601. 608/784-6070. European Headquarters: Wipperfürth, West Germany. Pacific Headquarters: Kowloon, Hong Kong.

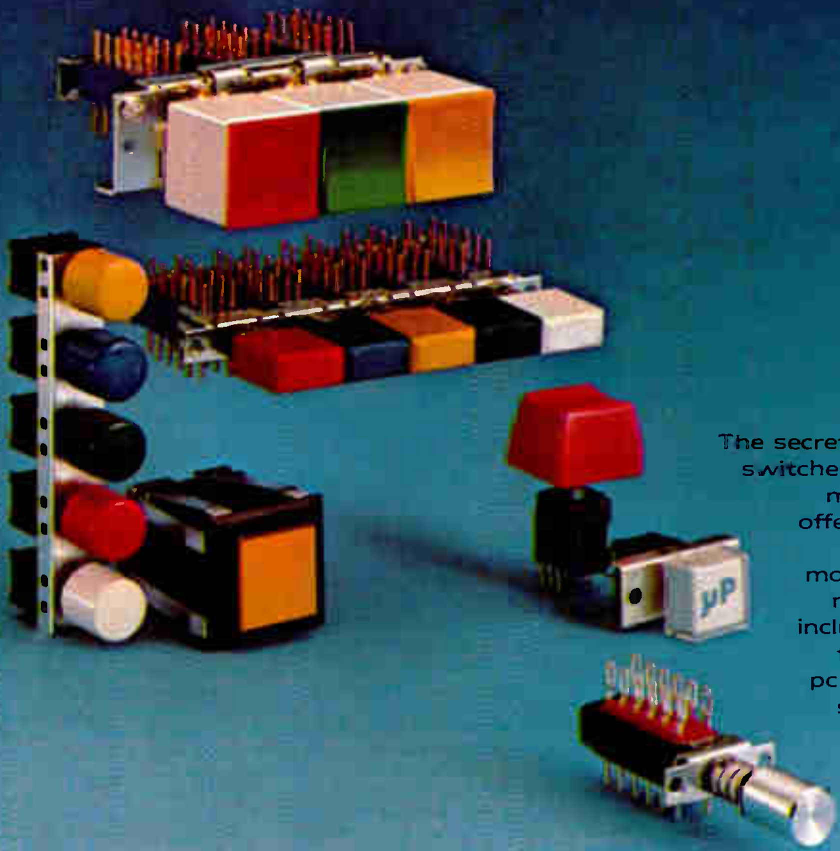
Norplex laminates by UOP

One of The Signal Companies

Circle 223 on reader service card

The foremost solution
to switch design flexibility...

Modular Pushbutton and Key Switches *from* CENTRALAB



The secret to widening your choice of pushbutton switches is the unusual flexibility of Centralab's modular pushbutton switch systems. We offer the versatile PBS Series for horizontal mounting; the MPS Series for vertical mounting. Our long list of options help you meet the most demanding requirements, including microprocessor applications. You'll find lighted and non-lighted switches for pc board or snap-in panel mounting; single station or ganged assemblies with 10 to 25mm spacings; 2-4-6 or 8 pole designs for push-push, push-pull, momentary or interlocking operation with lockout options; silver or gold contacts; epoxy sealed terminals; and a variety of switch housing materials. An outstanding choice of other options includes buttons, colors, lenses, filters and legends.

One feature of Centralab pushbutton switches that's not an option is our outstanding service. A nationwide network of Pushbutton Switch Distributors offers custom assembly and fast delivery of standard switches and options. And there's a Centralab Representative near you, ready to supply application help with your design.

Discover why the foremost source for switches is Centralab. Call your Centralab Distributor, Sales Representative or write Centralab Electronics, Division Globe-Union Inc., 5757 North Green Bay Avenue, P.O. Box 591, Milwaukee, Wisconsin 53201.

Circle 224 on reader service card

ates from 10 Hz to 110 kHz with 0.001% resolution. Automatic level setting allows the instrument to accept inputs from 100 mV to 13 V rms with no user interaction. Another automatic feature nulls out the fundamental frequency to further simplify operation.

The 6801 provides a distortion output for visual inspection or spectral analysis of the input signal after the fundamental has been filtered out. It also provides a low-distortion (0.003%) sine wave output for use as a standard in the determination of circuit or system distortion. A third analog output is a dc voltage proportional to the displayed percentage reading.

Priced at $1,600, the analyzer has a delivery time of 60 days.

Krohn-Hite Corp., Avon Industrial Park, 255 Bodwell St., Avon, Mass. 02322. Phone Ernie Lutfy at (617) 580-1660 [356]

Fast pulse generator delivers up to 5 kV

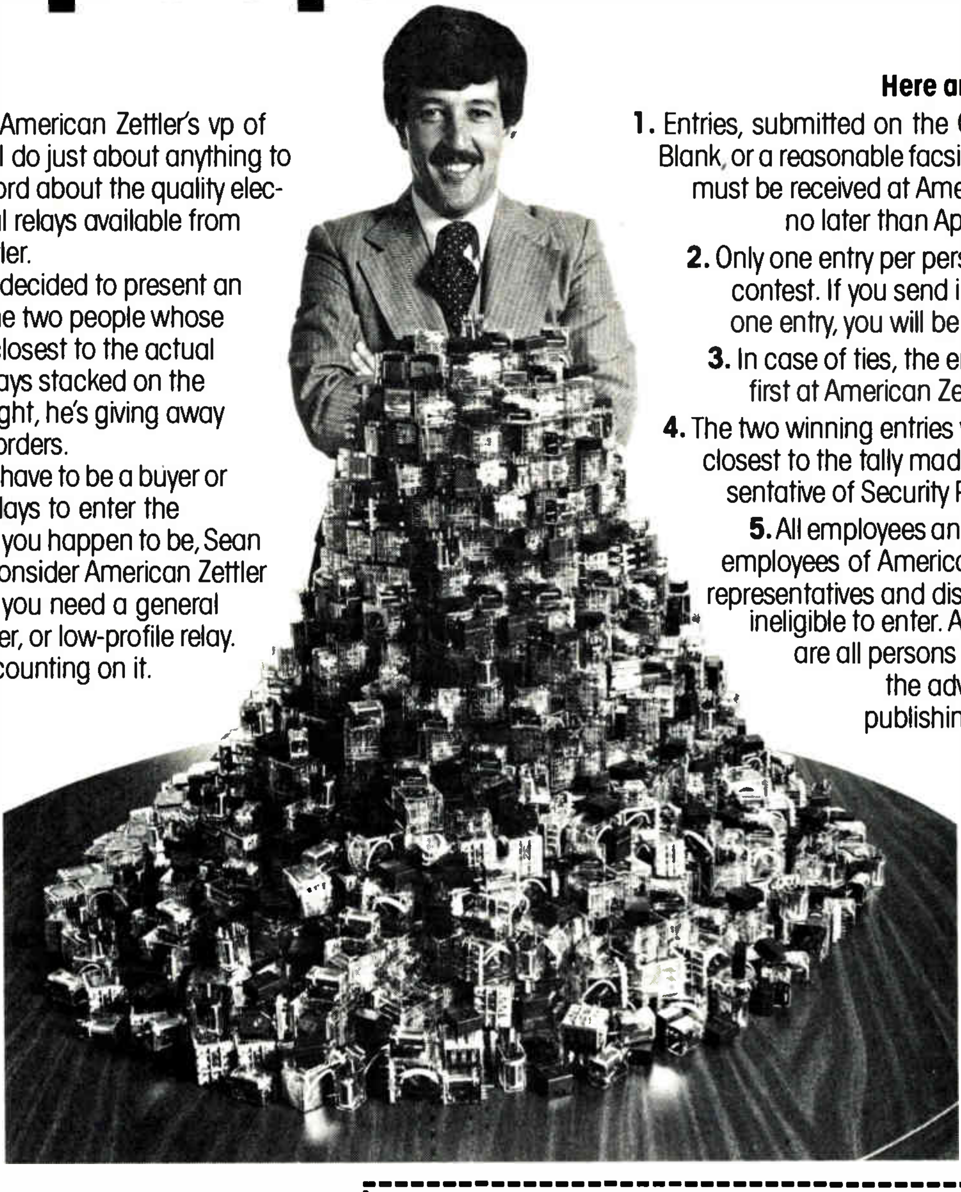
The model 7540 pulse driver is a high-voltage instrument whose repetition rate can be adjusted up to 100 kHz and whose separate positive and negative outputs can each be set as high as 2.5 kV for a peak-to-peak output of 5 kV. The instrument has no duty-cycle limitation, hence the pulse width may be varied from 0 to 10 μs at any pulse repetition rate all the way up to the 100-kHz maximum.

Designed to drive modest capacitive loads, the 7540 delivers pulses with rise and fall times of 100 ns or less when working at full output into a 50-pF load. It features delay times variable from 1 ns to 1 ms, pulse repetition rates as low as 10Hz, and digital display of pulse amplitude.

Single-output versions are available as are computer-controlled models. The pulsers fit into a standard 19-in. rack, weigh about 33 lb, and sell for between $5,000 and $7,000.

Rofin Inc., Echo Bridge Office Park, 381 Elliott St., Newton Upper Falls, Mass. 02164. Phone (617) 527-4884 [357]

Win an RCA Video Cassette Recorder. Tell Sean how many relays are on the table.



Sean Tierney, American Zettler's vp of marketing, will do just about anything to get out the word about the quality electromechanical relays available from American Zettler.

Now he's decided to present an RCA VCR to the two people whose entry comes closest to the actual number of relays stacked on the table. That's right, he's giving away two video recorders.

You don't have to be a buyer or specifier of relays to enter the contest. But if you happen to be, Sean hopes you'll consider American Zettler the next time you need a general purpose, power, or low-profile relay. Actually, he's counting on it.

Here are the rules.

1. Entries, submitted on the Official Entry Blank, or a reasonable facsimile thereof, must be received at American Zettler no later than April 30, 1980.
2. Only one entry per person for each contest. If you send in more than one entry, you will be disqualified.
3. In case of ties, the entry received first at American Zettler will win.
4. The two winning entries will be those closest to the tally made by a representative of Security Pacific Bank.
5. All employees and relatives of employees of American Zettler, its representatives and distributors are ineligible to enter. Also ineligible are all persons employed in the advertising and publishing industries.

The RCA VDT600 features 6 hours recording, 7-day electronic programming and electronic touch-button tuning.

AMERICAN ZETTLER, INC.

Official Entry Blank
All entries must be received by April 30, 1980.

Send to:
Sean Tierney, American Zettler, Inc., 16881 Hale Avenue, Irvine, CA 92714.

Number of Relays

Name__________

Title__________

Company__________ Division__________

Company Address__________

__________ State_____ Zip_____

Company Telephone Number__________

Grayhill's enclosed SMALL switches offer BIG value and BIG selection

Choice of ratings, circuitry, size, and features so you're sure to find a perfect fit!

Single Deck
½" diameter
SERIES 50, 51

22½° 30°, 36°, 45°, 60°, or 90° angles of throw—1 thru 4 poles—military and water sealed versions available.

Want more data? Circle 70

Quality and Economy
½" diameter, ¼ amp
multi-deck
SERIES 71

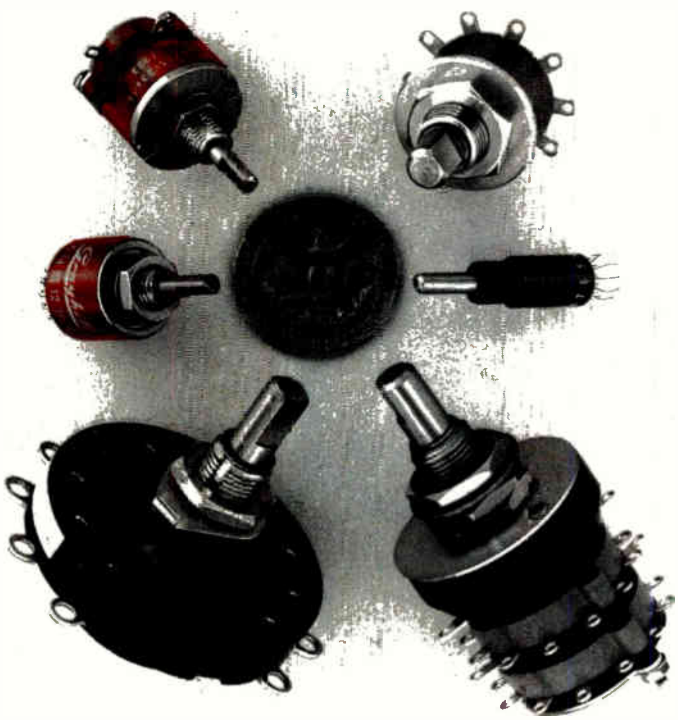
Value-engineered for premium enclosed switch performance at "open wafer" prices. Available in 30° or 36° angle of throw, 1-12 decks, PC or solder lugs, and many more options.

Want more data? Circle 71

Power Switch
SERIES 19

For the heavy loads, this 15 amp UL listed husky is the one. Up to 11 positions, 30° indexing, solder lug or "Faston" terminals.

Want more data? Circle 72



Single Deck Economy
SERIES 24

10 positions, 36° angle of throw. Choose plastic or stainless steel shaft, PC or solder lugs. The quality you expect from Grayhill, at under $2.75 (in 1000 piece lots).

Want more data? Circle 73

The World's Smallest
Rotary Switch
SERIES 75

Rated to make or break logic loads for 15,000 cycles minimum. Less than .300" diameter, 1 or 2 poles, 36° angle of throw.

Want more data? Circle 74

Grayhill's Best!
Rugged 1 inch, 1 amp
SERIES 42/44

All the features and options you could ask for, in the switch that's the work-horse of the industry.

Want more Data? Circle 75

Keylock operated

High quality switches with secure locks—available in 4 different Grayhill series. Flat or round key options, various key pulls.

Want more data? Circle 76

Military Qualified

Grayhill switches meet MIL-S-3786 SR04, SR13, SR20, SR35 and SR36, to provide the military product designer unequaled flexibility.

Want more data? Circle 77

A wide variety of special features and options

Spring return
Pull-to-turn/push to turn
PC mounts
Isolated positions
Unidirectional operation shaft
Panel seals
and many more.

Want more data? Circle 78

Adjustable stops

Available off-the-shelf from your Grayhill distributor in all popular series. They feature the exact electrical and mechanical characteristics of fixed stop switches and the convenience of a simple rotational stop mechanism that you set.

Want more data? Circle 79

And many more

described in the switch specifier's bible—the Grayhill Engineering Catalog.

Want more data? Circle 80

Grayhill *...the Difference Between Excellent and Adequate*
561 Hillgrove Avenue, LaGrange, IL 60525 312/354-1040

offshore and forestry equipment, as well as in other remote and portable applications. In quantities of 100 or more, the 10-W model is priced at $199, the 20-W model sells for $298, and the 40-W model sells for $476. They are available from stock.

Motorola Semiconductor Products Inc., P. O. Box 20912, Phoenix, Ariz. 85036. Phone Bob Hammond at (602) 244-5459 [383]

Cathode-ray-tube supply offers phosphor protection

A regulated, dc-to-dc power supply for cathode-ray-tube systems has such control features as phosphor-protection blanking, a logic-controlled enable circuit, and output-voltage status monitoring. The model RMC18PX900 operates from a 28-V dc source. A −10-to- −28-V dc negative bias source is required to operate the optional enable and monitoring circuitry.

The output voltages provided are: 18 kV at 200 μA, fixed, for the anode; 800 V at 200 μA, fixed, for the focus; 300 V to 600 V at 200 μA, adjustable for grid one; and −45 V at 40 μA for grid two (all ±5%). The line regulation for a ±5% change in the voltage is 0.02% of full scale for

all outputs. Anode load regulation is 0.05% (static) and 0.3% (dynamic) for a 0-to-200-μA load change. Ripple is 0.1% peak to peak at full load.

When the supply is turned off by command or by interruption of the input power, the first grid's voltage switches to under 682 V in 60 μs and holds there until the anode voltage bleeds down to less than 5 kV. This

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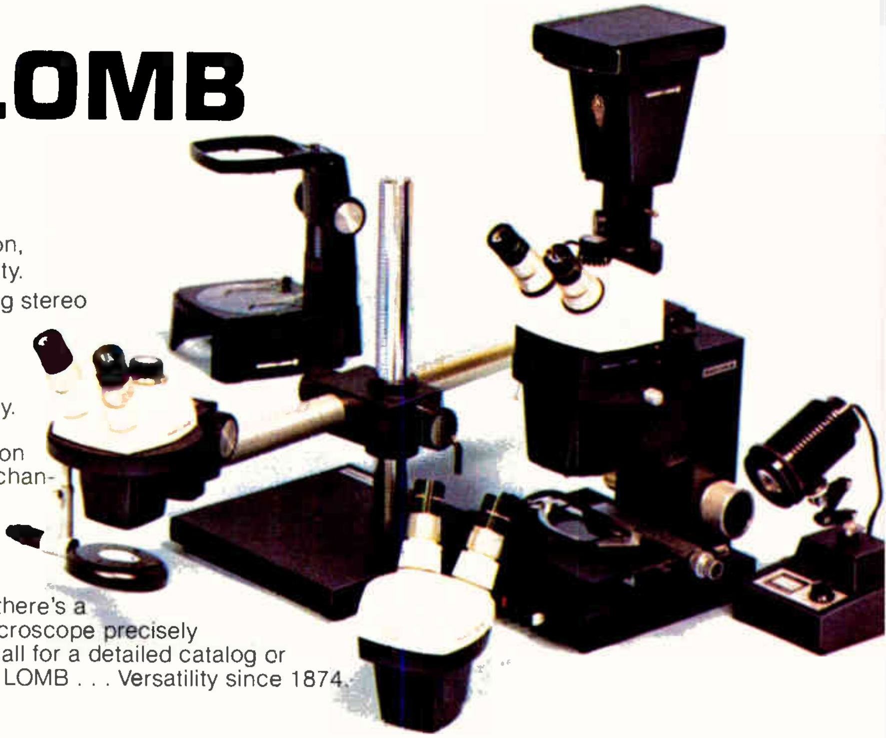

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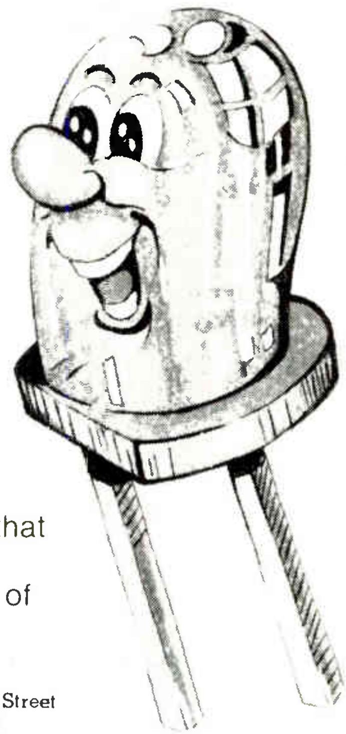

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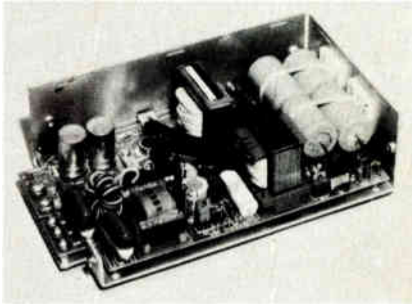
feature can be utilized in a sweep-failure or a beam-intensity sensing circuit to blank the CRT and automatically protect its phosphor against burns.

The power supply is available from stock to 12 weeks and is priced from $175 in high-volume production quantities.

Spellman High Voltage Electronics Corp., 7 Fairchild Ave., Plainview, N. Y. 11803. Phone Richard Becker at (516) 349-8686 [385]

150-W open-frame switcher is priced at $189



A series of open-frame switching power supplies has an output power of 150 W and sells for $189 apiece in single-unit quantities. Each ES-G series switcher measures 2.38 by 5 by 8 in. Efficiencies vary from 70% to 84%, and line and load regulation is within 0.2%. Regulation, modulation, and protective circuitry are all contained on a monolithic chip. The manufacturer quotes a mean time between failures of over 50,000 hours.

The switcher takes an input of 85 to 132 or 170 to 264 V ac at 47 to 63 Hz, thus providing effective brownout protection. The device has soft-start circuitry and is also protected against overvoltage, overload, short circuit, and reverse polarity. Hold-up time after loss of power is 16 ms; remote sensing is standard. The units meet Underwriters Laboratories and Canadian Standards Association requirements and are guaranteed for two years. Outputs are 5 V at 30 A, 12 V at 15 A, 15 V at 12 A, 24 V at 8 A, 28 V at 7 A, and 36 V at 5 A.

Power/Mate Corp., 514 South River St., Hackensack, N. J. 07601. Phone (201) 440-3100 [384]

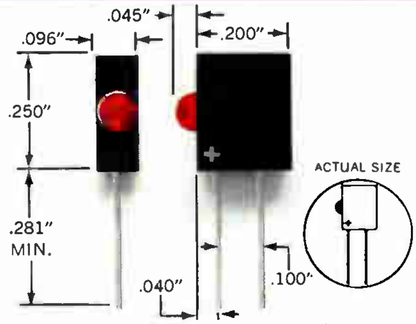
Power supply for floppy-disk drives provides five outputs

A 5-A power supply provides five outputs for single or dual Shugart floppy-disk drives in microprocessor systems. The drives plug into output connectors on the supply's printed-circuit board. The unit provides outputs of +5 V dc at 5 A, +12 V at 1 A, −5 V at 0.75 A, −12 V at 0.50 A, and +24 V at 1.5 A (with a 4-A surge rating). Except for the +24-V one, all outputs are regulated to 0.1%. Power input is 115 or 230 V ac at 50 or 60 Hz.

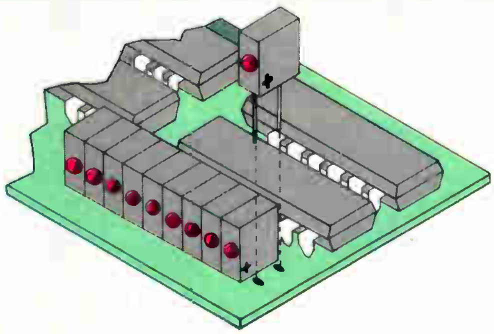
The FD502 is priced at $99 each in lots of 100 and is in stock.

CEI Corp., P. O. Box 501, Grenier Industrial Park, Londonderry, N. H. [387]

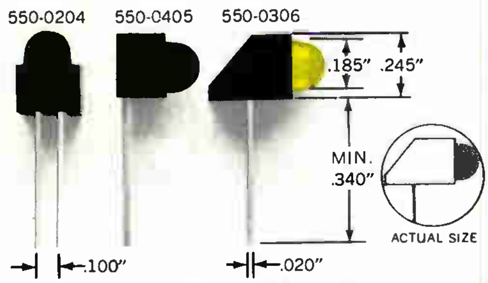
Dialight LEDs



555 SERIES LED logic state indicators available in 14 models with voltage ratings from 1.7 to 14. Suitable for dense packaging on printed circuit boards—up to 10 units to the inch—IC compatible. With built-in resistor. Polarity identified. Low power consumption. With pricing as low as .57¢ (1000 lot quantity).



These low cost LED logic state indicators are extremely versatile devices and lend themselves to a wide range of applications. Digital status indicators and circuit fault indicators are typical applications.



550 SERIES Mix 'em or match 'em. LED logic state indicators are available in red, yellow and green, in a variety of shapes, some with a built-in resistor. Can be driven from DTL and TTL logic. Designed for easy alignment on PC boards. Also available with high brightness LEDs. With pricing as low as .32¢ for standard brightness red (1000 lot quantity).

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Gold price rise to affect ICs

The skyrocketing cost of gold has forced integrated-circuit makers to reassess the prices of devices containing the precious metal. The latest announcement, from RCA Corp. in Somerville, N. J., is that "RCA will pass along the cost increment directly on a month-by-month basis," according to Benjamin Jacoby, vice president of marketing and international operations. **The increment will be referred to a base price of $350 an ounce.** Jacoby notes that the price increase will be applied across the board and will be tied to the shipment dates of the affected devices. The company's action follows on the heels of an announcement by National Semiconductor Corp., Santa Clara, Calif., that its increases will be referred to a $300/oz figure, will be updated monthly, and will be proportional to the gold price rise.

LEDs challenge incandescents in brightness

A series of highly efficient light-emitting diodes is said to offer comparable light output but far longer life than standard subminiature incandescent lamps. Manufactured by General Instrument Corp.'s Optoelectronics division in Palo Alto, Calif., the Illuminator series devices are fabricated using a new high-efficiency gallium phosphide technology **to produce more than 10 times as much light as other LED lamps.**

Terminal interfaces with many mainframes

A multifunction, multiprotocol computing terminal that interfaces with all major U. S.-made mainframes is being introduced here by the Austrailian firm ECS Microsystems Inc., whose American headquarters are in San Jose, Calif. **A 16-kilobyte buffer memory, combined with from 64 to 256 kilobytes of main memory, allows the Z80-based terminal to stand alone or to address selected computers from IBM, DEC, and other makers.** The terminal can be programmed in Basic, Cobol, and assembly language. Two minifloppy diskettes provide the model 4500 with 983 kilobytes of local mass storage.

CSPI enhances MAP array processors

Computer Signal Processors Inc., of Burlington, Mass., is strengthening its line of 32- and 64-bit MAP array processors with two series of memory modules and a programming panel. **Priced from $4,000, the HMOS main memories store 16 to 64 kilobytes and have cycle times of 170 or 300 ns.** High-density n-MOS main memories store from 64 to 256 kilobytes, have 500-ns cycle times, and start at $7.500. The model 7140 programming panel connects to MAP arithmetic boards, the central processing unit, and the main memory **to provide a display of the array processors registers, status input and output cues, and program counters.** The 7140 sells for $1,500 and has a delivery time of 30 days.

Good intentions pave road to . . .

There are more ways than one to change the accuracy of a digital-to-analog converter, and, unfortunately, we did it with a typo. Hybrid Systems Corp.'s 16-bit d-a unit featured in our New Products section last month [Jan. 31, p. 124] has true 16-bit linearity and is guaranteed to be linear to within ½ least significant bit. In expanding on this fact, we omitted a zero. **Maximum nonlinearity is 0.0008%.**

New products/materials

A one-component epoxy adhesive cured at temperatures as low as 212°F (100°C) provides tough bonds to clean metals, ceramics, and many rigid plastics. EP12's viscosity is maintained even after being stored for many months at normal room temperature. The material also has good chemical resistance and good dimensional stability.

Master Bond Inc., P. O. Box 522, Teaneck, N. J. 97666 [476]

A highly thixotropic material (one that flows only when pressure is applied), PCM-11 is especially suitable for heavy-duty applications. This resist has what the maker terms a shear thinning index of 3. A 1-mil coating cures at a conveyor speed of 20 ft/min under two medium-pressure 200-W/in. mercury-vapor lamps. The flash point of the material is 300°F, and it has a shelf life of six months at room temperature.

3M, Department EP9-28, P. O. Box 33600, St. Paul, Minn. 55133 [477]

Bonding adhesive Permabond 200 forms strong bonds in 10 to 20 seconds. Specifically designed for wire tacking on printed-circuit boards, the ethyl cyanoacrylate material can also be used to terminate coiled wires, to secure indicator lights, and for terminal strips, strain gage leads, patch circuits, and integrated circuits. The material is nonconductive. It needs no surface preparation nor solvents, catalysts, or heat treatments. Packed in polyethylene containers with dispensing tips, it is available in 2-g, ⅓-oz, 1-oz, and 1-lb quantities.

Permabond International Corp., 480 South Dean St., Englewood, N. J. 07631 [478]

This thick-film conductor, which contains frit, offers excellent adhesion to both 96% and 99% alumina and can be fired at 850°C. The fired film is over 91% gold and has a resistivity of less than 2 mΩ/sq/mil. Coverage is approximately 250 in.^{2}/troy oz (50 cm^2/g) at a fired thickness of 0.5 mil.

Electro Materials Corp. of America, 605 Center Ave., Mamaroneck, N. Y. 10543 [479]

Glasgow's unique attraction for new-technology industries dates from 1451

There are many parts of the world which are superficially attractive for new industries – but where you would have to start from scratch.

Not so in Glasgow.

There is already a concentration of new-technology industries in and around the city. So there is an existing pool of experienced technicians, research engineers and experienced labour. There are electronics design consultants. And there are sub-contractors and marketing organisations.

But there is yet another attraction which Glasgow possesses. Glasgow is, and has been since 1451, a university city. And its two universities – Glasgow and Strathclyde – have been exceptionally responsive to the new industrial technologies. Both have large electronics departments. Both provide consultancy, and undertake projects for industry.

So, when Honeywell brought a new research unit to the Glasgow area, its Managing Director, James McGregor, could say:

"There already exists in Scotland a heavy concentration of micro-electronics industries.

"This, together with our excellent relationship with many Scottish academic institutions, was the principal factor in steering the Solid State Applications Centre to Scotland."

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Contact Stuart Logan, Industrial Development Officer, Estates Department, Glasgow District Council. He's at 116 West Regent Street, Glasgow G2 2RW.
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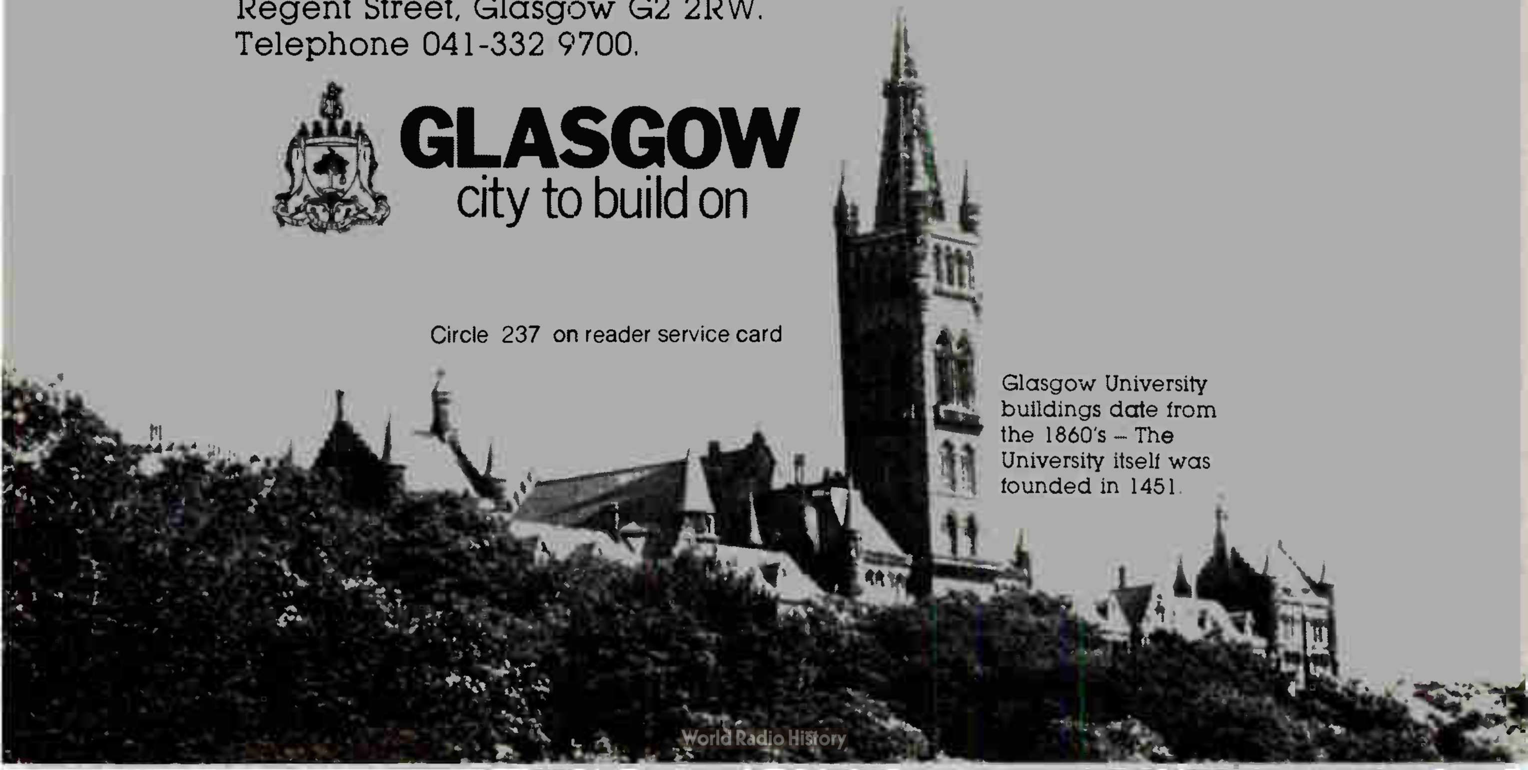

Glasgow University buildings date from the 1860's – The University itself was founded in 1451.

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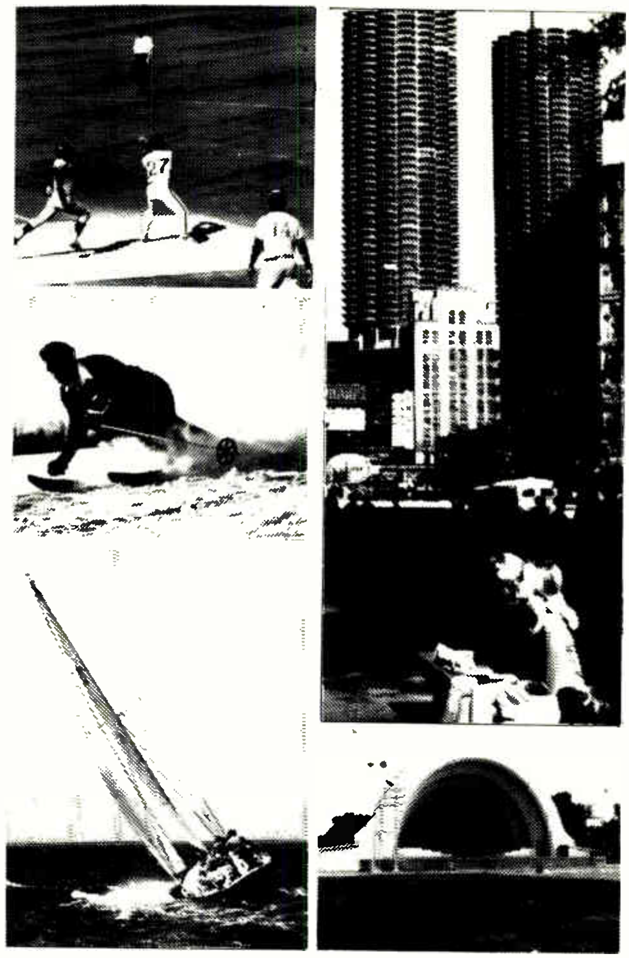

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February 14, 1980

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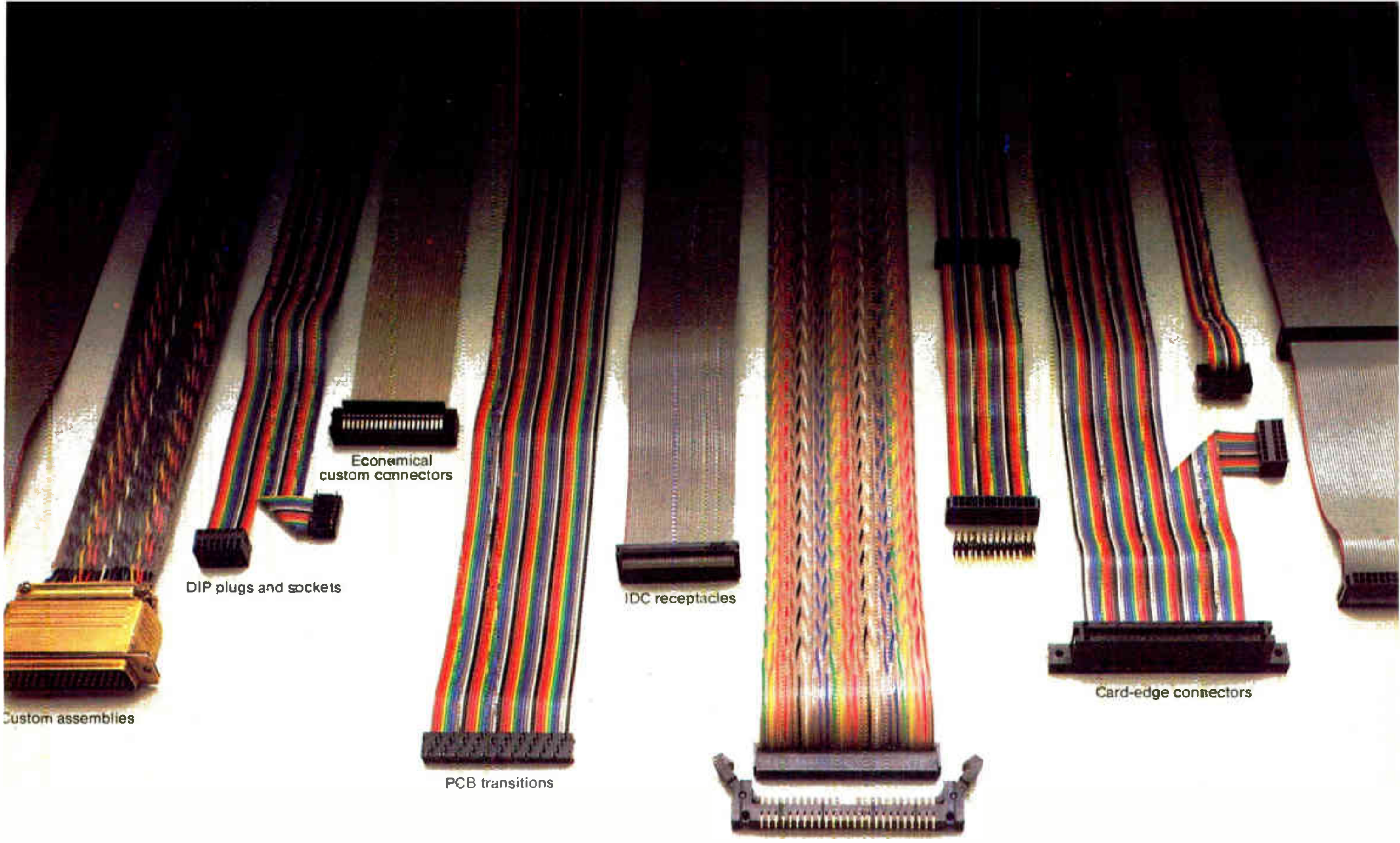

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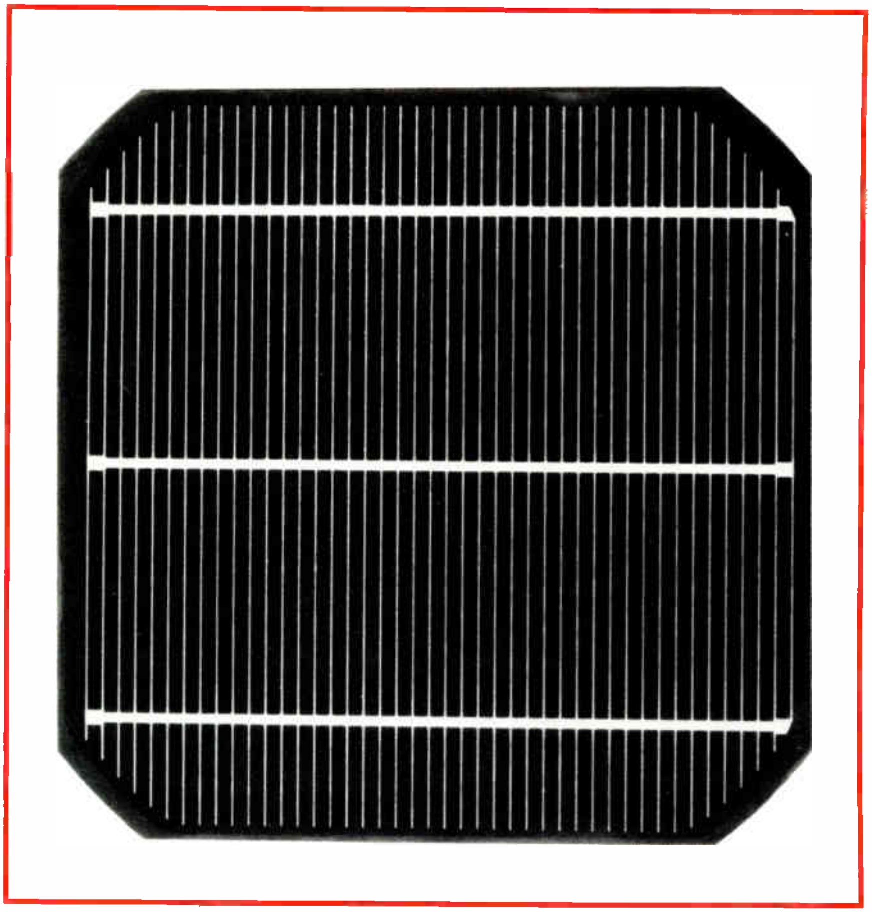

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Circle 250 on reader service card

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Power Supply	DC ±15V ±35mA		
Dimension	50W x 50D x 16H mm		

Usage

- Automatic zero & span calibration of pollution analyzers
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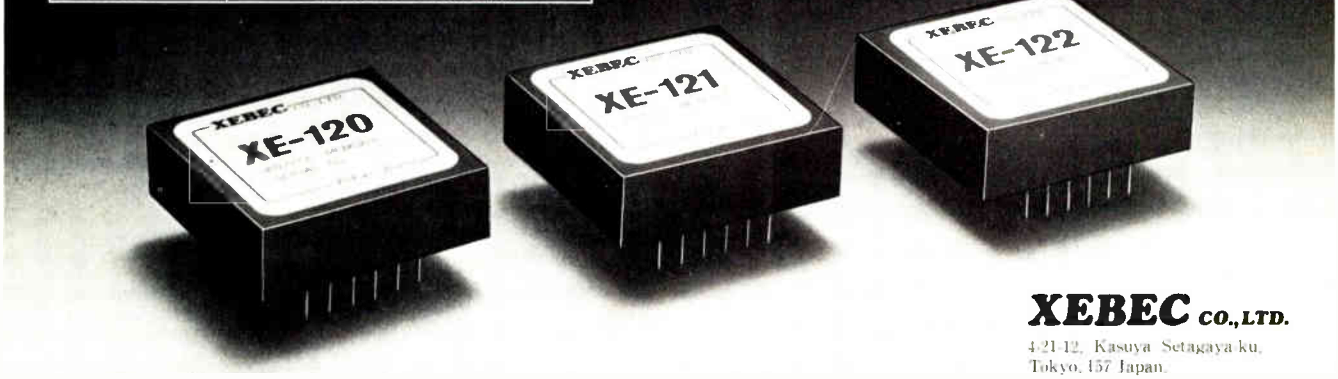

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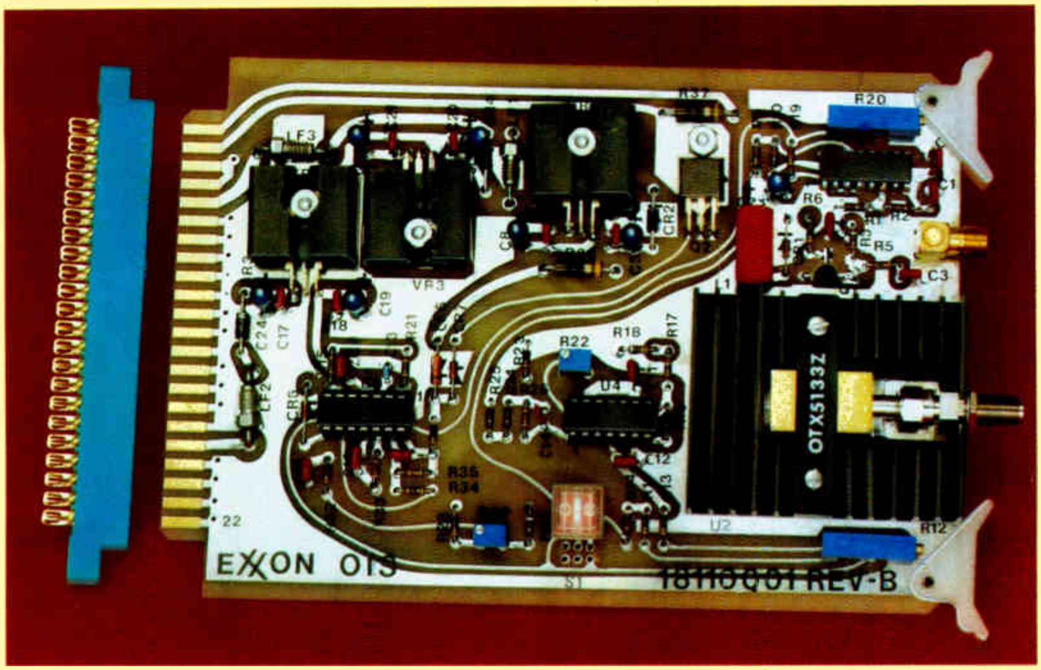

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Circle 901 on reader service card

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