APRIL 24, 1980

ELECTRO/80: BUS-LINKED INSTRUMENTS IN SPOTLIGHT/142

A microprocessor with virtual memory/123

Isolation techniques for data-acquisition systems/134

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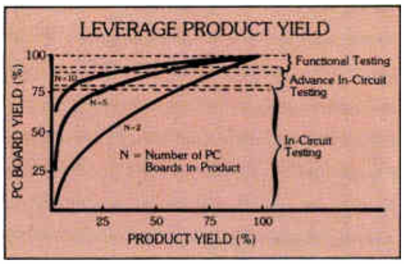
The secret! Leveraging.
There are any number of testing alternatives now available. However, HP's 3060A Board Test System combines the latest in-circuit testing technology with board level functional testing. The addition of functional testing to in-



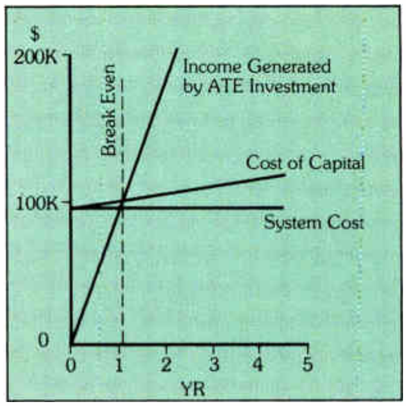
circuit testing provides a relatively small increase in board yield. But as you can see from the accompanying diagram, this small increase can mean a large improvement in product yield. For example, in a 5 PC board product, an increase in board yield of only 8% (from 90% to 98%) will leverage product turn-on rate from about 59% to 90%.

The impact of leveraging on production test costs.
As you may have already discovered, production testing costs increase exponentially. In other words, a fault that costs 18¢ to find during in-circuit testing can easily cost $20 or more if not detected until final product test. Why? Because of the additional time — and increased labor costs — associated with fault diagnosis and repair at this level.

By helping leverage product yield through in-circuit plus functional testing, the HP 3060A can help decrease production test costs. For example, in a five PC board product, with a product volume of 12,000 per year, the 3060A can slash production test costs as much as $19.94 per unit. And that's a total of nearly $250,000 per year.

Will it work for you?
As you can see from the graph, today's increasing cost of capital means the savings to be generated by an investment such as the HP 3060A must be substantial in order to produce a reasonable break-even point. How can you determine whether or not the 3060A would deliver a large enough reduction in production test costs — to justify its purchase?

To help you determine this for yourself, HP now offers a very helpful brochure titled "Financial Justifi-



cation — Circuit Test Systems." It includes a production test model worksheet, and has guidelines for calculating the 3060A Automatic Board Test System's payback period, average return on investment and/or discounted cash flow. You can use this information to determine the rate of return offered by the HP 3060A in your facility, even in light of today's high-interest economy. For your free copy of "Financial Justification — Circuit Test Systems," or for more information on the HP 3060A, (Priced at $82,000* for standard operational system) write to Hewlett-Packard; 1507 Page Mill Road, Palo Alto, CA 94304. Or call the HP regional office nearest you: East (201) 265-5000, West (213) 970-7500, Midwest (312) 255-9800, South (404) 955-1500, Canada (416) 678-9430.

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90/52

HP Circuit Testers — The Right Decision

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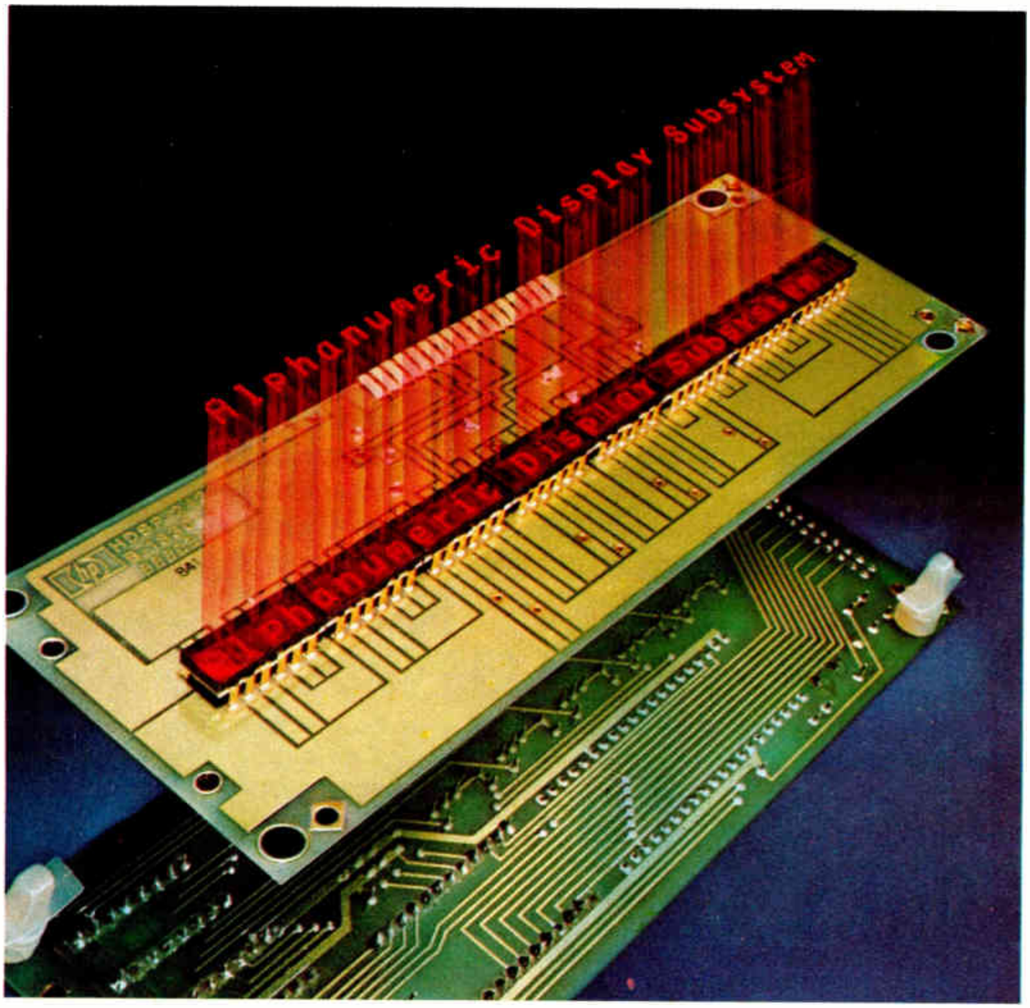

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For more information on the HDSP-24XX alphanumeric system or immediate off-the-shelf delivery, call any franchised HP distributor.

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HEWLETT PACKARD

Electronics
The International Magazine of Electronic Technology
Vol. 53, No. 10 • April 24, 1980

Highlights

Cover: Tests help designers harden RAMs against soft errors, 117

As 64-K dynamic random-access memories come into use, the problem of soft errors caused by alpha particles looms much larger, and reliance on error-correction circuitry to deal with them is not the whole answer. All routes to more reliable RAMs merit a good look. Accelerated testing, in which RAMs are exposed to much higher levels of radiation than they experience in their packages, is essential for early development of designs that are less vulnerable to the omnipresent alpha particle.

Cover illustration is by Jean-Marie Troillard.

FCC votes to cease most AT&T regulation by 1982, 104

Charles Ferris, Federal Communications Commission chairman, says the FCC's 5-to-2 decision "removes the barricades from the door to the information age," but litigation is promised aplenty—the Computer and Communications Industry Association and others will have their time in court. Some satellite data handlers, meanwhile, have "innovative" data-distribution ideas they want to sell the FCC.

16032 microprocessor addresses large virtual memory, 123

Addressing 16 megabytes of main storage is well within the range of microcomputers that benefit from virtual memory—a feature that relieves the programmer of a large software burden when disk store is a big part of a system's total. Once the exclusive domain of mainframes, a 16-bit chip has now entered the virtual memory field.

Choosing the right isolation for a data-acquisition system, 134

Optical isolation techniques have by no means displaced the venerable relay in systems where multiplexed inputs must be protected from common-mode voltages. In many applications, a flying-capacitor reed-relay multiplexer may be the most sensible form of isolation.

Microcomputers, software challenges dominate Electro, 142

Life in the digital age and approaches to the software task at hand will be much discussed in Boston when Electro/80 opens its doors on May 13. Now that gear compatible with the IEEE-488 bus is in wide use, for example, instrument system designers must tangle with a programming problem: the lack of standards at a higher level than those defined by 488.

. . . and in the next issue

Coverage of the National Computer Conference . . . a math processing chip teams up with a 16-bit microprocessor for high throughput . . . a programming language emphasizing portability bridges the gap between assembly and high-level languages for small machines.

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Publisher's letter

About a year ago, alpha particles were just a scientific curiosity to Mark Brodsky, a project engineer at Zilog Inc. specializing in packaging and development. Then he was handed the job of finding ways to protect the firm's 16-K dynamic random-access memories from soft errors caused by alpha particles. That included choosing coatings or plastics to resist alpha penetration, as well as special cell designs to cut down on soft errors. Brodsky did a complete survey of the literature available and found it inadequate; the result is the article that starts on page 117.

To get a clearer perspective on alpha-caused soft errors, Zilog started the comprehensive program described in his article. Near the end of the tests, company researchers discovered that a dynamic RAM's bit-select lines were extremely susceptible to alpha hits. A reexamination of earlier writings on the subject from Bell Laboratories and West Germany's Siemens revealed that scientists at those places had noticed the same phenomenon.

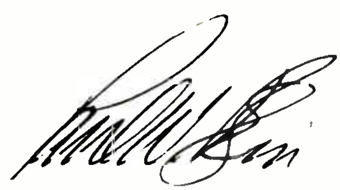
However, Zilog's researchers did find that two external factors independent of memory cell design—supply voltage and cycle time—could lessen soft errors if applied properly. Brodsky is now using his alpha particle experience to study the effects of soft errors on the firm's new, large quasi-static RAM.

In order to edit this article, packaging and production editor Jerry Lyman waded through many current papers and concluded that, if anything, the alpha particle problem will require increased attention in the design and application of new, larger dynamic and static RAMs. It appears that alpha particle protection in MOS devices will be a primary design consideration from now on.

As for Brodsky, the article is his first published technical work, but he says that he is not averse to firing off letters to Silicon Valley newspapers on topics that concern him and his family, such as housing problems in California or the damage that is being done to the local ecological system.

Designer's Casebook has never been known as a place for engineers to meet, but that's what happened to the two men who wrote "Protected regulator has lowest dropout voltage," on page 130 in this issue. It started with a Casebook in the April 12, 1979, issue by Kelvin Shih, who works at the General Motors Proving Ground in Milford, Mich. That article concerned a circuit to regulate the output of lithium batteries so that an input voltage as low as 5.2 volts could yield an output of 5 V. But an engineer at the Scott Aviation division of A-T-O Inc. in Lancaster, N. Y., wanted a regulator that could do better. That man, Thomas Vallone, in the course of trying to improve Shih's design, telephoned him. Their conversation led to a circuit that delivers 5 V from an input of 5.012 V. Which shows that the design you have in mind, if it is selected for Designer's Casebook, could get you not only the $50 honorarium but a collaborator as well.

We annually do a special report on the Electro show—as well as on Wescon and the National Computer Conference. This year, the Electro coverage begins on page 142. The most remarkable thing to those who have handled the story over the years is the way in which the trend in the number of companies attending, the number of booths they occupy, and attendance has gone steadily upward ever since the show's managers decided to make it one of a number of regional shows. Now we have—in addition to Electro and Wescon—Midcon and the upcoming Southcon due to start next year. All alternate between two cities in their areas. With next month's Electro/80 in Boston a sellout, word comes that Wescon, scheduled this year in Anaheim, Calif., Sept. 16–18, has already sold out all its booths. For *Electronics*' preview of that show, see our Aug. 28 issue.



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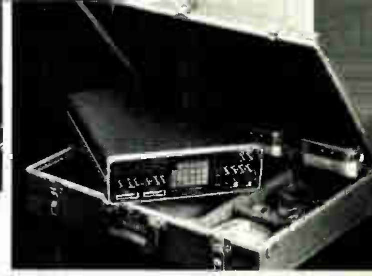

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For additional information 256

For a demonstration 7

Readers' comments

Human resources

To the Editor: In a Washington Newsletter [Feb. 28, p. 55] the Computer and Business Equipment Manufacturers Association is quoted as predicting power shortages in the mid-1980s. Such shortages, it is claimed, would halve the growth rate of the U. S. data-processing and electrical business-equipment industries. Rather than bemoan the fact that the power capability is not going to be there, why don't we push the design and application of computer and other technology to make rapid growth of time-of-day energy charges, local control of energy demand, remote control of air conditioners, etc., possible? Also needed are retrofit electronic schemes to control lighting levels.

George E. Gless
Boulder, Colo.

Corrections

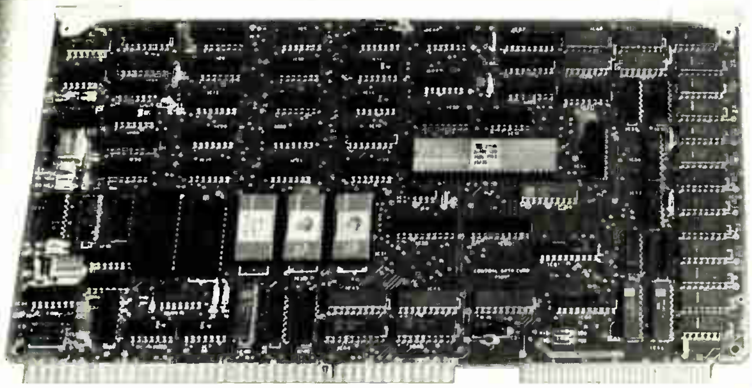
The price for GenRad's 1731 benchtop linear tester was incorrectly given in the Feb. 14 issue (p. 49). The correct price at that time was $25,900, the same as that for Analog Device's LTS 2000. As of April 1, GenRad increased the price of its unit to $28,500.

A number of errors appeared in "U. S. losing ground in the lab" (March 13, p. 81). The article shows that France, Japan, and West Germany spend proportionately *more on research and development than does the U. S. On page 83, the amount of R&D carried out by Thomson-CSF of France at its operating divisions and subsidiaries should read 93%, with 20% of its sales plowed back into R&D. On the same pages, the $17 billion in world sales for Siemens AG is the total for 1977–78, not for 1979. On page 85, an error in the use of conversion rates undervalued the West German government's expenditures on R&D—the figure should be $215 per capita, or 1.9% of its gross national product, a ratio close to that of the U. S.*

In the April 8 issue, a typographical error pinned the wrong company name to our story on Advanced Micro Device's AmZ8065 burst-error processor (p. 38). Our apologies.

INTRODUCING A NEW STAR IN MEMORY MANAGEMENT

The Multibus Z8000 CPU Board from Central Data



Featuring . . .

The Zilog/AMDZ8001 (segmented) 16 bit microprocessor chip. The Z8000 runs at a speed of 4 MHz and the board has full multi-master capabilities.

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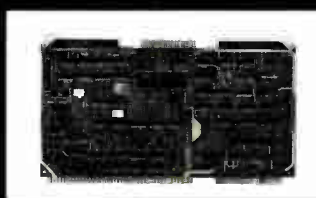
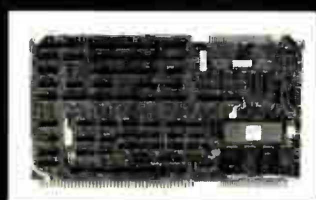
. . . and the finest supporting cast in the industry.

Static Ram Board adds either 16K or 32K of static memory to a Multibus system 16K — $495. 32K — $880.

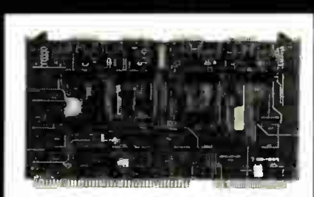


Double Density Floppy Disk Controller adds from one to four double density standard sized floppy disk drives, either single or double-sided. $255.

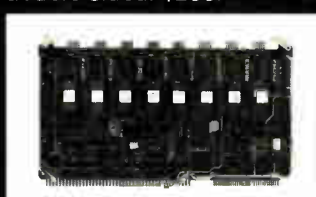


Cartridge Disk Controller Board provides DMA transfers to or from cartridge disk drives with capacities of 10 or 20 Mbytes. $335.

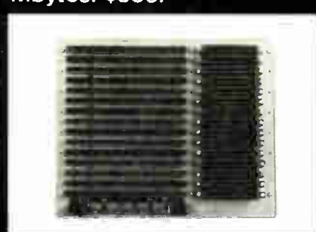
PROM Board allows the user to hook between 1k and 128K of PROM to a Multibus system. $110.



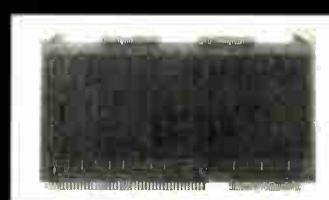
Quad Serial Interface Board hooks up to four EIA RS-232 interfaces to your system. $225.



Octal Serial Interface Board allows up to eight EIA RS-232 interfaces. $265.



Mother Board can hold up to 15 Multibus cards with both P1 and P2 provided for each card position. $255.



Prototyping Board will accommodate up to 95 16-pin sockets, allowing the user to wire wrap a prototype circuit. $45.

Extender Board will raise a board being tested up to a height of 6.9 inches. $50.

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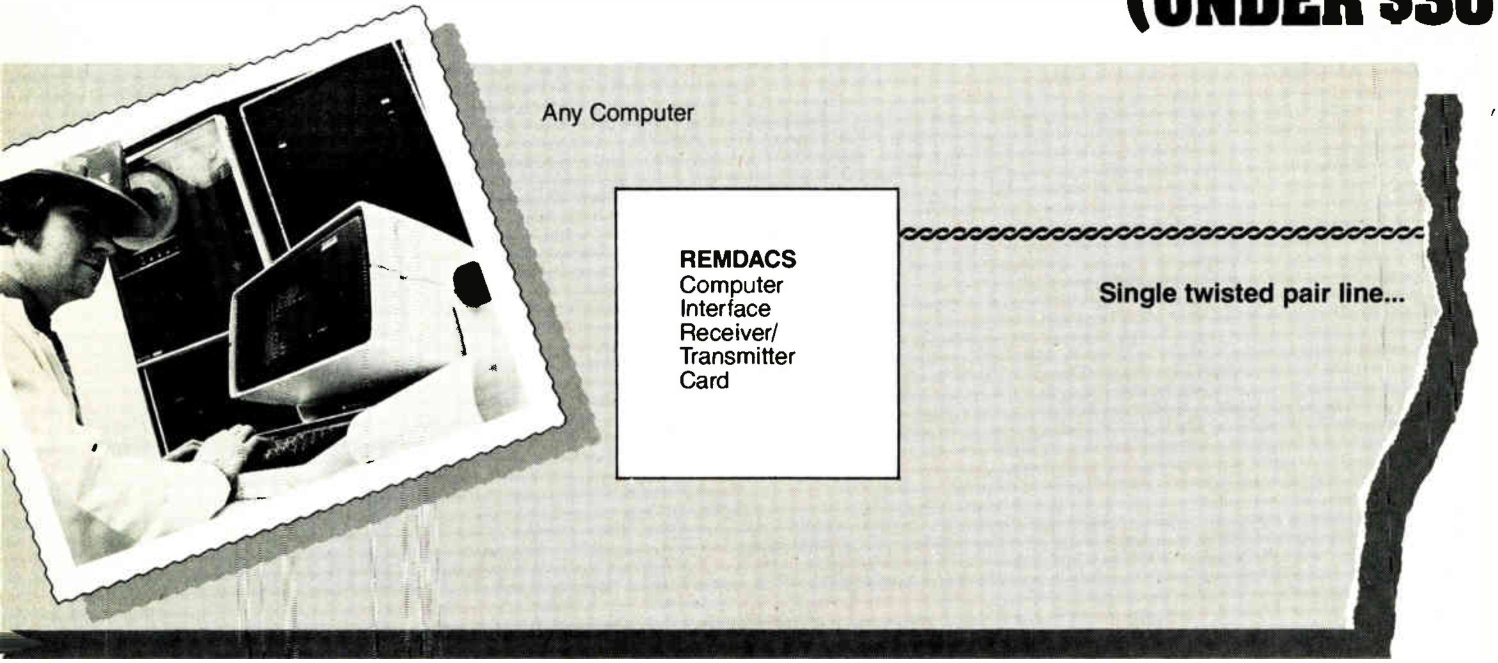

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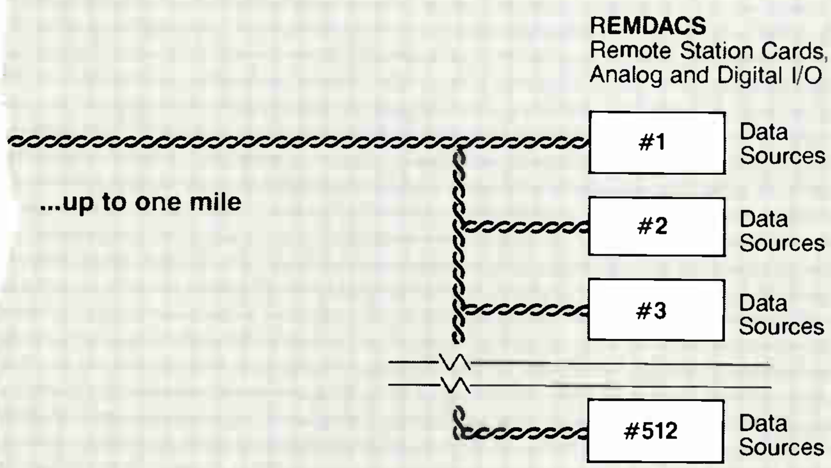

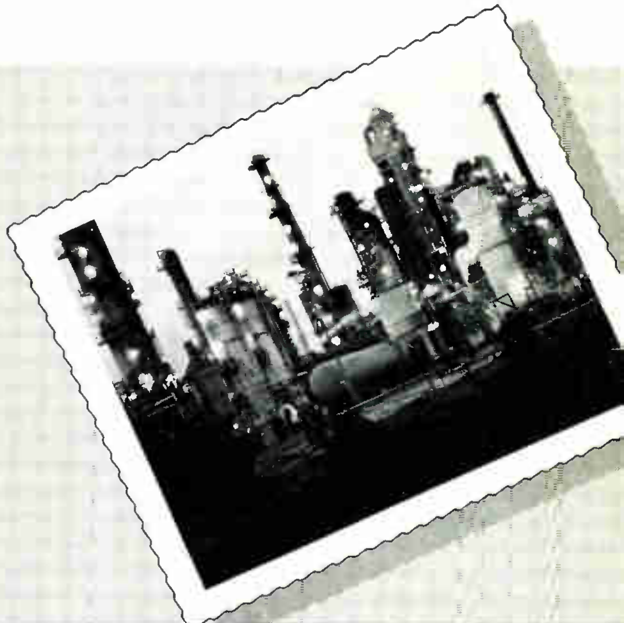

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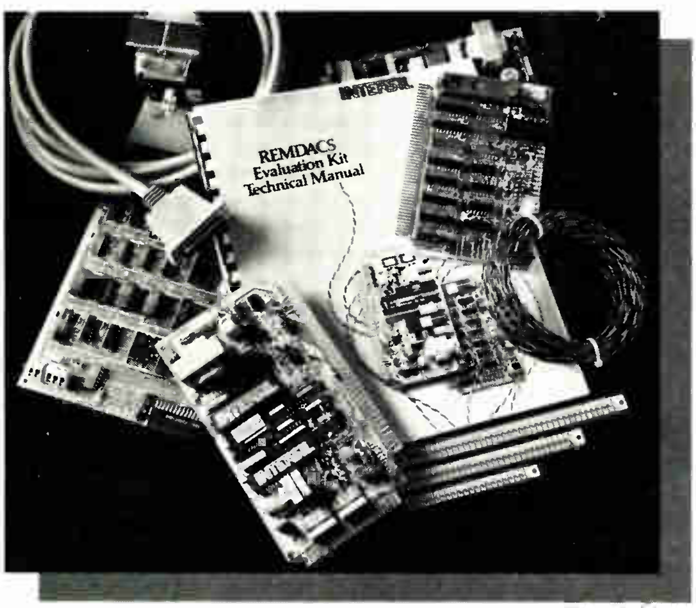

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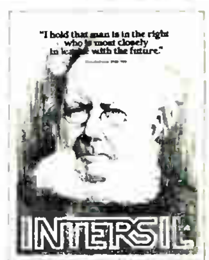

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Meetings

International Symposium on Circuits and Systems, IEEE, Shamrock Hilton Hotel, Houston, April 28–30.

28th Annual National Relay Conference, The National Association of Relay Manufacturers (D. D. Lingelbach, Oklahoma State University, 202 Engineering South, Stillwater, Okla. 74074), Oklahoma State University, Stillwater, April 28–30.

30th Annual Electronic Components Conference, Electronic Industries Association and IEEE, Hyatt Regency, San Francisco, April 28–30.

Second International Parametrics Conference, International Society of Parametric Analysis (P. O. Box 3104, Dayton, Ohio 45431), Sheraton Poste Inn, Cherry Hill, N. J., April 29–May 1.

Electronic Distribution Show and Conference, Electronic Industry Show Corp. (222 S. Riverside Plaza, Chicago, Ill. 60606) Las Vegas Hilton Hotel, Las Vegas, May 1–3.

Video '80—Congress and Exhibition on Video Systems, AMK GmbH (D-1000, Berlin, Messedamm 22), Berlin Fairgrounds, May 5–7.

World Electronics—Strategies for Success, Financial Times Conferences (10 Cannon St., London, England) and Mackintosh International, Loews Monte Carlo Hotel, Monte Carlo, May 5–7.

26th International Instrumentation Symposium, Instrument Society of America (A. E. Bowman, Hy-Cal Engineering, 12105 Los Nietos Rd., Santa Fe Springs, Calif. 90670), Red Lion Inn/Seatac Hotel, Seattle, Wash., May 5–8.

International Symposium on Computer Architecture, IEEE, La Boule, France, May 6–8.

15th Annual Microwave Power Symposium, International Microwave Power Institute (211 E. 43rd St., New York, N. Y. 10017), University of Iowa, Iowa City, May 6–9.

Microwave Power Tube Conference, Advisory Group on Electron Devices the Electron Devices Society of the IEEE, Naval Postgraduate School, Monterey, Calif., May 12–14.

Electro/80, IEEE, Hynes Memorial Auditorium, Boston, May 13–15.

Metrology of Modern Electronic Instrumentation, National Bureau of Standards (Barry A. Bull, B-162 Metrology Building, NBS, Washington, D. C. 20234), NBS, Gaithersburg, Md., May 13–15.

Tech-Transfair '80, Royal Netherlands Industries Fair (P. O. Box 8500, 3503 RM Utrecht, Holland), Utrecht, Holland, May 13–16.

Microcomputer Show '80, Japan Electric Industrial Development Association (3-5-8 Shiba Koen, Minato-ku, Tokyo 105, Japan), Tokyo Ryutsu Center, May 14–17.

Second Annual Conference on Electro-optical Systems and Technology, American Institute of Aeronautics and Astronautics (Dept. EOS, Box 91295, Los Angeles, Calif. 90009) *et al.*, Pacifica Hotel, Los Angeles, May 15–16; and Hilton Inn, Sunnyvale, Calif., June 5–6.

SRE-80 Reliability Symposium, TIE—Transportation, Information and Energy, Society of Reliability Engineers (Suite 1, 732 Wilson Ave., Downsview, Ont., Canada M3K 1E2), Holiday Inn Downtown, Toronto, May 15–16.

29th Annual Convention, The National Cable Television Association (Washington, D. C. 20006), Dallas, May 18–21.

Custom Integrated Circuits Conference, IEEE, Americana Hotel, Rochester, N. Y., May 19–21.

National Computer Conference, American Federation of Information Processing Societies Inc. (1815 North Lynn St., Arlington, Va. 22209), Anaheim Convention Center, Anaheim, Calif., May 19–22.

People

Caplan envisions design team of software, hardware experts

The importance of software to a computer product is not something David I. Caplan is likely to downplay. In fact, the integration of software and hardware design teams is topping his list of things to do as the newly appointed director of development for computer systems at Perkin-Elmer Corp.

The 50-year-old Caplan comes to the Oceanport, N. J., Computer Systems division with a good deal of experience and not a little Yankee ingenuity. Most recently the vice president and director of engineering at Raytheon Co.'s Intelligent Terminal Systems division, Caplan was also with Inforex Inc. in the mid-1970s as vice president of engineering. In 1952, he received an MS in mathematics from the Massachusetts Institute of Technology and in 1957 an MS in electrical engineering from the University of Pennsylvania. With this combined background in mathematics and engineering, Caplan should know what software and hardware integration is all about.

This integration is exactly what he plans to bring about at Perkin-Elmer. "The key is to have design teams that deal with all the ingredients," he says with regard to pulling hardware and software development much closer together. "Organizationally we're very traditional. The company is product-oriented and system-oriented," he says, adding that he hopes to build and extend these strengths.

Caplan, who sees software costs increasing at an accelerating rate, wants to have software planners involved even earlier in product development than they have been. "Hardware and software issues and differences will have to be resolved. Adding software later was the right way when what you developed in hardware represented a greater percentage of the costs," he observes.

"Perkin-Elmer has two thrusts: financial and engineering. Its focus is on credibility rather than on rapid growth," says Caplan. "And as I'm really a New Englander, that suits me fine." Caplan will make any changes within the development group at Perkin-Elmer with careful thought. Above all, he wants to keep his division a vibrant place to work. "This company grew out of Bell Labs, with a huge amount of technical competence. I want to make sure it continues to be an exciting place to work, because you don't keep guys by nailing their feet to the floor," he sums up.

Integrator. Perkin-Elmer's Caplan wants software people involved early in design.

Britton sees the computer as just another peripheral

"Business applications are becoming so varied that we need a whole new concept of a computer," asserts David L. Britton, the 43-year-old president of Britton-Lee Inc. of Los Gatos, Calif., and co-designer of the 8-inch Winchester disk. The problem is that the general-purpose computer originated with the Von Neumann model, which is good at number-crunching operations but poor in performing input/output-intensive functions. "But people who do business applications are finding that they are I/O-intensive functions"—he declares.

The answer to the problem, as Britton sees it, is the creation of specialized processors. Front-end processors such as the IBM 3705 have

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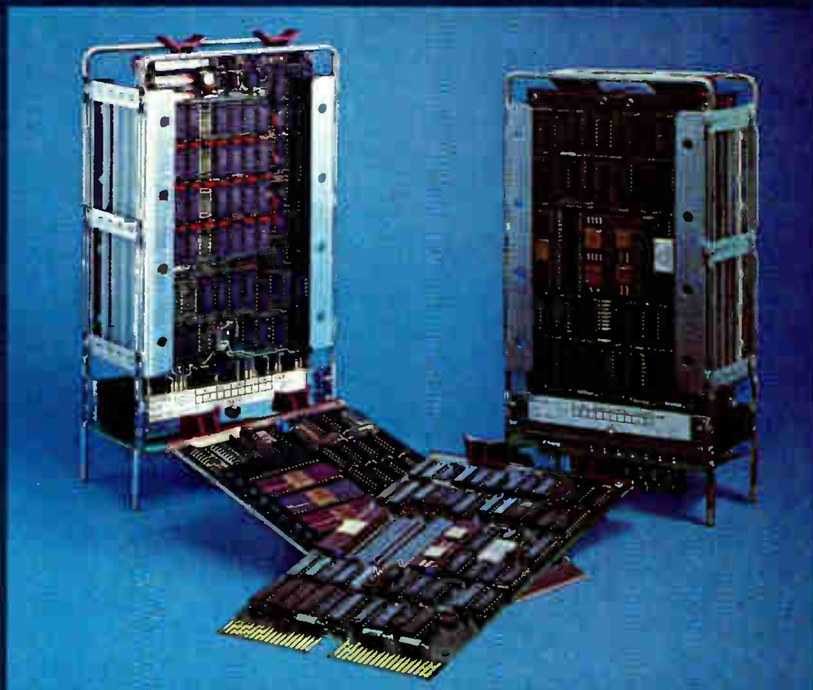

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corporate square/825 north cass avenue/westmont, illinois 60559/(312) 920-1050 appeared to handle the I/O-intensive processing interface between user terminals and the control processor, and now a hardware/software back-end processor has appeared to handle the data base (see p. 220).

"The point is, our back-end processor can bypass the computer altogether and communicate directly with intelligent terminals," Britton adds. "In most business applications, that is all that is needed, but the implications are more general. It means that, in a general data-processing system with both I/O and number-crunching routines, the task goes to the unit that can perform it best. The current general-purpose CPU then becomes, in effect, a peripheral that is kept on the line to perform the number crunching."

The intrafacility network schemes that will be introduced this year will only emphasize the connection of back-end processors to terminals. "After all, electronic mail is simply data base plus terminal," he adds.

Further boosting the back-end processor is the combination of the relational data bases that have been developed by the universities and the hardware components that have been developed by industry. The relational data base, Britton claims, allows the back-end processor to perform more tasks and to communicate with the central processor at a simpler, higher level.

Relational data bases have emerged from their earlier poor showings, in which they had run two to five times slower than hierarchical data bases, because, he notes, "universities were running their relational data-base models on the equipment they had—general-purpose computers whose operating systems were not compatible with the relational data base."

The result was that the data base was used inefficiently, with 25% to 30% needed to support the rest of the data base. "The key was to put that relational data base on a hardware/software–optimized processor operating at disk transfer speeds," he says. "That allows us to do efficient parallel processing and pipelining inside the back-end processor." □

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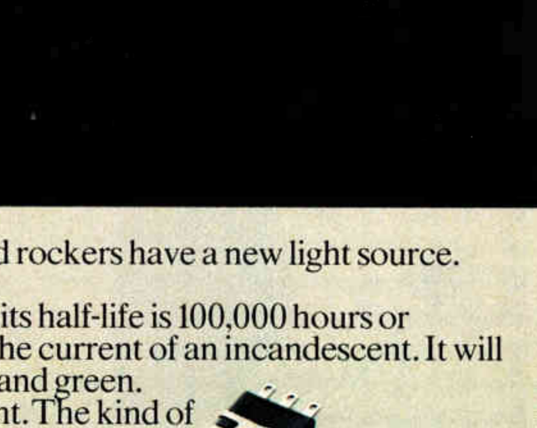

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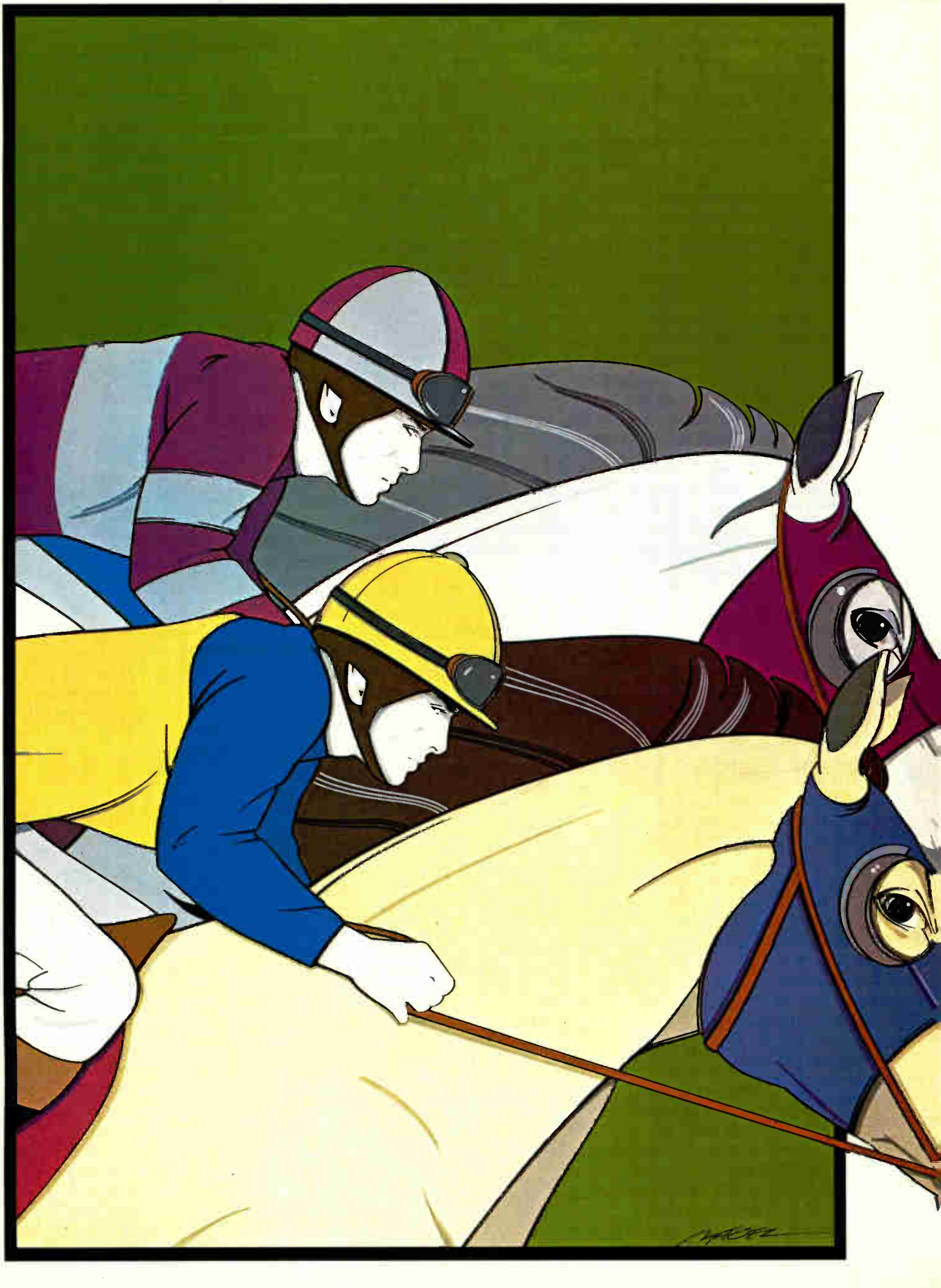

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2149H-3	55ns	25ns	180mA
2149HL-3	55ns	25ns	125mA
2149H	70ns	30ns	180mA
2149HL	70ns	30ns	125mA
2148H-3	55ns	55ns	180mA/30mA
2148HL-3	55ns	55ns	125mA/20mA
2148H	70ns	70ns	180mA/30mA
2148HL	70ns	70ns	125mA/20mA

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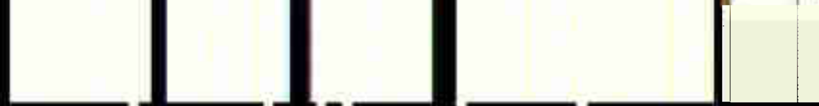
Tektronix announces the

HP announces a way to accelerate microcomputer development...

HP—When you depend on logic

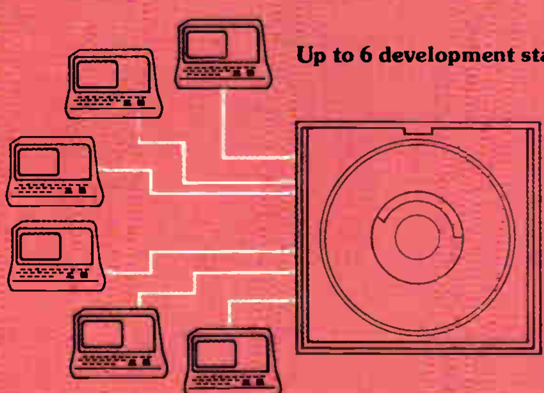


and put the brakes on development costs.

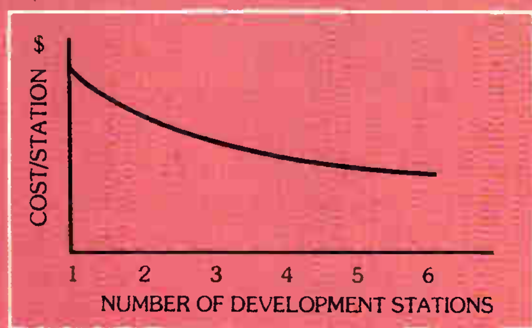
The new HP 64000 Logic Development System helps you speed microcomputer development and cut costs several ways. First, it uses a universal, rather than a dedicated, approach to microcomputer development. So you can use the HP 64000 to develop an 8080-based system today, and then a 6800-based system tomorrow. Or you can use it for different types of microprocessors in the same product, without paying the price of separate development systems for each. What's more, HP's powerful 64000 architecture is independent of processor type, bus-width or speed. So you'll be able to use this same basic system with future developments such as 16- and 32-bit processors.

Teamwork means faster system development.
Second, the HP 64000 can help shorten development schedules through efficient teamwork. HP's shared peripherals approach means that a number of operators share a common disc. This common data base serves up to six development stations. A powerful file manager encourages teamwork. Each user can work with his own copies of files, while a master set is maintained separately. Now, several programmers can work at the same time. Or designers can perform emulation, while programmers debug software.

The disc's high speed means each user is independent of, and essentially transparent to, every other. And all users have immediate access to the latest software for more efficient operation.



This HP approach is superior to a single-station, dedicated system for two other important reasons: With today's growing emphasis on microprocessor-based products, it's unlikely that any single system will provide the flexibility and growth path you'll need in future years. What's more, the 64000 offers significant savings when multiple development stations are contemplated (see chart below), and provides a practical way for you to obtain high-performance peripherals.



An accelerated path to market.
Third, because the HP 64000 has a powerful user-oriented display editor, rather than a teletype editor, it becomes a user-oriented system that speeds editing and debugging. Its advanced real-time emulation shows you precisely how your system will perform at speed, to help eliminate potential production problems and product entry delays.

In short, the HP 64000 ($18,500* for a minimum operating system) provides a way for you to optimize the efficiency of your development team, plan for the future, and expand development capabilities. Because the system is backed by Hewlett-Packard, you also enjoy the benefit of on-site service during the initial 90-day warranty period. Then, if you wish, you can get a complete HP service contract tailored to your needs that can also include on-site service.

To get complete details, write to Hewlett-Packard, 1507 Page Mill Road, Palo Alto, CA 94304. Or call the HP regional office nearest you: East (201) 265-5000, West (213) 970-7500, Midwest (312) 255-9800, South (404) 955-1500, Canada (416) 678-9430.

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It's time to recognize when less is more

At least a dozen studies—and they are just the top of the pile—show strikingly that when it comes to innovation and job creation, bigger companies are not necessarily better.

More than almost any other thing today, the U. S. needs new products, new jobs, new exports. And if those studies prove anything, it is that small business and new starts are far more efficient as innovators and as creators of jobs than the large companies that Americans have always been taught to believe are superior.

Item: A Canadian study shows that businesses with 20 or fewer employees created 72% of all new Canadian jobs between 1969 and 1977; meanwhile, companies with more than 20 employees were losing 124,000 jobs.

Item: An MIT Development Foundation study shows that innovative firms paid 34% more taxes than the mature firms, $2.3 billion to $1.5 billion during the 1969–74 period.

Though no one is about to call for the Government to break up GE or any other industrial giant—after all, the antitrust suit against IBM was filed on the final day of Lyndon Johnson's presidency and might still be in the courts when our grandchildren are fretting about their income taxes—but perhaps it is time to pay more attention to smallness. Perhaps it is time, given the state of the economy, to generate a more congenial climate for those proven innovators and job creators: new starts and small businesses.

Things are not rosy for today's entrepreneurs. Prime interest rates are in the 20% range, as is inflation. And many high-technology businesses—like the semiconductor industry—are becoming increasingly capital-intensive. Meanwhile, private venture capitalists seem to want a larger share of returns than in the heady days before the tax changes.

What's needed is less expensive money with which to encourage and support new ventures. The financial community is already considering lower interest rates on loans to smaller businesses. It might be time to apply the principle of the variable-rate mortgage to small-business loans as well.

Perhaps some form of long-term tax deferral like the systems operating in Puerto Rico and Ireland could be applied to American companies below a certain size. Those inducements have been very successful for the Irish and the Puerto Ricans, and the U. S. could profit by emulating them.

Obviously, it is not time to dismantle large firms; many industries profit from economies of scale. And small companies have a habit of growing, with the best-managed ones growing large indeed—the ultimate return on investment for the entrepreneur. Removing it would remove a key incentive to starting new companies.

But it is clear that small business is not being encouraged in proportion to its contribution to society and the economy. The facts are in hand; it is time for Washington, state capitals, and the financial community to do some creative thinking.

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200	IRF220 4 Amps	IRF230 7 Amps		IRF620 3.5 Amps	IRF630 6 Amps
400	IRF320 2.5 Amps	IRF330 4 Amps	IRF350 11 Amps	IRF720 2 Amps	IRF730 3.5 Amps
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Needed: a plan for educating engineers

by Ray Stata, *president and chairman, Analog Devices Inc., Norwood, Mass.*

If high-technology manufacturing is to take on major significance in the American economy, we will need to focus our attention on a resource problem that has never been encountered in industrial history. We'll need human resources—people with specialized levels of education and training, and in numbers that have never previously been required.

Any expanding industry requires people, but high-technology industry requires people with a high concentration of technical education and training. They don't exist to the extent needed for today's expansion, and we don't have anywhere near the educational resources necessary to create sufficient engineers for tomorrow's needs.

The electronics industries, one segment of high technology, have been growing at about a 17% annual rate for the last 10 years. In contrast, the number of electrical engineering degrees awarded annually has remained essentially constant over this period. Although engineering enrollments have picked up sharply in the last three or four years, the growth of demand continues to outstrip the growth of the supply.

In the past, cutbacks in Government spending have turned engineers into cab drivers and real estate brokers. The recession of 1974–75 also put engineers out of work and doubtless dissuaded many high school seniors from pursuing technological careers. Unfortunately, these painful disturbances in engineering employment in the past have led many to dismiss the seriousness of today's shortage as a temporary phenomenon. Concern over a future shortage sounds like another hysterical here-we-go-again doom-and-gloom reaction. Expand our college engineering resources, so the skeptic's argument goes, and the next Government cutback will create a new crop of hotdog vendors with Ph.D. degrees. But that scenario is no longer the case.

Back in 1968, the electronics industries did roughly $25 billion in business, much of it Government-funded. At the time, space and defense systems were a big employer of engineers and a dominant consumer of electronics. Ten years later, the electronics industries did $125 billion in business, with only a small proportion funded by the Government. Accordingly, even though military spending is sharply on the rise, cutbacks in Government procurement, should they occur again, will have a proportionately decreasing impact on electronics employment in the years ahead.

In short, the conventional arguments against expanding engineering faculties at our colleges and universities no longer make sense. The sheer size of the high-technology industry has changed the picture dramatically, even though historical fears of Government-created cutbacks remain.

Even if the urgency of the problem is generally accepted, it will be no simple matter to turn the human resources situation around. No doubt, universities will resist the upheavals that a redirected emphasis on technological education will create. In many areas of the country, colleges continue to produce school teachers even though jobs exist for only a small fraction of the graduates. What member of a teachers' school faculty will support expansion of the engineering department when doing so entails potential loss of prestige, a job, or both? For that matter, American universities annually graduate twice as many lawyers as engineers—some 15,000 engineers, compared with 30,000 lawyers. Once again, reallocation of finite educational resources is likely to entail severe resistance from the law faculty.

Significantly, Japan, whose high-technology industry is now challenging American companies, produces 40% more electrical engineers annually than the United States despite havin' half our population. Moreover, Japan gets b with a nationwide total of 15,000 lawyers, according to a recent estimate, whereas the U. S. finds employment for some 300,000.

Given Japan's penchant for innovation rather than litigation, one can imagine what advice the Japanese would offer our own Government on dealing with IBM's computer dominance. In all likelihood, instead of generating more lawyers to support the Justice Department's effort to break up IBM, the Japanese would generate more engineers. The natural process of competition, rather than antitrust litigation, would then determine IBM's market share.

Electronics *will periodically invite the expression of outside views on issues of importance to the electronics industries.*

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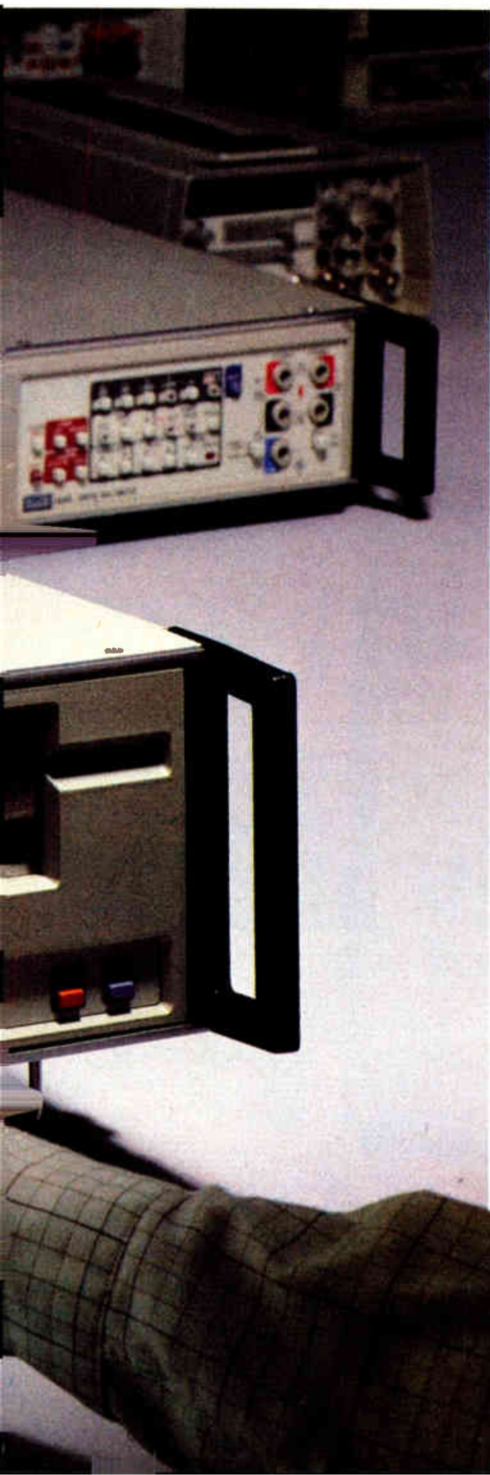

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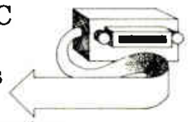

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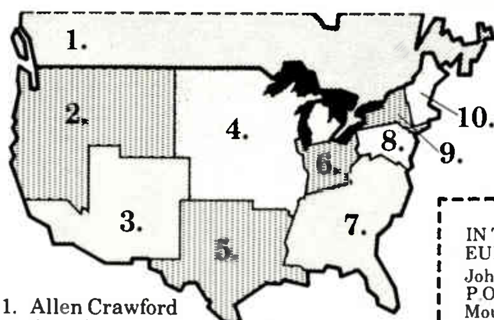

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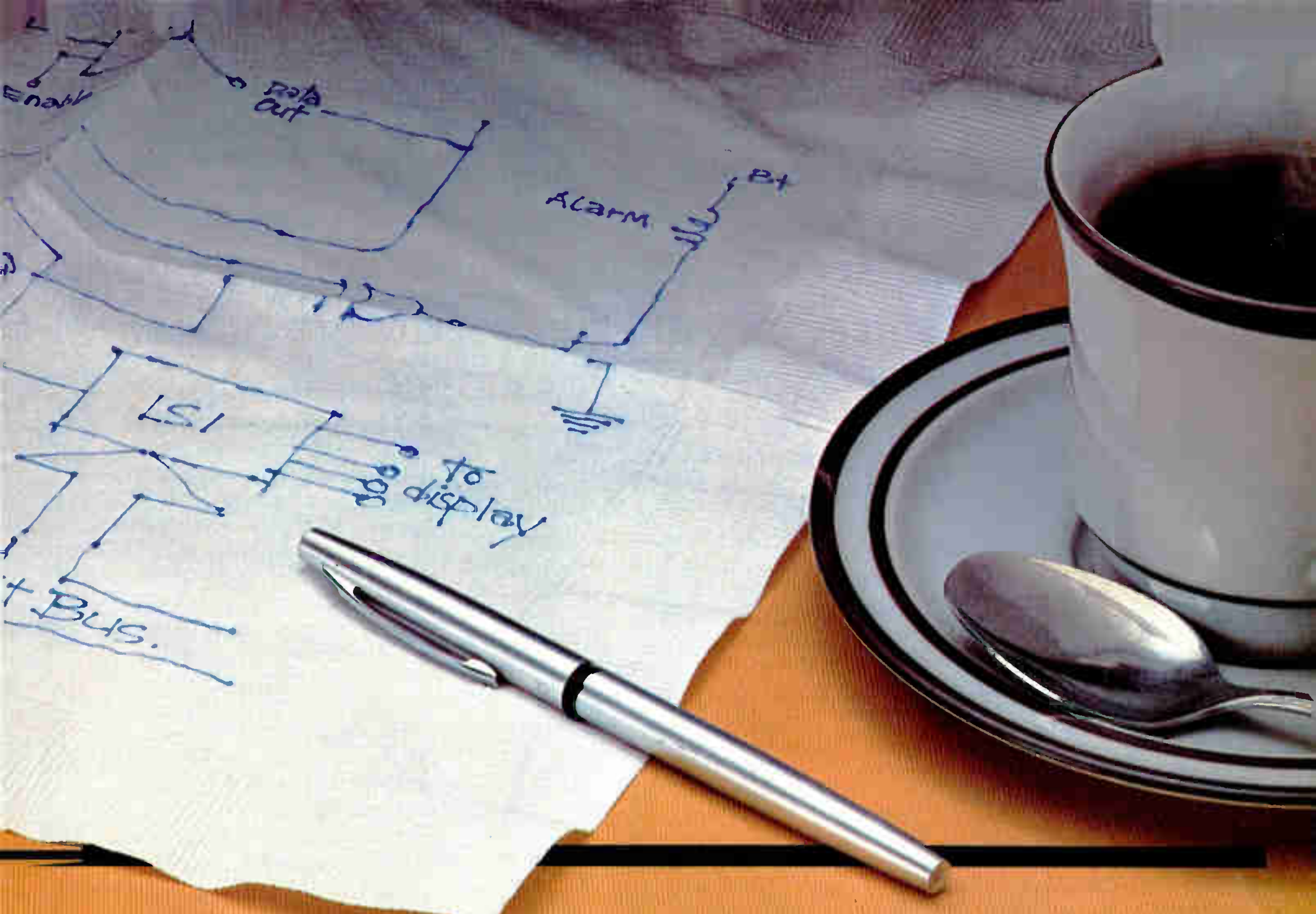

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Our new 8272 controller does more than drive up to four floppy disks simultaneously. It handles parallel seek on up to four disks for faster data access.

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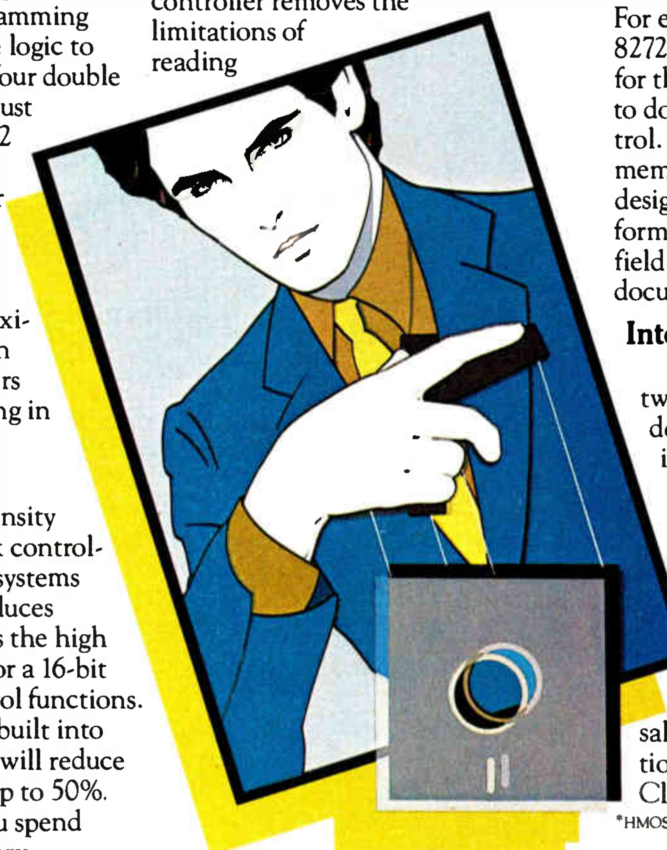

or writing only the number of characters a physical sector allows. The 8272 automatically transfers data across the disk's consecutive sectors... and, as a result, the CPU isn't forced to wait until the next sector is positioned. With Intel's new 8272, you not only free the CPU, you get the assurance of higher system performance.

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Circle 32 on reader service card

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Electronics newsletter

Data General's 32-bit machine is a multiprocessor

To be unveiled April 29, Data General Corp.'s long-awaited 32-bit computer—called Eagle—uses multiple processors and buses, plus dual caches, to run programs as large as 512 megabytes at high speed in multiuser configurations of up to 128 terminals. Truly a large machine, the Westboro, Mass., firm's **system operates within a logical address space exceeding 4 gigabytes.** In program capacity, by comparison, IBM Corp.'s 4341 can manage only 16 megabytes of memory and Digital Equipment Corp.'s VAX-11/780 only 32. The central processor is a 32-bit "hardware superset" of Data General's Eclipse, but almost all housekeeping tasks are off-loaded to three other processors.

Nine separate buses tie Eagle's architecture together for data transfer rates as high as 36.4 megabytes per second; the input/output transfer rate is 18.2 megabytes/s. Although compatible with the 16-bit software developed for earlier Data General computers, the new machine has a 32-bit instruction set with more than 400 operands and will be available with ANSI-standard 32-bit Fortran 77, PL/1, and Basic. Eagle's operating system allows 16- and 32-bit instructions to intermingle in the same program without mode-bit overhead. First shipments are scheduled for August or September.

Monolithic optical ICs promise 2 to 4 times faster conversion

Optical analog-to-digital converters two to four times faster than silicon designs are under development at the Massachusetts Institute of Technology's Lincoln Laboratory in Lexington, Mass. Staff member Frederick J. Leonberger and his colleagues have designed 2-, 4-, and 6-bit parallel-output, gray-code converters **that could reach speeds of 2 billion conversions per second.** The mostly monolithic designs include a number of parallel laser interferometers—one per bit—laid down on an electro-optic substrate, a pulsed, mode-locked laser diode, avalanche photodiode detectors, and emitter-coupled logic comparators. Optical phase shift, caused as a sampled voltage is applied to electrodes in one leg of an interferometer, would cancel or reinforce light coming through the other leg, yielding a binary optical output.

First Inmos device, 16-K static RAM, to be ready soon

Inmos Ltd. has completed the layout phase of its first product, a high-speed 16-K static random-access memory—the INS1400—and samples of the device will be ready shortly. The roughly 30,000-mil^2 chip will combine static and dynamic circuit expertise for improved performance. **Its 45-ns access time, to be improved with future scaling, is going after that of Intel's forthcoming 2167;** in fact, the two will be pin-compatible.

In addition to the new static memory, a 64-K dynamic RAM, and an advanced microprocessor, the Colorado Springs, Colo., company—majority-owned by the British government—now plans a 64-K electrically erasable programmable read-only memory.

Raytheon to unveil multipurpose PTS-2000 intelligent terminals

Raytheon Data Systems Co. of Norwood, Mass., is about to unveil its new PTS-2000 family of terminal systems. The line will encompass word, distributed, and network processing for jobs ranging from simple credit verification to interactive operations like handling orders. Raytheon claims that the PTS-2000 family will be "more expandable and cost less than any other competitive family of intelligent terminals." **It will eventually replace Raytheon's PTS-1200 programmable terminal line.** First in the new family will be the PTS-200, replacing Raytheon's mainstay terminal, the PTS-100, with "more capability at a lower price." It is ready for immediate delivery.

TI forecasts 20% growth in '80 for world markets

Taking a rosy view of the future, Texas Instruments Inc. has raised its forecast of the growth for the world's semiconductor markets in 1980 to 20%. Last year, it had pegged the number at 14%. The prediction, for total sales of $12.5 billion this year against $10.4 billion last year, came at the Dallas company's annual meeting and was delivered by president J. Fred Bucy. **He added that the total would increase an average of 17% annually to reach $45 billion in the late 1980s.** As for TI itself, the company grossed $956.4 million in the first quarter, up 33% from last year's corresponding quarter. Net income was $50.3 million, up 32%. Also it has raised its long-term growth goal to $15 billion for the late 1980s from $10 billion.

Memory tester sports 250-ps edge placement

Teradyne Inc.'s Semiconductor Test division in Woodland Hills, Calif., is about to take the wraps off its memory tester with edge-placement accuracy of 250 ps. Tailored for current and future high-speed dynamic and static random-access memories and designated the J389, the RAM tester incorporates automatic edge lock, **a computer-controlled method of compensating for edge-timing errors** through the use of time-domain reflectometry edge techniques. To be unveiled at next month's Semicon West in San Mateo, Calif., the J389 features Pascal-T, a high-level language with Teradyne-derived testing statements designed to minimize program-generation time by as much as 50%.

Control Data enters 8-inch disk race

Control Data Corp., the Minneapolis manufacturer of disk drives for original-equipment manufacturers, will unveil its long-awaited LARK 8-in. disk entry in time for next month's National Computer Conference. Unlike the spate of entries at last year's NCC, CDC's combines 8 megabytes of fixed disks with 8 megabytes of removable ones using a novel head technology that allows lightly loaded read/write heads to be retracted from the disks. Interface-compatible with its popular storage module drive, the LARK will reportedly be available for evaluation by November.

Addenda

To complement its *de facto* standard CP/I operating system for microcomputers and its MP/M multiterminal operating systems, Digital Research Inc. of Pacific Grove, Calif., **will introduce its network operating system, CP/Net,** at next month's National Computer Conference in Anaheim, Calif. . . . Look for Threshold Technology Inc., Delran, N. J., to offer within the next few months **a voice-recognition chip set consisting of three or four integrated circuits that can handle 20 words for under $20.** A 50-word module for industrial users will cost under $1,000. . . . To help original-equipment makers use its Naked Mini line of minicomputers, Computer Automation Inc. of Irvine, Calif., will introduce next month a **development system based on a top-of-the-line mini that it will unveil** at the same time. . . . Texas Instruments Inc. of Dallas is negotiating with Oki Electric Industry Co. of Tokyo for the purchase of **large quantities of complementary-MOS large-scale ICs for calculators.**

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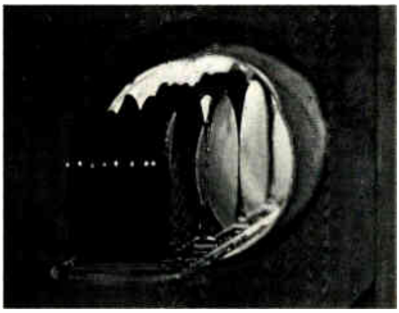

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Circle 37 on reader service card

Custom ECL chips boost performance in smaller mainframes

by Anthony Durniak, Computers & Peripherals Editor

Special emitter-coupled logic is implemented in LSI; that, plus innovative packaging, shrinks CPU to a single board

High-performance emitter-coupled logic is coming down to small and medium-sized mainframe computers. The Sperry Univac division of Sperry Corp. is using custom ECL large-scale integrated circuits in its new system 80—and is using state-of-the-art packaging, to boot.

The largest mainframes have gone to ECL for its impressive performance, but the chips have been costly and demanded special cooling. The LSI chips mitigate both problems.

Four chips. The heart of the 32-bit system 80 is four custom ECL circuits, each operating on 8-bit slices of data. The major functions of the central processing unit are partitioned between these chips, with one—the address and data interface unit—performing both the basic arithmetic and logic and the memory interface functions.

Beside reflecting computer houses' interest in custom LSI for the design flexibility it offers, these chips also show the importance such systems-plus-chip developments place on joint ventures. These parts were jointly developed by Fairchild Camera and Instrument Corp. and Motorola Inc. and are now marketed by Fairchild as the F100220 family [*Electronics*, Aug. 2, 1979, p. 120].

For supporting circuitry for these custom chips, Sperry Univac is employing a pioneering packaging technique that lets it put 16 standard ECL 10K family parts on a 16-layer ceramic carrier about 1 inch square. A recent analysis by Sperry Univac and Western Electric points to increasing use of this technique because of its ability to support LSI [*Electronics*, Jan. 17, 1980, p. 113]. The entire CPU fits on a 17-by-19-in. board just 3/4 in. high; the CPU of a comparable system 90/60 used 400 5-by-7-in. boards.

Other processors. Standard 2900 4-bit-slice processors are the basis of the disk channel controllers. Z80 microprocessors are employed in the work stations and communications controller, and other microprocessors are used to control other input/output devices.

Rather than just milk ECL's raw performance, considerable functions have been added in the system, says Jim Bloomquist, manager of the system 80's development. To increase reliability, for example, all data transfers within the computer are subject to parity error checking, and the memory has single-bit error correction and double-bit error detection. The new circuitry also gives the line lots of room to grow, since its performance is not fully taxed by the system 80.

To provide more powerful hard-

Faster. Sperry Univac uses custom large-scale integrated ECL chips in its new small mainframe with a central processing unit that fits onto a single board.

ware, the company also expanded its multitasking OS/3 operating system to support interactive operations with up to 39 local work stations and up to eight communications lines. Also, it can perform remote batch and remote job-entry communication and batch operations concurrently, the company says.

Replacement. Intended as the entry-level mainframe for the Blue Bell, Pa., division, the system 80 will replace its 90/25, 90/30, and 90/40 models, as well as its almost 16-year-old 9000 series. It will compete with IBM's popular System/3, System/38, and model 4331, as well as with machines such as Honeywell's level 62 and 64 processors, Burroughs B1800 and B1900, and the Hewlett-Packard HP3000 series, according to vice president of worldwide marketing H. Glen Haney.

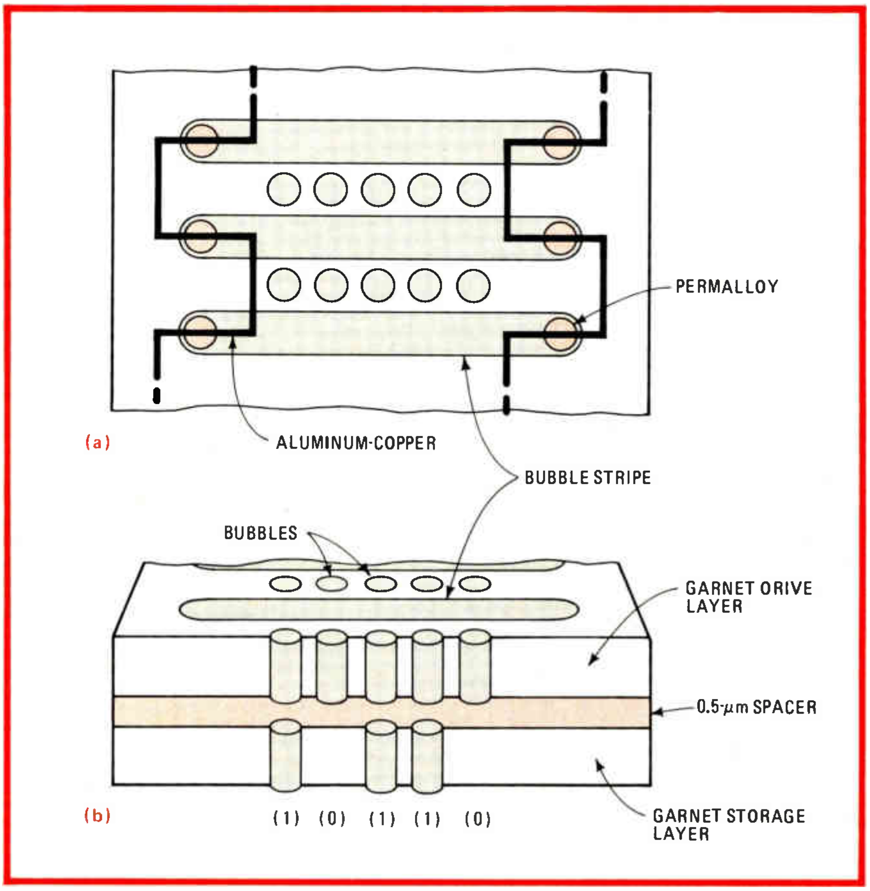
Available in two versions, the model 3 and the model 5, which offers 55% more power, the system 80 can handle from 262 kilobytes to 1 megabyte of main memory and eight 118-megabyte Winchester disk drives, as well as a variety of slower input/output devices such as diskette drives.

The CPU prices range from $55,869 to $94,647, the least expensive system it has ever offered in this performance range, Sperry Univac says. Systems prices with software range from about $70,000 to over $325,000. In comparison, IBM's 4331 CPU can be purchased for $68,250 with a 0.5 megabyte of main memory and for $76,100 with 1 megabyte.

Magnetics

Layered bubbles star at Intermag

Leading the list of advanced developments to be unveiled at this week's International Magnetics Conference in Boston is a novel memory technique with two layers of magnetic bubbles, one for storage and the other to move the bubbles in the first layer. But that is only one of some 275 papers on bubbles, tape and disk storage media, superconductivity, and other topics at Intermag.



Double bubbles. In a device co-designed by NASA and Sperry Univac, bubbles in an upper drive layer move bubbles representing digital information in a dense storage level beneath.

The multilayered current-access bubble memory is being described in a paper co-written by researchers for the National Aeronautics and Space Administration in Hampton, Va., and the Sperry Univac division of Sperry Corp. in St. Paul, Minn. The technique separates two magnetic garnet layers with a thin insulator (see figure).

Digital 1s and 0s are stored in the lower layer as the presence or absence of bubbles. The bubbles in the upper, drive layer act as small movable magnets to shift the bubbles in the storage layer.

The drive layer's bubble rows are separated by elongated bubbles called stripes. Permalloy propagation elements need be only along the edges of the part, and current pulses through the simple zigzag aluminum-copper conductor pattern shift the entire array in both layers.

One advantage is that the storage bubbles can be packed almost as densely as those in lattice files, where 1s and 0s are encoded as magnetic twists on a single bubble's wall. Lattice-stored data is much more difficult to detect than is the presence or absence of bubbles, however.

Another important benefit is the simpler propagation and conduction patterns, says NASA's R. L. Stermer Jr. These make for simpler registration procedures during manufacture.

Other developments. Intermag's organizer, the Magnetics Society of the Institute of Electrical and Electronics Engineers, is devoting 6 of the conference's 40 sessions to bubble memories, and one of these will be on megabit designs. Texas Instruments, Rockwell International, National Semiconductor, and Intel Magnetics each are describing their million-bit designs.

The give and take of discussion that follows may be the highlight of the show for systems designers. Unlike many of the other bubble developments described, the megabit parts are in or near production.

In a session on Permalloy devices, International Business Machines Corp., San Jose, Calif., expresses unusually strong support for conventional technology; in the past, it reported only on advanced structures far from production, such as bubble lattices. The about-face to more manufacturable technology may signal an intent to fit its typewriters or small computers with bubble storage in the near future.

Simulator. IBM's San Jose laboratory introduces a bubble memory simulator that might allow the behavior of Permalloy gates and detectors to be predicted through computer-aided design. So far, this process has been totally empirical.

Several papers present advances in bubble materials and processing. Liquid-phase epitaxy is used to deposit thin films of magnetic garnet onto a nonmagnetic garnet substrate, and Bell Laboratories, Murray Hill, N. J., shows a technique whereby 30 wafers can be dipped simultaneously. Two papers explain how laser annealing can be used to fashion propagation tracks in garnet in much the same way that ion implantation is used to construct contiguous disk patterns.

Hitachi Ltd. reports on its ability to prepare garnets that have a zero temperature coefficient. The magnetic properties of ordinary garnet materials change with temperature, which alters the effect of the bias field provided by external magnets.

Matching. Because a constant bias field keeps the bubble from changing size and even collapsing, other garnet materials require expensive barium-ferrite magnets with a matching temperature coefficient. Hitachi's development may allow the use of cheaper alnico magnets.

Bubbles are far from ousting disks and tapes from their roles as storage media, and Intermag sessions will reflect peripheral makers' plans for the next generation of these memories. One trend that is being emphasized is the use of semiconductor techniques in recording heads and media.

For instance, IBM's General Products division, also in San Jose, will explain its top-of-the-line 3370 disk drive, based on semiconductor techniques. Also, Fujitsu Laboratories Ltd., Kawasaki, will explain a novel technique for optically positioning the heads in a magnetic-disk system.

Two sessions are devoted to thin-film recording heads, the emerging technology that is viewed as critical to future peripherals because of the dramatic improvements in recording densities it promises. In addition to IBM's presenting the details of the thin-film head used in the 3370, another team from Fujitsu Laboratories will explain the fabrication of multiturn thin-film heads.

A group from Musashino Electrical Communications Laboratory of Nippon Telegraph and Telephone Public Corp. will discuss the fabrication of a floating thin-film head using ion-etching techniques. Sputter-deposited thin-film multilayer heads will be the topic of a paper by a team from Siemens AG in Munich.

Key to employing the new thin-film heads, however, will be new techniques for producing extremely smooth magnetic recording media. The topics presented in this session will include a paper on sputtered thin films. **—John G. Posa and Anthony Durniak**

Software

PL/1 shrinks to fit microprocessors

Now making waves in minicomputer programming, the IBM-originated high-level language PL/1 is starting to surface in the microworld. Digital Research, a Pacific Grove, Calif., software house, has reduced the compiler to 40 kilobytes of memory in its PL/1-80 package, which implements the compact, refined Subset G of the language for 8080,

Access scheme organizes data management

Data-base management systems are becoming increasingly popular—and important—in easing computer use, but translating data to fit into such a system remains a problem. Control Data Corp. is confident it will solve that problem with a new design methodology.

Called Information Analysis Services, the Minneapolis, Minn., firm's methodology expresses the relationships within the data in order to create useful information in a management system, says Stefaan A. DeSchrijver, general manager of marketing programs for Control Data Europe. "What you do is create sentences that link data by means of a verb, which expresses relationship," he explains.

The result of this process is what experts call a conceptual scheme for accessing the data base. The methodology was originated by G. M. Nijssen, executive consultant at CDC's Research Center in Brussels, Belgium, and has been tested by customers for over a year. Now licenses will cost between $895 and $2,780 monthly, or between $49,590 to $128,760 for unlimited use.

"The data base is a model of the real world, and there is a need for a method to move data from the real world to this model," agrees Eugene Lowenthal, program manager at one competitor, Intel's Commercial Systems division—the former MRI Inc.—of Austin, Texas. Currently data dictionaries are most popular for organizing data, but, as Lowenthal notes, it is still quite an art to arrange the data for the dictionary in the first place. Thus CDC thinks its new technique will prove popular.

At stake is a market for data-base management systems that in 1980 is estimated to reach $869 million worldwide, according to a recent report by Creative Strategies International. Making the systems easier to design and use will be critical to achieving the 82% compound annual growth rates that the San Jose, Calif., market research firm predicts will bring it to over $4.9 billion by 1983. **-Anthony Durniak**

Z80, and 8085 microprocessors.

It is, in fact, Subset G that has turned PL/1 into an effective programming tool (see p. 102). Digital Research's president Gary Kildall holds that it will prove better for business applications of microprocessors than Pascal, Cobol, or Basic.

The PL/1-80 package consists of a compiler, a relocating macroassembler, a linkage editor, and a run-time library. Its compiler contains optimizers that are used during code generation to reduce storage requirements greatly.

Shrinkage. The optimization takes only 38 kilobytes of code, as opposed to 400 kilobytes on a 370-PL/1 compiler. It is this shrunken memory requirement that makes the language feasible for microprocesors, and the shrinkage owes even more to the optimization technique than to the compactness of Subset G.

Digital Research uses what is called frame optimization, which covers the intermediate code one segment at a time as it flows to a forms processor—a table-driven module searching for repeating cases such as an expression being incremented by a constant. The result is greatly reduced compilation time and memory space, compared to global optimization.

Kildall notes that Pascal, in its standard transportable form, is not oriented toward business applications. PL/1-80, on the other hand, has a complete input/output structure, error-exception processing, and a much wider variety of data types than does Pascal.

Production. "PL/1-80 is a production language, not a teaching language like Pascal," Kildall argues. For example, he notes, decimal arithmetic in Pascal must be executed as a subroutine, whereas in PL/1-80 it is just another data type.

In addition, Pascal must be modified to allow the string manipulation that is necessary in word-processing applications, and such modifications affect the program's transportability. "One of the main reasons people like Pascal is that it is a block-structured, Algol-based language," says Kildall. "But so is PL/1-80.

"The fact is that we like Pascal, too, and are working on an 8080 compiler. But the language needs more applications-oriented standardization," he adds.

Others. For business applications, Kildall prefers PL/1-80 to Cobol and Basic. "Cobol and Basic are totally consumed in it," he remarks. "Anything you can do in either of those languages can be done at least as efficiently in PL/1-80."

A number of minicomputer makers agree with Kildall's assessment of Subset G's effectiveness as a business-oriented applications language and are implementing it. These include Wang Laboratories, Digital Equipment Corp., Prime Computer, IBM, and Data General.

PL/1 is intended for use with the company's CP/M operating system, popular in the microprocessor world. It can also run with the multiterminal versions of C/M and MP/M, as well as with CP/NET, the network operating system.

"We expect that within three years the CP/M community will have reached over 100,000 users, and that 25% of them will have either the full compiler package, or at least the run-time library," Kildall says. A noncommercial, single-processor licensing fee for the full package costs $500.

As well as originating CP/M, Kildall acted as consultant to Intel Corp. on its PL/M microprocessor language, and he makes a sharp distinction between the two of them. "PL/M is a systems language that was designed for operating systems; PL/1-80 is an applications language," he says. Also, "we now have a language that is upwardly compatible with PL/1; that is not true for PL/M," he notes. **-Martin Marshall**

Speech synthesis

Want a talking IC? TI says 'Call us'

After more than a year of refusing to sell its much-sought-after speech synthesis chip set to outside customers, Texas Instruments Inc. did an about-face last week. The Dallas company, announcing its intention to sell the set to original-equipment manufacturers, laid out plans to support OEMs in order to gain a major foothold for its linear-predictive coding technology. Its move comes in the face of budding competition

Speech recognition takes another stride

The other side of the speech coin is recognition, but it's much harder to get computers to listen than to get them to talk. IBM Corp., for one, however, is reporting great strides in the recognition of continuous speech.

Frederick Jelinek and the group he heads at the Thomas J. Watson Research Center in Yorktown Heights, N. Y., have programmed a System/370 168 to understand 25-word sentences built from a 1,000-word vocabulary with an accuracy of 91%.

Low-cost speech recognition would be a tremendous asset to the computer giant's line of office and data-processing equipment. Although the present system is speaker-dependent and takes 2 hours to train for each voice, Jelinek predicts that an experimental dictation machine might be possible within a few years—"capable, perhaps, of recognizing 1,000 to 2,000 words and requiring only 15 minutes of speaker-training time."

In IBM's setup, an acoustic processor samples the speaker's voice 20,000 times a second. A thousand samples at a time are put through a discrete Fourier transformation to produce spectral time samples that are in turn compared with samples recorded during training. A linguistic decoder program compares the incoming and stored patterns for each word.

It now takes 200 times longer to recognize a sentence than to speak it; 30 seconds of speech take 100 minutes to transcribe, for instance. But IBM feels parallel processing plus improved recognition technology will bring about experimental real-time recognition in this decade. **-John G. Posa**

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Circle 43 on reader service card

E-H International, Inc • 7303 Edgewater Drive, Oakland, CA 94621 • PH: 415/638-5656 • TWX: 910-366-725 from other semiconductor makers.

Bernard H. List, TI vice president who heads up the company's U. S. MOS operations, denies that recently announced speech-circuit marketing plans by National Semiconductor Corp. [*Electronics*, March 27, p. 39] and others are a driving factor in the TI move. Rather, List says, the move had to wait for a commitment to add production capacity and the ability to support customers in developing high-quality synthetic speech using LPC techniques.

Production quantities will be available during the second half of 1981, OEM-priced at about $13 for the two-chip set containing the TMS5100 speech synthesizer circuit and a TMS6100 128-kilobit read-only-memory. Prototype quantities of the synthesizer will be available as necessary this year.

p-MOS. These circuits are fabricated in p-channel MOS technology and are the same devices as those in TI's Speak & Spell [*Electronics*, Aug. 31, 1978, p. 109]. The combined learning aid and toy has been enormously successful, and, says TI, is the harbinger of a $3 billion semiconductor market by the late 1980s. That figure includes speech recognition and authentication—research areas in which the firm is active, as is IBM, among others (see "Speech recognition takes a stride," p. 42).

The 5100 and 6100 are the initial offerings in two new series of TI chips designated the TMS5000 and TMS6000 lines. The firm is believed to be developing additional p-MOS parts, including a synthesizer chip to work with 8- or 16-bit microprocessor controllers. It is pushing its p-MOS 4-bit TMS1000 family as the controller for the present chip set, noting that it will add only about $2.

Services. TI will immediately begin offering vocabulary and speech development services priced in OEM quantities at $200 per synthetic speech word, which is defined by the company as 1 second of utterances. The 128-K ROM can hold 100 words of synthetic speech, TI says.

In addition to the 5100 and 6100 components, TI will offer a version of its TM990/306 speech synthesizing module for industrial customers who want to develop their own vocabulary. The original 990/306 board was offered last year [*Electronics*, Nov. 8, 1979, p. 44] containing a standard vocabulary stored in erasable programmable ROM for use with the company's 16-bit TM990 microprocessor family for industrial control, test, and security applications. **-Wesley R. Iversen**

Business systems

Small computers gain sophistication

New technologies and new entrants are sprouting this spring in the already blossoming market for very small business computers. Multiprocessor architectures and some of the first uses of 8-inch Winchester disk drives are found in new units from the well established business computer maker Wang Laboratories Inc. and from Hazeltine Corp. and Applied Digital Data Systems Inc., both long noted for their computer terminals and now seeking opportunities in a new market.

Wang is unveiling new versions of its 2200 small business computers. The Lowell, Mass., company also introduced a novel multiplexer that shares a disk drive among several central processing units and a software package that requires minimal programming skills.

Winchester. Two models in the new series offer 8-in. Winchester fixed disk drives—Shugart's SA1000—melded with a floppy by a Wang-designed controller. "We are offering a well-balanced combination," says Sam Gagliano, director of small-business systems. "The controller makes the media compatible." Drive maker Shugart also sees the value of the combination; it is launching a controller module that will save design time for companies like Wang (see p. 208).

The 2200 LVP, the largest of the new machines, offers 32, 64, or 128 kilobytes of user main memory and 60 kilobytes of machine main memory. Selling for between $15,000 and $35,000, it can store 2, 4, or 8 megabytes in its fixed disks and 1 megabyte in its backup dual-sided double-density diskettes.

The smaller 2200 SVP is intended to compete with IBM's recently announced 5120 [*Electronics*, Feb. 14, p. 40]. The SA1000 is offered as

Software transforms data processor

Reflecting the importance software plays in harnessing computers to office-automation tasks is Prime Computer Inc.'s entry into the market. Two intelligent terminals and a letter-quality printer were all the hardware that the Newton, Mass., manufacturer of 32-bit minicomputer systems added to its 50 series. The heart of the Office Automation System is the software.

The 50 series [*Electronics*, Jan. 18, 1979, p. 174] is intended for business data processing. The software that transforms it is divided into three modules: word processing that lets users create, store, retrieve, and modify documents; advanced text management that provides a dictionary for automatic proofreading, hyphenation, and multilingual translation; and a management communications and support package that establishes an electronic mail system able to annotate, send, forward, or redirect mail, as well as file documents. All run under Prime's Primos operating system, have a one-time license fee of $15,000, and will be available in July.

Rather than develop the software from scratch, Prime acquired it from one of its customers, ACS America Inc., a New York City systems house. Prime president and chief executive officer Kenneth G. Fisher says that as software becomes more important to systems, outside development may be the best route for both the systems supplier and the software house. "If it's more expeditious for us to go outside, we will," he says. "We give a software package stability and the documentation it needs and can market it and distribute it in a way a smaller company couldn't." **-Anthony Durniak**

GenRad's 2245 In-Circuit/Continuity Tester.

GenRad's 2245 costs less than one-fifth what you'd pay for a functional or in-circuit test system.

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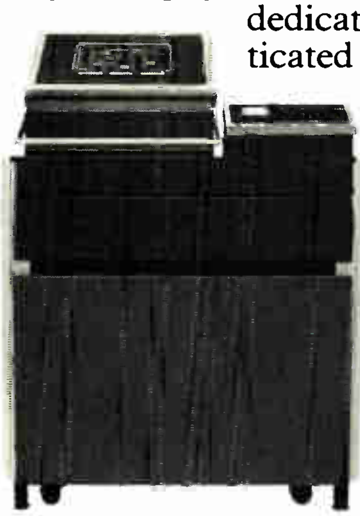

GenRad's 2245 In-Circuit/Continuity Tester offers you some other benefits as well. You can use it to test cables, box wiring and backplanes. You can program it in minutes. And thanks to its fixturing interface and cassette program storage, you can set up for a new board almost immediately.

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an option on the SVP, which has from 32 to 64 kilobytes of main memory. With a 500-kilobyte single-sided double-density diskette, terminal, and business-graphics software package, it sells for between $12,000 and $20,000.

The low end of the 2200 series, the new PCS-III, will maintain the $6,500-to-$10,500 price of the PCS-II it replaces for the very small business machine market. It incorporates single-sided double-density diskettes for up to 140 kilobytes of storage per drive. A disk multiplexer, the 2280, will allow up to three of the PCS-III or the larger 2200 computers to share the $2,000 hard disk. For all its 2200 family members, Wang is offering a code-generating software package: Ideas, for inquiry data entry access system.

"You don't need to know a computer language to program with Ideas," says Gagliano, because the software provides the user with a menu and then programs as requested. The $1,000-per-license software develops complete applications systems for data entry, inquiry, file management, and report generation.

Growth. The attraction for all this new technology is a market expected to reach $1.3 billion worldwide this year, according to a recent report by Creative Strategies International. The San Jose, Calif., market research firm predicts compound annual growth rates of 42%, so sales would top $3.7 billion by 1984.

With this in mind, Hazeltine will be pushing into the stand-alone word-processing systems market with its Opus 80. Based on a distributed logic design, the shared-resource system will support up to six work stations and three printers.

The Greenlawn, N. Y., firm has integrated intelligence throughout the system using multiple 8086s to oversee word processing in the work stations, to control 800 kilobytes of floppy-disk and 29 megabytes of hard-disk archives, and in the central processing unit. Initial deliveries are to begin in the fourth quarter; pricing will be announced in June.

Meanwhile ADDS, which has had its System 75, an 8080-based intelligent terminal, on the market for some time [*Electronics*, April 12, 1979, p. 42], is looking for a totally new market in small-business computing. The Hauppage, N. Y., company's family of small business computers consists of three vertically mountable components: the Multivision 1, containing an 8085A microcomputer with all input and output control needed to operate the two integral minifloppy disk drives and most standard display terminals; the Multivision 2, which adds an 8-in. Winchester hard disk in a second enclosure; and the Multivision 3, with which the user can add support for up to four display terminals and three additional terminal ports.

Prices for Multivision 1 start at $3,785, with a typically configured Multivision 3 selling for $12,885. The company will market them through retail computer stores and office supply outlets.

-Ana Bishop and Pamela Hamilton

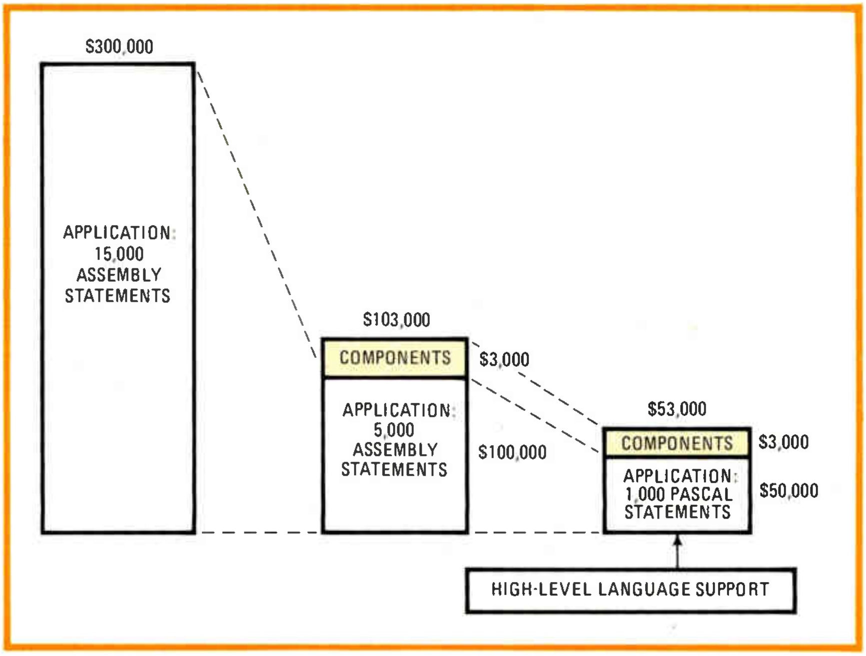
Software

Routines in ROM are hardware-like to allow modular programming

Texas Instruments Inc. is adding to its stable of 9900 software products in silicon with a new line of system programs, called software components, for the 16-bit microprocessor. These chunks of TI-written code are intended to execute out of read-only memory and can save the systems builder significant development costs, especially when used with high-level language support.

The first two products in the new line are a real-time executive and a file manager. TI says they potentially can reduce a 15,000-line, $300,000 application written in assembly language to a $53,000, 1,000-line Pascal program (see figure).

Some other semiconductor companies have been promising to contain ballooning program development costs by integrating more software components into ROM, but this latest announcement from the Dallas company adds to its long-standing commitment to solid-state software—a



Reducing plan. When used with a high-level language like Pascal, TI's system software components in read-only memory can dramatically whittle programming costs.

term it coined years ago. It already offers a program-debugging package called Tibug and executive modules called Timber [*Electronics*, May 10, 1979, p. 50], and its version of the Basic programming language, Power Basic, can be configured for ROM-based applications.

Modular. The new software components will allow a programming problem to be approached modularly, in much the same way that hardware is designed, says Kenneth Wickham, microprocessor software manager for the Dallas company's U. S. semiconductor group. Indeed, the real-time executive provides a kind of software bus to which other modules like the file manager are attached if they follow the executive's conventions for communications and parameter passing.

TI will also be offering interfaces to support other high-level languages. In the future, the file manager will talk to magnetic-bubble memories.

The software components will be shipped on disk, and the user will be able to tweak them before putting them into ROM. He will be provided with both the source-code version of the programs (written in Pascal) and the machine-language object code.

Thus there are many options for execution; if the application is written in Pascal, it can be joined with the Pascal versions of the system software and either compiled or interpreted. Another possibility is execution of the modules in machine code. **-John G. Posa**

Consumer

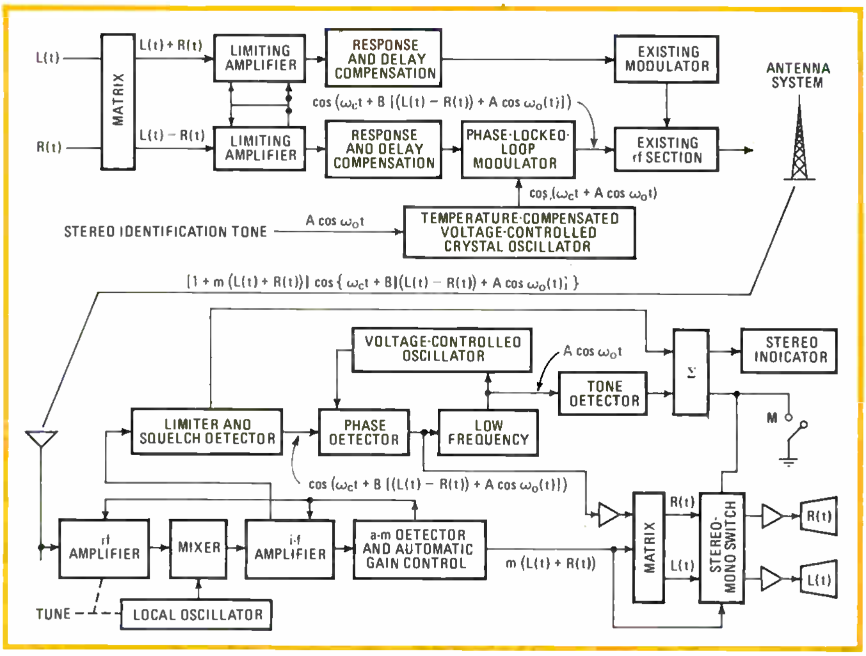
Magnavox stereo OK'd for a-m radios

The dust is settling from the Federal Communications Commission's selection of the Magnavox stereophonic a-m broadcast technique over four competitors—but the criteria by which the FCC made its decision still are not clear.

The basis for the 4-to-2 vote, with 1 abstention, has not been disclosed, although the industry has waited three years for the FCC to evaluate the systems. The commission was under industry and congressional pressure to come up with a single selection, but losing competitors may well challenge the outcome in court.

The technique devised by Magnavox Consumer Electronics Co., Fort Wayne, Ind., is relatively simple, according to its designers. To encode and broadcast stereo, Magnavox forms the sum and difference of left and right audio channels. The summed audio signal amplitude-modulates the carrier and the difference signal linearly phase-modulates it (see figure).

Identification. In addition, a 5-hertz subaudible tone is frequency-modulated onto the carrier for stereo identification by the receiver. The



Magnavox way. A-m stereo system puts left-plus-right channel information on a-m channel and left-minus-right on linearly phase-modulated channel. Phase deviation is 1 radian peak.

SBS sets satellite launch date

It's countdown time for Satellite Business Systems Inc.'s first satellite, which will be the world's first satellite-based business communications facility with customer-dedicated earth stations. The much-awaited Oct. 23 launch date is firm and represents a $375 million investment even before operational readiness is achieved, says Robert C. Hall, president of the McLean, Va., company. He notes that the likes of Aetna Life and Casualty, Boeing Computer Services, IBM, and the Travelers Insurance Company will be enjoying computer-to-computer communications, electronic mail, and video conferencing, among other services.

But a company will not have to be a giant to use the SBS system. Hall says it will also be possible for smaller customers to hook up by means of shared-facility use. According to industry observers, this statement, made to a Society of Security Analysts meeting in New York, represents a shift in SBS's market attitude. In previous times—less uncertain economically—it did not talk much about smaller customers and shared facilities.

Hall also said that SBS is seeking to get Federal Communications Commission authorization to conduct a demonstration of satellite communications involving mobile-radio and cable-TV links. It would be in conjunction with two other organizations—Tymnet Inc. and LDC, which is in turn a partnership between Aetna and M/A Com Inc. **-Harvey J. Hindin**

NO. 10

NATIONAL ANTHEM

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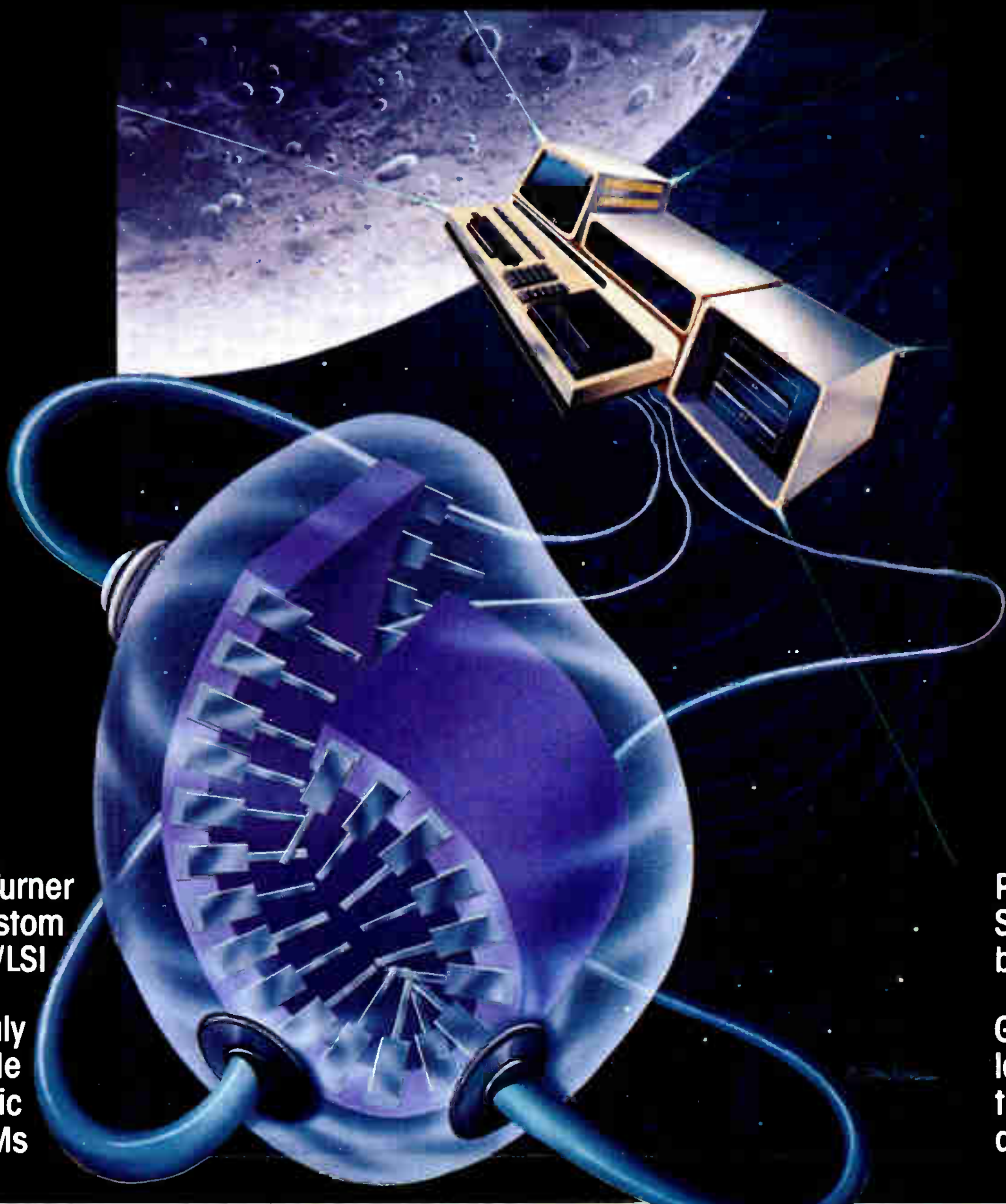

Mike Turner on Custom MOS/LSI

Truly reliable 16K dynamic RAMs

Practical Series/80 boards

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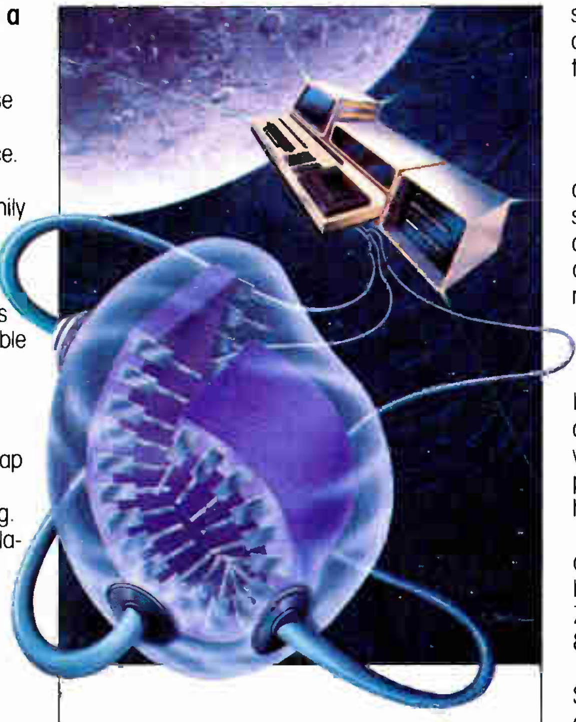

What is ISE?

National's ISE is a separate STARPLEX module housing 32K bytes of real-time map memory, plus all the necessary logic for breakpoints, tracing, and memory mapping. These resources are available for the emulation of any processor, since the individual emulation packages are the only components dedicated to particluar processors.

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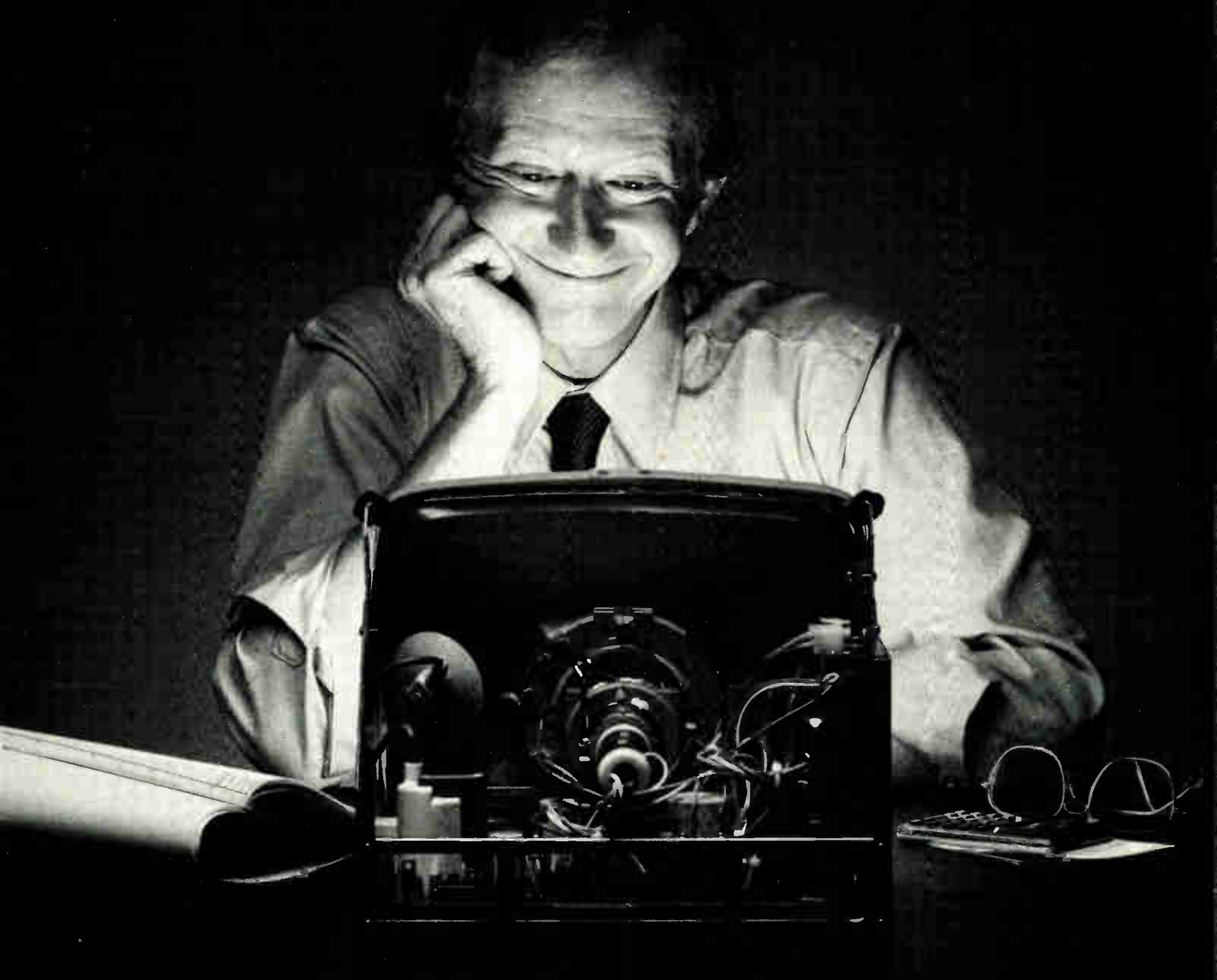

same tone can also carry other digital information to the receiver, such as time, frequency, or call-letter identification.

To reduce incidental phase modulation, transit time and amplitude are equalized in both sum and difference signal paths by compensating networks. All existing a-m transmitter equipment is easily supplemented with the mixing and modulation equipment needed for stereo.

Receiver. Decoding the transmitted stereo information in the receiver requires a limiting and phase-detection circuit, followed by a mixing network to recover left and right channels from the sum and difference signals. The 5-Hz stereo identification tone is extracted to switch the receiver from monophonic to stereo reception.

Magnavox feels that the main advantage of its system—and presumably a factor in its success—is that it can use a single intermediate-frequency stage and a standard envelope detector for the a-m channel, both common design techniques. Also the phase-modulated audio can be recovered with present integrated-circuit technology.

Competing systems submitted to the FCC came from Motorola Inc., Schaumburg, Ill., Belar Communications Corp., Devan, Pa.; Kahn Communications, Freeport, N. Y.; and Harris Corp., Cleveland, Ohio. Industry expectations are that one or more will challenge the commission's choice.

Stereo is seen by observers as major justification for manufacturers to produce higher-fidelity, better quality a-m receivers, which in turn, it is hoped, will rekindle consumer interest in the a-m bandwidth. It is estimated that 80% of the market for the receivers will be for installation in autos, since a-m broadcasts do not suffer the line-of-sight limitation on range that the higher frequency fm signals do.

In tapping Magnavox alone, the FCC has dispersed the specter of several mutually incompatible stereo systems appearing in the marketplace. Broadcasters, at least one of which has expressed apprehension

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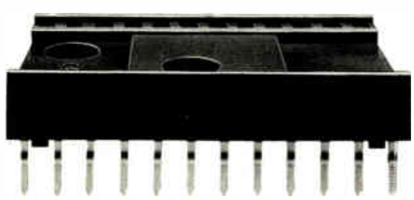

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*Patent pending

about the reduced modulation level of a-m stereo [*Electronics*, April 14, 1977, p. 82] would have been further burdened by having to conform to a multistandard system.

The decision to stay with one approach has also minimized the cost of adding stereo circuitry to the receivers. In fact, Magnavox says its system will have a negligible effect on the overall retail price.

However, another year may pass before one sees any a-m stereo equipment for sale, according to a Magnavox spokesman. He cites a number of reasons, among them a request to the FCC by the Electronics Industries of America that the installation of stereo broadcast equipment be postponed for nine months to give retailers time to clear their shelves of current inventory.

Once started, installation of stereo broadcast equipment will take four to six months. At that time Magnavox intends to have the stereo receivers available to consumers and says it will make the technology available to other radio makers.

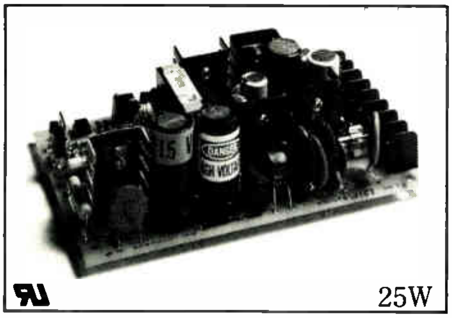
One spur to the U. S. market is expected to come from Japan, with its vast exports of cars and radios to this country. "But don't count on that fast market growth in cars," says an FCC staff member, noting it could be slowed "if the recession gets serious." **-Gil Bassak, Ray Connolly**

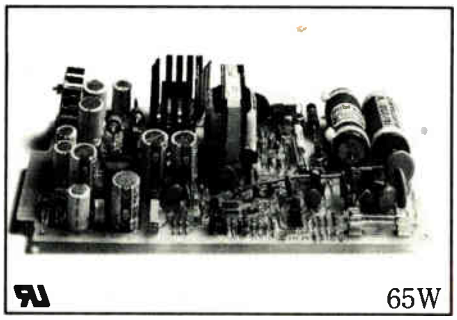
News brief

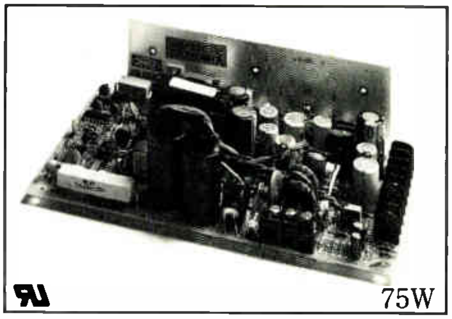
Siemens buys into Threshold

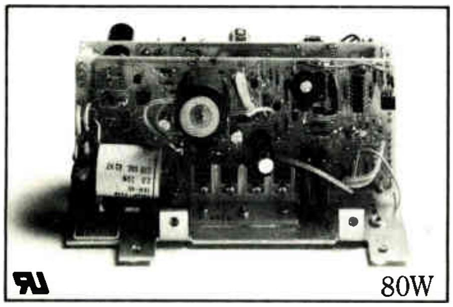
Threshold Technology Inc., known for its innovative work in speech recognition, has a new investor—the Munich firm Siemens AG paid $2 million for 24% of the stock and for $800,000 in subordinated convertible debentures, and a private investor bought an equal amount of the debentures, says Thomas B. Martin, Threshold's president. A portion of the proceeds will go toward the development of microprocessor-based speech-recognition equipment being worked on with the Delran, N. J. company's recently acquired semiconductor-development company, Auricle Inc.

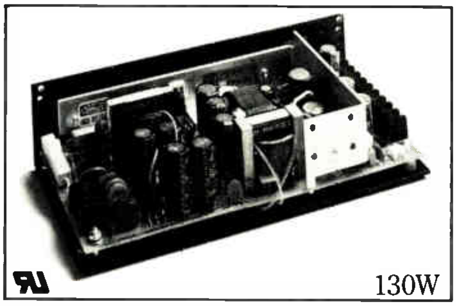
People are switching to Boschert

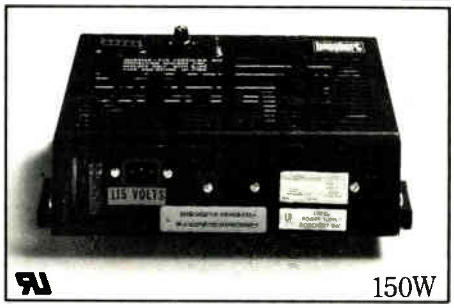


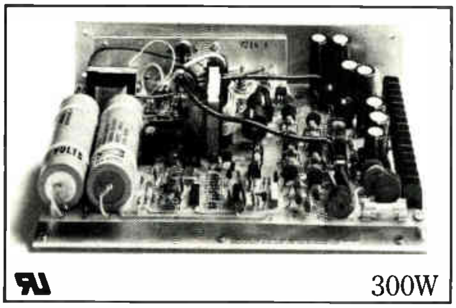


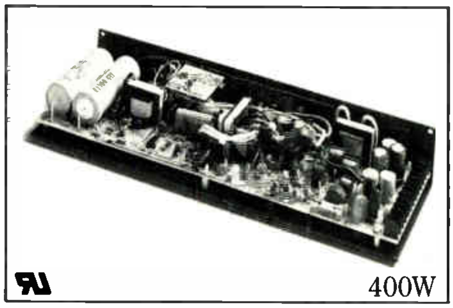












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Circle 57 on reader service card

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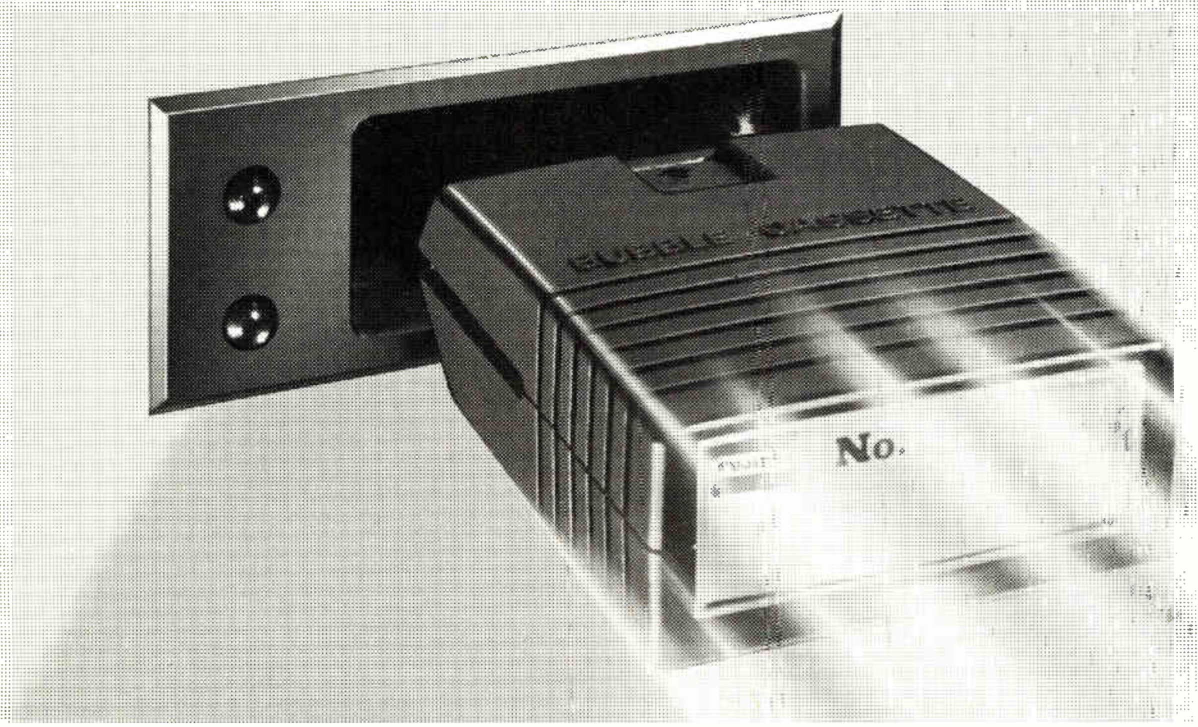

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Circle 59 on reader service card

Transatlantic cable using fiber optics forecast by 1988

Now that fiber-optic communications technology is proving its feasibility on land, and researchers are turning to the sea [*Electronics*, March 13, p. 39], the world's first transoceanic fiber-optic submarine cable could come as early as 1988. That transatlantic cable, dubbed TAT-8, would have three European landing sites and one in the U. S. It will be described at the April 22–25 meeting in Ferndown, England, of the North Atlantic Consultative Working Group as **one of seven possible options in U. S. cable and satellite plans for the 1986–1995 period.** The American input for the international planning session was prepared by a committee representing the Commerce Department's National Telecommunications and Information Administration, which recommends White House policy; the Federal Communications Commission; the Communication Satellite Corp.; and U. S. international communications carriers. Other options call for a fiber-optic cable in 1990 or 1992. The most optimistic plan also calls for beginning the replacement of the Intelsat V communications satellite with a larger Intelsat VI series as early as 1986.

Air Force tests LLLTV for A-10 gunship

The Air Force may successfully convert its Fairchild-Republic A-10 tank-busting aircraft to night and adverse weather operations following successful tests of a General Electric Co. low-light-level television (LLLTV) system that would complement the plane's forward-looking infrared (FLIR) system. Flight tests at Edwards Air Force Base, Calif., **show that the LLLTV as a night terrain-following sensor permits operations as low as 300 ft** for target identification and enhanced armor target location when dust, ground clutter, or nonoperating (cooled-down) vehicles reduce the effectiveness of FLIR. GE says its Utica, N. Y., operation is developing improved LLLTV optics; an advanced, third-generation image intensifier for use at lower ambient light levels, plus new video processing to neutralize bright point source light—like searchlights—in a scene and to prevent a relatively bright horizon's suppression of a scene's foreground details.

U. S. to upgrade its German net

The price tag to the U. S. for upgrading the circa-1940 military telephone network used by American forces in West Germany will be more than $125 million under a mid-April contract signed by the U. S. Army with the Deutsches Bundespost. **The West German telecommunications authority's contractor consortium is headed by Siemens AG.**

Landsat-D stalled as Hughes, GE run into problems

Sharp cost overruns and delivery delays by Hughes Aircraft Co. and General Electric Co. are causing the National Aeronautics and Space Administration to restructure the Landsat-D program, the fourth and most advanced earth resources-monitoring satellite. Hughes is having problems developing the new thematic mapper that would define earth imagery in more spectral bands and with a resolution to 30 m, more than twice that of multispectral scanners in the three earlier Landsats. NASA's Goddard Space Flight Center at Greenbelt, Md., also says GE has run into cost and schedule delays developing its flight and ground system for the satellite. Working with the National Oceanic and Atmospheric Administration, which operates the Landsat systems, NASA **says it may opt for launching Landsat-D and a backup with only available multispectral scanners,** or try launching one with a scanner, followed by another launch as soon as possible with both scanner and thematic mapper.

Washington commentary

The FCC's spur to Congress

In some quarters of Congress, the Federal Communications Commission's "final decision" this month in its Second Computer Inquiry is beginning to be called "the Bell Bill buster." Being designed to deregulate most telecommunications equipment and services, it obviates the need to rewrite the Communications Act of 1934, or so the feeling goes.

But that conclusion is as inaccurate as the description of the decision itself, for it is hardly final (see "AT&T ruling faces challenges," p. 104). Nevertheless, some congressional and communications industry advocates of dropping legislation plans as no longer necessary are beginning to be heard.

The "Bell Bill buster" is a misnomer on at least two counts. First, the legislation at stake is not the misbegotten Bell bill introduced into an earlier Congress and long since dead despite its support by American Telephone & Telegraph Co. and other carriers. Second, the FCC's April ruling has probably done less to bust the chances for passage of pending rewrites of the Communications Act than have the actions of the Congress itself.

Certainly this election year's legislative calendar is running out of time for consideration of such bills, which have been sponsored in the House by Rep. Lionel Van Deerlin (D., Calif.) and in the Senate by Ernest Hollings (D., S. C.). Even Van Deerlin, communications subcommittee chairman, concedes that his rewrite is in trouble. But it was in trouble in the House itself before the FCC decision.

Keeping the fire alight

None of that, however, diminishes the need to update the 1934 Communications Act to recognize the changes that have come in technology and the evolution of a competitive U. S. telecommunications industry. That need is supported by the fact that the FCC's deregulation action was spurred mightily by the prospect of legislation that threatened to restructure the commission. "Congress lighted a fire under the commission and it responded," observes one Washington communications lawyer. "Now Congress must not let that fire go out."

FCC commissioner Tyrone Brown put it another way: "Without the benefit of the debate that has occurred in the House and Senate communications subcommittees over the past two years, I doubt that the FCC would be ready to act. I would welcome congressional confirmation—or modification—of any aspect of our decision, particularly our construction of the 1956 consent decree" by which AT&T settled a Federal antitrust suit by limiting its business to regulated markets. "Without such confirmation," Brown goes on, "full implementation of our decision may be delayed by years of litigation. In any event, I wish to emphasize that my vote in favor of the decision rests in substantial part on the view that, as a legal matter, regulated carriers, including AT&T, can compete in unregulated fashion in the enhanced services and equipment markets" through arm's-length subsidiaries.

New calls for action

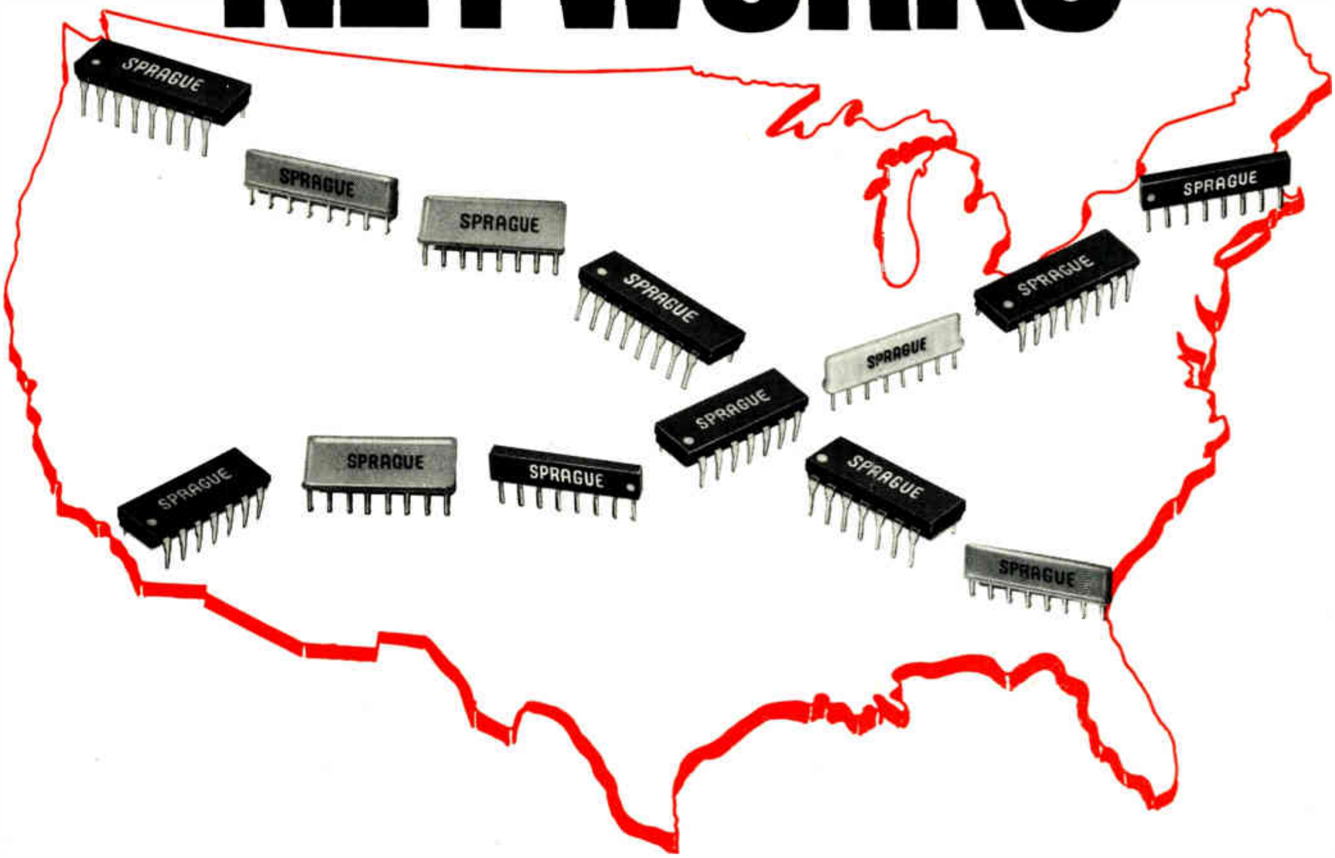
Since litigation of what Brown and others regard as perhaps the FCC's most important decision is virtually guaranteed, Congress must indeed act. National Telecommunications and Information Administration chief Henry Geller concurs in that view, and calls for action are coming from such diverse other interests as AT&T, the U. S. Independent Telephone Association, the Computer and Communications Industries Association, the Justice Department, and Congressman Van Deerlin himself.

AT&T vice chairman Janes E. Olson still wants "a legislative solution to the issues confronting our business" and says that "we shall continue to pursue that course." The Independent Telephone Association likes the idea of freeing telephone companies to compete, but still wants Congress "to resolve the basic issues relating to telecommunications competition." CCIA president A. G. W. "Jack" Biddle wants Congress to strengthen the safeguards against cross subsidization by common carriers of their new competitive hardware and software businesses with regulated telephone revenues. While he favors legislation, Biddle says Van Deerlin's revised H. R. 6121 bill "has a long way to go before it is satisfactory." The Justice Department, too, wants legislation that resolves the problems of the FCC's construction of the AT&T 1956 consent decree so that, explains one Justice source privately, "we won't be in the awkward and embarassing position of having the executive department suing another Federal agency."

In the face of all these renewed calls for telecommunications legislation coming on the heels of the FCC's decision, it can hardly be construed as a "bill buster." Indeed, it seems the opposite is true. The controversial FCC ruling could be the most important spur to Congress yet to appear.

-Ray Connolly

COAST-TO-COAST NETWORKS



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Pull-up/Pull-down 14 Pins, 13 Resistors	34A . . . 4 314A . . .	899-1-R . . .	760-1-R . . .	**914C . . . X2PE**
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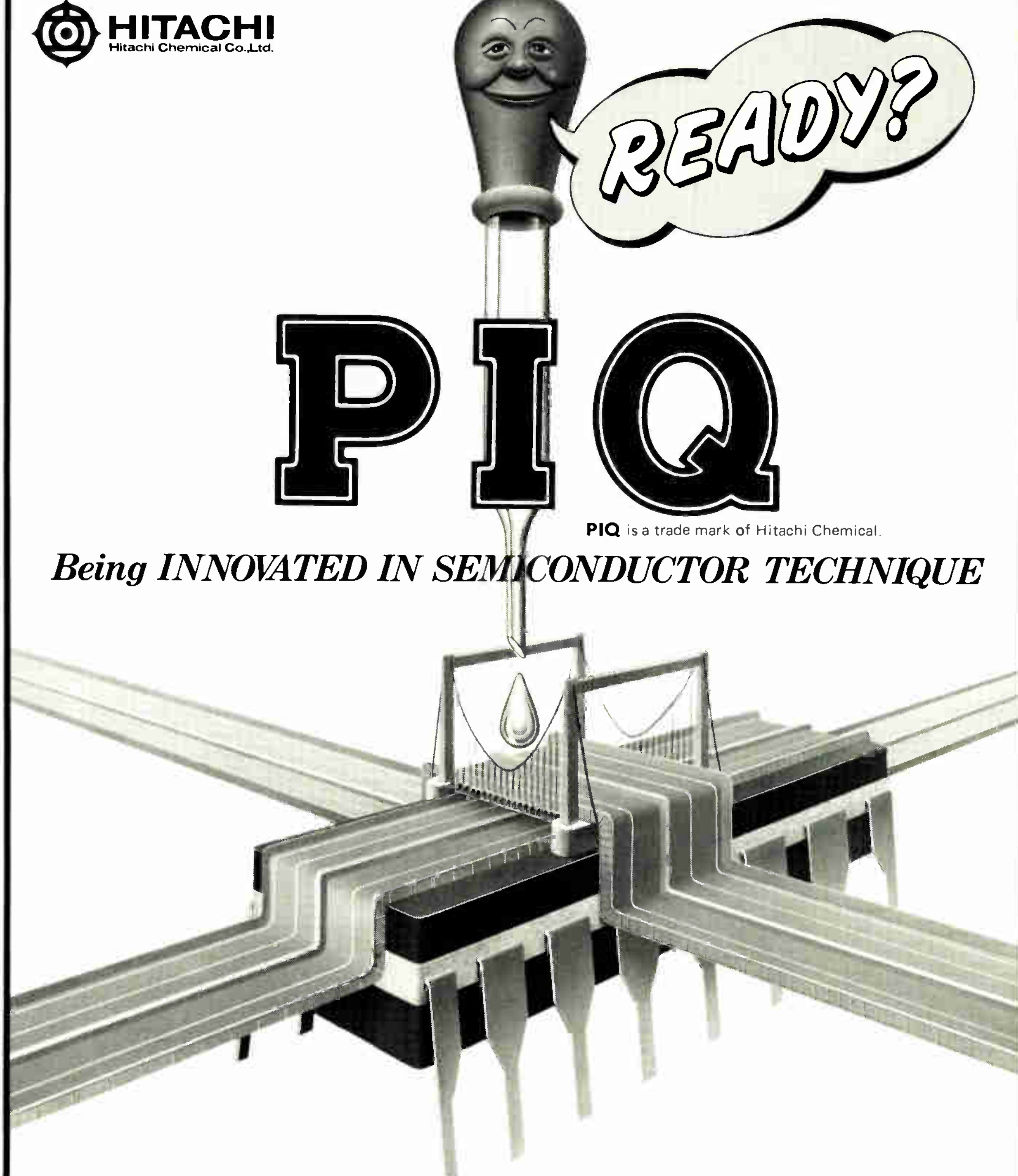

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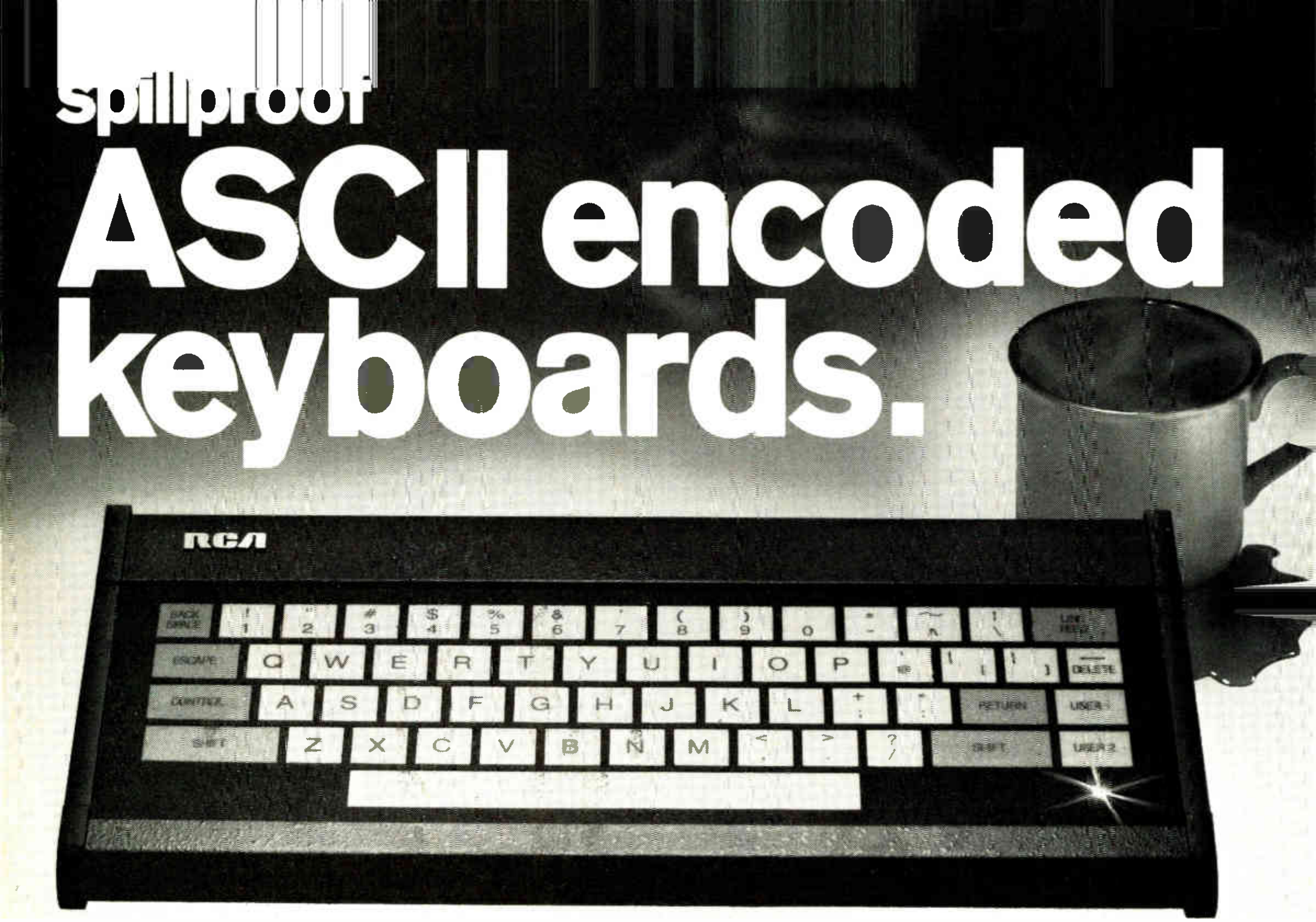

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- 3 ASCII encoded outputs: EIA RS232C compatible. 20 mA current loop. TTL.
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- Six baud rates, switch-selectable.
- Power-on or "prompt" LED indicator.
- 25-pin output socket mates with male "D" cable connector.

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St.-Gobain purchases Olivetti share

The purchase by St. Gobain-Pont-à-Mousson, Paris, of some 15% of C. Ing. Olivetti & Cie., the Italian office equipment maker based in Ivrea, near Turin, should strengthen the French conglomerate's diversification into electronics. The deal has reportedly found explicit support from the French government and backing by the Trade Commission of the European Community. It seems to presage a move by some in Europe to establish a **strong continental industry linkup that would be capable of competing with U. S. and Japanese giants, in particular with IBM Corp.** St.-Gobain currently controls 22% of CII-Honeywell Bull and makes no secret of its ambition to eventually obtain majority control of the Franco-American mainframe maker. CII-HB has been looking for a distribution network for the line of electronic office-equipment it plans to unveil shortly, and the tie-in with Olivetti could fill the bill. Olivetti, which has recently signed agreements with Japan's Hitachi Ltd. and the U. S.'s IPL Systems Inc. on medium-sized and large computer leasing, would win access to St.-Gobain's considerable cache of investment funds. St.-Gobain last year also began setting up Eurotechnique SA, near Marseilles, a joint integrated-circuit venture with National Semiconductor Corp.

Omega initiates touch sensors for wristwatch

The prestigious Swiss watch company Omega is introducing what it says is the world's first wristwatch to use touch sensors at this week's Basel Watch Fair. The quartz watch **boasts nine different programs activated by rubbing a finger over a flat capacitive sensor surface** and identified by symbols. It uses a 70-mm^2 complementary-MOS microprocessor chip and a specially developed linear chip to handle the sensor's signals. Research work on the sensor problem was begun at the Centre Electronique Horloger at Neuchatel and developed by Bienne-based Omega. The watch has a 12-digit, two-row multiplexed liquid-crystal display showing the time in hours, minutes, and seconds and the day and date, plus these programs: chronography with a split-lap possibility and 24-hour capacity, countdown functions with a signal given at a specified time, an alarm on a daily or a one-time schedule, chiming of the hours, two agenda functions for storing information (like a birthday) with a displayed signal, and a second time-zone indicator. The watch is some 9 mm thick, 35 mm long, and 34 mm wide (0.35 by 1.4 by 1.3 in.). Omega says the watch, to go on sale this summer, is geared for mass production. The price is about $280.

UK to test electronic mail

An electronic mail service some 50 times faster than the conventional 50-/75-baud Telex service and incorporating sophisticated store-and-forward terminals will go on trial in the United Kingdom later this year. The tests, to be held by the British Post Office at 150 sites, are paralleled by similar moves in Europe and Canada and **aimed at establishing an international electronic mail service,** designated Teletex, by 1982. West Germany in particular will establish its public national Teletex service next year. The new services will be compatible with existing Telex service and also with the BPO's viewdata service. The modular terminals for the UK trials are built round a store-and-forward switching unit from Racal-ESL Ltd. that interfaces both with the Telex net and with a 2,400-baud modem. A cathode-ray-tube display, a printer, and disk storage are also available.

Thomson-CSF to enter VLSI lithography arena

Thomson-CSF figures it has the technology and the marketing muscle to become a major supplier worldwide of lithography equipment for very large-scale integrated circuits and will back its instrument-making subsidiary Cameca with some $20 million to get into the business. Prototypes of a 1-μm wafer stepper and a direct-writing electron-beam machine will come out of the parent company's central research laboratory by the end of the year. **The wafer stepper's specifications call for a throughput of up to 80 4-inch wafers an hour** with an alignment accurate to ± 0.2 μm for chips up to 10 by 10 mm. For the electron-beam unit, the throughput will be 10 3-in. wafers an hour at 1-μm line widths, with 0.3 μm possible at a lower throughput. The Paris-based company says its machines will be competitively priced.

Philips launches its first 16-bit minicomputers

Four minicomputers and a microcomputer are the first products from Philips Data Systems France using Philips' new 16-bit FAST n-MOS P 800 microprocessor [*Electronics*, Nov. 22, 1979, p. 63]. The Paris-based firm notes that software developed for Philips' 8-bit minicomputers can be used without modification in the new 16-bit devices. The P 853, P 854, P 858, and P 859 **minis, as well as the PSBC P 870 single-board computer, are all designed for industrial production applications.** The P 853 can handle up to 64 kilobytes of erasable programmable read-only memory. It uses software developed for its predecessor, the P 851, but with a 15% improvement in average time per operation. With 32 kilobytes of memory, the P 853 will sell for about $4,900, nearly $300 less than a comparable P 851 configuration. The top-of-the-line P 859 has 16 registers and a maximum memory capacity of 1 million bytes. Cycle time is 0.65 ns. (See also story on p. 82.)

Oki gives up plans to buy U. S. chips

Oki Electric Industry Co. has announced that it is abandoning plans to have Silicon Valley firms make chips under contract for the U. S. market. The company says it ordered samples from three unnamed suppliers but was dissatisfied with the quality. For the moment, **this decision eliminates Oki's American "base," but the company is carefully studying construction of a plant there instead.** It asked for the samples last year because its domestic plants are too swamped to supply all the demand coming from the U. S. Oki supplied the masks for complementary-MOS large-scale integrated circuits for watches, among others.

Siemens' ink-jet printer triples predecessor's speed

Upgrading its PT80 impact printer, Siemens AG is coming out with an ink-jet version, the PT80i, which, at 270 characters per second, is three times faster than its predecessor. The new version, introduced at the April 16–24 Hanover Fair in West Germany, uses an 8085 microprocessor to control the bidirectional printing mechanism, the optimum direction depending on the makeup and layout of the text. Bidirectional printing ensures that the print head covers as few empty areas as possible. The head has **12 vertically arranged ink jets that can produce up to 125 different high-quality characters in a 12-by-9-point matrix.** The machine, which uses regular paper, can be switched for normal, cursive, and wide-character (twice as wide as normal) printing. With appropriate character generators, the PT80i can produce national alphabets as well as the standard ASCII international character set.

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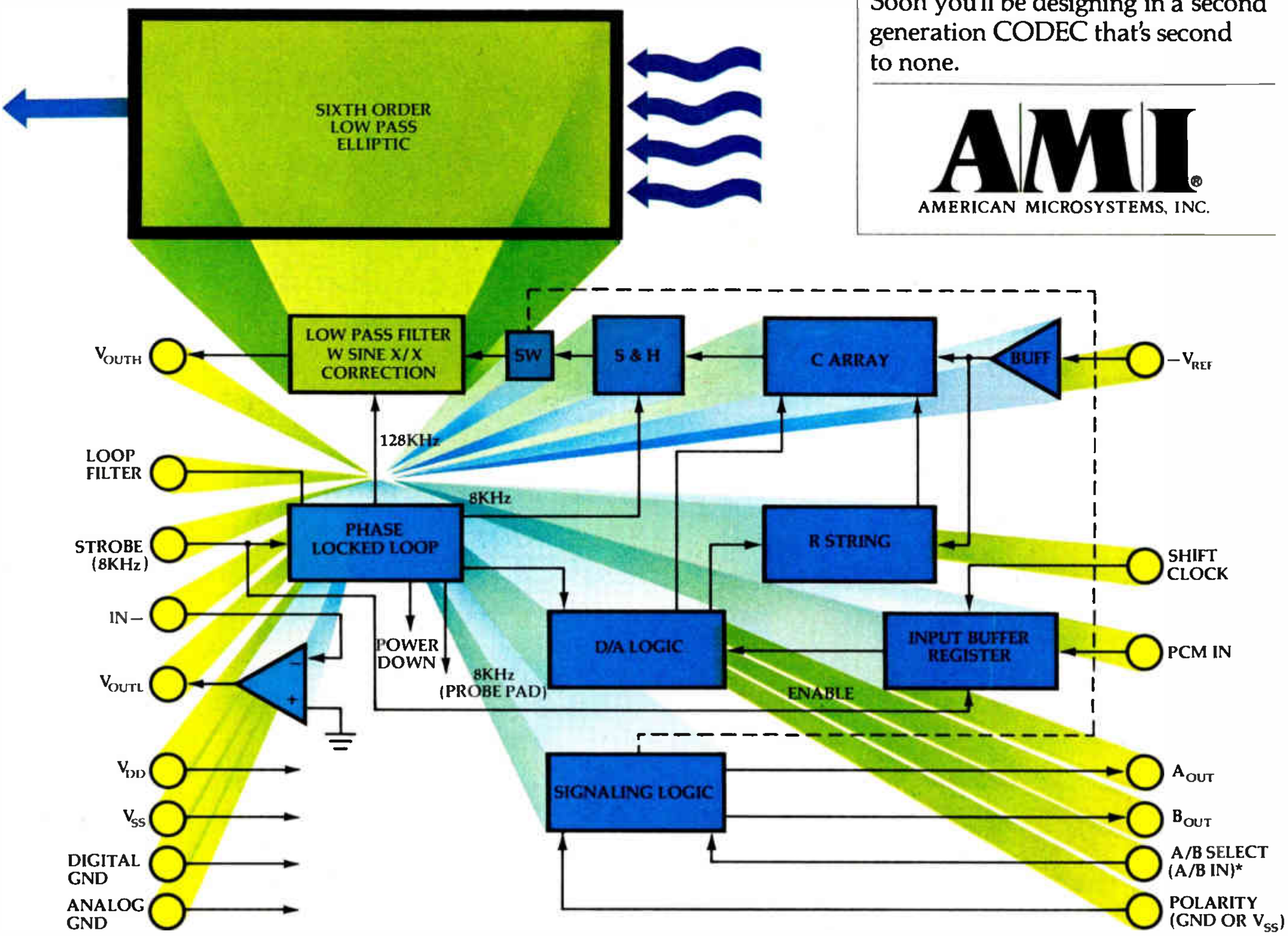

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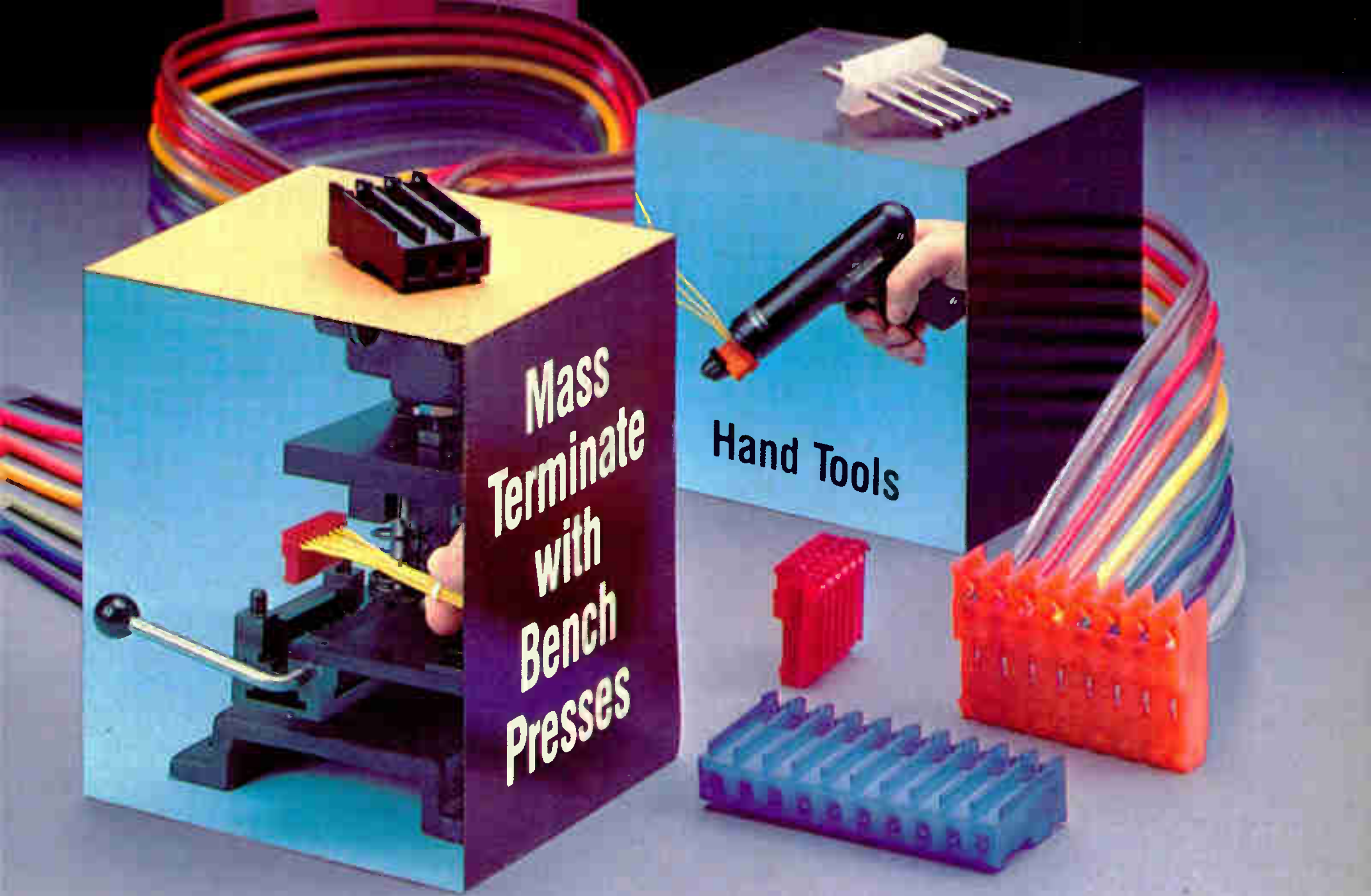

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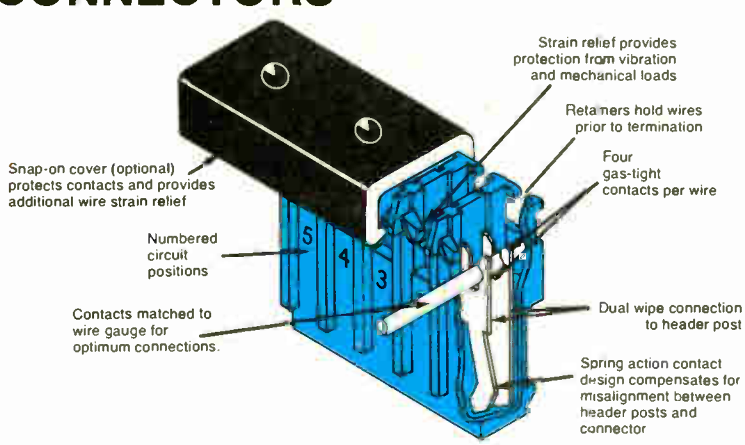

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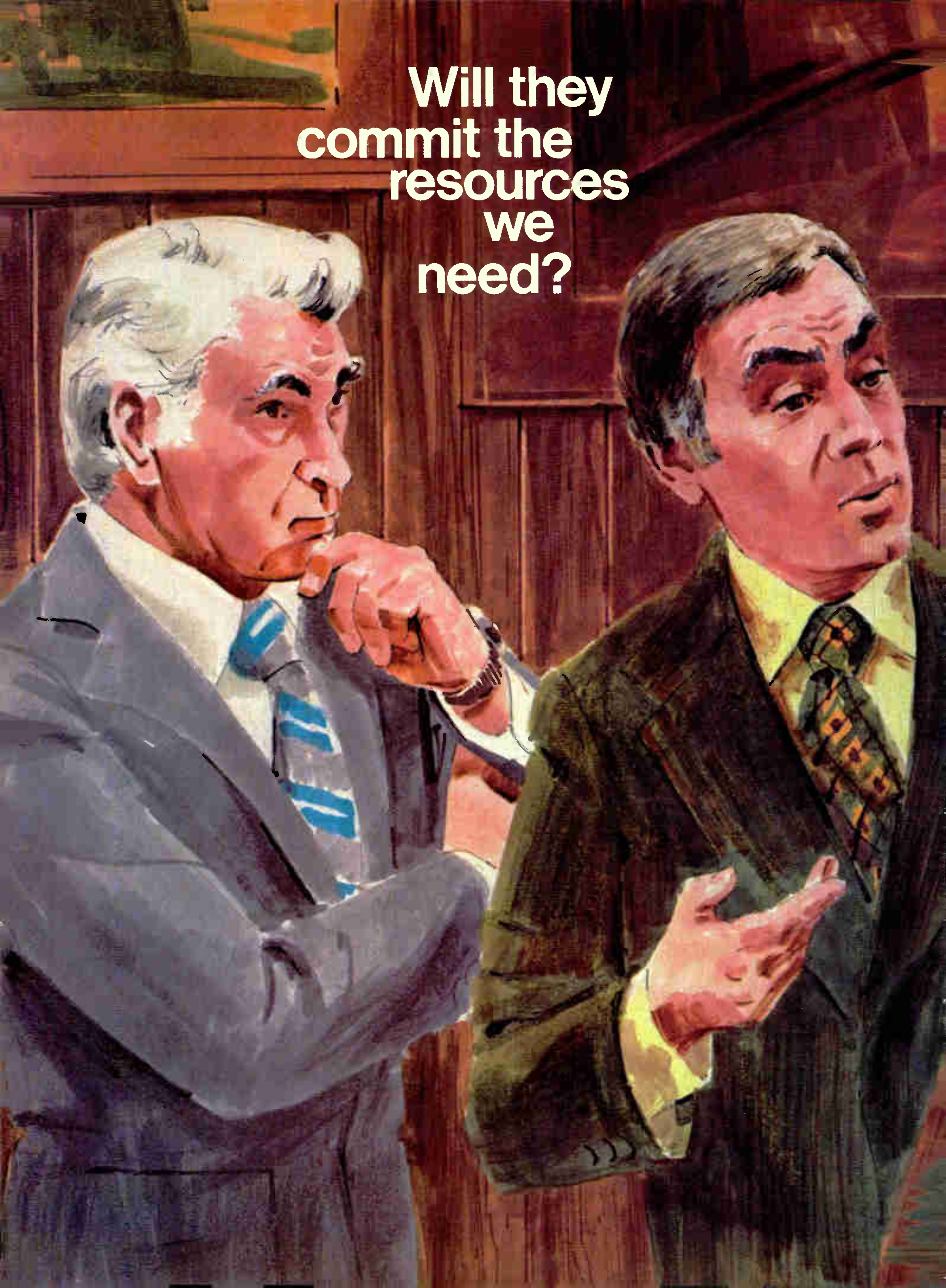
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96-by-96-cell array processes images in real time

by Kevin Smith, London bureau manager

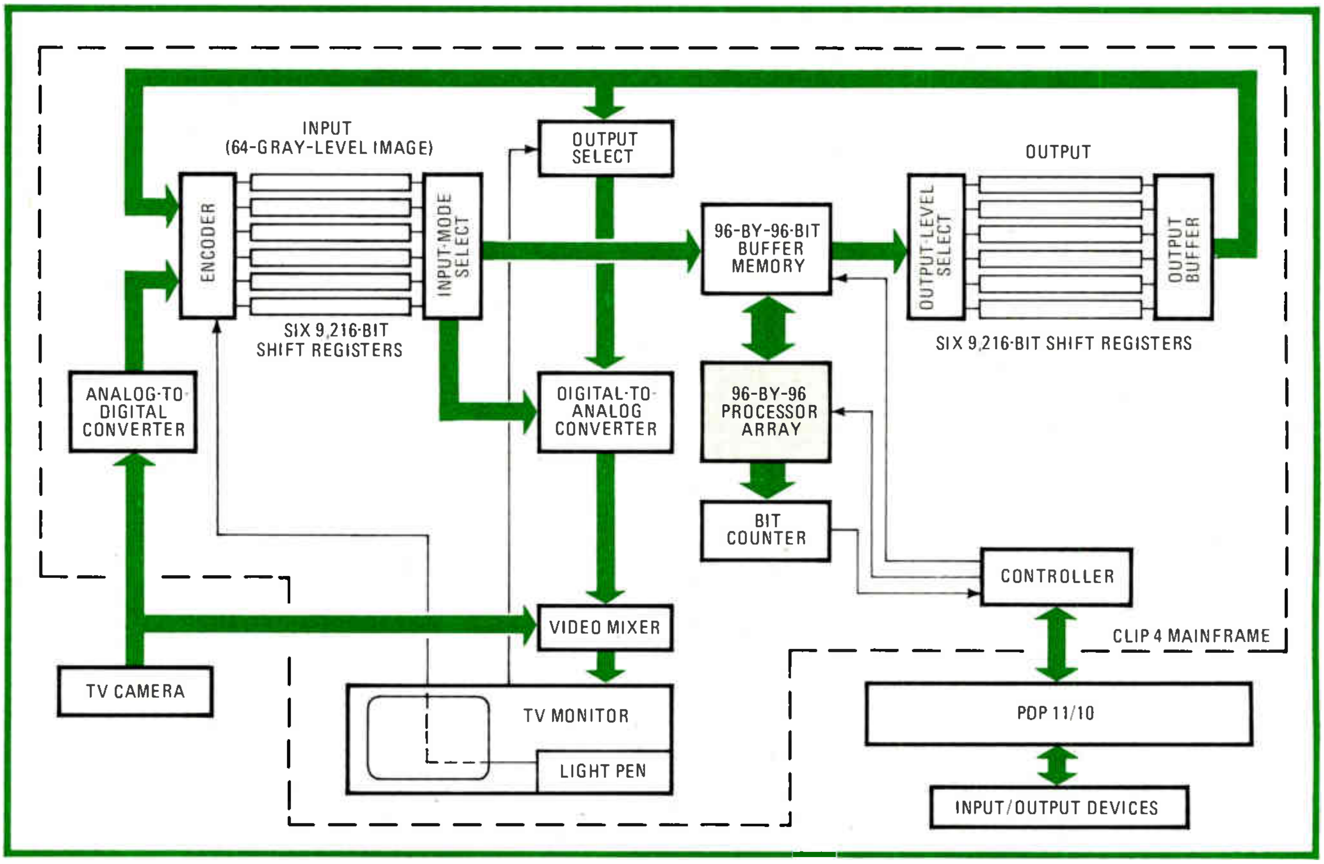
Using 8 processors per chip, prototype breaks TV camera image into 9,216 elements processed in parallel

Conventional serial digital computers have proved slow and altogether ill-suited to pattern recognition. To break a long-standing roadblock that has prevented the development of optically guided robots, reading machines, and inspection systems, researchers at University College, London, are exploring alternative approaches using an army of parallel processors.

Now being commissioned there, under the direction of Michael J. Duff of the department of physics, is an array processor called CLIP 4—for cellular logic image processor—comprising 9,216 1-bit processors in a 96-by-96-cell array. Unlike conventional optical character recognition machines, the CLIP 4 can process images in real time and interfaces with a TV camera that transmits a picture having 64 levels of gray.

Though primarily a research tool, the processor, which was funded by Britain's Science Research Council, may soon be doing a real job: one machine has already been provisionally ordered by the Medical Research Council, which plans to use it for chromosome identification and classification.

Work on parallel processors at



Getting the picture. The CLIP 4, from University College, London, contains 9,216 1-bit processors, each corresponding to one pixel. It processes images, from TV camera, having 64 levels of gray. Gray scale is converted into 6-bit code stored on six 96-by-96-bit pages.

University College dates back to 1973, but it was not until this year that Duff was able to get his ideas translated into silicon. In the final version engineered by the custom design house, Swindon Silicon Systems Ltd., and processed by General Instrument's Microelectronics division, eight units are packed onto a single n-channel MOS chip approximately 180 mils on a side. The chip sits in a 40-pin package and is clocked at 1 megahertz (though the design target was 5 MHz). Each unit contains a single-bit Boolean processor, a 32-bit memory, and gating logic connecting neighboring units.

One for one. Extremely fast image processing is achieved by providing one image processor for each picture element in the camera image. Since many operations carried out during pattern recognition are localized, each processor both sends to and receives from its eight immediately neighboring cells. In seeking the edge of an object, for example, all picture elements are simultaneously examined in relation to their neighbors to identify those where black elements abut white ones.

A central controller transmits instructions to all the processors in the array, defining which of 16 possible Boolean operations are to be performed and setting up lines that control the flow of data both on chip and between chips. The controller is microprogrammed, with the control instructions stored in a semiconductor random-access memory for flexibility.

The whole system interfaces with a television camera and monitor through two groups of shift registers, each of which can store a 96-by-96-element image coded as a 6-bit gray scale (see figure). Analog-to-digital and digital-to-analog conversion between the registers and the camera and monitor, respectively, proceed at the full video rate.

Pages. Instead of handling all 6 bits that describe each portion of the image as a group, the computer processes six 96-by-96-element pages, each element of which contains a single bit of the 6-bit code. Single-bit pages of data are loaded serially into the first group of six 9,216-bit shift register external to the array. Their content is then reconfigured into another six 9,216-bit shift registers, which discharge their data into the array rows.

Duff estimates that a commercial version of the processor would cost in the region of $140,000 to make. That is probably some 10 times too expensive for general-purpose applications, but he can already see inspection tasks—especially in medical research—where the array image processor's labor-saving potential would pay for itself.

Though directed specifically at image processing, the University College work is part of a growing interest in parallel processing. The definitive paper on the subject dates back to S. H. Unger in 1958 and from it has stemmed several machines. But before parallel processing takes over from the Von Neuman computer, Duff remarks, people have first to learn how to write high-level programs for them.

West Germany

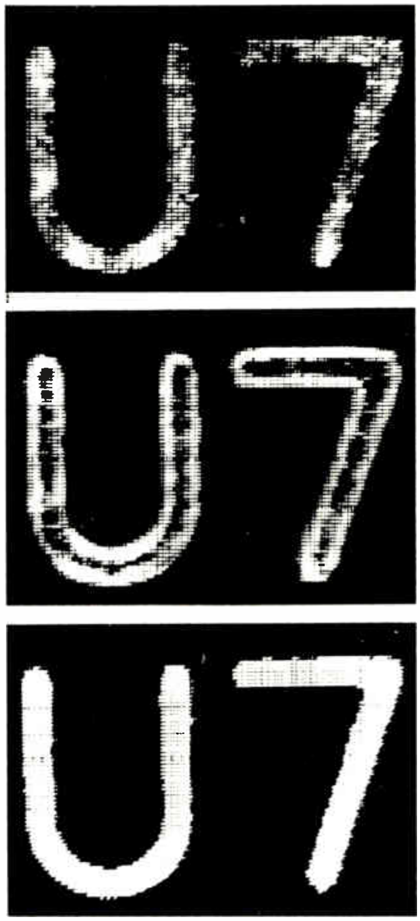
Image processor eliminates the grays

Optoelectronic methods for identifying characters, symbols, and object shapes automatically do not work reliably when the characters or objects involved have ill-defined, low-contrast edges or poor-quality surfaces. Researchers at Siemens AG have now found a simple way to overcome this limitation.

The method, developed at the company's Munich labs by Günter Doemens and Ulrich Hendricks, allows positive identification even of highly blurred images of characters or objects. Using analog techniques to convert images into blacks and whites only, it also considerably reduces the amount of data that must subsequently be processed.

Borrowed. In implementing their method, the researchers borrowed heavily from the physiology of human perception. As they explain it, a person differentiates between objects essentially by their edges; that is, he perceives primarily intensity changes, or transitions between light and dark, rather than absolute light or dark values. Mathematically, this kind of edge perception can be interpreted as a multidimensional image differentiation.

Such differentiation can be imple-



Differentiation. Siemens uses CCD technology to convert the poor-quality image at top (shown here in full contrast) first into one with the edges accentuated and the blurred areas suppressed (middle) and then to one whose internal areas have been made either pure black or pure white (bottom).

mented electronically by, for example, analog shift registers based on charge-coupled-device technology. With sufficiently fast microelectronic elements, even real-time image processing is possible.

That, indeed, is what Doemens and Hendricks have realized in a laboratory-type analog image-pro-

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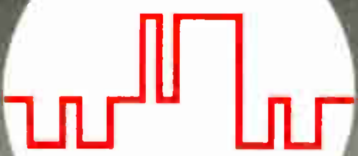

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cessing system they have put together using commercially available parts. It operates at a clock rate of 1 megahertz, which corresponds to a processing speed of 1 million analog picture elements, or pixels, per second. Once completed, the system will first be used in house for handling as yet unspecified tasks on Siemens' automated production lines.

Digital, computer-based systems, Doemens says, require minutes, rather than seconds, for processing an image and are therefore ill-suited to automated production. Siemens' system owes its speed to direct analog and real-time processing methods, eliminating the time-consuming data storage and retrieval needed for digital techniques.

From a blurry, low-contrast pattern with all its gray shades (see top photo), the new system produces a high-quality purely black-and-white image. First, the poor-quality pattern is scanned with a television camera using CCD sensors or with a linear array of diodes. The resulting analog voltage values, which are proportional to the image brightness, are continuously fed through a CCD shift register serving as an analog buffer memory. It can hold a matrix of six by six pixels.

Two-stage process. The pixels are then differentiated in all four directions of the matrix. In this process, the blurred or unsharp areas on the image surface are suppressed and the edges are accentuated. The image—its edges already well defined (middle photo)—is then fed to another analog CCD buffer memory, this one holding a matrix of five by five pixels. Next, by way of a so-called edge-detection logic circuit in the buffer, the image data is evaluated in all directions for all spots of maximum brightness, in order to make the edges even sharper.

Finally, in the last stage, a complete black-and-white image is produced by filling in the areas between the edges (bottom photo). This is done by assigning black and white values to the appropriate spots.

Since the image content is now made up of only black and white elements, with no gray shades, it constitutes a binary representation. This spells a considerable reduction of the amount of data that must be processed in any subsequent object indentification. **-John Gosch**

France

Method ups laser diodes' performance

This month, researchers at Thomson-CSF's Central Research Laboratory at Corbeville, southwest of Paris, reported in scientific journals on both sides of the Atlantic a pair of noteworthy results in its effort to push the performance of solid-state optoelectronic lasers: a gallium aluminum arsenide laser with an exceptionally narrow output beam and a room-temperature gallium indium arsenide phosphide laser diode on an indium phosphide substrate.

Sandwiched in. Both lasers have a double heterostructure, meaning that the active layer is sandwiched between layers of a different semiconductor material, grown by low-pressure metal-organic chemical vapor deposition (MO-CVD). This technology has high promise for stripe-geometry lasers because the thickness of the active layer and the doped layers that sandwich it can be closely controlled even over a large substrate area.

Jean Pascal Duchemin, who heads the laser materials research team at Corbeville, is quick to point out that his group is not the first to fabricate a double-heterostructure laser using MO-CVD. A team from Rockwell International Corp. reported that some two years ago. However, Duchemin adds that his group works with a horizontal reactor that can handle several 2-inch wafers at a time instead of an experimental vertical reactor.

For production. "Our method is suitable for mass production," he maintains. At the moment, Thomson has no timetable to shift to MO-CVD technology for the stripe lasers, fabricated by conventional liquid epitaxy, it actually has on the market, although it could happen within a couple of years.

The new GaAlAs laser is highly suitable for optical communications, Duchemin says. Its emission wavelength is 8,300 angstroms, a good match for optical fibers. The stripe, 300 micrometers long, is 5 μm wide and only 700 Å thick. As a result, the beam divergence (measured at the half-power points) is only 26° in the direction perpendicular to the plane of the active layer, so that most of the light output can be coupled into the fiber. What's more, the pulsed threshold current is low, typically 100 milliamperes. Some of the lasers have operated at continuous outputs of up to 10 milliwatts, but 5 mW is more typical.

Fabrication. To fabricate the laser, the team starts with an n^+ gallium arsenide substrate. Atop that, by MO-CVD epitaxy, goes n^+ silicon-doped GaAlAs 1.6 μm thick. Then comes the 700-Å active layer, essentially GaAs, since its composition is $Ga_{0.92}Al_{0.08}As$. It is topped by a zinc-doped p-type GaAlAs layer 1.7 μm thick on the p side.

After the contact layers are evaporated on, the stripes are delineated by shallow proton bombardment. Finally, the wafer is separated into individual chips, with sawed sides and cleaved faces 300 by 350 μm.

The researchers also have managed to fabricate double-heterostructure laser wafers using quaternary materials by the MO-CVD method. Their first devices emit at 1.15 μm, but as the fabrication method is optimized, Duchemin expects to see the wavelength move up to about 1.6 μm, another low-loss window for fiber-optic communications.

As far as Duchemin knows, his team is the first to achieve a gallium indium arsenide phosphide laser on an indium phosphide substrate that operates at room temperature. In this case, the substrate is tin-doped InP about 5 square centimeters in size. Then comes the first confining layer, n-type InP 2.2 μm thick. The active layer is 0.2 μm thick and undoped; it consists of $Ga_{0.20}In_{0.80}As_{0.43}P_{0.57}$. Last, there is a p-type InP layer 2.2 μm thick. Broad-area lasers

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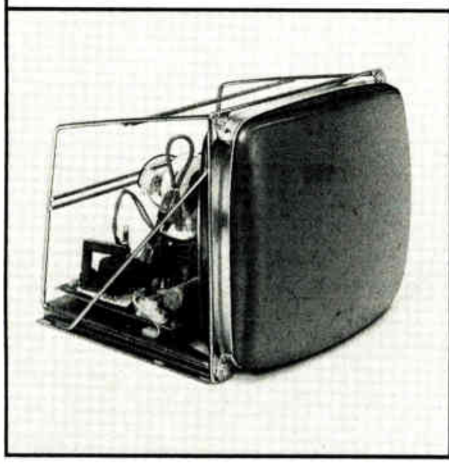	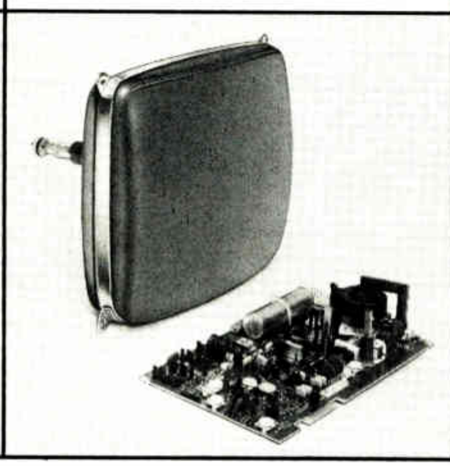	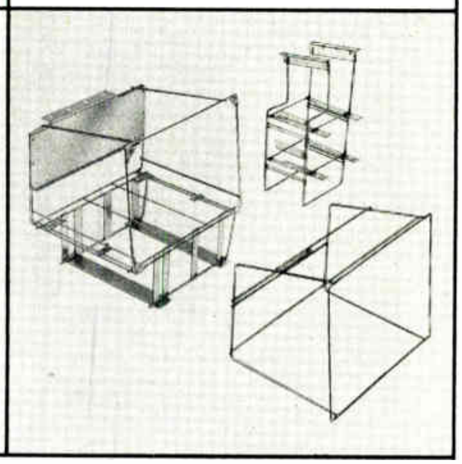

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-Arthur Erikson

The Netherlands

Philips to push small computers

NV Philips Gloeilampenfabrieken is out to establish itself more firmly in Europe's small-computer market. Drawing on the experience it has gained with more than 100,000 office-type installations—from banking terminals and accounting machines to small-business computers—the company's Data Systems division has come up with its P4500 interactive business computer system. It can be used in stand-alone applications, as well as in distributed data networks.

Having its debut at West Germany's April 16–24 Hanover Fair, the P4500 supplements and is compatible with Philips' P400 line of small-business computers. The Dutch company has sold about 2,000 units in this line, helping it to grab a sizable share of Europe's small-computer market. "With our new entry, we are determined to increase that share and thus strengthen our position," says Harry Barenbrug, product manager for small-business computers at the Data Systems division in Apeldoorn, Holland.

Team. One feature that Philips hopes will make the P4500 successful is the system's "team processor" architecture. This design allows each work station to function as an independent communications tool and gives computer power to everyone in the organization who needs it. That, plus what the company says is a powerful instruction set, provides the user with facilities such as true multiprogramming and the ability to handle up to 32 different application programs simultaneously.

Other sales arguments the firm is banking on are the system's economic applications software and its ergonomic design. The keyboard, for example, is claimed to be unique because of its low profile (see photo), which makes for convenient, fatigue-free operation. Also, the flicker-free screen of the cathode-ray-tube terminal can be tilted for different viewing angles and adjusted for lighting levels to suit ambient conditions. What's more, there is no glare or reflection from the screen.

Spread out. The P4500 spreads computing power around in an organization. Work stations can be located anywhere—at the shop floor as well as the boardroom—enabling the system to function as a source of information and as a data processor. Its ability to handle 32 application

A choice. With built-in data-communication facilities, Philips' P4500 multiprocessor computer can stand alone or serve as part of a network, like this travel agency work station.

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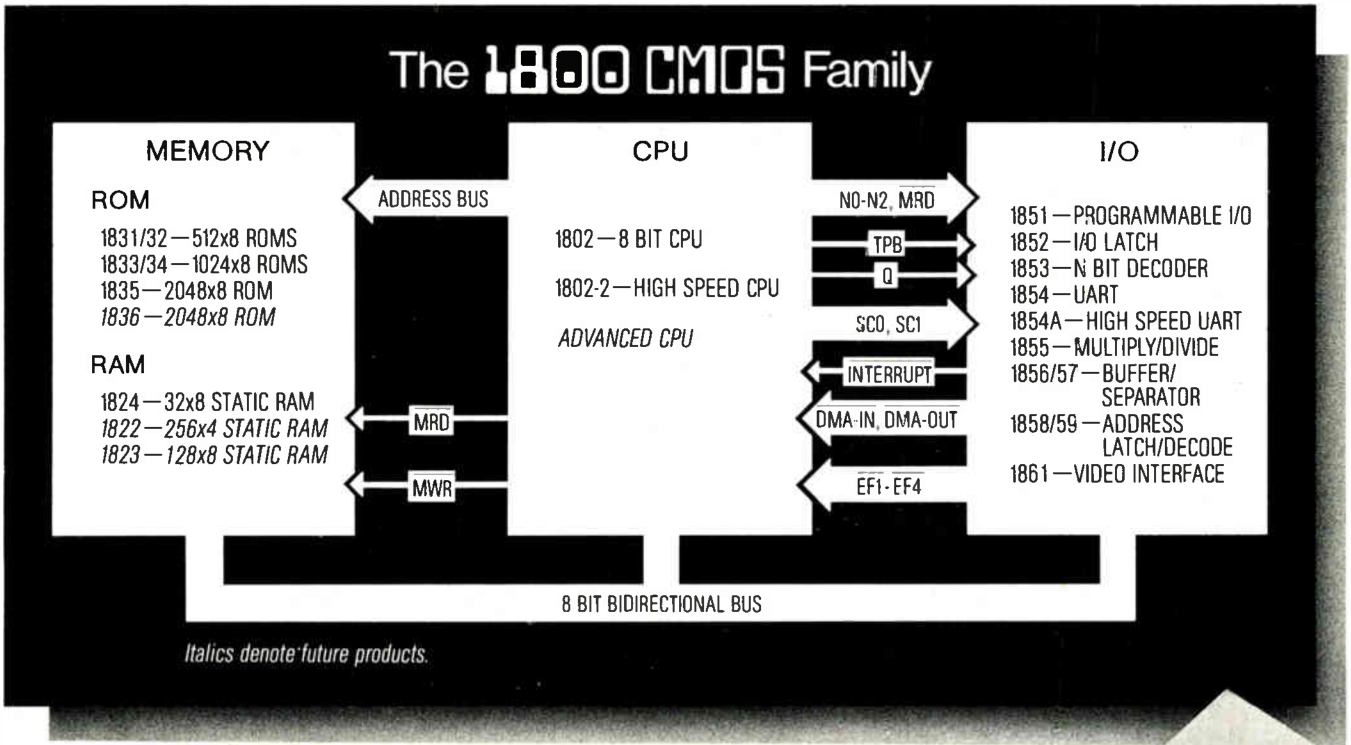

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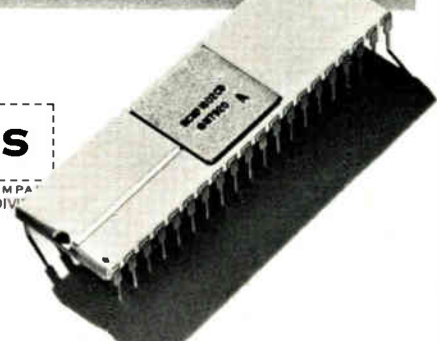

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programs simultaneously, Barenbrug says, allows it to keep virtually all files in the organization up to date.

A typical configuration has 256 kilobytes of main memory and 40 megabytes of disk storage—all in a single housing the size of a filing cabinet. The high-end configuration boasts 1 megabyte of main memory and 600 megabytes of disk storage; it can handle virtually any practical number of work stations. The basic cycle time for the main memory is 600 nanoseconds for 2 bytes, and the access time checks in at 550 ns.

The multiprocessor architecture delegates functions normally performed by a conventional central processing unit to intelligent, special-purpose processors, thereby relieving the CPU of large amounts of routine work. This concept, Philips says, allows even the smallest configuration to have a sophisticated combination of facilities—such as multiprogramming, transaction and batch operation, and data communications in different protocols simultaneously. In addition, it can diagnose its internal procedures, which will aid preventive maintenance.

Software. Furthermore, Philips offers application software packages to be customized by the user; they thus retain an individual character but do not have the high cost associated with individual, tailor-made programs. The main programming language is ANSI-standard Cobol, the well-proven language for business applications.

The P4500 will go to market during the first half of this year in five European countries: Austria, Belgium, the Netherlands, Switzerland, and West Germany. The rest of Western Europe will see it during the second part of 1980. Starting in 1981, the system will go on sale elsewhere around the world.

Prices run from $50,000 to $250,000. A basic system could be configured with a 256-kilobyte main memory, a 1-megabyte flexible disk drive, removable- and fixed-disk drives each with 20 megabytes, four CRT-terminal work stations that include a small hard-copy device, and a 300-line-per-minute printer. -J. G.

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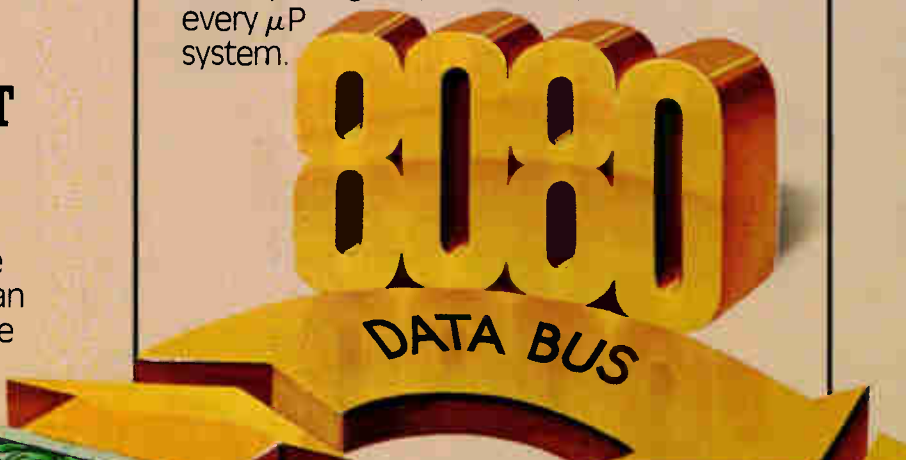

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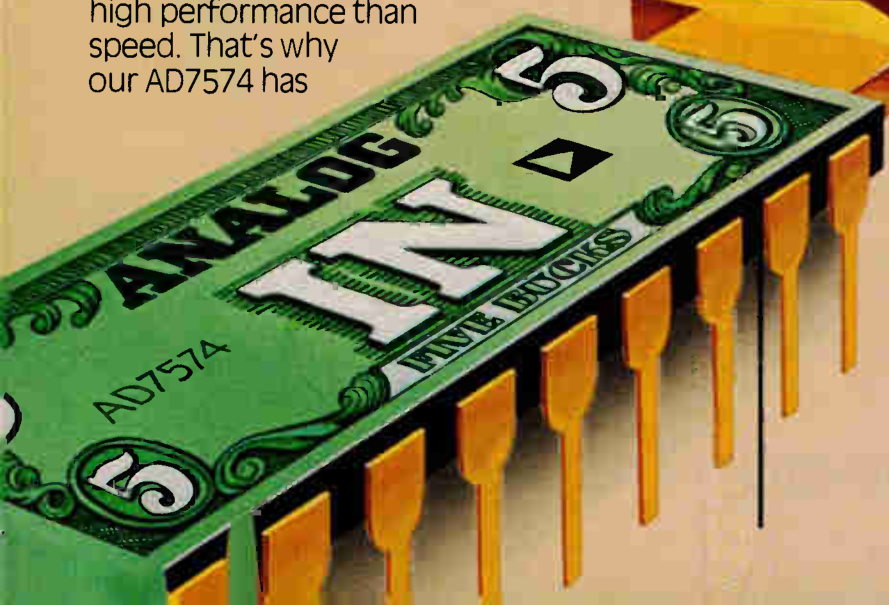

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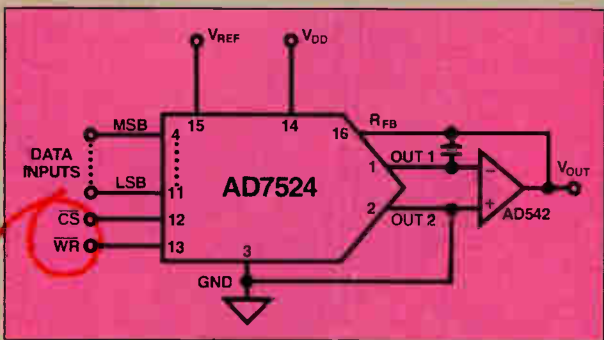

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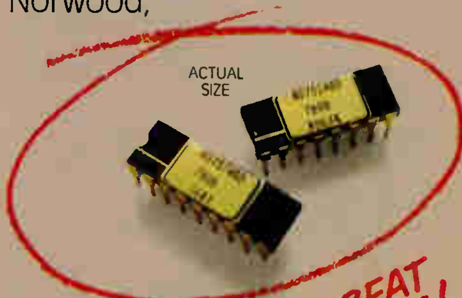

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R&D: some strategies that work

From TI's OST and IDEA to Motorola's road maps, companies find ways to encourage innovation

by James B. Brinton, Boston bureau manager

It can be hard to make a case for research and development funding in an economy in which inflation and the prime rate hover in the 20% range. Investments like Treasury bills offer a safer return on short-term investment than R&D—whereas for every 5 or 10 ideas, only one may prove a commercial winner. But U. S. business must "gamble" on R&D in the face of increasing competition from Europe and Japan and therefore must try to minimize risk through better management and the technique known as cooperative research.

Texas Instruments Inc., Dallas, offers a good example of the quandary in which many well-managed technologically based firms find themselves today. Over the past decade, TI's growth rate has been about 15% yearly; with inflation nearing 20%, 15% "growth" is contraction in real terms.

"The gap [on return] between very ordinary types of investment and R&D should be greater," says George H. Heilmeier, vice president for corporate research, development, and engineering. "The potential for innovative technological investment isn't as great as it should be; after all, you invest in R&D because you think the payoff's going to be greater [than with a safe investment]."

The man from OST. TI's Heilmeier wants R&D spending to be made more attractive

Heilmeier is not just talking about TI or the high-technology industries, but about the economy in general. R&D funding is becoming a problem of resource allocation, and consequently, research managers are looking for more cost-effective ways to spend scarce R&D dollars, with better management occupying a top spot as a key strategy.

TI's R&D funds do not seem scarce. According to Heilmeier, the firm invested about $155 million in R&D during 1979, and he expects the figure to rise, both as a percentage of sales and in dollar terms, in 1980.

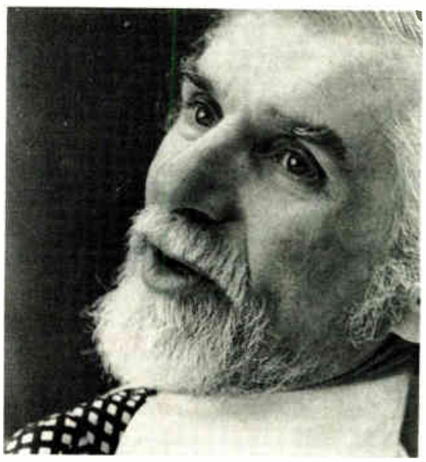
OST. Many of TI's R&D "gambles" will probably pay off; the company has the reputation of being one of the best-managed high-technology firms, and many of its competitors pattern their management structures after TI's OST—for objectives, strategies, and tactics—approach. OST allows the company to have separate strategic and operating budgets and a dual reporting system in which project-oriented management groups concentrate on future growth areas while a more conventional operating management addresses present profits.

OST is highly structured; managers are continually being measured relative to preset goals that are themselves under continuing review. Zero-based budgeting helps trim unhealthy programs from corporate plans before they become drains on scarce resources. Even so, TI's managers felt the need for something more.

"The key is to keep the ideas flowing," Heilmeier says. To create this environment, the company came up with the appropriately named IDEA—for identify, develop, expose, act—system. IDEA is designed to uncover innovation anywhere within the firm and thus the ideas and talented people that might form the cores of new ventures.

IDEA amplifies. The IDEA approach is not designed as a filter. "If only the good ideas are tolerated," says Heilmeier, "soon there won't be any ideas." Instead, the company considers IDEA an "amplifier" for management, exposing those in charge of OST to the sort of subtle and risky ideas from which important innovations may spring—raw material, as it were, for the OST system.

Under the system, an engineer approaches an IDEA representative



Pathfinder. Motorola technology vice president Cooper uses a "road map" system.

with a proposal that is outlined on a one-page form. The IDEA representative may approve the proposal on the spot, granting the proposer up to about $25,000 in company funds and up to six months of effort. This seed money is spent to prove to management that an idea can work, not to ensure that it will.

If the employee's proposal falls on deaf ears, it can be placed before any other IDEA representative within the firm; there are about 40 of them throughout TI, and as a group they dispense about $1 million yearly in such seed money. If an employee can get the approval of any one of them, he can go ahead, regardless of the number of times he has been turned down in the past.

From 30% to 50% of the IDEA proposals get funded, and some have led to the sort of product that in other circumstances might have been the germ of a new company. Among them were TI's $19.95 digital watch in 1977 [*Electronics*, Jan. 22, 1976, p. 44] and the speech synthesizer used in Speak & Spell [*Electronics*, Aug. 31, 1978, p. 109] and its teaching machine descendants.

Beyond the IDEA stage, OST takes over and there is more formality about the process of approving or denying an R&D proposal. But the system has proved its merit by allowing some wild ideas to surface in the usually stuffy environment of a large corporation.

Closet technique. That is a rare phenomenon, according to Guy L. Fougere, vice president of Arthur D. Little Inc., Cambridge, Mass., who says that the risk-reward climate in U. S. firms is so pervasive that in some, valuable research is carried out secretly, without management approval, until a product is capable of making a case for itself. Alternatively, he notes, lead times are falsified and goals made overly conservative to protect technical managers from the attacks of higher managers with accountant mentalities made narrower by the present weakness of the economy.

The importance of TI's cultivation of ideas in a low-risk environment is that it enables a large firm to move with some of the flexibility of a small company while still maintaining advantages of size, scale, and capitalization. There is good reason for large firms to want some of the characteristics of small ones: small companies, with their quick turnaround time from idea to product and their less formal innovation procedures, generate proportionately—and some times absolutely—far more innovation, growth, and jobs than larger ones (see Editorial, p. 24).

According to reports from the Massachusetts Institute of Technology, the American Electronics Association, the Canadian Federation of Independent Businesses, the Department of Commerce, and others, small firms innovate and provide jobs more efficiently than large companies. An Office of Management and Budget study is typical; it shows that between 1953 and 1973, firms with fewer than 1,000 employees accounted for almost half of the major innovations in the U. S. Further, the ratio of innovations to R&D employment was four times greater in such small firms than in larger ones. The total cost per R&D scientist or engineer is almost twice as great in larger firms as in those employing 1,000 or fewer. In spite of this record of efficient innovation, small business received only 3.5% of Federal R&D support in 1977, the year of the study.

Big growth. According to a 1978 AEA study, employment growth in newer, smaller firms was 115 times greater than that in companies more than 20 years old and 55 times greater than that in firms 5 to 10 years old.

Obviously, much of this apparent efficiency is due to the lack of constraint that TI's Heilmeier addressed. Thus, TI's IDEA system seems a good model for companies trying to deal with the problems of size while simultaneously retaining some of the growth potential of innovation-rich, small enterprises of the type scoring so well in studies.

Thomas A. Longo, vice president and chief technical officer of Fairchild Camera and Instrument Corp., Mountain View, Calif., would approve of OST. Electronics companies generally lack "long-term, noncyclical management objectives," he says and offers this background:

"Consider the cycles in electronics R&D over the last three decades. The traditional R&D powerhouses of the 1950s, like RCA, General Electric, and others, may have made the initial investments in semiconductor development, but none really made it big in the field." That was the role of others, "many of them startups who were not bound by traditional management systems. These new firms capitalized on the groundwork laid by traditional firms."

"Now," he continues, "the irony is catching up with these second- and third-generation companies. They must turn inward for the fundamental work now necessary, and they must realize that this carries with it the need for management to change its time constants." R&D goals must be set, and paths must be laid out to reach them. Managers find that they must take a long-term view despite the dynamism of their market—or perhaps because of it.

Applied, not basic. Longo feels that little basic research is done in the semiconductor industry; what research there is, he feels, is typically applied research or development. Whatever it is called, Fairchild is buying more of it: "About a year ago, we decided to significantly increase our R&D budget. Our acquisition by Schlumberger [*Electronics*, June 7, 1979, p. 42] reinforced this decision."

In an effort to bring technological research and product generation closer together, "Fairchild now puts three quarters of its R&D funding in the operating business entities and the rest in a central lab. That is a shift from our 1960s policy of spending two thirds of our R&D money in the central lab; obviously we shifted many technical people along with the money," Longo says.

At Motorola Inc., Schaumburg, Ill., there is a fairly new strategic planning system operating that, like OST, appears to be a form of management by objective. About five years ago, according to Martin Cooper, corporate vice president for technology, Motorola's board chairman, Robert W. Galvin, ordered his company's divisions to start plans to map the future of each major product line, not merely in market terms but in terms of the challenges and opportunities of emerging technologies as well.

After about three years as an experimental exercise, the system went fully on stream 18 to 24 months ago, with visible results: a bookcase full of "technology road maps." A typical road map might be an inch-thick looseleaf analysis of each product line with quantitative projections of the lines' future that are repeatedly updated.

Ten-year trip. The road map is the responsibility of a product line manager, who must project 10 years ahead, extrapolating the future of products not yet out of the lab. A typical set of charts might look like a set of compound, overlapping bell curves as products are introduced, penetrate the market, mature, and decline in sales, to be replaced by others. The road map also includes technology forecasts and suggested resource allocations.

One major purpose of the road map is to bring omissions to the attention of management. The maps are reviewed twice yearly for each product line at sessions attended by Motorola president William J. Weisz, board chairman Galvin, and other senior officials. R&D funding decisions are based on a road map's projections, including the product line manager's perceived needs to achieve expected sales.

A second effect is that during this evaluation, executives from a variety of levels within Motorola argue, cajole, compete, and generally communicate, generating constructive heat and energy. As with TI's OST, Motorola's road maps are an institutionalized attempt to open lines of contact and communication between the upper and lower strata of the company.

Each research project is justified by showing what sales or marketing goals would be missed if the R&D program were not funded at the time, rate, and magnitude suggested. By reviewing the product life cycles shown in the road maps, Motorola executives have a better feel of which research investments are the most profitable, according to Cooper. And to keep managers technologically abreast, there are technology road maps too; for example, Motorola's engineers keep a road map on photolithographic techniques, not because the firm plans to enter that field, but because photolithography paces semiconductor development, and advances there mean changes in product and market opportunities.

Thus, says Cooper, R&D funds are allocated on a product line basis, and are proportional to the income from that profit center. There are some areas where needs exceed the funding ability of a profit center. According to John F. Mitchell, Motorola's executive vice president and assistant chief operating officer, 20% to 30% of product line projects are funded beyond a line's ability to pay and thus get their money directly out of the corporate till. Examples of heavy funding include the firm's 16-bit 68000 microprocessor [*Electronics*, Aug. 16, 1979, p. 95] and cellular, land-mobile communications system.

Meetings and modules. Data General Corp., Westboro, Mass., organizes its strategic planning much like TI's OST program, "though it's not nearly so structured," according to Jeffrey C. Kalb, engineering vice president. "Management goals are written in both growth and profit terms," he says. That makes it hard to sacrifice growth for short-term profit, and it also allows a manager to lose money, as expected, during the cash-intensive, early days of a product's development. Beyond that,

The NSF's SBIR program

Washington's National Science Foundation (NSF) manages an effort to aid innovation in small business. It is known as the Small Business Innovation Research (SBIR) program, and its goal is to solicit high-risk, potentially high-payoff research proposals from small business.

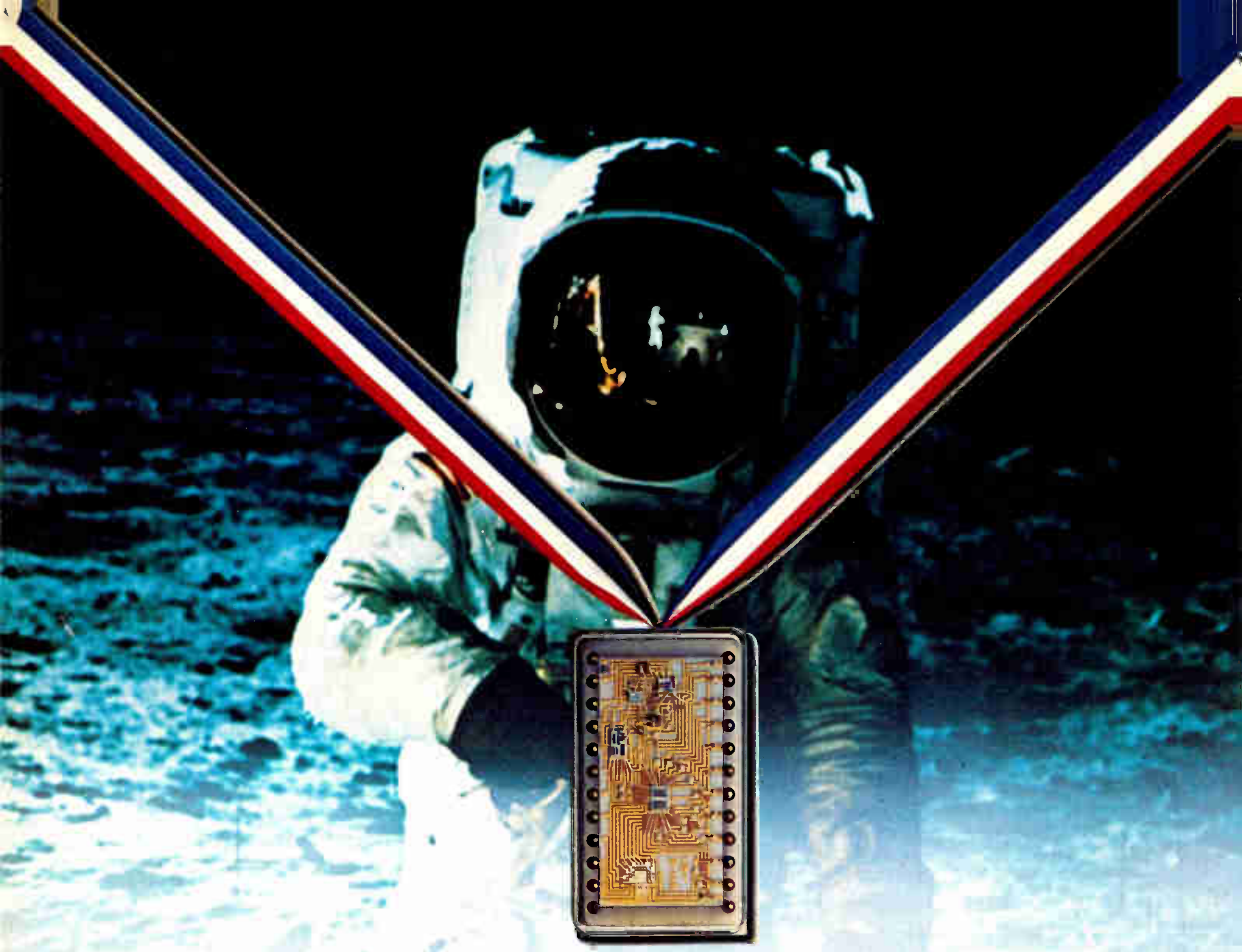
SBIR is a three-phase program that first surfaced in the mid-1970s as a program called Small Business Innovation Applied to National Needs, and Congress has been increasing its budget ever since, though perhaps not in constant dollar terms. In October 1979, the NSF made 54 awards under SBIR totaling about $1.3 million, all of them covering Phase 1 efforts in such areas as advanced instrumentation and technology to aid the physically handicapped. In response to its solicitation, the NSF received 408 proposals from companies ranging in size from 1 person to more than 350 employees.

The first two phases are funded by the NSF, and a third is targeted for venture capital funding by private industry. Phase 1 awards are limited to amounts of $25,000 or less and to a period of six months. According to the NSF, the size and duration of the first phase serves as a filter for the hundreds of proposals from small businesses while limiting the initial risk.

There is no preset limit on Phase 2 funding levels, although there are constraints. A typical Phase 2 effort will pay for two to three person-years of effort at the principal investigator level, but in addition to a second research proposal, there is a requirement for follow-up venture capital from a third party in an amount at least equal to the funding requested from the NSF. An average Phase 2 award is for about $200,000. This requirement acts as a "coupling" to the marketplace and tends to ensure that the work funded in Phase 2 is going to demonstrate some return on investment in the form of a new product, capability, or service. The NSF refers to this as "socioeconomic benefit from Government research." The committed venture capital funds a potentially open-ended Phase 3. According to an NSF source, "Federal funds are for research; private venture capital funds development toward commercial objectives."

The NSF claims that SBIR may be one of the fastest and most capital-efficient ways to bring new technology to the attention of business and the market. SBIR may also be arousing international attention. As early as the spring of 1979, the Swedish Industrial Corporation and the Israel-U. S. Binational Industrial Research and Development Foundation were discussing possible funding support or joint R&D efforts with SBIR participants in return for technology licenses.

-J. B. B.



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Inside the news

Data General has a product board of review, continuing staff meetings in the office of president Edson D. de Castro—one of the advantages of moderate size—and a general policy of encouraging ideas to "bloom early," as Kalb puts it.

As a result, over the past decade Data General has spent just about as much on research and development as it has made in net earnings. "We've been within a few hundred thousand dollars of our net every year for the past 10," says Kalb.

R&D line items are based on the programs they support—"that's 80% to 90% of the argument right there," Kalb says—and 10% to 20% on the discretion of management at various levels within the firm. This has worked out so that in 1978, for example, "equal thirds went to R&D on software, central processor development and refinement, and research on new peripherals." He adds that the proportion being spent on software is growing, as might be expected, but that Data General is trying to maximize the value of its software development costs through modularity, that is, by using the software more than once. This effort, in turn, has affected hardware development.

The idea has been to design programs in sections that can be linked as needed, coupled with the appropriate header, and thus run on different machines with different end results. The trick to this tactic is to identify common code out of which different programs can be assembled and, having found it, make repeated use of it.

Something borrowed. An example of this approach's effect on both hardware and software is the company's forthcoming 32-bit computer. Although it will be offered with a 32-bit instruction set having more than 350 operands, it will be able to use almost all of the 16-bit software that Data General already developed for its Eclipse and Nova series. The commonality is such that the machine can run programs in which 16- and 32-bit instructions intermingle.

Consequently, while many businesses need the higher power of 32-bit machines, Data General customers will be able to run appropriate 16-bit applications software—faster—on the new machine. This capability saves software development money not only for Data General but also for users faced with developing otherwise unnecessary 32-bit applications packages.

Personal styles are important to the R&D environment, too, and Kalb insists that he wants ideas to flow freely up from the lower ranks. "I don't want an engineering bureaucracy; I do want a lot of thoughtful engineers," he says. Thus he tips his hat to the spirit, if not the structure, of TI's system.

As modular software is becoming more common at computer firms as a means of getting more use out of a line of code, modular hardware design is growing in popularity because it allows designers to spread subsystem design and development costs over a larger number of products.

Modules do the job. At Hewlett-Packard Co., Palo Alto, Calif., Al Bagley, engineering manager for the Instrument Group, notes that "development of a product is a team effort, but trying to speed things up by adding members to a team can be tricky—like asking nine women to produce a baby in one month." Nevertheless, the development time of both digital and analog products has been speeded up.

"One way to shorten development time and extend product lifetimes as well," says Bagley, "is to use modular construction. There are a number of areas where, if you do a good job of this the first time around, you can extend product lifetimes 8 to 10 years [before a complete redesign is necessary]." Often, such redesign as is necessary can take place at the

The unpracticed art of strategic planning

Strategic planning is not the high art it should be, in the opinion of Derek E. Till, vice president of Arthur D. Little Inc., Cambridge, Mass. "Most management in this country focuses on the short term," he says. "Even though there's lots of lip service given to long-range planning, R&D policies and corporate risk-reward climates just don't reflect such planning." Often, he says, the man on the spot is a local executive or profit center manager; not only is he expected to make a profit, but to plan for research and development for the next generation of products as well. But, as Till puts it, "he has other, conflicting interests generated by his line management responsibilities." Thus the short-term view propagates downward in many firms.

"Even though companies are beginning to accept corporate strategic planning," he continues, "technical strategic planning is still poorly developed and perhaps needs some innovation of its own." Managers are now becoming willing to think about and use technical strategies, he says, but internal implementation problems are delaying their use.

"For example," Till notes, "product maturity curves often militate against new research. Over time, a firm spends a lot developing a new product, which can take off on a steeply rising curve of growth. This eventually flattens out into a plateau of steady sales, and though it seems foolish to expect such a plateau to last forever, some managements act as if it would. It becomes very hard within some firms to generate the backing for new R&D during a plateau phase—much less earlier, during a growth phase. But in high-technology industry, with shortening product lifetimes, it is often becoming more necessary to begin developing new capabilities even before others have reached market."

There are some ways around the problem, not all of them pleasant. "One industry can affect another and jar it out of its lethargy," says Till, pointing to the effect of microelectronics on the toy business. He would rather see managements trying to induce technology injection rather than reacting to it.

The other way Till sees to get a company off its plateau is to institute strong internal planning that can then enable the company itself to research and develop new technology or acquire it. That is even rarer than the unexpected injection of new technology, he notes. **-J. B. B.**

modular level, saving development dollars.

One excellent method of boosting the return on R&D investment is cooperative research—research conducted by an academic institution for industry, occasionally with Government funding or approval. There is a natural division of labor between theory and practice, basic research and targeted development.

Although in theory it should be possible to pursue research goals more efficiently using the people and resources of two organizations rather than one, in practice it has not been easy at all. Potential partner organizations often find themselves coming to grief over matters such as academic freedom, the right to publish, and proprietary information. In addition, corporate R&D managers must justify to themselves and their superiors the expenditure of R&D funds outside their companies. Human nature is such that matters of suspicion and accountability and the diversion of funds from pet internal projects or those with visible short-term payoffs become overwhelmingly important to some firms. Still, according to Government figures, more and more cooperative research is being done yearly, and the trend has been rising since at least the mid-1970s despite the estrangement of business and academe that followed World War II.

There were three reasons for the divergence of interests: industry began to feel that the interests of universities were separate from their own, graduate students lost interest in industrial research, and industry lost interest in basic research. Underpinning all three trends was the role of Government as a research sugar daddy during World War II, the Korean War, and the post-Sputnik era.

Now. That is the view of Denis J. Prager, senior policy analyst in the White House Office of Science and Technology Policy (OSTP). But now that economic pressures are cutting real-dollar Federal funds for R&D, the old partnership is being renewed, he says. Industry is looking more attractive as a source of funds for university work, as an employer of graduates, and even as a source of part-time faculty—and all without Government red tape. Government accountability regulations, human- and animal-experimentation rules, biohazard regulations, and affirmative-action programs have often impaired the independence of the academic scientist receiving Federal funds for his or her work.

Industry has its share of incentives, too. Research sponsored at a university offers the opportunity to gain knowledge at relatively low cost, since the sponsoring company carries essentially no regulatory burden on research—no corporate fringe benefits and usually little in the way of capital costs. Thus the universities give industry the opportunity to draw upon talented researchers without having to expand in-house facilities or hire new staff—and the isolation of "risky" basic research in a relatively low-overhead campus environment has attractions for the business mentality.

For smaller companies, there are levels of cooperation suited to their size. Various universities and firms combine in industrial associate programs, one goal of which is the quick transfer of research results from university to industry. In exchange for industry funds, the universities offer an inside track on new developments, regular interaction with faculty, and the opportunity to find areas of common interest that might result in cooperative research programs.

From the industry end, Bell Laboratories maintains a large number of individual-to-individual scientific and technical liaisons with faculty around the country. These are typically peer relationships, according to Prager and Gilbert S. Omenn, the OSTP's associate director for human resources, generally oriented toward basic rather than applied research and away from proprietary efforts. They have their foundation in the reputations of many Bell Laboratories scientists, which allows them to interact as equals with academics, something few other firms can boast.

Research consortiums offer the chance for several firms to take advantage of a school's particular talents. Though funded at only about $500,000 a year, the Polymer Processing Program at Massachusetts Institute of Technology is one of the best known, involving up to a dozen member firms and about 25 projects in advanced chemistry, with most of the monies supporting graduate student efforts. There are similar consortiums at universities such as Cornell, North Carolina State, the University of Delaware, and Carnegie-

Control Data, Minnesota University unite

An ambitious plan to bring together industry and academic research capabilities recently culminated in the formation of a Center for Microelectronics and Information Services at the University of Minnesota in Minneapolis. So far, the only two formally declared participants in the project are the university's Institute of Technology, which incorporates many scientific and engineering departments, and Minneapolis-based Control Data Corp., whose $2 million grant last December to operate the center represents the first industry funding. But, says William Franta, computer sciences professor and acting codirector of the center, the aim is to draw in more U. S. and international companies and at least three more universities for "cooperation on a grand scale" in research involving scientists on the campus and in the plant in such areas as large-scale and very large-scale integrated architecture and software sciences.

Franta points to the benefits of shared resources, multidisciplinary approaches to problems, and exposure of students to the interests and methods of industry as part of their training in explaining hopes for the widest possible participation of private and academic interests. Technical programs to be pursued by research teams based at the center are still in the planning stages but could be getting under way by summer 1980, he says. Organizational details still being pounded out include the thorny issue of patent and copyright sharing and the ongoing efforts to bring in additional sources as well as attempts to attract membership by institutions other than Minnesota.

-Linda Lowe

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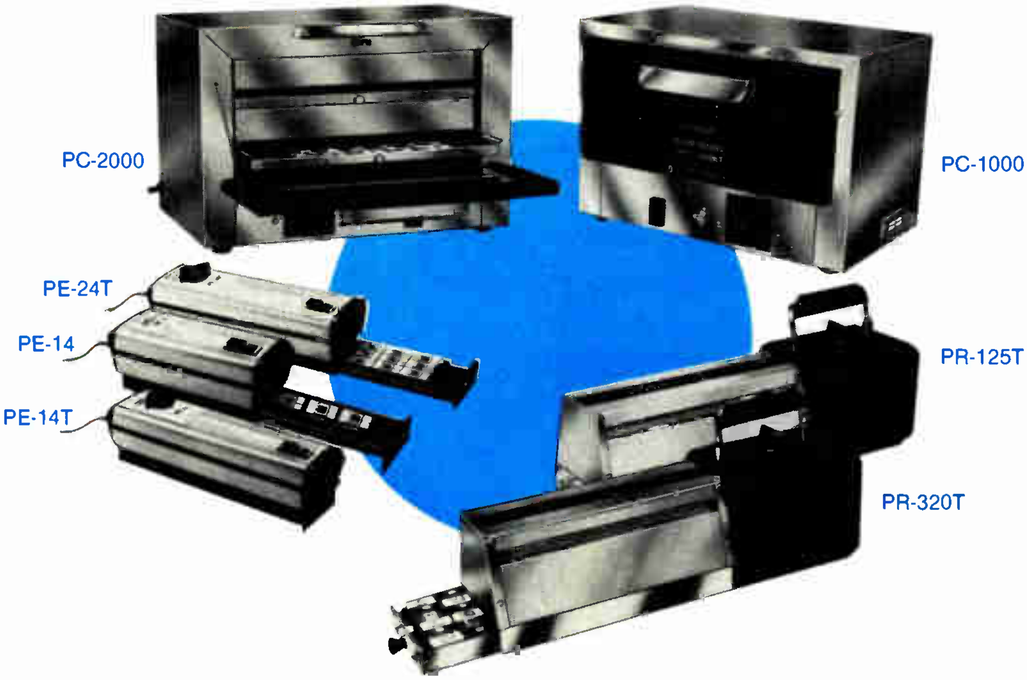

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Mellon University in Pittsburgh.

Less well known, but larger, are the consortiums sponsored by MIT's Energy Laboratory that offer a variety of programs to companies in that field. Malcolm A. Weiss, the laboratory's deputy director, is currently very enthusiastic about an effort called Aspen—for advanced system for process engineering.

A 150,000-line computer program for simulating fuel conversion and process engineering, Aspen was developed at the Energy Laboratory under a $3 million Department of Energy award. "Now we are beginning to transfer this knowledge to industry," says Weiss.

Service. "For $15,000 to $20,000, we will teach a firm's personnel how to get the most from Aspen, we'll run some of their problems through our system, and we'll get Aspen up and working on their own computers," according to Weiss.

The firms now participating in Aspen are paying for the privilege by being guinea pigs and love it. "We know there are bugs in Aspen," says Weiss. "It's the purpose of the present program to get them out." But the program's payoff potential is so great that companies are lining up to participate in the debugging process, even though it will be published in full, perhaps as early as late 1981.

That is not surprising, since Aspen is probably the most sophisticated process-modeling system ever developed, according to Weiss. It holds the promise of designing more efficient process systems with almost across-the-board cost reductions and reduced pollution to boot. Currently, there are 40 to 50 companies getting to know the program at the Energy Laboratory. The DOE had synthetic fuels in mind when it funded development, but industry is applying it far more broadly with an eye firmly fixed on cost savings.

The Energy Laboratory's Electric Utility Workshop costs only about $3,500 to join and gives participants access to general seminars and targeted workshops in which utility firms can discuss their needs and MIT faculty can describe current capabilities and research in which the utility companies might be interested. As a result of this exchange of information, says Weiss, "interested industry and faculty parties often agree to cooperative projects, usually short-term ones of about a year."

Some 10 to 15 such projects come out of the workshop yearly, generating $500,000 to $700,000 for MIT and knowledge for industry. Some projects with wide application are funded by multiple sponsors on an ability-to-pay basis; MIT retains patent rights.

The laboratory's Center for Energy Policy Research (CEPR) involves about 30 organizations at present, with more apparently on the way. They contribute to an unrestricted fund out of which MIT pays for research in any field related to energy policy. Members are assessed according to their means, with some members like the League of Women Voters, the Environmental Defense Fund, and the National Urban League paying far less than, for example, the Hughes Tool Co. or Exxon Corp. "The list of associates shows that what we are after is intelligent participation in the CEPR," notes Weiss, "feedback on our data and research results, and so on."

In addition to sponsoring research, the CEPR holds government-industry symposiums on policy issues, new concepts in utility management and control, and world petroleum supply and demand and the resulting effect on electricity pricing. One of the more interesting technical research efforts dealt with homeostatic electric control, where power to the consumer can be controlled by the utility as well as by demand alone.

According to Weiss, the CEPR is a booming success, with a waiting list of participants. And when the word gets out, the same may be said of industry-academic cooperative research in general. □

This is the last article in a three-part series. The others appeared on Jan. 17 and March 13.

People talking to people

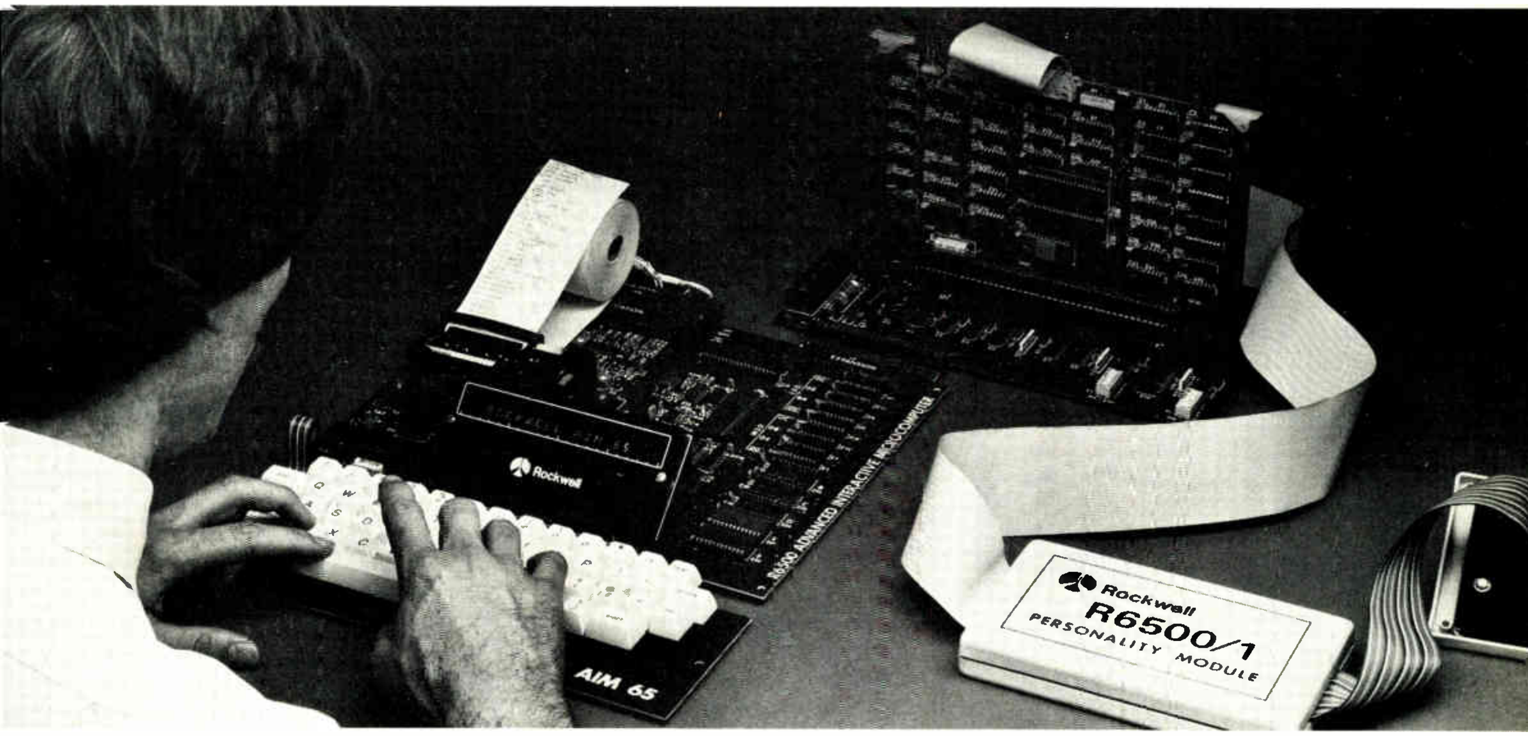
Cooperative research efforts linking campus and industry can give more mileage for their R&D investments, and not just for the obvious reason that shared talent and resources stretch further. The other reason is that the diverse people and disciplines they bring together often create more fertile ground for innovation. An example of such an alliance is that funded by GTE Laboratories Inc., Waltham, Mass., to study light-controlled factors in the interface between semiconductors and solvent electrolytes.

The job teams an automatic test equipment engineer specializing in such interfaces, a solid-state physics expert at the Massachusetts Institute of Technology, and a chemist at the Worcester Polytechnic Institute, Worcester, Mass. Each has full control of his own line of inquiry, but the three meet at least monthly to compare notes and discuss possible new directions their research should take.

Begun in September 1979 as a prototype of future programs—some of which now are in the planning stage—the arrangement stresses collegial, peer relationships, according to William F. Nelson, director of GTE's advanced technology laboratory. "We are careful to avoid the role of sponsor calling the tune, which I think is the usual pattern when a company funds academic research," he says. "Leaving the faculty members free to develop their own areas of interest is one way of attracting people who otherwise would not be interested in industry-related research." Their work, he feels, as well as GTE's, is enhanced even as it helps generate well-documented findings that GTE can use relative to larger research questions.

The immediate goal of the program, Nelson says, is to foster basic scientific understanding and information exchange. The longer-term criteria of success will be "if we can look back and see that an effort led to commercial applications." GTE's formal contracts with MIT and Worcester Poly include provisions for sharing rights under any patents generated by the team's research; GTE also would have a royalty-free, nonexclusive license to use any patented results of the effort. The project will run for three years, Nelson says, "giving the researchers the assured continuity they need to plan their work." **-L. L.**

Rockwell announces in-circuit emulation at evaluation board prices.



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Micro Power

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Slimmer PL/1 seeks popularity

Subset G eliminates problems that had made language unsuitable for smaller machines and manufacturers are starting to offer it

by Martin Marshall, West Coast Computers & Software Editor

Pushed by IBM Corp. for more than a decade as the language to end all languages, PL/1 has soured many a programmer once it was fully implemented. "It's a huge monstrosity," maintains Bruce Ravenal, president of Language Resources Inc. of Sunnyvale, Calif., and the software designer of the 16-bit 8086 microprocessor [*Electronics*, April 10, p. 14]. "It's too complex, has too many options, and it's loaded with pitfalls." Adds Dave Clouttier, software marketing manager for Intel Corp.'s single-board computer division in Hillsboro, Ore., "I don't think it was a success even inside IBM—the debugging of programs was just too difficult." But now, some timely modifications have made PL/1 a hot item among minicomputer makers and even opened the door to microcomputer applications (see p. 41).

Some 10% of the programming written for large mainframes is in PL/1, including programs for Control Data, Burroughs, and Honeywell mainframes, as well as those of IBM. The advocates of the language point to its data typing, string handling, and powerful primitive instructions as the reasons for its use. These merits have prompted a number of representatives of computer manufacturers and users to try to improve the language by cutting it down to a more usable subset—and in the process to allow it to run on minicomputers as well as on large mainframes.

The group, which became committee X3J1-PL/1 of the American National Standards Institute, has now completed its work, and its product—titled Subset G, for general-purpose subset—should be published as an ANSI standard by midyear. As a result of this work, a rash of Subset G offerings by the major minicomputer manufacturers either has been or shortly will be introduced.

"It was only about 10% to 20% of PL/1 that was causing problems," observes committee chairman Phillip Koch of Dartmouth College. "We believe we have identified and removed these parts and thereby eliminated 90% of the difficulties." (See "Making PL/1 more usable," below.)

The net result of these reductions is that Subset G now allows minicomputer manufacturers to create compilers that are upwardly compatible with the full PL/1 language run on mainframes, while reducing by an order of magnitude both the memory space required and the possible sources of programming errors. "With its drawbacks greatly reduced, PL/1 becomes a better business language than Cobol," Koch says. "Subset G, for example, supports strings of varying lengths, which Cobol does not. Pascal in its standard form doesn't support strings at all."

Most minicomputer manufacturers were represented on the committee, and as a result several have already brought a Subset G option to market. Data General Corp. of Westboro, Mass., was the first, with a 32-kiloword (16 bits per word) Subset G compiler for its Eclipse series. Applied Information Systems Inc., of Chapel Hill, N.C., has developed a Subset G package for the PDP 11 series that can run under the RSX-11M, -11D, IAS, RSTS/E, or VAX/VMS operating systems. Next month, it will announce a 28-kiloword version that can run under an RT-11 operating system, thereby opening up applications for the LSI-11 microcomputers. The run-time library for this introduction is now

Making PL/1 more usable

Portions of the full PL/1 that were thrown out by the Subset G committee:

- Half of the scalar data types, mostly forms of complex data and little-used forms of picture data.
- Array-valued expressions, which are useful in scientific applications, but which require excessive overhead. Structure-valued expressions and mixed-aggregate-type expressions were also eliminated.
- Default, entry, and locate statements.
- User-defined names except those identified by a declare statement or label prefix.
- Many implicit conversions of data types.
- Several explicitly designated conditions and all condition prefixes.
- Controlled storage classes and reference options.

Formats were restricted to constant values and data-directed stream input/output to reduce code and simplify the compilers. Also, the "do" statement was greatly simplified and the "defined" attribute was restricted to simple and string overlay defining.

working, and the compiler (expected to be priced under $4,000) will be available in the early third quarter. Digital Equipment Corp. of Maynard, Mass., is also believed to be readying its own Subset G package, but feels that it is too early to comment upon developments.

At Prime Computer Inc. in Wellesley, Mass., Subset G has already been bundled into a $5,000 compiler-plus-library package. "There are a few extensions and restrictions, but our version is almost exactly Subset G," notes Jim Pules, manager of language products. The extensions include a percentage replacement statement; built-in functions for rank, byte, and trim; and an extension for read/write string files into line-oriented input/output.

They also include the use of an A format without a field width to read a variable-length input line and the use of both upper- and lowercase letters in names. The Prime implementation allows use of the options (short) specifier to control space allocations for pointer variables.

Because the Prime implementation was developed before the committee's work was made final, there also are a few features of Subset G that Prime's version does not support. For example, it does not support character indices for key files, a feature that will become available next month. It also does not allow the assignment "array equals scalar," or the conditions FIXEDOVERFLOW, OVERFLOW, UNDERFLOW, ZERODIVIDE, and UNDEFINABLE. "Read with set" is not allowed, nor is the string option allowed in a GET or PUT.

Wang Laboratories Inc., of Tewksbury, Mass., is expected to follow suit shortly. This summer, the company expects to announce a Subset G package for its VS and VS-100 computers. The package, which has not yet been priced, contains a compiler, a symbolic debugger, a runtime library, and an editor. The reason for going to Subset G, according to Phillip Florence, manager of new product development, is that "it offers a major, block-structured language with fully defined I/O. It can also accommodate the power of both Cobol and Fortran."

IBM, which started it all with PL/1, has also closely monitored the developments of Subset G through its committee member, Alexander J. Arthur of the Santa Teresa, Calif., division. The company did not, however, opt to go with a strictly Subset G package for its Series 1 computers. Instead, IBM will release EDX PL/1 at the end of this month. Termed an "event-driven executive," EDX PL/1 consists of two parts—the compiler and resident library ($6,180) and the transient library ($1,140). Both parts are required to compile and execute a program, but only the transient library is required for the execution of programs listed above.

More choices. The EDX PL/1 is generally less restrictive than Subset G and therefore offers the programmer more choices and more complexity. It does, for example, allow the full range of implicit conversions, whereas the subset restricts some. Other additions that EDX PL/1 has made beyond the subset include sensor I/O for both analog and digital material, and a full multitasking language. Also, the subset does not allow a position attribute, but EDX PL/1 does. The primary portions of Subset G that are not included in the Series 1 release are the support of asterisk-length strings, and some of the open-statement options. EDX PL/1 will support only the input, output, and update functions of the open-statement options.

The most prominent name missing from the list of minicomputer manufacturers implementing PL/1's Subset G is Hewelett-Packard Co. of Palo Alto, Calif. HP did not have a representative sitting on the Subset G panel, and it currently has no plans to implement a Subset G option. "PL/1 simply dropped off the bottom of our list of priorities," says HP 3000 marketing manager Robert Bond. "Our users have indicated they are interested in Cobol, Basic, Fortran, and Pascal, rather than getting involved in PL/1. We do, however, read reports of the Subset G activity, and every year and a half we ask the priority question anew." HP, for its part, has placed a heavy software development effort into Pascal. □

Communications

AT&T ruling faces challenges

Deregulation of all terminal equipment is welcomed by some, but CCIA plans court action over feared cross-subsidies

by Ray Connolly, Washington bureau manager

The decision in early April by the Federal Communications Commission that, in effect, permits American Telephone & Telegraph Co. and General Telephone & Electronics Corp. to compete freely after March 1982 is being hailed as a landmark action. "It removes the barricades from the door to the information age," says the FCC's chairman, Charles D. Ferris.

The decision limits the FCC's regulatory powers to only basic telephone service after March 1982 and then deregulates all terminal equipment—from telephones to computers. But Ferris, in his declaration that "the supply of communications products and services will be limited only by the ingenuity of businessmen and scientists," clearly overlooks the role still to be played by judges and lawyers as opponents of the FCC's "final decision" in the Second Computer Inquiry under Docket 20828 stand ready to file court appeals.

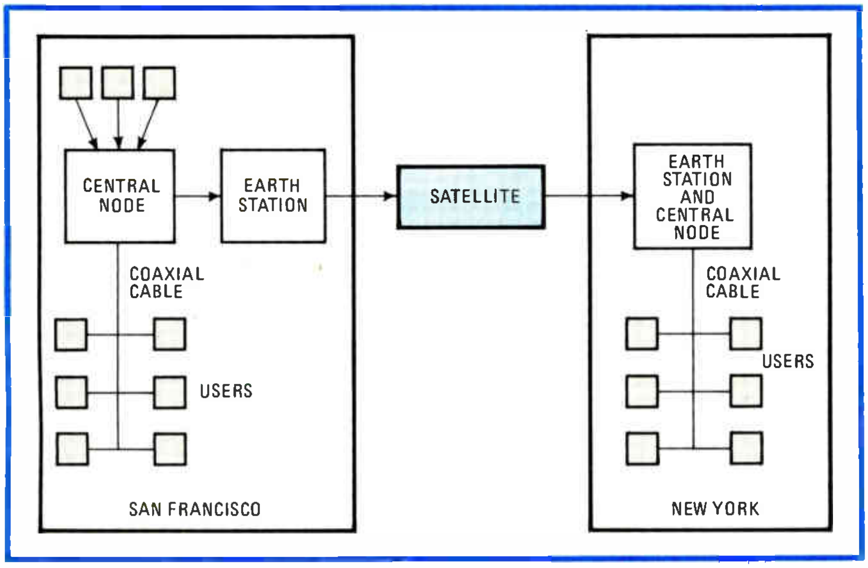
As commissioner Robert E. Lee put it to Common Carrier Bureau chief Phillip L. Verveer during the hearing on the vote, "Who's going to sue us? 'Everybody?' " Verveer's reply: "That's a fair assumption." What potential litigants—including the Department of Justice—await is a final order now being drafted by Verveer's staff. One of them says the draft order now runs to more than 130 pages and should be approved by the commissioners by the end of April for release.

Justice Department officials are remaining silent until they study the final order, but they are clearly concerned about the FCC's interpretation of the 1956 antitrust consent decree barring AT&T from participation in unregulated markets. "The FCC's rationale," says one Justice official informally, "seems to be that it retains regulatory jurisdiction over AT&T but will forbear from regulating in markets for enhanced equipment and services like information and data processing in favor of the competitive marketplace. The Attorney General may not buy that."

Even faster court action can be expected from the Computer and Communications Industry Association, says president A. G. W. "Jack" Biddle. The CCIA will go straight to the U. S. District Court of Appeals for the District of Columbia, instead of petitioning for reconsideration by the FCC. Biddle says the CCIA is pleased with the FCC call for arm's-length subsidiaries for the sale of enhanced services by AT&T and GTE but is distressed that manufacturing subsidiaries for customer premises equipment, or CPE, will not prevent "cross-subsidies in both hardware and software systems" by the telecommunications industry giants.

Other equipment makers and trade groups have reservations similar to the CCIA's, but say they want to wait for the FCC's final order. But the fact that AT&T and GTE each could create what another association official calls "a department store subsidiary to market all kinds of equipment" troubles companies that suspect that this development could also make it extremely difficult to track cross-subsidization.

Even AT&T. Moreover, AT&T itself is not altogether happy with the FCC ruling. Though the company likes the interpretation of the 1956 consent decree and "looks forward to competing in a deregulated terminal market and in data-communications products and services," vice chair-



Another request. The FCC has been asked to approve this system to distribute digital data within cities via satellites. As with AT&T decision, approval could result in lengthy litigation.

man James E. Olson says the two-year transition period for unbundling products and services "is all too brief." AT&T is also "troubled by the degree of separation between the Bell operating companies on the one hand and Bell Laboratories and Western Electric on the other." Other officials like FCC commissioner Joseph R. Fogarty—one of two dissenters in the action, along with Ann R. Jones—argues that unbundling telephone terminals from the capital investment rate base on which telephone charges are set could raise basic telephone service rates for many users who can least afford it.

Yet another concern in Congress and industry is the FCC action's impact on the fate of H. R. 6121, the faltering bill to deregulate the telecommunications industry and restructure the FCC that is sponsored by Rep. Lionel Van Deerlin (D., Calif.). Many congressional observers suspect that the FCC ruling may have finally killed the bill's declining prospects for passage in this session [*Electronics*, Jan 31, p. 50], and even Van Deerlin concedes that "the FCC has hit a home run with its new policy." But he still sees the need for legislation, as do AT&T and the Commerce Department's National Telecommunications and Information Administration, policy agency for the White House.

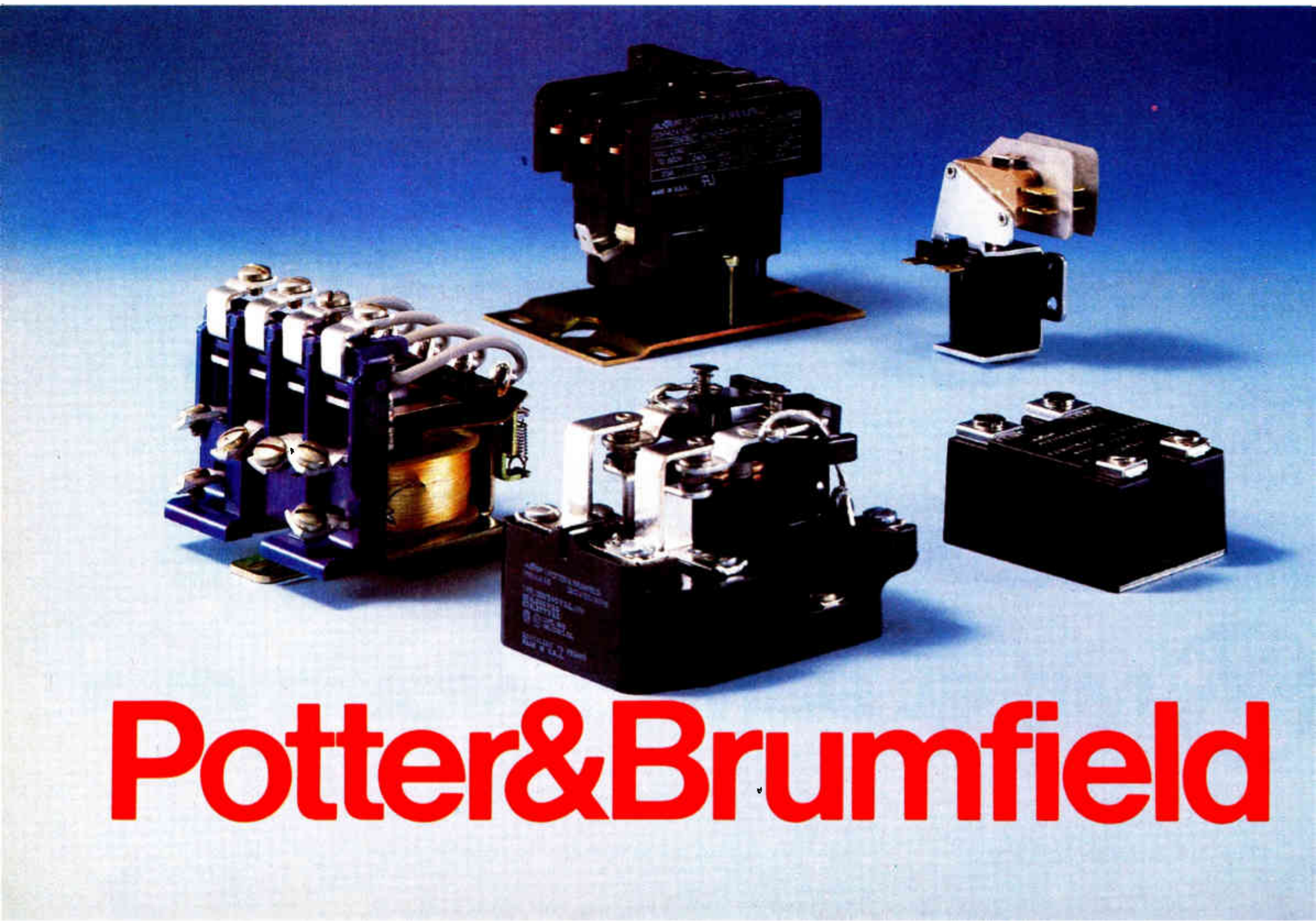
Three issues. Van Deerlin sees three unresolved issues in the wake of the FCC ruling. "First, local phone rates will rise sharply unless the FCC quickly replaces the telephone industry's crumbling separations and settlements process with a new, equitable access charge," he points out.

"Second, the fate of the 1956 consent decree remains clouded. Finally, the commission continues to hold the possibility of regulation like a club over a rapidly changing industry. The FCC's authority to preempt local jurisdiction is challengeable.

Even the 5-to-2 split among the FCC commissioners on the vote, plus the fact that six issued separate statements explaining their action, reflects some uncertainty within the commission itself.

Distinguishing between its latest "final decision" and last year's "tentative decision" to open the marketplace [*Electronics*, June 7, 1979, p. 92], FCC chairman Ferris explains that reaction to last year's judgment "convinced us that this distinction [between regulated basic service and deregulated enhanced services] was no more useful than the computer–data procesing dichotomy of the First Computer Inquiry" that ended in 1975. "The realities of the marketplace and the likely evolution of the technology simply do not support such a distinction. Therefore, we have decided to deregulate all customer equipment, including the simple rotary dial telephone found in most homes."

While details of the Docket 20828 decision are still being spelled out, the packed FCC hearing room on decision day heard the Common Carrier Bureau identify the nine areas of action, three dealing with



customer premises equipment and the rest with services.

In addition to ordering carriers to separate or unbundle CPE costs by March 1982 to allow their deregulation and optional sale by arm's-length subsidiaries of AT&T and GTE and anyone else in the market, the FCC will convene a Federal-state joint board to cope with the issue of payments for services after deregulated CPE is removed from the rate base. Not only does the FCC expect that "a customer's total bill for equipment and service will not increase," says chairman Ferris, but furthermore, "over time we anticipate that consumers in general will pay less and will have a much broader array of products from which to choose" because of competition.

Whereas common carrier services defined as "basic" (the transmission for movement of information) will continue to be regulated, services that are "enhanced" (that is, when information is restructured by computers or other equipment) will not be. Those services may be offered by anyone, with only the dominant carriers, AT&T and GTE, required to do so through separate subsidiaries.

Though all sellers will pay the same tariff, industry officials suspect that AT&T and GTE could favor allocating capacity to their subsidiaries at the expense of competitors. "That is one likely issue for litigation," says one communications lawyer, "unless distinct safeguards are spelled out."

Another request. As potential litigators prepared to challenge the commission's "final decision" in the computer inquiry, the FCC was faced with another potentially troublesome competitive issue: a request by Satellite Business Systems Inc. and Tymnet Inc. to demonstrate jointly the "innovative" intracity distribution of digital data from satellites, eliminating the need to connect with local carriers and employing data rates of up to 56 kilobits per second.

Also involved would be a new partnership called LDC to be formed jointly by M/A-COM Inc., owned by MCI Telecommunications Corp., Washington, D. C., and Aetna Life & Casualty, as owner of SBS along with Comsat General Corp. and International Business Machines Corp.

SBS, which is set to launch its first satellite for intercity business communications on Oct. 23, with an eye to beginning commercial operations in 1981, says it wants FCC approval for demonstration ground stations in New York's Wall Street area and in San Francisco. The LDC partnership would install and use coaxial cable in both cities for the SBS ground stations, and Tymnet would also install and operate in San Francisco an additional cellular radio distribution system to office building antennas. The technique to end-run local carriers could eliminate, says SBS, "local transmission bottlenecks posed by traditional local loop facilities in metropolitan areas."

The new proposal—which would supplement SBS plans to offer its own customer rooftop ground stations—is sure to attract strong opposition from local AT&T affiliates and independent telephone companies. □

Letter from Southern California

That boom you hear is L. A. County

Electronics firms are flocking to area west of city, where major attraction is the professionals already living there

by Larry Waller, Los Angeles bureau manager

Just a few years ago, as the 1974–75 recession waned, prospects for hard-hit electronics firms in Southern California looked dull. Except for booming Orange County, where fast-moving minicomputer makers pulled everything along in their wake, the outlook was for stagnation at best. Big aerospace firms, long the dominant employers, lay dormant, and more publicized semiconductor firms 350 miles north in Silicon Valley were primed as action centers.

But a funny thing happened in the interim. Instead of quietly taking a back seat, the region from Santa Barbara south to the Mexican border is off on a healthy growth curve. Although reliable figures for electronics activity alone in the region are apparently nonexistent, industry employment shows an expansion rate that can hold its own with that of any other area. Jobs grew nearly 26% for the period.

Coming up with sweeping conclusions based on little data can be misleading, however, especially in such a transient, fast-changing place. However, the following points stand out:

- Massive Los Angeles County not only has shown a steady upswing since the recession, despite dire predictions of a mass exodus from high taxes and costs, but it boasts what is likely the fastest-growing area of all.
- Orange County, the star of the 1970s, is peaking out, a victim of too rapid growth. That has slowed to a rate of about 7% last year.
- San Diego is the scene of the best-planned, most ambitious effort to attract industry in the state and has an impressive track record.
- Reasons for the surge—and what some say put a floor under any possible decline—relate to the age-old attractions of California. People simply like living in a pleasant place, one with so many amenities.

Quiet noise. By itself, the last point probably ranks as the big factor behind what is occurring along the Ventura Freeway west of Los Angeles. "A quiet explosion," says veteran industry-watcher Charles Elkind, longtime Southern division manager for the American Electronics Association.

There, entrepreneurs have planted new companies in Agoura, Westlake Village, Thousand Oaks, Newbury Park, and Camerillo, and other firms are coming. Executives and engineers already living in developments that dot the rolling brown hills and commuting for hours into Los Angeles proper are easy pickings for recruiters selling a 5- or 10-minute daily drive. In effect, the industry is going to the personnel.

But nearly 100 miles south of the new boom, Orange County industry faces a basic barrier: a crunching labor bind, particularly for hourly assembly workers. At the low end of the pay scale, they are in short supply inside the county (4.7% unemployment) and cannot be brought in because of the high cost of apartments and gasoline for long commutes. Furthermore, manufacturers are plagued by high turnover.

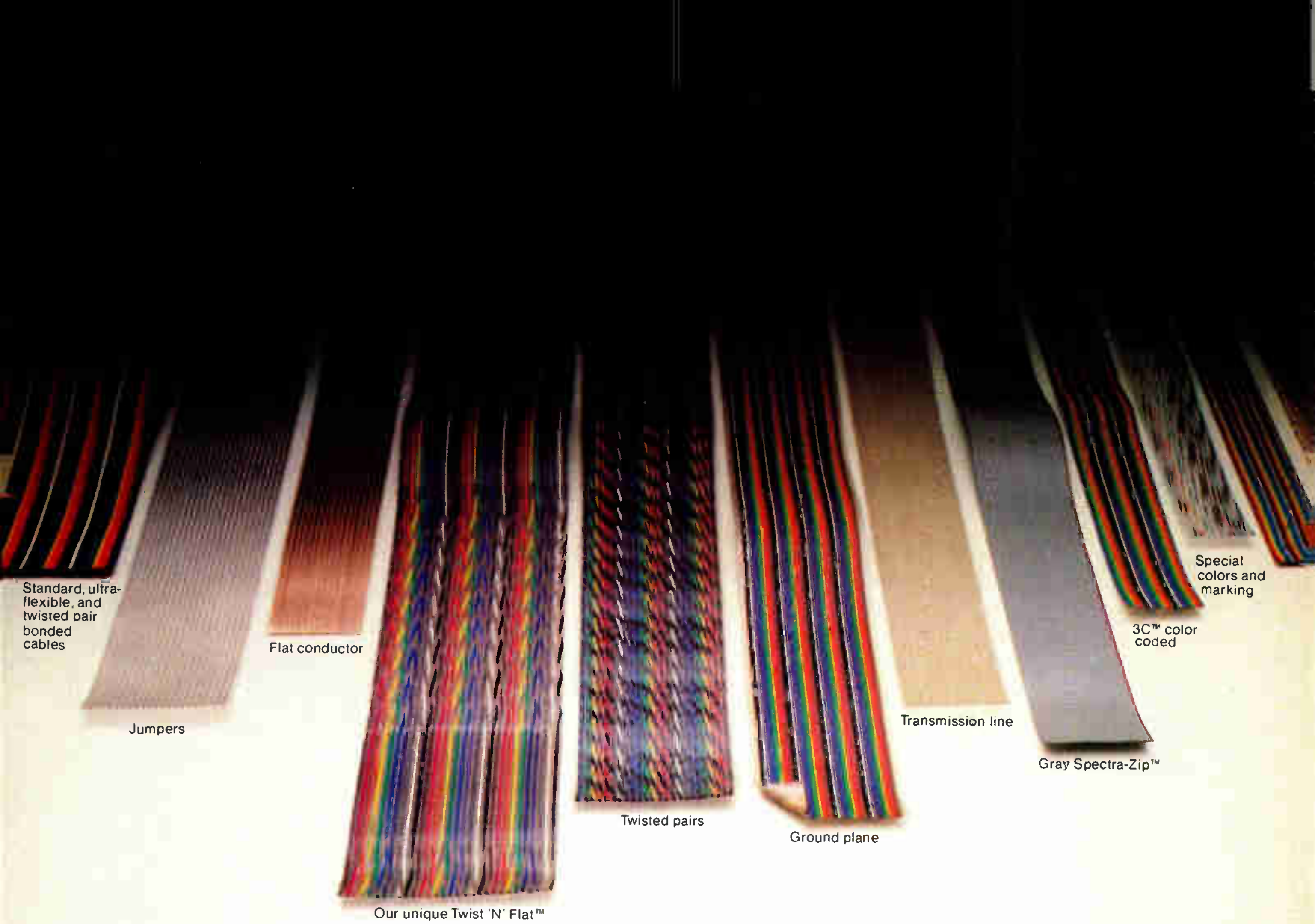
Behind this condition lies a cause seldom mentioned by companies, ironically one that attracted many in the first place: hourly rates average $6.67 lower than all contiguous counties.

Job hopping. However, for professionals the picture is different. Low pay is far from a problem for Orange County engineers, with many moving regularly from one minicomputer firm to another, always with nice raises. Some have worked for most of the major companies—General Automation, Computer Automation, Microdata, and Sperry Univac (formerly Varian). One result is a tightly knit group where news at one firm makes the rounds quickly.

Even farther south, San Diego in the past two years has picked off some major plants by aggressively seeking prospects and offering a hospitable environment. The roster includes Hewlett-Packard, Burroughs, NCR, Oak Industries, and others. □

California gets another proposition

The tax situation of California electronics firms and their top employees has improved considerably since 1978, with more relief possible. Since a heavy tax burden tends to drive both companies and engineers out of state, the change is important. First, the widely heralded Proposition 13 passed in June 1978 drastically slashed property taxes. Supporters call this a boon to the state's economy because freed funds go into more productive uses than government spending. Though some dispute this, most businessmen believe it. Then, last year the legislature finally killed the tax on inventory that industry had long fought. Proposition 9 is on the June ballot; it would cut state income levies about in half. It is given a better than even chance.



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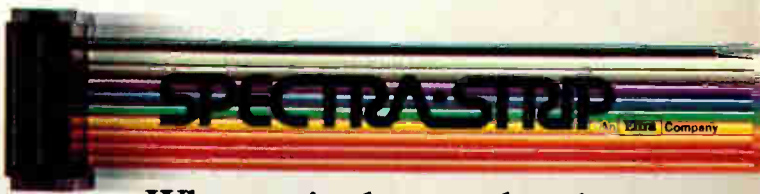

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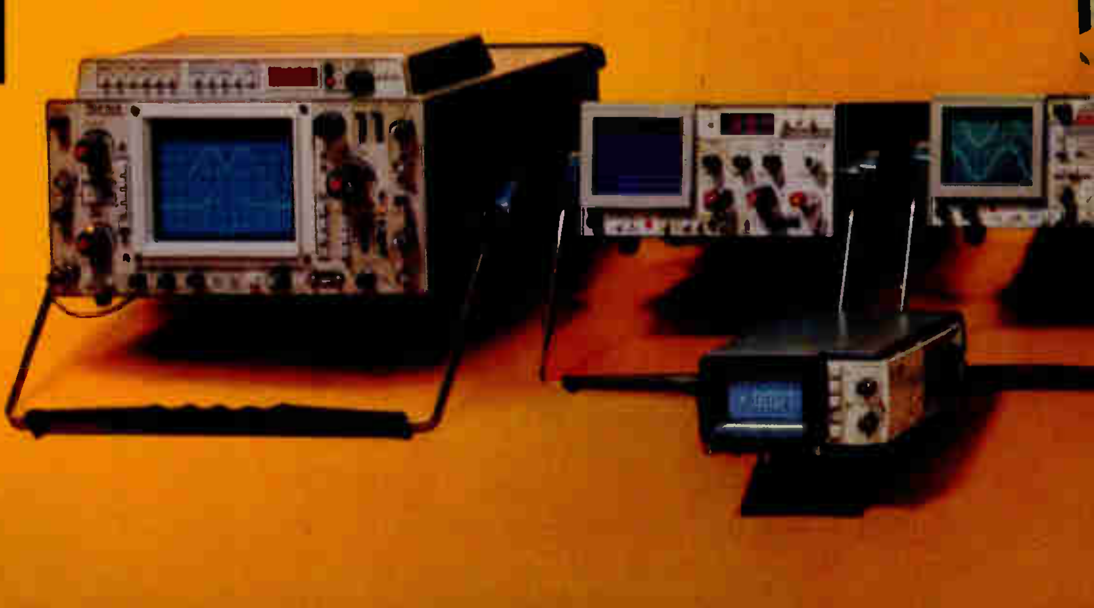

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	464	100 MHz @ 5 mV/div	yes	yes	5 ns/div	110 div/µs stored writing speed
	434	25 MHz @ 10 mV/div	yes		20 ns/div	Split-screen storage
	314	10 MHz @ 1 mV/div	yes		100 ns/div	Only 10.5 lbs (4.8 kg)
	214	500 kHz @ 10 mV/div	yes		1 µs/div	Only 3.5 lbs (1.6 kg)
	T912	10 MHz @ 2 mV/div	yes		50 ns/div	Low-cost bistable storage
Nonstorage Models	485	350 MHz @ 5 mV/div	yes	yes	1 ns/div	Widest bw in a portable
	475A	250 MHz @ 5 mV/div	yes	yes	1 ns/div	High-performance 250-MHz portable
	475	200 MHz @ 2 mV/div	yes	yes	1 ns/div	Highest gain-bw in a portable
	465B	100 MHz @ 5 mV/div	yes	yes	2 ns/div	Cost effective for 100-MHz bw
	465M	100 MHz @ 5 mV/div	yes	yes	5 ns/div	Triservice standard 100-MHz scope
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	305	5 MHz @ 5 mV/div	yes		0.1 µs/div	Autoranging DMM
	221	5 MHz @ 5 mV/div			100 ns/div	Only 3.5 lbs (1.6 kg)
	213	1 MHz @ 20 mV/div			400 ns/div	DMM/Oscilloscope @ 3.7 lbs (1.7 kg)
	212	500 kHz @ 10 mV/div	yes		1 µs/div	Low cost for dual trace & battery
	T935A	35 MHz @ 2 mV/div	yes	yes	10 ns/div	Variable trigger-holdoff and differential
	T932A	35 MHz @ 2 mV/div	yes		10 ns/div	Delayed sweep and differential
	T922	15 MHz @ 2mV/div	yes		20 ns/div	Low-cost dual-trace scope
	T922R	15 MHz @ 2mV/div	yes		20 ns/div	Rackmount version of T922
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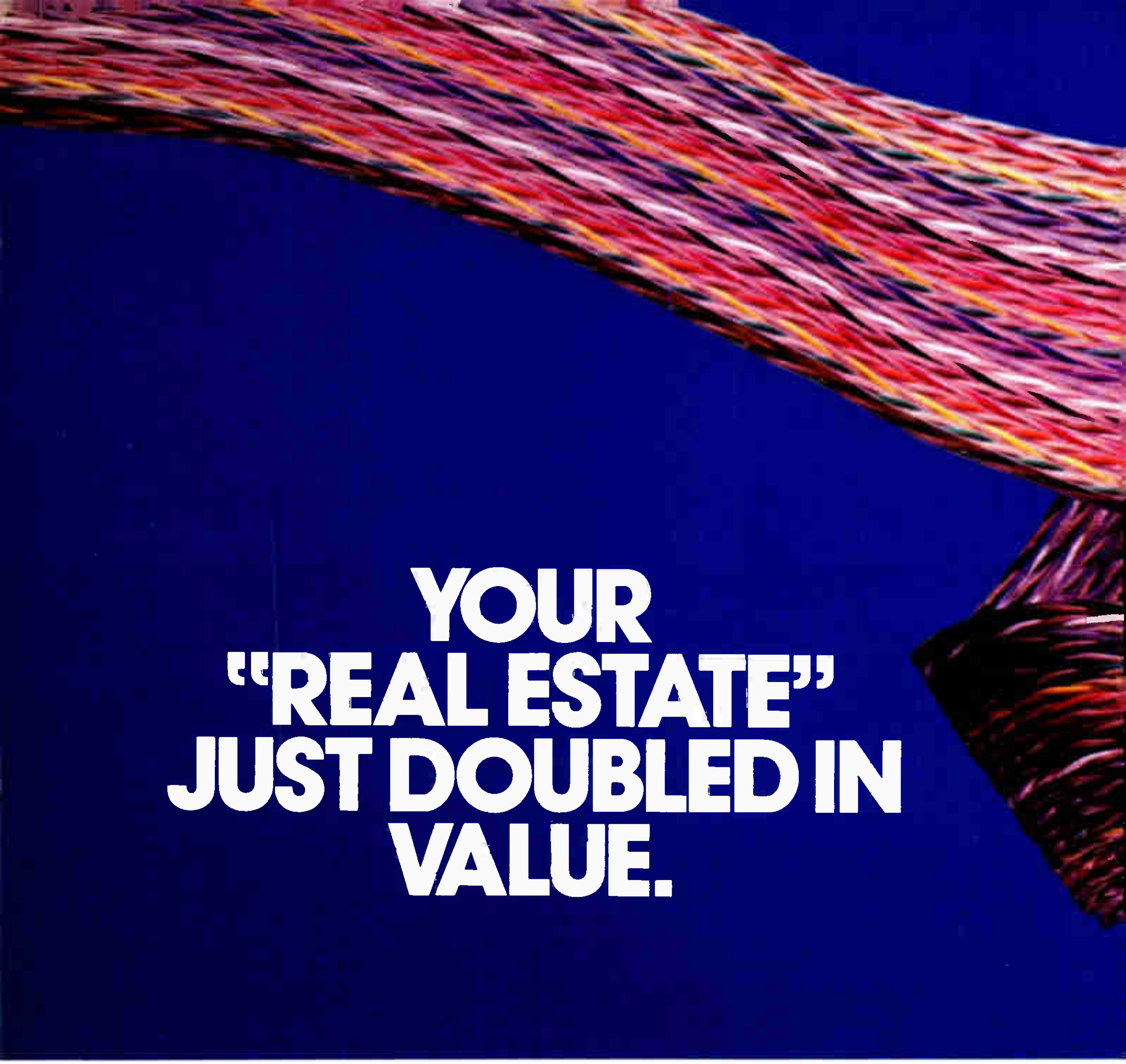

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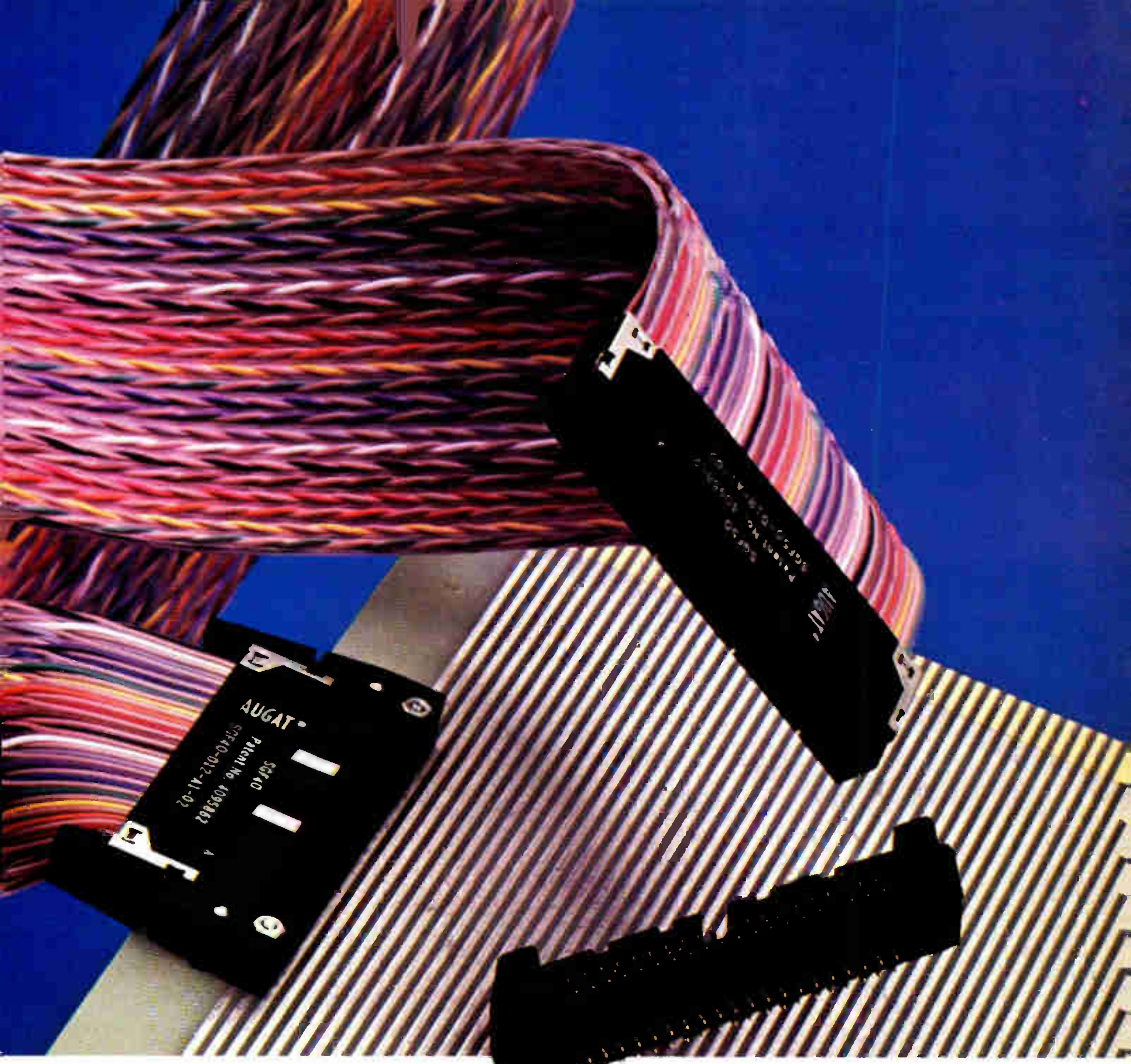

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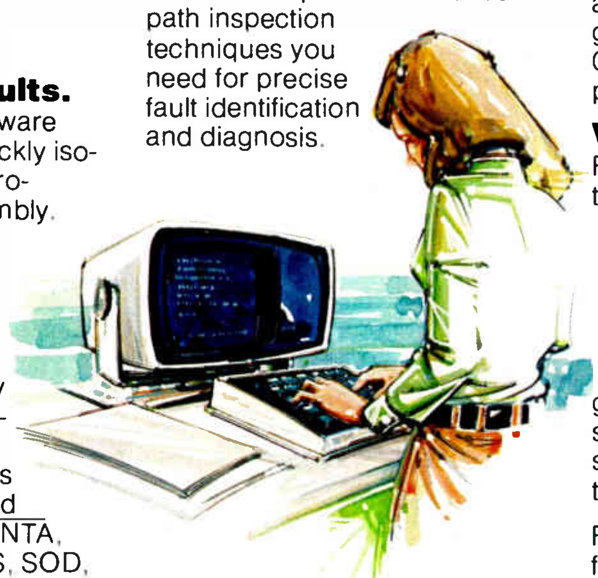

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Hardening RAMs against soft errors

Accelerated tests pinpoint effects on alpha-induced soft errors of dynamic RAM design changes, supply voltage, and cycle time

by Mark Brodsky, *Zilog Inc., Cupertino, Calif.*

☐ Since soft errors were first noticed in 16-K dynamic random-access memories more than two years ago, a barrage of technical papers detailing the physics of the phenomenon have been published. Much of this solid-state physics tends to confuse the end user of dynamic RAMs, who would benefit from a practical approach to the subject.

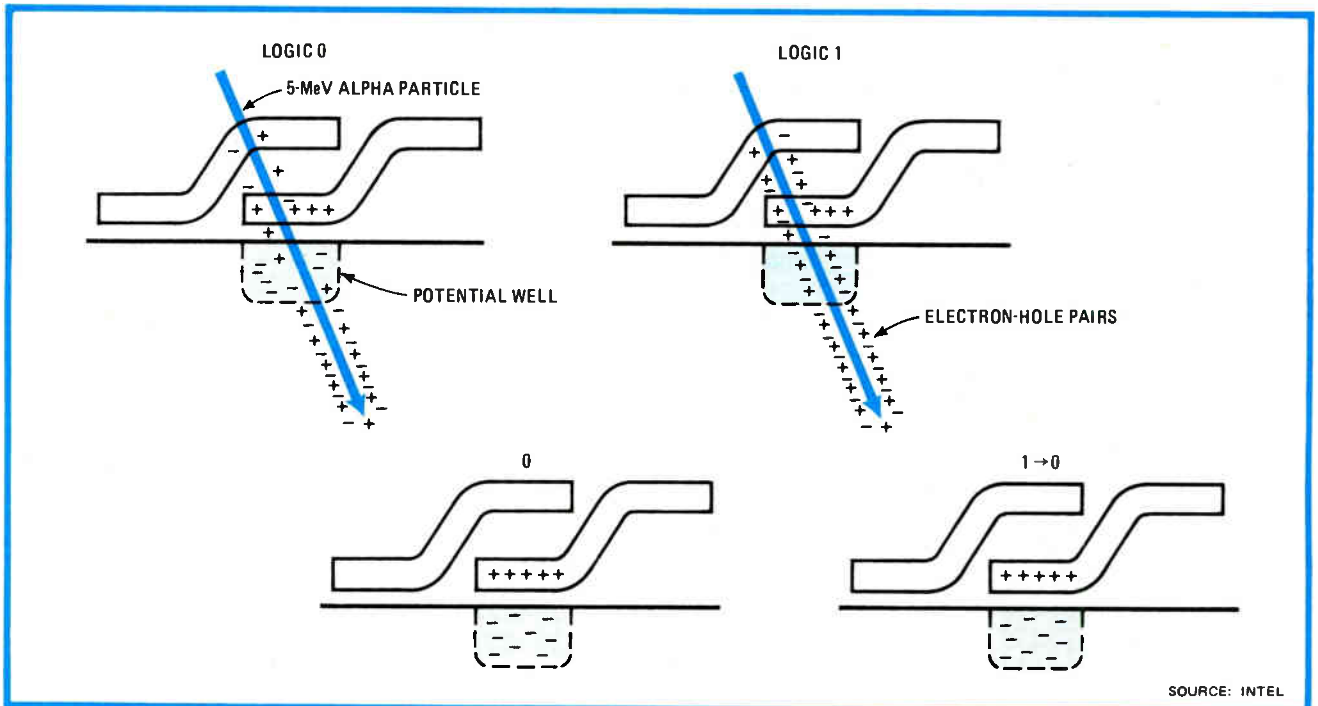
The following discussion of soft-error mechanisms centers around a description of instrumentation and test procedures developed by Zilog for measuring device susceptibility to alpha radiation and leads to recommendations for dynamic-RAM design, packaging, and operation that can reduce soft errors.

Dynamic RAMs rely on charge stored in cells; the level of charge determines the cell's bit state (logical 1 or 0). In a paper given at the April 1978 Reliability Physics Symposium, Tim May and Murray Woods of Intel Corp., Santa Clara, Calif., reported that the charge used to determine bit state could be upset and altered by alpha radiation coming from trace elements in a ceramic package. The resulting soft errors—in which a bit is switched from a 1 to a 0, or vice versa—cause no circuit damage and leave no tell-tale signs to indicate that they ever occurred. (Soft errors can, however, be detected and reversed using error-correction circuitry.)

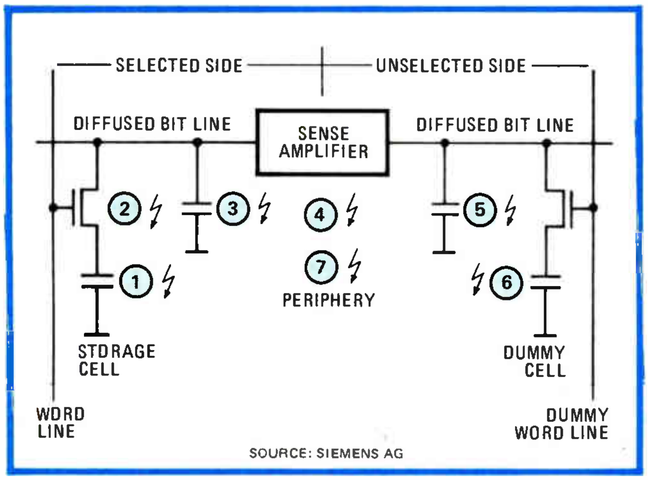
Fighting the flux

Recent papers from Bell Labs and Siemens have pinpointed the bit lines of dynamic RAMs as their most alpha-particle–sensitive areas. Meanwhile, systematic parametric testing of 16-K RAMs at Zilog has disclosed that errors caused by alpha radiation can be cut by raising supply voltage and lowering cycle frequency.

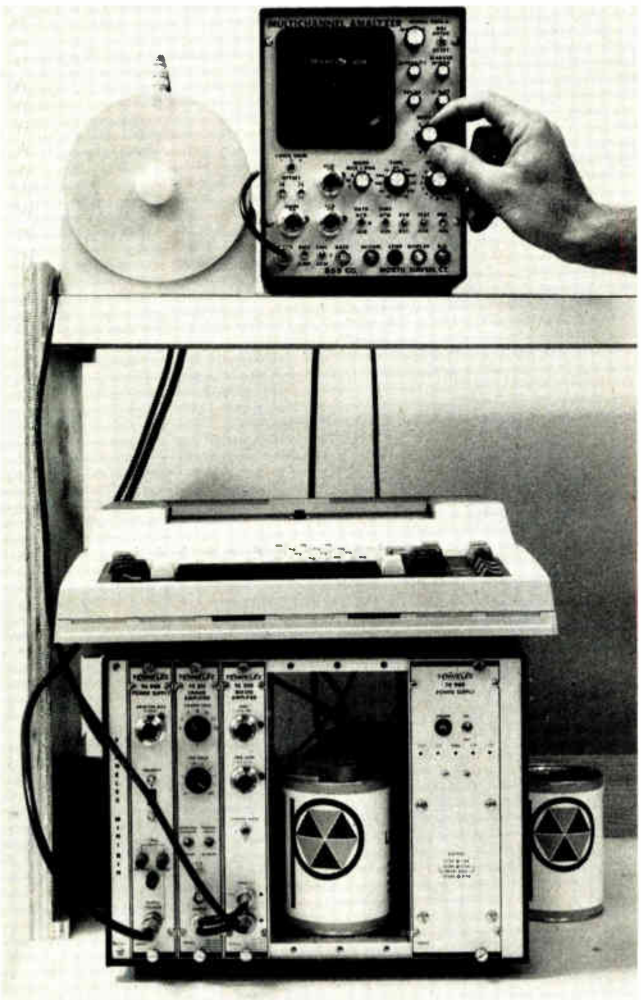
Alpha particles are helium nucleii (consisting of two



1. Penetration model. In an early model for alpha-induced soft errors in dynamic random-access memories, a particle strikes cells in both the logic 0 and 1 state (top). The cell in a 0 state is unchanged, but the 1-state cell's potential well is filled, changing its state to 0 (bottom).



2. Line hits. The numbered dynamic-RAM locations have been shown to be sensitive to alpha-particle hits. Depending on the location, either type of binary error can be generated: bit-line hits on the selected side (3), for example, can cause erroneous 1s.



3. Calibration. Calibrating alpha-particle sources improves data accuracy in accelerated soft-error testing. Zilog calibrates using a silicon-barrier detector (in vacuum chamber at top left), a multichannel analyzer, amplifiers, power supplies, and a printer.

protons and two neutrons, for an atomic mass of 4) ejected from atoms during nuclear decay of radioactive elements. Alpha flux, defined as the number of alpha particles emitted from a surface over time, is measured in alpha particles per square centimeter per hour ($\alpha/cm^2/hr$). Alpha radiation can be found almost everywhere since it comes from naturally occurring substances. For example, typical soil samples produce 1 or 2 $\alpha/cm^2/hr$. In fact, as little as one part per million of a radioactive contaminant will produce this level.

Practically all very large-scale integrated circuits—high technology devices such as RAMs, read-only memories, or microprocessors—are packaged with ceramic, sealing glasses, and quartz and alumina fillers. As it turns out, trace elements in ceramic are a source of alpha particles. Studies of ceramic packaging materials have found flux ranging from 0.01 $\alpha/cm^2/hr$ to 100 $\alpha/cm^2/hr$. Due to the fact that the ceramic only emits alpha particles from the side, the bottom poses little danger. The effective radiation a chip will experience is typically less than 0.5 $\alpha/cm^2/hr$, though some ceramic packages produce an effective flux of as much as 1 $\alpha/cm^2/hr$.

Uranium and thorium traces are the major radioactive contaminants to be found in semiconductor packaging materials. These elements emit alpha particles with energies that range up to 8.78 million electron volts. Studies by Bell Labs show that alpha particles of 5 million electron volts or less entering the silicon at an angle cause the most soft errors in dynamic RAMs.

When alpha particles hit and penetrate the surface of a silicon device, the particles slow down and produce about 1 million electron-hole pairs of charge. The higher the energy content of the alpha, the deeper the charge penetrates into the silicon. Penetration is typically to tens of micrometers.

A soft cell

Two general physical models have been proposed to explain soft errors in dynamic RAMs. May and Woods of Intel based their explanation of soft errors on a cell model. In this model, the energy generated by a penetrating alpha (1.4 million electron-hole pairs generated to a depth of 25 μm) was large enough to offset the existing charge on a memory cell it hit or passed close to.

Figure 1 illustrates May and Wood's model. The top two views represent the equivalent of two cells in a 16-K dynamic RAM. The cell at top left is in the binary 0 state, its potential well filled with electrons. The cell at top right is in a binary 1 state with its potential well empty.

In the two bottom views, an alpha particle with an energy of 5 million electron volts strikes each cell and penetrates to a depth of 25 μm. The 0-state cell with its full potential well is unaffected. The 1-state cell's previously empty potential well is filled with the excess charge and the cell is switched to a binary zero state.

In this model, if the charge of a cell's potential well is high (binary 0) or if the cell is isolated from alpha-induced charge, there is little chance of a soft error in that cell.

In May and Wood's model, only binary ones can be converted to zeros. But actual tests on 16-K devices show

Alpha-particle interest accelerates

Alpha-particle–induced errors in dynamic RAMs are no longer the scientific curiosity they were when first reported in 1978. Soft errors are serious business now, as evidenced by the large numbers of technical papers being given on the topic. Still another indication is the appearance of in-house 16-K dynamic random-access memory specifications that for the first time actually give a maximum alpha-particle–induced error rate for purchased devices: Hughes Aircraft Company has set a soft-error rate spec of 1 error in 5 million operating hours on a 16-K dynamic RAM.

Four papers on this topic were given at this year's International Reliability Physics Symposium held on April 8–10 at Las Vegas, Nevada. Among the four papers was "Parametric Influences on System Soft Error Rates," by J. W. Peeples and T. J. Every, NCR Corp., West Columbia, S. C. This paper described a test system capable of monitoring two megabytes (1,024 16-K dynamic RAMs) of system memory for assessing the effects of critical system parameters on alpha-induced soft errors.

A second paper, "Collection of Alpha Particle Generated Charge by VLSI Device Structures," by T. C. May and B. F. L. Ward of Intel Corp., Santa Clara, Calif., looks at the collection of charge deposited by alpha particles impinging on various MOS memory structures with regard to total charge collected and the time profile of the collection. Measurements are compared with theory and results discussed in terms of the reliability of future devices.

The third, by B. J. Masters of International Business Machines Corp., Hopewell Junction, N. Y., was titled "Experimental Studies of ZnS Alpha Particle Counters and Methods for Minimizing Detector Background." It discussed a zinc sulfide scintillation counter employed at IBM for low-level alpha-flux monitoring of devices and packaging methods. Experimental measurements of contributions to the total background count rate by electrical noise, cosmic radiation, and radioactive contamination were discussed.

Perhaps the most useful paper was "Alpha-Particle-Induced Soft Errors and 64-K Dynamic RAM Interaction" by R. McPartland, J. Nelson, and W. Huber of Bell Laboratories, Allentown, Pa. This paper took up where earlier papers on 16-K RAMs leave off, reporting on the cause of alpha-induced soft errors and design changes made to reduce their frequency of occurrence in a 64-K RAM.

The authors reported that tests were first run on an early preproduction 64-K RAM, which uses a double-polysilicon cell structure and polysilicon bit lines. Bell measured alpha soft-error rates by exposing lidless memories to a calibrated alpha-radiation source and then scaling the error rate down to expected package radiation levels, a method similar to Zilog's (see main text).

A high rate of soft errors was found to be due to cell hits, as well as sense-amplifier bit-line hits. Those results agree with Bell's earlier theories on the cause of soft errors in 16-K RAMs.

In a revised design of the 64-K RAM, cell sensitivity to alpha hits was almost eliminated by increasing the cell's stored charge; however, that required a memory array redesign, which increased cell area significantly.

The redesigned RAM's sense-amplifier bit-line soft errors remained high. Selective masking showed that those errors were caused by alpha hits on the sense-amplifier node. To reduce the sense-amplifier soft-error rate, the impedance of the devices connecting the bit lines to the sense amplifiers was lowered. These and other fixes in timing and reference cells allowed the Bell engineers to achieve an overall alpha-induced soft-error rate of about 4 failures in 17 operating hours on their 64-K memory.

It is certain that specs of this type will soon be appearing on the data sheets of all commercially available dynamic memories. **-Jerry Lyman**

that alpha particles can change either bit state.

A more realistic model for dynamic RAMs has been proposed by David Yaney, J. T. Nelson and Lowell Vanskike of Bell Laboratories, Allentown, Pa., based on a floating capacitor model. In their analysis, the primary soft-error mechanisms are alpha hits on the bit lines, sense amplifiers, and peripheral circuitry.

Gunter Schindlebeck of Siemens AG, Munich, West Germany, presented a detailed analysis of this model in a paper given at the April 1979 Reliability Physics Symposium. Figure 2, taken from Schindlebeck's paper, is a representation of the alpha-sensitive areas of a 16-K dynamic RAM. The model shown is quite close to the simplified equivalent circuit of a cell of an actual dynamic RAM.

Depending on where an alpha particle strikes in this model, binary 1 errors, binary 0 errors, or both can be generated. Referring to Fig. 2, alpha-particle impacts on the spacings between memory cells (2), the sense amplifiers (4), and the peripheral circuits (7) are sources of both types of errors.

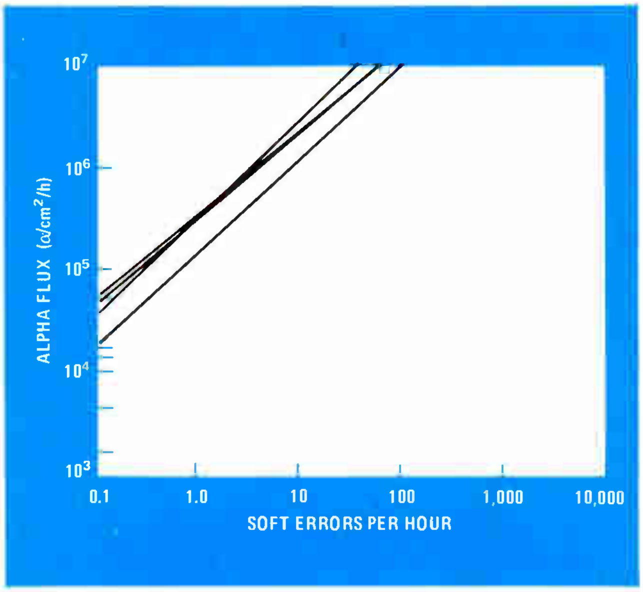
Hits on the storage capacitor (1) of the memory cell and the diffused bit line of the selected side (3) result in erroneous binary 1s, whereas hits on the dummy cells (6) as well as the nonselected bit lines (5) can be a source of binary-0 errors.

It is important to keep in mind that soft errors are also a function of the RAM's timing. Dynamic memories are constantly being cycled to refresh cell charge and to read and write new data. During each of these cycles, the contents of the cells must be compared with a reference cell. This determines the present value of the cell so it can be rewritten.

A well-placed alpha particle hitting at just the right time in this sequence will cause false information to be read or rewritten. Although cell charge may be sufficient to survive alpha hits, the design and timing of the sensing circuits for 16-K dynamic RAMs makes them susceptible to alphas.

Accelerating errors

There are two possible ways to measure soft-error rates of 16-K dynamic RAMs. One is to test units over long periods and the other is to run accelerated tests. The former uses a large memory system with many 16-K devices. The system is monitored for soft errors for a period of weeks or months. Results fairly accurately tell the expected rate of soft errors per device-hour. How-



4. Microprocessed. A microprocessor monitors RAMs for soft errors while they are irradiated by calibrated alpha sources in a small test setup. Plots from data on four 16-K dynamic RAMs tested at two radiation levels can be extrapolated to package radiation levels.

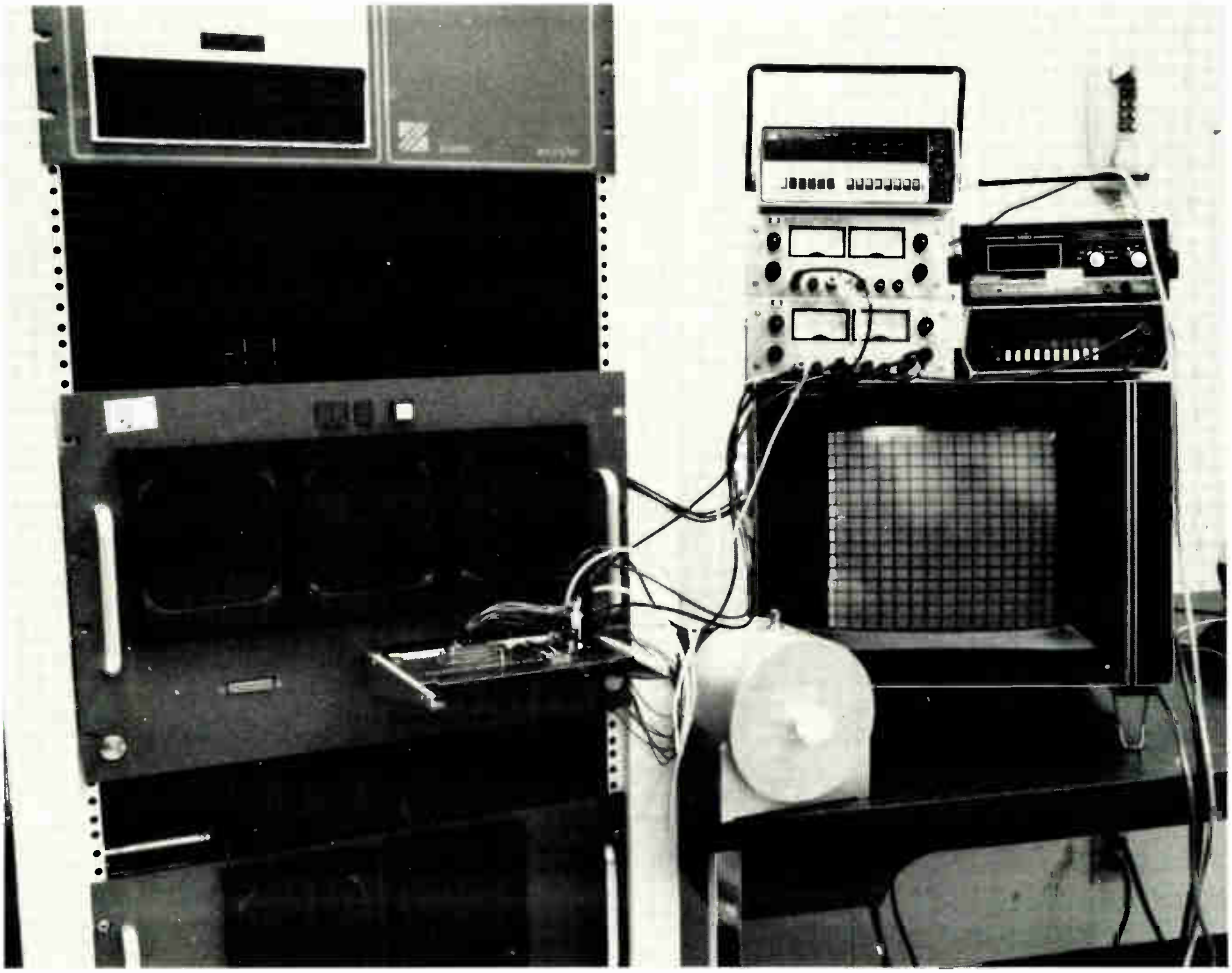
ever, the excessive test time and lack of test-condition flexibility make this mode of testing impractical.

A better approach is to speed up the alpha-caused soft errors. This involves exposing individual devices to alpha radiation stronger than their residual package radiation. If the test dose is not too large, an accelerated soft error rate can be extrapolated back to the package's alpha radiation level. The main advantage is that the test can be run in hours and not weeks, as in real-time testing.

In the accelerated test mode, a source is used with alpha flux varying from 50,000 to 50,000,000 $\alpha/cm^2/hr$. It is vital to accurately calibrate the intensity of the alpha flux striking the IC chip, since any interpolation calculations depend on an accurate starting point.

If uncalibrated sources are used, two types of errors will crop up. First, certain alpha sources have short half lives. This means these sources may yield far fewer alpha particles than their posted Curie level would predict. Second, sources with long half lives may have contaminants that add to the alpha flux.

Zilog has used a calibration setup that includes a silicon-barrier detector made by Princeton Gamma Technology Inc., a 1056A multichannel analyzer from DSD Co., a thermal printer for hard copy of the data, and



5. Errors displayed. A larger test setup includes a raster-scan display for evaluation of circuit-parameter changes. The large-screen cathode-ray tube shows the state of all bits of a single RAM; a soft error causes the corresponding bit symbol to dim or brighten.

amplifiers and power supplies (Fig. 3). Test sources are exposed to the charged junction layer in a vacuum chamber (the cylinder at top left). As alpha particles strike the detector, the energy is amplified and fed into the multichannel analyzer, which shows the number of alpha hits and their relative energy levels. The alpha detector is easily calibrated with fixed-energy sources to ensure accurate reading of the test source's flux.

It is important to calibrate an alpha source under the actual conditions of a soft-error test. Typically the source would be in air at a distance of 0.25 centimeter from the surface of the barrier detector.

Testing softly

Soft-error detectors vary from a simple setup built around a microprocessor to a complex memory raster that graphically displays a large pattern of all the bits of a dynamic memory.

In the microprocessor-based approach, memories to be tested have their lids removed and calibrated alpha sources are taped on top. The microprocessor then writes a pattern of 1s and 0s into the memory. The microprocessor continually reads the memory's contents and checks for any change in state.

After several days, the number of soft errors per unit per hour is plotted against alpha flux on log-log paper. Results from tests on the same device using two or more different sources will produce a straight line on log-log graph paper.

An example of microprocessor-based results is shown in Fig. 4. Here four samples of an MOS 16-K dynamic RAM have each been tested with two radiation sources—americium 241 and thorium 232.

Soft-error rates at the package-radiation level of a RAM can be found by extending the straight lines of Fig. 4 to the point where they intersect the actual package-radiation level. Based on the straight-line relationship of Fig. 4, alpha particles from the ceramic packages of the units tested should cause less than one soft error every 5 million operating hours.

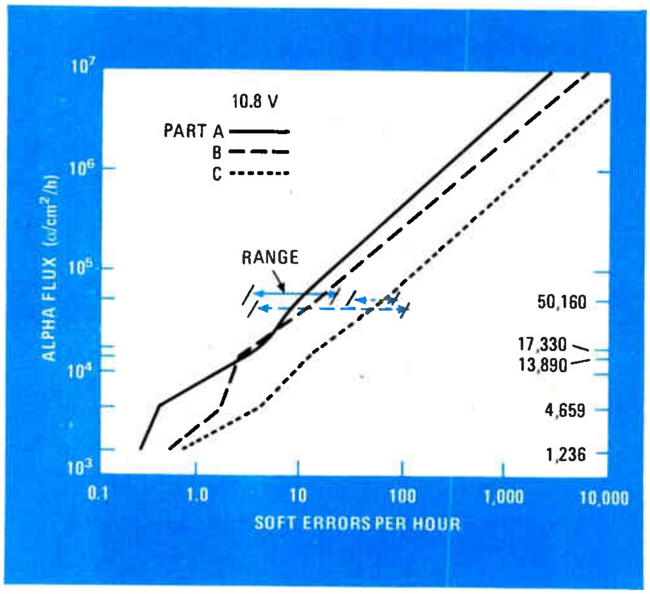
A major drawback of the relatively simple microprocessor error-detection system is its lack of flexibility: controlling parameters such as charge level and cycle frequency of the dynamic memory are fixed. For more analytical work, a larger device tester called a raster-scan tester should be employed.

The raster equipment is shown in Fig. 5. The device under test is placed in an evacuated cylinder (lower center) along with its calibrated radiation source. Control circuitry, shown at left, feeds a pattern of all binary 1s or 0s into the dynamic memory.

The states of all 16 K bits are displayed as dots on the face of a cathode-ray tube (lower right). As a soft error occurs, the corresponding location will dim or glow brighter, indicating a change of bit state.

Soft-error rate is computed in the same manner as in the microprocessor test, by measuring the soft errors per hour. Fig. 6 shows an analysis of three different groups of 16-K RAMs, each from a different manufacturer.

To increase the accuracy of the data, four alpha-particle blocking screens made of polyimide were constructed to restrict the alpha flux generated by a thorium



6. Screening sources. Five calibrated levels of radiation from a single source were used to evaluate three goups of 16-K dynamic RAMs for soft-error rate. The five radiation levels (right) were obtained with alpha-particle–blocking screens made of polyimide.

foil. After the first unscreened reading, the four screens were used to provide five calibrated levels of alpha radiation ranging from 500,000 down to 1,700 $\alpha/cm^2/hr$. The data approximates the expected straight-line patterns when plotted on log-log paper.

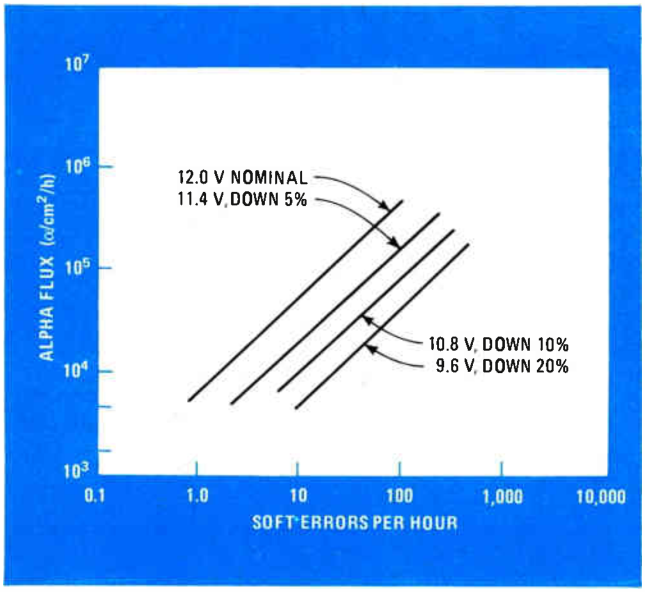
The primary advantage of raster testing is its ability to vary dynamic-RAM parameters that affect soft errors. Two of the more important variables are supply voltage (V_{dd}) and cycle time (the interval between the call for and delivery of information).

Supply voltage controls the absolute charge in a dynamic RAM cell. This voltage also determines the difference in voltage between the cell and the comparison (or dummy) cell used to determine cell state during read and refresh cycles.

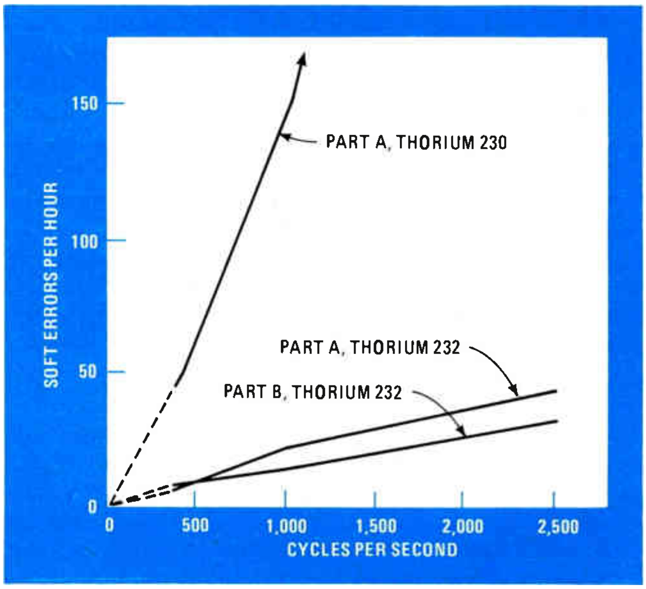
The effect of varying the supply voltage is shown in Fig. 7. A 16-K dynamic RAM has its V_{dd} varied from a nominal 12 volts to 9.6 V in four steps. These test results show that a 20% reduction in source voltage will increase soft errors by an order of magnitude. So it is safe to conclude that increasing supply voltage increases the alpha-particle resistance of both the memory cell and the reference-comparison sequence.

Each refresh, read, or write cycle opens time "windows" during which a well-placed alpha particle can cause a soft error—so cycle time must influence soft-error rate. To verify this, tests were run on the raster system using two different alpha-particle sources and varying the RAM cycle time. One type of RAM was exposed to a thorium 232 source with an alpha flux of 50,000 $\alpha/cm^2/hr$, and the second RAM type was tested with both thorium 232 and thorium 230 (273,000 $\alpha/cm^2/hr$) sources. The results of these tests (Fig. 8) show that the soft-error rates of these devices go to zero as the cycling rate decreases.

Additional tests can be developed to isolate other individual aspects of cycle susceptibility. Kamal Gunsag-



7. Supply-voltage effect. Decreasing a dynamic RAM's supply voltage brings up its soft-error rate, according to results from raster-scan tester. In this test, a RAM in a ceramic package has its lid removed and a thorium-235 foil taped on its top as a source of alpha radiation.



8. Varying cycle time. Results plotted for two dynamic RAM types show that slowing the rate of read, write, and refresh cycling reduces the RAM's soft-error rate. RAMs of type A were subjected to two levels of radiation from different sources in this test.

er of Zilog is presently developing results of tests into a general 16-K characterization model. This model (to be published in the future) relates the individual cycle-mode susceptibility to specific fabrication and timing design criteria.

Error reduction

The previous tests show how external factors like increasing supply voltage and increasing cycle time can cut soft-error rates. There are other factors at the packaging, device design and processing, and system levels that should also be considered in the effort to minimize soft errors.

As far as the device's ceramic package goes, a totally alpha-free material is not currently available and it is unlikely that it ever will be. Although radiation levels are low in typical ceramic packages, as a safety precaution to cull out high alpha rate materials, all ceramics should be monitored for a maximum alpha level of about 0.05 $\alpha/cm^2/hr$ at incoming inspection.

It is possible for a surface-barrier material applied to either the die or package lid to give 100% alpha protection, but Zilog does not think this necessary. This material must have sufficient alpha-stopping power, ionic purity, low bond-wire stress, good die adhesion, and an ability to withstand package-sealing temperatures without degrading hermeticity. That is a tall order for the less-than-ideal conditions found in large-scale production. Actually, soft-error rates of some 16-K devices are already so low that these coatings are unnecessary.

The designer of the chip circuitry can make his device less susceptible to soft errors in several ways. These include increasing charge capacity in the memory cell, lowering the resistivity of the substrate, and going to metal bit lines.

There are two ways to increase charge capacity. The first requires a larger cell, an undesirable change since this means a bigger die and consequently lower yield per wafer. The second way relies on the recently improved integrity of thin-oxide films. This allows a thinner gate oxide for the storage capacitor, which increases the amount of charge stored. Additionally, novel cell designs will allow increased charge capacity for the same storage area.

If the resistivity of a dynamic memory's substrate is lowered and if diffusion lengths are short, most of the electron-hole pairs generated by the dissipation of alpha-particle energy would recombine before disturbing the charge-storage cells. However, the trend is toward substrates with higher resistivity in dynamic RAMs—to reduce junction capacitance. A possible solution is to develop a high-resistivity epitaxial layer over low-resistivity material.

In present dynamic RAM designs, most circuit nodes float for some time during the cycle—and that is when they are most susceptible to alpha hits. A design with better timing between successive clock pulses could conceivably cut down this float time.

Finally, replacing a diffused bit line with a metal line results in a smaller junction area. This in turn makes the metal bit line more resistant to alpha particles.

Clean layout

A clean board layout with adequate decoupling would cut down soft errors resulting from the combination of alpha hits and system noise. Another system fix, as noted earlier, is to skew the power supply voltage toward the high side of the device specifications.

Alpha radiation is here to stay. Although material suppliers are hunting for purer ceramics, this problem will not go away. Even though the soft-error rate of some current 16-K RAMs is quite low, future dynamic RAMs must be designed with the effect of alpha radiation and the reduction of that effect in mind. □

16-bit microprocessor enters virtual memory domain

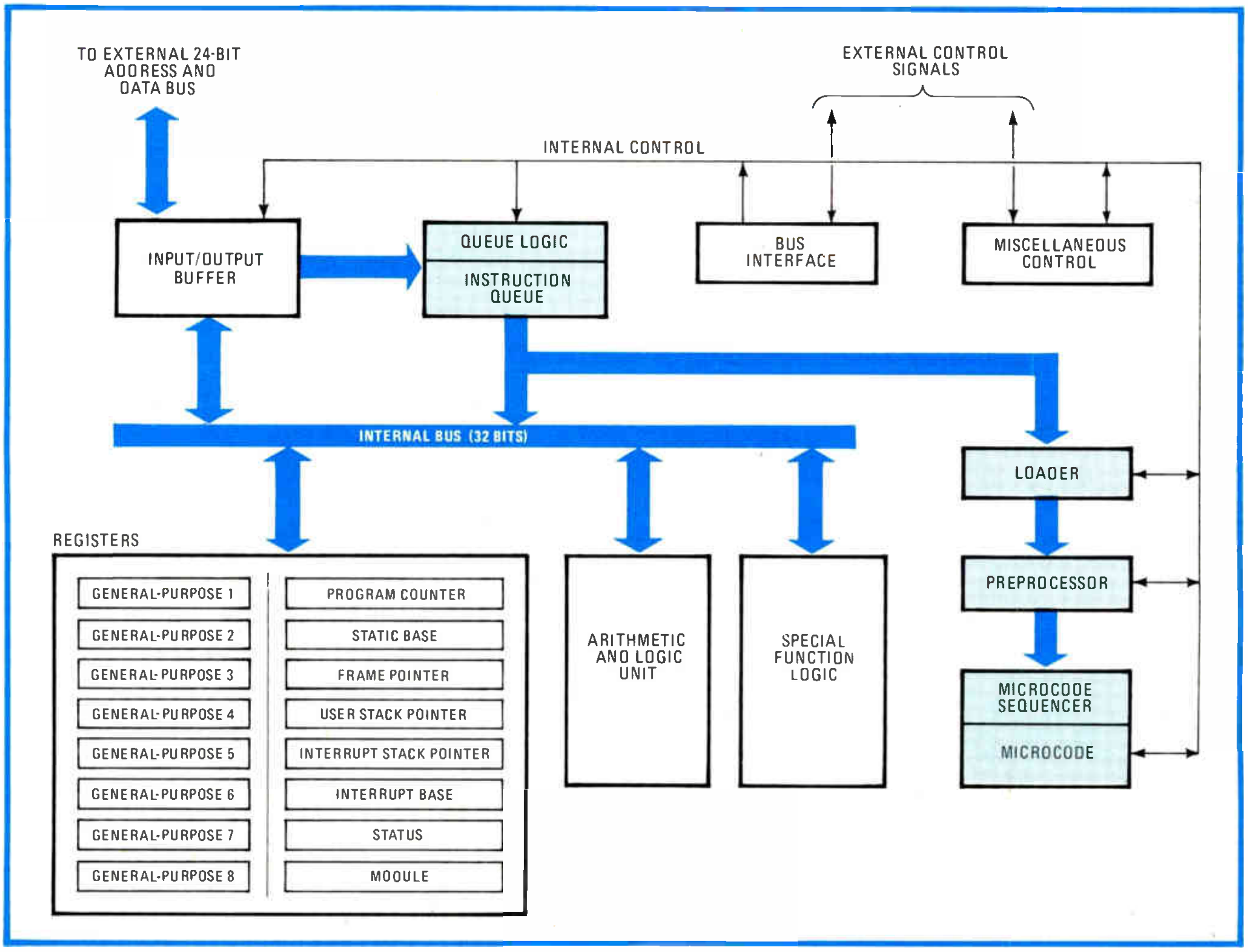
Central processing unit supports 24-bit addresses; memory management unit offers instruction-aborting facility vital to virtual memory systems

by Yohav Lavi, Asher Kaminker, Ayram Menachem, and Subhash Bal, *National Semiconductor Corp., Santa Clara, Calif.*

☐ The concept of virtual memory used to be the exclusive domain of mainframe computers. Now that the capabilities of high-end 16-bit microprocessors are approaching those of bigger systems, they, too, are finding virtual-memory–based designs necessary and desirable.

The latest of these advanced microprocessors, the NS16032 central processing unit uniformly addresses 16 megabytes. In addition, it fully supports virtual memory systems. When the device is used in conjunction with the NS16082 memory management unit, it enables the user to construct a flexible page-oriented virtual memory system that, with the proper operating system software, can address 16 megabytes of virtual memory.

The driving force behind virtual memory systems is the desire to increase storage size while making memory management functions transparent to programmers. Among the reasons for wanting large storage space is the current trend toward larger applications programs, as well as toward larger and more sophisticated operating



1. Big brother. The largest of the 16000 family of microprocessors, the 16032 central processing unit operates on 16-bit data but features 32-bit internal bus and general-purpose registers and a three-stage instruction pipeline. It uses 24-bit addresses to access 16 megabytes.

The virtues of virtual memory

Memory has been a problem from the time the Eniac computer was first switched on in 1946. Programmers realized almost immediately that managing it was a major overhead chore. One early solution was to allocate memory before a job was run, but the allocation would not be changed once execution of the program was started.

A more sophisticated approach was developed by a group of researchers at Manchester University, Manchester, England, in the late 1950s. Memory was divided into logical pages, which were then swapped between a peripheral drum memory and the main core memory as needed. In this way the system itself handled the housekeeping chores of memory allocation. The Atlas computer, completed in 1962, was the first to implement what later became known as virtual memory.

The first commercial computer to employ this type of memory management was the Burroughs B6500, introduced in 1966. But not until IBM coined the virtual-memory name and added it to the System/370 model 158 and 168 in 1972 did the idea catch on. Now it is widely used in the mainframe industry and on many larger minicomputers.

With virtual memory the user regards the combination of main and peripheral storage devices as a single large storage space. Consequently, the user can write large programs without worrying about the physical memory limitations of the system.

To accomplish this, the operating system software places some of the users' programs and data in peripheral storage. When they must be brought into main memory for execution, the system performs an operation called a page swap. Information not currently in use is removed from the main memory and returned to peripheral storage, making room for the new material. For efficiency, when the referenced location has to be brought from the peripheral to main memory, other locations likely to be referenced next are brought also.

Of course, the beauty of virtual memory is that the user, or programmer, does not have to be aware of this process. He uses one consistent set of addresses, called virtual addresses. The memory management hardware keeps track of where the information resides at any moment and converts, or translates, the virtual address to its real location in main memory. When the hardware finds the virtual address requested unavailable in main memory, it initiates a swap procedure.

systems software. Furthermore, business, teleprocessing, and communications applications require increasingly large data spaces. Efficient multiprogramming demands virtual memory. The continuing reduction in memory prices—both electromechanical and solid-state—makes it economically feasible to include a large virtual memories in a system.

Economical expansion

However, the solution for large storage requirements does not necessarily lie in physically large memories in the form, for example, of many random-access memory chips. Such a simple memory addition is not economical, especially since programmers will generally use all the available memory. This approach also makes it difficult to add new tasks to a system because it forces programmers to resort to memory management techniques, such as overlay memory structures, that limit programming efficiency.

On the other hand, a virtual memory scheme allows the expansion of storage quite economically since a significant portion of the memory can be less expensive than mass storage such as disk (see "The virtues of virtual memory," p. 124). Also, it frees the programmer from worrying about the housekeeping details of memory management. That is especially important because software development costs represent an ever increasing portion of system development cost.

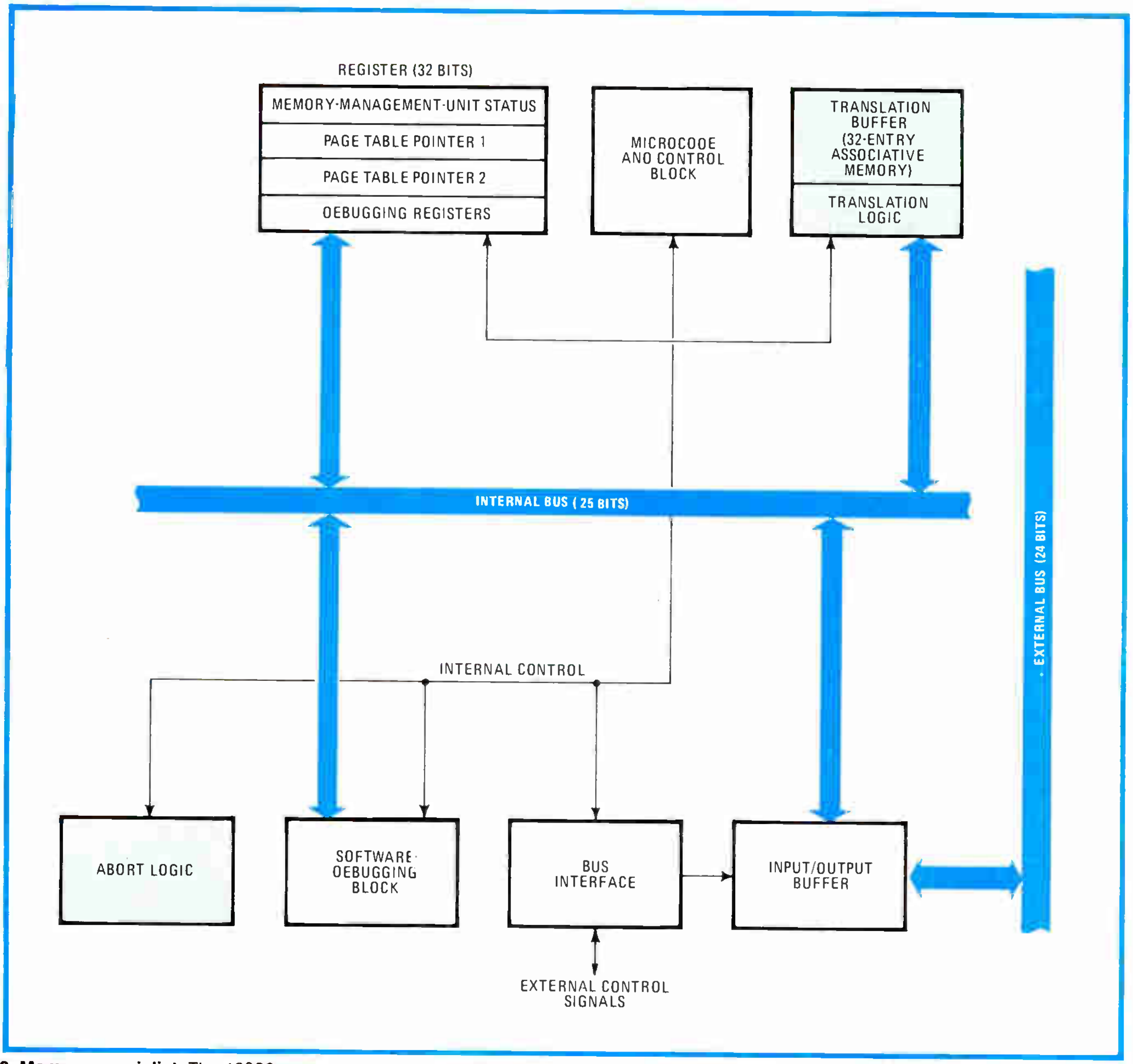
But a microprocessor chip—like any computer—needs dedicated hardware to support virtual memory system software. This special hardware, not available on current microprocessors, is now provided on the 16032 CPU and the 16082 memory management unit.

Before examining this special virtual memory hardware, it is useful to describe the basic 16000 architecture. The 16032 is the largest of the 16000 family of microprocessors, which also includes the scaled-down NS16008 and NS16016. (Although architecturally compatible, these parts do not support virtual memory and are instead intended as low-cost CPUs for small and medium-sized systems). These parts will be available in sample quantities by the end of the year or the first quarter of 1981 at the latest. The 16000 family's architecture supports a single uniform address space and allows 32-bit addressing that can access 4 billion bytes of memory. In the initial offering of the 16032, however, only 24-bit addresses are implemented, which allows access to 16 megabytes.

Also supported in the 16000 architecture are 16 32-bit general-purpose registers and 17 special-purpose registers. Eight of the general-purpose registers are contained on the 16032 CPU chip, along with 8 special-purpose registers (Fig. 1). The other 8 general-purpose registers are contained on the special NS16081 floating-point mathmatics chip, along with the floating-point status register (see "Expanding the architecture through slaves," p. 126). The rest of the special-purpose registers are in the memory management unit described later.

Addressing modes

Nine addressing modes are provided in the 16000 architecture, four of which are unique. Top-of-stack addressing allows manipulation or referencing of an operand on a stack by all instructions as in a stock machine. Relative addressing lets the pointer reside in memory rather than in a register. External addressing supports the 16000's software module concept (see "Modular software leaves room for growth," p. 128), which allows the modules to be relocated without linkage editing. Finally, scaled indexing can be added to any of the addressing modes to index and address automatically by units of 1, 2, 4, or 8 bytes, providing easy addressing



2. Memory specialist. The 16082 memory management unit handles virtual address translation and memory protection. A unique feature of this chip—vital to virtual memory schemes—is the abort facility that interrupts instructions on the CPU when needed data is not in memory.

of arrays of byte, word, double-word, or quad-word quantities.

Along with these memory-addressing features, the 16000 architecture includes over 100 basic instructions. This instruction set is symmetrical—any instruction can be used with any addressing mode and any operand length, including byte, word, and double-word. These instructions allow operations between memory locations as well as between registers, a feature that facilitates register allocation for compilers.

Internally, the NS16032 has 32-bit-wide data paths and features a pipeline organization. An instruction queue holds up to 8 bytes of instructions for decoding by a preprocessor before a microcode sequencer actually locates the microprogram necessary for executing the instruction.

The CPU chip interfaces with the outside world through a 24-bit-wide multiplexed address and data bus. To facilitate the design of operating systems, the 16032 operates in two modes—user and supervisor. Privileged instructions for the operating system cannot be executed when the CPU is in the user mode.

To make this microprocessor into a virtual memory machine, the 16082 memory management unit (MMU) is paired with the 16032 CPU. The two could be conceived of as a single CPU that simply produces a physical memory address. Because of limitations in chip size, however, the MMU was fabricated as a separate chip that operates as a slave processor to the CPU.

The MMU shares the external multiplexed address and data bus with the CPU and can assume full control of this bus for fetching information from main memory tables.

The MMU contains the logic for doing the dynamic address translation as well as for memory protection. A

Expanding the architecture through slaves

The NS16000 architecture's novel design supports additions to its instruction set with specialized slave processors. To the programmer, the computer looks like a single central processing unit with a large set of instructions. In reality, the hardware consists of several specialized or slave-processor chips attached to a CPU.

When the CPU receives an instruction that is to be executed by a slave, it routes that instruction with the appropriate data to the slave processor for execution. If the necessary slave processor chip is not in the system, the CPU generates a software trap, allowing the instruction to be emulated with software routines.

Currently, there are two slave processors in the NS16000 family: the NS16082 memory management unit and the NS16081 floating-point processor. Compatible with the floating-point arithmetic standard proposed by the Institute of Electrical and Electronics Engineers, the latter can operate on both 32-bit single-precision operands and 64-bit double-precision operands. It contains eight 32-bit data registers plus a floating-point status register with control information for dealing with the CPU. Three separate processors in the chip manipulate the mantissa, sign, and exponent, respectively, under the control of microcode stored on the chip.

One advantage of the slave approach is that the user can build an entry-level system without slaves using software emulators. Later, higher performance systems can be built by adding the slave chips and removing the software emulators. Another advantage is that as technological advances make it possible to integrate these functions onto a single chip, no software changes are necessary.

special section also facilitates software debugging. In addition to the address translation tables stored in main memory, the MMU has an on-chip translation buffer that holds the 32 most recently referenced virtual addresses and their translations. As will be explained, this can eliminate redundant translations of addresses and speed memory access. Special instructions are provided to control the MMU, and those instructions can be executed only when the CPU is in the supervisor mode. Attempting to execute an MMU instruction when the CPU is in the user mode results in a trap.

At any given time, either one or two address spaces can be supported by the 16082 MMU. In the single-space mode, each user shares a single virtual memory space of 16 megabytes with the operating system. They have common translation tables. In the dual-space mode, each user and the operating system have separate virtual memory spaces of 16 megabytes. The MMU circuitry does not limit the number of users.

As seen in Fig. 2, the MMU contains several registers. The MMU-status register (MSR) has an error-class field that holds the reason for the last memory error. Two page-table base pointers (PTB1, PTB2) on the 16082 point to the starting location of the translation tables in physical memory used for user space and supervisor space. Other registers control the debugger portion of the MMU.

Aborting facility

The MMU's most significant feature, however, is the aborting facility that supports the virtual memory operation system. To understand its importance, it is helpful to examine the execution of an instruction in a virtual memory environment. After fetching and decoding the instruction, the CPU sends the virtual addresses of the operands to the MMU. The MMU examines each address to determine if it resides in main memory. If so, it translates the virtual address to a real, or physical, address and sends it to the memory.

If the necessary data is not in main memory, however, the MMU sends a signal to abort to the CPU. The MMU will also abort the memory access if the CPU is trying to access a protected section of memory. At this point the CPU will stop executing the instruction and return any register that was altered by the instruction to its condition before the instruction started. It will then call the virtual memory operating system routine, initiating the memory page load. This routine will locate the needed data on the peripheral memory and load it into main memory, swapping unused data from main memory, if necesary, to make room. During the page loading, the CPU is free to perform another task if the operating system is arranged for multiprogramming.

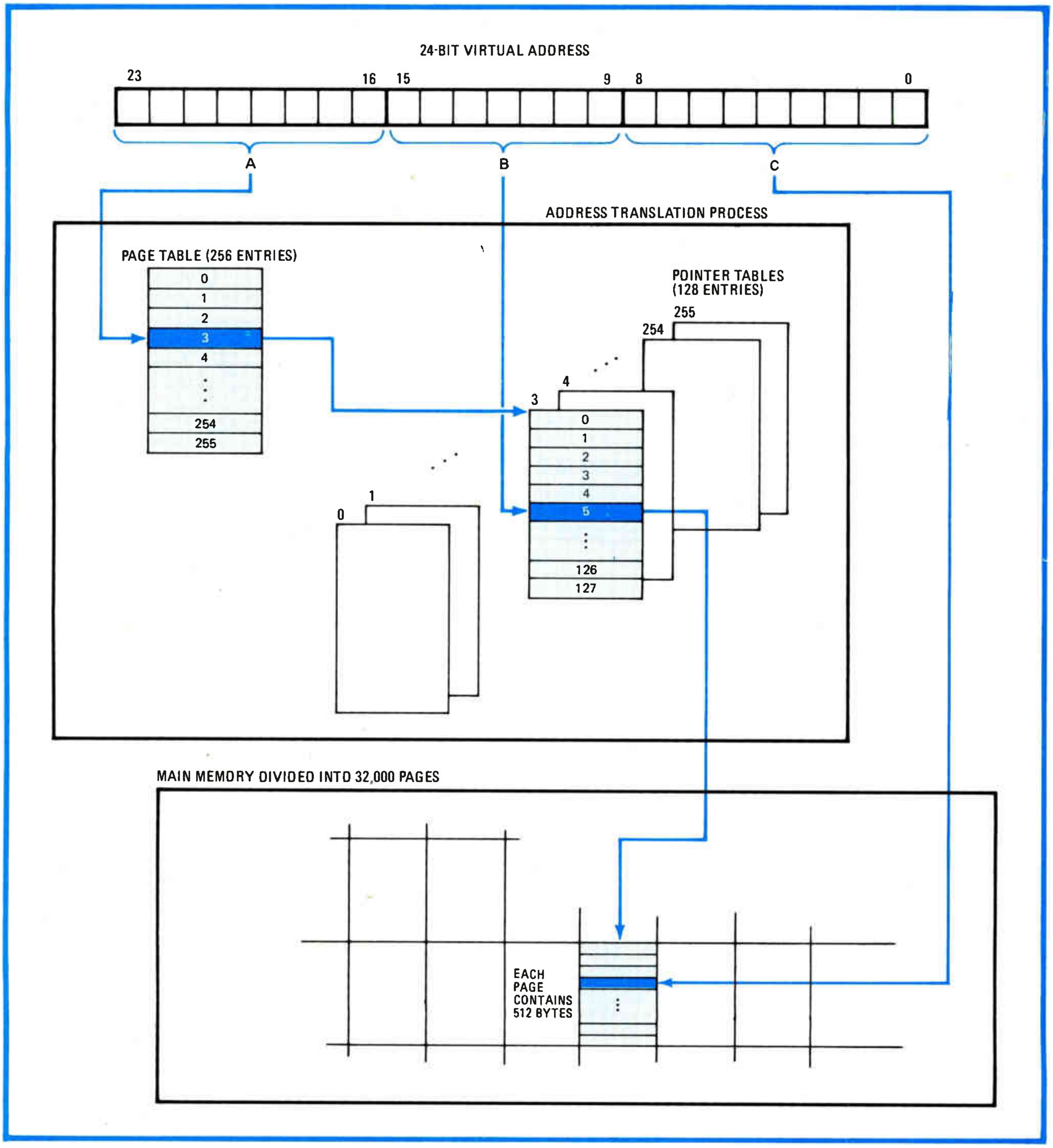
Of course, since the instructions themselves are treated as virtual memory, they may not be present in main memory when needed, resulting in the same signal to abort. Unlike regular interrupts, this signal cannot be held pending until the instruction is executed. The instruction must not be allowed to finish, since some of its operands are not available.

The CPU and MMU also ensure that the aborted instruction can be re-executed once the virtual memory management software provides the appropriate data. To accomplish this, when an abort occurs, the CPU is returned to the state it was in prior to the aborted instruction.

As a result of an abort, the program counter is automatically saved. The instruction will be retried when the page is loaded and the operating system performs a return-from-trap instruction. In addition, the condition codes in the processor's status register are affected by many instructions and therefore must be restored. Similarly, the stack pointer register, which is decremented or incremented when the top-of-stack addressing mode is used by an instruction, is restored. The program counter is normally incremented for the execution of the next instruction and must be decremented. Special hardware on the 16032 automatically restores these registers to their previous value.

Because the 16032 CPU instruction stream is pipelined, provisions must be made for the instructions in the pipeline when aborting takes place. The 16032 aborts only the instruction being executed, ignoring others.

Signals to abort generated while the instructions are



3. Virtual. The upper 8 bits (A) of the virtual address point to one of the 256-page table entries, which in turn points to one pointer table. The next 7 address bits (B) index an entry indicating a page in main memory. The last 9 bits (C), untranslated, locate a byte.

being prefetched are suspended until the instruction is about to be executed. This prevents instructions following certain program flow-control instructions, such as call, return, and jump, from generating an unnecessary abort state when they are not intended to be executed and may not reside in virtual memory at all.

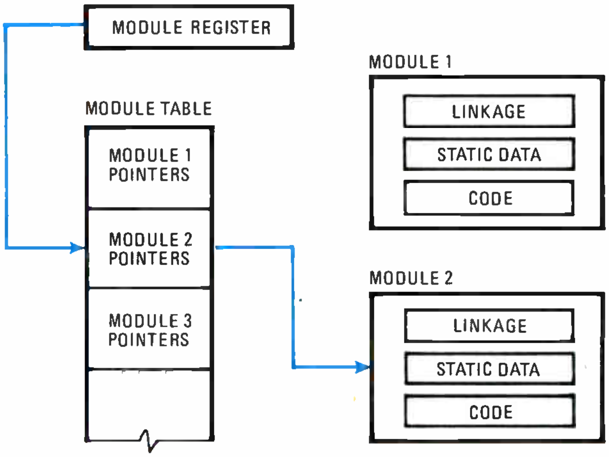
The string type of instruction, in particular, requires special handling during an abort. Obviously it is not desirable to have a long string instruction repeated from the beginning if an abort occurs somewhere in the string. The 16032 provides for the aborted instruction to be reexcuted from the point where the problem occurred.

Obviously the other major function of the MMU is to translate the virtual, or logical, address used by programmers and generated by the CPU into the real, or physical, address used to address the physical main memory. When the translation hardware finds that the virtual address is not in physical memory, it starts the abort process above.

For the purpose of virtual memory management, both

Modular software leaves room for growth

To allow software packages to be developed independently of other packages, without regard to their individual addressing, the NS16000 supports the concept of modular software design. This concept lets the software modules be stored in read-only memory and accessed as needed by the central processing unit.



To support this approach the NS16032 provides a static base register and a MOD register and sets up a module table in random-access main memory. The static base register points to scratchpad area in main memory that contains the data for the software module currently being run. The MOD register indicates the portion of the module table that points to the module being executed.

Each module has three components. The code component holds code for execution by the processor, and the static-data portion contains the local variable and data for that particular module. The linkage component holds the information required to link references from one module to another. The static data and linkage components typically reside in RAM, though the code component can be either RAM or ROM.

Because of the pointer construction of the module table and the provision for linkage references within each module, the modules can be added to the system independent of each other and relocated anywhere in the memory. The CPU will keep track of them in a way that is transparent to the programmer.

the logical and the physical address spaces are divided into 32,768 pages each with a fixed size of 512 bytes. It is the MMU's job to keep track of the logical addresses and their corresponding locations in physical memory. It does this by means of two sets of address translation tables, called page and pointer tables, stored in main memory.

The upper, or most significant, 15 bits (sections A and B) of the 24-bit virtual address represent the virtual address of a page and, once translated by the MMU, define a physical page of 512 bytes. The lower 9 bits are used to address a byte within this page and are not translated (Fig. 3).

Tables for translation

The translation is carried out by tables. The page table has 256 entries, each 32 bits wide. Thus, its total size is 1,024 bytes. Section A of the virtual address, which is 8 bits long, is used to index an entry of this table. The contents of this page-table entry, in turn, point to the beginning of one of 256 different pointer tables, which could also be stored in main memory. These pointer tables contain 128 32-bit entries each. Section B of the virtual address is used to index one of the pointer table entries, which points to the actual physical page.

Although at first glance this scheme appears to occupy a large portion of available memory space to maintain table entries, the overhead is actually very small. A maximum system of 16 megabytes of virtual memory will use one page table of 1,024 bytes plus 256 pointer tables of 512 bytes each, for a total of 132,096 bytes of mapping entries. But since a typical system would use a much smaller virtual memory size, it should be possible to reduce the amount of page table entries required. Also, the pointer tables may be paged in and out of main memory just like other parts of virtual memory.

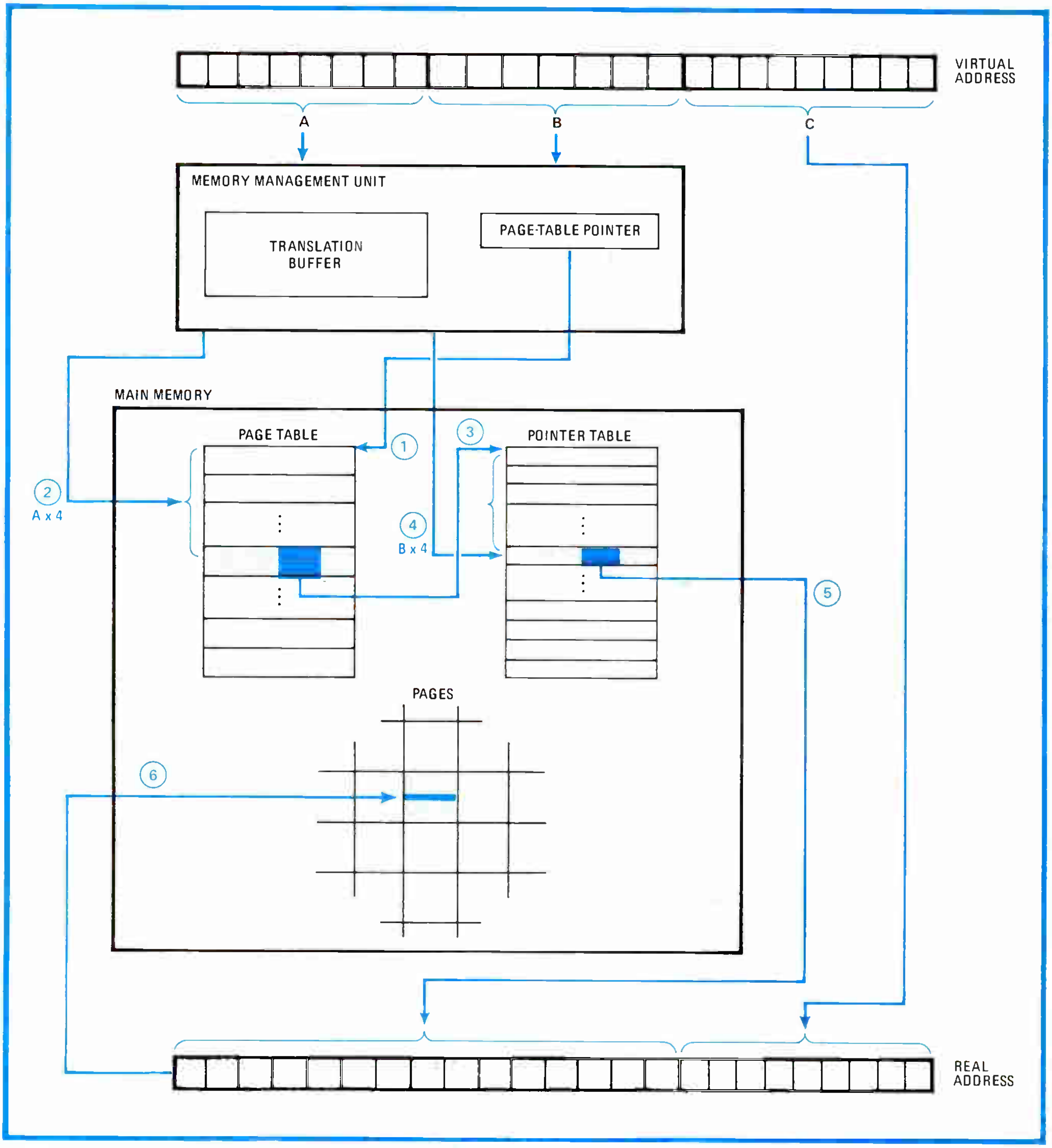
The translation process starts when the MMU receives the 24-bit virtual address from the CPU. The first thing the MMU does is compare the upper 15 bits of the virtual address with the 32 entries in its translation buffer. This associative memory contains the most recently accessed virtual addresses with their translated physical addresses. Thus, if the address is in this table—as it is expected to be 97% of the time—the physical address can be available in only one clock cycle.

If the address is not in the translation buffer, however, the MMU refers to the page and pointer tables in memory and updates the buffer. This process takes 16 clock cycles. While the MMU is performing the translation the CPU is kept inactive, since the MMU must have access to the external bus to access its translation tables in main memory.

The MMU's pointer base registers (PTB1 or PTB2) are controlled by the operating system. These registers contain the starting address of the page table in main memory. The MMU then takes the top 8 bits of the virtual address, multiplies that number by 4, and adds it to the starting address to point to one of the 256 page table entries (Fig. 4).

Each 32-bit page-table entry contains a 16-bit page-frame number as well as 8 flag bits and memory protection information. The ninth bit in the entry is ignored, and the uppermost 7 bits are reserved for future use. Among the flag bits is a valid bit that signals unused or invalid page entries that are not present in physical main memory.

As for the referenced bit, it is set whenever a corresponding page is referenced and is used by the operating system to help determine the least needed page. The modified bit is used to alert the operating system that a page has been modified, and therefore its copy in peripheral memory must be updated before that page can be removed from main memory. The other bits in the entry



4. MMU at work. If a virtual address is not in the MMU's translation buffer, it uses its pointer base register to locate the page table in main memory (1). Multiplying virtual address section A by 4 locates an entry that points to a pointer table (2 and 3). Multiplying section B by 4 locates the correct entry (4), 15 bits of which become the upper portion of the physical address (5). The lower 9 bits (C) are untranslated.

are used to hold memory protection information.

This 16-bit page frame number is then used by the MMU to locate one of the 256 pointer tables in main memory. The MMU takes the second 7 bits of the virtual address, multiplies that number by 4, and adds it to the page frame number to locate one of the 128 entries of the pointer table. Each entry on this table is similar to those on the page table. The MMU now takes the 15-bit page-frame number and appends it to the unchanged lower 9 bits of the virtual address to create the 24-bit physical address of the information in main memory.

Obviously, if an address is already in the translation buffer, the translation can be completed much more quickly. For this reason, a replacement algorithm stored in the MMU replaces addresses in the translation buffer that have not been recently used with recently accessed addresses. The translation buffer, by the way, is invisible to the user. □

Protected regulator has lowest dropout voltage

by Thomas Valone, *A-T-O Inc., Scott Aviation Division, Lancaster, N. Y.*
and Kelvin Shih, *General Motors Proving Ground, Milford, Mich.*

Providing an output of 5 volts at 10 milliamperes for an input of only 5.012 V, this regulator is ideal for use in many micropower applications, such as regulating the output of lithium batteries that drive low-power detection and recording instruments in the field. The circuit is useful in high-current situations also, as it can deliver up to 1 ampere at 5 V for an input of only 6.0 V. Short-circuit protection in this instance is provided by a single V-groove MOS field-effect transistor.

Contributing to the low-dropout characteristic of the circuit is the 2N6726 output transistor, which has a large junction area that allows a lower emitter-to-collector drop than most other devices, including Darlington arrangements. Thus the input-to-output voltage differential, 12 millivolts, is 6% that of one of the best low-dropout regulators reported to date.[1]

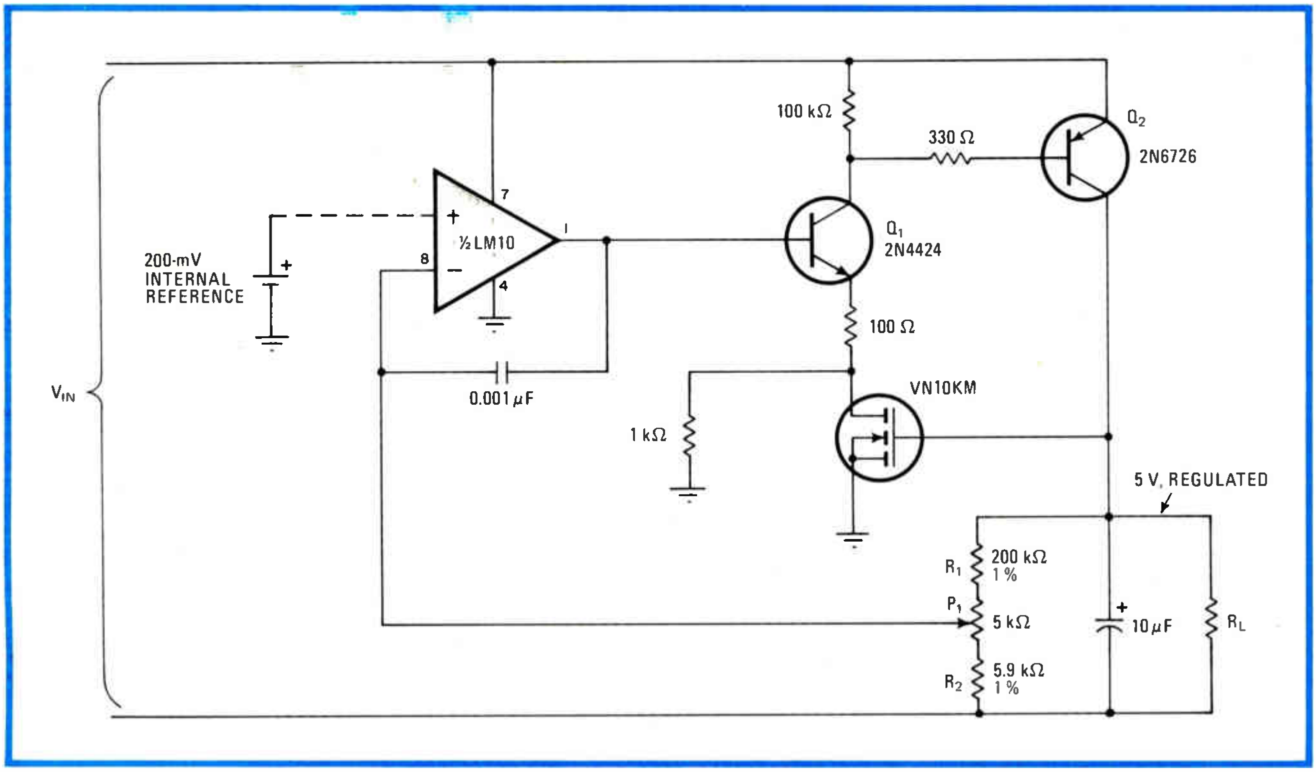
The input-to-output differential is only 350 mV at a load current of 500 mA. The 2N6726 is physically a small transistor but can dissipate 1 watt safely without a heat sink.

Short-circuit protection is provided by a Siliconix VN10KM, which presents a resistance of less than 10 ohms to the emitter circuit of the 2N4424 drive transistor under normal conditions. However, when the output is shorted to ground or excessive current is demanded, the drain-to-source resistance of the FET rises, safely shutting down the pass transistor. This characteristic can be used to advantage in adjustable current limiters, where the trip point is set by the input voltage. This method, incidentally, is more effective than any transistor foldback technique.

In operation, the LM10CH reference amplifier compares the voltage set by potentiometer P_1 to its internal 200-mV reference and through Q_1 acts to minimize voltage differences at the amplifier's input. With suitable selection of the component values in divider network R_1–R_2, the circuit will regulate over any voltage from 1 to 40 V. The operational-amplifier half of the LM10CH is available for other uses.

The load regulation is to within 0.3% for the range 0 to 100 mA and to within 1% for the range 100 mA to 1 A. The regulator's idle current is 320 μA. □

References
1. Kelvin Shih, "Micropower regulator has low dropout voltage," *Electronics*, April 12, 1979, p. 130.



Dropout limit. This low-power regulator, using output transistor operating in common-emitter configuration and having large junction area, can deliver 10 mA at 5 V for an input voltage only 12 mV higher and up to 1 A at 5 V for a 6-V input. Input-to-output voltage differential is only 650 mV at load currents of 750 mA. The V-MOS field-effect transistor provides short-circuit protection in such instances.

PSK modulator resolves phase shifts to 22.5°

by Noel Boutin
University of Sherbrooke, Quebec, Canada

Requiring little more hardware than the circuit proposed by Chawdhury and Das[1] and eliminating the software entirely, this phase-shift-keyed modulator offers an even more versatile and less expensive solution to sending binary data over long distances. One of its great advantages is that carrier phase shifts can be resolved to 16 bits—22.5°.

Only three low-cost chips and a means for generating four-input binary data are required, as shown. The carrier signal is first divided by 16 and applied to the CD4015 eight-stage shift register. Because the register is clocked by the carrier at a rate 16 times that of the signal to be shifted, a discrete eight-phase version of the carrier appears at the output of the register, each shifted by 360/16 = 22.5° from its neighboring stage. These signals are then introduced to the CD4051 multiplexer.

The first 3 bits of each of the modulating data inputs, A–D, address the CD4051 also. Thus any desired phase shift from 0° to 157.5° may be selected (see large table). The eight remaining values, from 180° to 337.5°, may be selected with the aid of the D input, which at the output of the last stage of the register inverts the phase of the signals that have already been generated.

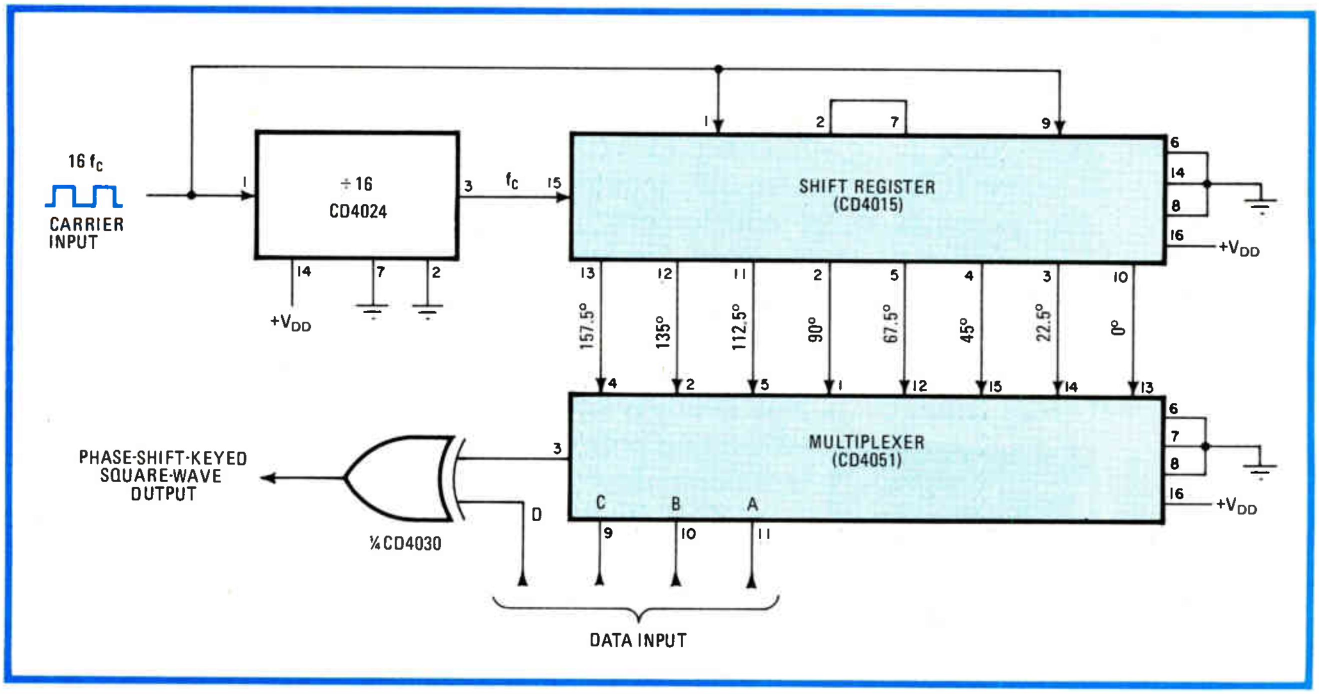
There may be instances where it is desirable to transmit fewer than 16 levels. The small table summarizes the A–D states required to achieve this. ☐

References
1. F. B. Chawdhury and J. Das, "8085 performs PSK modulation for data-line transmission," *Electronics*, Jan. 31, 1980, p. 108.

DATA				ϕ
D	C	B	A	
0	0	0	0	0°
0	0	0	1	22.5°
0	0	1	0	45°
0	0	1	1	67.5°
0	1	0	0	90°
0	1	0	1	112.5°
0	1	1	0	135°
0	1	1	1	157.5°
1	0	0	0	180°
1	0	0	1	202.5°
1	0	1	0	225°
1	0	1	1	247.5°
1	1	0	0	270°
1	1	0	1	292.5°
1	1	1	0	315°
1	1	1	1	337.5°

NUMBER OF PHASE LEVELS	A	B	C	D
2 ϕ	0	0	0	DATA
4 ϕ	0	0	DATA	DATA
8 ϕ	0	DATA	DATA	DATA
16 ϕ	DATA	DATA	DATA	DATA

Multiphase. Three-chip circuit performs PSK modulation on square-wave input, resolving carrier shifts to 22.5°. First three bits of modulating data inputs select shifts from 0° to 157.5°, with D input required for higher values. Truth tables summarize operation.



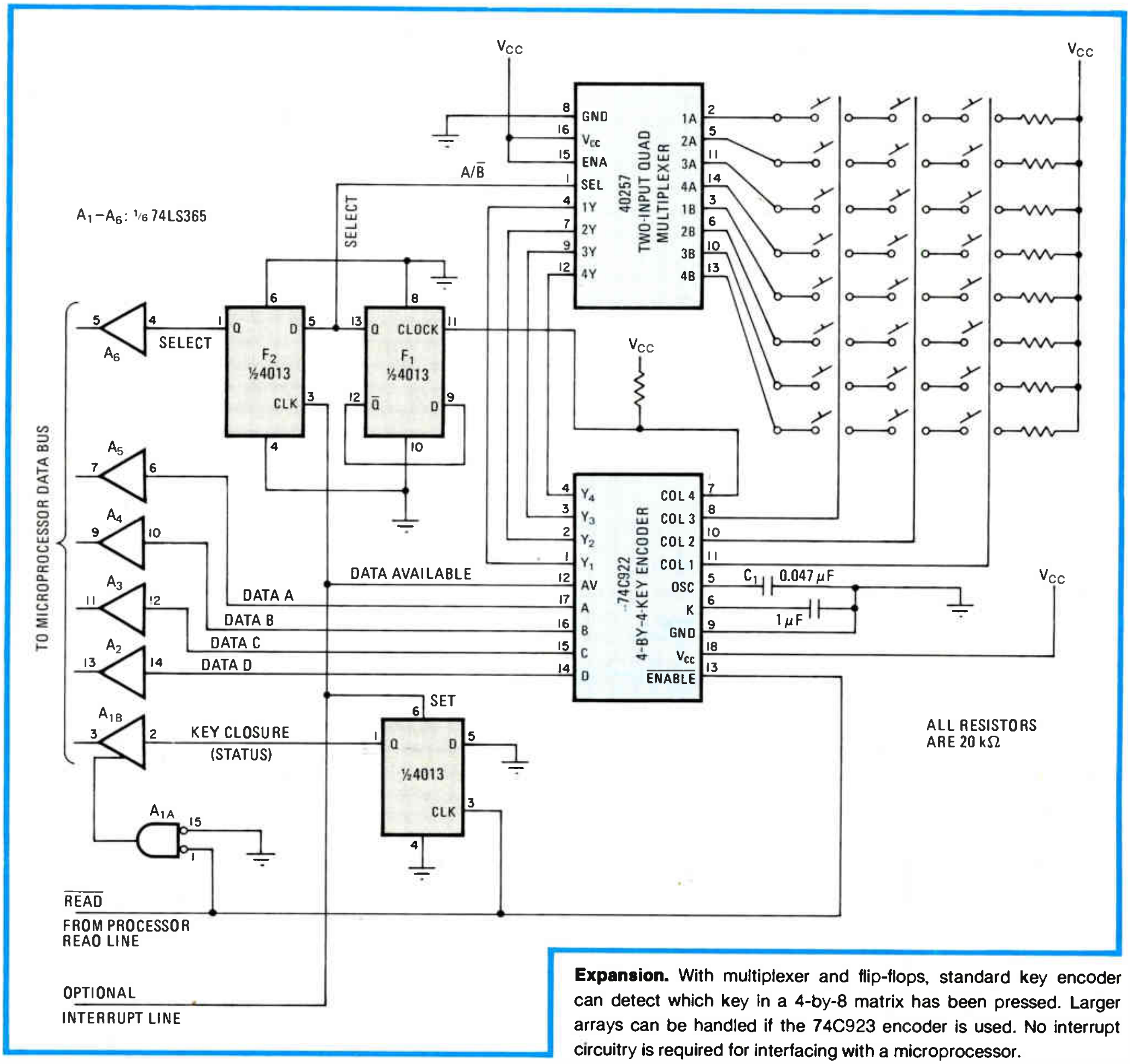
4-by-4–matrix chip encodes larger arrays

by James H. Nixon
Southwest Research Institute, San Antonio, Texas

With this circuit idea, the standard encoder for a 4-by-4–matrix keyboard can be made to handle arrays as large as 4 by 8. In fact, arrays as large as 4 by 10 can be readily accommodated if a 5-by-4-line encoder, such as Motorola's 74C923, is used. Interfacing with a microprocessor is easy and the generation of interrupts is not required.

As seen in the circuit example of a 3-by-8-line encoder, the 74C922 scans keyboard columns 1 through 4 (pins 7, 8, 10, and 11) at a rate set by its internal oscillator components and C_1. Each line is grounded in sequence until a key closure forces one of the row sense lines low, which in turn drives the data-available line high and halts the scanning process until the key is released. Meanwhile the appropriate input of the key encoder corresponding to the key pressed is brought high and the results of the row-column detection appear at the analog-to-digital outputs of the 74C922.

Each time the column 4 line is scanned, pin 7 of the key encoder moves high and clocks the 4013 flip-flop, F_1, causing the complementary-MOS 40257 data selector to switch between rows 1 to 4 and rows 5 to 8. The output from F_2 and A_6 thereby indicates which of the two row sets was accessed. The key closure line indicates if the data has been previously read and thus prevents redundant entries to the processor. □



Expansion. With multiplexer and flip-flops, standard key encoder can detect which key in a 4-by-8 matrix has been pressed. Larger arrays can be handled if the 74C923 encoder is used. No interrupt circuitry is required for interfacing with a microprocessor.

Protect data-acquisition systems with the right input isolation

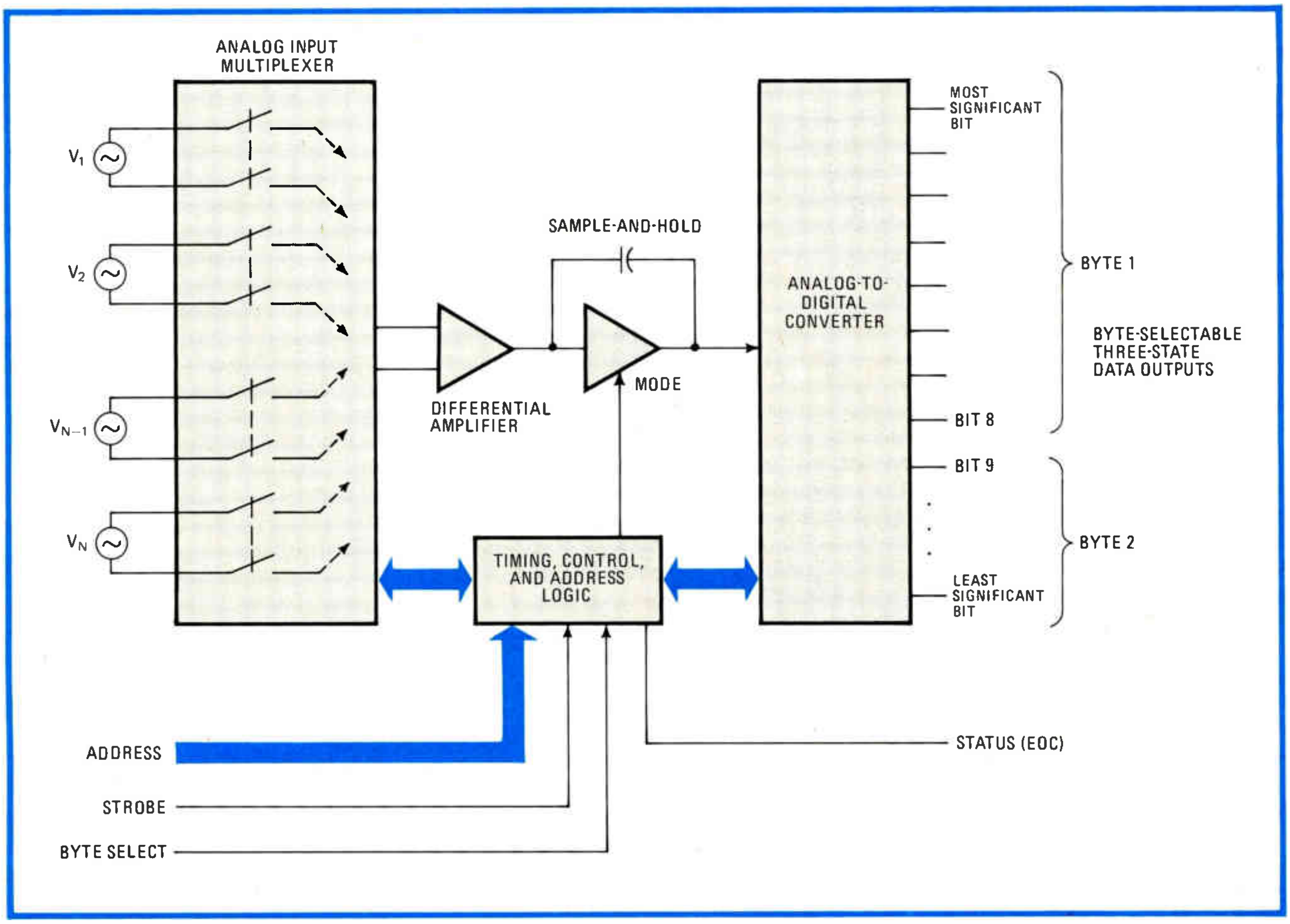
Of the many popular methods in use, the flying capacitor approach offers a clear advantage in its price-performance ratio

by Steven Connors, *Data Translation Inc., Natick, Mass.*

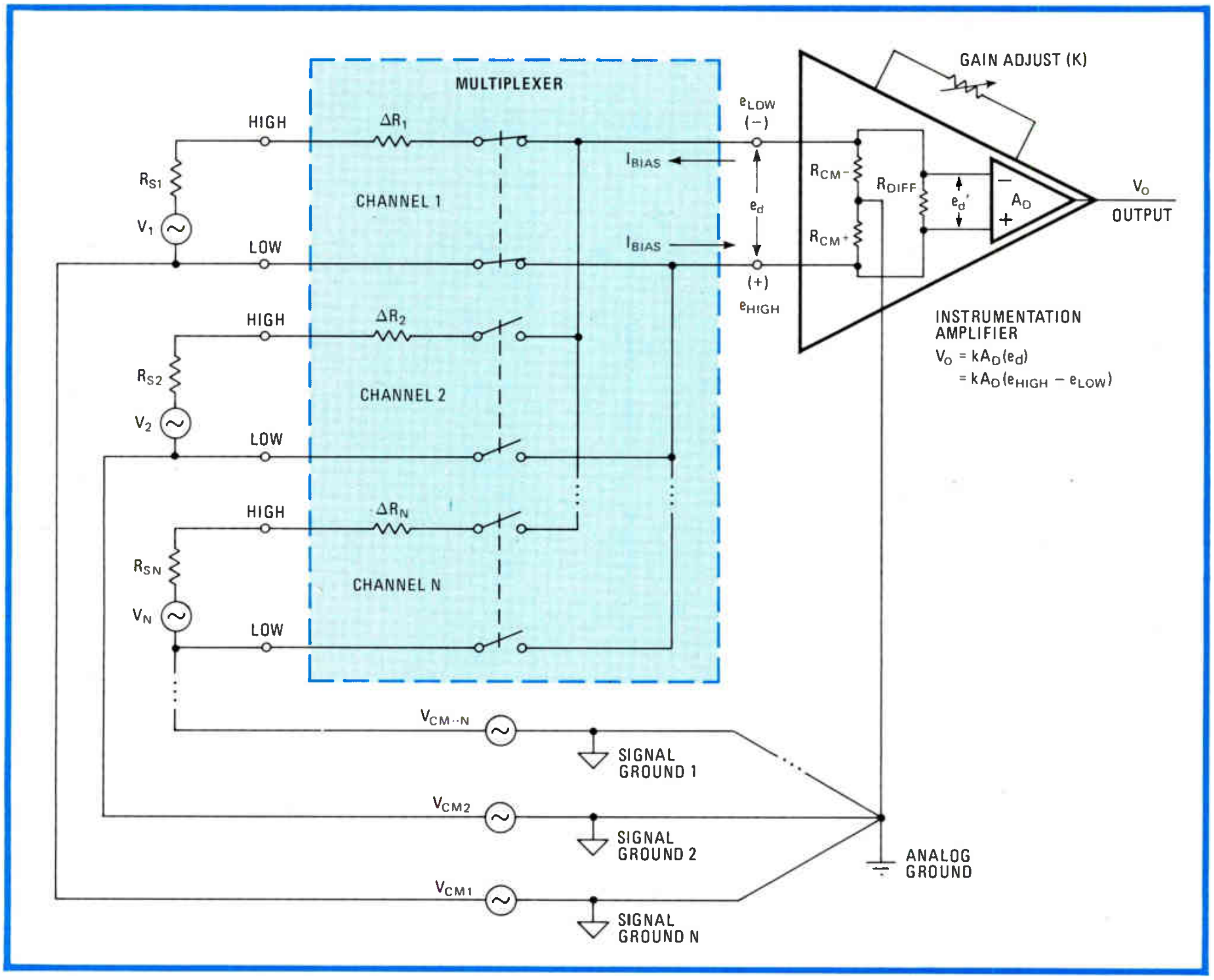
☐ Engineers have at their disposal an impressive arsenal of design options for isolating the inputs of data-acquisition systems, which depend heavily on such isolation in industrial-control operations. In these applications, common-mode voltages caused by improper circuit and/or power grounding can attain levels that cause nonisolated systems to malfunction or fail.

Isolated data-acquisition systems do, however, carry a higher per-channel price tag than nonisolated ones. Their increased circuit complexity also reduces the number of channels possible per printed-circuit card. Another penalty is that isolation reduces the data acquisition's speed or throughput rate. Fortunately, for the majority of transducers (like thermocouples and strain gages) that interface with industrial-control data-acquisition systems, the lower throughput rate does not seriously degrade system performance. This is because such transducers change slowly in response to the variables they sense.

Figure 1 illustrates a basic data-acquisition system. In low-speed systems, the output of the instrumentation amplifier may be fed directly to the analog-to-digital



1. Data acquisition. A typical data-acquisition system is basically a switched-input analog-to-digital converter that is vulnerable to common-mode voltages. For high-speed systems, the differential amplifier's output may be fed directly to the input of the a-d converter.



2. Multiplexer. The multiplexer of a data-acquisition system is typically configured with differential inputs. Input channels are selected digitally, by the multiplexer, through the use of solid-state switch arrays or relays. Selection can be sequential or random.

converter's inputs. For high-speed systems, however, this output is first fed to a sample-and-hold amplifier, where it is held until the a-d converter completes each of its digitizing cycles.

Their proximity to the system input makes the multiplexer and instrumentation amplifier particularly sensitive to any common-mode voltage. Even a low one can disable a nonisolated system, where power-supply voltage levels of 12 to 15 volts can be considered excessive.

As shown in Fig. 2, a system multiplexer is typically configured with differential inputs. It can be digitally instructed to select one of several input channels, randomly or sequentially, through the use of either solid-state switch arrays or various types of relays.

Unbalances can cause errors

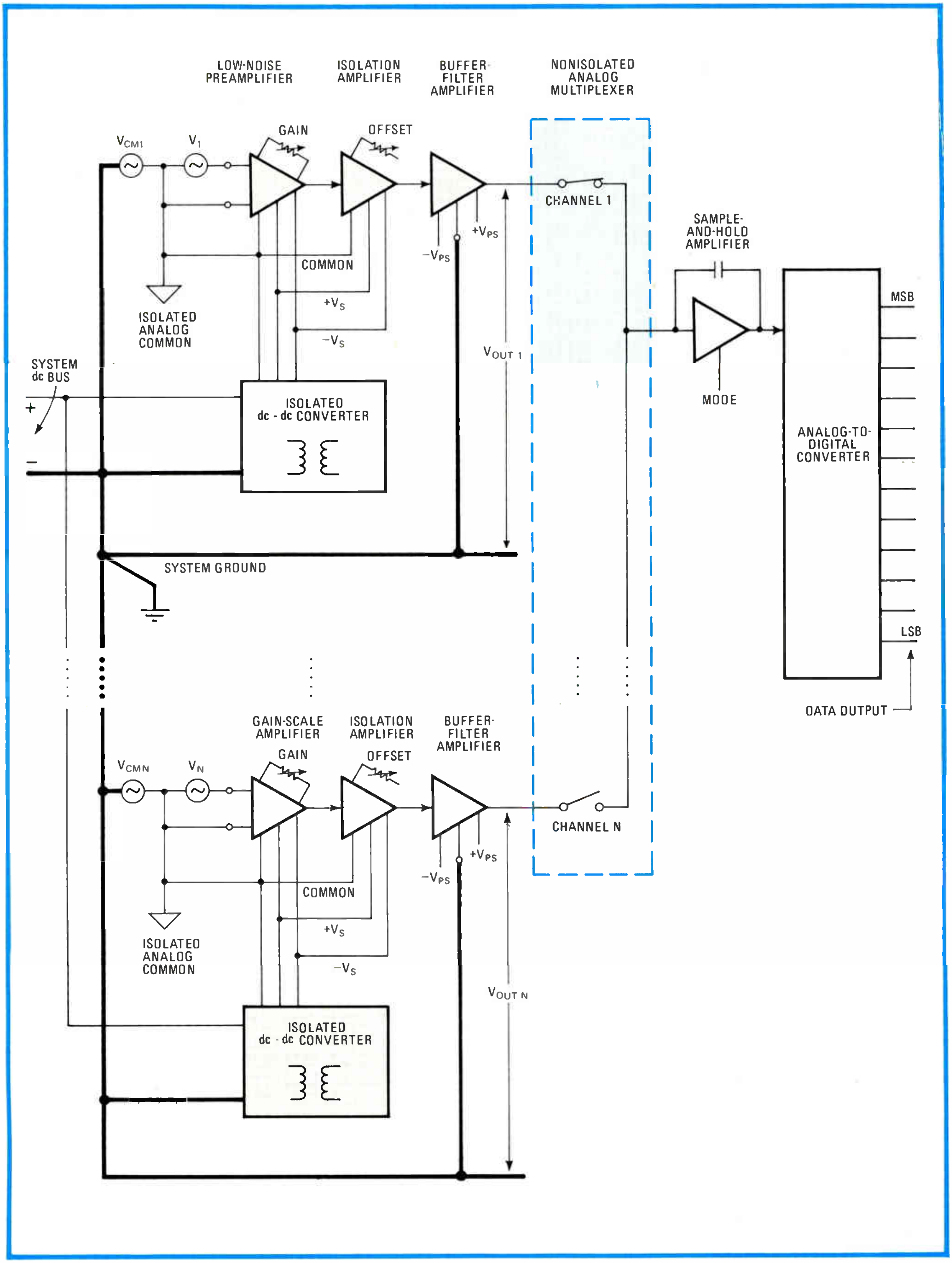
Because the common-mode rejection ratio (CMRR) of an instrumentation amplifier is influenced by several conditions, it is important to spell out all such conditions completely. For example, CMRR increases with the amplifier's closed-loop gain and decreases as frequency increases and with unbalances in its differential line-pair impedance.

Theoretically, an instrumentation amplifier can provide infinite CMRR at no response. This results when the inputs V_{low} and V_{high} (e_{low} and e_{high} in Fig. 2) are symmetrical and equal but opposite in polarity. In practice, however, these voltage signals traverse long multiplexed line pairs that are resistively unbalanced.

Varying attenuations

For each input channel, R_s is the source resistance of the remote input signal, and ΔR is the resistive unbalance of the differential switch pair's on-resistances. When the common-mode input resistances of the circuit of Fig. 2 become equal ($R_{CM+} = R_{CM-}$), the instrumentation amplifier's V_{high} common-mode input signal is attenuated more than that of the V_{low} path. An output is thus produced by the amplifier, and CMRR becomes less than infinite. CMRR can be further degraded with time-varying inputs such as those of stray capacitive unbalances. These can cause input attenuation to vary with frequency, often in an unpredictable manner.

For the circuit of Fig. 2, errors from input unbalances are not a serious problem since the amplifier's common-mode input resistance is several orders of magnitude



3. Premultiplexer isolation. In a basic data-acquisition system with premultiplexer isolation, each input channel is isolated by a differential isolation stage. One of its disadvantages in systems with many channels is that an equal number of isolation amplifiers is needed.

greater than source and channel resistances. The amplifier can thus serve as an impedance buffer to minimize source loading and resulting calibration errors. And with adjustable gain, it can control system symmetry.

Like all amplifiers, an instrumentation amplifier generates temperature-sensitive input bias currents. These currents flow through its signal terminals and the conductive path connecting them. Any resistive unbalance will transduce these currents to a differential-input offset voltage that varies with temperature. Thus all data-acquisition systems must strive for high input impedance, symmetry of inverted and noninverted instrumentation-amplifier gains, and balanced-impedance differential inputs.

There are two general isolation schemes for data-acquisition systems. Premultiplexer schemes can be implemented with either optical or transformer isolation. Postmultiplexer isolation is done by electromechanical or reed relays. The former general scheme differs from the latter in that an isolation amplifier is needed for each data-acquisition channel. (One well-known isolation type that will not be discussed in this article is that of optically isolated voltage-to-frequency and frequency-to-voltage converters, as it is not common in single-board data-acquisition applications).

In a basic premultiplexer-isolation data-acquisition system (Fig. 3), each input channel is isolated from high common-mode voltages by a differential isolation stage. Each stage consists of a low-noise gain-scaling preamplifier, an isolation amplifier with offset adjustments, and an isolated dc-dc converter for powering both amplifiers. A nonisolated buffer-filter amplifier translates the signal return reference to system ground, enhances normal-mode noise rejection, and unloads the isolation amplifier output by virtue of its high input impedance. Although the preamplifier and isolation amplifier are shown as separate elements in Fig. 3, in practice they may be combined as a single circuit element.

The topology and characteristics of the isolation stage determine the overall performance of the circuit in Fig. 3. A key element is the preamplifier, which has the greatest effect on system noise and drift. It should therefore exhibit extremely low noise and have low dc offset drift with time and temperature and a sufficiently high bandwidth for good frequency response. The low noise and drift characteristics are important, since any noise is amplified by subsequent gain stages. The preamplifier must also exhibit high common-mode rejection when hooked up as in Fig. 3.

Double duty

The isolation amplifier in Fig. 3 has a dual role: it not only isolates the signal from ground, but also provides adjustable gain and offset cancelation.

Depending on the specific isolation technique employed, the buffer-filter amplifier may be incorporated within the isolation amplifier or be a separate circuit element. Like the multiplexer and subsequent data-acquisition system components, this amplifier is nonisolated and is powered by nonisolated supplies.

The isolated dc-dc converter powers the preamplifier and isolation amplifier while creating an analog input common that is well isolated from system ground. Thus the input-signal return reference is comparatively noise-free and does not have to contend with troublesome interference from system grounds.

Input-signal returns, particularly those at low levels, must be fed through an analog common line since they are prone to ground-noise problems in isolated or nonisolated circuits. The system-ground conductor, which conceivably could be miles long, often contains large voltage gradients. It can also carry large transient currents caused by digital circuitry and inductively activated control components such as electromechanical relays and solenoids. In addition, ground potential can differ by the full ac-line voltage between two widely separated locations, due to faulty grounding of the ac power line.

Optical isolation is relatively simple

Figure 4a illustrates a basic approach to optical isolation of an input stage to a multiplexer channel. Light-emitting diode CR2 transmits equal mounts of light to matched photodiodes CR1 and CR3. By circuit design, the LED's output is proportional to the differential input, voltage V_{input}. Negative-feedback coupling of CR2's light to CR3, via CR1, reinforces this proportionality.

Since CR1 and CR3 are closely matched and receive equal amounts of light, currents flowing through them are nearly identical in magnitude. This is expressed by the relationships:

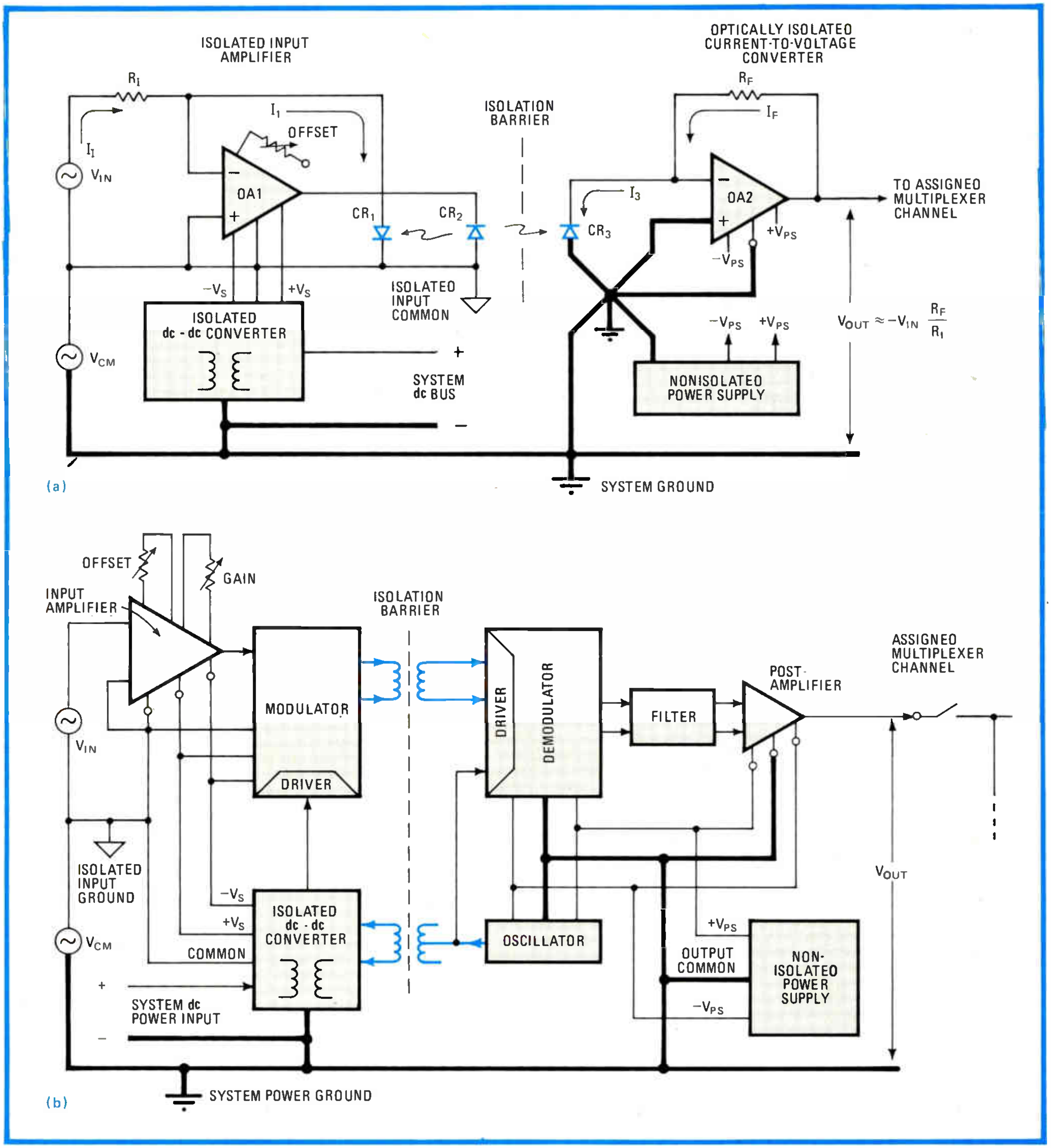
$$V_{input}/R_{input} = I_1 = I_3 - (V_{output}/R_{feedback}) - (R_{feedback}/R_{input})$$

Light coupled from CR2 to CR3 is thus transformed into current. Operational amp OA^2 then converts this current into a voltage, which is subsequently amplified to higher levels. The electrical isolation between CR2 and CR3 is known as an isolation barrier. The isolated dc-dc converter in Fig. 4a floats the input stage relative to system ground, for voltaic and galvanic isolation.

Optically coupled amplifiers located before the multiplexer are simple, low in cost, and small in size. They withstand common-mode pulsed inputs of 5 kilovolts and more, while boasting CMRR on the order of 100 decibels (at 60 hertz) and bandwidths ranging from 15 kilohertz up. They are also free of high-frequency modulation spikes and exhibit long-term stability (an average gain change of 0.075% over 10,000 hours of operation, as per one manufacturer's claim).

A disadvantage is poor gain linearity. It is typically within 0.05% at best, a performance unacceptable in 12-bit data-acquisition systems.

The use of an isolated input stage per multiplexer channel means that an isolated dc-dc converter must be used for each channel as well. This adds to the per-channel cost and can introduce the need for additional filtering of dc-dc noise spikes. Since each input amplifier in the circuit of Fig. 4a requires two adjustment potentiometers—one for zero and one for gain—an n-channel system would mean 2n potentiometers, which increase costs and are too time-consuming to be adjusted. Also the potentiometer resistance can change with time and temperature, and the more potentiometers used, the greater this drift problem becomes. Still another disadvantage is the need for isolated digital inputs for pro-



4. Optical isolation. A multiplexer's input stage may be optically isolated with this basic circuit (a). Photovoltaic and galvanic isolation of the input stage from ground is maintained by the dc-dc converter. A transformer can also be used for isolation (b).

gramming the optically coupled amplifier's gain by software. The isolated digital inputs are necessary to keep the input amplifier isolated and allow it to be gain-switched.

Transformer isolation

Fig. 4b shows a data-acquisition channel isolated by a transformer, before the multiplexer stage. Transformer isolation can be achieved by various types of synchronous modulation/demodulation techniques and by different inductive-coupling configurations. More complex and generally more costly than optically isolated designs, transformer-isolation designs offer a wide range of price, performance, and size options. For example, where small physical size is not important, transformer-coupled modular amplifiers can provide gain linearities to within 0.005%, suitable for 12-bit applications. Of course such modular amplifiers are typically 10 to 30 times larger than hybrid amplifiers.

Modular transformer-coupled amplifiers can achieve high CMRRs, from 110 to nearly 180 dB at 60 Hz. They can withstand greater than 5-kV pulsed inputs and have small-signal bandwidths extending to 2.5 kHz.

Hybrid transformer-coupled amplifiers are available with even better isolation and bandwidth ratings, but are limited in gain linearity to 12-bit operation. Such units can withstand 8-kV input pulses, feature 125-dB CMRRs (at 60 Hz), and have 35-kHz small-signal bandwidths. And they are, of course, considerably smaller than modular units.

Like optically coupled amplifiers, each transformer-coupled amplifier requires a zero and a gain potentiometer—again, a penalty of 2n potentiometers for an n-channel multiplexed system. Another similar disadvantage is the need for isolated digital inputs for software-programmable–gain applications. Though some transformer-coupled amplifiers contain an isolated converter, most do not. Supporting the isolation given by transformer coupling therefore requires one internal or external converter per isolated channel. In either case, this increases the per-channel cost.

A problem unique to transformer-coupled amplifier designs is the presence of harmonic-laden spikes caused by imperfect switching within the modulator and demodulator circuits. The high-frequency components of these spikes can couple into and disrupt nearby system circuits by conduction via parasitic reactive paths, or by electromagnetic radiation.

For many applications, the use of an individual isolation stage for each analog input channel can be a needless extravagance that only complicates system calibration and adds to system complexity. Figure 5 gives an example of postmultiplexer isolation in which a single input stage can gain-scale, isolate, and impedance-buffer many analog channels. Electromechanical relays multiplex the external signal sources to the isolated-amplifier inputs, by analog switching techniques.

Relays warrant consideration. Unlike solid-state multiplexing switches, they can withstand large common-mode voltages. In addition, even general-purpose relays exhibit low on-resistances, typically in the milliohm levels, that help minimize input calibration errors in low-signal-level precision applications.

Reduced costs

The circuit in Fig. 5 reduces per-channel cost, yet tolerates high common-mode voltage levels. Further, this configuration requires only one set of zero and gain adjustments and only one set of isolated logic for software-programmable gain-switching. Several basic disadvantages remain, however. For 12-bit systems, a costly, high-accuracy isolation amplifier is needed, which in turn requires isolated logic for programmable gain-switching. Since the response time of an electromechanical relay exceeds that of a solid-state analog switch, the maximum channel-selection rate for a relay-type multiplexer will fall far below that of a solid-state multiplexer. The time corresponding to the maximum rate must be long enough to guarantee that a relay can achieve a break-before-make transition when switching from the one channel to another. This time can range from tens of nanoseconds for a solid-state multiplexer to tens of milliseconds and more for a relay equivalent.

The lower speed of a relay-based multiplexer precludes its use in high-speed applications. Consequently, systems with relay multiplexers are used for acquiring slowly varying signals, such as those found in many geophysical and scientific applications. The a-d converter associated with relay multiplexing is usually a low-speed integrating type. Such a converter trades off speed for the ability to reject the power line frequency and its major harmonics, plus higher-frequency noise.

The multiplexer in Fig. 5 has a serious reliability problem. The finite input impedance of the isolated differential amplifier lets current flow through the contacts of a selected channel relay, which reduces relay contact life by orders of magnitude or more.

Yet another problem is one of random catastrophic failure. Parasitics from capacitors C_S and $C_{S'}$, which couple the multiplexer output rails to ground, are the culprits. The problem occurs this way: capacitors C_S and $C_{S'}$ are first charged to a very high common-mode voltage level (assume a level V_{cm1} for channel 1). If another channel is selected, with associated common-mode voltage V_{cm2} also very large and opposite in polarity to V_{cm1}, at the instant of channel selection, each relay contact of channel 2 (K2A and K2B) will experience a large voltage differential, made up of V_{CM1} and V_{CM2}. Such a differential voltage is likely to cause relay contact arcing and premature failure. The use of current-limiting resistors R_S and $R_{S'}$ reduces this problem somewhat but does not eliminate it.

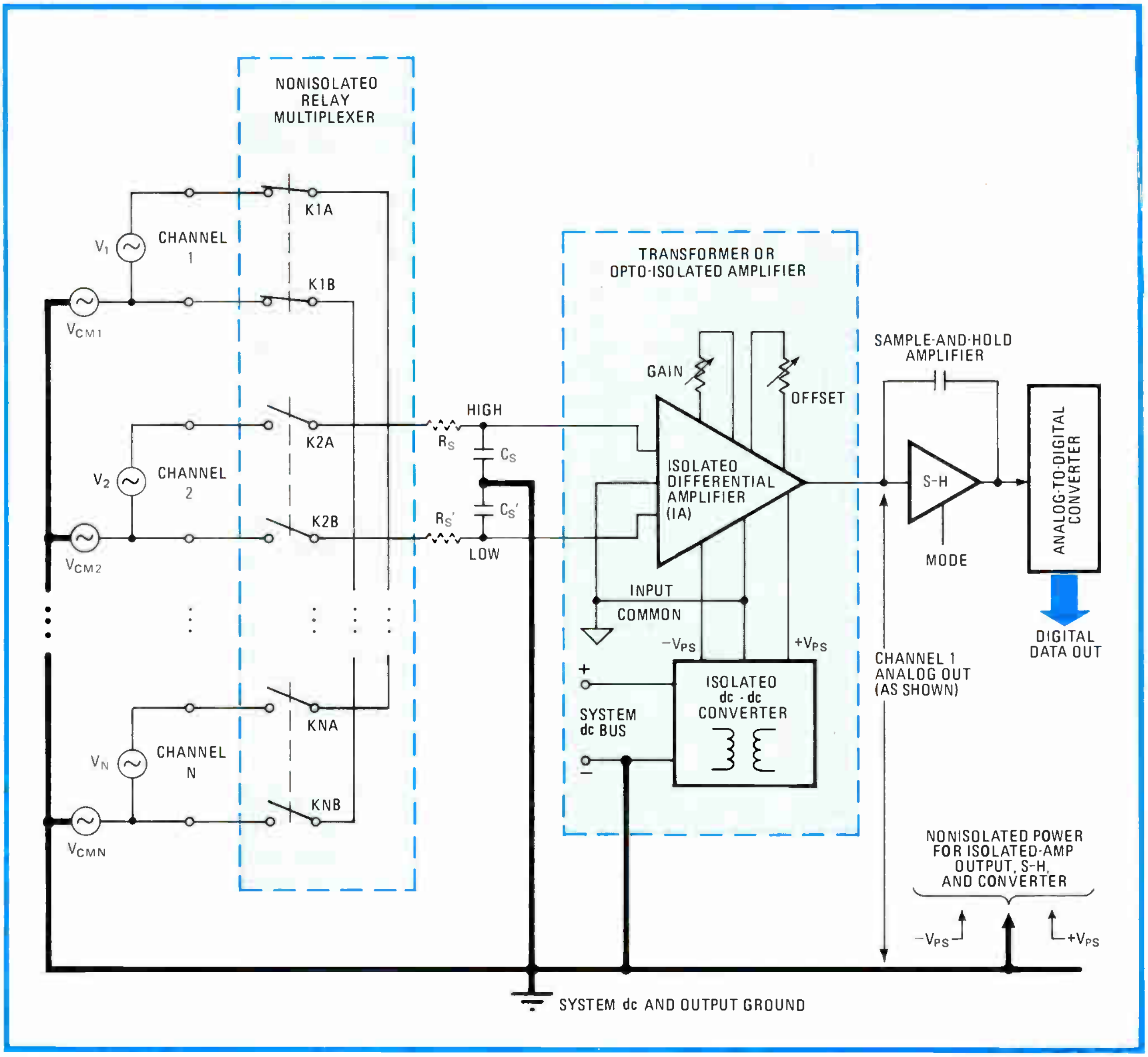
Optimum performance with the flying capacitor

Figure 6 illustrates the reed-relay flying-capacitor isolation technique that Data Translation uses in its family of low-signal-level, wide-dynamic-range, and high-isolation data-acquisition modules. Each channel (1 through n) contains its own storage capacitor and differential relay. A selected-channel relay first connects the channel storage capacitor across an external voltage to be measured. Later, the relay switches the charged capacitor across the amplifier input terminals. After being gain-scaled, the signal is digitized by the a-d converter.

The circuit in Fig. 6 performs the complete data-acquisition function, yet it requires but a single nonisolated amplifier and no dc-dc converters for channel isolation. This is because the reed-relay flying-capacitor multiplexer isolates high common-mode voltages while providing excellent CMRR and improved reliability through circuit simplification.

When commanded, each storage capacitor in Fig. 6 measures and holds an amount of charge corresponding to the true differential value of its assigned external voltage source. Because the common-mode voltage appears at both terminals of each capacitor, it contributes zero charge to the capacitor. In practice, external resistive and reactive unbalances limit CMRR to a value greater than 126 dB at 60 Hz, at a 1-kilohm source unbalance.

Connected as shown, the relays determine the common-mode voltage isolation level, typically about ±250 V. This level is less than that possible using optically coupled and transformer-coupled designs, but it is cer-



5. Relay isolation. Postmultiplexer isolation of a data-acquisition system can be achieved by the use of electromechanical relays. The use of relays eliminates the need for an isolation stage for each channel, a need common with premultiplexer optical and transformer isolation.

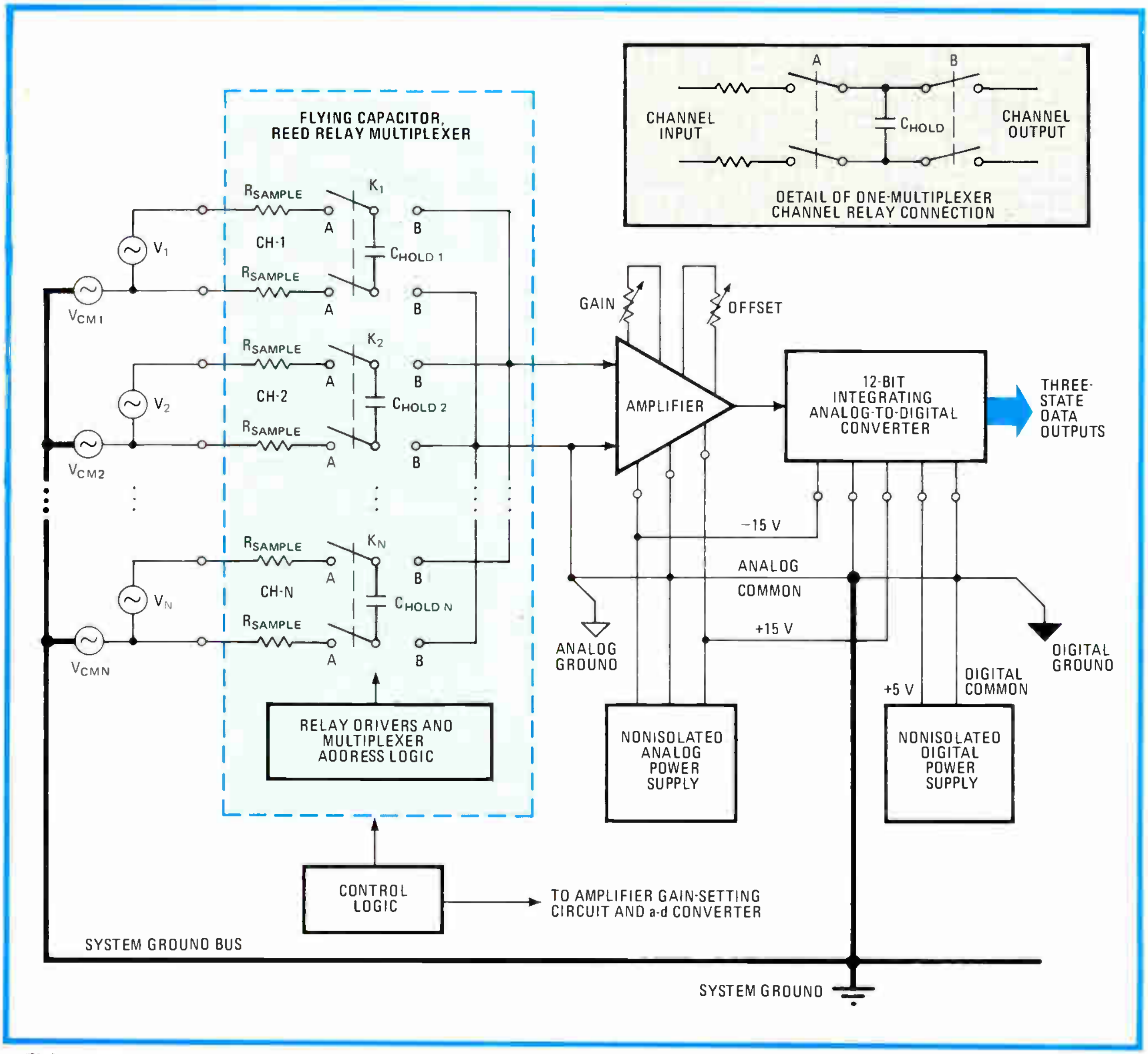
tainly adequate for a large number of industrial control and measurement applications.

The amplifier in Fig. 6 presents a high input impedance to the multiplexer and exhibits stable resistor-programmable gain, along with low noise and dc drift. Its input impedance is on the order of 100 megohms and the dc gain error is approximately 0.006% at a closed-loop gain of 1. Since the amplifier is not isolated, its gain-switching need not be isolated. Further, the system it is used in is expandable to as many as 1,024 channels, and the single input amplifier can serve them all.

Compared with premultiplexer isolation methods requiring one amplifier per channel, the reed-relay flying-capacitor approach reduces offset and gain adjustment times by a factor of 1,023. In addition, it eliminates the need for 1,023 amplifiers and 1,024 isolated dc-dc converters, improving reliability and reducing cost.

An integrating type of a-d converter is used in Fig. 6. This type of converter is inherently linear and moderate in price. Its sampling period can be set equal to the period of the power-line frequency for near-infinite rejection of 60-Hz and its harmonics. In addition, this normal-mode rejection increases at 6 dB per octave near the frequency at which the multiplexer's CMRR begins decreasing at the same rate. This tends to maintain the overall CMRR over a wider band of frequencies.

The normal-mode noise bandwidth of the system in Fig. 6 is limited at the input by the $R_{sample}C_{hold}$ networks in the multiplexer and within the system by the low-pass filter of the a-d converter. This limitation has its advantages, enabling the system to resolve and precisely digitize extremely low-level input signals. The multiplexer addressing logic of Fig. 6 contains provisions to prevent simultaneous selection of more than one channel under all operational conditions, including power-up and power-down. In addition, the A and B contact pairs assume



6. Flying capacitor. Optimum isolation of a data-acquisition system is achieved by the flying capacitor technique. Each input channel contains a storage capacitor and a differential relay. The relay charges and discharges the capacitor from input to output terminals.

an open state for logic faults and power loss conditions. Normally, either the A or B contacts are closed, but never both. For unselected channels, the A contacts are closed, allowing the external sources to charge their assigned channel capacitor.

The flying-capacitor approach eliminates yet another component, the sample-and-hold amplifier. Instead, the $R_{sample}C_{hold}$ input networks are proportioned to maintain a droop commensurate with 12-bit accuracy over the required sampling period. The R_{sample} resistors also serve as input current limiters, and ultimately as fuses, for certain fault conditions.

The reed-relay flying-capacitor multiplexer circuit provides excellent low-signal-level, multichannel performance (up to 1,024 channels) with simple, minimum-component circuitry at an extremely competitive price.

The circuit of Fig. 6 can also use mercury-wetted relays. But despite bounce-free operation and low on-resistance, these relays are sensitive and costly, requiring relatively large amounts of heat-generating drive power. Mercury solidification limits their low-temperature operation, and large size limits their packaging versatility.

More sophisticated

Modern reed relays are more sophisticated and reliable than their predecessors. The relays used in the data-acquisition modules incorporate oxygen-fired rhodium contacts attached to nickel-iron reeds, all in a glass-enclosed, dry-nitrogen atmosphere. For uniformity, the relays are assembled by automated machines to keep bimetallic voltage levels as close as possible to each other, from unit to unit. Typically, reed relays feature lifetimes of more than 100 million cycles. Compared with mercury-wetted relays, reed relays are smaller, lower in cost, are insensitive to position and require less drive power for reduced on-card thermal problems. □

Electro/80

☐ Eastern electronics' annual rite of spring—the Electro conference and exhibition—will fill Boston in April with engineers trying to prove that the show's theme, "Electronics Leads the Way," is in earnest. And leading the way for those engineers and Electro itself, measured by the number of technical sessions devoted to them, will be instrumentation and the microprocessor.

When Electro/80 opens on May 13 for its three-day run, Hynes Memorial Auditorium will be sold out and filled to its rafters with electronics companies and their representatives displaying products. The totals: more than 350 exhibitors occupying more than 730 booths. If there is indeed a recession abroad in the land, no economist could prove it from the business curve of Electro.

In 1976, when the show inaugurated its policy of alternating Boston with New York, Hynes had 265 exhibitors in 509 booths; by 1978, the respective numbers read 350 and 655. In fact, in the larger quarters available in New York last year, there were about 400 exhibitors, just 50 or so more than will be at Boston for Electro/80. And Boston's attendance is expected to equal New York's 30,000.

One significant trend in exhibitors is the increasing number of Japanese firms at Electro. From a low in 1977 of 8 booths occupied by 5 companies, the numbers have climbed steadily to 14 booths and 7 exhibitors in 1978, 15 booths and 8 companies in 1978, and a big jump to 24 and 13 respectively for Electro/80.

That is one side of the coin. The other, technical and professional presentations, is a good indicator of equipment rather than of business trends. With instrumentation and the use of the microprocessor the most popular topics, almost half the 34 sessions will be devoted to one or both of those subjects. In addition to discussions of technology, there will be a panel discussion on engineering education, as well as sessions on starting and operating a small high-technology business and on new ideas for engineering managers.

Single-chip microcomputers are the subject of session 29, "Total Solution on a Single Chip," and session 33, "Single Chip Microcomputers as System Components."

The former looks at the trend toward putting interface circuitry on chip along with the existing central processing unit and memory. The papers here, each one introducing a new device, new applications for existing ones, or both, come from companies like National Semiconductor, Texas Instruments, American Microsystems, Rockwell International, and Motorola.

One of the new single-chip microcomputers is Motorola Inc.'s MC6805R2. Built by its Austin, Texas, group from high-performance MOS, known as H-MOS, the 8-bit unit features, in addition to a CPU, an on-chip clock, 2 kilobytes of read-only memory, 64 bytes of random-access memory, 32 input/output lines, and, most importantly, an on-chip four-channel analog-to-digital converter. A block diagram of the converter is shown on page 144. It uses successive approximation and a four-input multiplexer, controlled through a status word, to select an input channel. A conversion takes about 30 machine cycles to complete.

Session 33 broaches single-chip microcomputers from a different angle: how they are being converted to act as slaves of master microprocessors (in addition to being able to stand alone). The resulting chips are generally referred to as peripheral interfaces or universal peripheral controllers. The first of these was Intel Corp.'s UPI-41A, which the Santa Clara, Calif., company will discuss in a paper along with other of its peripheral chips. Mostek Corp. of Carrollton, Texas, discusses its serial communications unit, the SCU 1, a 3870 preprogrammed for industry-type functions [*Electronics*, Dec. 7, 1978, p. 46]. Motorola unveils its own intelligent peripheral controller, the MC68120, which has a dual-port RAM and semaphores for synchronization.

High-end processors

High-performance microprocessors are the topic of session 19, "Advanced Architectures: Hardware and Software Considerations for New 16-Bit Microprocessors and Beyond," which attempts to match present software requirements with the latest hardware offerings. Here Intel, National, Motorola, and Advanced Micro Devices point to their architectures—the 8086, NSC16000, MC68000, and AmZ8000, respectively. Western Digital Corp. illustrates the advantages of Pascal pseudocode interpretation with its Microengine chip set.

Those attending session 19 might benefit most from the first paper, however, which is written by a software house that has examined the architectures of the 8086,

HOW THREE FLOATING-POINT SYSTEMS COMPARE

		Payne – Strecker	Kahan – Coonen – Stone	Fraley – Walther
Range	single	$[2^{-128}, 2^{127}]$	$[2^{-128}, 2^{128}]$	$[2^{-127}, 2^{127}]$
	double	$[2^{-1,024}, 2^{1,023}]$	$[2^{-1,022}, 2^{1,024}]$	$[2^{-1,023}, 2^{1,023}]$
	quadruple	$[2^{-16,384}, 2^{16,383}]$	–	$[2^{-16,383}, 2^{16,383}]$
Precision (bits)	single	24	24	24
	double	53	53	53
	quadruple	113	–	113
Exponent bias (bits)	single	128	127	not specified
	double	1,024	1,023	not specified
	quadruple	16,384	–	not specified
Operations		add, subtract, multiply, divide, compare, find the square root, and convert at all levels of precision		
Integer to floating-point conversions		conversions specified at all levels of precision	binary to decimal, remainder, round to integer	binary to decimal, extract function; conversions specified at all levels of precision
Arithmetic		real arithmetic rounded to level of precision specified		
Rounding	default	unbiased to nearest representable number		
	other	toward 0 toward +∞ toward −∞		
Reserved operands		sign bit = 1 exponent = 0	exponent all 0s exponent all 1s	two exponent fields (encoding not specified)
Exceptions	underflow	trap mandatory (default; replace with 0)	denormalize (trap optional)	replace with + UN (trap optional)
	overflow	trap mandatory (default; replace with ∞)	replace with ± ∞ (trap optional)	replace with ± OV (trap optional)
	division by 0	trap mandatory	replace with INVALID (NAN) (trap optional)	replace with ∞ (trap optional)
	square root of negative	trap mandatory	replace with INVALID (trap optional)	replace with special symbol ERR (trap optional)
	reserved operand	trap mandatory	use special arithmetic rules (trap optional)	use special arithmetic rules (trap optional)
	inexact	–	raised when result is rounded from computed answer	–
Compare with reserved operands		trap mandatory	invoke special rules of comparison	invoke special rules of comparison (different from KCS rules)
Extended registers		use double for single, quadruple for double	optional; single extended need not be the same as double in precision	optional

Z8000, and 68000 with an eye toward programming efficiency. The three 16-bit devices are compared in terms of system-call mechanisms, byte manipulation, 32-bit data handling, and the effects these features might have on software design. Conferences like Electro can use more of these unbiased sources.

Software for microcomputers surfaces again in session 31, which targets high-level language execution. The titles of the first three papers are also the names of the most popular structured high-level programming languages today: Pascal, C, and Ada. Pascal is covered by Softech Inc., which recently acquired exclusive rights to distribute the University of California at San Diego's version of the language, UCSD Pascal. The advantages of C are summarized by Whitesmiths Ltd. of New York, and Ada is outlined by Prof. Peter Wegner of Brown University, Providence, R. I.

Although Ada was based upon Pascal, Wegner spends much time discussing C and UNIX, a Bell Laboratories operating system written in C. "Ada usage will overtake Fortran usage by 1995," he says—a prediction of interest to the many who want to prepare for the impact of Ada, developed for the Department of Defense.

Like the choice of a high-level language, the standardization of floating-point mathematics—the subject of session 18—is controversial. The fact that the topic is very hot and all those involved are participating should make this session, titled "Floating Point Standards for Micros and Minis," one of the most interesting. Three proposals are currently being considered by the Institute of Electrical and Electronics Engineers. They are called the K-C-S, P-S, and F-W proposals, the acronyms standing for the names of the persons involved in the drafting of the proposal. Harold Stone (the "S" in K-C-S) moderates the session, and the table on page 143, which he prepared, compares the three proposals.

Though not specifically related to microprocessors, digital gate arrays have become a key means of consolidating random logic. They are the topic of session 22, which brings together manufacturers and users.

The new products announced here attest to the growing density and speed of these arrays. As one example, Fairchild Camera and Instrument Corp. of Mountain View, Calif., will, for the first time, publicly announce its F300 gate array, which has the equivalent of 2,000 emitter-coupled-logic gates. The F300 is expected to span a power-delay range from 400 picoseconds at 8 watts to 1.2 ns at 2 W.

Another new gate array is being unveiled by Fujitsu Microelectronics Inc. of Santa Clara, Calif. Its high-performance Schottky array has the equivalent of 500 gates. Meanwhile, Motorola describes new standard parts in its line of ECL Macrocell arrays. The new entries, called the M10900 family, include an 8-bit arithmetic and logic unit, that can work in binary and binary-coded-decimal formats.

Microprocessors to depend on

As microprocessor- and microcomputer-based systems become more widely used, their reliability becomes more critical. One of the more versatile of the devices to focus on that aspect is Advanced Micro Devices Inc.'s 2960, and it is being explained in session 25 by Warren Miller, senior applications engineer at the Sunnyvale, Calif., company.

An error-correcting device, the 2960 can generate and then check a 7-bit error-checking code using a modified Hamming code that detects all single-, double- and triple-bit ones [*Electronics*, April 10, 1980, p. 38]. Although designed to operate with the 2900 family of bit-slice processors, the 2960 can be used with a variety of microprocessors, Miller notes.

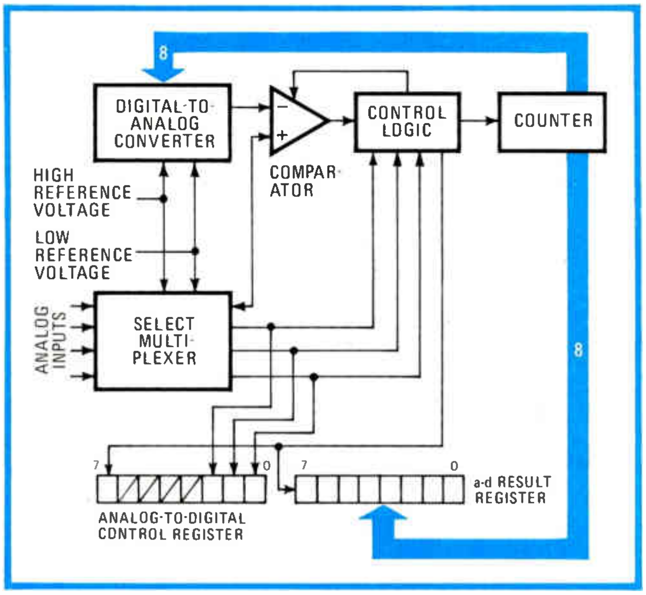
This single chip replaces the 20 to 30 medium-scale chips required to perform the function previously, he says. Furthermore, it can be cascaded to handle data fields either 32 or 64 bits long. To aid diagnosis of the system using the 2960, the syndrome bits indicating the failing bit are available.

Another interesting chip being discussed in that session is the IDM29110 microprogram controller from National Semiconductor Corp. of Santa Clara, Calif. Designed to control bit-slice processors, the 29110 features a 20-megahertz clock speed and instruction pipelining to speed operations and can support up to 8 kilobytes of control store. In its most elaborate pipelined mode, the 29110 can overlap access to the control store, generation of the next micro-instruction address, and execution of another instruction by the arithmetic and logic unit.

As storage densities of solid-state memory devices improve, it is increasingly attractive to employ more of these devices in computer systems. Session 10 will examine the trends in the memory devices that are leading candidates—RAMs and bubble memories.

Bulk storage goes solid-state

But despite the increasing use of memory, Sam Young, strategic marketing and applications manager at Mostek Corp., sees the rate of growth of the RAM demand slowing over the next few years. Such slowing is almost inevitable since, he notes, the industry shipped as



On-chip a-d converter. Motorola's latest version of its 6805 single-chip microcomputer sports four analog input channels. The a-d section of the chip, shown above, uses successive-approximation techniques and takes 30 machine cycles to complete a conversion.

many bits of MOS memory in 1980 as in all the preceding years put together. But even with the slower rate of growth, it still is a staggering 50% a year, which will see the industry shipping 15 million devices by 1984. Of that amount, the majority will still be 16-K devices. He assumes the learning curve for 64-K RAMs will be similar to the one for 16-K versions, resulting in a similar increase in shipments. Thus by 1984 the industry should be shipping some 80 million 64-K parts, he projects.

Because of this increasing use of memory devices, easier design techniques are needed, Young says. One attempt to ease engineering is Mostek's Bitwyde concept, which provides for pinout compatibility between its current parts and the newer 4532 32-K, 4164 64-K, and the 4538 128-K parts.

The popular floppies explored

This year the floppy-disk industry is expected to ship more than 2 million floppy-disk drives, and session 7 will examine the technical trends behind the popularity of this device. Improvements in floppy-disk controller chips will be discussed, along with advances in the drive itself and the magnetic media.

In one of the more interesting papers, Marshall Nathanson, Jeffre Bobicki, and Jack Taranto of Burroughs Corp.'s Peripheral Products group in Westlake Village, Calif., will explain how they designed a floppy-disk drive capable of storing 3 megabytes. Now available as the model MD122 flexible-disk drive, the device tripled the track densities of conventional floppy disks to 150 tracks per inch by reducing the core structure of the read/write head to one third its former size. In addition, improvements in the medium made recording densities of 7,000 bits per inch possible. Average access time is 100 milliseconds, about twice as fast as other floppy drives. A microprocessor-based controller, built around the Motorola 6802, handles interfacing, drive control, and diagnostics.

Arithmetic made easy

This year several companies are planning to introduce specialized single-chip arithmetic processors, making sophisticated arithmetic options much more affordable for systems designers and easier to program. Two of the makers will use Electro to detail their plans in session 14.

Krishna Rallapalli, manager of MOS microprocessor applications for Advanced Micro Devices, will discuss the Am9512 single-chip floating-point processor (see p. 153). Although it links onto an 8-bit external data bus, the Am9512 uses 17-bit internal data paths to perform single-precision arithmetic on 32-bit operands and double-precision arithmetic on 64-bit operands. Data formats and the floating-point arithmetic procedures are consistent with the proposed IEEE standard.

Chuck McMinn, 8086 product manager for Intel Corp., will provide details of the 8087 numeric data processor first unveiled at the International Solid State Circuits Conference last February [*Electronics*, Feb. 14, p. 144]. In addition to floating-point arithmetic on up to 80-bit binary numbers, the 8087 will do 2's complement arithmetic on 16-, 32-, or 64-bit numbers, convert to and from binary-coded-decimal format, and calculate square roots, logarithms, and trigonometric functions.

Catching the bus

The single session devoted to the IEEE-488 interface standard at last fall's Wescon [*Electronics*, Aug. 30, 1979, p. 170] attracted so much attention that three bus-related sessions have sprung up at Electro. They are spread out over the first day.

At 9 a.m., Jim Geisman of Tektronix Inc., Beaverton, Ore., will run the first session, number 3, "IEEE-488: User Fundamentals." According to Geisman, who also organized and headed the Wescon session, "There are many new users who can profit from the experience of others, and sophisticated users are uncovering some subtleties in the use of the bus that need to be aired at this meeting."

First to formally air those subtleties at Electro will be Dave Ricci, of Hewlett-Packard Co., Palo Alto, Calif., one of the authors of the original IEEE-488 standard. He will discuss the bus's impact on building automatic test systems for the laboratory and the production floor. Although the bus has reduced most of the process to a few simple steps, Ricci points out that "the relative simplicity with which a system can be designed and put together can lull the first-time venturer into ATS into a false sense of accomplishment." To prevent that, Ricci will take a careful look at programming 488 systems: test program planning, language selection, and various communications protocols.

An example of what can be done using a chip set to implement the 488 will be given by George Buchanan of Texas Instruments Ltd. of Bedford, England. Knowing the foibles of individual chip sets is important to designer and user alike; as Geisman points out, "widespread use of a few interface-bus chips means that semiconductor manufacturers will be setting a *de facto* standard."

For the present, however, "specifications among instrument manufacturers for IEEE-488 performance are as varied as the instruments themselves," according to Pat Donahoo of the John Fluke Manufacturing Co. of Mountlake Terrace, Wash. He will offer guidelines on what to look for in them and which ones are important to different classes of applications.

Maris Graube of Tektronix will wrap up the morning session with a brief look at the problems due to a lack of communications protocols for the bus. That will set the stage for his session 6, "IEEE-488 Case Histories: Progress and Problems," which Graube will preside over at noon.

Graube sees a "negative synergism phenomenon" with respect to IEEE-488 systems: "The sum of the problems of a system is greater than the sum of the problems of its component parts." But the problems are being solved, he points out, and his group of metrologists from the electronics community at large will present those solutions. Gordon Minns of AMS Corp., Lake Elms, Minn., will discuss the use of the bus in high-technology research and development; Ken Sangren, metrology consultant at Sperry Univac in St. Paul, Minn., will talk about his company's instrument selection and integration process; and Chuck Corbridge of Tektronix will discuss the bus's use in metrology and calibration.

The bus's growing impact on measurement instruments and systems raises the question of how much intelligence—in the form of user-programmable microprocessor—should reside in the instrument or in a system controller. Henriecus Koeman of Fluke will head the 3 p.m. session devoted to that topic, "Future of Intelligent Measurement Instruments and Systems."

Koeman sees three approaches evolving: programmable, self-contained instruments; single-board controllers interfaced with analog modules by a microcomputer bus; and IEEE-488 systems. The wide-ranging session will explore each approach, with Tom Rousseau of Tektronix discussing the intelligent oscilloscope [*Electronics*, Feb. 28, 1980, p. 39] and Martin Larson of Fluke covering the smart digital voltmeter [*Electronics*, March 13, 1980, p. 157].

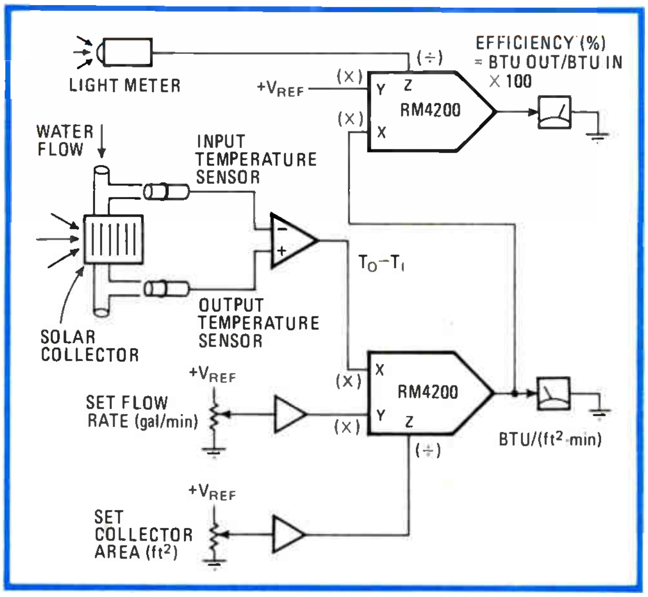
Development systems in the spotlight

The hottest software instrument, the microprocessor development system, will be covered in two sessions, one on Thursday morning and one in the afternoon. The sessions are similar to ones held at Wescon and will be run by the same people—Dave West of Millennium Systems Inc., Cupertino, Calif., and Jeff Krawitz of Solid State Scientific Inc., Montgomeryville, Pa., respectively. Although the topics are the same, the field is moving so fast that new bits of information have been added. For example, in the morning, in West's session 23, "Evaluation or Revolution to Next Generation Development Systems," John Marshall of HP will talk about the theory and practice of real-time emulation, and Mary Elmore of Intel will reveal her company's immediate MDS plans. In the afternoon, in session 27, "But How Does Your Microprocessor System Develop My System?" Krawitz will pit manufacturers of various systems against each other, which should generate some heat, particularly in the light of recent announcements.

Linking the largely inexpensive and straightforward digital world and the more costly and more complex analog world is the topic of session 4, "State-of-the-Art Data-Acquisition Systems." It was organized and is headed by Daniel Abenaim, business group manager for data-acquisition products and conversion, Analogic Corp., Wakefield, Mass. Abenaim will also deliver one of the session's papers, "Encroachment of Digital System Design Approaches into the Analog World." Despite the expansion of digital techniques into the analog world, he says, analog signal processing must still be contended with. The microprocessor has undoubtedly made things easier for systems designers, but a good understanding of data-acquisition system fundamentals is a must, Abenaim says.

In the same session, Donald Chase, product marketing manager for minicomputer-based products for Analogic, will deliver a paper on "Large Scale Digital Acquisition Problems." He will describe how such things as common-mode voltage and ratio and ground loops can greatly impair the accuracy of a system, no matter how large or small it is. A thorough understanding of the interactions of data-acquisition system components is the only way to get a handle on such problems. Tony Livingston, telecommunications marketing manager for Intel, will deliver "An LSI Approach to the Analog World." He will discuss various signal-processing applications for the firm's model 2920 analog-signal microprocessor, among them filtering, signal analysis, and conditioning.

L. Jefferson Gorin, product planning manager for



Solar computer. The output and efficiency of a solar collector can be measured with this handy circuit. Heart of the circuit are two analog multiplier-divider ICs. Both use logarithmic-antilogarithmic principles to perform simultaneous multiplications and divisions.

application systems products at Motorola in Mesa, Ariz., will concentrate on the system-level design of analog conversion to digital microcomputer. In his talk, "Analog I/O in Microprocessor-Based Systems," he will emphasize that, thanks to the microprocessor, conventional off-the-shelf converter components can now be used for high-performance requirements.

The many possible analog-to-digital and digital-to-analog converter technologies are covered in session 20, "A-d and D-a Converter Technology," organized and run by Al Sanchez, chief engineer for a-d and d-a converter products at Analogic. Sanchez will also provide an overview of converter technologies, the different conversion techniques possible, and some of their subtleties and idiosyncrocies. Doug Grant, microcircuits applications engineer for Analog Devices Semiconductor, Wilmington, Mass., tackles the world of "Monolithic Converters." First he will examine representatives of the "complete" integrated-circuit converters that depart from the simple building-block context such devices have traditionally been viewed in. Then he will try to show that modern monolithic converters can serve as building blocks for extremely complex system designs.

Hybrids and monolithics can co-exist

The hybrid side of the technology will be discussed by Richard Tatro, vice president of Micro Networks Corp., Worcester, Mass. He will explain that despite prevailing opinion, hybrid and monolithic converters compete with each other very little. Tatro will show that just as soon as a new monolithic converter is introduced to the market (and sometimes before), it is scooped up by hybrid converter makers and made into a still higher-performance hybrid converter.

The world of extremely high performance is of course dominated by modular a-d and d-a converters that make use of discrete components. Richard I. Powers, senior project engineer for Analogic, will discuss this side of converter technology in "A-d and D-a Discrete-Component Modules." He will show why such converters can still be found in many applications, where hybrid and monolithic designs cannot foot the performance bill.

Analog data processing flourishes

In the age of the digital computer, there is a tendency to rely on digital intelligence for information processing, a tendency that is often unnecessary, inefficient, and inadequate, notes Jeffrey R. Riskin, manager of applications engineering for Analog Devices Semiconductor, and chairman and organizer of session 12, "Applying the New Generation of Analog Computational ICs."

Kicking off this session will be Riskin's colleague Lew Counts, analog engineering manager, with "New Family of Monolithic Rms-to-dc Converters," in which he will describe his firm's AD536A and AD636 units. He will be followed by Joel Silverman, manager of applications engineering, Exar Integrated Systems Inc., Sunnyvale, Calif. Silverman's paper, "Applications of Multiplier/Modulator ICs in Analog Communication Systems," outlines applications for these.

James C. Schmoock, senior linear design engineer at Raytheon Co.'s Semiconductor division, Mountain View, Calif., will describe his firm's RC4200 IC multiplier-divider and how it can be used in a variety of applications, in "A Versatile Monolithic Analog Multiplier/Divider." One interesting application is in a solar-cell computer circuit.

Bridging analog and digital worlds

"Techniques for Bridging the Gap between Linear Applications and the Microcomputer" is the title of session 17, organized and headed by Robert L. Morrison, applications engineer for Burr-Brown Research Corp., Tucson, Ariz. In "Unusual Techniques for Difficult Analog Applications," Morrison reviews the changes that have taken place in the design and application of analog data converters and data-acquisition systems.

Jared E. Larsen, senior applications engineer with Synertek Systems Corp., Sunnyvale, Calif., shows how multitasking can be used to get more performance out of a microprocessor and microcomputer for analog data-acquisition applications. In his paper, "Multitasking in a Data Acquisition System," he shows three multitasking methods, ranging from a simple interrupt-driven approach to a more sophisticated multitasking executive scheme.

High-temperature electronics at new frontiers

Session 16, "Frontiers of High Temperature Electronics," is one of the most interesting Electro/80 sessions. It was organized and is presided over by Tony Veneruso, division supervisor for Sandia National Laboratories, Albuquerque, N. M. Veneruso will present an overview, "High Temperature Technology—Potential, Promise and Payoff." He will be followed by M. G. Reagan on "High Temperature Hybrid Thick Film Circuits"; Reagan is a senior production engineer with Teledyne Philbrick Co., Dedham, Mass.

John L. Prince of the department of electrical and computer engineering at Clemson University, Clemson, S. C., will give selected results of detailed investigations of the behavior of linear and digital ICs at up to 325°C, in "Characterization of Analog and Digital Commercial Integrated Circuits at High Temperature." A review of analog ICs for high-temperature operation is given by J. D. Beasom, manager of analog technology for Harris Semiconductor Corp., Melbourne, Fla. His paper, "High

Temperature Integrated Circuits," also discusses the firm's 200°C family of analog ICs and a Sandia-funded 300°C quad operational amplifier project.

As today's integrated circuits become faster and denser, they also become increasingly sensitive to static electricity, which is capable of zapping the thin dielectric layers of MOS devices. Static electricity particularly affects the handling of MOS-loaded boards. Many methods of on-chip protection have been developed but found to be of only limited value. This ongoing situation is why session 32, "Static Protection of High Density Circuit Components and Assemblies," is so critical to engineers whose specialty is production, assembly, and testing of boards loaded with expensive and static-sensitive ICs.

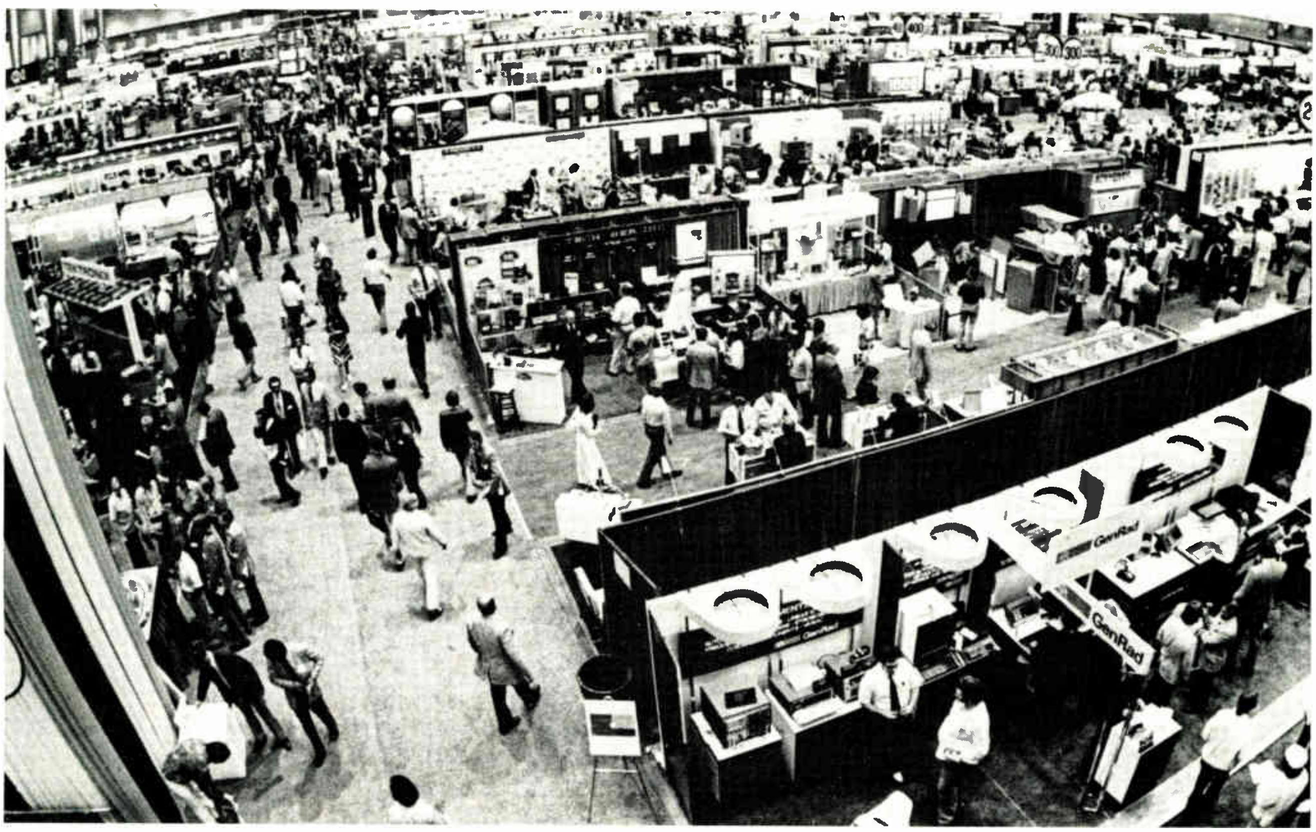
The most useful paper, "Fundamental Requirements for Static Protective Containers," is from 3M Co.'s Static Control Systems, St. Paul, Minn., and is by James Huntsman, Donald Yenni, and Gerald Mueller. It presents the required characteristics of static protective containers used not only for shipment and storage but also as temporary carriers for the transfer of components within a plant. Bags, tote boxes, and dual in-line package tubes are examined to characterize their protective nature against static voltage transients.

Five types of bags normally used to handle loaded printed-circuit boards are first examined: plain polyethylene, two types of antistatic coated polyethylene, two types of carbon-loaded bags, and two types of metal-laminated bags. A metal-laminate bag with a resistivity of 100 ohms per square was found to be superior to all other bags.

Similar tests with tote bags and DIP tubes made with a wide range of materials showed that the less the resistance around the container, the more effectively it protects its contents against static. The authors' figures show the average level of static protection afforded MOS devices by various carriers and confirm the high level of static protection provided by low-resistivity materials.

Talk by the numbers

Electro/80 will not neglect communications—digital microwave, and electro-optic. Session 34, "Digital in the Telephone Subscriber Loop Plant," might be subtitled "How the New England Telephone Co. is incorporating digital technology into its system." No less than four of the five papers presented are given by its engineers and describe, as assistant vice president C. W. Anderson puts it, "the experience in exploiting available and announced digital technology and concepts in telephone loop plant applications."



The loop plant is the phone company's link with its business and residential customers, and the details of just how the new technology is meshed with existing analog technology—which, because of cost considerations, cannot be thrown away—makes especially interesting listening for telephone and communications systems engineers. Still, the strong emphasis on cost-effectiveness in the designs makes a good object lesson for all comers.

The only paper not from New England Telephone is given by John B. Gordon of GTE Service Corp. in Stamford, Conn. It is an overview of previous publications on digital network planning by GTE.

"Microwave engineers only" is perhaps too strong a statement to describe what will go on in session 2, "Integrated Solid State Microwave Amplifier Design," run by W. Allen Davis—he is with Raytheon Co. in Bedford, Mass.—but it is close. The five papers in this session range from a summary of the properties of microwave IC materials by Murray Olyphant of 3M Co. in Saint Paul, Minn., and a tutorial by Harlan Howe of Microwave Associates Inc. in Burlington, Mass., to a pair of design papers by Stan Mason of HP's San Jose, Calif., operation and Glenn Thoren of Cornell University in Ithaca, N. Y.

Mason's paper—"Low Noise GaAs FET Amplifier Design"—is a practical one that leads the listener by the nose through the real design of a state-of-the-art amplifier made with gallium arsenide field-effect transistors. The last 0.05 decibel is squeezed out of the first stage noise figure. The paper is a listenable summary of a five-class design originally discussed at the 1979 International Solid State Circuits Conference.

For Glenn R. Thoren, it is clear that millimeter-wave systems with Impatt amplifiers are the wave of the future—at least for certain air-to-air and cruise missile radiometry and for secure communications. "They are not only feasible but are actively being developed," he says. His paper in this session features a state-of-the-art chart for the 30-to-300-gigahertz range and tells how to do it with Impatt diodes.

Inside the light pipe

Fiber optics is the name of the game for today's new communications technology, and sessions 24 and 28 will give the inside story of both components and data buses. Since fiber technology is making rapid inroads into computers, communication links, and almost every field of industrial process control, anyone involved with these areas should attend.

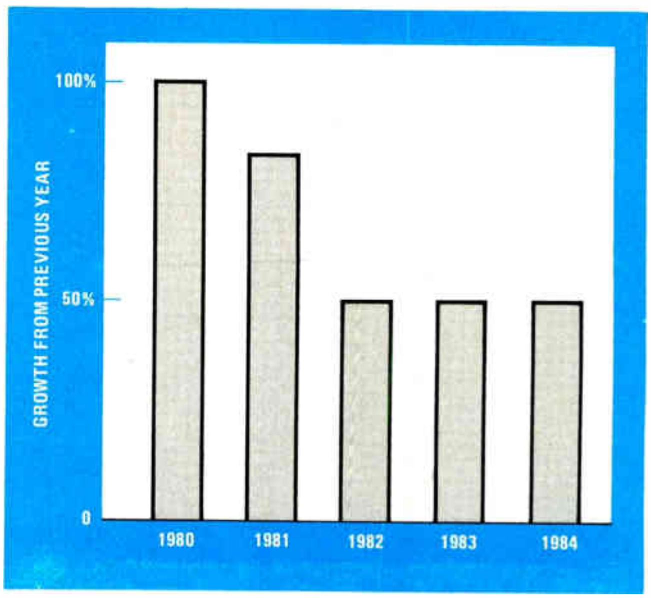
Session 24, headed by Harry Lockwood of GTE Laboratories in Waltham, Mass., surveys sources, detectors, and systems. The four papers are split evenly among GTE and RCA Corp.

Practical devices are discussed—fiber splicers, hermetically packaged lasers—as is the best way to detect received light. And perhaps most interesting, a genuine 44.7-megabit-per-second transmission system being used by telephone companies to transmit 672 digitized voice channels at once will be described.

Session 28 covers "Fiber Optic Data Buses Status and Applications." These buses are unique because, unlike wire data buses, they require no tuning and have no ground loop problems. According to chairman Al Bender of ITT Electro-Optical Products in Roanoke, Va., some of these data buses "are viable for near-term implementation." The five papers in his session—from Harris Corp.'s Government Communication Systems in Melbourne, Fla.; the Air Force Avionics Laboratory in Dayton, Ohio; IBM's Federal Systems division in Oswego, N. Y.; and two from Bender's Roanoke operation—represent the latest in this most promising field. As Bender puts it, "Fiber data buses have incredible capabilities." He says that "1 megabit per second is virtually off the shelf today, and 20 to 50 Mb/s can be had with custom design."

Finding a space in the crowd

Attacking the severe problem of spectrum crowding in the high- and ultrahigh-frequency region, session 5 covers "Recent Developments in Communications Receiver Design" that will help rf designers to secure receiving systems of sufficient dynamic range and selectivity to cope with today's band conditions. And orga-



Growth leveling off. While production of dynamic random-access memories will grow by 100% this year (in terms of the number of bits turned out), the figure will drop to about 80% next year and then level off to 50% the following three years, as shown in this chart.

nizer M. F. "Doug" DeMaw of the American Radio Relay League, one of the individuals instrumental nearly 10 years ago in changing industry's receiver design philosophy, has assembled three well-known experts to address the issues and provide the answers.

Ulrich L. Rohde, president of Rohde & Schwarz Inc., Fairfield, N. J., opens the session with his paper, "Recent Developments in Communications Receiver Design to Increase Dynamic Range," which deals with efforts to reduce noise in local oscillators and provides in-depth information on low-noise frequency synthesizers used in both transmitters and receivers. Rohde also introduces a new and simple noise blanker of high dynamic range that does not introduce in-band intermodulation distortion and is effective in eliminating the Russian over-the-horizon radar (Woodpecker) signals that have been heard throughout the hf bands in recent years.

Ed Oxner, senior engineer at Siliconix Inc., Santa Clara, Calif., then shows how the V-groove field-effect transistor lends itself to receiver applications in his paper "Large- and Small-Signal Applications for Field-Effect Transistors in Modern Communications Receivers." Pointing out the difference between the static and the dynamic transfer characteristic of an active device, Oxner then defines the subthreshold, square-law, and constant g_m regions of the curve in order to present the biasing criteria for linear service and to show that the V-MOS FET, although not the inherently linear device some have thought it to be, can provide greater range than bipolar transistors and even junction FETs.

Mike Elliot, senior project engineer at R. L. Drake Co., Miamisburg, Ohio, gives advice on the rules of the road and the design pitfalls to avoid in optimizing the strong-signal performance of a receiver with "The Real World of High-Performance Receiver Design." He emphasizes the necessity for designing a linear first mixer to reduce intermodulation products and low-noise oscillators to maintain dynamic range, as well as the importance of achieving selectivity in the early stages of the receiver and the need to equalize the gain distribution. He also discusses the relatively new method of up conversion used to achieve high image rejection.

The related session 8, "Current Developments and Applications in the Rf Power Device Field," also organized by DeMaw, examines the present state of radio-frequency device technology as it applies to the high-efficiency broadband transformers, bipolar transistors, and V-MOS power FETs that are used in transmitting applications. Jerry Sevick of Bell Laboratories, Murray Hill, N. J., first looks at the classic tradeoffs between tap ratio, network bandwidth, and efficiency in his paper, "Transmission Line Transformers with Low Transformation Ratios." But in a turnabout, he then covers the case of a tapped multiple-winding affair that will exhibit transformation ratios as small as 1.36:1 at efficiencies that are comparable with, and sometimes equal to that attained by, the standard two-winding 4:1 transformer.

Larry Leighton and Ed Oxner of Siliconix next discuss "Automatic Level Control for the V-MOS Rf Power Amplifier," showing that the use of such control without rf sampling is effective for wideband (30-to-90-MHz), high-power (100-W) service. They conclude that this technique can be utilized to achieve high-efficiency low-level amplitude modulation in power V-FETs.

Nathan Sokal, president of Design Automation Inc., Lexington, Mass., winds up the session by demystifying "Parasitic Oscillations in Solid-State Rf Power Amplifiers—Causes and Cures—Demystified." Sokal identifies the three basic forms a parasitic oscillation assumes and their causes by several phenomena, and he demonstrates that remedial measures for eliminating one type often will not be effective for eliminating the others. □

Seat of the commonwealth. Not only is Boston the major city in Massachusetts, but it is the capital of the Bay State. Here is the historic State House, one of the spots of interests to those attending Electro when they see the city between technical sessions.

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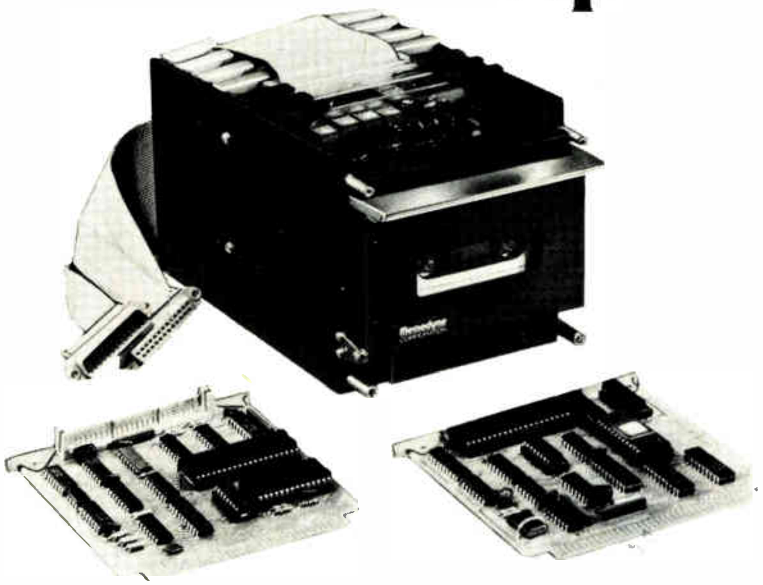

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Chips make fast math a snap for microprocessors

Fixed- and floating-point arithmetic processor performs trig and log functions, too; floating-point unit offers double precision

by Krishna Rallapalli and Joe Kroeger,* *Advanced Micro Devices Inc., Sunnyvale, Calif.*

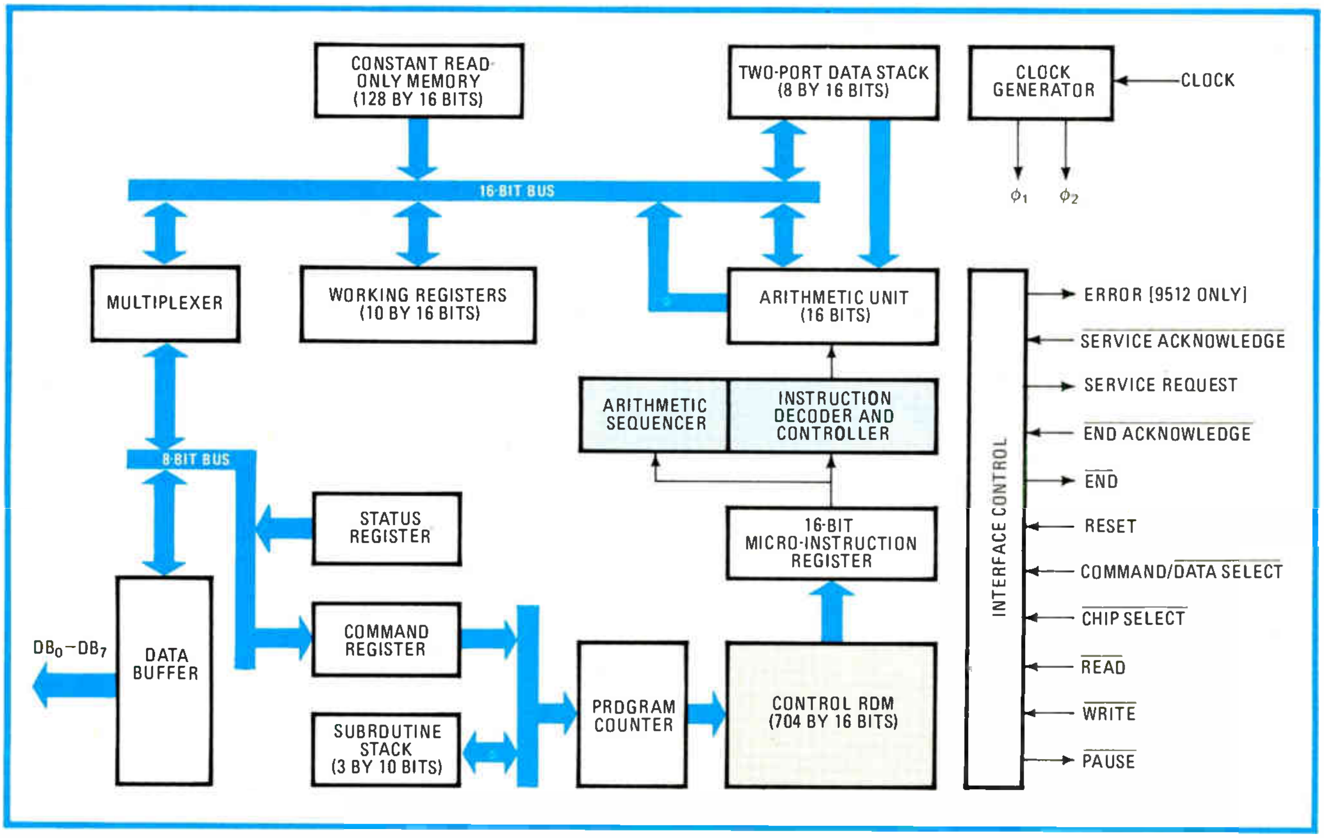
☐ Microprocessors need mathematical capabilities more than ever as they move increasingly into more complex control applications. For such real-time uses as machine-tool and process control and signal processing, they simply are not powerful enough, mathematically speaking, and minicomputers may be too expensive.

A large-scale integrated circuit, however, is quickly establishing itself as being up to these tasks. It has computational capabilities similar to those of scientific calculators, speed and economy comparable to those of microprocessors, and flexible interfacing as good as any microprocessor peripheral device's. The IC, which is second-sourced by Intel Corp., takes two forms: the Am9511A arithmetic-processing unit (APU) and the Am9512 floating-point processor unit (FPP).

The 9511 performs 16- and 32-bit fixed-point operations, as well as 32-bit floating-point arithmetic. In addition to the basic addition, subtraction, multiplication, and division, the chip performs many complex operations like calculating square roots, raising large numbers to a power, and evaluating logarithmic and trigonometric functions. Moreover, its versatility is enhanced by such convenience functions as conversion from fixed-point to floating-point and floating-point to fixed-point numbers.

The 9512 shares many of the 9511's attributes. The

*Now with International Microcircuits Inc., Santa Clara, Calif.



1. Math units. The Am9511A arithmetic-processing unit and the Am9512 floating-point processor share a basic architecture. The 9511 performs 16-bit fixed- and 32-bit fixed- and floating-point arithmetic, as well as trigonometric and logarithmic functions. The 9512 forgoes the fixed-point and special functions for single-precision (32 bits) and double-precision (64 bits) floating-point arithmetic.

TABLE 1: THE 9511's COMMANDS

Mnemonic	Execution cycles	Description
16-BIT FIXED-POINT OPERATIONS		
SADD	16–18	add contents of TOS to that of NOS; place result in NOS; pop stack
SSUB	30–32	subtract contents of TOS from that of NOS; place result in NOS; pop stack
SMUL	84–94	multiply contents of NOS by that of TOS; place lower result in NOS; pop stack
SMUU	80–98	multiply contents of NOS by that of TOS; place upper result in NOS; pop stack
SDIV	84–94	divide contents of NOS by that of TOS; place result in NOS; pop stack
32-BIT FIXED-POINT OPERATIONS		
DADD	20–22	add contents of TOS to that of NOS; place result in NOS; pop stack
DSUB	38–40	subtract contents of TOS from that of NOS; place result in NOS; pop stack
DMUL	194–210	multiply contents of NOS by that of TOS; place lower result in NOS; pop stack
DMUU	182–218	multiply contents of NOS by that of TOS; place upper result in NOS; pop stack
DDIV	196–210	divide contents of NOS by that of TOS; place result in NOS; pop stack
32-BIT FLOATING-POINT PRIMARY OPERATIONS		
FADD	54–368	add contents of TOS to that of NOS; place result in NOS; pop stack
FSUB	70–370	subtract contents of TOS from that of NOS; place result in NOS; pop stack
FMUL	146–168	multiply contents of NOS by that of TOS; place result in NOS; pop stack
FDIV	154–184	divide contents of NOS by that of TOS; place result in NOS; pop stack
32-BIT FLOATING-POINT DERIVED OPERATIONS		
SQRT	782–870	calculate square root of contents of TOS; place result in TOS
SIN	3,796–4,808	calculate sine of contents of TOS; place result in TOS
COS	3,840–4,878	calculate cosine of contents of TOS; place result in TOS
TAN	4,894–5,886	calculate tangent of contents of TOS; place result in TOS
ASIN	6,230–7,938	calculate inverse sine of contents of TOS; place result in TOS
ACOS	6,304–8,284	calculate inverse cosine of contents of TOS; place result in TOS
ATAN	4,992–6,536	calculate inverse tangent of contents of TOS; place in TOS
LOG	4,474–7,132	calculate common logarithm of contents of TOS; place result in TOS
LN	4,298–6,956	calculate natural logarithm of contents of TOS; place result in TOS
EXP	3,794–4,878	raise e to the power represented by the contents in TOS; place result in TOS
PWR	8,290–12,032	raise contents of NOS to the power represented by the contents of TOS; place result in NOS; pop stack
DATA AND STACK MANIPULATION OPERATIONS		
NOP	4	no operation; clear or set service-request line (SVREQ)
FIXS FIXD	90–214 90–336	convert contents of TOS from floating point to fixed-point format
FLTS FLTD	62–156 56–342	convert contents of TOS from fixed-point to floating-point format
CHSS CHSD	22–24 26–28	change sign of fixed-point operand in TOS
CHSF	16–20	change sign of floating-point operand in TOS
PTOS PTOD PTOF	16 20 20	push stack; duplicate contents of NOS in TOS
POPS POPD POPF	10 12 12	pop stack; move contents of NOS to TOS; rotate contents of TOS to bottom
XCHS XCHD XCHF	18 26 26	exchange contents of TOS and NOS
PUPI	16	push floating-point constant π into TOS; move contents of TOS to NOS

NOTE: TOS = top-of-stack position; NOS = next-on-stack position.

main difference lies in its ability to perform 32-bit (single) and 64-bit (double) precision floating-point arithmetic according to the format proposed by the Institute of Electrical and Electronic Engineers. It does, however, sacrifice the ability to perform fixed-point and transcendental operations to achieve this precision. Operations of the 9511 are summarized in Table 1; Table 2 lists those for the 9512.

Both processors use an 8-bit bidirectional data bus to communicate with a host processor. In fact, since the two are so similar internally, the following discussion will center on the 9511 APU.

The architecture of the APU

The 9511 employs a stack-oriented microprogrammed architecture with 16-bit-wide data paths (Fig. 1). It receives one of its operands from the data stack, which is an 8-word-by-16-bit two-port memory with last-in, first-out (LIFO) operation. The second operand is supplied by the internal 16-bit bus. In addition, that bidirectional bus carries the output of the processor. Writing into the data stack always takes place over the bus, as does communication with working registers and the constant ROM—that portion of read-only memory providing the constants required to perform the mathematical and other operations.

Communication between the external world and the 9511 takes place on bidirectional input/output lines DB_0 through DB_7. Those lines connect to an internal 8-bit bus through interface and buffer circuitry. Multiplexing facilities allow bidirectional communication between the internal 8-bit and 16-bit buses. The 9511's status register and command register are also tied to the 8-bit bus.

Chip operations are dictated by the microprogram contained in the control ROM. The program counter, loaded from the command register, sequences the micro-program. Associated with the program counter is the subroutine stack, where return addresses are stored for the micro-subroutine calls. The micro-instruction register holds the micro-instruction currently being executed while access to the control ROM is made for the next micro-instruction; such a pipeline architecture greatly improves the 9511's speed. The instruction-decoding logic generates various internal control signals to operate the chip, and the arithmetic sequencer implements multiplication and division algorithms in hardware.

The interface control logic accepts external inputs and provides several handshake-related outputs to facilitate interfacing with microprocessors. The signal present at the clock input sets the master timing, and the clock-generator logic provides internal timing signals.

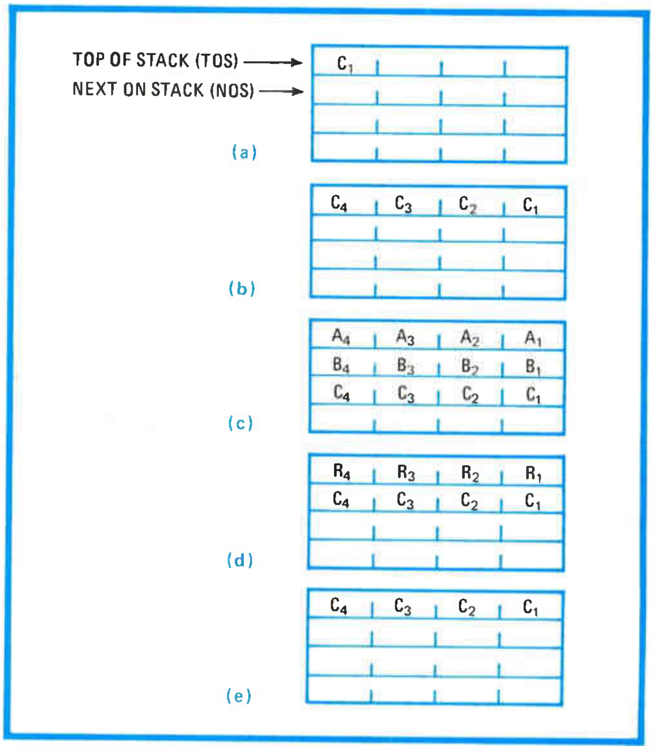
Data stack

The 9511 operates on the operands located in the LIFO data stack. Data always enters the stack 1 byte (8 bits) at a time, passing from the internal 8-bit bus to the internal 16-bit bus and then to the stack. Single-precision fixed-point operands are 2 bytes long; thus, the stack can accommodate eight such operands. Double-precision fixed-point—and all floating-point—operands are 4 bytes long, and four such values can be maintained in the stack.

TABLE 2: THE 9512's COMMANDS

Mnemonic	Description	Clock periods
SADD	add contents of TOS to that of NOS with single precision; place result in NOS; pop stack	58
SSUB	subtract contents of TOS to that of NOS with single precision; place result in NOS; pop stack	56
SMUL	multiply contents of NOS by that of TOS with single precision; place result in NOS; pop stack	198
SDIV	divide contents of NOS by that of TOS with single precision; place result in NOS; pop stack	228
CHSS	change sign of TOS single-precision operand	10
PTOS	push single-precision operand in TOS to NOS	16
POPS	pop single-precision operand from TOS; move contents of NOS to TOS	14
XCHS	exchange contents of TOS and NOS with single precision	26
CHSD	change sign of TOS double-precision operand	24
PTOD	push double-precision operand in TOS to NOS	40
POPD	pop double-precision operand from TOS; move contents of NOS to TOS	26
CLR	clear status register	4
DADD	add contents of TOS to that of NOS with double precision; place result in NOS; pop stack	578
DSUB	subtract contents of TOS from that of NOS with double precision; place result in NOS; pop stack	578
DMUL	multiply contents of NOS by that of TOS with double precision; place result in NOS; pop stack	1,748
DDIV	divide contents of NOS by that of TOS with double precision; place result in NOS; pop stack	4,560

NOTE: TOS = top-of-stack position; NOS = next-on-stack position.



2. Sequence. The 9511 and 9512 use a LIFO stack. A 32-bit operand, C, enters the top-of-stack (TOS) position a byte at a time (a) until it is filled (b). Operands B and A enter in a similar manner, pushing C further onto the stack (c). An operation on A and B places the result R in the TOS position, while C rises to the next-on-stack position (d). Removing the result pops C to the TOS position (e).

For those operations that need only one operand—like square-root calculation—the top-of-stack (TOS) position contains the operand. Operations requiring two operands—such as addition or subtraction—place the operands in the top-of-stack and next-on-stack (NOS) positions.

Push and pop

Operands are pushed onto the stack least significant byte first. Once the 9511 performs a specified operation, it pushes the result onto the stack; consequently, after completion of an operation, the top-of-stack position contains the result. The host processor pops the stack to get the result, the most significant byte of which is available first.

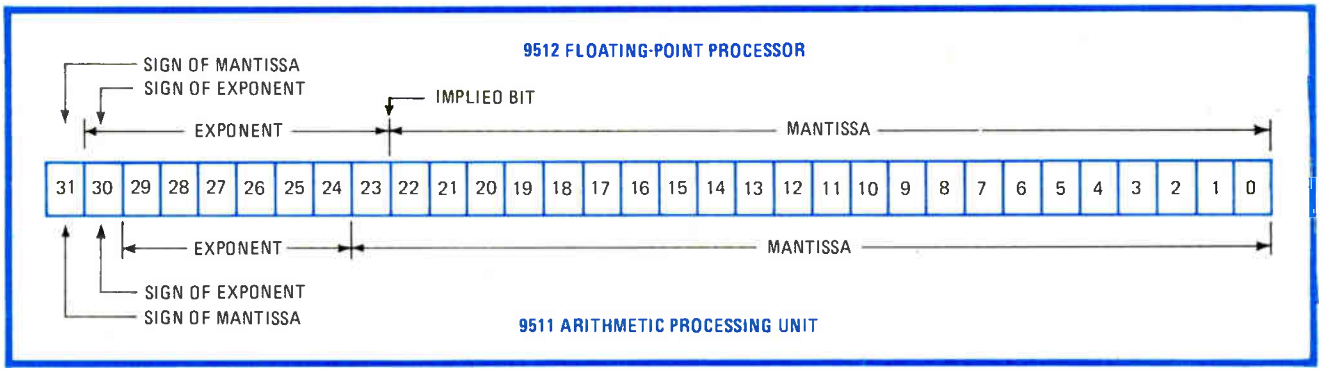
Figure 2 shows a typical data stack sequence for 16-bit operations. Figure 2a represents the stack after the entry of the least significant byte of operand C; Fig. 2b illustrates the stack contents after the entire 4 bytes of the operand have entered. When operands C, B, and A are fully entered, the stack appears as in Fig. 2c.

If a command is then issued—to add B to A, for example—the stack contents appear as in Fig. 2d, where R is the result of B+A. Finally, Fig. 2e shows the stack after the complete retrieval of R.

Note that data transfers into and out of the stack must always be in even multiples of bytes appropriate for the chosen operand format. Also, if the stack's capacity is exceeded, data will be lost from the bottom of the stack.

The fixed-point operands handled by the 9511 can be of 16-bit (single) or 32-bit (double) precision and are always treated as signed integers in 2's complement notation. The most significant bit is the sign of the operand, with a 1 denoting negative and a 0 denoting positive.

Figure 3 shows the format used for representing floating-point data, which is always 32 bits long: in the 9511



3. Formats. The formats for floating-point data, always 32 bits long, differ in the 9511 and 9512, since the latter performs only floating-point operations. The former uses a 24-bit mantissa and a 7-bit unbiased 2's complement exponent whose most significant bit is the sign. The 9512 has an 8-bit exponent and a 23-bit mantissa, to which it appends an implied bit 1 just beyond bit 22 for normalizing.

the least significant 24 bits represent the mantissa, or fraction; the next 6 bits are used for the exponent; the next bit represents the sign of the exponent; and the MSB is the sign of the mantissa. The exponent (including its sign bit) is a signed integer in 2's complement notation, whereas the mantissa (and its sign bit) is a signed fraction in sign-magnitude notation. The 9511 requires that all floating-point numbers be in a normalized form—that is, bit 23 must be a 1—except when representing the value zero, which is represented by 0s in all 32 bit positions.

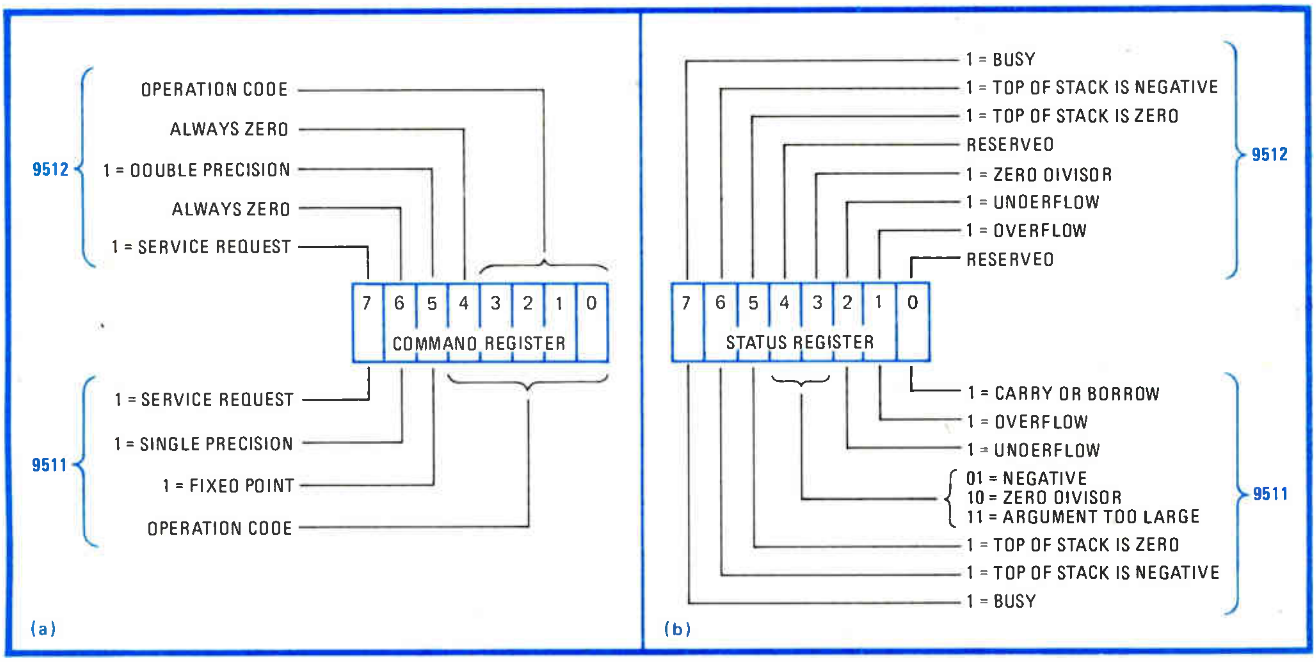
Since the 9512 deals only with floating-point operands, it handles them differently. Rather than requiring a 1 in the bit 23 position as the 9511 does for a normalized floating-point number, the 9512 assumes an implied 1 beyond the most significant bit of its mantissa (that is, between bit positions 22 and 23). The 9512 restores this implied bit internally before performing arithmetic. It then normalizes the result and strips the implied bit before returning the results to the stack. The binary point is between the implied bit and bit 22 of the mantissa. This approach allows the exponent to be expanded to a 7-bit argument. As a result, the 9512 has twice the range of the 9511, which handles negative and positive numbers from 2.7×10^{-20} to 9.2×10^{18}.

In a similar manner, the 9512's 64-bit floating-point quantity increases its range with an implied bit format. Bits 0 to 51 form the mantissa, bits 52 to 61 the exponent argument, bit 62 the sign of the exponent, and bit 63 the sign of the mantissa.

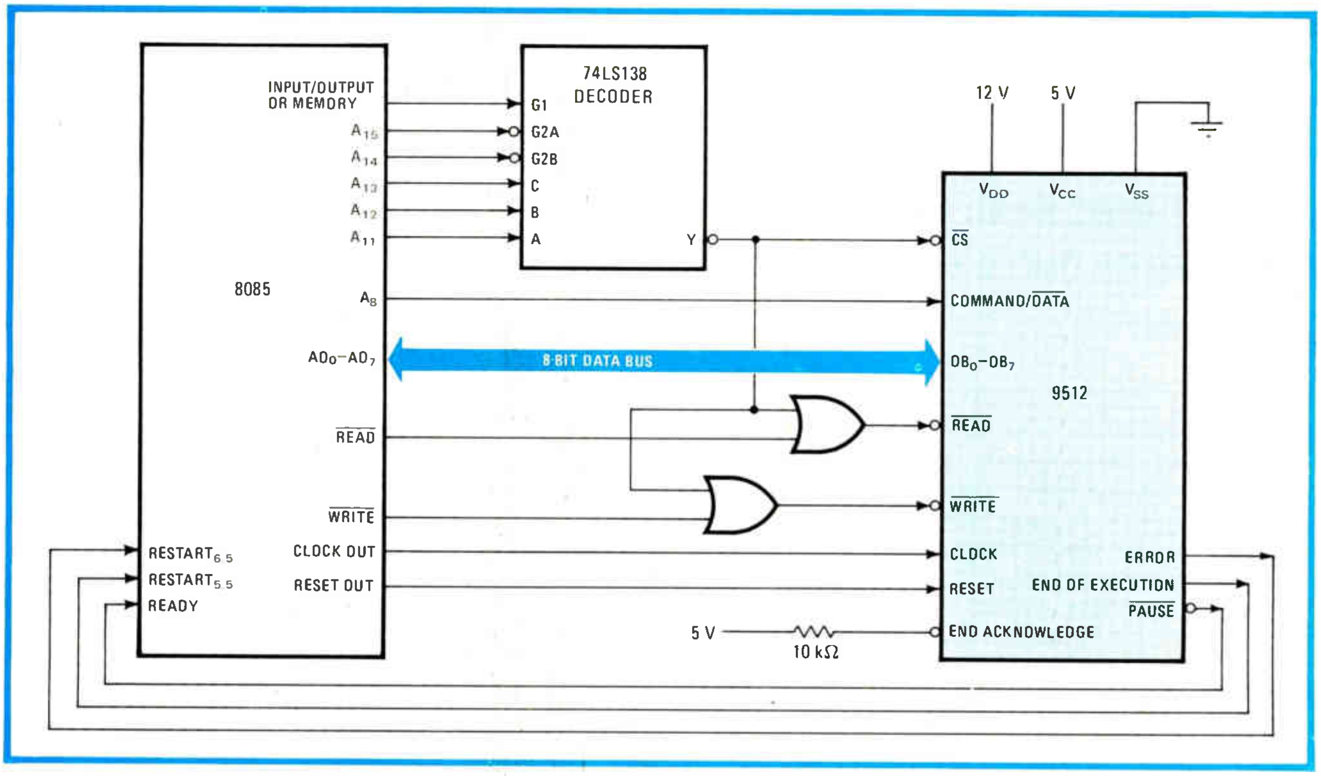
Command performance

All operations are initiated by 8-bit instructions called commands that are issued by the host processor. The command format is illustrated in Fig. 4a. Commands fall into two main categories: arithmetic and data manipulation. Data manipulation includes changing sign, exchanging operands, and pushing or popping operands onto or off the stack.

As mentioned earlier arithmetic operations place



4. Status and command. Formats for the 8-bit registers that hold commands (instructions) and machine status in the 9511 and 9512 also differ slightly. The 9511, with more commands, requires a 5-bit operation code, as opposed to the 9512's 4-bit op code, for example (a). Also, because of instruction-set differences, bits 0–4 of the status register represent different conditions in each unit (b).



5. Interface. Hooking the 9512 floating-point processor to an 8085 microprocessor requires few parts for a minimum configuration. The 74LS138 4-bit decoder drives the math unit's chip-select input by decoding higher-order address bits. Error and end-of-execution flags connect to the 8085's interrupt inputs, $RST_{5.5}$ and $RST_{6.5}$. Data is transferred over an 8-bit bus.

operands in the TOS and NOS positions in the internal stack and always return the result to the top of the stack. Also, the result from an operation always has the same precision and format as the operands.

Accuracy will differ in the 9511 and 9512 for the same 32-bit floating-point arithmetic operations, however. Even though both units have a 24-bit mantissa, the 9511 truncates its result (for faster speed), whereas the 9512 employs a rounding algorithm in order to provide greater accuracy.

As can be seen in Fig. 4a, bit 7 in the command register indicates whether a service request is to be issued after the command is executed. If the bit is a 1, the service-request output will go high at the conclusion of the command and remain high until reset by a low level on the chips' service-acknowledge pin ($\overline{SVACK}$) or until completion of a succeeding command in which bit 7 is a 0. The end-of-execution output pin ($\overline{END}$) also indicates that execution of the previously entered command is complete. It is cleared by an end-acknowledge ($\overline{EACK}$), reset, or any read or write signal to the device.

Qualification

The 9511 and 9512 have an 8-bit status register (Fig. 4b) to qualify the results of an operation. Note, however, that the status register's contents are valid only when the first, or busy, bit, is a 0, indicating that the present operation is completed and another operation can be initiated. The status register can be interrogated by an external device without any restriction.

Since the 9511 and 9512 are designed with a general-purpose 8-bit data bus and interface control, they can be conveniently used with any microprocessor. Figure 5 shows an example of a minimum configuration.

Timing for the execution of commands makes sense only if given in terms of clock cycles; from there, actual timing can be obtained only after ascertaining the system's clock period and the parts' maximum specified clock rate. Basic 9511 and 9512 devices are specified at 2 megahertz, and premium parts at 3 MHz.

Execution timing

At 2 MHz the 9511 performs a 16-bit fixed-point addition in 8 microseconds, a 32-bit floating-point addition in 27 μs, a 32-bit floating-point multiplication in 73 μs, and a 32-bit floating-point exponentiation (x^y) in 4.415 milliseconds. An equivalent 32-bit floating-point addition and multiplication with the 9512 take 28 and 93 μs, respectively—the longer execution time is the result of the 9512's more precise rounding algorithm. For 64-bit floating-point operations, addition requires 276 μs, subtraction 253 μs, multiplication 766 μs, and division 2.043 ms.

Those times are only approximate, however, since substantial data-dependent variations are possible. Total execution time must also make allowances for operand transfer into the chips, command execution, and result retrieval from the devices. Except for command execution, those times will be heavily influenced by the nature of the data, the control interface used, the speed of the memory, the host processor used, the priority allotted to direct-memory-access and interrupt operations, the size and number of operands to be transferred, and the use of chained calculations. □

Time-shared analog bus multiplexes audio signals

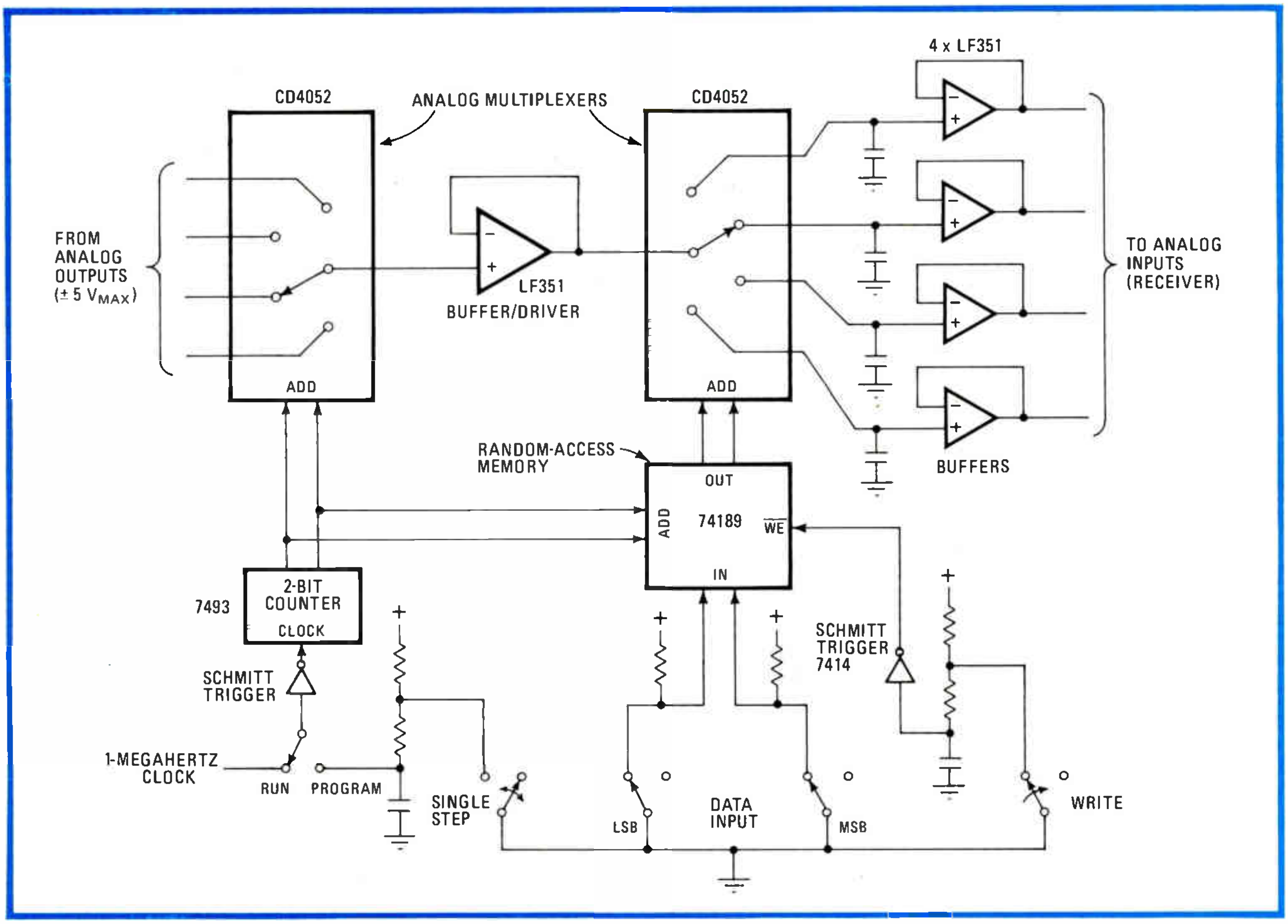
by Colin Johnson
Madison, Wisc.

A multiplexed analog bus can be easily realized by means of complementary-MOS analog switches and rudimentary sample-and-hold circuits. Thus the advantages gained by the time-division multiplexing of digital signals—mainly the multichannel sharing of processing hardware—may be also secured for audio waveforms.

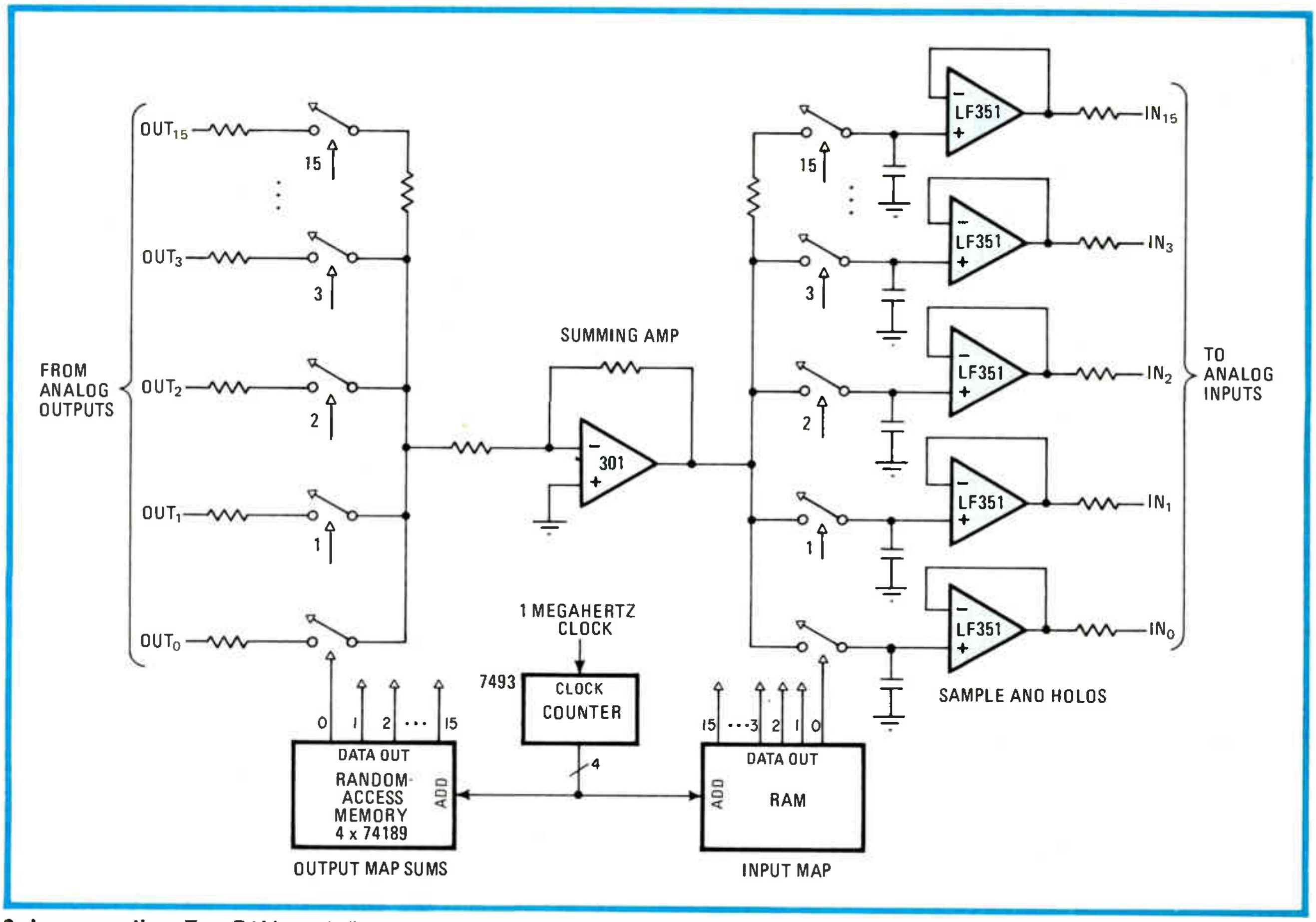
Each analog driver output is connected to the bus through an analog switch. Each analog receiver input is attached to the bus via a simple capacitor/operational-amplifier sample-and-hold stage. As each output is switched onto the bus, the corresponding inputs it is connected to are also engaged. During this aperture time, the hold capacitors are charged. The specific input/output map is stored in a random-access memory. If a computer is available, a memory-mapped scheme lets the user implement changes easily and affords convenient cataloging of any patch on a mass-storage device.

C-MOS analog multiplexers serve as the central switching element in the four-channel multiplexer shown in Fig. 1. These devices are bidirectional and have separate TTL-level address inputs, enabling the switching of analog input signals in the range of ±5 V.

The bus technique is not confined to a four-input multiplexer, of course, and many other configurations can be constructed. Figure 2 shows a design using discrete analog switches and a summing amplifier that mixes 16 unique sums of outputs to any number of 16 inputs. Multiplexing is done at 62.5 kilohertz in this case (47 KHz if an additional 250-nanosecond settling time is permitted). This sampling frequency is sufficient to process audio signals below 20 KHz without significant distortion. When tape recording and other baseband equipment is used, a low-pass filter will be required to eliminate the switching noise that is generated. □



1. Four by four. Analog multiplexers combine four analog signals over a common bus. Counter, driven by 1-MHz clock, sequentially selects analog outputs and sends signals over bus to receiver. RAM containing input/output map delivers signals to required port.



2. In summation. Two RAMs and discrete analog switches enable multiplexer to deliver up to 16 sums of outputs to any number of 16 receiver inputs. Number of sums is proportional to length of RAM. Multiplexing is done at 62.5 kHz to ensure coverage of audio band.

Implementing interrupts for bit-slice processors

by Vern Coleman
Advanced Micro Devices Inc., Sunnyvale, Calif.

Interrupt detection and handling at the microprogram level can be easily implemented in the Am2900 bit-slice processor family thanks to versatile components like the Am2914 priority interrupt encoder and others. The interrupt scheme can generally be extended to other systems at the cost of additional circuitry.

As shown in the figure, the components required are the 2914, the 2910 microprogram sequencer, a 29775 programmable read-only memory, and two separate PROMs for mapping instructions from main memory and interrupt vectors from the 2914 into starting addresses for the 2910.

If an interrupt is detected by the 2914 as the 2910 executes an instruction, the interrupt-request output of the encoder moves low. This action turns off the carry input of the 2910, for all practical purposes causing the sequencer to halt for a microcycle. It also causes any data that would normally appear at the Y_i outputs to be stored in the sequencer's program counter.

The interrupt request also forces the output of the sequencer into a high-impedance state. This allows an interrupt-handling vector to be applied at the Y_i outputs, thereby addressing the first instruction of the interrupt routine in the microprogram memory.

The 2914 is thus instructed to place an interrupt vector on its output port. The same word in microprogram memory also enables the output of the vector-mapping PROM to allow decoding of the interrupt vector. The result is then applied to the D inputs of the 2910 while it does a jump to the appropriate subroutine. Thus the first address of the interrupt routine is brought in, and the address to which the previously executed program is to return after the interrupt is serviced is stored away. If there is a point in the microprogram routing where no interrupts are to be allowed, a logic 0 can be applied to the interrupt disable input pin on the 2914.

The microcode for handling interrupts is shown in the table. The first entry commences with address I. This vector instructs the 2914 to execute a jump to subroutine if its condition code input is low. The encoder is then commanded to place its interrupt vector associated with the current interrupt request on its output port. At this time, it may be desirable to disable any further inter-

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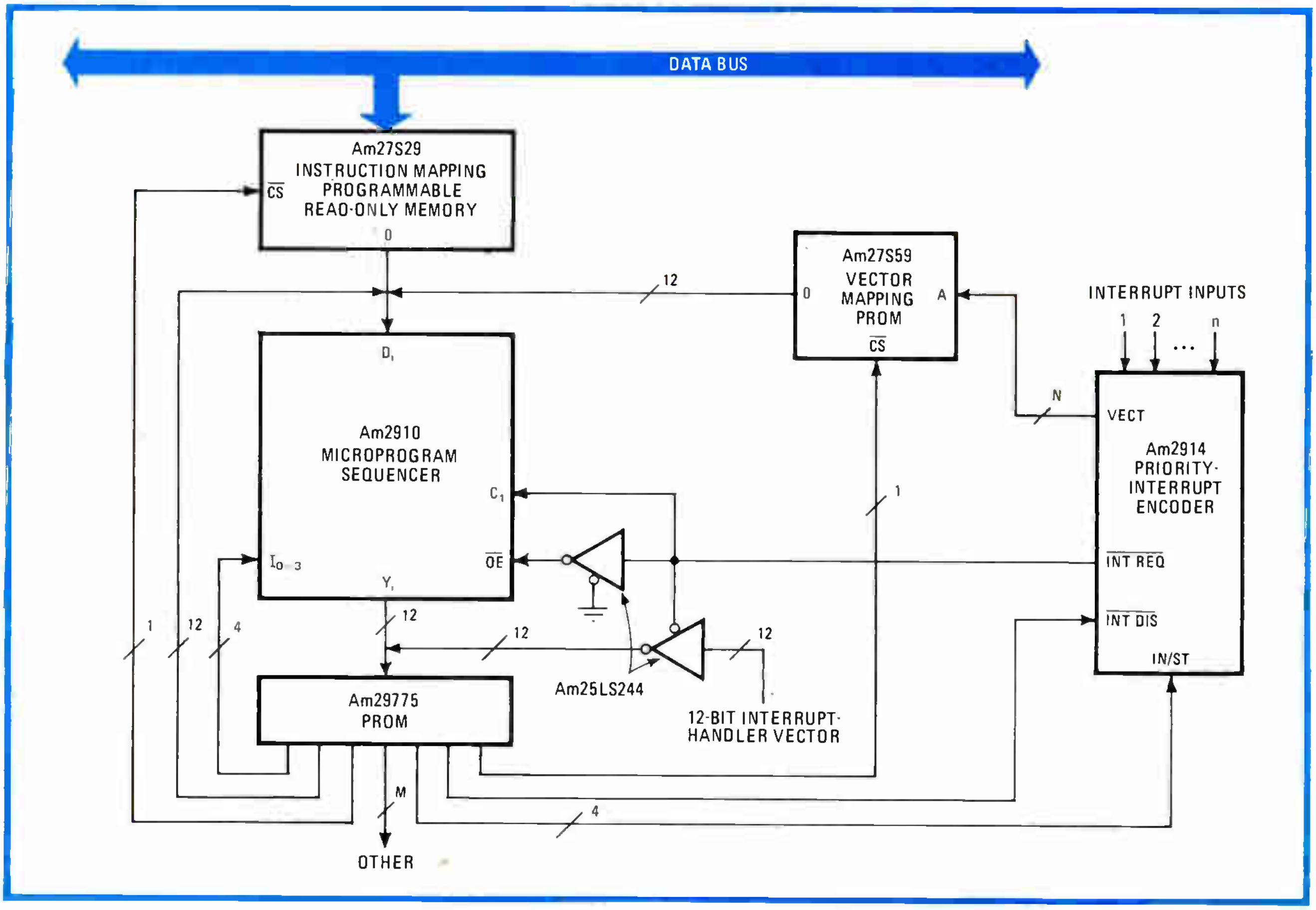

Interrupt address	Am2910 instruction	Am2914		Vector-mapping PROM	Data-mapping PROM
		Instruction	Interrupt disable		
I	CJS	Read vector	0	0	0
I + 1	–	Clear interrupt, last vector read	0	1	–
I + 2	–	Enable interrupt request	1	1	–
I + 3	CRTN	–	1	–	–

Stop. Standard elements of the Am2900 family are easily configured to provide interrupt capability for bit-slice microprocessors. Architecture is applicable to stacked interrupt systems. Microcode for handling interrupts (see table) is fast and simple.

rupts, in which case the appropriate pin should be brought low, as explained above. A logic 0 is also placed on the vector-mapping PROM while a logic 1 is placed on the data-mapping PROM's output-enable lead and the pipeline output-enable of the 29775. Thus the vector-mapping PROM will be the sole source of any input to the D port of the 2910.

At address I+1, the interrupt associated with the previous vector read into the 2914 may be cleared, and the vector-mapping PROM disabled by bringing its output-enable lead high. At address I+2 and subsequent addresses, the 2914 may be commanded to accept any interrupt by use of the enable interrupt request. The vector-mapping PROM is first disabled with a logic 1 signal. At this time the interrupt-disable pin of the 2914 is deactivated. At the end of the interrupt routine, an exit is achieved via the conditional-return instruction of the 2910. A logic 0 should be simultaneously applied to the condition-code inputs of the sequencer.

There is nothing that precludes the use of this architecture in a stacked-interrupt system. The number of interrupts that can be stacked is limited by the depth of the 2910. It is only necessary to issue a simple command to return from the subroutine utilized to the main program, for each stacked interrupt. □

Engineer's notebook is a regular feature in *Electronics*. We invite readers to submit original design shortcuts, calculation aids, measurement and test techniques, and other ideas for saving engineering time or cost. We'll pay $50 for each item published.

Engineer's newsletter

Software club provides Pascal tools

"Although Pascal is ideally suited for serious systems and applications programming on microcomputers, it is new enough in popularity that relatively few Pascal programs have been widely available to date. Moreover," says Jim Gagné, president of DataMed Research in Los Angeles, "needed software tools—a cathode-ray-tube mask generator and maintainer, a package of routines for complex variables, and a double-precision arithmetic package, etc.—have not been generally available." To help meet this need, Gagné has formed the UCSD Pascal Users' Group, a software club offering inexpensive, machine-readable media packed with Pascal programs. At the present time, the main focus of the group is UCSD Pascal. In the future, **as the CP/M-compatible compilers become more mature and more popular, they, too, will be supported.**

For further information, send a self-addressed, stamped envelope to 1433 Roscomare Rd., Los Angeles, Calif. 90024, or call Jim at (213) 472-8825.

Newsletter has Telidon information

Anyone interested in the burgeoning video information industries throughout the world—like Antiope in France, Prestel in England, and the various systems being tested in the U. S. and Canada—will want to receive the Telidon Reports newsletter. **Intended to keep manufacturers of Telidon-compatible equipment and system users informed about significant developments in the Canadian government's interactive television system** [*Electronics*, April 10, p. 44], it will be published every two months and is available on request from Telidon Reports, DOC-DGSRP, Room 200, Journal Tower South, 300 Slater St., Ottawa, Ontario, Canada K1A OC8. The newsletter can also be called up on the Telidon network by anyone with an appropriate setup.

NBS hosts fiber-optic symposium

Because the parameters to be measured are unfamiliar to electrical engineers and instrumentation is not generally available, measurement technology is the weak point in the growing field of fiber optics. Cognizant of this problem, the National Bureau of Standards, in cooperation with the Institute of Electrical and Electronics Engineers' Committee on Fiber Optics and the Optical Society of America, will sponsor the Symposium on Optical Fiber Measurements on October 28–29 at the NBS's Boulder, Colo., laboratories. **The meeting will focus specifically on measurement problems,** provide a forum for the presentation of current work, and allow time for discussion of some of the more difficult tasks facing the optical communications industry. About two thirds of the program will be devoted to contributed and invited papers, with the remaining time devoted to workshops.

Papers are being solicited on attenuation measurements, bandwidth measurements, radiation-pattern and mode-distribution measurements, index profiling, physical measurements, joint (connector-splice) evaluation, single-mode fiber characterization, system field measurements, link performance prediction, and standards. Instructions for submitting summaries, as well as registration, accommodation, and program information, may be obtained from D. L. Franzen, General Chairman, Electromagnetic Technology Division, NBS, Boulder, Colo. 80803. **The deadline for submitting summaries is July 18.** For more information, contact Ken Armstrong at (303) 499-1000, ext. 3787.

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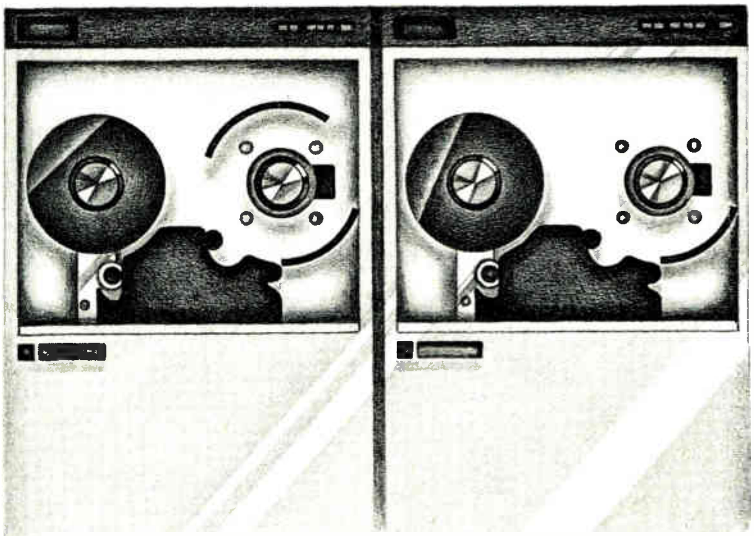

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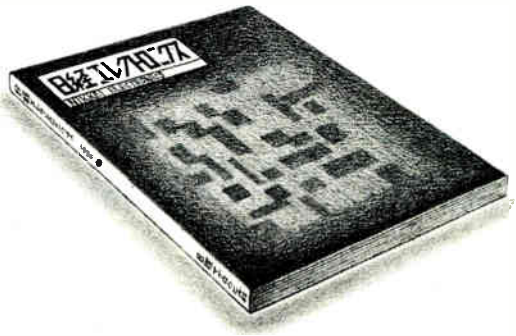

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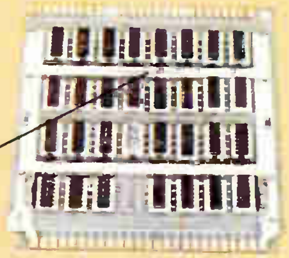
How the smart companies



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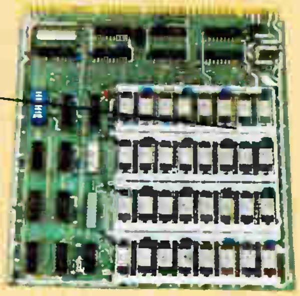
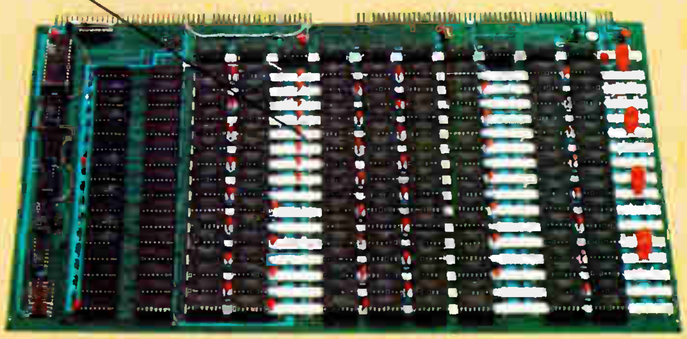


and avoid multi-layer boards



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Circle 167 on reader service card

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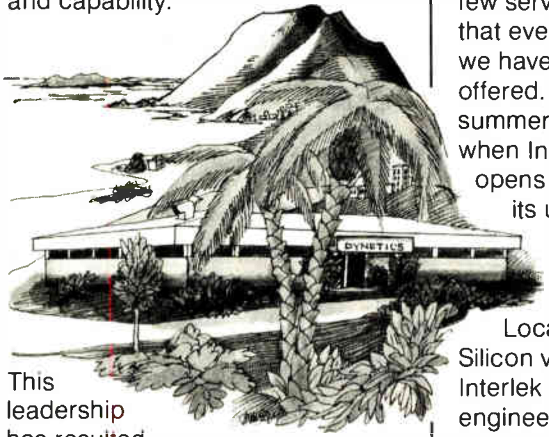

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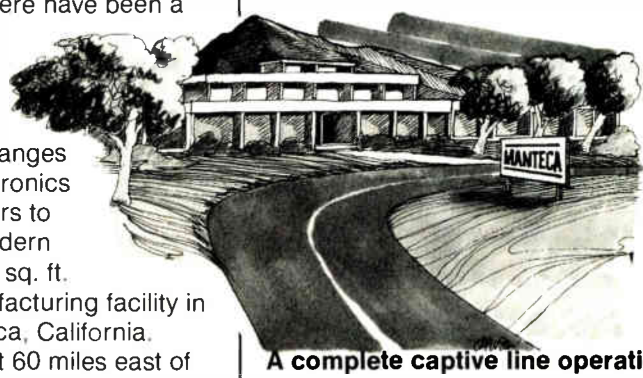

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Displays photographed separately to simulate typical appearance. 610/03

Circle 169 on reader service card

This year's annual show sponsored by the IEEE will have on display from May 13 to 15 at Boston's Hynes Auditorium products that range from capacitors to development systems

Electro/80

RCA adds full-screen editing to microcomputer development line

RCA Corp.'s Solid State division is improving its offering in microcomputer development systems with the Cosmac System IV, a developmental tool that will be shown for the first time at Electro. Also designated CDP18S008, it is an upgraded version, based on a cathode-ray tube, of RCA's earlier 005 and 007 systems. As with these older versions, the 008 is a development system for RCA's 1802 8-bit complementary-MOS microprocessor. It can also be used with the 1804 microcomputer. Featuring full-screen editing capabilities, the system also comes with a dual-drive floppy disk, a keyboard with 58 standard ASCII keys and 14 special-function keys for the full-screen editing, a separately housed Micromonitor debugging and development tool, 28 kilobytes of user random-access memory, and high-level language capabilities.

New chips. The system uses two new C-MOS integrated circuits to generate the character set for the CRT, as well as a new chip, the CDP1871, for keyboard scanning. The CDP1869 and CDP1870 are incorporated in a chip set that can provide character generation, sound, motion, graphics, and color. Not all of these features are used in the 008 development system, however. The chips will generate 24 80-character lines; if sold as separate components, they generate 24 40-character lines for the screen.

"The full-screen editing is significantly faster and easier to use than text-editing systems," says C. Michael Caterina, manager of product marketing for microprocessor systems. "The user has instant verification of changes he makes."

In addition to this editing feature, the 008 also has a disk-based CDOS operating system that manages disk files. Included with the 008 is an assembler and editor for the 1802, and a Level II macroassembler. The 008 has a built-in programmable read-only memory programmer that can be used with any PROM up to and including the industry standard 2716s, according to Caterina. The development system may also be used to program the CDP18μ42 erasable PROM, a 256-by-8 C-MOS

device soon to be announced by RCA.

Included in a second chassis are two drives for 8-inch single-sided single-density floppy disks, giving a total capacity of 0.5 megabyte. Also shipped with the system as a stand-alone unit is a real-time monitor and debugger for the 1802. Available for the last several years, the Micromonitor is similar to an in-circuit emulator, but can also be used as a portable test instrument in the field. The Micromonitor is controlled by its own internal microprocessor; it uses the microprocessor, power supply, clock, memory, and associated hardware of the system under test to run the user's program. It is used primarily for prototype-system software and hardware debugging.

A Centronics-compatible printer interface is included with the system; RCA plans to offer an optional printer for the system shortly. Priced at $3,000, the unit will be bidirectional, and print at 340 characters/s.

Available with the system as options will be three high-level languages: microForth, PL/M 1800, and Basic 1. MicroForth has been available for use with the 1802 for some time, but both PL/M and Basic are recent additions to the 1802 catalog. As a stand-alone software package with 32 kilobytes of random-access memory, the PL/M offering will sell for $2,700. The language of the $300 fixed-point Basic 1 package can be either interpreted or compiled.

"In addition to adding the integral CRT and full-screen editing capabilities, the 008 provides the customer with everything he needs for hardware and software development. This is everything to do program development, even without the high-level languages," Caterina notes.

The CDP18S008 will sell for $11,000, with deliveries to begin in the third quarter.

RCA Solid State Division, P. O. Box 3200, Somerville, N. J. 08876. Phone (201) 685-6605 [391]

Microcomputer develops software

By combining modular Multibus-based hardware with the CP/M2.0 disk operating system, Matrox Electronic Systems has managed to come up with a microcomputer that can be used for software development as well as in computers at the original-equipment–manufacturer level. The MACS-10 marks Matrox's first venture into the data-processing market; the Montreal firm had until now been supplying only controllers related to video display.

The system is configured around the Z-80A (4-MHz) central processing unit. It also includes 48 kilobytes of random-access memory and sockets for 8 kilobytes of read-only memory or erasable programmable ROM. A 2-kilobyte monitor program, a dual 8-in. double-density floppy-disk drive and controller, and interfaces for a video terminal and line printer are also included in the package. Other peripherals can be connected through additional ports at the rear of the MACS-10 chassis.

Matrox offers Pascal, Cobol, Basic, and Fortran packages for the MACS-10, but users can also choose from the hundreds of applications programs written by independent software houses. Software development is speeded up by board-based software support for CP/M2.0 and can be done on the same hardware that is used in the target systems.

MACS-10 hardware is modular, so available separately are: the model ZBC-80 single-board computer, the model FFD-1 floppy-disk controller and RAM card, the CCB-7 seven-slot card cage and backplane with power supply and fan, and the DF-28 dual floppy-disk drive.

The card cage-backplane and the dual floppy-disk drive both conform to the Electronic Industries Association's recommended 19-in. rack spacing. The ZBC-80 and FFD-1 cards occupy two slots in the card cage, leaving five slots for system expansion. If more slots are needed, up to three card cages can be stacked together for a maximum of 19 free card slots.

Support hardware for the MACS-10 system includes a 128-kilobyte RAM card and what Matrox claims is "the industry's widest selection of alphanumeric and graphic video display controllers."

Delivery is 30 to 45 days after receipt of order. A single MACS-10 is priced at $5,990.

Matrox Electronic Systems Ltd., 5800 Andover Ave., T. M. R., Quebec H4T 1H4, Canada. Phone (514) 735-1182 [393]

IC regulates power switchers

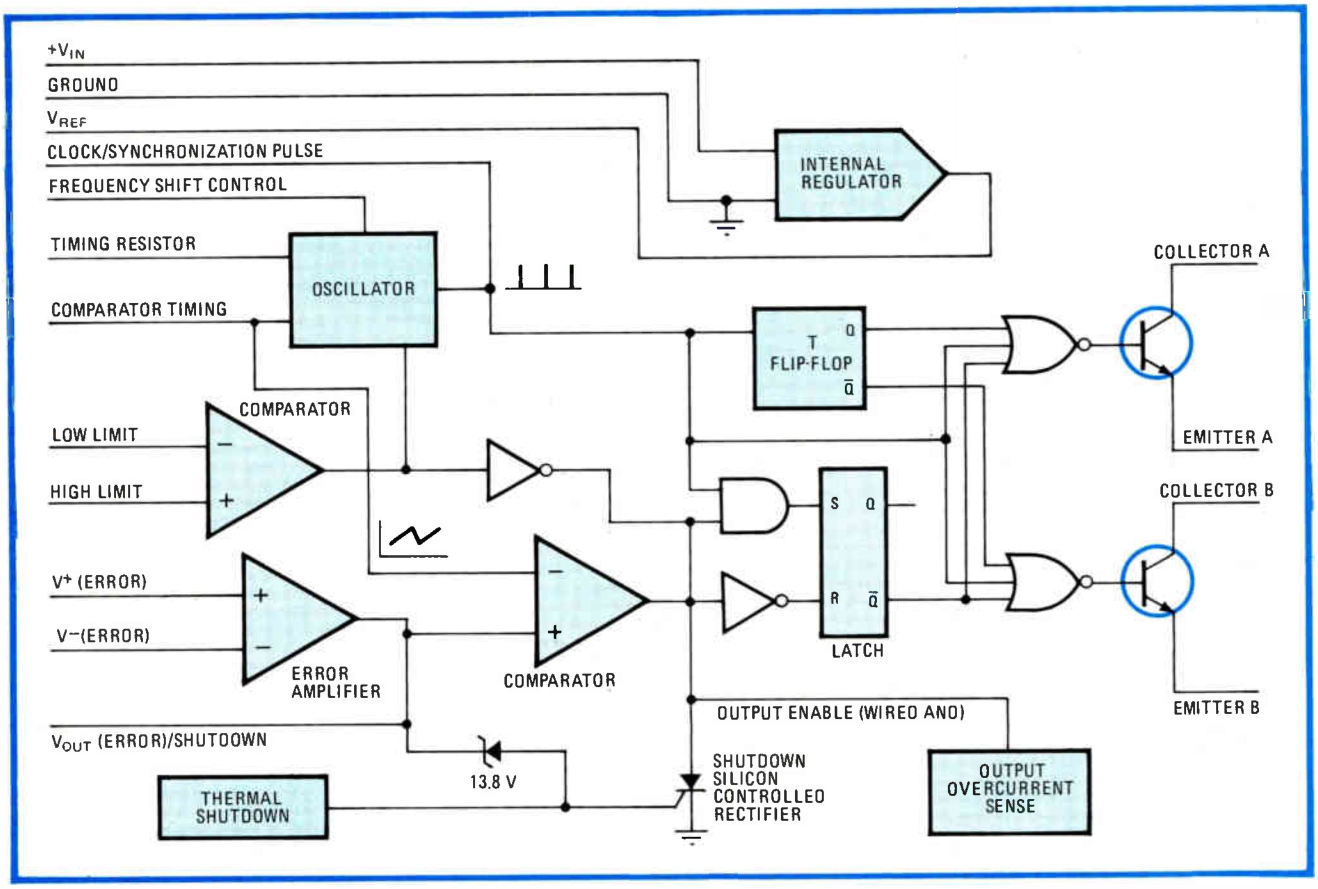
Since switching power supplies have gone solid-state, a major effort for the next generation has been to cut the number of components. With its switching regulator integrated circuit, Lambda Semiconductors promises a means of doing just that.

In fact, the LAS3800 is a monolithic switching regulator specifically developed for use in fixed power control applications, such as switching power supplies and motor controls.

"The LAS3800 replaces more than 75 components found in the first generation of switching power supplies," claims Merrill J. Simon, vice president for Veeco Instruments Inc., the Melville, N. Y., manufacturer of Lambda Semiconductors' products. The device itself contains some 200 to 300 components, according to Simon.

Besides replacing the discrete parts, the LAS3800 is also providing some functions not found with other switching controllers. Among these is a dynamic volt-time symmetry correction feature—provided in double-ended systems—to control the alternate cycle of the pulse-width modulator, making the average magnetic field in the transformer zero.

"In other words, the transformer doesn't go into saturation," says Suneil Parulekar, marketing manag-



er for semiconductors. An ultrahigh-speed current-limiting comparator—operating within 0.5 μs typically and 0.9 μs maximum to shut down the output—protects the switching transistors. A thermal shutdown mode at 150° C minimum, 175° C typically, and 200° C maximum also protects the chip.

The IC features dual 0.5-A output transistors that enable it to drive most switching transistors directly, as well as drive a transformer directly when operating at 40 V. These two symmetrical npn devices offer output overcurrent protection as well.

The LAS3800 will operate at 10 to 40 V, with a temperature-compensated 1.65-V reference. The sawtooth oscillator has overcurrent frequency shift functions from dc to 500 kHz; the frequency shift is programmable, as is the dead time of the device. The unit has linear "trailing-edge" pulse-width modulation with double-pulse–suppression logic. In addition, the LAS3800 features an uncommitted error amplifier and a soft start capability.

Useful in implementing switching regulators of either polarity, the LAS3800 may also be used in transformer-coupled dc-dc converters, voltage doublers not using transformers, polarity converters, and dc or ac motor controls. The device will operate in a temperature range from 0° to 125° C.

Selling for about $15 each in 1,000-unit quantities, the LAS3800 can be delivered within four to six weeks.

Lambda Semiconductors, 515G Broad Hollow Rd., Melville, N. Y. 11747. Phone (516) 694-4200 [394]

Unit acquires data for $275

The new DT5712, from Data Translation Inc., is an 8- or 16-channel data-acquisition system that handles both high- and low-level signals and offers optional programmable gain—at a base price of $275.

The basic DT5712 is a high-level-only unit capable of working with inputs in the ±10-V range. Its gain, set by a user-selected resistor installed adjacent to the module, is fixed and identical for all channels. Gain can range from unity to 1,000.

For engineers working with high-level inputs alone in applications where all inputs are of roughly similar values, the bare-bones DT5712 offers very good value for its price, according to the Natick, Mass., firm, and it may even be the lowest-cost such device available. Within its 3-by-4.6-by-0.375-in. shielded package is a multiplexer, an instrumentation amplifier, a sample-and-hold network, and control logic. The output is tristate and microprocessor-compatible, and inputs are at MOS/TTL logic levels.

The throughput is 40 kHz, or 25 ms per channel; sample-and-hold aperture time is 50 ns with an uncer-

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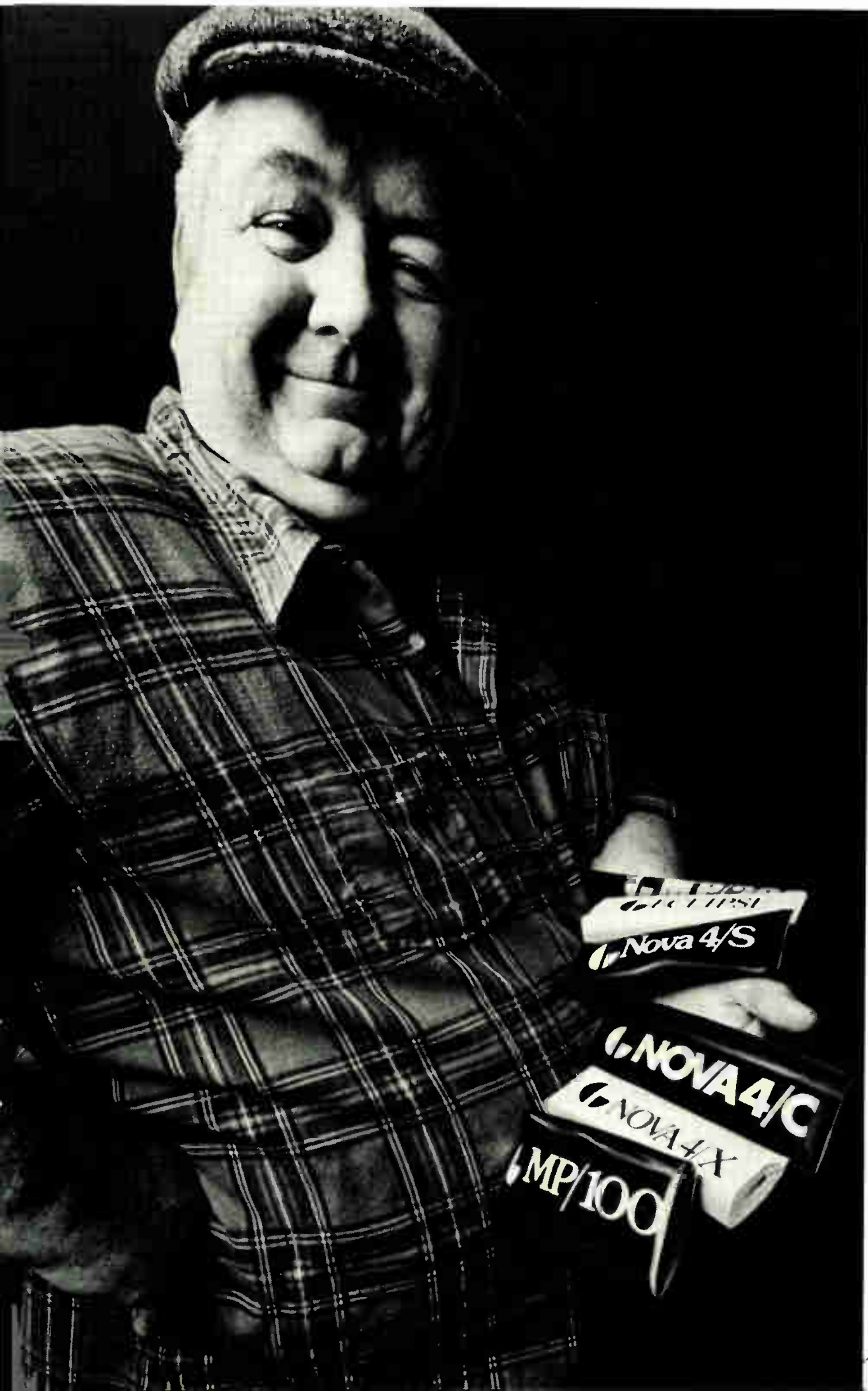

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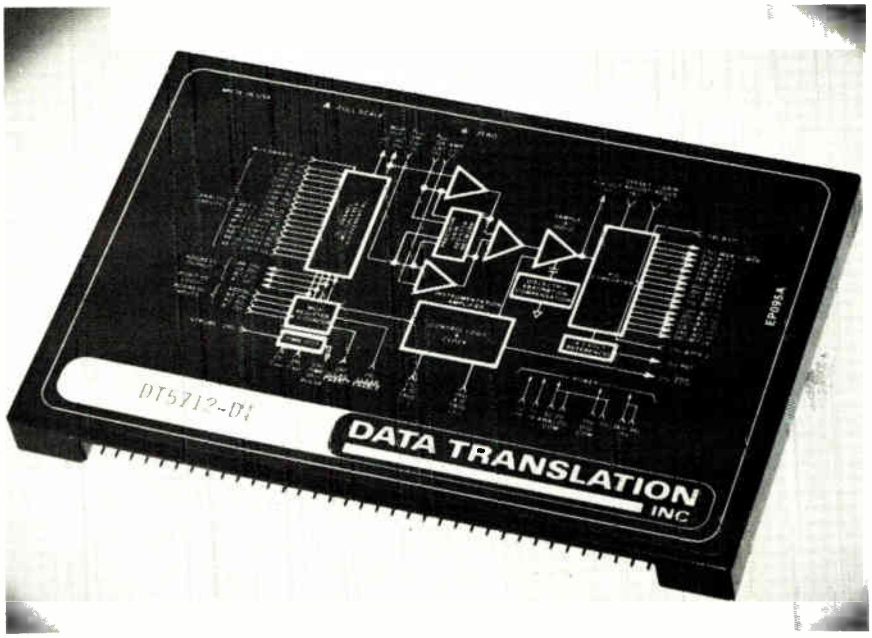
Circle 175



tainty of 10 ns. Conversion time is a reasonably quick 10 ns.

Linearity is within ±½ least significant bit, with differential linearity and unity-gain system accuracy both within 0.03%. At higher gains, system accuracy is somewhat lower, falling to within 0.05% at a gain of 100, for example. The unit can handle both 16 single-ended and 8 differential inputs.

The device is designed to interface easily with microprocessors. It is also available on analog interface boards that are compatible with Digital Equipment Corp's PDP-11 and LSI-11 systems, as well as with the Intel/National Multibus, Computer Automation's LSI series, the Mostek/Prolog STD bus, and Zilog's MCB. Control inputs are at MOS/TTL levels, and the DT5712's output often can be spilled directly onto a microprocessor bus. Output consists of an 8-bit byte and a 4-bit nibble, and both are accessible either serially or in parallel as required.

To this basic capability, the user can add options for programmable gain and low-level operation. Ordered at the time of purchase, these two options make possible channel-to-channel gain changes under software control via the module's microprocessor-compatible inputs. The PGH option, for ±10-V inputs, offers gains of 1, 2, 4, or 8; the PGL option—which also moves the DT5712 into the low-level, ±20-mV range—offers gains of 1, 10, 100, and 500. The electronics for these options are added to the module at the time of assembly and are housed within the unit's shielded enclosure for protection against radio-frequency interference.

Data Translation claims that the availability of these options is unique to the market, though some competitors offer programmable gain as a standard feature of some more costly, high-level modules. The firm says, though, that industrial applications requiring interchannel gain ranging are a major applications area.

Delivery of the DT5712 takes five days.

Data Translation, Inc., Four Strathmore Rd., Natick, Mass. 01760. Phone (617) 655-5300 [395]

Mica capacitors offer stability

A series of mica chip capacitors to be shown at Electro by Arco Electronics Inc. offers high-frequency characteristics over a wide capacitance range. The UC family covers 1

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With its snap-on covers, the TM 515 Travel Lab is attractive as well as durable. It fits easily under most airline seats and weighs only about 30 lbs. fully loaded with plug-ins.

For trips next door or down the hall, there's the Model 3 Cart. With a Tektronix Oscilloscope on top, up to two TM 500 Mainframes can fit on the lower decks. A large accessory drawer at the base lets you store all your odds and ends. And four permanent power outlets are joined to a single 15-foot line cord.

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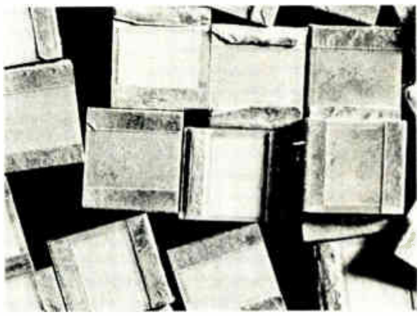


to 2,000 pF at a 100-working-volt (WV) dc rating and 1 to 1,200 pF at a 500-WV dc rating.

Irwin Wolberg, marketing director, says, "Highlights of the product include a special lamination method which does not use metal foils. With their high-frequency characteristics and extreme stability, mica capacitors are superior to other capacitors," he claims. "No special treatment is needed for soldering, nor will the capacitor undergo cracking because of thermal shock. There is a high mechanical-strength stability because of the mica," Wolberg says. The only special requirement for soldering is that the solder must be 2.5% to 3% silver; the soldering is done easily because silver is used for the electrodes.

The temperature characteristics of the capacitors are as follows: for nominal capacitance greater than or equal to 1 pF, but less than or equal to 10 pF, the temperature coefficient is between 0 and 200 ppm/°C with a capacitance drift of ±(0.5% +0.1 pF); nominal capacitance that is greater than 10 pF, but less than or equal to 30 pF, has a temperature coefficient between 0 and 100 ppm/°C with a drift of ±(0.1% +0.1 pF); and nominal capacitance greater than 30 pF has a temperature coefficient between 0 and 50 ppm/°C, with a drift of ±(0.05% +0.1 pF).

Capacitance tolerances that are available range from ±0.25 pF to ±5 pF for capacitances greater than or equal to 1 pF, but less than or equal to 10 pF; for capacitances greater than 10 pF, the tolerances available go from ±0.25% to ±5%, with a minimum of ±0.25 pF.

For a capacitance range of from 1 pF to 100 pF, the step is 0.5 pF; for a range of from 100 pF to 1,000 pF, the step is 1 pF; and for 1,000 pF to 2,000 pF, the step is 10 pF.

Typical measurements of capacitance compared with frequency are as follows: at 5 pF, the capacitance remains stable to beyond 200 MHz; at about 10 pF, it remains stable to about 150 MHz; at about 50 pF, to 50 MHz; and at about 100 pF, to about 30 MHz.

For a capacitance between 10 pF and 330 pF, the Q is between 6500 and 8500 at 1 MHz. Below 10 pF, the Q drops to 3,000 to 4,000 at 1 MHz. The dissipation factor, for a life test, for a 2000-pF capacitor rated at 100 WV, with a ±5% tolerance, is between 0.02% and 0.03%.

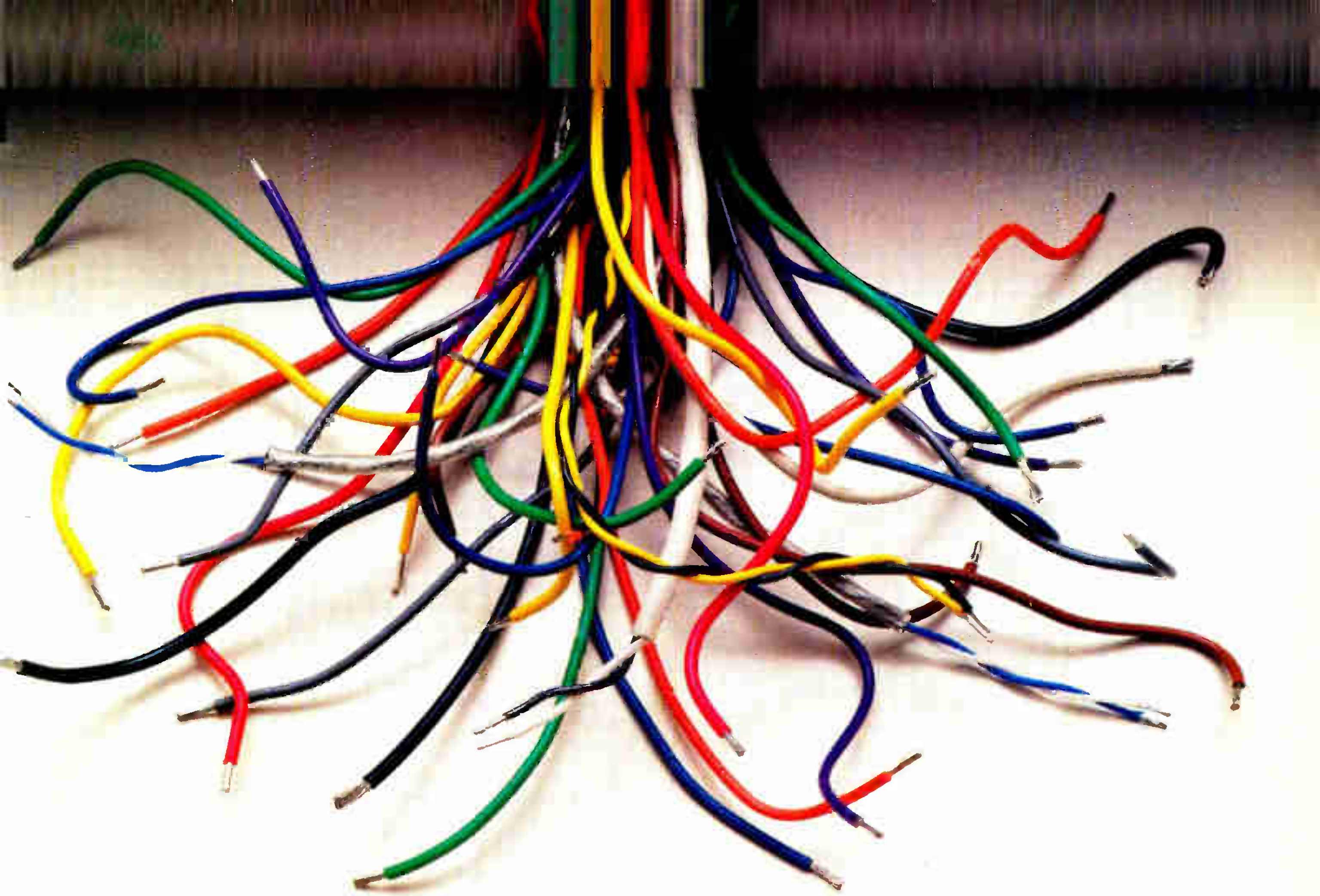
The size of these mica chip capacitors varies according to the capacitance range and working voltage rating, and prices vary accordingly. For example, a typical member of the UC family of mica chip capacitors, a 100 pF capacitor with a tolerance of 0.25%, sells for $1.50 in small quantities; however, for a 100 pF capacitor with a tolerance of 2%, the price drops to 62¢ in similar quantities. Delivery time on the units runs from about 8 to 12 weeks after an order is received.

Arco Electronics Inc., 400 Moreland Rd., Commack, N. Y. 11725. Phone Ronald Travis at (516) 864-7000 [396]

Analyzer covers broad spectrum

Sporting a frequency range from 30 Hz to 200 MHz, Marconi Electronics' newest spectrum analyzer also features a 100-dB displayed dynamic range. The TF 2371 has a resolution of 0.1 dB and 5 Hz. In the manual mode, the frequency resolution improves to 1 Hz. A built-in tracking generator, covering the full 200-MHz range, permits measurement of voltage standing-wave ratios and frequency responses for component testing and amplifier and filter characterizations.

The 2371 has a recirculatory digi-



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Circle 179 on reader service card

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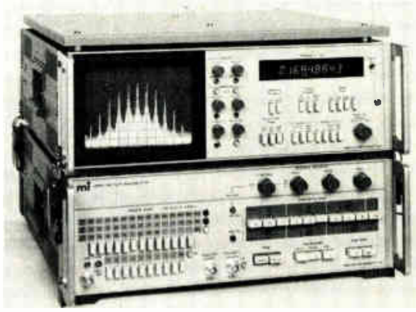

tal store built with MOS field-effect transistors that produces input for a 256-by-512 point display. This stored information is continuously scanned and shown on a 130-by-100-mm display.

Stored data display. A split-store mode divides the display in half to show two recorded displays at once—each composed of 256 by 256 points; updating one store while retaining the other for comparison is thus possible. Also included with this display system is an electronic graticule that is movable in the frequency and amplitude directions to ease the measurement of relative frequencies and amplitudes.

The flicker-free image will remain on the screen without fading as long as it is needed. The analysis of the stored signal can be done using a bright line cursor and a frequency counter to identify signal components, spurious signals, and amplifier and filter bandwidths.

Frequency measurement. A nine-digit electronic counter can read out in megahertz, with automatic positioning of the decimal point. It operates in three modes: in the past center mode, the center frequency measured is displayed whenever the data is renewed; in the bright line mode, the counter displays the frequency corresponding to the position of the bright line cursor; and in the so-called diff mode, the counter displays the difference between these two values—which is useful in measuring sideband frequencies in relation to a carrier.

For tuning, the 2371 uses four reference-frequency controls to cover the ranges of 0 to 200 MHz, ±1 MHz, ±70 kHz, and ±1 kHz, respectively. The analyzer resolves to

1 Hz in the manual mode with a 5-Hz filter and a 200-Hz scan width.

For amplitude measurement, there are two vertical scale ranges: +30 to −159 dBm using a 10-dB/division scale; and +30 to −109 dBm using a 1-dB/division scale, with each division equaling about 1 cm. The accuracy for these ranges is: for 10-dB steps, ±0.3 dB per 10 dB, with a cumulative error of less than ±1.5 dB; and for 1-dB steps, ±0.1 dB per 1 dB, with a cumulative error under ±0.3 dB.

There are two logarithmic and one linear vertical scale displays. The logarithmic displays are 10 dB/division for a 100-dB full-screen display, accurate to within ±1 dB for 0 to −80 dB and to within ±1.5 dB for −80 to −100 dB; and 1 dB/division for a 10-dB full-screen display accurate to within ±0.1 dB. The quantization error for both display ranges is ±0.25% of full scale for filter bandwidths of 5 Hz to 5 kHz. The linear vertical scale is 300 mV/division to 300 nV/division, in a 1, 3, 10 sequence on a 10-division display. The volts-per-division nonlinearity is ±1.5% of the full-scale range.

The broad frequency range of the 2371 will be especially useful in radio-frequency communications, broadcasting, frequency-division multiplexing, pulse-code modulation and, single-sideband communications.

Priced at $21,500 in single quantities, the spectrum analyzer is available within 30 days.

Marconi Electronics Inc., 100 Stonehurst Court, Northvale, N. J. 07647. Phone (201) 767-7250 [401]

Audio oscillator has stable output

Once set, the amplitude of the model 4400 oscillator's output varies so little (±0.05 dB) as frequency is tuned from 1 Hz to 110 kHz that the need to monitor voltage levels during audio frequency-response testing is eliminated. That, along with a sine-

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Circle 266 Circle 267 Circle 268 Circle 183 wave output with distortion of less than 0.001%, makes the 4400 effective at measuring harmonic distortion in audio preamplifiers and power amplifiers.

The 4400 can work with low-distortion analyzers from other makers as well as with Krohn-Hite's to make up a complete distortion-measurement system, says the firm.

The 4400 will not only deliver a 7-V rms maximum sinewave into 600-Ω loads, but can put out inverted and quadrature versions simultaneously. This equips the oscillator for circle-generator and phase-locked-loop test applications.

Frequency accuracy holds to ±1% of frequency setting. Both frequency and amplitude are stable to 0.1% for up to an hour, or to 0.05%/°C.

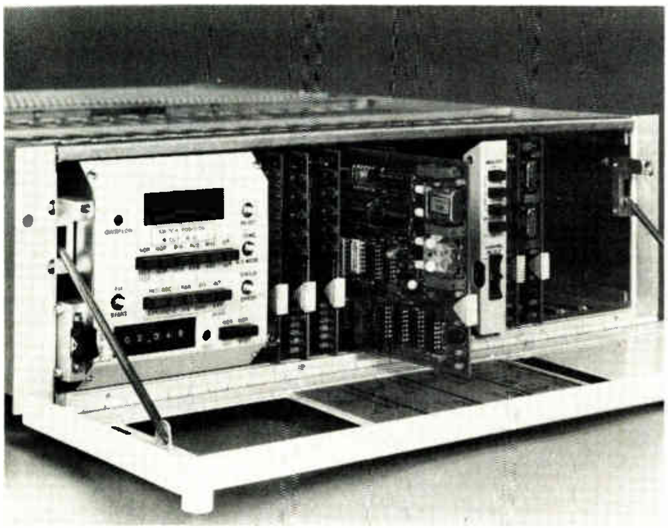
Two rotary switches calibrated to 1 Hz and 0.1 Hz control and select frequency and a calibrated vernier provides continuous coverage between 0.1-Hz steps; there is a five-decade pushbutton multiplier with overlapping ranges. A three-position pushbutton attenuator calibrated in 20-dB steps from 0 dB to −60 dB controls main-output amplitude; with the 20-dB vernier, total dynamic range is 90 dB. Amplitude accuracy is ±0.025% per 20-dB step, or ±20% of amplitude setting.

Hum and noise are more than 100 dB below output level, with a rear-panel switch on the 4400 floating circuit ground from chassis ground to maintain the low noise level. The unit uses switch-selectable 90- to 132-V or 180- to 264-V power; single-phase figures are 50 to 400 Hz and 6 W. The price is $550 per unit. Delivery is in 30 days.

Krohn-Hite Corp., Avon Industrial Park, Bodewell St., Avon, Mass. 02322. Phone (617) 580-1600 [397]

$30 isolators have dc-dc converters

What may be the industry's most inexpensive complete function isolators have been announced by Analog



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Ampex calls it the *M² Digital Encode/Decode Unit.* You'll call it the most cost-effective modem you've ever seen for high density digital multi-channel transmission applications.

Used in conjunction with an analog instrumentation recorder, the Ampex M² Encode/Decode Unit gives you a digital capability of 5 megabits/second at 120 ips, working in Biphase-L, Miller or M² codes. And you can get as many as 10 channels of record/playback in a package only 5¼ inches high by 19 inches wide.

The built-in test option functions as an error counter with a digital readout to diagnose input rates, and it also serves as both a tape and a total system certification system, displaying number of errors in either 10^6 or 10^8 bits. It can also be used as a frequency counter.

Use this unique unit as a digital recording front end, as a self-standing modem on wideband telephone and a signal circuits, or as a multichannel diagnostic adjunct. Power supply is 115/220V, 47 to 400 Hz, and price ranges from about $6,000 to $12,000 depending upon channel count and installed options.

Rene Chikhani can provide complete technical and performance specifications, and he'll work with you on custom system applications. Call Rene at 415-367-2758, or write to him at Ampex Data Systems, 401 Broadway, Redwood City, California 94063.

AMPEX

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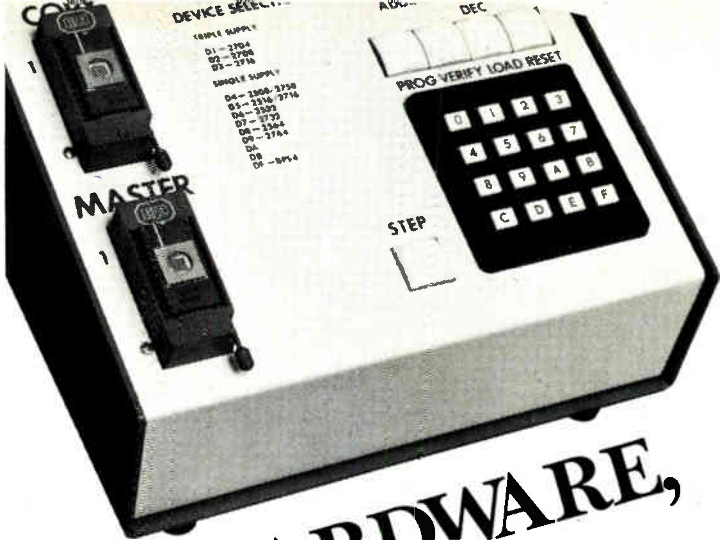

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Devices Inc. The models 290A and 292A are designed for single-channel and multichannel industrial applications, respectively, and are not only priced as low as $30 in 100-unit quantities, but also include built-in dc-dc converters.

Such converters can add more than $10 to the price of other isolators; for example, the optoisolators nearest in price to the 290A and 292A cost $26 and $28 in hundreds—but their dc-dc converter circuitry comes at added cost.

The new isolators use modulation techniques and transformer isolation to interrupt ground loops and leakage paths and to halt voltage transients while providing a frequency response that goes from dc to 2,000 Hz.

The 290A also has a built-in oscillator. The 292A requires an external oscillator, but multiple 292As can be slaves to the same master oscillator to operate in unison.

Both models feature adjustable gain from unity to 1,000, ±1,500-V dc isolation, 100-dB minimum common-mode rejection at 60 Hz, and 1-kΩ source imbalance.

The input noise of the units is a low 1 microvolt peak-to-peak for a 10-Hz bandwidth and a gain of 100. Nonlinearity is ±0.1% at 10-V p-p output, and the units have an input-output dynamic range of 20 V p-p.

Analog Devices expects the units to be used in data-acquisition systems, computer interface systems, process signal isolators, and instrumentation for applications with high common-mode voltage.

Because of their built-in dc-dc converters, the units need only a single power-supply voltage, nominally +15 V. Actually, any voltage between 8 and 16 V suffices, making battery operation possible.

Gain stability is 0.001% per 1,000

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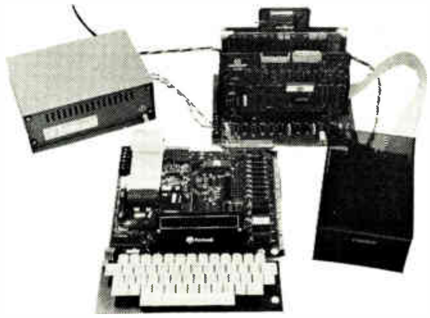

A complete disk system for the Rockwell Aim 65. Uses the Rockwell Expansion Motherboard. Base price of $850 (U.S.) includes controller with software in Eprom, disk power supply and one packaged Shugart SA400 Drive.

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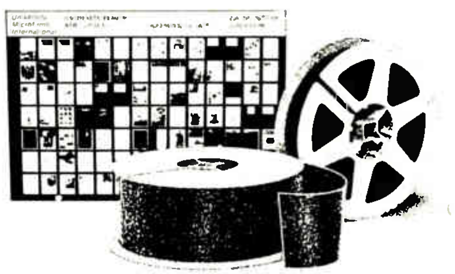

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Circle 187 on reader service card

hr; stability with respect to temperature is ±0.0075% per degree C. Input offset voltage is 5 mV, can be trimmed to 0, and varies with temperature at about 10 μV/°C. Output offset voltage is 55 mV, and in the 290A varies 160 μV/°C. Thus drift is a somewhat higher 260 μV/°C for the model 292A.

Obviously, an isolator cannot itself be a source of noise nor be prone to interference pickup, or else its installation is moot. The 290A and 292A are both relatively immune to radio-frequency and electromagnetic interference. Analog Devices engineers tested the units with a 27-MHz walkie talkie at 1 meter and found that when set for a gain of 1, the isolators provided a 40-dB signal-to-noise ratio. At higher gains, the figure improves; for example, at a gain of 100, the signal-to-noise ratio is 80 dB. It was necessary to bring an electric drill to within a foot of the units to produce any noticeable interference. Therefore, the isolators should be perfectly at home in industrial environments and safe to install near relays and motors.

Both devices are packaged in small 1.5-by-1.5-by-0.62-in. modules. The isolators are priced at $49 for single units and $39 for between 50 and 99 units, with the price for 100 units and up falling to $30. Evaluation units are available from stock. In production quantities, it takes about six weeks for the isolator to be delivered.

Analog Devices Inc., Route One Industrial Park, P.O. Box 280, Norwood, Mass. 02060. Phone (617) 329-4700 [398]

Automatic unit clips leads

The process of clipping component leads by hand is both slow and inexact, and automatic machines dedicated to this process can be costly and large. But a product to be shown at this year's Electro by Roto Form Sales Corp. promises to increase board throughput time at a signifi-

The trouble with most delayed-sweep scopes is the delay—not the electronic kind, but the delivery delay. B&K-PRECISION has solved that problem, so now you can have the delayed-sweep scope you need, when you need it.

The new model 1530 delayed-sweep scope from B&K-PRECISION is not only available at local distributors now, but it has all of the most frequently needed features. Thirty MHz response, 2mV division sensitivity and rectangular CRT assure that the 1530 will handle the requirements of most engineers involved in digital and microprocessor circuit development. High-triggering sensitivity and very-flat frequency response also allow the 1530 to be useful well beyond its rated bandwidth.

Five ranges of time-base delay from 1nS to 100mS highlight this new instrument. The delayed-sweep capability of the 1530 is a major advantage in the evaluation of digital pulse trains and other complex waveforms. Complex signals can be expanded by as much as 1000 times for examination of signal components and troublesome "glitches." The absolute minimum magnification is 5 times at frequencies to 30MHz. The delayed-sweep feature is also useful in the measurement of rise and fall times of pulse signals.

For highest display accuracy, the 1530 offers a variable hold-off function. This ensures triggering at the first pulse of a multi-pulse signal, preventing improper waveform display. The 1530 can also display two signals that are unrelated in frequency by alternately triggering on both the channel A and B signals.

Other convenient features include a FIX mode to eliminate trigger level adjustments, differential input capability, single sweep operation, selectable triggering filters and a built-in video sync separator.

If you're looking for the kind of features and performance found in the 1530, but without delayed-sweep capability, B&K-PRECISION offers the 35MHz model 1535. While costing somewhat less than the delayed-sweep model, the 1535 is a high-performance instrument that doesn't sacrifice performance.

For immediate delivery, a 10-day free trial or in-plant demonstration, contact your local B&K-PRECISION distributor.

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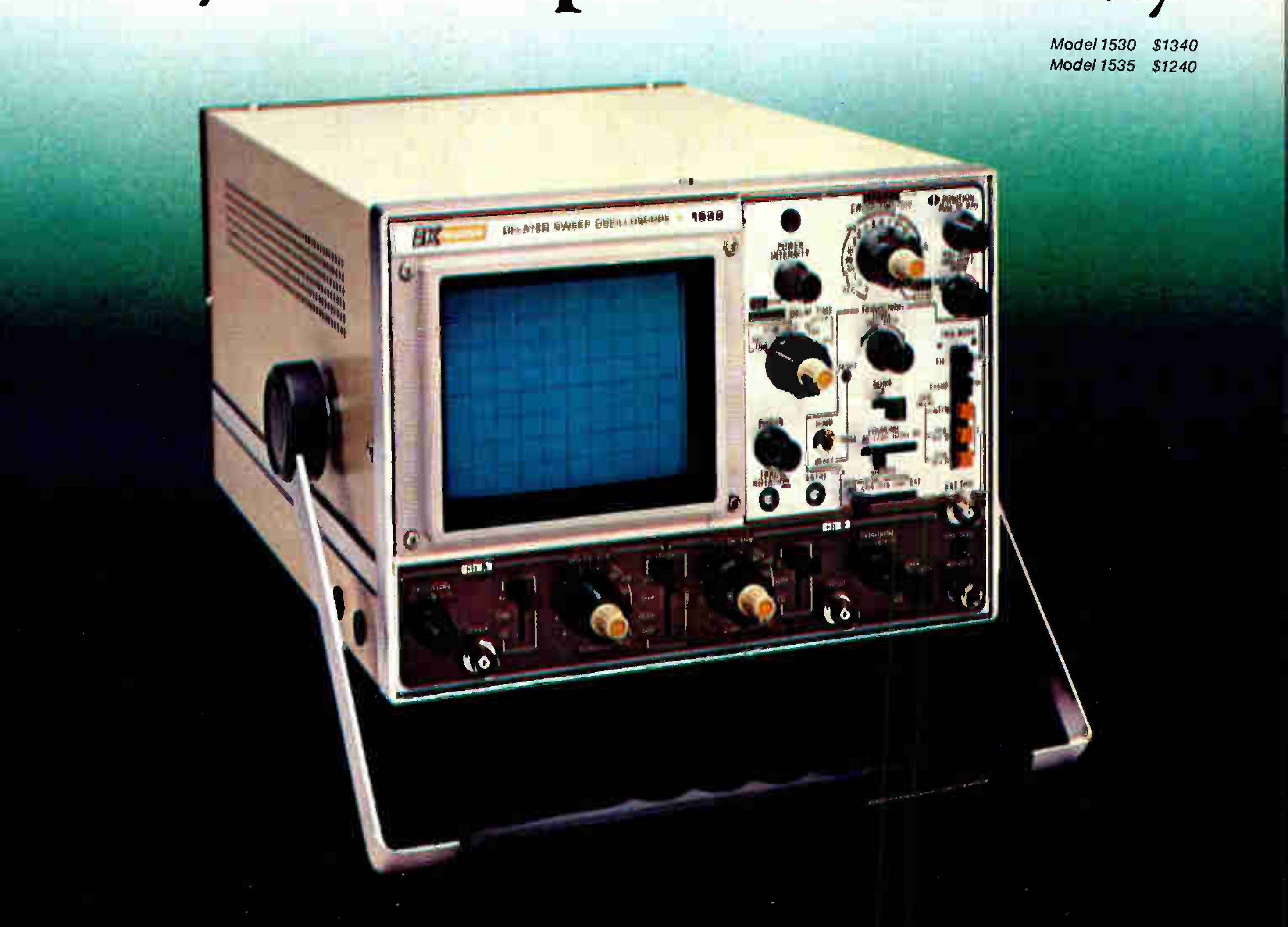

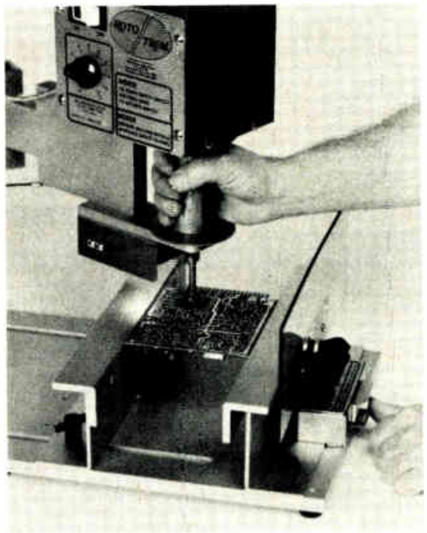

cantly lower cost than that of other machines currently available.

The Roto-trim has been specifically developed to take the place of hand-clipping component leads that extend through the bottom of printed-circuit boards after insertion and soldering. The machine consists of a base plate that measures 24 by 14 in., on which an upright column supports a moveable arm with two pivot points. At the end of the arm are a variable-speed motor, speed controls, and a power switch. The shaft of the motor is attached to a collar with precision bearings. The collar has an adjustable chuck holding a 0.25-in. rod brazed to a 1.25-in. diamond-ground carbide cutting blade. A board with components is mounted on a spring-loaded fixture and is held in place for trimming by extruded dovetail grooves.

Using a vertical adjustment feature, the operator may vary the blade's height from 0.5 in. to within 0.025 in. above the epoxy base of the printed-circuit board. To clip, the user presses down on the drive handle with one hand, while with the other, he presses a series switch. This safety feature ensures that both hands are away from the cutting blade. Then, using the drive handle to steer the cutting blade in any direction, the user trims the excess away from the component leads.

Among the advantages of this automatic clipping process is that the operator may selectively trim the

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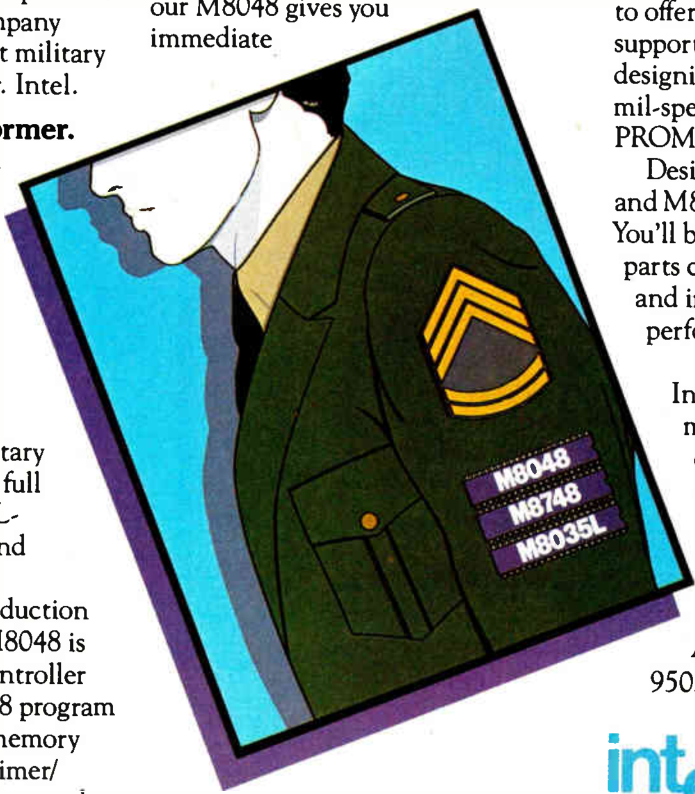

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leads while avoiding nuts, bolts, and other devices such as static-sensitive components. Also, the cutting operation takes only a few seconds, whereas hand clipping takes several minutes. The variable cutting speed accommodates copper, steel, or kovar leads, and the availability of optional warpage-correction jigs allows the user greater flexibility in loading boards. "It's 15 to 20 times faster than hand clipping," Baldwin notes, "with no damage to either the components themselves or to the leads."

Baldwin expects that most small circuit-board assembly sites will be able to afford the $1,695 unit. "Roto-trim can be used in any size shop manufacturing circuit assemblies," he observes. "The Roto-trim weighs about 135 lb and uses 120 v ac, so it's portable," says Wilbur A. Baldwin, president. "Most other such machines are much larger." The machine takes six weeks to deliver.

Roto Form Sales Corp., P. O. Box 188, Lake Grove, N.Y. 11755. Phone Bud Baldwin at (516) 586-2237 [399]

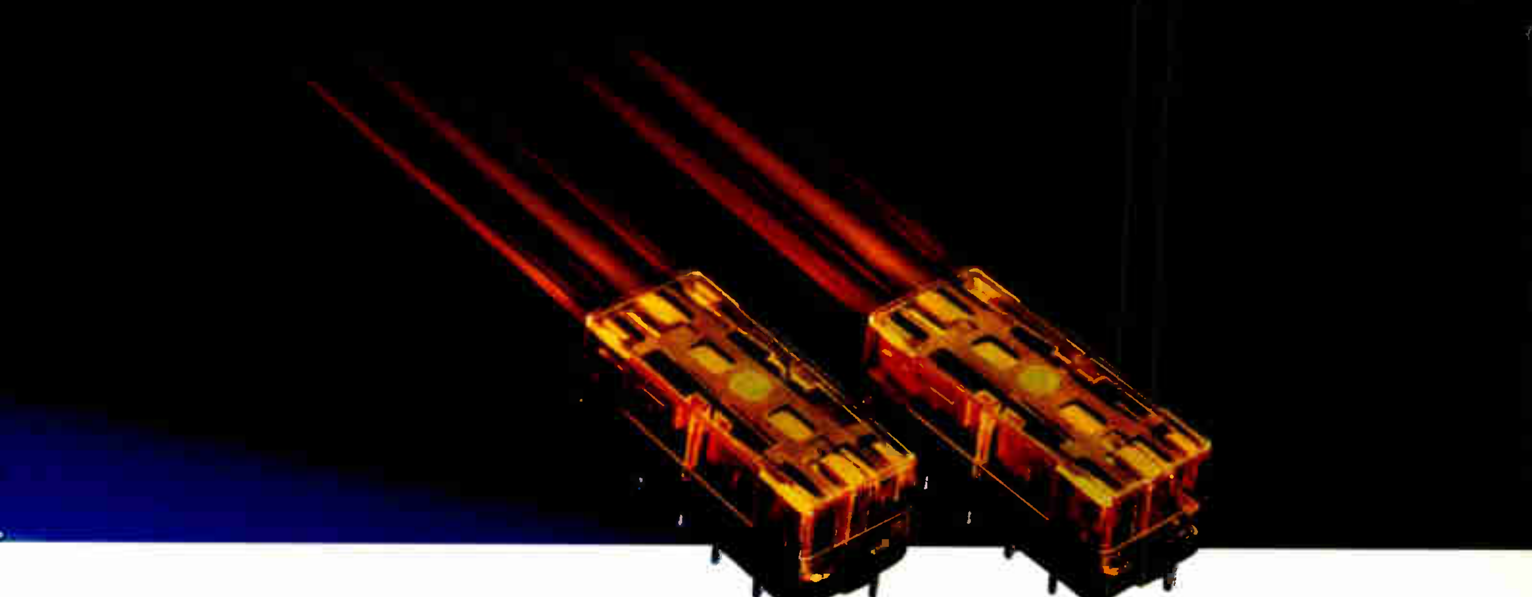
Zero is a plus in ZIF sockets

Sockets permitting easy insertion are becoming more important as devices gain leads. Aries Electronics Inc. will show its version of a zero-insertion-force socket at Electro. The ZIF socket comes in 24-, 28-, 40-, and 64-pin sizes, with either tin- or gold-plated contacts.

The company stresses that the ZIF sockets are not low-insertion-force sockets, but true zero-force types. The sockets feature heat-treated beryllium-copper contacts that are normally open. With a unique cam action—similar to the movement of an automotive camshaft—the contacts grip on the smooth flat surface of the integrated-circuit leads. The last 15° of movement of the cam provides a sliding action on the leads, thereby removing any residue

Aromat SE Amber Relays... a pure product of "relay efficiency."

$$\text{Relay efficiency}(\eta) = \frac{\text{The sum of all contacts' switching capacity (VA)}}{\text{Operating power(W)} \times \text{Volume}(cm^3)}$$



A breakthrough in relay efficiency.

The SE Amber relay's key to higher efficiency lies in greater miniaturization coupled with high reliability and greater switching capacity.

- **High sensitivity in small size.**
  [Operating power (W) x Volume(cm^3)]
  The SE Amber relay's 4-gap balanced armature delivers a highly efficient polarized magnetic circuit–sensitive enough to be driven directly by an IC, in a space 28L x 12W x 10H mm.

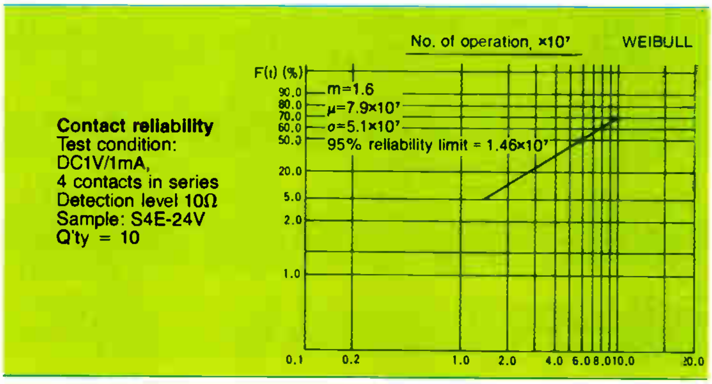
Sensitivity

Pick-up power	100 mW
Nominal operating power	200 mW

Dimensions

Volume	28L x 12W x 10H mm	1.102 x .472 x .394 inch
Header area	336mm²	.521 inch²
Height	10mm	.394 inch

- **Wide switching range.**
  [The sum of all contacts' switching capacity (VA)]
  Switching is possible from 100μA 100mV DC to 4A 250V AC, thanks to the 4-gap balanced armature system and special multi-layer clad contacts. A single SE relay can handle maximum and minimum switching simultaneously.
- **High reliability and long life.**
  The balanced armature system with permanent magnets gives larger contact pressure. Bifurcated contacts and lower contact bounce add to contact reliability and expected contact life.
- **Amber design and construction.**
  Designed for automatic wave soldering and cleaning, the sealed SE Amber relay performs reliably under conditions where hydrogen sulfide, silicone and ammonia fumes prevail.
- **High vibration/shock resistance.**
  The balanced rotating armature provides great resistance to shock and vibration. Vibration resistance: 10 to 55G (amplitude: 3mm) Shock resistance: 50G (11msec.).
- **Varied contact arrangement.**
  SE relays are available with bifurcated contacts in 2a2b and 4a contact arrangements.
- **Multiple latching.**
  2-coil latching types are available, in addition to single side stable types. Single SE relays have a latching capability with multiple contacts, one contact can control the circuit while the other can switch the load simultaneously.
- **Low thermal electromotive force.**
  Because the SE relay has completely separate coil and contact chamber areas, extremely low thermal electromotive forces are possible.
- **Dual in-line package arrangement.**
  This 2-track terminal arrangement allows easier component insertion, easier layout and identification of terminal locations, and simpler in-line checking.



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built up during storage or plating. A tapered entrance guides the leads as the device is moved into position.

The body of the socket consists of 30% glass-filled thermoplastic; it is available with solder tails in sizes of 24, 28, or 40 pins on 0.600 centers, and 64 pins on 0.900 centers. Measuring 0.450 by 0.790 in., the socket can be used for many different applications with electrical or mechanical devices such as solenoid or pneumatic actuators. No special tools have to be used in order to insert the integrated circuits.

The sockets range in price from $2.50 to $8.00, depending on size and quantity, with delivery in four to eight weeks.

Aries Electronics Inc., Box 231, Frenchtown, N. J., 08825. Phone (201) 996-4096 [400]

Connectors are resonance-free

A family of 3.5-mm high-performance precision microwave coaxial connectors features resonance-free performance up to 34 gigahertz and sells for under $20 each in large quantities. No system redesign is necessary to use the rugged APC-3.5 since it mates directly with SMA connectors.

Key to the electrical performance of the APC-3.5 is its air dielectric interface. The center contact is supported by a close-tolerance bead dielectric, together with precision tolerance machining of the beryllium-copper alloy connector body to yield the resonance-free performance. The unit's .020-in. outer conductor shoulder can take hundreds of matings without damage or loss of repeatability.

Available now are a plug and jack for 3.5-mm rigid air line; plug, jack, and panel jack for .085 semirigid coaxial cable; plug, jack and panel jack for .141 semirigid coaxial cable; and panel jack launcher.

Amphenol North American Div., Bunker Ramo Corp., 33 East Franklin St., Danbury, Conn. 06810. Phone (203) 743-9272 [403]

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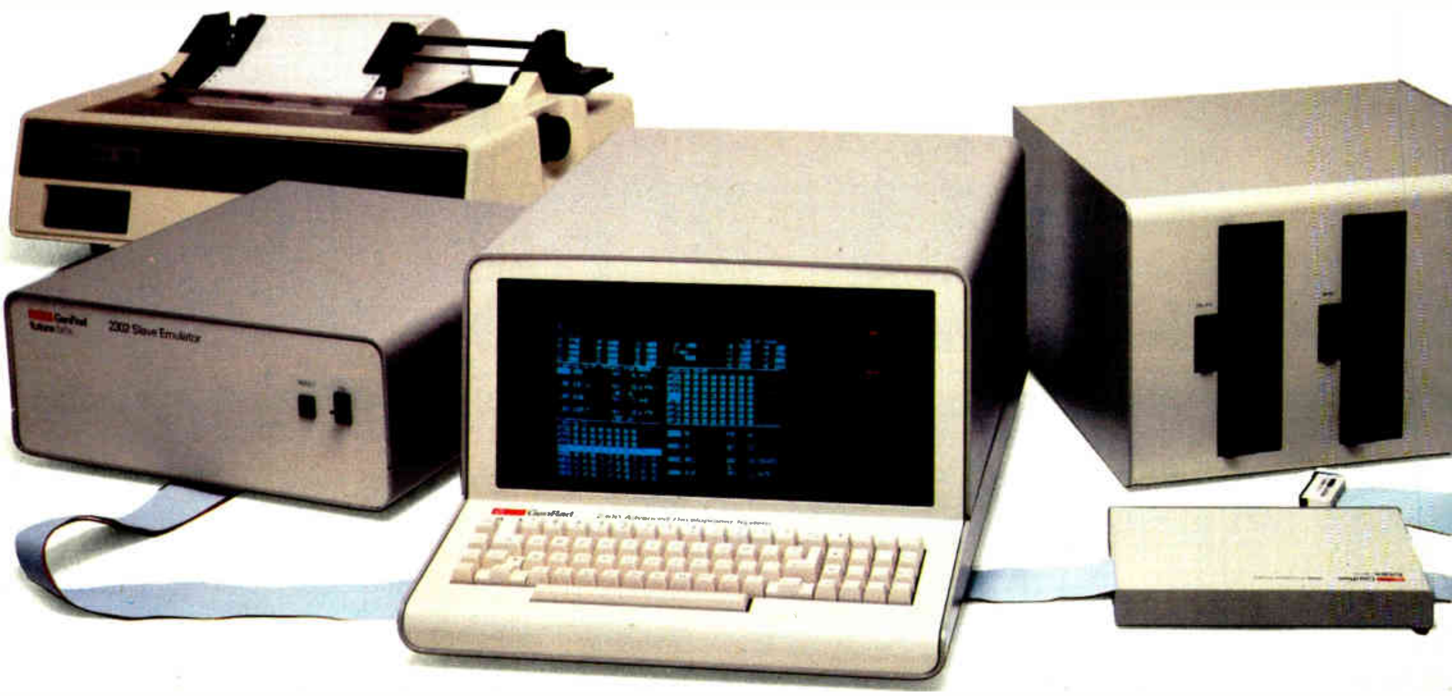
Thanks to our unique slave emulation system we can add new chips to your system in a matter of weeks. Remember, we don't make the chips – just the development system. And we don't have to redesign our system for each new chip – we just add another slave emulator. And, that's all you pay for. So, we're faster and more economical, too.

WE SET THE PACE FOR EMULATION

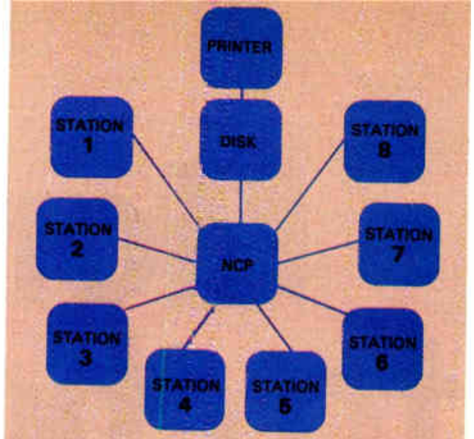
Ours is the only system capable of delivering transparent, non-stop, full-speed emulation



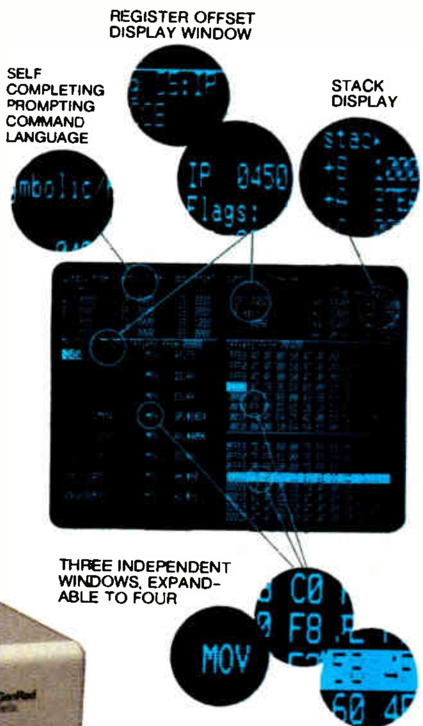
to 10 MHz. And it's the only system capable of emulating many different processors simultaneously.

Transparent, non-stop, full-speed emulation takes all the guesswork out of choosing the right microprocessor for your application. It allows you to evaluate each chip thoroughly, accurately and objectively.

The ability to emulate several different chips simultaneously paves the way to development of smart products using more than one processor.



2300 Series multi-station networks share disk and printer with up to eight stations. Each station is universal and may be ordered with the software and/or hardware capabilities required.



TYPICAL 8086 SNAPSHOT

The 2302 Slave Emulator allows you to view your program in single-step, snapshot or logic analyzer modes. This view can be formatted to match your requirements even for the most complex memory segmentation, interrupt-driven or multi-processor environments.

WE KEEP YOU IN THE FAST LANE

Our system has been designed to make hardware and software development fast, efficient and productive. With our high-speed CRT, high-level language programming and powerful software, things happen fast – sometimes instantaneously. Now available with highly block structured PASCAL compilers, our system can cut your programming time by 50% or more.

WE DELIVER THE MOST COST-EFFECTIVE SOLUTION

Lower initial cost, universality and expandability make our system a prudent, long-term investment. Any of our systems can be upgraded to network status. By sharing costly and under-utilized resources (disks, printers, emulators, analyzers and even software) you can stop paying your designers to stand in line. Networking can lower your cost-per-station by 20% or more.

WE'RE HERE TO STAY

There is no finish in the smart-product race. To stay ahead you're going to need flexible, productive, expandable development systems and a supplier with staying power capable of giving you in-depth, after-sale service and support. Ask for a demonstration of the 2300 Series Advanced Development System. Sales and service offices in major cities.

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GenRad/Futuredata universal development systems – expanding your world of microprocessor-based design.

Circle 197 on reader service card

More reasons to choose CMOS over NMOS.

RCA Microprocessor Development Systems make designing with CMOS easier than ever.

COSMAC DOS Development System. Includes a chassis with 28K RAM, dual drive floppy disk, Disk Operating Software, plus utility programs and extensive documentation.

High Level Languages. In addition to microFORTH, we're adding a Basic 1 Compiler/Interpreter and PLM 1800 Compiler.

Designers everywhere are learning of the advantages of CMOS over NMOS for their mircroprocessor designs.

Advantages such as low heat generation, low power drain, high noise immunity, wide operating temperature range and wide power supply voltage range.

Now, RCA is adding still more benefits to our 1800 series.

We're adding three new timesaving development tools to our already substantial line.

New Disk Operating System.

On the hardware side, we're introducing our new COSMAC DOS System (CDP 18S007). This new system is a powerful development and prototyping tool for designing hardware/software systems with our 1802 microprocessor and RCA Microboards.

If you have our CDP 18S005 Development System, we also offer an upgrade package CDP 18S837 with Disk Operating Software and other accessories that gives your older model operating capability equivalent to our new DOS system.

High Level Languages: PLM and BASIC. On the software side, we've developed two new packages designed to operate on our new DOS development system.

Designed for the experienced programmer, our new PLM-1800 Compiler (CDP 18S839) is the most powerful structured programming tool available for 1802 designs.

If you're designing in BASIC, our Basic 1 Compiler/Interpreter package (CDP 18S834) can both simplify and shorten your programs.

You can also use Basic 1 to compile programs into machine code for compactness and faster program execution in your final design.

A go-anywhere Micromonitor.

Here's a portable development tool that works as well in the field as it does in the lab. Our acclaimed COSMAC Micromonitor (CDP 18S030).

The Micromonitor is a complete diagnostic and design tool, capable of real-time, in-circuit hardware and software debugging, factory checkouts and field testing.

CMOS Evaluation Kit: $350.

For just $350 (optional with distributors), the CDP 18S025 gives you everything you need to build a microprocessor evaluation system: CPU, RAMs, ROMs, I/O, passive components, p.c. board, hardware, even a fully assembled microterminal.

You can use the kit to learn about basic system design, hardware interfacing and programming.

Other timesavers.

Additional RCA development tools include: a Micromonitor Operating System software package, fixed point and floating point arithmetic subroutines, a PROM programmer. And even more design aids are in the works.

Plus, 36 RCA "Systems Appointed Distributors" offer technical assistance, systems demonstrations and off-the-shelf delivery.

A complete list of Systems Appointed Distributors appears on the following page.

For more information on our broad line of development tools for the RCA 1800 series, contact your local RCA Solid State Distributor.

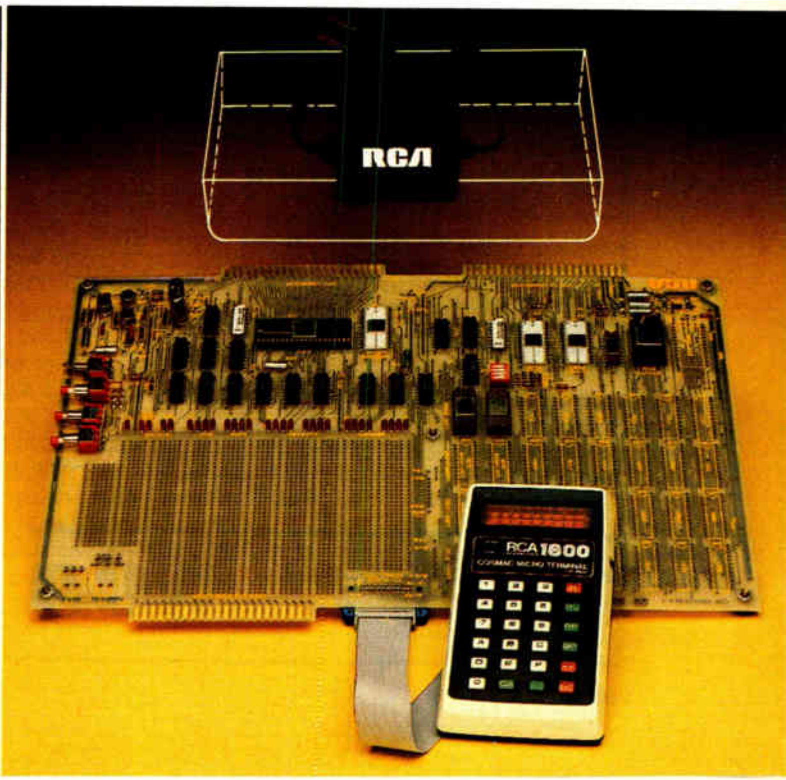
Or contact RCA Solid State headquarters in Somerville, New Jersey. Brussels, Belgium. Or Tokyo, Japan.

RCA

Circle 199 on reader service card

Portable Micromonitor. Our Micromonitor is a powerful, portable 1802 microprocessor real-time, in-circuit hardware/software diagnostic tool. Yet it weighs only 16 pounds.

Low cost Evaluation System. To see how compact our CMOS systems can be, compare our Evaluation Kit power supply with a typical NMOS supply (white outline).



They've got all the power and versatility you need to make your wildest product dreams come true. They're already the fastest growing microprocessor family.

And we'll keep adding superior new members. So you can add futuristic features to dazzle your customers and zap your competitors.

Some innovative newcomers include the brainy, omnipotent S6809. Our screen star, the cost-cutting S68045 CRT controller. Our low cost single chip MCU, the S6805. And the fastest MPU in this league, our 2.5 MHz S68H00. This isn't just a bunch of individualists, either. They're part of the stellar AMI system. Instead of merely selling you parts, we'll look over your present design and, if we can, show you how to cut out some components with a custom peripheral. Or work out a more streamlined

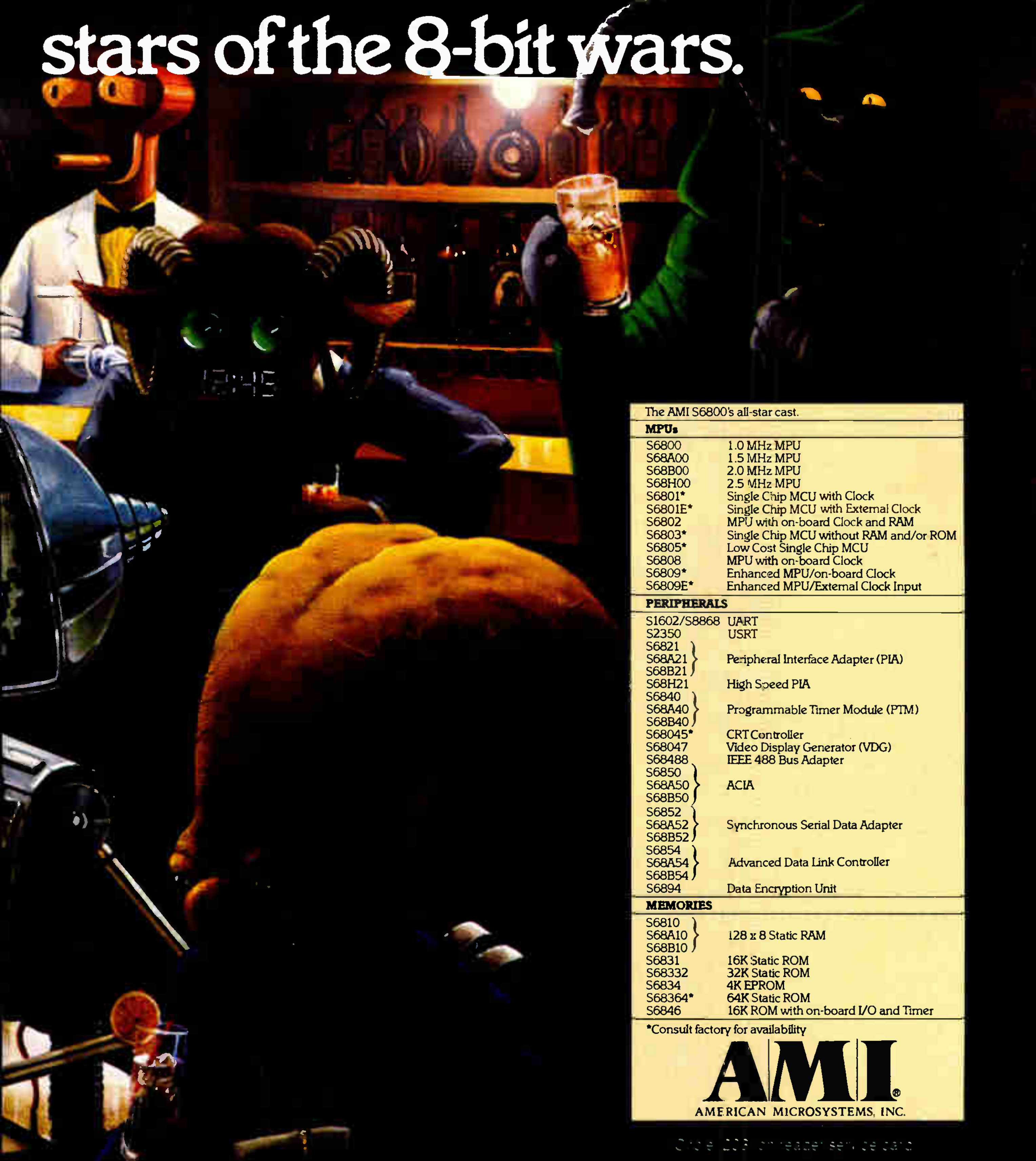
Meet the AMI S6800 Family:

S6800 system, including both standard and custom parts. Perhaps even customizing the MPU.

And there's another way the S6800 can make you a winner. Turn to the next page and enter our "name the family" contest. If you have any questions, call your nearest AMI distributor. Or contact us at AMI S6800 Marketing, 3800 Homestead Road, Santa Clara CA 95051. Phone (408) 246-0330.

However far-out your plans are, our family will make light work of them.

stars of the 8-bit wars.



The AMI S6800's all-star cast.

MPUs	
S6800	1.0 MHz MPU
S68A00	1.5 MHz MPU
S68B00	2.0 MHz MPU
S68H00	2.5 MHz MPU
S6801*	Single Chip MCU with Clock
S6801E*	Single Chip MCU with External Clock
S6802	MPU with on-board Clock and RAM
S6803*	Single Chip MCU without RAM and/or ROM
S6805*	Low Cost Single Chip MCU
S6808	MPU with on-board Clock
S6809*	Enhanced MPU/on-board Clock
S6809E*	Enhanced MPU/External Clock Input
PERIPHERALS	
S1602/S8868	UART
S2350	USRT
S6821, S68A21, S68B21	Peripheral Interface Adapter (PIA)
S68H21	High Speed PIA
S6840, S68A40, S68B40	Programmable Timer Module (PTM)
S68045*	CRT Controller
S68047	Video Display Generator (VDG)
S68488	IEEE 488 Bus Adapter
S6850, S68A50, S68B50	ACIA
S6852, S68A52, S68B52	Synchronous Serial Data Adapter
S6854, S68A54, S68B54	Advanced Data Link Controller
S6894	Data Encryption Unit
MEMORIES	
S6810, S68A10, S68B10	128 x 8 Static RAM
S6831	16K Static ROM
S68332	32K Static ROM
S6834	4K EPROM
S68364*	64K Static ROM
S6846	16K ROM with on-board I/O and Timer

*Consult factory for availability

AMI®
AMERICAN MICROSYSTEMS, INC.

Circle 203 on reader service card

Standard ECL chip has custom look

Devices on 8-bit ALU are interconnected by first-layer metalization for low-cost customizing

by Larry Waller, Los Angeles bureau manager

For its first standard emitter-coupled logic part to spin out of the semicustom MECL 10,000 Macrocell array line, the Motorola Semiconductor Group has settled on an 8-bit parity bit-slice arithmetic and logic unit. Called the MC10900, it is 8 bits wide, sliced parallel to data flow, and expandable to larger word lengths by connecting circuits in parallel.

The ALU takes advantage of the Macrocell development, in which a customer specifies logic functions to be configured on Motorola's basic ECL chip via a computer-aided design program. Devices on this chip are interconnected by first-layer metalization to create what amounts to a custom integrated circuit at much lower cost than that of conventional custom ICs.

Prospective buyers of the ALU slice therefore get the benefit of a custom-designed chip that already has proven itself, points out Jerry Prioste, systems engineer for Motorola's bipolar large-scale-integrated and memory products in Mesa, Ariz. Most likely applications would be in mainframe computers, which need the blazing ECL speed, but minicomputers, test equipment, and signal processors are also good prospects. The typical propagation delay for an 8-bit addition is 8.6 nanoseconds; a two-part 16-bit adder has a 12.8-ns delay.

A major advantage of the MC10900, in Prioste's opinion, is that "all parity checking is done independently on the chip, which frees a user from doing it separately." On-chip circuits can detect any parity errors in incoming data by comparing the data with independent calculations by the ALU. Another feature of the Motorola part is its capability for 4-bit shifts in addition to the usual 1-bit shift, which saves going through the ALU four times, says Prioste. This is particularly useful in handling floating-point calculations.

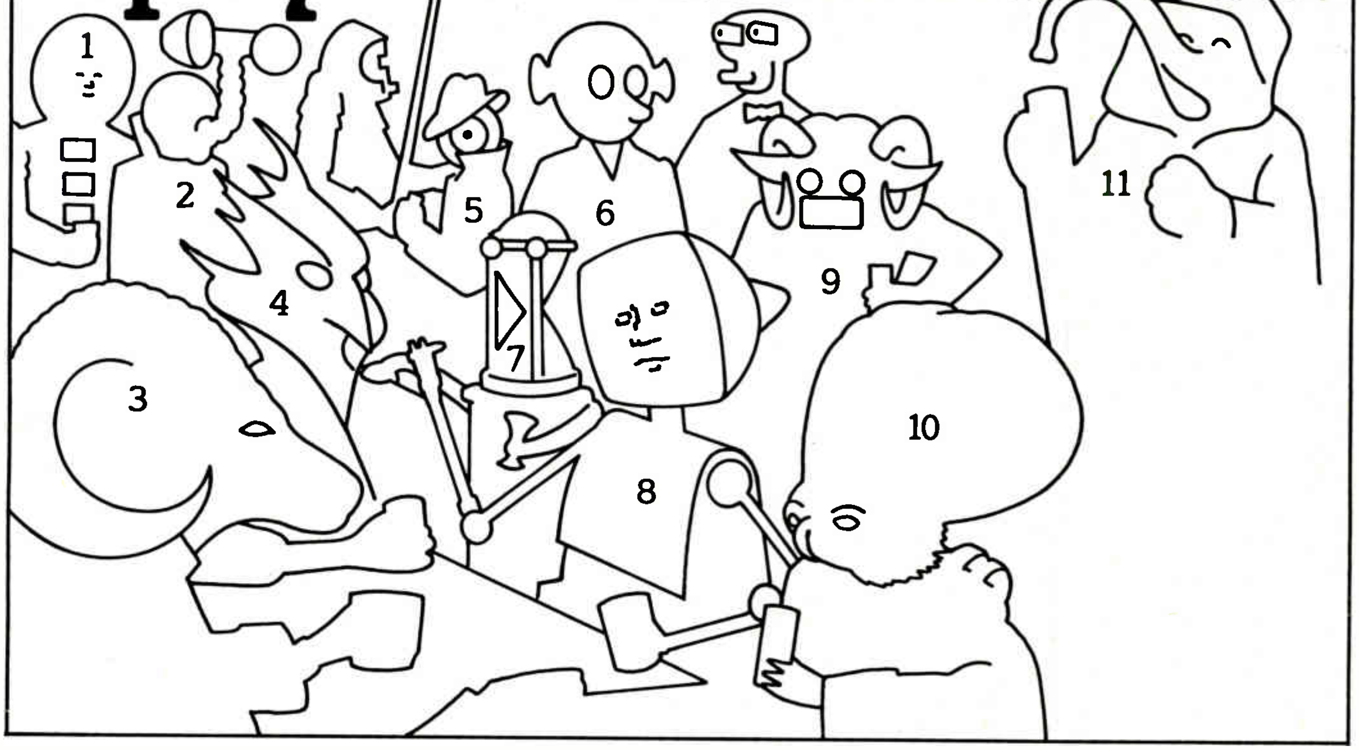
On the bipolar integrated circuit are logic functions, shift network, arithmetic logic, input/output latches, and parity-detect logic. Six select lines and three latch lines control all operations. The chip's features include performance of all logic and arithmetic operations; two input data ports; internal latches on input/output ports; internal look-ahead carry with propagate and generate outputs; status outputs for carry-out, zero detect, and parity-error detect; and internal carry signal for overflow detect.

The ECL chip has typical power dissipation of 3.1 W and 3.9 W maximum. The supply voltage specification is −4.68 to −5.72 V dc, with functional operating temperatures of 0° to 70° C. Its output drives 50 Ω transmission lines. Operation is based on an air flow of 500 linear feet per minute.

The MC10900 is packaged in a 68-pin leadless case that measures 0.695 in. square. It has an introductory price of $100 in quantities of 100 and is available in sample quantities.

Motorola Semiconductor Group, Bipolar Integrated Circuits division, 2200 West Broadway Rd., Mesa, Ariz. 85202. Phone (602) 962-2857 [339]

It pays to call us names!



That's right. You come up with the best names for our way-out S6800 family members, and we'll come up with some super prizes.

In fact, by just sending in the coupon, you can get a colorful 23" x 34" reproduction of the original oil painting used in our ad.

But, by playing the game, you can also win:

FIRST PRIZE: Millennium System's Microsystem Emulator™ with the S6802 Emulator and Real Time Trace.

SECOND PRIZE: Your choice of Atari® 800™ Personal Computer or an Apple® II Plus Systems (Personal Computer).

THIRD PRIZE: An Atari® 400™ Personal Computer System.

FOURTH THROUGH FOURTEENTH PRIZES: Hewlett-Packard's HP 31E Calculators.

Here's all you have to do to win. First, identify all the characters by their AMI part numbers. (You'll find them in our ad's chart on the previous page.) Then give each of them imaginative names like "Space Face," "Lame Brain" or whatever. The closer the name gets to describing the function of the part, the better.

The first three prizes will be awarded for the most creative list of names, taken as a whole. The next eleven prizes will be awarded for the best individual names. So first identify, then name the whole family, if you can. Then fill out the coupon and mail us the page.

The contest, which ends **June 6, 1980,** will be judged by a panel of S6800 Marketeers, and their decision will be final. And remember, you'll get a poster worth framing simply by sending in the coupon.

So call us some names soon. Before long, you could be a winner in the 8-bit wars.

ENTRY FORM

AMI part number	Your name for it
1.	
2.	
3.	
4.	
5.	
6.	
7.	
8.	
9.	
10.	
11.	

Name ____________ Title ________

Company ____________

Address ____________ M/S ________

City/State/Zip ____________

Phone ( ) ____________ Ext. ________

Contest is void where prohibited by law. AMI employees, representatives, distributors, vendors and their families are ineligible to participate. All entries become the sole and exclusive property of AMI.

SEND ENTRIES TO:
American Microsystems, Inc.
S6800 Contest
3800 Homestead Road
Santa Clara CA 95051

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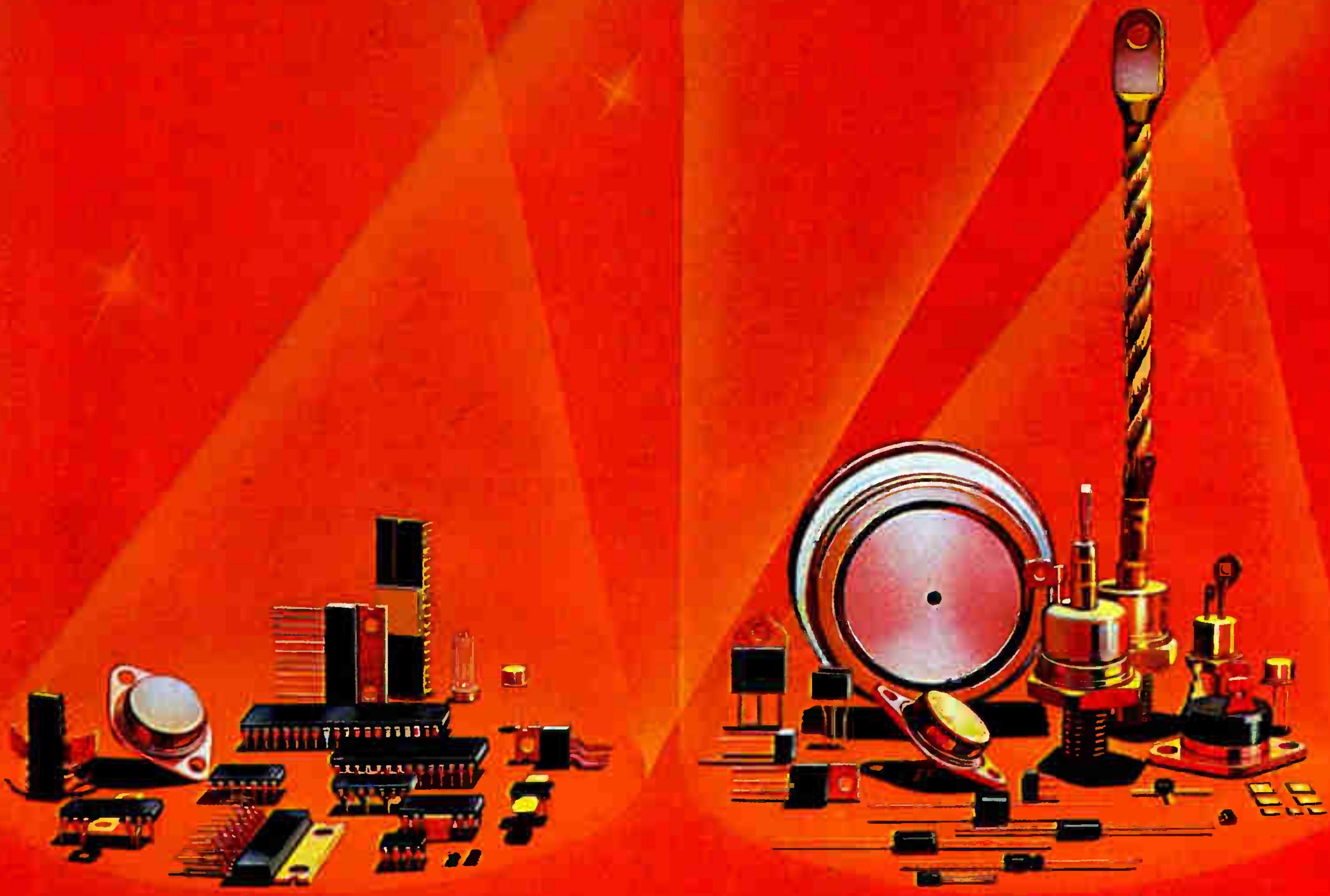


Controller handles floppies, fixed disks

Intelligent unit with on-board data separator can control four drives, relieves CPU of many disk-control tasks

Bruce LeBoss, San Francisco regional bureau manager

Providing a middle-of-the-road answer to the microcomputer and minicomputer systems design debate over floppy versus fixed Winchester disk drives is Shugart Associates' microprocessor-based disk controller with on-board data separator logic that can control four drives. These can be combinations of the firm's Winchester and floppy units. It will also relieve designers of the task of putting together a discrete controller.

The SA1400 controller family is based on Advanced Micro Devices Inc.'s 2900 bit-slice microprocessor. This firmware relieves host computers of many disk-control functions.

Among the significant intelligence features are automatic copying of a block of data from a source logic unit number (LUN) to a destination LUN, sector interleaving, and an error-correction scheme separate from the central processing unit.

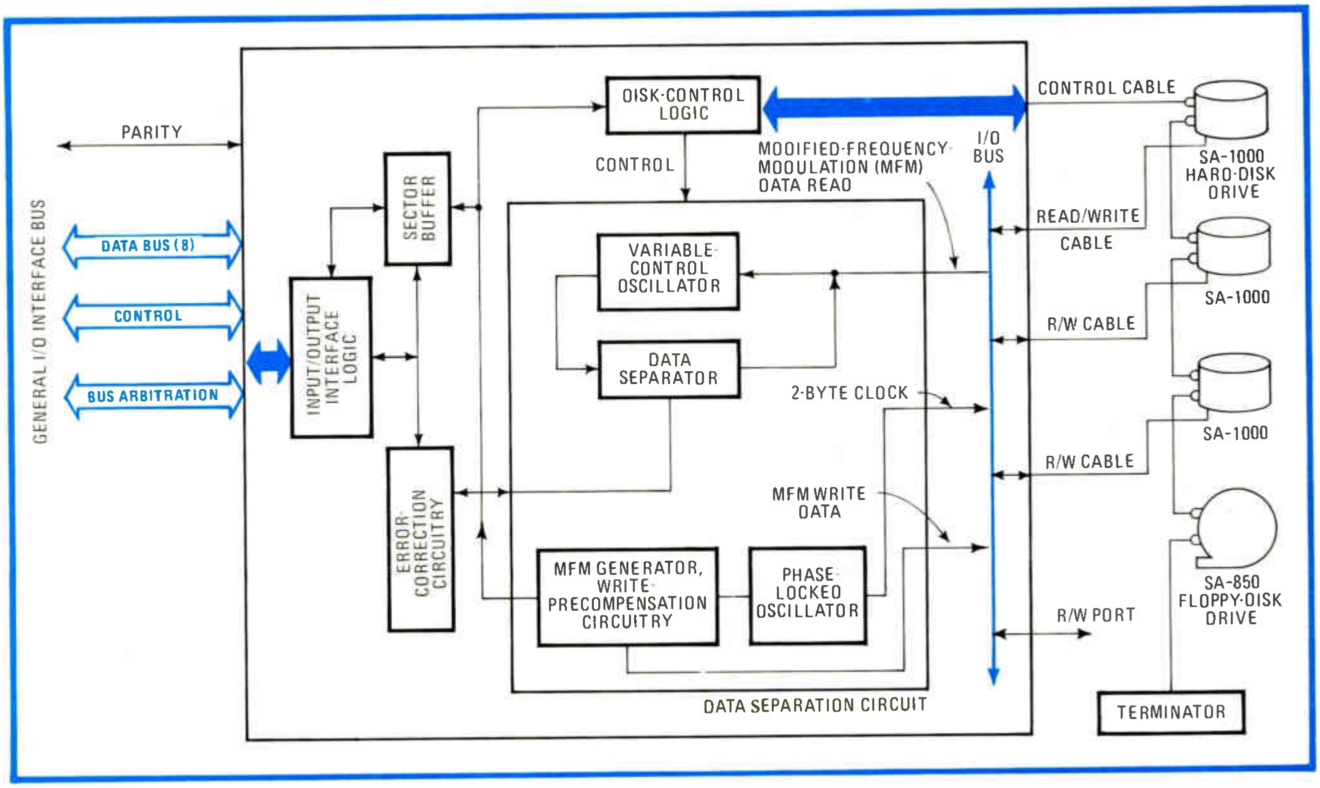
Copying from one disk to another may be carried out by the controller logic with no CPU involvement. Sector interleaving makes more efficient use of disk space and significantly improves system throughput. This technique also compensates for differing transfer rates when copying data between a Winchester disk and a floppy.

Shugart's standard SA800/850 floppy-disk protocol and either the 8-in. SA1000 or the 14-in. SA4000 fixed-disk protocols are used for the interface with the drive. A general-purpose interface is used to transfer commands and data between the host CPU and the controller.

The controller fits onto an 8.25-by-13.7-in. circuit board and will operate at +5 V at 4.6 A, −5 V at 500 mA, or +24 V at 100 mA. It will be formally introduced at the May National Computer Conference.

It is available now in five configurations that range in price from $995 for the SA1401, handling two SA1000 drives to $1,420 for the SA1406 and SA1407 for four 1000 or 4000 drives, respectively, plus a 0.25-in. 20-megabyte tape cartridge.

Shugart Associates, 415 Oakmead Pkwy, Sunnyvale, Calif. 94086 [340].




LOGIC ANALYZERS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FIXED LINEAR
ARRAY RECORDERS


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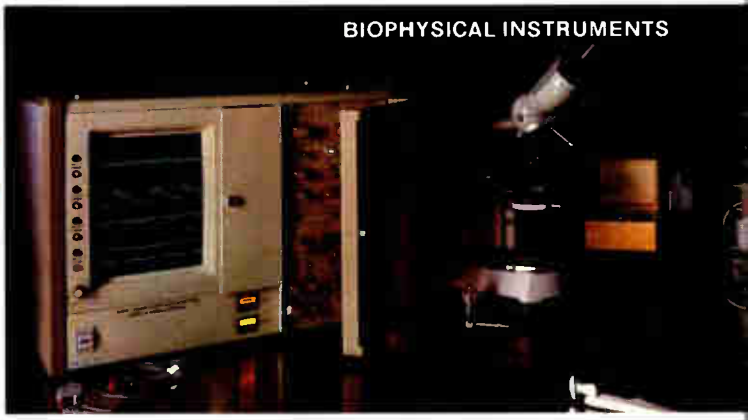
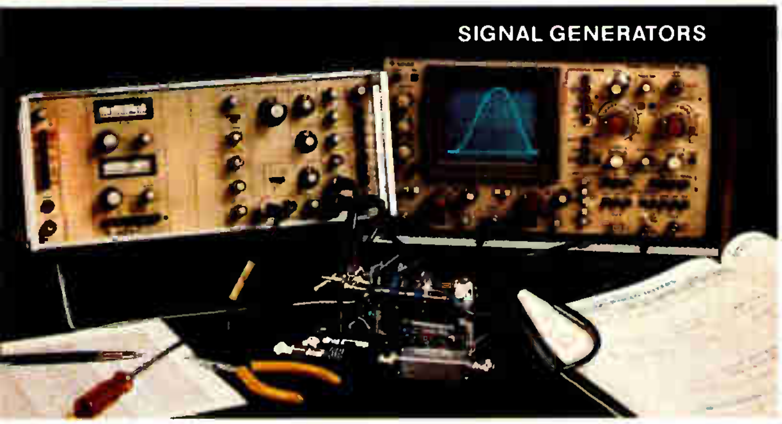
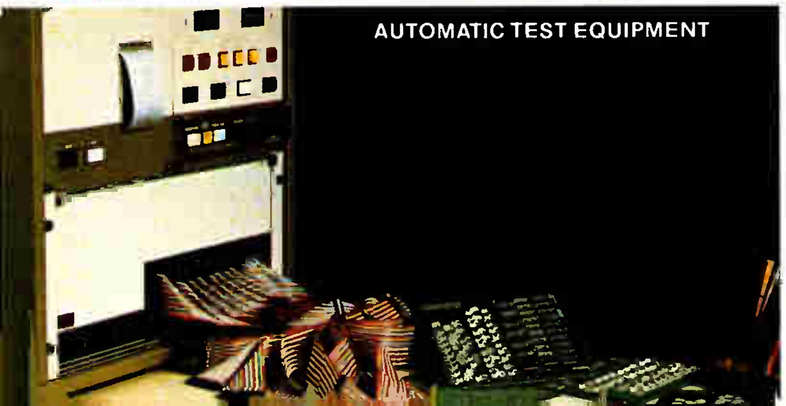

BIOPHYSICAL INSTRUMENTS


SIGNAL GENERATORS


DIGITAL COUNTERS/MULTIMETERS


AUTOMATIC TEST EQUIPMENT


ANALYTICAL
INSTRUMENTS

Microcomputers & systems

LSI 11/23 gets analog boards

Two boards allow users of the new microcomputer to digitize low-level inputs

Two analog boards from ADAC Corp. allow users of Digital Equipment Corp.'s new LSI-11/23 microcomputer to digitize low-level, slow-varying millivolt and thermocouple inputs in a wide range of industrial-control, laboratory-measurement, and data-acquisition applications. The 1113 series boards also are compatible with DEC's LSI-11 and LSI-11/2 microcomputers, fitting directly into system buses.

The 1113AD module contains an analog-to-digital converter, a software-programmable gain amplifier with automatic zeroing, and six gain settings for full 12-bit resolution over bipolar ranges of 10, 20, 50, 100, 200, and 500 mV. ADAC offers an optional programmable read-only memory-based cold-junction-compensation circuit for direct interface of the board to standard thermocouples. Also optional is a dc-dc converter for users connecting the board to the computer-system buses via ADAC's backplane.

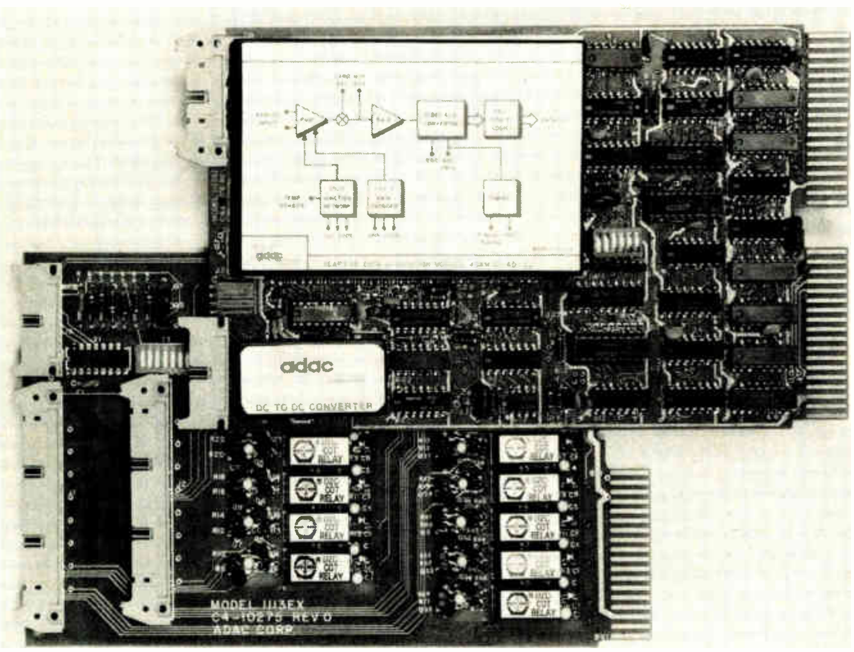
Operating with the 1113AD is an 8- or 16-channel companion board, the 1113EX. It contains a multi-reed, very low thermal electromotive-force flying-capacitor multiplexer for processing low-level analog inputs in electrically noisy environments. Common-mode isolation is good at 250 V, and common-mode rejection is 120 dB at 60 Hz. Up to eight 1113EX cards may attach to the daisy chain from any 1113AD board, letting the board accept differential low-level analog inputs from a maximum of 128 channels, at a rate of 200 channels/s. Minimum sampling time for each channel is 5 ms. The 1113EX also contains circuitry for the optional cold-junction compensation feature, and an eight-pole dual-in-line-package switch providing card selection for each 1113EX on a daisy chain.

Users can load the 1113AD's 16-bit, bus-addressable control status register to select operating modes. A-d conversion may take place under program control or be triggered by an external pulse generator or an onboard oscillator. Channel selection may be random or sequential. The 1113AD's bus interface can operate under program control, or using a multilevel program-interrupt scheme compatible with the interrupt structure of the LSI-11/23. In applications requiring direct memory access to the computer, ADAC's model 1620DMA module can work with the 1113 cards to transfer data directly into computer memory.

Both 1113 series boards are half-quad size, 5-by-8.5-in. cards able to fit on 0.5-in. centers in backplanes either designed for half-width boards or having Q-bus connection on one side only.

The 1113AD costs $495 per board, and the 8- and 16-channel cards are $500 and $800, respectively. Cold-junction-compensation capability is an additional $75, and the dc-dc conversion option is $100. The analog boards can be delivered in 30 to 45 days.

ADAC Corp., 70 Office Tower Park, Woburn, Mass. 01801. Phone (617) 935-6668 [371]



Z80 central processing unit zips to 6 MHz

Microprocessor applications that do not require full-blown 16-bit power but can benefit from more than run-of-the-mill performance from an 8-bit machine will be the prime candidates for Mostek's new souped-up Z80 central processing unit. Beginning May 1, the Carrollton, Texas, firm—which already builds 2.5-MHz and 4-MHz versions of the Z80 as a second source to Zilog Inc.—will make available samples of its latest Z80 device, which is specified to run at 6 MHz.

The new machine, designated the MK3880-6, will offer a 50% greater throughput than its 4-MHz predecessor and a 140% improvement over the 2.5-MHz device, Mostek officials say. The 3880-6 should be "an ideal candidate for system upgrades" in applications including communications, says Jim Booth, an applications engineer.

The n-channel MOS 6-MHz machine will require some ingenuity on

Quality you can count on: Gould direct writing recorders.

Quality features are built into every Gould 2000 series recorder to provide performance, versatility and reliability second to none.

Performance. You get it in unequaled frequency response in 1 to 8 channels across 40mm, 50mm or 100mm channel spans. Traces are crisp, clean, smudge-free at all pen velocities thanks to our exclusive pressurized ink writing system.

Versatility. It results from our modular design that will meet your present—and future—needs. More than 20 plug-in signal conditioners are available for each model so you can configure the recorder to meet your specific need.

Reliability. Proven Gould designs and high quality components and materials add up to reliability. Routine maintenance is minimal and easy with fast access to all major components.

Let us tell you more about the accepted leader in direct writing recorders—the quality Gould 2000 series. Contact Gould Inc., Instruments Division, 3631 Perkins Ave., Cleveland, Ohio 44114.

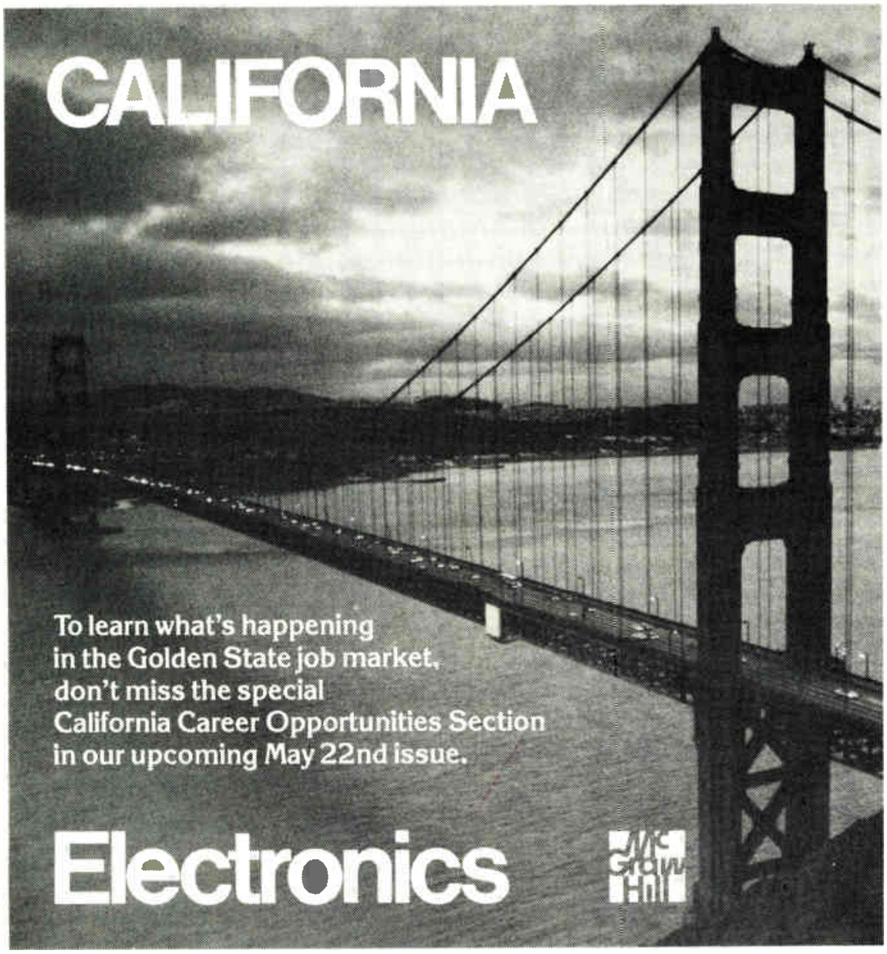
For brochure call toll-free: (800) 331-1000. In Oklahoma, call collect 918-664-8300.

In Europe, contact Gould Instruments S.A.F., 57 rue St. Sauveur, 91160 Ballainvilliers, France.

GOULD

An Electrical/Electronics Company

Circle 213 on reader service card



the part of the designers, Booth indicates, since it will execute too fast for currently available MOS read-only memories and programmable ROMs. For example, systems that currently make use of the 4-MHz CPU frequently utilize 2716-type memories, but to upgrade such a system to the 6-MHz central processing unit, techniques for downloading the 2716 to random-access memory for execution might be needed, Booth says.

No decision has been made on whether Mostek's family of five Z80 peripheral chips will also be offered in 6-MHz versions, says David A. Hayes, microcomputer components marketing manager. Depending on the application, a lack of 6-MHz peripherals to work with the faster CPU could reduce the throughput improvement, Mostek officials concede. But the 6-MHz Z80 CPU can be made to work with 4-MHz peripherals, they say, adding that customers contacted have indicated a willingness to work around any difficulties encountered in using the slower peripherals with the faster central processing unit.

Mostek support chips currently available in both 2.5- and 4-MHz versions include the MK3881 parallel input/output controller, the MK3882 counter timer circuit, the MK3883 direct memory access, and the MK3884 serial I/O controller. The MK3886 combo chip—a sole-source Mostek design that features a serial I/O port and two programmable timers on board with 256 bytes of RAM—is currently available only in a 2.5-MHz version but is expected in a 4-MHz version.

Prices for the 6-MHz chip are not yet available from the company.

Mostek Corp., 1215 W. Crosby Rd., Carrollton, Texas 75006 [372]

STD-BUS card gives TRS-80 development-system capacity

The XTD-TRS interface card, about half the size of an S-100 card, allows the TRS-80 computer to function as a development system for STD-BUS

The scope that never forgets.

Gould's digital OS4000 stores event data for the life of the scope. Solid state memory lets the Gould OS4000 give you instant replay of stored event data for as long as you need it (while the unit is getting power). In addition to the event itself, the OS4000 uniquely stores and displays what happened before the event and after it. The OS4000 can then expand the event display so you can study it in slow motion detail. Plus, it also allows you to compare delayed and original sweeps. And, when needed, the OS4000 can perform as a real-time scope with a bright, stable, flicker-free display

The Gould OS4000 is easy to operate whether it's being used as a digital storage or conventional oscilloscope, waveform recorder, transient recorder, comparator or signal generator. Interfaced with a recorder, the OS4000 can generate hard copy data from both ongoing events or 'replayed' displays.

For more information on the scope that out-remembers any tube storage scope on the market, contact Gould Inc., Instruments Division, 3631 Perkins Ave., Cleveland, Ohio 44114.

For brochure call toll-free: 800-331-1000 (in Oklahoma, call collect 918-664-8300).

GOULD

An Electrical/Electronics Company

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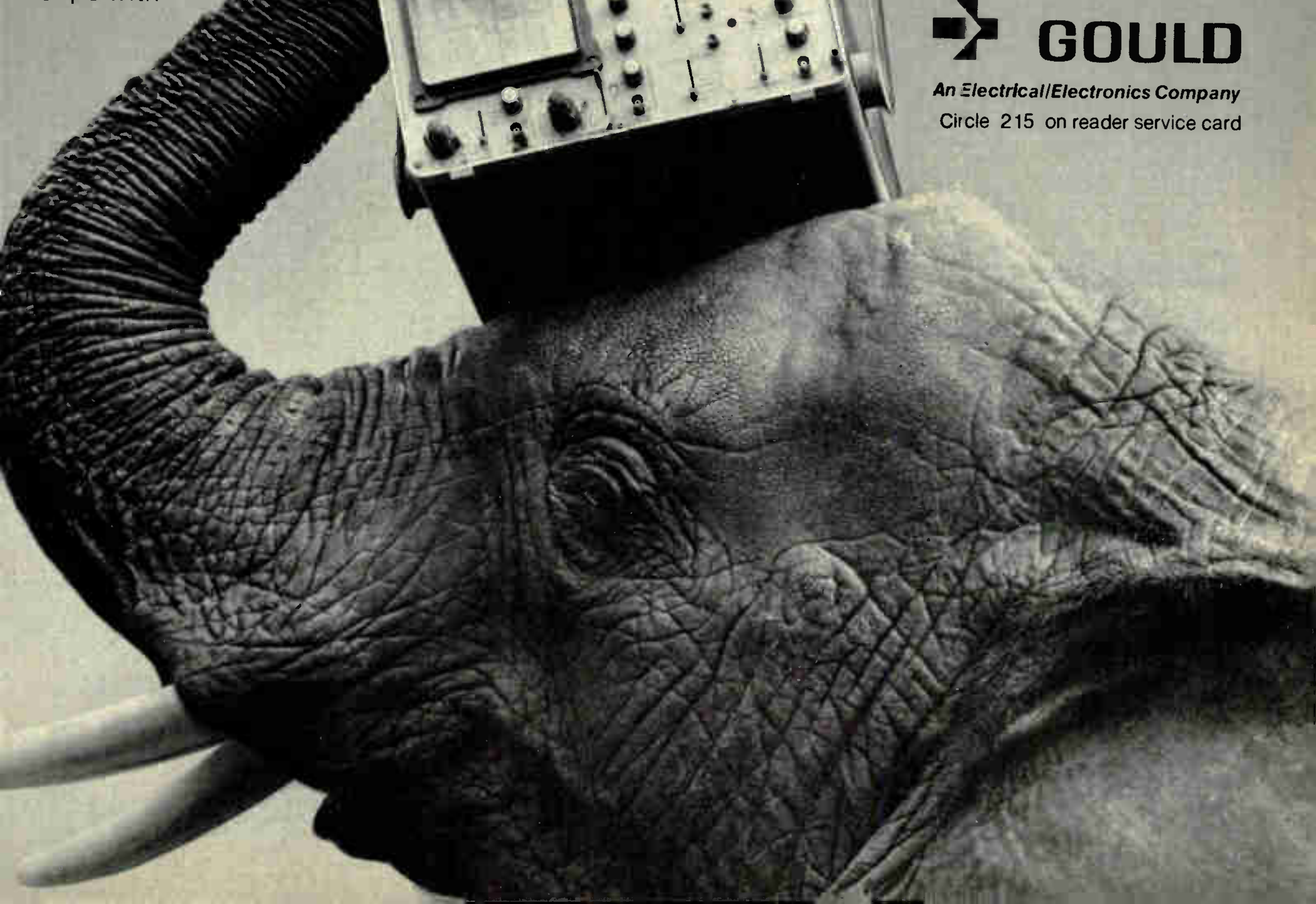


Check Beckman's specs before you select your source for Converters.

Beckman's Series 7580 and 7541 12-bit D/A converters replace the popular DAC 80 and 7541 pin-for-pin. But they offer better performance, use less power and are priced competitively.

Now *you* can write in better specs because *our* specs are better over a wide range of temperature and power supply variations. And Beckman converters offer much tighter end-point linearity specs than other manufacturers, resulting in better full-scale accuracy. Calibration is simpler, too. You need only to set zero and full scale once to fully calibrate your system.

You can also expect greater design flexibility because Beckman's CMOS DACs consume less power and are TTL and CMOS compatible.

Just as important, the 7580 and 7541 are competitively priced in both military and commercial versions. And they're available now–from stock.

Better performance, lower power consumption, greater design flexibility and competitive prices right from stock. Maybe you should check Beckman's specs. You might just find us to be your prime source for converter products.

For more information, contact your local Beckman representative or write: Advanced Electro-Products Division, Beckman Instruments, Inc., 2500 N. Harbor Blvd., Fullerton, CA 92634. (714) 773-7935.

Design Beckman converters in. Design problems out.

BECKMAN

Circle 216 on reader service card

products. With the XTD-TRS, Z80 firmware for STD-BUS applications may be assembled and edited on a floppy-disk– or cassette-based TRS-80 system, then transferred directly into the STD-BUS system for execution and debugging. In the debugging mode, the TRS-80 serves as the console device through which DDT-80 debugging firmware is accessed.

In addition, the card allows the TRS-80's input/output capability to be expanded through direct interfacing with such STD-BUS cards as analog-to-digital and digital-to-analog converters and industrial control products.

The $260 introductory price includes the circuit board with 2 kilobytes of read-only memory and an interface cable for connecting directly to either a TRS-80 keyboard or an expansion interface.

QC MicroSystems, P. O. Box 401326, Garland, Texas 75040. Phone (214) 343-1282 [373]

In-circuit emulator made for 8-bit microprocessor

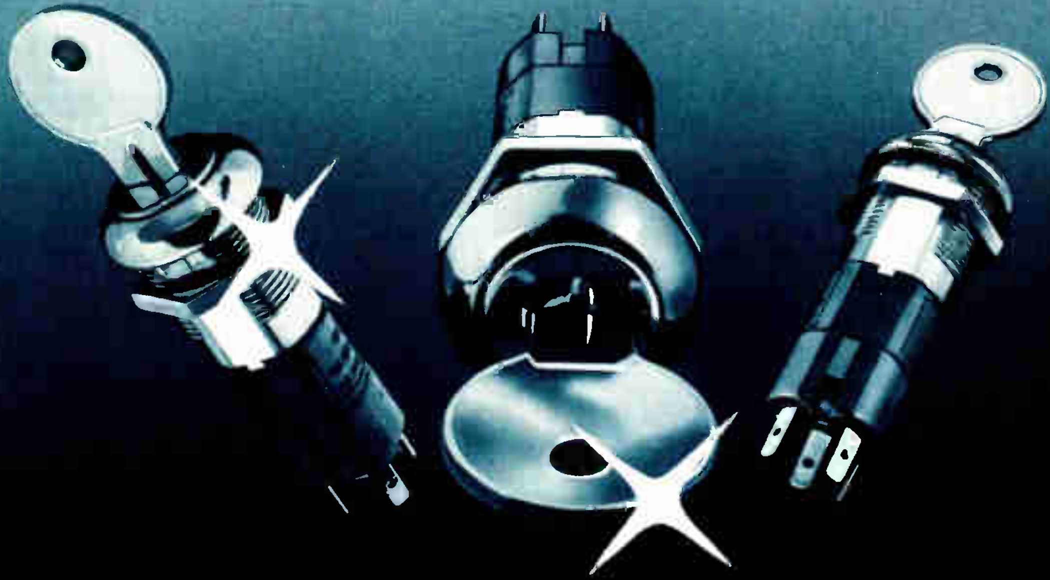
A new in-circuit emulation module for the Intel 8088 8-bit microprocessor, when combined with Intel's Intellec microcomputer development system and an 8086/8088 software development package, has full capability to develop and debug a user's application hardware and software.

The ICE-88 hardware links Intellec with a user's 8088 system through a buffer box and cable that replace the 8088 central processing unit during debugging and testing. The ICE-88 software contains commands that control the user's debugging session. It can disassemble the results directly from the user's program memory or from a trace of execution, thus converting the binary object code into assembly mnemonics, which are intelligible to the user. The price of the ICE-88 is $5,500, with delivery four to eight weeks after receipt of order.

Intel Corp., 3585 S. W. 198th Ave., Aloha, Ore. 97005. Phone Paula Kelly at (503) 641-8086 [376]

Protect data processing equipment against static discharge ...up to 20,000 volts

Oak Anti-Static Keylock Switch.



System error and logic circuit destruction is possible—and likely—from static discharge. As little as 500 volts will introduce impulses that can activate peripheral equipment. 2000 to 4000 volts can destroy MOS and IC's.

The potential of the human body due to static charge can easily exceed these voltages, under a broad range of conditions.

Eliminate this danger with the OAK anti-static keylock switch—and at the same time, provide security for your equipment. Available in a wide range of switching combinations, it reduces your costs by replacing the components normally needed for static discharge protection.

OAK DISTRIBUTORS stock the most popular types for immediate off-the-shelf delivery. For additional information, contact your OAK distributor, or OAK field sales office.

SPECIFICATIONS

- Circuit protection to 20,000V of static discharge with a good ground
- UL and CSA listed
- Rated at 3A@120VAC, 1A@28VDC
- Switching life, 10,000 operations minimum
- Measures only 2$\frac{1}{16}$″ deep, $\frac{3}{4}$″ diameter
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- Enclosed switching
- SPST, SPDT, SP3T, SP4T, DPST
- Wide range of key options

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Computers & Peripherals

Processor does data-base tasks

Back-end processor handles data base only, sells for $15,000 to $50,000

Instead of dedicating an entire general-purpose computer to data-base tasks, the makers of the IDM intelligent data-base machine have specialized the back-end processor. The IDM searches and compares the contents of a large data base for information, relieving its host central processing unit of those input/output-intensive functions.

This specialization has enabled Britton-Lee Inc. to market the IDM for between $15,000 and $50,000, depending upon options. "On strictly data-base applications, our IDM will outperform an IBM 370/168," claims company president Dave Britton. The good price-performance ratio of the new unit is the result of having separated the data-base tasks from the traditional general-purpose computer.

Aimed at the original-equipment manufacturer, the IDM can handle, multiple data bases containing up to 32 gigabytes of total capacity, with transaction rates of 2 to 25 transactions per second. Its SMD disk controller supports up to four disk drives. In its minimum configuration, the IDM has 256 kilobytes of random-access memory, but it is expandable in 256-kilobyte increments to a maximum of 3 megabytes.

The IDM has eight input/outputs that can accommodate up to eight programmable terminals using asynchronous communications. Using an IEEE-488 data link, the IDM can serve multiple host CPUs or intelligent terminals. Communication between the CPUs and the IDM is accomplished with relatively little effort on the original-equipment manufacturer's part. "If he already has a query language in his system, then we have given him 90% of what he needs for the interface," Britton asserts.

If the OEM does not have a query language, then he can use a high-level language like Pascal, Cobol, or Fortran to interface with the IDL query structure provided by Britton-Lee. The IDL language is identical in structure to the Quel and Sequel languages. It can be called up as a subroutine as a high-level language.

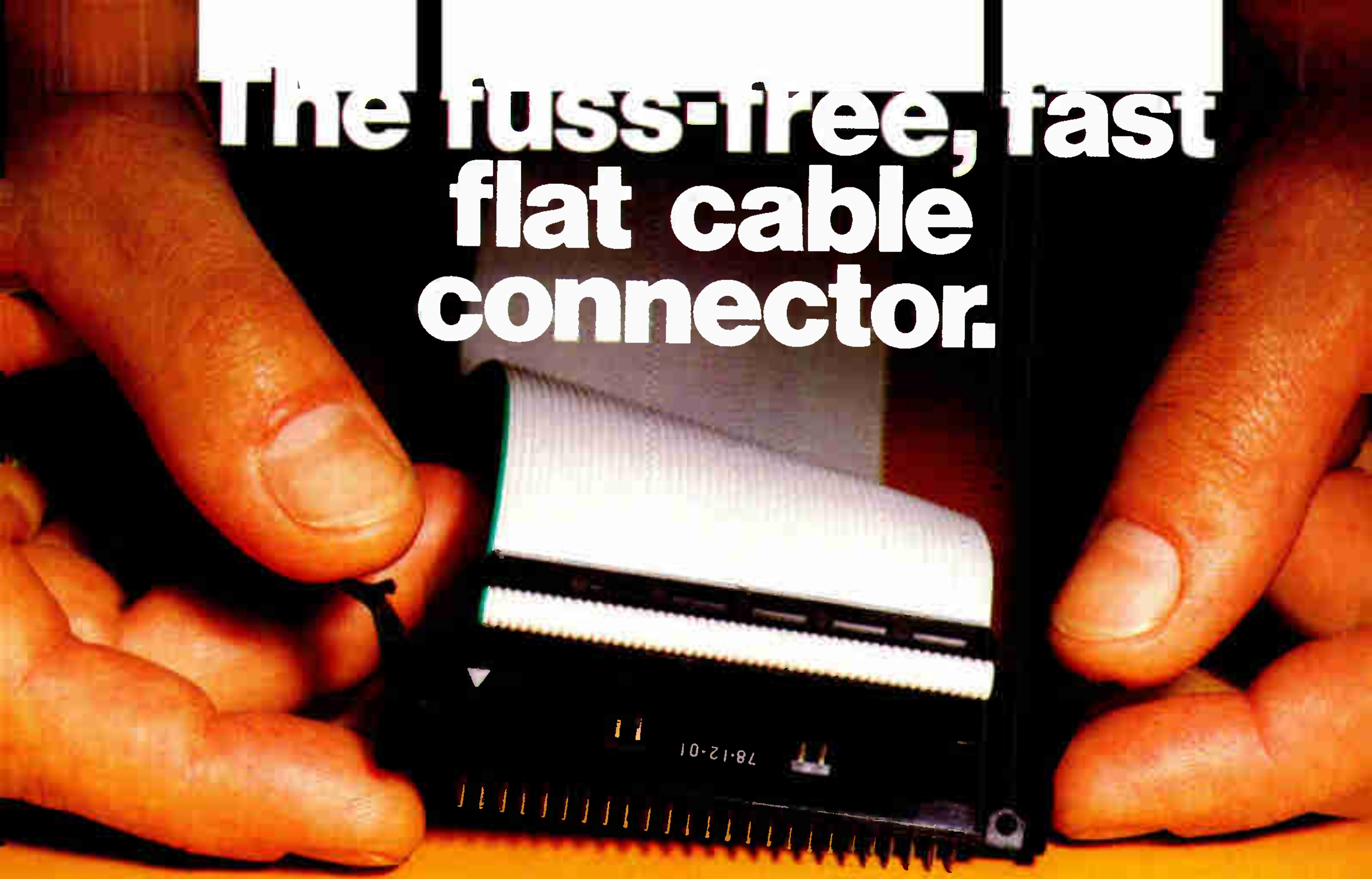
"The new result is a tremendous reduction in the applications software effort required of the OEM designer," notes Britton. "If his previous application took him 2 man-years, this will reduce it to a few man-months. If it was man-months, then it will become man-weeks." The user can also imbed the query language in the high-level language he is using.

Asynchronous communication. The IDM can also communicate directly with asynchronous intelligent terminals like Hewlett-Packard's 2645A, thereby eliminating the need for host computers altogether in systems oriented to the storage and retrieval of information. The data-base package included in the IDM contains such features as transaction management, concurrency control, and data-protection backup and recovery. Once formulated, an oft-used query can be stored and run again by supplying the query name plus the relevant parameters.

The IDM presents its information to the user as a relational data base. This is a table-driven cathode-ray-tube display in which the two axes represent the two factors being related. One advantage of data in a relational form is that it allows the user to make *ad hoc* queries. That is, it can call up new tables that have not previously been formatted, to show the relationship between two parameters. Another advantage is that the end user can create new data reports without the aid of a programmer.

The processing portion of the IDM uses both bit-slice processors and 16-bit MOS microprocessors. It contains both a data-base processor and an

The fuss-free, fast flat cable connector.



The new Amphenol® IDC Connector. Fuss-free because it locks when it mates. Fast because there's no wire stripping.

Simply insert the socket into the header and push gently. Click! The connector locks. No doubt about it. You heard it lock. You can see it's locked.

These connectors also have integral polarizing keys. There is no chance of mismating.

To unlock, just flip the ears and pull the connector apart.

The insulation-displacing contacts mean there's no wire stripping. So assembly is faster. And that cuts costs.

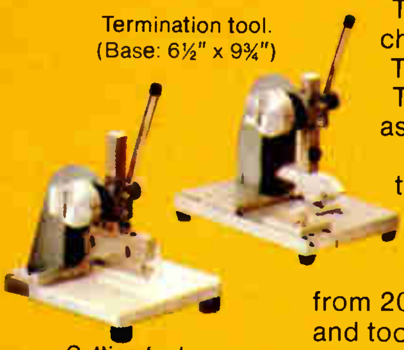
The socket and header bodies are made of UL-recognized 94V-O thermoplastic. Which should make it easier for you to get UL approval.

Additional coding and keying guides are available if several connectors of similar configuration are on an assembly.

New Amphenol IDC Connectors are offered in six sizes, with from 20 to 60 contacts. Also offered are matching cutting tools for flat cable and tools for connector termination.

For complete information, technical data, dimensions, and prices, contact your nearest Amphenol North America sales office or distributor.

Termination tool.
(Base: 6½" x 9¾")



Cutting tool.
(Base: 7⅞" x 10⅛")

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Circle 221 on reader service card

optional data-base accelerator.

The data-base accelerator increases the speed of the machine tenfold, achieving operating speeds of up to 10 million instructions per second. It couples tightly to the disks, operating on the byte stream at disk transfer speeds of about 1.2 megabytes/s. The accelerator takes care of searching, comparing data, matching, and responding to the mainframe CPU or intelligent terminal. "By performing all searches at the disk—and at disk speeds—the IDM greatly reduces both the I/O traffic to the host computers and the CPU overhead associated with the search function," notes Britton.

Although the IDM will be demonstrated at the National Computer Conference next month, deliveries of evaluation units are not expected until the fourth quarter, with production volumes set for January.

Britton-Lee Inc., Albright Way, Los Gatos, Calif. 95030. Phone (408) 378-7000 [361]

Daisy printer offers choice of two interfaces

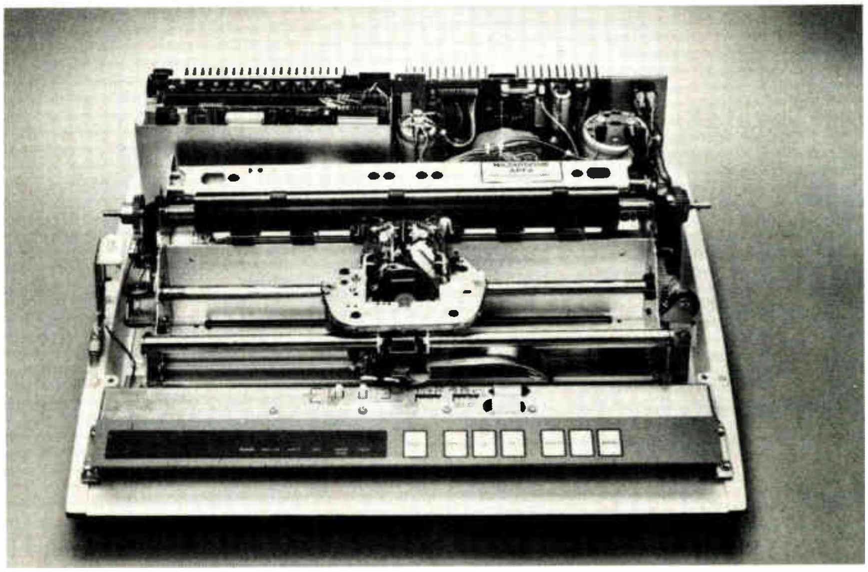
Systems builders looking to incorporate a high printing quality in the form of daisy-wheel style printers into their systems now have a choice of interface in the model 630. Those desiring to write their own printer control software can connect to the printer's 8-bit Intel-8080–compatible bus. Their signals to the printer must specify which spoke of the daisy wheel is to be printed, the amount of energy to be used to fire the hammer, and the width of the character to control spacing.

Those desiring a simpler interface can purchase an optional communications interface board that accepts standard RS-232-C inputs and handles all control of the printer. This includes control of bidirectional printing, column justification, and proportional spacing.

Ronald R. Ogg, product marketing manager for printers, says the extensive use of new electronics, including custom integrated circuits, provides other benefits for the original-equipment manufacturer. "We've reduced the number of mechanical parts by 30%, thus improving reliability." In addition, the unit uses 70% fewer electronic parts, Ogg says.

Instead of the six printed-circuit boards used in the previous model HyType II, the new model 630 uses just one board for the digital electronics and one for the analog electronics that control the printing mechanism. Two Intel 8041 microprocessors are the heart of the digital interface board, whereas seven custom analog ICs handle the mechanism control.

Another benefit of the new electronics is a feedback control loop



Circle 223 on reader service card

that senses the mass of the print wheel and automatically sends the proper amount of drive current to its motor. This unit is also programmed to drive both plastic and the more massive metal print wheels, providing the OEM with a wide choice of print styles without the need to stock two printing mechanisms, Ogg notes.

Printing at up to 40 characters per second, the unit is almost 15% slower than the HyType II, Ogg admits, but is priced between 30% and 40% less depending on configuration. The basic mechanism with control electronics and microprocessor interface is $860 in OEM quantities of 500, and a fully configured unit with the RS-232-C communications interface, power supply, platen, and covers is $1,705 in similar quantities. Deliveries will be 120 days after receipt of order, starting this month.

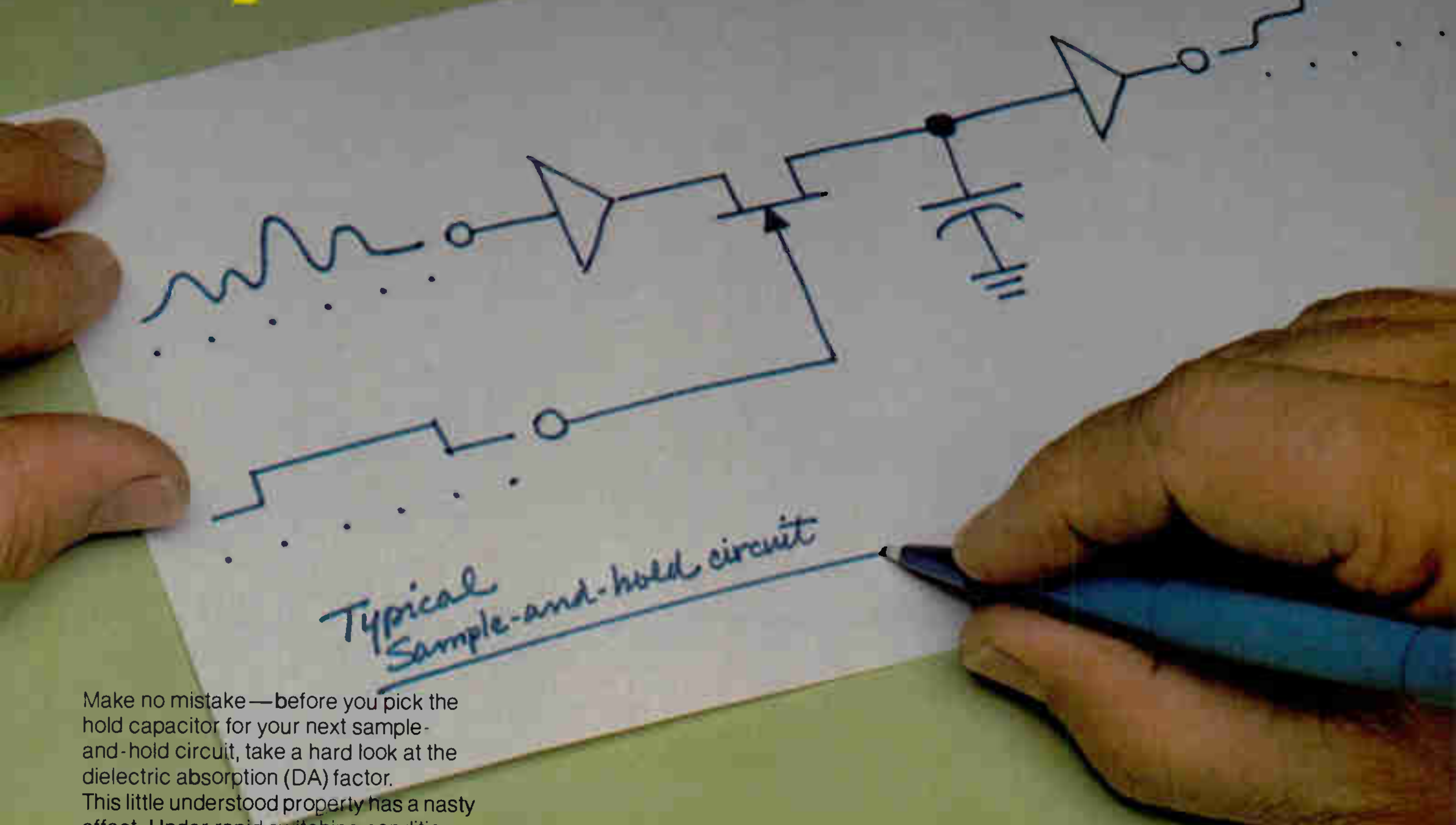
Diablo Systems Inc., 24500 Industrial Blvd., Hayward, Calif. 94545. Phone (415) 786-5000 [362]

Prompting computer comes in 17-lb terminal

Computer Devices Inc. will show a portable computer that prompts the user at May's NCC [*Electronics*, March 27, p. 34]. Central to the design of the 17-lb computer are its ease-of-use and compatibility features, which allow inexperienced operators to use the unit in applications ranging from process control to local communications networks.

The Miniterm model 1206/PAT

Tradeoffs in capacitor selection

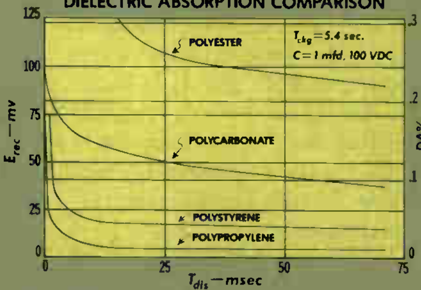


Make no mistake—before you pick the hold capacitor for your next sample-and-hold circuit, take a hard look at the dielectric absorption (DA) factor.

This little understood property has a nasty effect. Under rapid switching conditions, it can cause the capacitor to become an active source of DA error. Another concern is leakage.

DA results from stored charges in the dielectric which behave as parasitic RC components. These subversive elements serve to aggravate output voltage error, which obviously means a loss of accuracy. How much loss of accuracy depends primarily on the dielectric material. Typical DA percent values (i.e., voltage error), measuring accumulated charge after a controlled discharge, are:

DIELECTRIC ABSORPTION COMPARISON



(These values also, incidentally, are affected by capacitor value, size and configuration.)

The tradeoffs: polypropylene is clearly superior to the others in DA. It also is superior in insulation resistance (leakage). On the other hand, it comes in third, behind polystyrene and polycarbonate but ahead of polyester, in temperature coefficient.

Upshot: if high accuracy in your sample-and-hold circuit is a must, polypropylene is a must, too.

Next decision: source. TRW researched, developed and introduced polypropylene for use in miniaturized precision capacitors. We made it work in the real world. We suggest, therefore, that you test our Type X363UW for your next sample-and-hold design. It can save you a lot of design time.

Today's S/H circuits are another reason why capacitor selection is a whole new ball game. It needs to be a studied project or it'll cause sticky problems. But you needn't let the discipline nag or nettle you.

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E 4

TRW CAPACITORS
ANOTHER PRODUCT OF A COMPANY CALLED TRW

Circle 225 on reader service card

(Programmed Applications Terminal) has been developed to work with the company's earlier 1206/PRO, a portable programmable computer. The PAT model allows programs to be loaded into it from either the PRO or any other machine operating under asynchronous ASCII protocol, eliminating the need for on-site programming. Because the PAT uses 105 to 135 V ac at 50 to 60 Hz and comes with an acoustic coupler, it can be used almost anywhere.

The basic 1206/PAT features an 80-column, 50-character/s thermal printer, an integral minicassette tape drive, a built-in modem, and an acoustic coupler. An optional bar-code scanner and a disk operating system capable of supporting up to 1.44 megabytes of minidiskette storage are also available.

The 1206/PAT portable computer will sell for $5,195 in single quantities and deliveries are scheduled to begin in the third quarter.

Computer Devices Inc., 25 North Avenue, Burlington, Mass. 01830. Phone Frank Graham at (617) 273-1550 [369]

CRT for computer graphics has 24-line/cm resolution

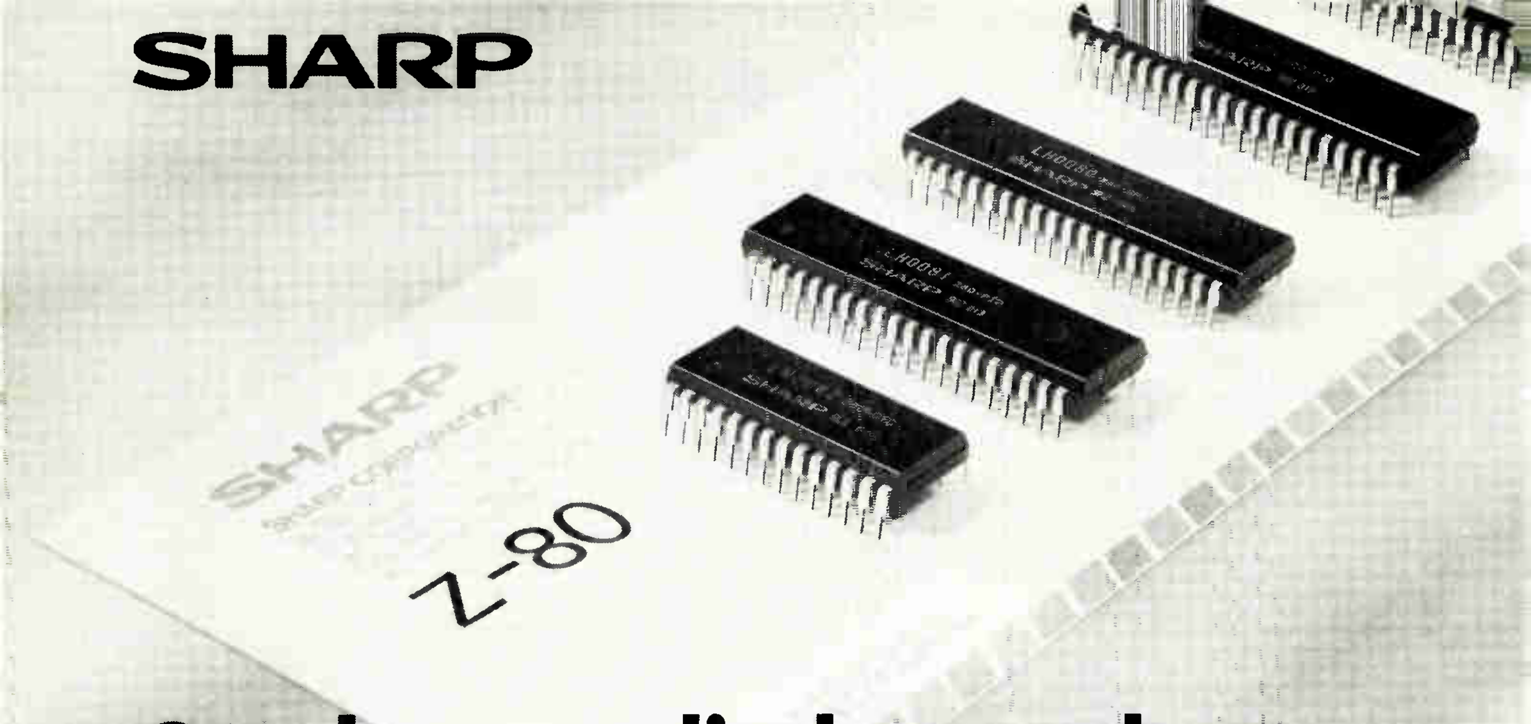
Designed for use as a graphics computer peripheral, the cathode-ray-tube display model 1311B has a resolution of 24 lines/cm (60 lines/in.) at center screen. Using a 14-in. screen, the unit includes high-speed deflection circuits, a Z-axis amplifier with a 25-ns rise time, and regulated power supplies.

Spot resolution of the CRT display is 0.43 mm (0.017 in.). The spot remains well focused over the entire screen, which allows many characters to be written clearly around the picture edges. The 1311B can write in less than 500 ns including the settling time. Rise times for both X- and Y-axis amplifiers are less than 75 ns. The CRT requires only 115 VA maximum.

The 1311B sells for $5,300 and delivery time is about 30 days.

Hewlett-Packard Co., 1507 Page Mill Rd., Palo Alto, Calif. 94304 [367]

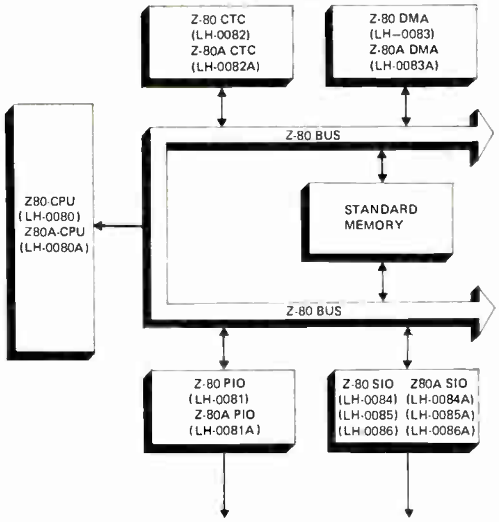
SHARP



Can be supplied anywhere, anytime and in any quantity by SHARP!

SHARP CORP. is the second source manufacturer of ZILOG Z-80 Series.

SHARP has a full line of 4-bit to 8-bit microcomputers to meet various demands: SM Series (C-MOS 1 Chip: SM-4 & SM-5) for low level, Z-80 Series (CPU, PIO, CTC, SIO & DMA) for high level. The Z-80 Series are designed for controllers and terminals requiring complex processing while the SM Series are suitable for consumer appliance. Also available is the Z-80A series – high speed types for clock frequency 4MHz.



ZILOG	SHARP Type No.	Explanation	Features	Package
Z-80 CPU Z-80A CPU	LH-0080 LH-0080A	Central Processing Unit	• 158 instructions – includes all 78 of the 8080A instructions • Three modes of maskable interrupt plus a non-maskable interrupt • 22 internal resisters • •	40 DIP
Z-80 PID Z-80A PIO	LH-0081 LH-0081A	Parallel I/O Controller	• Two independent bidirectional ports • Any one of the following modes of operation may be selected for either port: Byte input/output, Byte bidirectional bus, Bit Mode • •	40 DIP
Z-80 CTC Z-80 CTC	LH-0082 LH-0082A	Counter Timer Circuit	• Four independent programmable 8-bit counter/16-bit timer channels • Single phase clock • •	28 DIP
Z-80 DMA Z-80A DMA	LH-0083 LH-0083A	Direct Memory Access	• Single channel 2 port • Three classes of operation • 3 Modes of operation • Up to 1.25MB search rate • •	40 DIP
Z-80 SIO/0 Z-80 SIO/1 Z-80 SIO/2 Z-80A SIO/0 Z-80A SIO/1 Z-80A SIO/2	LH-0084 OH-0085 LH-0086 LH-0084A LH-0085A LH-0086A	Serial I/O Controller	• Two full duplex channels • Asynchronous operation • Binary synchronous operation • HDLC IBM SDLC Mode • 0 ~ 550k bits/Sec • •	40 DIP

Vcc (V): +5 • Z-80: clock frequency 2.5MHz Z-80A: clock frequency 4MHz

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30 MHz delayed sweep – $1,530.

LBO-515B is a compact, precision oscilloscope at a moderate price. Using a PDA 4-inch CRT with parallax-free internal graticule, it features 5 mV sensitivity and delayed sweep for viewing and measuring complex waveforms. Also has 120 ns signal delay, trigger hold-off and x-y operation at full sensitivity.

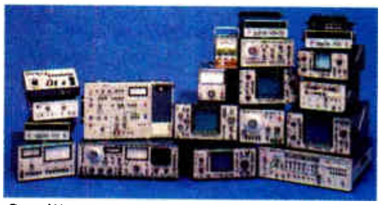
30 MHz with signal delay – $1,100.

LBO-520 combines a 11.7 ns rise time with 5 mV sensitivity and 120 ns signal delay lines. Has single shot triggering, X10 sweep magnifier and bright, sharp PDA CRT. Triggers to 50 MHz.

For Product Literature circle 153

20 MHz dual and single trace – $835., $610.

LBO-508A and LBO-507A give you versatility at low cost. Rise time is 17.5 ns with 1 MΩ (35 pFd) input impedance. Automatic or external triggering, X5 sweep magnifier, 10 mV/cm sensitivity and add/subtract modes.



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LBO-514 has both vertical and horizontal X5 magnifiers. Sensitivity is from 1 mV/cm to 10 V/cm. Sweep speeds from 0.2 s/cm to 0.1 µs/cm. Auto or normal triggering. Z-axis modulation. (Single trace version, LBO-513, $495.)

20 MHz battery/ac portable – $950.

LBO-308S provides lab performance and high reliability in field service applications. Sensitivity is 2 mV with a complete set of triggering controls and 18 sweep ranges to 0.1 µs/div. with X5 magnifier. Compact, lightweight with 3-inch rectangular, internal graticule CRT. (Optional 2 hour internal battery pack is recharged during ac operation, $75.00.)

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For Product Demonstration circle 229

Semiconductors

GPIB chip set completed

Transceiver plus two earlier Intel chips constitute a complete IEEE-488 interface

The 8293 general-purpose interface bus (GPIB) transceiver joins the recently announced 8291A talker/listener chip [*Electronics*, March 13, 1980, p. 44] and the 8292 controller chip from Intel Corp. to complete a three-chip set that provides an entire IEEE-488 interface. In the 8293, the manufacturer is using HMOS-II technology; it has four programmable modes that reconfigure its internal circuitry, permitting it to function both in talker/listener and talker/listener/controller environments.

Previous implementations of an IEEE-488-1978 interface have required up to 40 TTL integrated circuits, plus passive components such as resistor networks. No auxiliary components are needed with the new three-chip set, however, because bus terminations and hysteresis characteristics required by the standard are built into the transceiver.

Each 8293 chip contains nine line-drivers (transmitters) and nine receivers. In addition to taking care of bus terminations and hysteresis requirements, the 8293 has power-up and power-down protection, so that the GPIB bus is not disturbed by power transitions.

Each driver can sink 48 mA and drive high-capacitance loads at high speed. At 30 pF it can provide a throughput time of 35 ns, whereas at an IEEE-488 worst-case of 4,500 pF it provides bipolar throughput times in the 200-ns range. It can be configured as an open-collector or a three-state driver, depending on the operation requirements of the programmed mode.

The use of HMOS II technology allows a significant reduction in power-dissipation levels. Two 8293 transceivers, for example, will dissipate 0.75 W to perform functions that would ordinarily require up to 9 TTL devices dissipating a total of 3.5 W.

The 8293 represents Intel's first use of HMOS II technology to achieve high drive currents rather than high functional density. Notes Mark Olson, product marketing manager for peripheral products, "The technologically interesting part of the 8293 is that, for this application, we have proved that MOS technology is as good as bipolar—not just in speed, but in drive currents as well."

The 8293 operates on a single 5-V power supply, with a typical supply current of from 75 to 100 mA. Its bus power-down leakage current is less than 10 μA. In the plastic package, the 8293 is priced at $11.50 in quantities of 100. Samples of the part are available now and production quantities are planned for the end of the second quarter.

Intel Corp., 3065 Bowers Ave., Santa Clara, Calif. 95051. Phone (408) 987-8080 [411]

Buffer FIFO operates at 15-MHz data rate

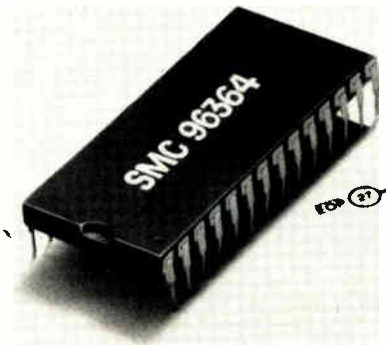
Designed for use as a buffer in real-time digital signal-processing applications, this first-in, first-out integrated circuit is guaranteed to operate at a data rate of 15 MHz, 50% faster than an earlier 10-MHz MMI FIFO device. The 67401A serial memory can be used for digital television, as a communication buffer, and as a high-speed disk controller.

The FIFO is used to assemble incoming data in a word-serial buffer to be read out later in the order written, but at a different rate. The bipolar device operates in synchronous as well as asynchronous modes and has TTL inputs and outputs. Organized as 64-by-4-bits, the commercial version of the device sells for $38 in quantities of 100 and up. Delivery is from stock.

Monolithic Memories, 1165 E. Arques Ave., Sunnyvale, Calif. 94086. Phone Ray Gouldsberry at (408) 739-3535 [413]

CRT controller interfaces to computers or stands alone

A CRT controller that handles all the functions required for a 16-line-by-64-character video display easily interfaces with any computer or microprocessor and can serve as a stand-alone video processor. The CRT 96364A generates a 50-Hz vertical sync and the 96364B generates



a 60-Hz vertical sync. Both devices require only a 5-V power supply at less than 100 mA and incorporate a proprietary n-channel silicon gate technology. Contained in a 28-pin dual in-line package, the controllers are priced at each in single-piece quantities.

Standard Microsystems Corp., 35 Marcus Blvd., Hauppauge, N. Y. 11787. Phone (516) 273-3100 [414]

8-kilobyte RAM has 300- and 500-ns access times

Suited for microprocessor applications, the 8-kilobyte static random-access memory comes in a 24-pin Cerdip package and is pin-compatible with the 2708 erasable-programmable read-only memory. Organized as 1,024 by 8 bits, the 8118 is available with access times of either 300 or 500 ns. The device can be connected to a data bus through its common input/output pins, is TTL-compatible on all its inputs and outputs, and operates from a 5-V power supply. It dissipates less than 60 mW in

SYSTEM 19 NOW PROGRAMS MORE THAN 200 DIFFERENT PROMS WITH ONLY ONE SOFTWARE SELECTABLE MODULE.

Our new System 19/UniPak lets you program most MOS <u>and</u> bipolar PROM'S from AMD, Fairchild, Harris, Intel, MMI, Motorola, National, Raytheon, Signetics and Texas Instruments. UniPak's software assembles the programming algorithm and selects the correct socket for 16, 18, 20, 24 and 28-pin PROMS.

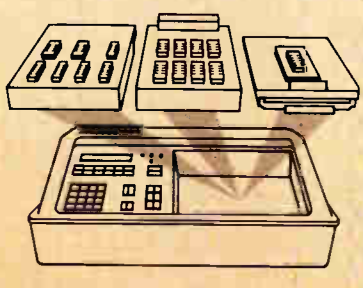
System 19/UniPak gives you design and purchasing freedom. This means you can select the best PROM for each application, and you can second-source for the best price and availability.

Semi-house approvals and easy calibration help maintain higher device yields. UniPak has earned written approval from device manufacturers. And easy calibration lets you keep performance within PROM manufacturers' specifications.

UniPak algorithms shorten programming time enhancing System 19's use as a production tool. UniPak is the first module to use a newly developed algorithm which makes it possible to program a 64K EPROM in less than half the time it takes to program a 16K EPROM using standard methods.

And the System 19/UniPak is easy to operate, with a minimum of operator training.

New System 19 concept is open ended to keep it state of the art. The System 19 is designed around a standard main frame and plug-in modules.



Modules available now include the UniPak, a gang programming pak for MOS devices, and a series of programming paks for logic devices and individual PROM families.

23 communication formats including six for development systems. Development systems, computers, teletypes and CRT terminals interface easily with the System 19. The System 19 accepts micro-processor instruction codes from Motorola, Intel, Tektronix, Fairchild, FutureData and other development systems without intermediary equipment.

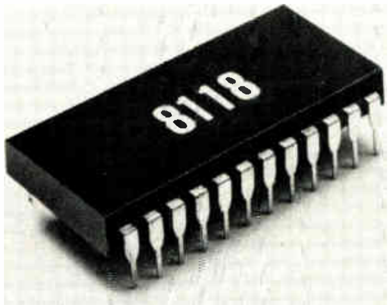
Let us show you the future. The new Data I/O System 19/UniPak is available now. To make arrangements for a demonstration or to get your free copy of this valuable 32-page book, circle reader service number or contact Data I/O, P.O Box 308, Issaquah, WA 98027. Phone 206/455-3990 or TOLL FREE: 800/426-9016.

DATA I/O

Circle 231 on reader service card

the disabled mode and less than 270 mW in the enabled mode.

In 100s, the 300-ns device sells for $31.20, and the 500-ns unit costs



$30. Delivery is from stock.

GTE, Corporate Communications Department, One Stamford Forum, Stamford, Conn. 06904. Phone Roy C. Evans at (602) 968-4431 [415]

ICs allow phase control between 0° and 180°C

A series of integrated circuits is designed to control industrial power circuits such as electric motors, light dimmers, and heaters. The family includes four phase control ICs: the UAA145B, UAA146B, U111B, and TEA1007, as well as U106BS and U217B zero-crossing switches. According to the company, these ICs will help conserve energy.

The UAA145B and UAA146B allow phase control over the temperature range from 0° to 180°C with separate outputs for the positive and negative half cycle of the sync signal. Both of them can be powered from the line supply. The U111B incorporates a thermally stable reference source on chip and an extra operational amplifier for user-defined applications; the TEA1007 is a scaled down version of the U111B.

The U111B comes in a 14-pin dual in-line plastic package; the TEA1007 comes in an 8-pin DIP; and the UAA145B and UAA146B are housed in 16-pin packages. In quantities of 1,000 units, the 145B and 146B sell for $3.75 each. The 111B sells for $2.50 each and the 1007

Our new, dual-channel Model 619 electrometer/multimeter offers you electrometer sensitivity, multimeter ease, systems capabilities and will not interfere with system level decisions. Unless you want it to.

The 619 is loaded with real-world features which make it as flexible as your imagination. It will correct for internal voltage offsets, store up to 50 readings for examination later at the convenience of the system, define a baseline allowing you to read either absolute values or deviations from the baseline—all automatically.

Optional dual-channel capability gives you two instruments for the price of one. Ratio. Difference. Capability for charge or logarithmic current measurement. Speeds up to 18ms/conversion. 4½ or 5½ digit resolution. On the bench or on the IEEE-488 bus.

As an electrometer. As a systems multimeter. As a picoammeter. As a current source.

It lets you decide what it should or shouldn't do.

From its status-at-a-glance annunciators to its programmable trigger modes, every detail of the 619 was painstakingly thought through to give you, the user, full command of the instrument and your application.

Sensitivity. Adaptability. Ease of use. Value. If ever there was an example of Keithley's user-oriented, price/performance design philosophy, it's the 619. It's as much or as little as you need, whenever and however you need it.

Contact your Keithley representative. He'll be happy to show you how the 619 does exactly what you expect a sophisticated measurement instrument to do—and not do.

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Keithley Instruments Ltd.
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Keithley Instruments, SARL
44, Rue Anatole France/F-91121 Palaiseau Cedex/(01) 014-22-06/Telex: (842) 204188

Circle 233 on reader service card

sells for $1.65 per unit.

AEG-Telefunken Corp., Route 22-Orr Dr., P. O. Box 3800, Somerville, N. J. 08876. Phone (201) 722-9800 [416]

Octal bus transceivers have 15-ns propagation speed

The models MD74C245A and MD54C245A circuits are octal bus transceivers designed for two-way, high-data-rate, asynchronous bus applications. Both devices have a propagation speed of 15 ns, a typical quiescent power dissipation of 5 μW, and a typical operating power of 50 μW. The devices operate over the voltage range from 3 to 6.5 kV. Prices vary with specification. The model MD74C245AE, for example, sells for $3.50 each in 100 units and for $2.60 in 1,000 units. Delivery is from stock.

Mitel Semiconductors, P. O. Box 13089, Kanata, Ottawa, Ontario, Canada. Phone (613) 592-2122 [417]

HEXFETs have turn-on time of 55 ns

Having a turn-on time of 55 ns, the IRF line of HEX field-effect transistors are encased in both TO-3 and TO-20 packages. Based on a chip measuring 90 by 138 mils, the medium-current devices need only the drive current to charge an input capacitance of 450 pF. The transistors are designed for such applications as switching power supplies, motor controls, inverters, choppers, audio amplifiers, and high-energy pulse circuits.

In quantities of 1 to 9, the IRF120 sells for $10.80, the IRF220 for $13.20, and the IRF320 for $16.80, all in TO-3 packages. In the same quantities, the IRF520 is $9, the IRF620 is $10.90, and the IRF720 is $15. Samples are available from stock, with production quantities delivered in four to eight weeks.

International Rectifier Corp., Semiconductor Division, 233 Kansas St., El Segundo, Calif. 90245. Phone (213) 772-2000 [418]

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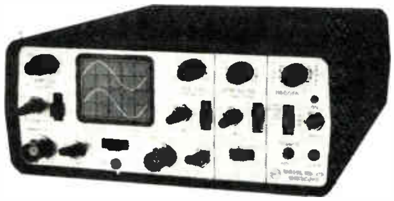
● Weight: 3 lbs. ● Battery or line operated. ● Single- or dual-trace models.

MS-15 $349.80
15 MHz — Single-Trace
- External & internal trigger.
- Line synchronization mode.
- Power usage—<15 W.
- Battery or line operation.
- 2.9" H x 6.4" W x 8.0" D.

Circle 117 on reader service card



MS-215 $465.45
15 MHz — Dual-Trace
- External & internal trigger.
- Line synchronization mode.
- Power usage—<15 W.
- Battery or line operation.
- 2.9" H x 6.4" W x 8.0" D.

Circle 118 on reader service card

MS-230 $598.15
30 MHz — Dual-Trace
- External & internal trigger.
- Line synchronization mode.
- Power usage—<40 W.
- Battery or line operation.
- 2.9" H x 6.4" W x 8.6" D.

Circle 236 on reader service card

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Circle 136 on reader service card

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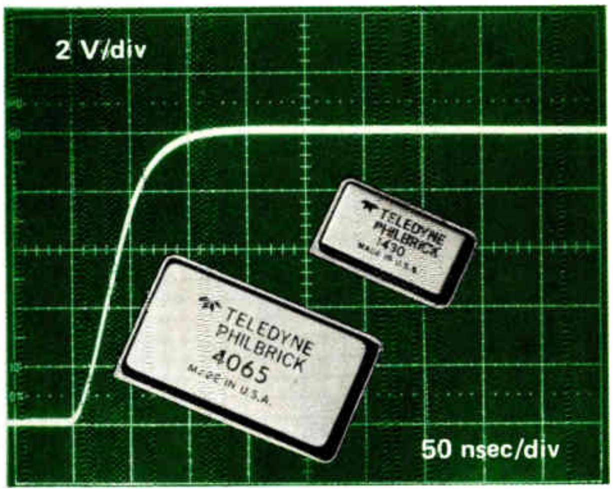

True 12-Bit D To A Conversion

. . . is achieved by combining our 4065 current DAC and our 1430 fet operational amplifier. The result is a 12-bit hybrid voltage DAC system with a voltage settling of under 300 nsec to 0.01%. In addition, these units offer operation from −55°C to +125°C and the high reliability that is inherent in MIL-STD-883 screening.

For more information or special OEM pricing, contact Ted Serafin, Product Marketing Manager.

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Circle 238 on reader service card

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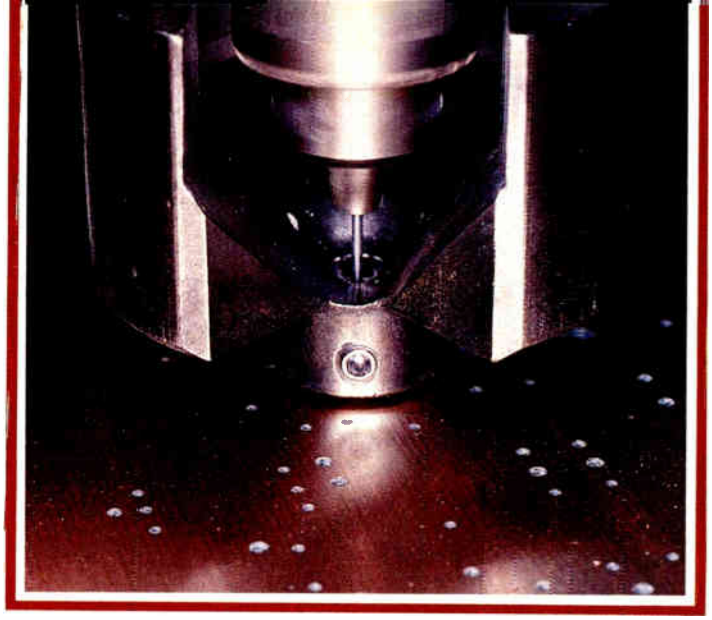


THE HOLE TRUTH

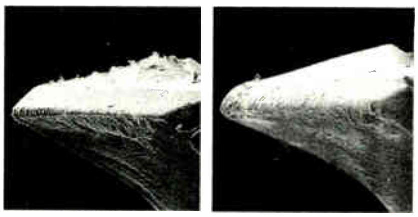
New GE Engineered FR-4.
An advanced laminate designed to reduce drilling abrasion, improve thru-hole quality, and lower processing costs.

Now there's a PC board laminate with even better processing qualities than conventional FR-4. It's the new *Engineered* FR-4 epoxy-woven glass laminate from General Electric.

You can process Engineered FR-4 in exactly the same way as conventional FR-4, and tests by PC manufacturers have shown that you can enjoy improved yields and substantial productivity benefits.

The key to these benefits is a GE discovery: an exclusive epoxy adhesion promoter that greatly enhances the 3-D bonding of the epoxy resin to itself, and to the woven glass layers. The resulting uniform matrix gives the laminate much greater integrity than possible before.

As a result you can expect greater thermal shock resistance and reduced tendency toward delamination during processing. But the opportunity for cost reduction is greatest in the drilling and plating-thru operations. Less abrasion encountered during drilling means reduced heat generation and longer drill life. This is illustrated in the 260X photomicrographs below. Note differences in tip sharpness and wear.



Drill bit edge after 9300 holes in Engineered FR-4 | Drill bit edge after 9300 holes in conventional FR-4

Because there is less drilling abrasion and less heat generated, the quality of thru-holes is greatly improved. With Engineered FR-4, there is less resin smear, rifling, void formation; and fewer torn glass bundles. This in turn provides a superior, more uniform surface for electroless copper plating.

New Engineered FR-4 is the first of a series of technology-oriented PC laminates designed to keep you ahead of today's application requirements. And it's now being produced at our high-capacity plant at Coshocton, Ohio. The unique GE Laminate Technical Center is located there, too, with sophisticated R&D instrumentation devoted to solving your PC processing problems.

See the hole truth for yourself. Contact us for a detailed brochure, and to arrange a trial run of new Engineered FR-4 at your facility. General Electric Company, Laminated and Insulating Materials Business Department, Box EL-4, Coshocton, Ohio 43812.

GE LAMINATES: THE DIFFERENCE IS TECHNOLOGY

GENERAL ELECTRIC

Circle 239 on reader service card

New products

Instruments

LRC bridge has built-in CRT

Bridge measures 11 traits at 3,000 frequencies from 20 Hz to 20 kHz

As microprocessor operating speeds go up, as resolution increases in analog-to-digital and digital-to-analog converters, and as op amps get more precise, designers call for passive components that meet more stringent specifications. The test equipment industry, in turn, is being pushed to produce instruments that provide both greater accuracy and an expanded menu of test conditions.

Perhaps the first to address this need is Electro Scientific Industries Inc. of Portland, Ore., which is about to take the wraps off a new inductance-resistance-capacitance (LRC) bridge. The bridge's built-in cathode-ray tube gives it the flexibility it needs to allow test-condition specifications that closely emulate operating environments.

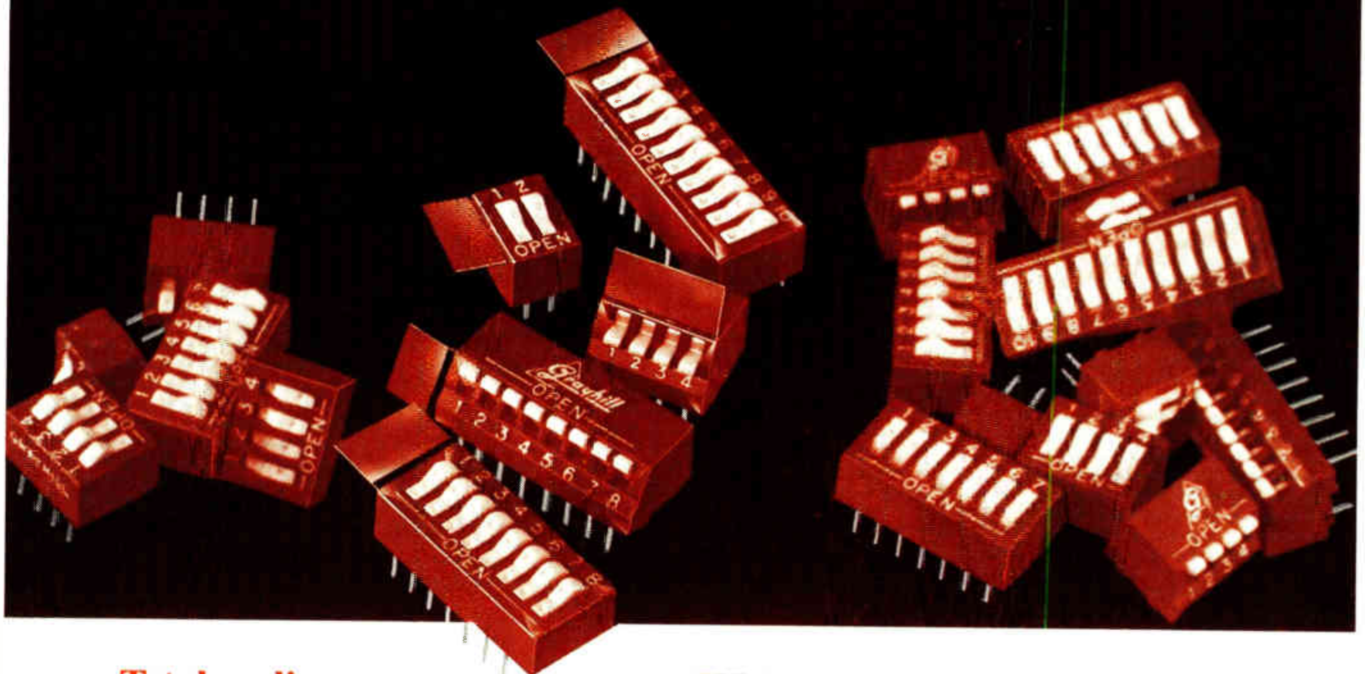
Designated the model 2100, the LRC bridge is capable of measuring 11 impedance characteristics in series or parallel modes at 3,000 discrete frequencies, selectable from 20 Hz to 20 kHz. The number of selectable frequencies is more than an order of magnitude greater than it is in currently available instruments, and the low-frequency response has been extended. Most of the additional frequencies were put at the lower end of the spectrum, "where the need for precision impedance testing is most critical," points out Jim Currier, ESI's product marketing manager for instruments.

Controlled by a Z80 8-bit microprocessor, the 2100 is to be introduced at next month's Electro exhibition in Boston. Its test voltages are selectable up to 1 V rms, and test currents can be varied up to 75 mA. In addition, the instrument has external bias capability and provides accuracies ranging from 0.1% to 0.02%, depending on the measurement mode.

The front panel of the 2100 features a 32-key interactive keyboard and the 5-in. CRT that displays two 5½-digit values of such parameters as inductance, resistance, capacitance, dissipation factor, conductance, impedance, and admittance, among others. Also on the display is the complete system status, including test level, test frequency, series

Grayhill totally sealed DIP switches

better than ever better than others



Total sealing

Each Grayhill SPST Rocker DIP Switch is now potted as part of the assembly process, to provide a more professional and economical bottom seal, with maximum seal integrity. Flux entry during wave soldering is totally prevented; contamination is eliminated; reliability is enhanced; and prices are unchanged . . . there is no cost premium for this important new feature. Grayhill also offers 3 topside sealing options, for raised or recessed rockers—a tape seal, applied at Grayhill; cards of tape seals, for your application; or re-usable protective covers. Whichever you choose, you get complete freedom during PC Board cleaning.

Exceptional reliability

All Grayhill DIP Switches incorporate our exclusive spring-loaded, sliding ball contact system. This highly reliable contact system provides positive wiping action, immunity to normal shock and vibration, and exceptional 50,000 cycle life.

Wide ranging choice

Grayhill Sealed Base Rocker DIP Switches are available SPST, from 2 to 10 rockers, with raised or recessed rockers. Grayhill also provides the Piano DIP™ SPST side-actuated DIP Switch, sealed; the Toggle-DIP (SPDT or DPDT) for front panels, plus SPDT or DPDT back panel programming DIP Switches.

Off-the-shelf distributor availability

Procurement made simple—call Grayhill or your local distributor, for off-the-shelf delivery of most types. Only Grayhill offers you this purchasing convenience!

Make sure you have your copy of the most recent DIP Switch Catalog . . . free on request.

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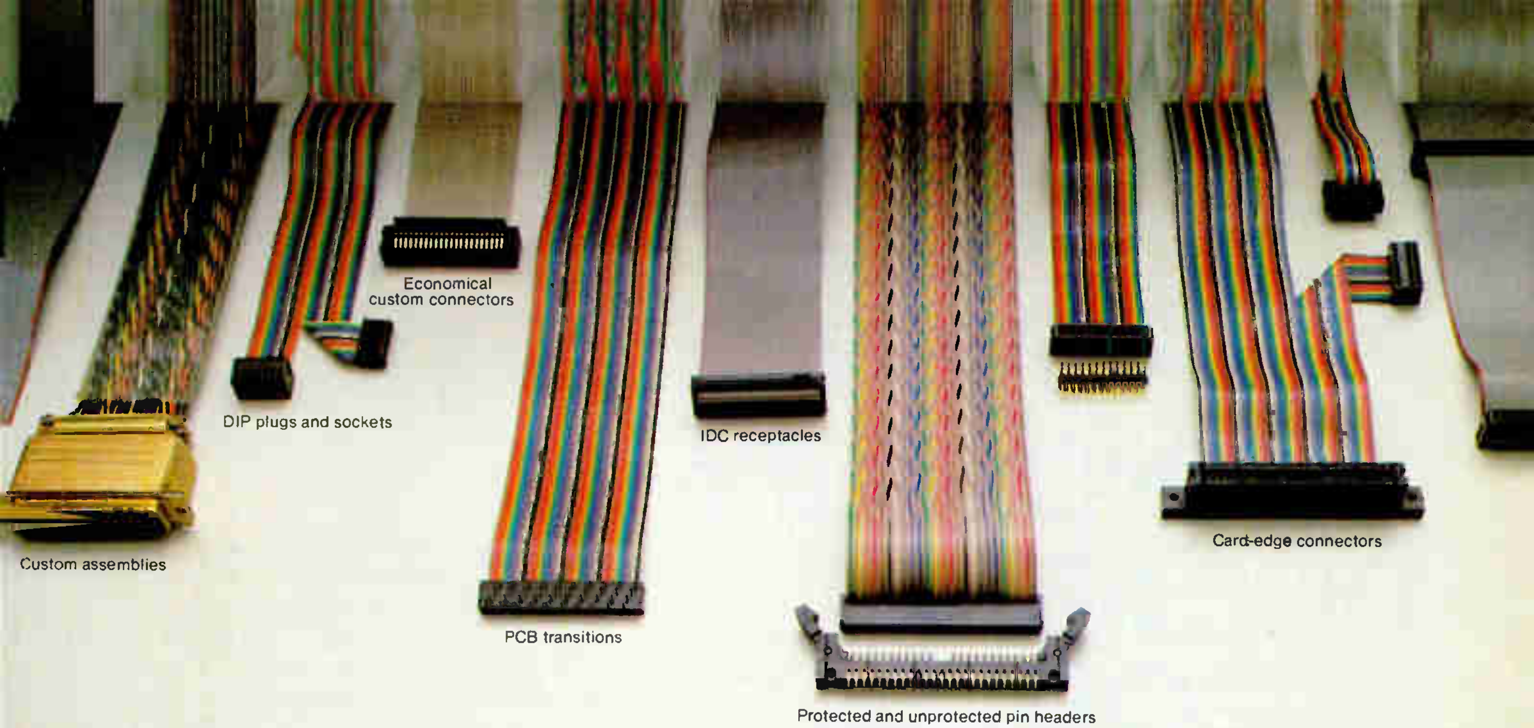
or parallel mode, and programmable settling and integration times.

According to Currier, "having a built-in CRT with almost unlimited presentation of either test conditions or test data means being able to satisfy divergent needs—from providing operating simplicity at incoming inspection to affording access to obscure component traits." As an example of the 2100's flexibility, he notes that the instrument can be programmed to display pass-fail or sorting information for up to 20 bands for reactive measurement, plus one for loss rejection. At the same time it keeps track of the number of parts being sorted into each band.

Typically, when an application demands the translation of raw data into statistical profiles from lot samplings, for example, an IEEE-488 interface can, with a few hours of programming, provide such an output to a controller and calculator and to a printer, Currier notes. The need for this kind of component analysis, he adds, prompted the development of another version, the model 2110, that adds mass storage, lot sampling, and data massaging capabilities via a cassette reader-recorder and optional software packages. These field-installable software modules, to be available in the fall, will be created to meet the demands of specific applications. Options will provide the derivation of temperature coefficients, hard copy histograms, and standard deviations, eliminating some data reduction presently done by hand.

The modular design of the 2100 and 2110 (also to be introduced at Electro) allows for removal and exchange of the power supply, CRT circuitry, and measurement system, and provides for field-installable options such as dual RS-232-C, IEEE-488, and parts-handler interfaces, as well as the addition of nonvolatile memory. Priced at approximately $4,200 and $4,900, respectively, the 2100 and 2110 are both slated to be available in quantity this September.

Electro-Scientific Industries Inc., 13900 N.W. Science Park Dr., Portland, Ore. 97229. Phone (503) 641-4141 [351]



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And, if we don't have the standard IDC connector you need to solve your mass termination problem, we'll invent one that will.

We'll take total responsibility for all your interconnect needs from jumpers and flat cables to IDC connectors and ready-to-go custom and standard planar assemblies, so check us out. You'll quickly see why so many happy endings begin with a call to us.

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See us at Electro 80 booths 1130/1132

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When you're down to the wire

Circle 243 on reader service card

Thermal-array recorder prints grids and traces

The TA 600 analog graphic recorder offers thermal-array writing and an optional dedicated microprocessor for remote control of basic recorder functions. The unit can record both slow-changing process data and high-speed telephone switching transients.

By using a newly developed fixed–linear-array thermal head, the TA 600 does away with pens that may cause overshooting and hysteresis problems. Grids are selected and printed along with the traces, so plain thermal paper can be used on this machine. The unit can handle up to 32 overlapping channels and has space for four dual-channel signal conditioners.

System accuracy and linearity are both to within ±0.2% of full scale, with a resolution of 512 thermal styli spaced at 100/in. The sine-wave bandwidth is 100 Hz accurate to within 2%, and the unit can reproduce square waves at even higher frequencies, recorded exactly as they occur.

Digital inputs available are: serial RS-232-C, ASCII current loops, an ASCII keyboard port that is TTL-compatible, and a digital interface that includes a 2-kilobit random-access memory for entering ASCII characters or raster data. The basic TA 600 (without preamplifiers or microprocessor) is priced at $4,650. Deliveries begin in May.

Gould Inc., Instruments Division, 3631 Perkins Ave., Cleveland, Ohio 44114. Phone (216) 361-3315 [353]

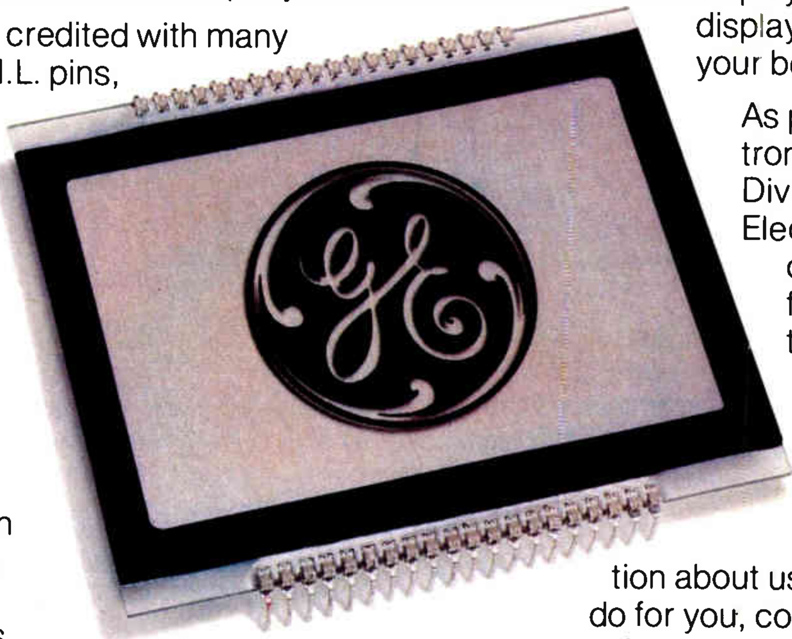
2-MHz function generator comes in industrial package

The model LFG-1300S sweep-function generator is an industrial-grade instrument that covers frequencies of 0.0002 to 2 MHz in eight ranges. The device is packaged in a sturdy, all-metal housing suitable for use in design, testing, and service applica-

General Electric, the new name in LCD's.

The business you've known as Liquid Xtal Displays has a new name. A new name because last September, LXD became a part of the General Electric Company.

As LXD, we were credited with many industry firsts, D.I.L. pins, integral back lighting and dot matrix displays were among them. Our R&D activities produced materials which expanded the operating range and established new performance levels in the industry. Now, with the added resources of GE's Corporate Research and Development Laboratory, we'll be able to provide you with the most advanced technologies available. And they will be tested and proven reliable, in the General Electric tradition.



Today, our production facilities are three times what they were just six months ago.

So General Electric's Liquid Xtal Displays Operation (as we're now known) is your best source of "off the shelf" standard displays or custom displays. That's right, your best source.

As part of the Electronics Components Division at General Electric, we, like other component manufacturing operations, within GE, are geared to supply products to a wide variety of manufacturers.

For more information about us, and what we can do for you, contact your local sales representative, or write: General Electric Company, Liquid Xtal Displays Operation, 24500 Highpoint Road, Cleveland, Ohio 44122. (216) 831-8100. Telex 98-5442. In Europe, A.B. Gosta Backstrom (Stockholm, Sweden) Data Modul (Munich, W. Germany) or Norbain Optoelectronics (Reading Berkshire, England).

GENERAL ELECTRIC

Visit us at Electro/80. Booth 2441-2443. May 13-15, 1980.

tions and is covered by a two-year parts and labor warranty.

The LFG-1300S includes linear and logarithmic sweep modes with sweep widths up to 1,000:1 and sweep rates of 0.5 to 50 Hz. The generator's output frequency may also be varied by an external 0- to 10-V signal. Waveform outputs include sine, triangle, sawtooth, and pulses. The symmetry of the pulse output is variable from 9:1 to 1:9 and adjustments of pulse width do not change the pulse-repetition rate. The output level is continuously variable from 0 to 20 V peak-to-peak (50-Ω load). A push-button attenuator provides up to 70-dB attenuation in 10-dB steps.

The instrument is available off-the-shelf from Leader distributors and sells for $495.

Leader Instruments Corp., 380 Oser Ave., Hauppauge, Long Island, N.Y. 11787. Phone (800) 645-5104 or George W. Zachmann at (516) 231-6900 [356]

Precision standard calibrates voltage, current, temperature

A new precision calibration standard has ±0.02% dc voltage, current, and temperature capability. The model 2553/2560 standard is fully programmable and features 10-mV, 100-mV, 1-V, and 10-V ranges; 1-, 10-, and 100-mA ranges; and five temperature ranges for all commonly used thermocouples. Resolution is 1 μV and 1 μA.

The model 2553 can be controlled and programmed remotely via an optional general-purpose interface bus that meets IEEE-488, so the unit is compatible with other instrumentation systems that use this type of control. Photocouplers and microprocessors in the unit replace conventional electromechanical switches for range selection, increasing reliability, and long-term accuracy.

Prices for the 2553 start at $1,950 and deliveries take approximately 10 weeks.

Yokogawa Corp. of America, 5 Westchester Plaza, Elmsford, N.Y. 10523. Phone (914) 592-6767 [357]

New 8-bit microcomputer joins Mostek family

Sporting a serial input/output port that will handle data either synchronously or asynchronously, the long-awaited MK3873 from Mostek Corp. [*Electronics*, Aug. 31, 1978, p. 217] will take its formal bow at next month's Electro show in Boston. As the latest in the 3870 family of 8-bit single-chip microcomputers from the Carrollton, Texas, firm, **the 3873 will contain 2,048 bytes of read-only memory** and 64 bytes of scratch-pad random-access memory. The serial I/O port consists of a 16-bit shift register that can be read from or written into by the central processing unit while data is being shifted in or out. Serial I/O clocking can be done either externally or with an internal baud-rate generator.

Samples of the 3873 are scheduled to be available in May, housed in Mostek's MK3874 p-channel programmable read-only memory package, which uses an external erasable PROM inserted above the microcomputer die in piggyback fashion for ROM program development. Initial production orders will be taken for third quarter delivery. Price information is not yet available.

Process monitor offers customized I/O cards

Appearing at Electro but not scheduled for formal introduction until this summer will be the series 079 digital manufacturing-process monitor from Airpax/North American Philips Controls Corp. The Fort Lauderdale, Fla., firm will offer it with customized input/output cards so that **customers will not need to program the device.** Based on an MCS-48 microprocessor, the 079 acquires sine-wave, TTL-level, or contact-closure input signals; performs all mathematical and logical functions; and transmits data to relays, displays, or a host computer. Prices will start at about $3,000, with delivery set for 16 weeks.

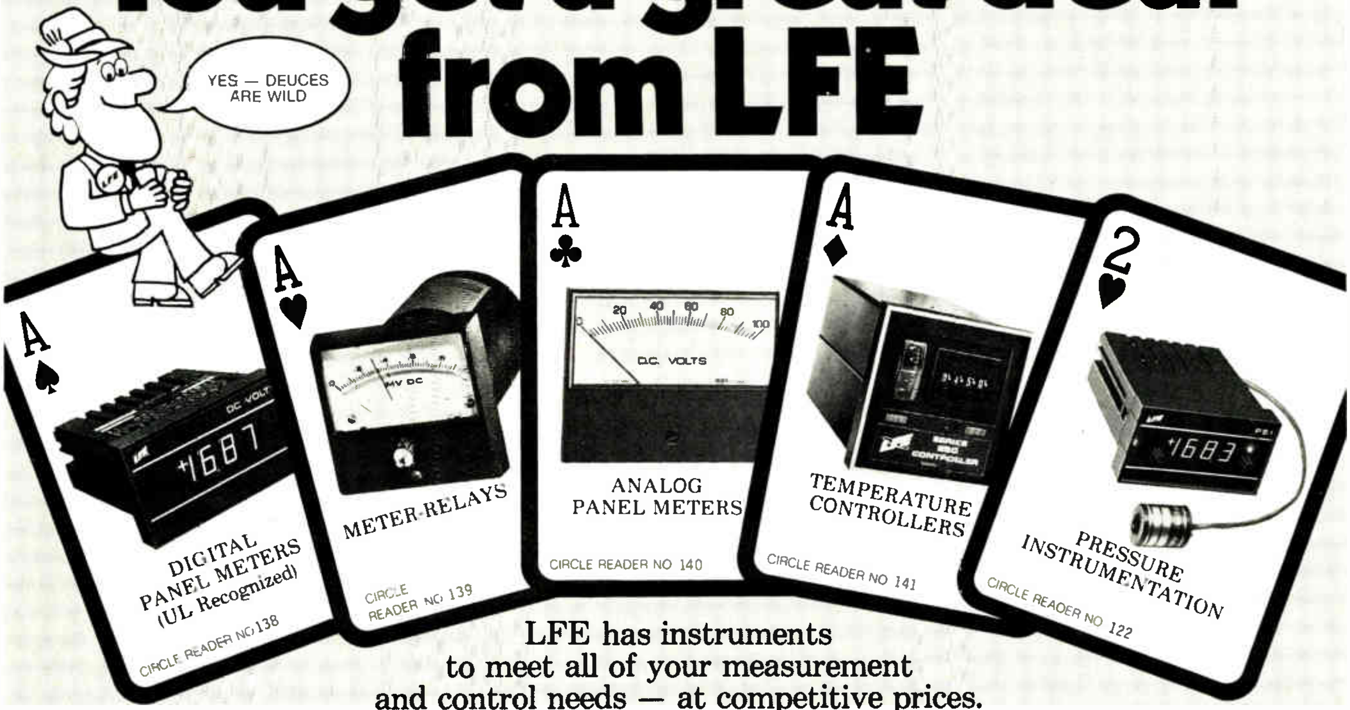
Card expands Apple II's software capabilities

By the end of May, the 6502-based Apple II computer **will be able to handle programs written for Z80- and 8080-based microcomputers** "with minimal alteration." The alteration is the Z80-based Softcard made by Microsoft Consumer Products of Bellevue, Wash. It plugs into one of the Apple II's bus slots and includes two diskettes. One diskette carries the CP/M operating system from Digital Research, and the other carries Microsoft's Disk Basic. To support the Softcard, an Apple must have at least 48 kilobytes of random-access memory and a single disk drive.

Intel enhances memory system family

At month's end, Intel Corp. will introduce the first enhancements of its series 90 memory system modules. The CM-90 series dynamic modules cycle in 350 ns and require only 5-V power supplies. They contain the newer model 2118 16-K random-access memories and can be directly upgraded when 64-K RAMs become available. **The new CM-92 static memory modules will require 50% less power than the earlier versions,** store up to 64 kilobytes, and have 250-ns cycle times. They can later be upgraded with Intel's 16-K HMOS static RAMs. Both series perform error checking, correction, and logging. The Santa Clara, Calif., company is also developing a 5-V, 300-ns replacement for the CM-901 series of 400-ns dynamic memory modules. Prices for the CM-92 and CM-93 memory system modules are, respectively, $15,875 for 256 kilobytes of static storage and $77,650 for four megabytes of 350-ns dynamic storage.

You get a great deal from LFE



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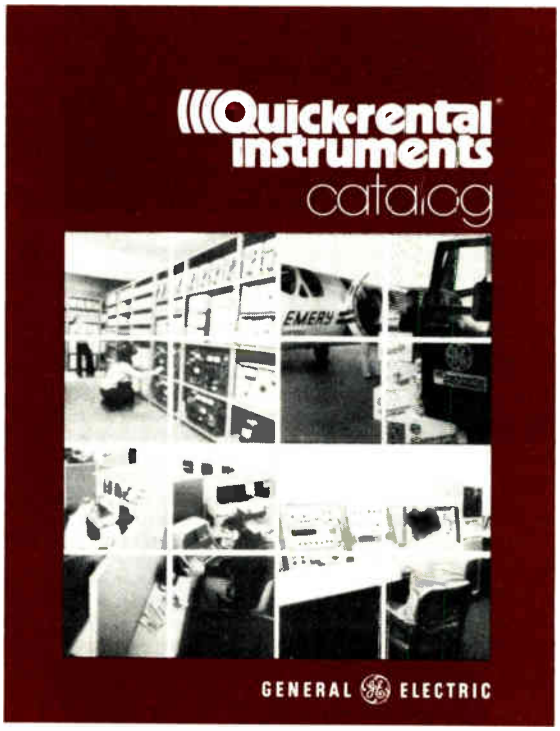

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New literature

Components. The "1980 Component Data Catalog" contains specifications for and descriptions of commercial, industrial, and military devices, support products, and services. Data is provided for Intel's one-megabit bubble memory and support chips, the 2920 signal processor, and the 8089 16-bit input/output processor and peripherals. A schedule and description of the company's 1980 microcomputer workshops, ordering procedures, and packaging information are included. The catalog sells for $7.50. Intel Corp., Literature Dept., 3065 Bowers Ave., SC3-3, Santa Clara, Calif. 95051.

Courses. A comprehensive catalog describes courses offered throughout the U. S. and Europe for engineers, scientists, technicians, and engineering managers. Included are courses on Pascal programming, distributed processing, computer communications, interactive computer graphics, digital image processing, structured programming, and voice input/output for computers. Integrated Computer Systems Inc., 3304 Pico Blvd., P. O. Box 5339, Santa Monica, Calif. 90405. Circle reader service number 422.

Power supplies. A line of switching and linear single- and multiple-output dc power supplies are described in an eight-page brochure. It gives such specifications as input and output ratings, power ranges, and mounting dimensions for the 9E and 9N SuperSwitcher, SM submodular, and original-equipment-manufacturer linear supply lines. Other products listed include the RP series of floppy-disk supplies, military power supplies, and a low-profile silicon dc series. Powertec Inc., 20550 Nordhoff St., Chatsworth, Calif. 91311 [423]

Isolation amplifiers. A 16-page catalog explains what an isolation amplifier is, gives its primary features, and tells how to select an amplifier. It also gives the characteristics and features for several isolation amplifiers. Intronics, 57 Chapel St., Newton, Mass. 02158 [425]

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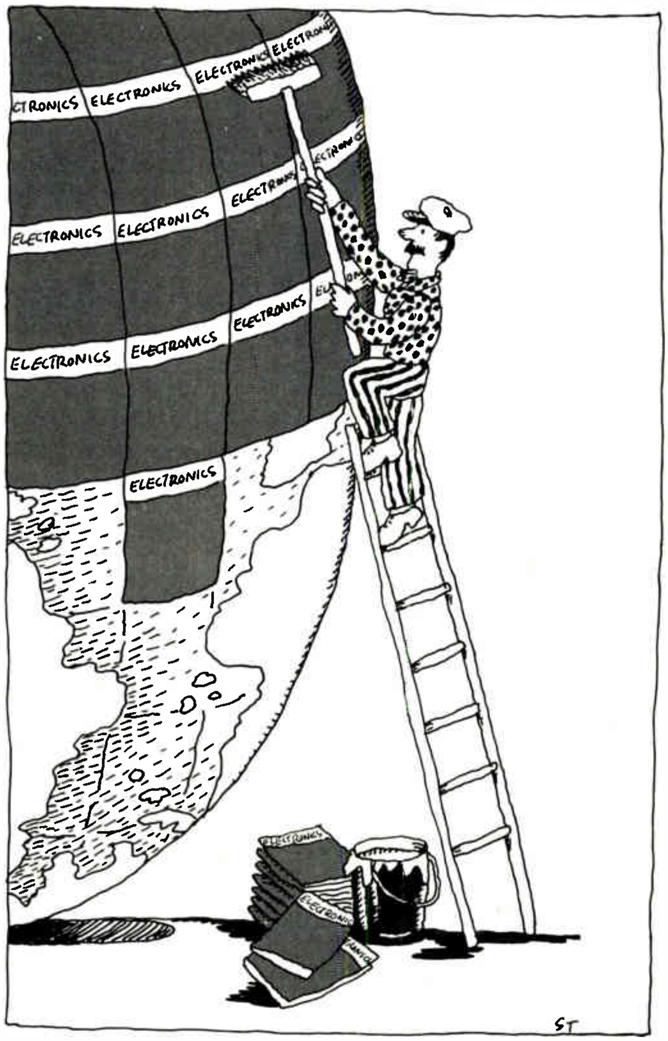

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5. ☐ ☐ ☐ **Your design function:** ***(Insert each letter that applies)***

A. I do electronic design or development engineering work
B. I supervise electronic design or development engineering work
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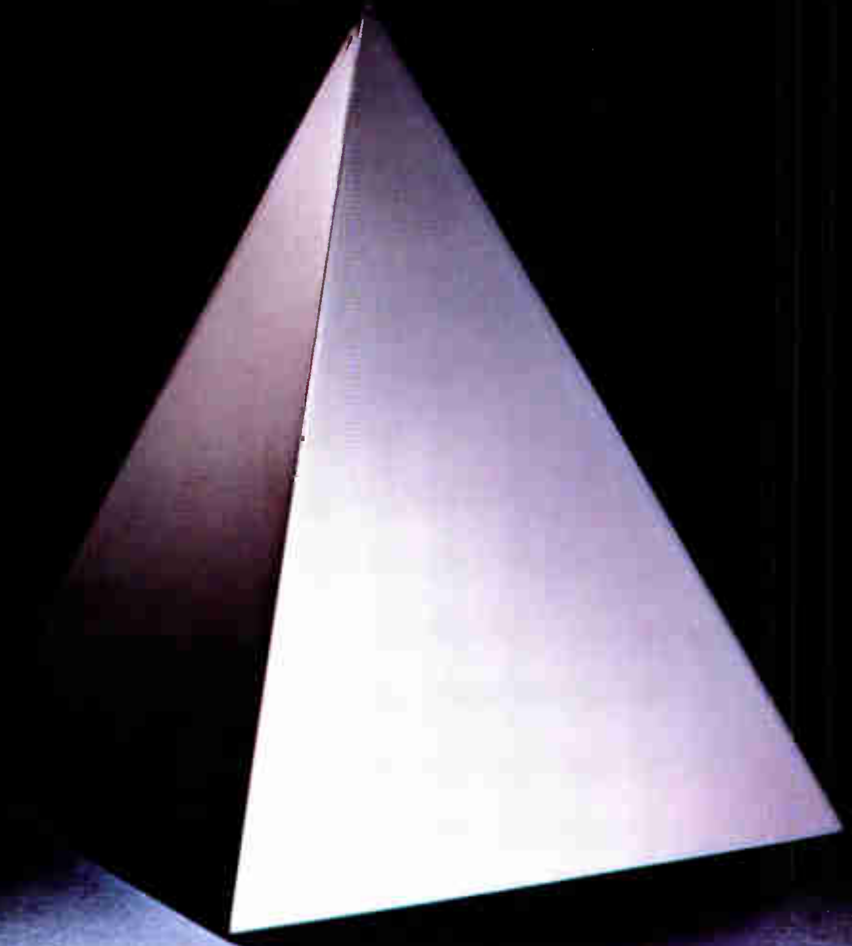

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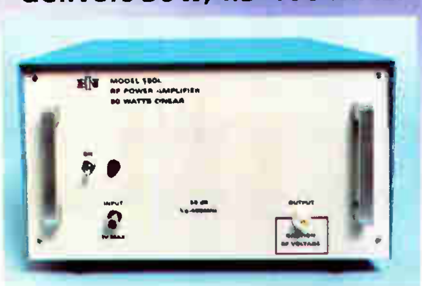

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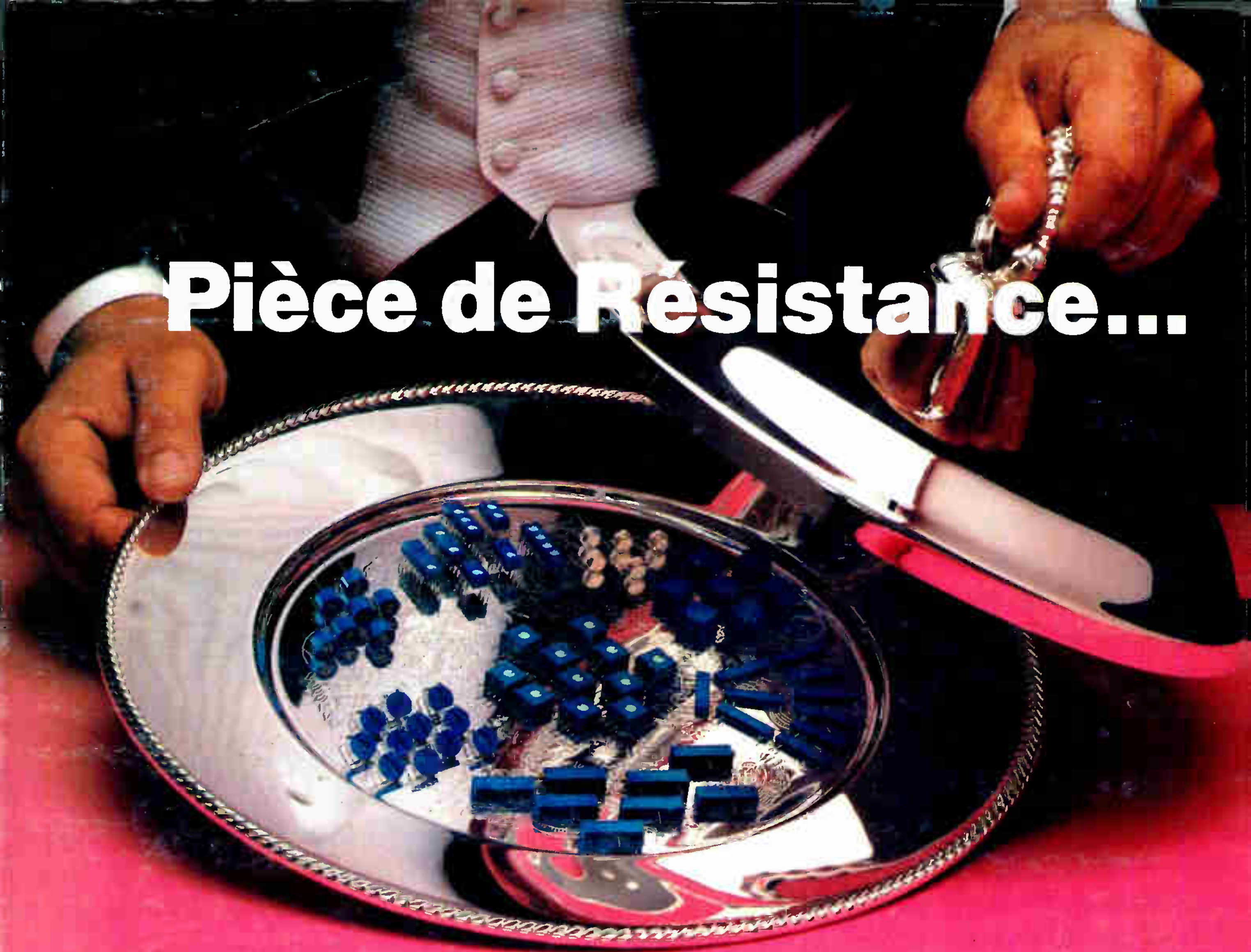

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