A McGRAW-HILL PUBLICATION

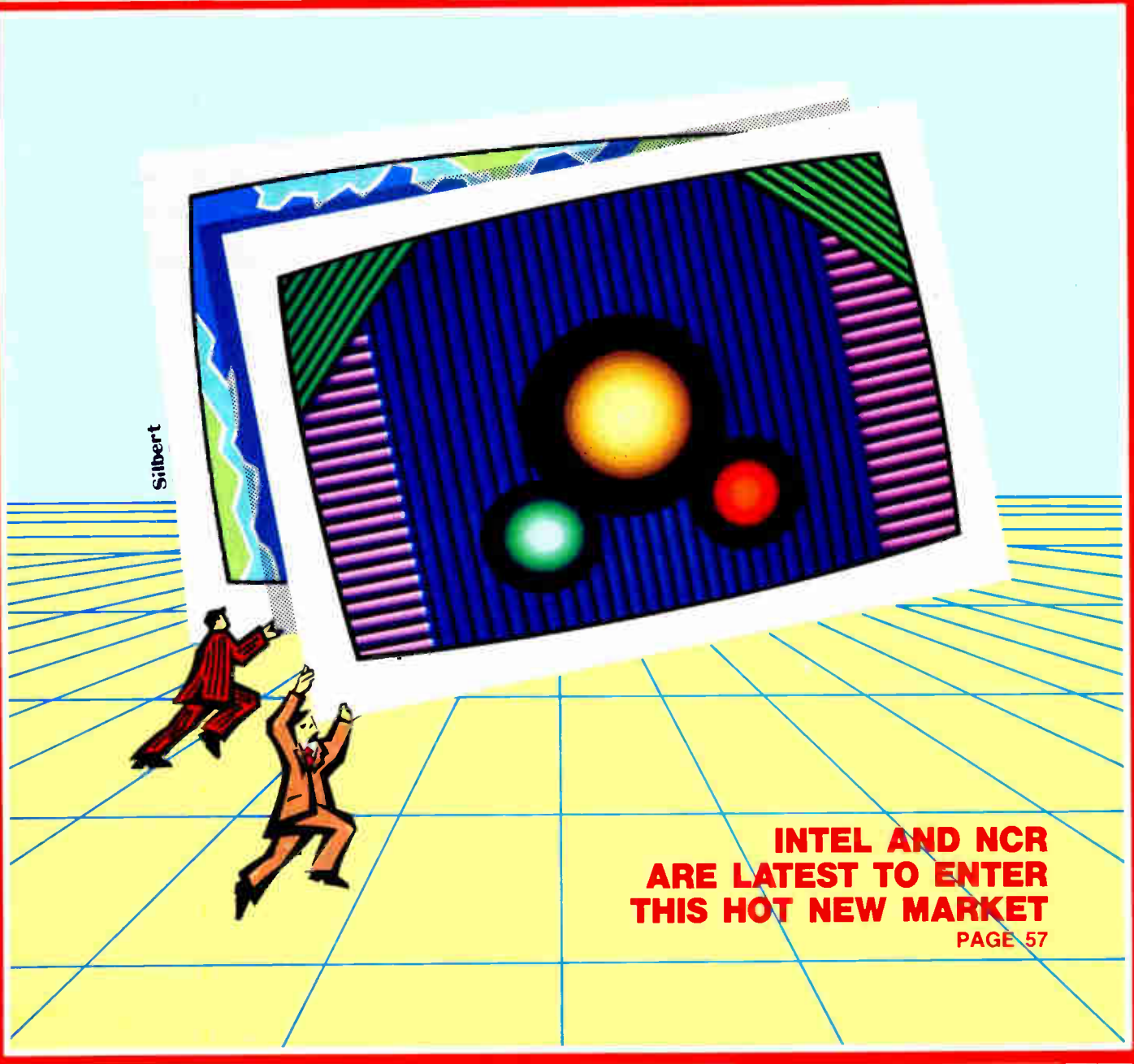
THREE DOLLARS

# Electronics

THE WORLDWIDE TECHNOLOGY WEEKLY

MAY 19, 1986

# THE SCRAMBLE TO WIN IN GRAPHICS CHIPS



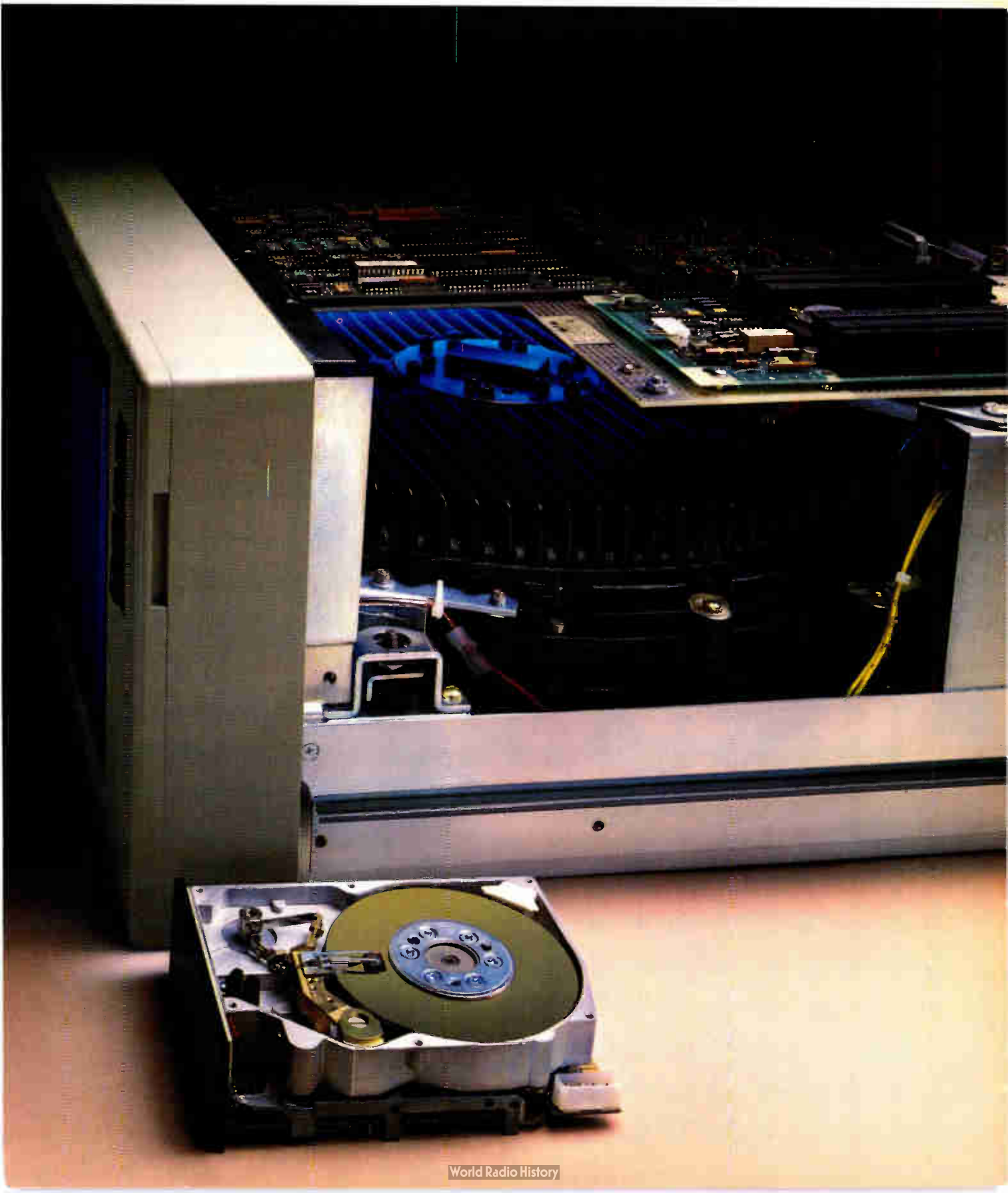

**INTEL AND NCR ARE LATEST TO ENTER THIS HOT NEW MARKET**

PAGE 57

**SPECIAL REPORT: THE OPTIONS MULTIPLY IN MASS STORAGE/28**

**HOW GENRAD'S NEW TESTER COPES WITH VHSIC CHIPS/49**

National Semiconductor Corporation



# Take our mass storage VLSI chip family out for a little spin. Or a big one.

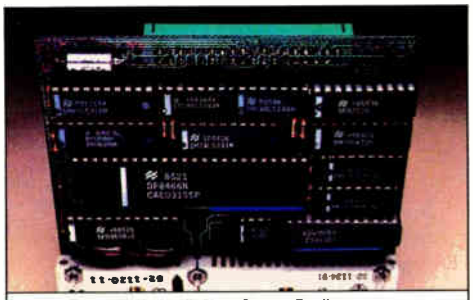
## Only one family of mass storage chips can move you along the entire design spectrum–from 50 Kbps to 25 Mbps. Without shifting gears.

The disk industry today has a lot of heads spinning. With drives of all sizes, shapes, types and interface requirements. With more advanced technologies pushing transfer rates and densities ever higher. And with users demanding higher capacities — but in smaller, lower-power packages.

That's why hundreds of designers have already specified National's DP8466, the hard disk controller, and its complete family of support chips. The only chip set versatile enough to handle today's broad range of drive products. From the PC to the mainframe.

The DP8466 makes key operating features user programmable. So things like data formats, error correction codes, and interface characteristics can be configured interactively for virtually any drive — using the *same* controller chip. Then too, the DP8466 and supporting parts work with National's Series 32000® microprocessor and any other 8-, 16- or 32-bit microprocessor. And they conform to all major drive interface standards.

Wherever your system falls in the price/performance spectrum, our mass storage family has you covered. With data rates ranging all the way from 50 Kbps to 25 Mbps. With advanced VLSI architecture that integrates more disk data path functions than has been possible before. And with exceptionally low controller power consumption, using microCMOS. All of which reduces your overall *system* costs, and boosts both your competitive edge *and* your profits.



**National's Mass Storage Family**

| | | |
|---|---|---|
| DP8466 | (NS 32966) | Disk Data Controller |
| DP8462 | (NS 32962) | 2,7 Data Synchronizer |
| DP8463B | (NS 32963B) | 2,7 Endec |
| DP8464B | (NS 32964B) | Pulse Detector |
| DP8465 | (NS 32965) | Data Separator |
| DP8470 | (NS 32970) | Floppy Disk Data Separator |
| DP8472 | (NS 32972) | Floppy Disk Controller Plus |

So whatever type of high-performance disk product you're designing, look to National for the complete controller solution. We can help you get to market quickly. Without spinning your wheels.

For full details, contact your local National office today.

National Semiconductor Corporation, MS/23-200, P.O. Box 58090, 2900 Semiconductor Drive, Santa Clara, CA 95052-8090 (408) 721-5893

Advanced Peripheral Processing Solutions APPS™

National Semiconductor Corporation

Drives courtesy of Control Data Corporation and Rodime, Inc.
APPS is a trademark of National Semiconductor Corporation.
Series 32000 is a registered trademark of National Semiconductor Corporation.




Circle 1 on reader service card

MITEL SEMICONDUCTOR

# ISDN

COMPONENT NEWS

Vol. 3

# Bypass Your Competition With T1/CEPT Access Components To ISDN By Mitel

Demand for T1/CEPT communications facilities is opening unprecedented opportunities for your MUX, LAN, Data Switch, PBX or other communications product.

T1/CEPT Interfaces belonging to the Mitel *ST-BUS*™ family of ISDN-compatible components can provide the competitive edge you need with:

- The smallest size and lowest cost per function in the industry.
- Redundant links at the same price as our competitors' single link interfaces.
- DMI and CPI compatibility.
- Software-controlled diagnostic and maintenance functions.
- Drop and insert capabilities.
- Signaling selection options for simultaneous voice, data and video transmission over a single T1/CEPT link.

The following devices offer a variety of functional and packaging choices that will minimize the cost, time and complexity of your design-in:

- **MT8974/75** – T1 Interface ICs with extensive interface support functions.
- **MH89740/50** – T1 Interface Module with Clock extraction and line equalization.
- **MH89756** – T1 Interface Module with line coupling transformers, microprocessor control port, time slot switching, clock sources and PLL synchronization.
- **MH89780/785** – CEPT family of 2.048 Mbit/s interface components that functionally are compatible with our T1 Interfaces.

Don't let the opportunity bypass you – pick up the phone now and talk with us about worldwide Primary Rate Access.

MITEL® SEMICONDUCTOR

**UNITED STATES** – San Diego, California. Telephone: (619) 276-3421. San Jose, California. Telephone: (408) 249-2111. Oakbrook, Illinois. Telephone: (312) 655-3930. Boca Raton, Florida. Telephone: (305) 994-8500. **CANADA** – Kanata, Ontario. Telephone: (613) 592-5630. **UNITED KINGDOM** – Portskewett, Newport, Gwent, South Wales NP6 4YR. Telephone: +44 291-423355. **ASIA** – Tsuen Wan, Hong Kong. Telephone: +852 0-463641. **EUROPE** – Denmark. Telephone: +45 1-612566. Milan, Italy. Telephone: +39 2-8245222/8245177. West Germany. Telephone: +49 711-7701522.

Circle 2 on reader service card

MAY 19, 1986 VOLUME 59, NO. 20

# Electronics

## NEWS



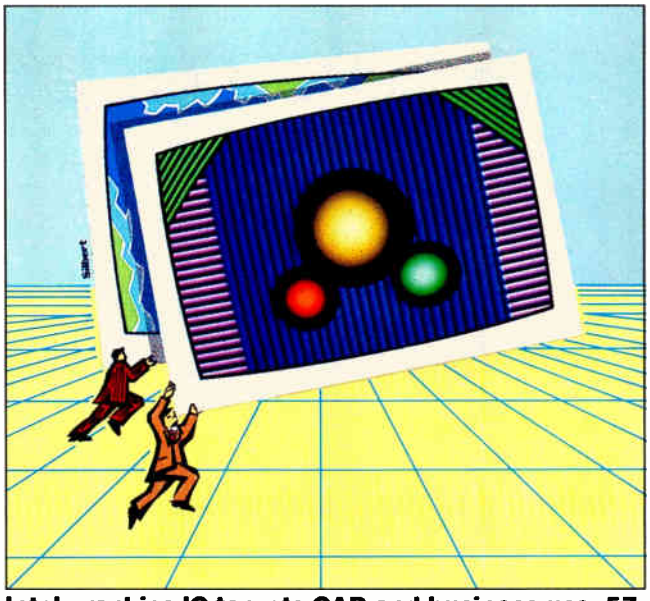
## INSIDE TECHNOLOGY



## PROBING THE NEWS



## COVER





*Cover art by Bill Silbert*

## NEW PRODUCTS



## DEPARTMENTS

# A TO D FOR YOUR HP

## The Analog to Digital Converter for HP Series 200/300 Computers.


When you want to do analog to digital conversion on your HP 9000 Series 200/300 computer, you don't have a lot of choices. So fortunately, one of the few choices you do have is the Infotek AD 200 data acquisition card.

Fast and easy to use, the AD 200 performs 12 bit analog to digital conversion and features 16-channel input while occupying only a single I/O slot. Sample rates are as high as 200,000 samples per second (using HP's DMA card) with little degradation during multi-channel scanning—ideal for test and measurement, structural analysis and a range of other applications. Installation of the AD 200 is easy and multiple cards can be chained together to meet more complex requirements. Interfacing is accomplished using one of three optional mating connectors.

Because the AD 200 is an intelligent interface, it operates independently of the computer, except during data transfer. And it doesn't require special programming. The AD 200 uses simple ASCII commands and communicates using HP's standard GPIO protocol.

As with all Infotek HP enhancement products, the AD 200 demonstrates its exceptional reliability with a full two-year warranty. So when you need A to D for your HP, make the one choice that's the best choice. Call Infotek Systems today at (800) 227-0218, in California (800) 523-1682 or (714) 956-9300, 1400 North Baxter Street, Anaheim, California 92806-1201, TELEX 182283.

Circle 4 on reader service card

**INFOTEK SYSTEMS**
A DIVISION OF ALS CORPORATION

**Your Second Right Decision.**

**TEAN.** Editors Cole, McLeod, and Barney in front of new office.

We have moved our Silicon Valley bureau from Palo Alto to more spacious quarters 11 miles up the San Francisco peninsula in San Mateo. Now there will be plenty of room for bureau chief Cliff Barney, semiconductor editor Bernie Cole, and test & measurement editor Jonah McLeod.

The move was something that Cliff is not eager to repeat soon. Moving is a headache, he says, and moving a whole office is Excedrin headache No. 432. "Everything has to be packed and labeled, then unpacked and stored in unfamiliar places, while business proceeds as normal," he grumbles. "It's like trying to file papers with the fan on."

Nevertheless, the pleasant new surroundings go a long way toward making the move worthwhile, Cliff reports. Also, the San Mateo location is between Silicon Valley and San Francisco, and though it puts the valley 10 minutes farther away, it is more central to other facilities—it's just a mile from the San Mateo Bridge to the East Bay and near the San Francisco airport.

The move itself went smoothly. "We left Palo Alto on a Friday afternoon and then just showed up for work at San Mateo the next Monday," Cliff reports.

There are still problems with a new phone system, and some office renovations and unpacking are still going on. But most of the old editorial routines have been re-established, and a new one has been added. "The new building has a health club," Cliff says. "Instead of taking a lunch hour, I can jog, exercise, and shower. It's a lively way to break up the day."

Like every move, this one had its misadventures. Among the items to be packed, Cliff explains, were several shelves of bound volumes of *Electronics*, dating back to the 1960s. "We rarely look at them, and they wound up stacked at the very rear of the storeroom."

Naturally, among the first calls received at the new office was one requesting information from the Dec. 2, 1960, issue. It hasn't been found yet.

The bureau's new address is:
951 Mariner's Island Boulevard
San Mateo, Calif., 94404
Telephone: 415-349-4100

Laurence Altman


*May 19, 1986 Volume 59, Number 20*
*95,322 copies of this issue printed*

Electronics (ISSN 0883-4989). Published weekly by McGraw-Hill Inc. Founder James H. McGraw 1860-1948. Publication office: 1221 Avenue of the Americas, N.Y., N.Y. 10020; second-class postage paid at New York, New York and additional mailing offices. Postage paid at Montreal, P.Q. Registration Number 9034.

Executive, editorial, circulation, and advertising addresses: Electronics, McGraw-Hill Building, 1221 Avenue of the Americas, New York, N.Y. 10020 Telephone (212) 512-2000. Teletype 12-7960 TWX 710-581-4879. Cable address: MCGRAWHILL NEWYORK

Subscriptions limited to professional persons with active responsibility in electronics technology. No subscriptions accepted without complete identification of subscriber name, title or job function, company or organization, and product manufactured or services performed. Based on information supplied, the publisher reserves the right to reject nonqualified requests. Subscription rates, the United States and possessions $32 one year, $55 two years, $76 three years; company addresses and company libraries $40 one year, $67 two years, $93 three years; Canada and Mexico $34 one year, $57 two years, $78 three years; Europe $50 one year, $85 two years, $125 three years; Japan, Israel, and Brazil $85 one year, $140 two years, $200 three years; Australia and New Zealand $95 one year, $170 two years, $240 three years, including air freight; all other countries $50 one year, $85 two years, $125 three years. Limited quota of subscriptions available at higher-than-basic rate for persons allied to field served. Check with publisher for these rates. Single copies $3.00. Please allow four to eight weeks for shipment.

Officers of McGraw-Hill Information Systems Company: President: Richard B. Miller, Executive Vice Presidents: Frederick P. Jannot, Construction Information Group; Russell C. White, Computers and Communications Information Group; J. Thomas Ryan, Marketing and International; Senior Vice Presidents: Francis A. Shinal, Controller, Robert C. Violette, Manufacturing and Technology; Senior Vice Presidents and Publishers: Laurence Altman, Computers and Communications; Harry L. Brown, Computers and Communications; David J. McGrath, Construction; Group Vice President: Peter B. McCuen, Communications; Vice Presidents: Fred O. Jensen, Planning and Development; Margaret L. Dagner, Human Resources.

Officers of McGraw-Hill Inc.: Harold W. McGraw Jr., Chairman; Joseph L. Dionne, President and Chief Executive Officer; Robert N. Landes, Executive Vice President and Secretary; Walter D. Serwatka, Executive Vice President and Chief Financial Officer; Shel F. Asen, Senior Vice President, Manufacturing; Robert J. Bahash, Senior Vice President, Finance and Manufacturing; Ralph R. Schulz, Senior Vice President, Editorial; George R. Elsinger, Vice President, Circulation; Ralph J. Webb, Vice President and Treasurer.





Subscribers: The publisher, upon written request to our New York office from any subscriber, agrees to refund that part of the subscription price applying to copies not yet mailed. Please send change-of-address notices or complaints to Fulfillment Manager; subscription orders to Circulation Manager, Electronics, at address below. Change-of-address notices should provide old as well as new address, including zip codes. Attach address label from recent issue. Allow one month for change to become effective. Subscriber Service: call (201) 356-7980, 9 a.m. to 4 p.m. EST. Postmaster: Please send address changes to Electronics, att. Fulfillment Manager, CN 608, Martinsville, N.J. 08836.

**Editorial department phones:** Administration (212) 512-2645, News and New Products (212) 512-2685, Technology (212) 512-2666. Bureaus: Boston (617) 262-1160, Chicago (312) 751-3811, Dallas (214) 458-2400, Los Angeles (213) 480-5234, New York (212) 512-3322, San Francisco/San Mateo (415) 349-4100, Washington (202) 463-1650, Frankfurt 72-5566, London 493-1451, Paris 42-89-03-80, Tokyo 581-9816. **Business departments:** (212) 512-3469 (Business departments follow the Advertisers' Index).

# WEEK 30

Introducing the Am29C01 4-Bit CMOS Microprocessor Slice. The latest CMOS part of AMD's 2900 family. Advanced Micro Devices created the 2900 phenomenon in the first place. So you can count on the Am29C01 being a product of elegant engineering.

Because the Am29C01 is in CMOS, it uses a mere 25% of the power used by the bipolar version. But it doesn't ask you to give up anything in performance. Anything.

**Am29C01**

## The arrival of the fittest.

And this new breed is the quick, cool, multi-talented, plug-in replacement for our industry standard Am2901. It comes in PLCC and LCC packages. And a military version will soon be available.

The Am29C01, Am29C10 and the Am29C101 are here now. Soon you'll be able to get the Am29C116/117 and the Am29C516/517. All so you can create the next generation of high performance, cooler boards.

So keep up with evolution. Give AMD a call.

Design and application seminars are available for this product. Write or call for information.

Circle 151 on reader service card

# WEEK 31

Introducing the Am29331—the fastest 16-Bit Interruptible Microprogram Sequencer anywhere. It's the second member of AMD's remarkably fast, ingeniously-designed Am29300 family.

**Am29331**

## Real time needs unreal speed.

The Am29331 has Real Time Interrupt. By building in Test Generation Logic (which no one else does), we cut down on chips and allow for faster system cycle time. Without having to wait for the additional cycle you usually need to accommodate an interrupt, you get faster throughput.

More reasons why the speed stays white hot: Errors can't get too far in the Am29331. They're detected at the source, not at the memory level. It's transparently interruptible at any microinstruction boundary, and Built-in Trap Handling insures speedy re-execution.

The Am29331 16-Bit Interruptible Microprogram Sequencer is just one of AMD's 29300 family. Other members of the family are the Am29332 32-Bit ALU and the Am29334 Four Part Dual Access Register File.

You can use the Am29331 with non-family members if you must. Just make sure the microprocessor you choose can keep up with it.

Design and application seminars are available for this product. Write or call for information.

Circle 152 on reader service card

# WEEK 32

There are two things every mother board should have: The 82C54 CMOS Counter Timer and the security of knowing there's a complete second source mother board kit to the Intel 286 PC/AT package. And AMD is proud to hold high the banner for motherhood by announcing both.

**82C54**

## Every mother needs them.

The 82C54 is a general purpose microprocessor peripheral. With low CMOS power, dissipation is only 6% of NMOS parts. The 82C54 is also very fast—it operates at 8 and 10MHz. And naturally, it's a plug-in replacement for Intel's part.

But just as important as the 82C54 CMOS Counter Timer is the fact that you finally have a second source for the 286PC/AT mother board kit. Along with the Counter Timer, the kit contains an 82284 Clock Generator, an 82C288 Bus Controller and an 80286 CPU. But best of all, once you're in production, you don't have to worry about availability, quick delivery and all the other things you worry about when you don't have a second source.

So get up and call AMD: The mother board's little helper.

Circle 153 on reader service card

# WEEK 33

If you hate waiting around crowded registers, AMD's new Am29524 Dual 7-Deep Pipeline Register is for you. It's designed for applications that need ground or data pass-through. So now your input data can fly directly to the output or your output can be all zeroes.

**Am29524**

## Direct flights.

The Am29524 has 14, not 16, registers like the Am29525. But it shares many of the same attributes. With the Am29524 you can dip into the data registers in any order, at any time. You could think of it as a random access register. It's programmed by microcode instructions to hold, shift or load data. Its internal ECL technology gives the Am29524 incredible speed (it has a 21ns propagation delay) and the I/O is three-state TTL compatible.

Need to get rid of some excess baggage like a register and bus buffer? The Am29524 does the work of both. And we packed it all in a 28-pin DIP package.

Flying the Am29524 isn't for just everyone. Only the people who want to travel direct.

On October 1, 1985, Advanced Micro Devices told the world it would deliver fifty-two new products in one year. A new product every week. Tall order.

So where's seeking the impossible gotten us? Right where we expected. After twenty-six weeks, we're 26 for 26. Batting a cool 1,000. And here's what the world is telling us:

"Reduced networking costs." "State machines that have simplified the state-of-the-art." "More powerful, smaller air traffic control systems." "Extraordinary graphics for ordinary workstations." "PC's with fax capabilities."


And more. But that's only half the story. Watch this space for more chances to make your best idea better than you hoped it could be.

More new products. One a week. Every week. On the shelf. In volume.

Watch us open up the lead.

**Advanced Micro Devices**

901 Thompson Place, P.O. Box 3453, Sunnyvale, CA 94088
Call toll free (800) 538-8450, ext. 5000, inside California, call (408) 749-5000.



Circle 154 on reader service card

## LETTERS

### A honey of an array

**To the editor:** Though generally outstanding, "Special Report: VLSI Gives Bipolar a Second Wind" [*Electronics*, April 7, 1986, p. 24] had a few numbers and references wrong. The ADB-III is a 1.25-μm bipolar process, not 1.5 μm, and the HE8000 gate array combines current-mode logic with emitter-coupled-logic input/output buffers, not integrated Schottky logic. Our new business unit is the Signal Processing Technologies Center; the word "Digital" is not part of the name.

*David G. Wick*
*Digital Product Center*
*Honeywell Inc.*
*Solid State Electronics Division*
*Colorado Springs*

### A matter of class

**To the editor:** Your article about Performance Semiconductor Corp. [*Electronics*, April 7, 1986, p. 14] says the company has a Class 2 clean room, and the accompanying photo shows the room. I see two cushioned chairs, which make it impossible to maintain Class 2 status. Operators getting on and off the chairs will stir up particles, and that alone would make it a Class 100 or 1,000 facility. Class 2 equipment will not alone make any facility Class 2—environmental factors count also.

*Ashok Kumar*
*Austin, Texas*

*Performance Semiconductor president Thomas A. Longo says the Class 2 designation results from measurements taken with laser counters at 11 strategic areas with people at work. The resulting average was 1.6 particles measuring 0.2 μm/ft³.*

### That's Bellcore!

**Correction:** *In the April 28, 1986, issue, the headline "Bell Labs Finds a Better Way to Speed Up CMOS" (p. 20) is incorrect. Work described in the article is being done at Bell Communications Research, the arm of the seven regional Bell operating companies. Bellcore was spun off from AT&T Bell Labs.*

### Chicago site for ICCE

**Correction:** *The correct location for the June 4-6 International Conference on Consumer Electronics is the Westin Hotel-O'Hare, just outside Chicago (April 28, 1986, p. 66).*

### The name game

**Correction:** *In the May 12, 1986, article on the Data General One Model 2, the names of Robert Miller and Ronald W. Pipe are transposed underneath their photographs (p. 36).*

# TECHNOLOGY NEWSLETTER

## SUPERCONDUCTIVE MAGNETS COULD CUT GaAs PRODUCTION COSTS

Superconductive magnets are the key to a method that may lower the production cost of gallium arsenide wafers to one third that of current techniques, say Toshiba Corp. researchers. Last week, Toshiba announced that the method had yielded 3-in. ingots from which 50 usable wafers can be sliced. Toshiba began using the new process for limited in-house use last fall, and the Kawasaki, Japan, company expects to make a decision on volume production in the near future. Toshiba's technology applies a 3,400-Gauss magnetic field to the furnace, and that helps hold temperature variations of ingots to within 0.5°C, compared with a range of 15°C for earlier methods. □

## TUNGSTEN-ZIRCONIUM GUN SPEEDS SUBMICRON MASK WRITING

Speeding submicron lithography by a factor of 10, a new tungsten-zirconium thermal-field emission gun developed by researchers at AT&T Bell Laboratories in Murray Hill, N. J., is helping AT&T Co. in its drive toward 0.5-μm technology (see story, p. 21). The gun is the main feature of EBES4, the upcoming generation of machines based on the electron-beam exposure system (EBES), which became a de facto standard in 1975 when AT&T licensed the technology for commercial use. Current-generation EBES3 machines can take four to five hours to process a single 4-in. reticle coated with resists that have a sensitivity of about 8 $\mu C/cm^2$, according to James Clemens, head of the Lithographic Technology Department at Bell Labs. He says the new system, which uses the same operating system, can process the same substrate in only 30 min because of its higher-power electron beam. The emission gun, when heated to 1,800 K and excited with 20,000 V, produces a fixed beam of 250 nA on a 0.125-μm spot. That beam can write 1.25-μm lines on reticles and, when used in direct-write applications, can go down to 0.125 μm. □

## GERMANS PRODUCE COMMERCIAL DEVICES USING X-RAY LITHOGRAPHY

Three West German electronics organizations are making progress in efforts to make synchrotron X-ray lithography feasible, having fabricated what they say are the first commercially practical devices. The synchrotron X-ray technology allows submicron features and a resolution down to 0,1 μm with minimum scattering effects and little diffraction. The devices that Telefunken electronic GmbH in Heilbronn, the AEG Research Center in Ulm, and the Fraunhofer Institute for Microstructure Technology in West Berlin (where the synchroton is located) have produced are dual-gate n-MOS FETs with 1-μm gate lengths for operation at frequencies up to 1.2 GHz. In the just-begun second stage of the X-ray lithography program, MOS FETs with 0.5-μm gate lengths and gallium arsenide metal-semiconductor FETs with 0.3-μm gate lengths will be made. □

## FINNISH TEAM SEES WAY TO CUT ETHERNET DOWNTIME

A team of Finnish engineers thinks it is on to a solution for one of the major disadvantages of Ethernet local-area networks. The group from the Tampere University of Technology has a scheme that is aimed at significantly reducing or even eliminating the downtime that occurs in a network after a collision of the signals. By terminating the transmission fiber of each station connected to an Ethernet highway in two-branch couplers, the system permits incoming and outgoing data to be identified and controlled. In this way, it ensures that each station transmits into a free time slot, eliminating collisions. The prototype network has a 20-megabaud line rate and it can be used as a direct replacement for current Ethernet LANs. □

# YOU CANNOT OUTDISTANCE CONTROL DATA.

No one covers more ground than Control Data. There is no other OEM supplier of data storage peripherals in the world who is larger or more experienced. And no other who can give you more choices or support.

There is no other supplier in the world who can give you a broader selection of high capacity, high performance, high quality storage products. In total, we offer over 50 different configurations of size, capacity and interface. From our Wren™ series—the largest-selling high capacity 5¼ inch drive in the industry. Through our ultra-fast XMD—the highest capacity rack mount disk drive in the world. To our LaserDrive™ 1200—utilizing the latest in optical technology.

No other support program, foreign or domestic, is as far-reaching as ours. With worldwide applications engineering, training, parts, and field service, Control Data will make sure you are never left in need.

Being the world's leading OEM supplier is a serious responsibility. With sales more than twice that of our nearest competitor, we listen. Because your success is our success.

That's why, we've launched a steady stream of new products. Better. Faster. Smaller. More. More new, more reliable products, than ever before.

So no matter what direction you're headed in the OEM market, you can count on Control Data to always be a step ahead. For more information write Control Data Corporation, OEM Marketing (HQW08X), P.O. Box 0, Minneapolis, MN 55440.

CONTROL DATA

Circle 11 on reader service card

# The INMOS 256K CMOS DRAM. Feel the exhilaration of unparalleled speed.

INMOS sets performance standards again with the new IMS2800 family of second generation 256Kx 1 DRAMS. It's upwardly compatible with 64K x 1 and first generation 256K devices.

With $\overline{RAS}$ access times of 60 to 150ns and cycle times down to 121ns, the IMS2800 family maximizes the speed-power benefits of CMOS without compromising traditional DRAM system costs.

INMOS continues to lead with an address multiplexing scheme that eliminates timing constraints while reducing speed loss associated with traditional DRAM designs. INMOS' unique 2ns Row Address hold time saves 10 to 15ns in the address multiplexing sequence. This, in addition to Static Column mode accessing, allows no wait state operation with the new generation of fast 32 bit microprocessors including Motorola's 68020, Intel's 80386 and our own T414 Transputer.

The IMS2800 from INMOS. Experience the speed for yourself.

| Part Number | Function | Address Access Time (Max.) | $\overline{RAS}$ Access Time (Max.) | $\overline{RAS}$ Read/Write Cycle Time (Min.) |
|---|---|---|---|---|
| IMS2800-60* | Static Column Decode | 32ns | 60ns | 121ns |
| IMS2800-80 | | 43ns | 80ns | 146ns |
| IMS2800-10 | | 53ns | 100ns | 176ns |
| **Part Number** | **Function** | **Column Access Time (Max.)** | **$\overline{CAS}$ Access Time (Max.)** | **Page Mode Cycle Time (Min.)** |
| IMS2801-60* | Enhanced Page Mode | 32ns | 11ns | 35ns |
| IMS2801-80 | | 43ns | 13ns | 46ns |
| IMS2801-10 | | 53ns | 16ns | 56ns |

Data on Nibble Mode and Extended Serial Mode versions available upon request.

*Contact factory for delivery.

INMOS, Colorado Springs, Colorado, Tel. (303) 630-4000
Bristol, England, Tel. 0272-290-861
Paris, France, Tel. (1) 4 687-2201
Munich, Germany, Tel. (089) 319-1028.

inmos®

When you're ready to cool down your competition, call INMOS.

INMOS, Transputer, and IMS are trademarks of the INMOS Group of Companies.

# ELECTRONICS NEWSLETTER

## FCC FREES BOCs AND AT&T IN COMPUTER INQUIRY III DECISIONS

The Federal Communications Commission last week adopted the key provisions of its landmark Third Computer Inquiry, thereby freeing the regional Bell operating companies and AT&T Co. to offer enhanced services, such as packet switching and voice storage, without structural separation from their basic phone services. As expected, the order will replace the separate, arm's-length subsidiary requirements for enhanced services imposed in Computer II with accounting safeguards designed to prevent cross-subsidization by revenues from basic services. The regional operating companies must still go before Federal District Court Judge Harold H. Greene, who is overseeing their entry into competitive ventures. In addition, the FCC formally endorsed the controversial concept of "comparably efficient interconnection" [*Electronics*, Feb. 17, 1986, p. 17] as a way of ensuring that all enhanced-services providers have equal access to the regional operating companies' monopoly central-office switching facilities. The commission also said it will consider whether protocol conversion should be an adjunct to the basic or enhanced regulatory framework or whether it should be handled separately. □

## JAPAN LAUNCHES OPTOELECTRONIC IC PROJECT

Japan is stepping up its efforts in optoelectronics by organizing another massive national technology project, this one in integrated circuits for communications and computer use. The project goals are to develop optoelectronic ICs to be used as transmitters and receivers on chips, thus eliminating the need for wiring between them, and to develop microprocessing technology capable of increasing transmission speeds to 10 Gb/s from the present 1 Gb/s. The government-supported Japan Key Technology Center in Tokyo heads the 10-year project, which includes Fujitsu, Hitachi, Mitsubishi Electric, Nippon Sheet Glass, and Toshiba. The effort is capitalized at about $90 million for its first year, which starts in June. The center will share subsequent costs with the private companies. □

## MORE U.S. CHIP CUSTOMERS ARE ROLLING THEIR OWN

As if U.S. semiconductor makers didn't already have enough to worry about, it is becoming apparent that some of their best customers are producing more chips internally. The latest breakdown from consultant In-Stat Inc. underscores what could be an important shift: in 1985, captive semiconductor operations supplied 36.7%, or some $4.69 billion worth, of the total U.S. chip consumption. Although the contraction in the merchant market during 1985 partially explains the sharp increase from a 29.6% share for captive operations in 1984, In-Stat believes it is no one-time occurrence. The Scottsdale, Ariz., company projects that captive sales will grow to some 38.3% this year. Sources say major users are intent on producing more integrated circuits internally, and new orders to suppliers of semiconductor-manufacturing equipment already reflect this trend. □

## A BIG DESIGN WIN FOR A FAST NEW CHIP SET

Look for the next generation of three-dimensional color work stations from Silicon Graphics Inc. to significantly surpass the 86,300 transformations/s of the current generation. The Mountain View, Calif., company will use the just-introduced 10-million-instructions/s chip set from Mips Computer Systems Inc. [*Electronics*, May 5, 1986, p. 56] instead of the Motorola 68020 it is now using. Like the 2.5-mips 68020, the Mips chip set supports AT&T Bell Laboratories' Unix. The original-equipment-manufacturer agreement is valued at $15 million over three years, Silicon Graphics says. □


# Only one company is ready to ship Data Acquisition products for MicroVAX II.

Data Translation is ready to ship today. Hardware. Software. A full range of data acquisition solutions for the new MicroVAX II for scientific and industrial applications.

Call now for delivery in five days or less. But, please, be quiet, others are sleeping.

**MicroVAX II Data Acquisition Boards and Software**

| Product Characteristics | Model Numbers | Features | Software Support |
|---|---|---|---|
| Polled or Interrupt driven Analog I/O | DT2762 ADV11-C | 12-16 bit resolution, 50kHz, A/Ds 10mV-10V inputs, up to 64 channels | MicroVMSLIB |
| | DT2766 AAV11-C | 4 12-bit D/As per board Settling time 3us per DAC | MicroVMSLIB |
| | DT2781 DT2785 AXV11-C | A/D and D/A boards – 12-16 bit resolution A/Ds, 8DI/16SE, 10mV to 10V input, 2 12-bit D/As | MicroVMSLIB |
| Analog I/O with Continuous Performance DMA | DT2752 DT2757 | 12-16 bit resolution A/Ds, up to 8DI/16SE, throughput up to 250kHz, and programmable gain | MicroVMSLIB |
| | DT3382 | 12-bit A/D, up to 32DI/64SE throughput up to 250kHz, m to n channel scans, and programmable gain | MicroVMSLIB |
| Digital I/O | DT2751 | Two 12-bit D/As designed for waveform generation and point-plotting | MicroVMSLIB |
| | DT2768 DRV11 | Digital I/O board with 16 input and 16 output lines | MicroVMSLIB |
| | DT2769 | KWV11-C equivalent. Real-time clock | MicroVMSLIB |

Continuous Performance is a patented technique of Data Translation for the collection or output of large amounts of data without losing a single data point.

## Call (617) 481-3700


**See our new 646 pg. catalog/handbook or see us in Gold Book 1986. Or call for your personal copy today.**

FIVE DAY 5 DELIVERY

# DATA TRANSLATION

**World Headquarters:** Data Translation, Inc., 100 Locke Dr., Marlboro, MA 01752 (617) 481-3700 Tlx 951 646
**European Headquarters:** Data Translation, Ltd., 13 The Business Centre, Molly Millars Lane, Wokingham Berks, RG11 2QZ, England Tlx 851849862 (#D)
**International Sales Offices:** Australia (61) 2-6635289; Belgium (32) 2-7352135; Canada (416) 625-1907; Chile (2) 2-253689; China (408) 727-8222, (86) 87214017; Denmark (02) 187188; England (44) 0734-793838; Finland (358) 0-372-144; France (33) 146306839; Greece (30) 031-527039, (30) 13-614300; Hong Kong (852) 3-324563; India (91) 2-231040, Israel (972) 3-324298; Italy (39) 2349751; Japan (81) 3-502-5550, (81) 3-348-8301, (81) 3-355-1111; Korea (82) 753-3101; Malaysia (60) 3-362-99; Morocco (21) 9-30-6949; Netherlands (31) 70-96360; New Zealand (61) 2-663-5289; Norway (47)(02) 559050; Peru (51)(14) 31-8060; Philippines 818-0103, 818-3073, 818-4230; Portugal (351) 1545313; Singapore (65) 271-3163; South Africa (27) 12469221; Spain (34) 14558112; Sweden (46) 87617820; Switzerland (41) 17231410 (41) 22360830; Taiwan (86) 2-721-7864, (86) 2-531-2434; West Germany (49) 89809020.



Circle 14 on reader service card

# PRODUCTS NEWSLETTER

## NOW THERE ARE CHIP SETS FOR SCSI AND ESDI DISK-DRIVE CONTROLLERS

Designers of SCSI and ESDI disk-drive controllers can throw away their discrete logic: Silicon Systems Inc. is introducing a set of 11 chips that, with a microprocessor and RAM, will handle all electronic functions for high-performance Small Computer Systems Interface disk drives. The Tustin, Calif., company plans to make the SCSI set available in surface-mountable packages by fall for $160 in large quantities. It will also offer a nine-chip set for the Enhanced Small Disk Interface for $130 beginning in late summer. Both chip sets will perform such functions as read/write, control and interface, servo-head positioning, and motor control. □

## TI WILL ENTER ECL MARKET WITH BIT-SLICE PROCESSOR

Texas Instruments Inc. will be entering the emitter-coupled logic market with a family of very large-scale integrated bit-slice processors and other logic circuits fabricated in TI's 1.5-μm Impact-X process. The processors, fabricated in 10K and 100K ECL technology, are enhanced versions of TI's 74AS888 advanced Schottky chip and can as much as quadruple performance of TTL systems, to 50 million instructions/s. This performance level is based on a 20-ns instruction cycle time, which is achieved at a power dissipation level of about 5 W. To be available in the third quarter, the chips will be priced in the $50 to $60 range. □

## HONEYWELL PACKAGE MAKES IT EASIER TO DESIGN MAP NETWORKS

A turnkey hardware and software package from Honeywell Inc. will ease development of factory networks based on the Manufacturing Automation Protocol. Mapstart will enable network manufacturers to program, simulate, and test MAP-compatible nets that incorporate equipment from multiple vendors. It uses Honeywell's 68000-based WCC 1250 work-center controllers and will be available in two to three months for around $176,000. Honeywell's Manufacturing Systems Division, Phoenix, Ariz., announced Mapstart at last week's MAP Users Group meeting in Seattle. □

## TOSHIBA'S CMOS STANDARD LOGIC IS AS FAST AS TTL

Toshiba Corp. will soon market advanced CMOS standard-logic ICs that are speedy enough to replace the fastest TTL products now used in computers and telecommunications equipment. The new TC74AC series is designed with 1.5-μm rules and features typical propagation-delay times of 3 ns with buffered gates—about the same as TTL—and a maximum clock frequency of 150 MHz. At 0.01 μW on standby, the Toshiba ICs use less than 1/100th the power of TTL, while providing an equivalent output current drive of 24 mA. The Kawasaki, Japan, company will begin delivery in August. Prices range from 60¢ to 80¢, about the same as for TTL. □

## A MESSAGE SYSTEM THAT USERS TAILOR TO THEIR APPLICATIONS

The first product from Comverse Technology Inc. is a voice-message management system that aims at easy customization. The key is the system's dialogue generator, which supplies audio menus and verbal prompts. Working with these, users can create custom applications—for example, an audio form that allows a salesperson to call in orders to a computer. The system, named Trilogue, enables a standard tone-key telephone to access such applications as voice mail, call screening, and text-mail integration. The system is available now from the Woodbury, N. Y., company in three configurations, offering 8 to 70 hours of storage with prices from $35,000 to $185,000. □

Electronics

# NOW THERE'S A U.S. CHAMPION FOR JAPANESE CHIP MAKERS

## SANCTIONS ARE COUNTER-PRODUCTIVE, SAYS OKI'S CROWLEY

**PHOENIX, ARIZ.**

There has been something missing this past year in public discussions of the trade imbalance in semiconductors between Japan and the U.S.: a forceful advocate of the Japanese position. Now, it looks as if Jerry R. Crowley, president and chief executive officer of Oki Semiconductor Inc., the U.S. subsidiary of Tokyo's Oki Electric Industry Co., is opening a campaign to defend the Japanese semiconductor industry.

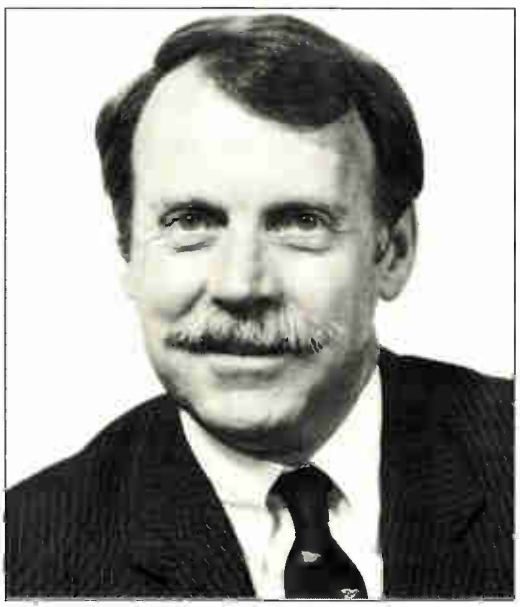
Observers agree that in defending the trade disparity in the semiconductor business, Crowley became the first well-known industry figure to take such an unpopular stance—publicly, at least. But he did more than explain the Japanese position. Crowley, in fact, predicted dire consequences for U.S. companies if present antidumping sanctions and legal actions addressing the trade imbalance continue against the Japanese.

"The temporary relief provided to the American semiconductor industry by U.S. government action will be offset by fiercely competitive Japanese-owned manufacturing facilities located in the U.S.," says Crowley. An equally unsavory outcome would be U.S. manufacturers moving assembly operations offshore to Pacific Basin countries to buy components more cheaply than in the U.S., and at the same time dodging protectionist charges. This move would "reduce the American semiconductor salesman's access to orders and will provide Japanese salesmen new customer access," he warns.

So far, sanctions include posting cash deposits or bonds equal to the estimated dumping margins for erasable programmable read-only memories and 256-K dynamic random-access memories. These sanctions are the result of a preliminary determination by the Commerce Department; its final determination is due May 27. The International Trade Commission will probably make its final decision on these cases by July. Preliminary rulings by both Commerce and the ITC also favor the U.S. complainant—Micron Technology Inc. of Boise, Idaho—in a 64-K DRAM dumping charge.

In addition, the ITC is investigating a complaint filed on Jan. 24 by Texas Instruments Inc. charging that eight Japanese companies, including Oki and one South Korean company, are violating TI's semiconductor patents. The same day, TI filed a patent-infringement lawsuit in federal court against the Japanese and Korean companies.

The Japanese garnered 11.9% of U.S. semiconductor sales in 1985, while the U.S. had only an 8.9% share of the Japanese market, according to the Semiconductor Industry Association. The disparity might not seem large enough to raise such a ruckus, but the realistic U.S. market share would be about 30% if equal access were given, say SIA officials. This is the average share held by U.S. chip makers in other offshore markets. Japanese officials have offered the U.S. a 14% share, says Crowley, but were turned down by U.S. negotiators.



**FILLING A VOID.** Crowley has become the first well-known industry figure to defend Japan's trade practices.

Not surprisingly, Crowley's remarks at market consultant In-Stat Inc.'s annual semiconductor forum [*Electronics*, May 12, 1986, p. 15] raised the hackles of many of the 200 top-rank executives in attendance. "It's pretty much an apology for Japan Inc.," says SIA president Andrew Procassini. He took the Crowley appearance seriously enough to address the major points in detail during a quickly scheduled speech of his own the next day. One reason, even Crowley's critics agreed, is that the Oki executive came across very effectively.

**ADVERSARIAL CHARGE.** Procassini's major argument against Crowley's speech is that it deliberately ignores the causes of the trade disparity. "What this is about, and specifically why the cases were filed, is access to the Japanese market and dumping into the U.S.," says the SIA president. He charges the Japanese with conducting "adversarial trade . . . a Japanese practice since MacArthur got on the plane to come home [in 1951]." The root of both the access and dumping issues, he maintains, is that "they are building capacity at 35% a year in an industry growing at nearly 20%."

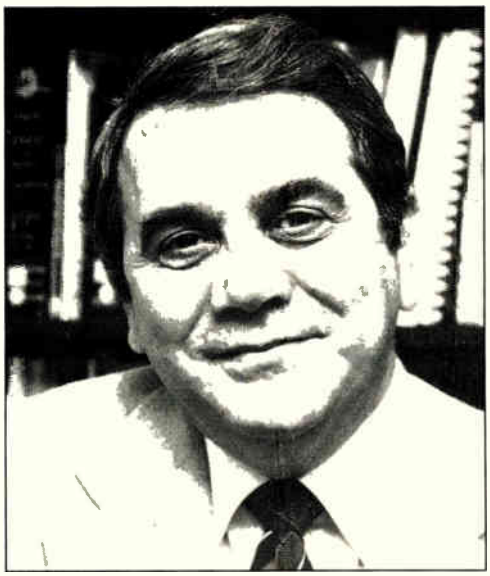
Crowley's predictions about the adverse effects of dumping sanctions against Japanese semiconductor companies also were challenged by representatives of U.S. industry. Douglas L. Powell, vice president and director of strategic marketing at Motorola Inc.'s Semiconductor Sector, offered a typical observation: "I don't agree. They [dumping penalties] already are having an effect and will have even more."

Powell notes that the ITC ruling against Japanese companies for dumping 64-K and 256-K DRAMs is acting as a restraint on their sales efforts in the U.S. In addition, he and others say that U.S. systems companies already had been moving offshore at an increasing rate before the chip cases surfaced, and will continue no matter what.

Crowley's explanation of why U.S. semiconductor makers cannot seem to sell to Japanese customers also irritated the audience's especially sensitive nerve endings. According to the Oki official, U.S. manufacturers lack low-cost CMOS chips to address the Japanese consumer-products segment, which, at about 44%,

is the largest part of the Japanese semiconductor market: "The problem is, what will U. S. manufacturers market in Japan? They are neither currently producing nor have they stated they will produce these [consumer] products."

This statement evoked spirited responses from such industry veterans as John R. Welty, a retired Motorola executive and founder of the SIA, who also was a speaker. "That consumer stuff may be true now, but it doesn't mention why. We sold them consumer devices for years, until they kicked us out 20 years ago. Does anybody think we couldn't build them now if the Japanese would buy?" Adds SIA's Procassini, "That 44% argument doesn't make any sense."



**REBUTTAL.** SIA's Procassini sees Crowley's contentions as "pretty much an apology for Japan Inc."

An example of the kind of consumer chips Japanese manufacturers need but can't get from the U. S. is advanced, low-cost circuitry to control 35-mm cameras, according to Crowley. "That's simply ridiculous," scoffs Delbert Whitaker, senior vice president of TI's Semiconductor Group. He points out that TI now sells a similar product for a best-selling Japanese camera and turns out a vast line of CMOS chips for consumer goods made throughout the world.

Crowley says that the In-Stat meeting was the first time—though it probably won't be the last time—he has approached the trade issues systematically. "U. S. company guys don't understand how all this confusion troubles the big customers," he says. "Some of the biggest tell me they just want it to be settled so they can plan."

"He's a very articulate spokesman for that view," agrees Welty, "and it was a well-done speech, but the logic doesn't track." The truth, says the semiconductor pioneer, is that dumping actions "show the present laws do work if they're enforced." The industry will continue to seek their protection, despite what appears to be a Japanese smokescreen, vows Procassini. *–Larry Waller*

*SEMICUSTOM ICs*

# HIKING THE ACTIVE AREAS IN DENSE SEMICUSTOM ICs

**ROCHESTER, N. Y.**

The number of gates that can be put on a gate-array or standard-cell chip has been increasing rapidly to between 40,000 and 50,000, about two to four times the density of top-of-the-line arrays only a year ago. Unfortunately, however, as gate densities have risen, engineers' ability to use a high percentage of the gates on a chip in practical designs has fallen away precipitously.

Gate utilization can be as high as 70% to 80% for small arrays. But in very large-scale integration, gate utilization plummets to as little as 20% to 30%. Continuing investigation into ways to combat this problem was a major emphasis of this year's Custom Integrated Circuits Conference held in Rochester last week.

As ICs grow larger, more and more real estate must be devoted to interconnection wiring at the expense of area used for active gates. This problem is not limited to semicustom chips; interconnection also takes up a huge percentage of the area of full-custom VLSI devices.

But the problem is exaggerated for gate arrays and standard-cell chips. The highly complex designs that the largest of these semicustom chips are used for demand the use of ever-larger macrocells, or predefined circuit blocks. As the large cells are interspersed with smaller ones, longer interconnection paths are required to route signals around them.

*The solution is schemes that cut the wiring area*

Furthermore, the circuit complexity demands the use of automatic layout and routing tools: it takes far too long to design such chips by hand. As good as modern placement-and-routing tools are, they must by nature use conservative design rules—they cannot afford to take the kinds of shortcuts a clever designer can improvise.

At the conference, proposed ways to boost gate utilization ranged from more efficient automatic placement-and-routing schemes to alternative methods of layout and logic implementation.

**THE HIGHER THE BETTER.** In the first category is a channelless gate-array technique from Hughes Aircraft Co.'s Semiconductor Division in Newport Beach, Calif., that can boost gate utilization to about 50%. Oddly enough, the technique actually improves gate utilization as densities go up.

Implemented in a family of 2-$\mu$m double-level-metal CMOS gate arrays ranging in density from 1,000 to 41,000 gates, the channelless architecture from the General Motors Corp. subsidiary is a "sea-of-gates" structure [*Electronics*, July 22, 1985, p. 40]. It consists of an array of identical eight-transistor basic cells containing the equivalent of a pair of two-input gates replicated in the horizontal and vertical directions.

Basic cells are combined to form active-cell rows with alternating channel areas, each with room for one to seven interconnection tracks. The symmetrical design of the cell minimizes the number of wasted tracks because active-cell rows can be selected using half the basic cell height.

Connections to macrocells formed from the basic cells are made by using either the first layer of metal running horizontally in the channel area or via the second layer running vertically over the cells. Using standard gate-array layout systems, gate utilization with this technique ranges from 35% to 43% on 19,000-gate arrays to as high as 50% on a 41,000-gate array.

Addressing the same problem in standard-cell designs, engineers at Daisy Systems Corp., Mountain View, Calif., have found a way to decrease the area occupied by channels by as much as 20% through the use of a gridless channel-routing and compaction scheme. Applicable to any cell-based IC design using blocks of arbitrary size and shape, this technique uses a number of proprietary algorithms to derive channels for an arbitrary floor plan.

The key is the use of a routing scheme in which the interconnections are compacted with reference not to a predetermined grid, but to lines on each wiring layer similar to contour lines on a map. Routing-area reductions range from 10% to 20%. Further, a customized floor plan rather than one limited to straight parallel channels reduces wasted space when an IC is designed with irregularly sized blocks, which often oc-

curs in current approaches.

Other researchers at the conference described multiple-level logic-gate schemes that reduce the need for additional interconnections as densities increase. Although the methods use more complex multiple-level gate-cell structures, they achieve higher speeds and densities and reduce wiring area.

**Stacked logic also can reduce the wiring area**

One such scheme comes from the Department of Electrical Engineering and Computer Science at the University of California at Berkeley. It uses four basic two-level logic gates: series-wired AND-AND, parallel OR-OR, AND-OR, and OR-AND pairs, configured into a multilevel matrix on a MOS chip.

Because many of the gates can be connected to the associated second level of logic in the same basic cell, interconnection to gates outside the cell is reduced as much as 50%. That can also boost speed, almost doubling it in many cases.

A multilevel differential logic scheme has also been developed for bipolar logic by designers from Ferranti Electronics Ltd., Hollinwood, England [*Electronics*, Nov. 11, 1985, p. 21]. Unlike conventional single-ended current-mode logic gates, this differential-logic gate makes use of long-tailed pairs of transistors stacked on top of each other.

Ferranti can stack up to four levels of logic using a 5-V power supply. The results, designers say, are four- to eightfold improvements in speed and half the power dissipation of conventional bipolar logic. *–Bernard Conrad Cole*

*DATA PROCESSING*

# SCANNER HANDLES TEXT, IMAGES SIMULTANEOUSLY

**SANTA CLARA, CALIF.**

Computers have made it possible to generate documents electronically in greater variety and volume than ever before. But going the other way—from paper to computer-readable form—has always been difficult. Documents must be typed laboriously or scanned by machines that are both expensive and very limited in their capabilities.

Among the first of a new generation of intelligent machines that simplify the scanning process is the Compound Document Processor unveiled last week by Palantir Corp., Santa Clara. The system is called "compound" because it scans text as optical character recognition systems do and digitizes images on the same page using techniques similar to those of facsimile machines.

There are other scanners, such as the JetReader from Datacopy Corp., Mountain View, Calif., that enter both text and images into a system. But a user must tell the system whether to deal with a given page as text only or as an image; JetReader cannot apply both OCR and image-scanning methods to the same page at the same time, in contrast to Palantir's CDP. The CDP distinguishes between text and images automatically.

Furthermore, Palantir's system recognizes alphanumerics printed in virtually any type font, without being taught the specifics of individual fonts. It digitizes images such as photos and drawings at 300 dots/in., which corresponds to the resolution of most popular laser printers. And the $39,500 system preserves the layout of a page, so that the images and text on a stored and retrieved page retain their original relationships.

Palantir sees applications for the CDP in technical publishing, forms processing, data-conversion services, and a variety of document-archiving systems. It already is a part of the Army's giant 600S contract for putting thousands of technical manuals into electronic storage, where they can be easily updated.

The CDP will be sold as a peripheral to a host computer, such as an IBM Corp. Personal Computer or a Digital Equipment Corp. VAX, or to an optical-disk system, says product manager Leonard Feldman. It supports applications for AT&T Bell Laboratories' Unix and IBM PC-DOS operating systems, and can be tied with hosts through RS-232-C, Multibus, and Ethernet links.

**BRAINS OF THE OPERATION.** The intelligence of the CDP comes from a half dozen proprietary algorithms that run on four Motorola Inc. 68000 chips, a 68008, and two gate arrays that perform character recognition and separation. The algorithms recognize alphanumerics by abstraction rather than by matching matrices or by feature extraction. In this way, a single character reference represents many type fonts. The system is also sensitive to context, so it can distinguish between similar characters, such as "1" and "l".

The CDP can be tailored for use with standard forms through a feature that allows the user to divide a document into as many as 256 zones of varying sizes. The zones can be defined as containing text, image, or a mixture.

Images are scanned at 1 bit/pixel but are stored according to one- and two-dimensional compression techniques fitting the International Telegraph & Telephone Consultative Committee standard to permit a thirtyfold saving over the original. A standard page of images, which if not compressed would require 1 megabyte of storage, can thus be packed into 35-K bytes. Decompressing on the fly, the system can restore a full-page image in about 45 s, the company says. The scanning rate for text is up to 100 characters/s. *–Clifford Barney*

## THE CD-ROM THAT MAPPED TOKYO

**A new use for** compact-disk read-only memories should add fuel to a market that's rapidly heating up [*Electronics*, March 10, 1986, p. 11]. Hitachi Ltd. and Zenrin Co., Japan's top publisher of detailed residential maps, have jointly developed an electronic map system that uses a personal computer and maps stored on a CD-ROM. They'll show the system at the 62nd Business Show May 21-24 in Tokyo.

Zenrin makes the electronic maps and stores them on CD-ROMs; Hitachi manufactures the P-MAP (for Personal Mapping) system using its B16-series 16-bit personal computer, a CD-ROM drive, a digitizer, and an optional printer and plotter. Hitachi and Zenrin first developed a detailed residential mapping system two years ago, using computer-aided design techniques. Putting the maps on CD-ROMs will make them cheaper.

The CD-ROM has a 552-megabyte capacity and can store 400 to 500 residential maps, each covering a 750-by-500-meter area, using a scale of 1/1,500. This means Tokyo's 23 ward maps can be stored on five to six CD-ROMs. The maps include geographical features such as roads, rivers, buildings, and train lines, and information such as road names and building addresses.

The system's CAD function enables users to store additional data on a 20-megabyte 5¼-in. hard disk or two 5¼-in. floppy disks that store 1.2 megabytes each. Data stored on either CD-ROMs or magnetic disks can be displayed in eight colors on a 14-in. screen. Users can select and display information according to their needs; for example, they can find out which apartment buildings are within some specified distance of a particular train station.

The map system is expected to be used by banks, insurance and real-estate companies, public utilities, delivery services, urban planners, and market analysts. Shipment begins in July; other city maps could follow. *–Mari Matsushita*

BUSINESS

# DESPITE DOUBTS, INDUSTRY BACKS SENATE TAX BILL

**WASHINGTON**

The U.S. electronics industry views the tax reform bill approved recently by the Senate Finance Committee as a significant improvement over previous tax reform proposals, primarily because it provides for lower rates for corporations and retains the industry's coveted tax credit for research and development. But industry trade groups believe the package still requires some fine-tuning in areas such as capital formation and accelerated depreciation schedules.

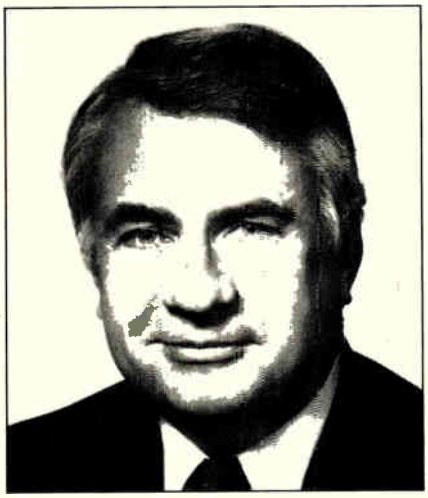
The industry is generally seeking a tax package that will improve its international competitiveness. The American Electronics Association, for example, has in the past argued that the current tax code harms the global standing of U.S. exporters of electronic products by "subjecting them to higher effective tax burdens than most sectors of the economy and a higher cost of capital than our major international competitors."

The AEA board was still debating its position on the Senate tax proposal late last week, but Ken Hagerty, vice president for government operations, labeled the bill a "real mixed bag." The AEA opposes the House tax reform package approved last fall because, it says, that version reduces incentives for innovation, capital formation and investment, and exports. For one thing, that version would reduce the R&D tax credit from 25% to 20% and extend it for only three more years.

**RESEARCH SUPPORT.** By contrast, the AEA and other industry groups praise the provisions for R&D tax credits contained in the Senate bill. These include a four-year extension of the 25% credit through 1989 and enhanced provisions for corporate-funded university basic research. The Reagan Administration has proposed a three-year extension of the 25% credit, and the industry itself favors making the credit permanent [*Electronics*, June 3, 1985, p. 13].

The Senate package, however, does not include a tax credit for startup companies, an important industry concern.

"This is a super start," says Mark V. Rosenker, a staff vice president of the Electronic Industries Association in Washington. "But it will still need some fine-tuning." The EIA is concerned that a shift of the tax burden toward corporations, along with the Senate proposal's negative effect on depreciation rates and schedules, will hinder their ability to attract capital for investment. "The short lives of high-tech products demand accelerated depreciation," argues EIA president Peter F. McCloskey.



**EIA's McCLOSKEY:** The electronics industry needs provisions for fast depreciation.

Nevertheless, Rosenker voices approval on balance for the Senate panel's plan, concluding that "the positive aspects may outweigh the negative aspects."

Ted Heydinger, vice president of the Washington-based Computer and Business Equipment Manufacturers Association, cites the reduction of business tax rates and retention of the R&D tax credits as "stimuli to the high-technology community. American high-tech companies need these tax provisions, especially the R&D credit, to remain competitive in the international marketplace."

But as well as sharing the industry's opinion about the shortcomings of the proposed tax legislation, Heydinger remains concerned about Internal Revenue Service regulations that prevent the allocation of R&D expenses to income from foreign sources. Cbema and EIA both favor a permanent moratorium on those regulations.

Electronics industry officials generally appear optimistic about the bill simply because Sen. Robert Packwood (R., Ore.), chairman of the Senate Finance Committee, was able to keep tax reform on track at a time when many observers said it would die in an election year. Heydinger emphasizes that whatever shape Cbema's final floor strategy takes, it will resist anything that harms the total tax package. "This bill just means too much to us in terms of fairness," he says. *–George Leopold*

MICROPROCESSORS

# CAN ZILOG-AT&T TEAM SCORE IN THE 32-BIT RACE?

**BOSTON**

Until last week, semiconductor-industry handicappers figured that Intel, Motorola, and National Semiconductor would distance themselves from the pack in the race for shares of the 32-bit-microprocessor market. Now the handicappers will have to go back to their charts: two companies projected to lead the remaining pack—Zilog Inc. and AT&T Technology Systems—have decided to run as a combined entry for at least one chip set.

The pairing-up was announced last week at the Institute of Electrical and Electronics Engineers' Electro/86 Show in Boston. Zilog, the Campbell, Calif., chip-making subsidiary of Exxon Corp., will second-source the WE32100 microprocessor family developed by the Berkeley Heights, N.J., telecommunications heavyweight. For an initial period of five years, the pact gives Zilog the right to market the chips under its own trade name; Zilog also has the right to develop and market new 32-bit peripherals based on AT&T technology as AT&T adds them to its catalog.

**SACK:** Zilog has 32-bit microprocessors for three key markets.

Janet Oncel, an industry analyst at Dataquest Inc., San Jose, Calif., sees the deal as good for both parties. Zilog, she says, missed the market window for its own Z80,000 32-bit chip by such a wide margin that it had to design AT&T's WE32100 chip into its work station. "They shot themselves in the foot with that move," Oncel says. And AT&T, intent on becoming a major player in the 32-bit market, needed a second source for the chip.

"AT&T will eventually be a winner in the 32-bit marketplace, but not until the 1990s," Oncel says.

Her reasoning: office automation, where AT&T Bell Laboratories' Unix operating system is increasingly popular, will drive the 32-bit microcomputer market. And though Intel Corp., which supports both Unix and Microsoft Corp.'s MS-DOS on its 80386, is a clear favorite now [*Electronics*, May 5, 1986, p. 40], AT&T has plenty of time to build a market.

The second-source deal is "another major step in Zilog's growing relationship with AT&T," says Edgar Sack, Zilog's president and chief executive officer. "In 1979, we took out a license for Unix. Then last year, our Systems Division selected the WE32100 as the engine for its 32-bit supermicrocomputer. We believe the WE32100 will be a leader in the emerging 32-bit market."

*The deal furthers Zilog's ties with AT&T*

Sack, though, is not betting all of Zilog's 32-bit chips on the WE32100. "We are a microprocessor company and want a presence in all three major markets: The AT&T family gets us into the Unix market. For MS-DOS, we have [NEC Corp.'s] V series. For military systems, we have the Z80,000," he says. After a year of teething troubles, Zilog began shipping Z80,000 samples in January and expects to have it in production in the last quarter. For MS-DOS applications, Sack is high on NEC's V60 and V70 chips [*Electronics*, May 12, 1986, p. 41]. The large cache memory of the V-70 could make it a winner, he believes.

AT&T, predictably, is concentrating on Unix with the WE32100 and a planned "third-generation" 1-μm, 20-MHz family, the WE32200. AT&T won't discuss sales, but Bill Dugan, a vice president at the Components and Electronic Systems Division, says the company's fabrication plants in Allentown, Pa., and Orlando, Fla., have the capacity to handle 6,000 wafer starts a week. Dugan says AT&T expects to add another second source for the family in the U.S. and one overseas. *–Arthur L. Erikson*

**SUPERCOMPUTERS**

# WEST GERMANS SHOOT FOR WORLD SPEED RECORD

**KARLSRUHE, WEST GERMANY**

By early next year, a small, 14-month-old company in this southwest German town plans to bid for top honors in price/performance ratio among international supercomputer makers. That's when Integrated Parallel Systems plans to unveil its TX2 family, based on an extended binary-tree structure that allows processing of many functions in parallel. The top-of-the-line model will boast an average processing speed of 4 billion instructions per second and a price between $3 million and $4 million.

Wolfgang Wöst, president of iP-Systems, an engineering spin-off of the prestigious Technical University of Karlsruhe, says the 4-bips average envisioned for the family's top parallel machine will compare with the peak speed of about 1 bips for the fastest supercomputers developed thus far [*Electronics*, May 5, 1986, p. 16]. Going up against such well-established giants as Control Data, Cray, and Floating Point Systems in the U.S., as well as Fujitsu in Japan, the company says the top TX2 model will sell for roughly one third the price of the competition's fastest machine. Peak speed of the TX2, iP-Systems says, will be as high as 7.2 bips.

Though the company doesn't even have a prototype yet, it says use of commercially available processors will make it possible to go to market early next year. The top TX2 model will have 4,096 modules, each of which will have its own 16-bit, 10-MHz microprocessor as well as a 256-K dynamic random-access memory.

IP-Systems says the limits of the system extend way beyond the 4,096 modules, however, and tens of thousands of processor/memory modules could be tied together. The TX2 will support floating-point operations. In addition, the supercomputer will use 1-Mb DRAMs when they become available.

Wöst, 35, came up with the idea for this supercomputer in the early 1980s while he was working as a researcher at Karlsruhe University. In March of last year, with the help of venture capital and government money, Wöst founded iP-Systems to implement his idea.

**NO BOTTLENECKS.** "A unified concept that adapts hardware, software, architecture, and application to one another" is the key to the new machine, says Wöst. The extended binary-tree structure—for proprietary reasons, Wöst will not reveal the nature of the extensions—ensures that bottlenecks in processing cannot occur.

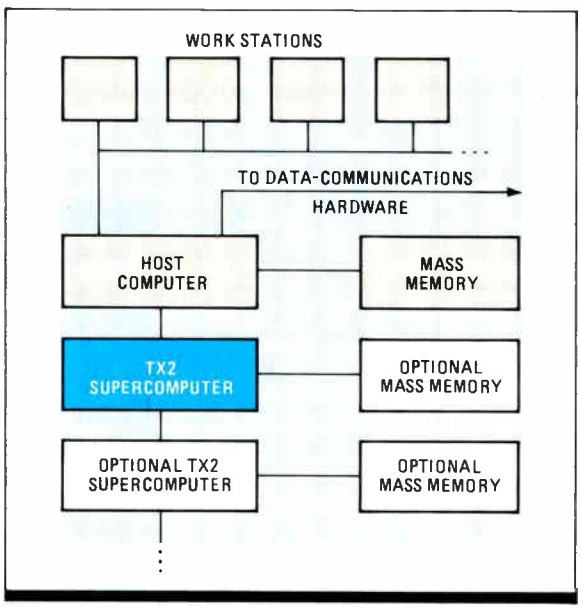
Instead of a common bus and common memory, on which most traditional computers rely, the TX2 has many buses and one memory for each processor. Thus simultaneous communication among many processors is possible, and delays in accessing a common memory are eliminated.

The TX2 also eliminates delays caused by a processor waiting for a global scheduler's decision. During compilation, the programmer determines which processor is to perform which task.

From an early stage of development, iP-Systems has been paying as much attention to software as it has to hardware. "Normal software will not do for a parallel high-performance system," Wöst says.

To tap the machine's full power, the user, supported by compilers and heuristic models, will convert existing programs to parallel format and feed them to the system, or use the parallel extensions of the high-level computer languages Pascal, C, Modula-2, or Fortran. If the user wants fast compilation of existing programs, a precompiler can be used for automatic conversion to parallel format. With Prolog, no paralleling is needed since this extended language already has a high degree of parallelism.

The company also claims the TX2 family will be easily expandable. It will be possible to link two or more machines to form a faster, more powerful system. For example, several of the family's smallest machines—each carrying 16 processor/memory modules and set to sell for around $27,000—can be built up into the equivalent of the top model, increasing processing power more than 250 times. Conversely, a simple software




**EXPANDABLE.** Users will be able to join additional TX2 units, mass memories, and printers to a TX2 supercomputer.

instruction can split a large machine into several smaller units.

The machine will also be programmable to work as a fault-tolerant system. In normal operation, it will recognize a fault. For fault-tolerant operation, an instruction selects the desired degree of fault tolerance. No change in hardware or software is necessary, but system speed may be somewhat reduced.

The TX2 will operate together with a number of host computers (diagram). These can range from a personal computer to a mainframe and will allow the TX2 to communicate with other computers or with work stations. The interface with the host computers is universal and adapted to the host's operating system. Optional mass-storage devices and printers will operate through the host or the TX2.

As an entry-level system, the smaller TX2 version will enable users to move into the supercomputer class at low cost. Because the TX2 is not a family of specialized computers but of general-purpose machines, there are plenty of applications for which it can be used besides mere number crunching.

First applications, Wöst says, will probably be at research establishments, performing such tasks as complex simulations involving hundreds of partial differential equations—those needed, for example, in determining what can go wrong with nuclear power plants and in predicting the weather. Other potentials exist in aircraft design, engine construction, and expert systems.

Besides allowing hookup of tens of thousands of processors without modification to the basic design, the TX2 series promises to accommodate the ultradense, high-speed devices of future circuit technologies. *–John Gosch*

*MILITARY*

# UNCOOLED IR SENSORS SHRINK SCOPES

**WASHINGTON**

Uncooled infrared-sensor technology is about to move from the laboratory to the firing range. Two Pentagon contractors—Texas Instruments Inc. and Honeywell Inc.—have been working on a rifle scope that will use uncooled IR technology to reduce bulk and weight, and prototypes are expected to be delivered to the Army by August. The scope is being developed as a part of the Short-Range Thermal Sight Program at the Army's Night Vision Electro Optical Center at Fort Belvoir, Va.

The main advantage of the new technology is reduced size. Conventional IR sensors must be cryogenically cooled for high performance, and the cooling systems add significantly to size and mass.

Researchers acknowledge that today's uncooled IR sensors lack the resolution and sensitivity to temperature differences of current cooled IR imaging technology. But such sensors, made with lithium tantalate and other proprietary materials, can still complement cooled IR sensors as uncooled performance increases over the next several years, say project engineers.

**SMALL BUT HUNGRY.** With cooling eliminated, researchers have reduced the scope's size to fit in the 14-by-3½-by-3½-in. package specified by the Army. (Allowing for larger optics, however, would offset some of the uncooled sensors' lower resolution, researchers say.) Weight is also down, and power consumption ranges from 4 to 6 W—much higher than for image-intensifying sensors, which work in the milliwatt range, but much less than for conventional cooled sensors, which operate at 77 K.

TI and Honeywell will each deliver three scopes meeting the same weight, size, and performance specifications, but the six designs will all differ slightly from each other. Magnavox Government & Industrial Electronics Co. will also deliver three scopes that use conventional thermoelectrically cooled lead selenide technology; their weight and power consumption are expected to be comparable to the uncooled designs.

Depending on engineering development and Pentagon budget constraints, full-scale production of scopes for the M-16A2 rifle could begin in the early 1990s. Meanwhile, other uses are being investigated. Short-range applications for uncooled IR sensors include missile-targeting systems, autonomous munitions sensors, and helmet-mounted sensors that would allow firefighters to see victims and hot spots through smoke.

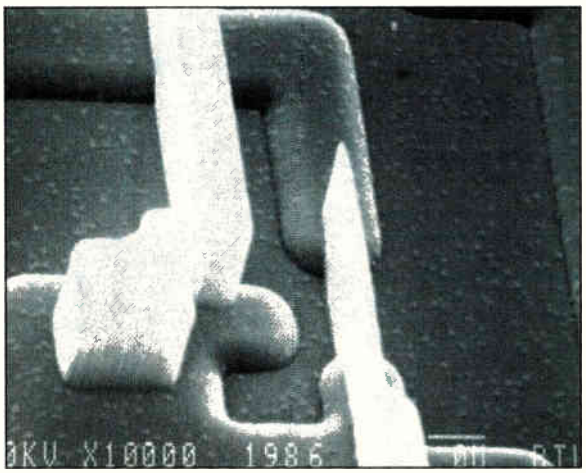
The Army will select two scope designs for engineering development by the end of 1987, with procurement to follow in the early 1990s. After they are delivered, the scopes will undergo sensitivity and resolution tests in the lab before field testing at Fort Benning, Ga. If engineering development is successful, the Army could eventually order about 63,000 scopes for between $6,000 and $7,000 each. *–George Leopold*

*IC PRODUCTION*

# DEEP-UV STEPPER PRINTS 0.25-MICRON STRUCTURES

**MURRAY HILL, N. J.**

Just when the rest of the chip-making community is earnestly delving into the minute world of 1-μm geometries, AT&T Co.'s Bell Laboratories is keeping its eyes set firmly on the future by seeking ways to break the 0.5-μm barrier. Bell Labs researchers have designed an optical lithography system that can print most features as small as 0.4 μm—and isolated features as small as 0.25 μm. Built around a commercial wafer stepper from GCA Corp., Bedford, Mass., the system is called the deep ultraviolet stepper because it uses short-wavelength light.

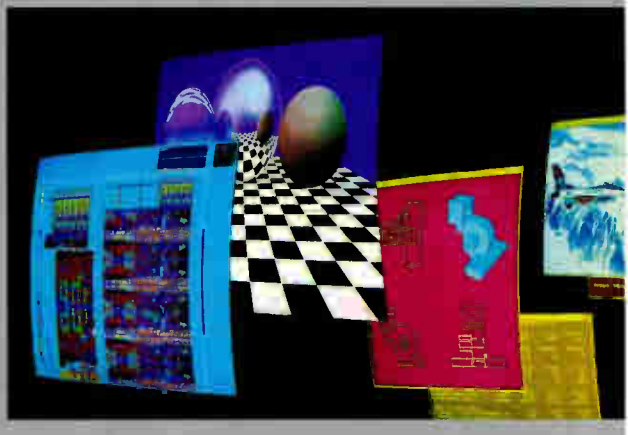



**THE POINT.** Bell Labs' deep ultraviolet stepper was used to fabricate the 0.25-μm gate in an n-MOS ring oscillator.

Using a laser-based projection system that reduces the features masked on a reticle by a factor of five, the system projects a circular field with a diameter of 14.5 mm, allowing for the projection of a chip 1 $cm^2$ in size. The system can consistently define 0.5-μm lines and spaces, and 0.35-μm lines and spaces have been achieved as well, according to Victor Pol, a researcher with the Lithographic Systems Development group in Murray Hill.

The beauty of the new

# Digital has it now.



Now there's a UNIX™ workstation that lets each graphics window tap the power of the network. Digital's VAXstation II/GPX,™ with its innovative X Window System, offers multiple, transparent windowing to any ULTRIX™ or UNIX (4.2 Berkeley) computer, anywhere on your network.

A different application can run in each window, or within an application, individual windows can be linked to a larger computer. You can also access VAX/VMS™ systems via DECnet-ULTRIX™ networking software, or other vendors' systems via the SNA gateway, X.25 or TCP/IP protocols. And with larger systems handling compute-intensive tasks, the built-in MicroVAX II™ CPU and GPX

# VAXstation II/GPX: The first UNIX workstation to put the power of a mainframe in every window.

graphics coprocessor can concentrate on what they do best: delivering exceptional graphics at tremendous speeds.

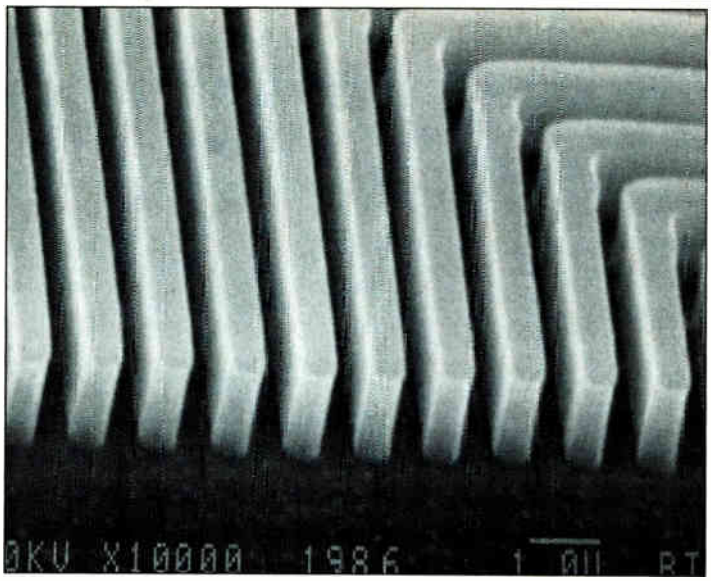
VAXstation II/GPX lets you utilize your existing UNIX applications through ULTRIX, Digital's UNIX operating system. ULTRIX is a true Berkeley 4.2 BSD implementation and compatible with AT&T's System V.™

VAXstation II/GPX. Everything an engineer wants in a workstation, backed by all the service and support he needs. For a brochure, write to: Digital Equipment Corporation, 200 Baker Ave., West Concord, MA 01742. Or call your local sales office.

digital™

system is as much a matter of the way it was produced as it is of its ability to print such fine geometries, Pol says. That's because the group didn't start from scratch in its development effort, but it chose instead to adapt a commercially available step-and-repeat system in order to make it easier to move the technology from the laboratory to the foundry.

Starting with GCA's model 4800 wafer stepper, Pol and his colleagues completely redeveloped the optical reduction system. The new projection system uses a pulsed krypton fluoride excimer laser fitted with optics that narrow its bandwidth from about 1 to only 0.005 nm.



**CONSISTENT.** The DUV stepper demonstrates a crucial characteristic—consistency over a chip's area—with a pattern of 0.5-$\mu$m lines and spaces.

The use of a commercial system modified to a large degree with commercially available parts makes the stepper more than a research marvel incompatible with real-world applications, says Pol. "We built it on the fundamental premise that with some modifications it could be used in the manufacturing environment," says James Clemens, head of the Lithographic Technology Department.

"What we have is a practical system that can routinely print lines and spaces over a large chip," Pol adds. "We built a tool we can use."

**SHORT WAVES.** Building such a tool meant developing a method to achieve the high resolution that such fine lines require. In these systems, Pol says, resolution is affected by two factors: the wavelength of the light source and the aperture of the projection lens. The choice was simple, he says: he decided to cut down the wavelength of the light source because widening the lens aperture would have sacrificed depth of focus, which in turn would have adversely affected the resolution.

A very intense laser with a wavelength of 248.4 nm—a little more than half the 436-nm wavelengths used in many current steppers—was chosen, and special etalons—mirrored filters that narrow the laser's bandwidth—were constructed and mounted inside the laser cavity for optimum efficiency. But with such a short wavelength, another difficulty arose: most optical materials will not transmit light so far up the spectrum. So the group had to incorporate a lens of pure fused silica, or quartz.

Pol says the smallest feature the DUV stepper has yet printed is a 0.25-$\mu$m gate on an n-MOS ring oscillator (photo, p. 21). The gate was defined by the stepper in a 5,000-Å layer of Microposit 2400-17 resist atop a 1,200-Å layer of silicon dioxide and a 1.8-$\mu$m layer of HPR-206 resist used to planarize the wafer surface. Etching then removes material from all three layers.

But the ability to define a small isolated feature is overshadowed by a stepper's ability to consistently define such small geometries across a chip's surface, Pol says. He says his machine has demonstrated that ability in a test pattern etched into the same material, in which 0.5-$\mu$m lines are evenly spaced 0.5 $\mu$m apart (photo).

Clemens says his group is now working with other Bell Labs chip-design groups. Both silicon and gallium arsenide design labs are now working to produce fine-line-geometry designs that can make use of the new technology and be used in further refining the system.

AT&T is actively discussing the technology with outside vendors, and the company may eventually license it for use in commercial products, according to Clemens. But long before the technology becomes commercially available—at least five years from now, Clemens says—AT&T will be producing chips with it. *–Tobias Naegele*

***ARTIFICIAL INTELLIGENCE***

# AI FINE-TUNES SPEECH RECOGNITION

**TURIN, ITALY**

Ing. C. Olivetti & Co. is counting on artificial intelligence to boost performance of its future speech-recognition systems. Researchers at the voice-processing laboratory of Italy's foremost producer of office-automation and data-processing systems are integrating an expert system into the company's prototype speech-recognition system.

In essence, the expert-system program applies data about language—including grammar, semantics, and linguistics—to eliminate recognition errors by the system's signal-processing scheme. First estimates show that the expert system eliminates more than half of those errors.

The company hopes, in several years, to have a large dictionary system that operates on a bottom-of-the-line piece of equipment such as an electronic typewriter, says Vittore Vitorelli, manager of the Olivetti central research department's voice-processing laboratory. Vitorelli refuses to comment on current hardware development. But the recognition system now under development is hardware-independent and boasts a vocabulary of up to 5,000 words, with recognition success rates that approach 100%, he says.

**OPEN DICTIONARY.** IBM has recently announced a research speech-recognition system with a vocabulary of 20,000 words [*Electronics*, March 24, 1986, p. 13]. But Vitorelli points out that, unlike IBM, "we have avoided using a predefined dictionary."

This, he claims, makes the Olivetti system far more flexible, because its vocabulary is made up of words arranged in classes. A fixed-vocabulary system requires entry of complex statistical data and default values for each new word; with the Olivetti system, a word is simply entered into the appropriate classes.

Dividing words into classes also shortens the time it takes to train the system to a user's voice. Olivetti's system requires no more than five minutes of training; IBM's reportedly needs four times that, in addition to an external data-processing step required to ready it for operation.

Interestingly, Vitorelli also argues that because the most common words in any language are usually the easiest to mistake in speech recognition, sheer vocabulary size is not necessarily an indi-

cation of how advanced a system is. Uncommon words are usually longer than common ones and thus provide more elements that help identify them. Vitorelli reckons that a vocabulary of about 10,000 words is adequate for most European languages if the recognition system is flexible enough to permit the easy addition of necessary words.

The Olivetti system is based on the phoneme—which is the smallest distinguishable unit of speech—and utilizes a linear predictive-coding signal-processing scheme. When an operator speaks into a microphone, the energy level of the person's voice is sampled at 16,000 12-bit samples/s. Using the training-session data as a reference, the system then breaks the signal down into a probable string of phonemes.

That string is then compared with the phoneme strings in the system's vocabulary, and the impossible matches eliminated. At this point, the system will consider up to either 1% or 3% of the total vocabulary, the choice being made by a software switch. The former is faster, the latter more accurate.

The chosen list of words is then refined to a short list using phonetic fine-tuning, until only one to five words remain. If necessary, the expert system then chooses, using such criteria as whether a sentence under consideration is grammatically legal or whether the use of a given word is probable in the context under consideration. Using the 3% option, the system chooses the correct word as much as 99% of the time.

Development is being done on a Digital Equipment Corp. VAX 11/750 computer with a response time of about 15 seconds. Real-time operation is an eventual goal. *–Robert T. Gallagher*

***INSTRUMENTATION***

# PC-IN-A-BOX GIVES MAC A PUSH INTO ENGINEERING

**AUSTIN, TEXAS**

Apple Computer Inc. is getting a little help in its attempt to loosen IBM Corp.'s grip on personal computers in the engineering workplace. A new plug-in box from National Instruments Corp. lets the Macintosh Plus support the myriad third-party add-on cards that turn IBM Personal Computers and compatible machines into low-cost engineering tools.

The plug-in MacBus box is, in essence, half of an IBM PC AT, and it combines the best of both microcomputer worlds, says James J. Truchard, president of the Austin-based manufacturer of IEEE-488 interface products. The box and Macintosh Plus plug together with a Small Computer System Interface. The Macintosh gives engineers an icon-based user interface, while the MacBus opens up the use of AT-compatible boards within the Mac's closed architecture. The box also gives the Macintosh an intelligent, real-time interface to the IEEE-488 parallel instrumentation bus, a widely used interface for laboratory equipment.

"What we are providing is an add-on data-acquisition box to the closed architecture of the Macintosh," notes Don Nadon, vice president of sales. "We have seen a lot of engineers getting hooked on the graphical interface of engineering work stations, which is similar to the Macintosh. Now, we believe engineers are seeking ways to use the Macintosh in their work." As many as 40,000 technical users could become Apple customers, he speculates.

Apple, which has worked with National Instruments on the SCSI interface, is also attempting to bolster the use of its Macintosh in engineering applications. In March, the Cupertino, Calif., company launched a still unnamed strategic business organization to get the Macintosh into computer-aided design, laboratory automation, test controls, and data acquisition. The technical-market thrust is part of Apple's recently announced move to open up the architecture of the Macintosh with Microsoft's MS-DOS, the operating system used by the IBM PC, and AT&T's Unix [*Electronics*, May 12, 1986, p. 24].

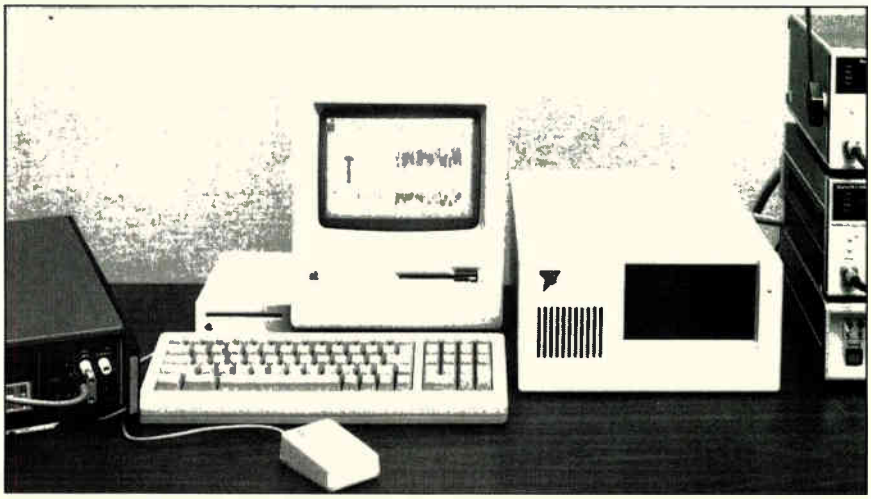
**IN THE BOX.** Inside the MacBus box is a central-processing-unit card containing a NEC V50 16-bit microprocessor and circuitry to generate a subset of a PC AT-compatible 16-bit bus. The GPIB-V50 processor card also contains an instrument-bus control language, which acts as a real-time operating system and provides control of the 488 bus.

The operating system has the intelligence to provide real-time responses. The system can accept data from the parallel 488 bus, buffer it, perform front-end processing, and even send back commands without having to interrupt the host Macintosh. The MacBus can also execute complex stored commands written in Forth from its own CPU memory after they are initiated by the Macintosh. After the commands are initiated, the V50-based MacBus executes the programs, freeing the Macintosh for the user.

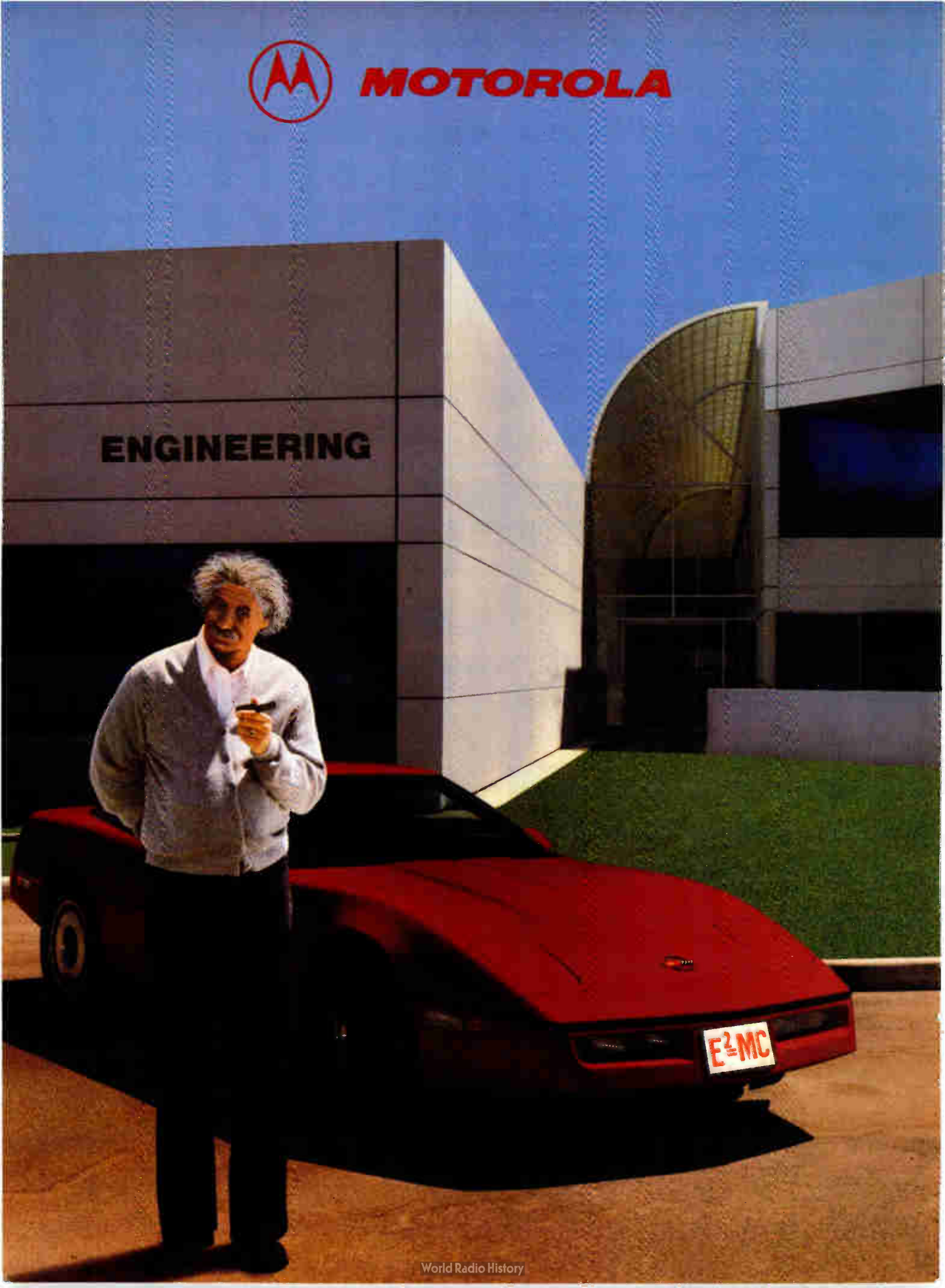
An SCSI card occupies one of the MacBus slots, feeding data to and from the Macintosh Plus. Three expansion slots are available for PC AT-compatible plug-in cards. The MacBus costs $1,495 and standard software for the Macintosh is another $200. The two enable users to program the interface box in C or Basic. A second $1,995 software package, LabView, controls the MacBus box and attached instruments with a unique icon-based graphical programming language [*Electronics*, May 12, 1986, p. 63]. Both LabView and MacBus debuted at last week's Electro show in Boston.

"The Macintosh tends to use up its computer power with the user interface and graphics capability," according to Truchard. "This box provides another operating environment, and LabView goes one step further in that it is a parallel-programming language, enabling the execution of programs on multiple processors."

Separating the user interface from the MacBus CPU also lets the unit apply the full strength of its V50 microprocessor and optional floating-point coprocessor to the applications. The result is three to five times the speed of a PC AT, adds Truchard. *–J. Robert Lineback*



**HALF AND HALF.** Truchard says the plug-in MacBus box is, in essence, half of an IBM PC AT.



# $E^2$=MC. Win a new Corvette.

## Creativity with on-chip $E^2$PROM is the key to Motorola's new MC68HC11 design contest.*

You don't have to be an internationally venerated genius to win a new Corvette or one of four runner-up cash prizes in Motorola's 1986 MC68HC11 design contest.

Every designer who enters could win. The key is creativity in using the host of MC68HC11 on-chip features, with emphasis on the $E^2$PROM. Once you've given it this much thought, you'll realize on-chip $E^2$PROM is more of a necessity than a luxury when designing innovative products for the demanding markets of the immediate future.

### Everyone wins.

And, every designer who buys the Contest EVB will win. An assembled and tested M68HC11 Evaluation Board to work with is yours at the provocative special price of just $68.11, a resounding $100.00 off the regular price, as long as the contest supply lasts or up to the 7-31-86 cutoff date.

It gets even better. If you submit a bona fide contest entry, your $68.11 for the EVB will be rebated. Even if you don't win the Corvette, you're already way ahead with a free M68HC11 Evaluation Board, and you might still win one of the cash prizes for second through fifth place.

### Here's how the contest works.

Use this coupon or get one from your Motorola sales representative or local authorized distributor. Contest M68HC11EVBs are available only from participating distributors, so present your filled-in coupon at one of their locations and make the special $68.11 purchase that qualifies you.

Use the EVB and other contest materials to develop and debug the design of your choice. Complete and submit the design to Motorola by 11-15-86. Working prototype and all necessary documentation are required. We'll rebate the $68.11 for the contest EVB when your qualified entry is received at Motorola $E^2$=MC Design Contest, 6501 William Cannon Drive West, Austin, TX 78735.

Judging criteria include innovativeness of on-chip $E^2$PROM use, demonstrable benefit of HCMOS and application of on-chip peripherals—A/D, Asynchronous and Synchronous Serial Systems, Pulse Accumulator, Main Timer, Parallel I/O, STOP and WAIT modes, Watchdog Timer, and Variable Priority Interrupts. Judges decisions are final.

Winners will be announced and notified by 12-31-86. Design contest entries will be returned.

To purchase your Contest EVB and become eligible for the Motorola $E^2$=MC design contest, present the coupon to your participating Motorola distributor. If the coupon is gone, your Motorola sales representative or distributor can provide one.

### Participating Motorola distributors.

You probably already have a preferred distributor for Motorola semiconductors, but if you're not sure which distributors in your area are participating, call us toll free any weekday between 8:00 a.m. and 4:30 p.m., MST, from anywhere in the U.S. or Canada at 1-800-521-6274. Tell us where you are and we'll give you the names of the participating distributors in your area.

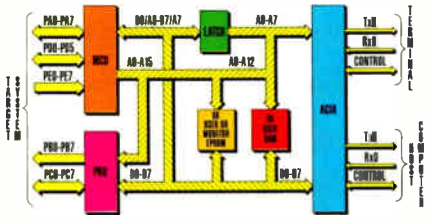
### MCU training is available.

We don't offer special training just for the contest, but any designer can sign up for one of Motorola Technical Training's acclaimed MCU courses. They're scheduled regularly throughout the year.

We're on your design-in team.

MOTOROLA

### Your $E^2$=MC Contest EVB.




- Economical means to debug user-assembled code and evaluate target systems incorporating the MC68HC11 MCU.
- One-line Assembler/Disassembler.
- Host computer downloading capability.
- RS-232C compatible terminal/host computer I/O ports.
- MC68HC24 Port-Replacement Unit-based MCU I/O expansion circuitry.
- MC68HC11 Programming Reference.
- Complete documentation and entry materials.

*Design contest valid in U.S. and Canada only. Not open to Motorola SPS Employees or their immediate families.

## Motorola $E^2$=MC Design Contest

Good for $100.00 off the list price of the MC68HC11 Evaluation Board for a net price of $68.11 plus tax for my Contest EVB when presented at my participating Motorola distributor while supplies last or no later than 7-31-86, whichever comes first.

**I am:**

Name_____ Phone (____)____-____

Company/Division_____

Address_____ Mail Stop_____

City_____ State_____ Zip_____

**My first sales contact is:**

Name_____ SS#_____

**Distributor, please fill this in:**

Distributor_____ Location_____

Invoice #_____

Contest EVB #_____

**Quantity Limited. Act Quickly. Only first 2,000 orders will be honored.**

# INSIDE TECHNOLOGY

# SPECIAL REPORT: THE OPTIONS MULTIPLY IN MASS STORAGE

## THEY'RE COMING FROM IMPROVING OPTICAL AND BUBBLE TECHNOLOGIES

*Digital data-recording technology has come a long way from where it began with bulky magnetic drums. Mass-storage devices for computers now range across three technologies—magnetic disk drives, optics, and bubble memories. Magnetic recording on disks still dominates, despite periodic assaults by other technologies. But increases in bit density are becoming harder to wring out of the basic technology. By contrast, optical devices are breaking away from their limited read-only uses as media and finally are being developed for erasing and rewriting optical data. Though the bubble memory never made it to the big time commodity markets, it is plugging along in niche markets, and a new, extremely dense storage technology may soon emerge from the basic bubble to challenge the disk drive. Leading companies as well as startups and university researchers are pushing hard on the technology in each area. So it looks like the spiral of ever-larger bit densities will go on, even if no one can yet say if optical or bubble-based technology will knock magnetic disk drives off their perch.*

*MAGNETIC STORAGE*

### TECHNICAL ADVANCES GET HARDER TO COME BY

It's getting harder and harder to keep coming up with the technical advances that will continue pushing bit density higher in magnetic recording on disks. Today's disk drives already are crowding the physical limits of recording and reading small magnetic domains, and any future gains will have to depend heavily on increasingly intractable technology.

For example, the highly touted technique of perpendicular recording, which bounded onto the scene with great promise four years ago, has so far failed to deliver any significant products. Thin-film heads, which appeared in the early 1980s, have yet to be available in volume in the merchant market. Yet another example of the leveling off of magnetic technology advances is thin-film media: many manufacturers are still struggling to produce them reliably, economically, and in quantity.

Still, many researchers think the problems are solvable and that disk drives stand a good chance of warding off the challenges from optical and bubble storage. The ongoing quest is for higher areal densities—the measure of bits per square inch. This quest has taken three forms. First, researchers are considering alternative recording schemes—different ways of orienting magnetic domains, thereby reducing their length and increasing areal density. Researchers are also exploring recording-head technologies, with the goal of constructing heads that will write to smaller magnetic domains. And finally, advanced recording media are being developed.

It has been an uphill fight for U. S. manufacturers working on perpendicular recording. "The market for perpendicular recording developed more slowly then we thought," says Robert Potter, president of Lanx Corp., San Jose, Calif.

In traditional longitudinal recorded media, the poles of adjacent magnetic domains are oriented in the plane of the recording surface in such a way that the domains tend to demagnetize one another. In perpendicular recording, adjacent vertical domains are in polar opposition, so the fields tend to reinforce one another. Cell boundaries of perpendicular recording media are sharply defined, so they can be packed more closely together than longitudinal recorded media.

Part of the reason for the slow acceptance of perpendicular is that its benefits do not justify its cost. Some say that the performance promise of perpendicular has been overhyped. "I don't see much difference between longitudinal and perpendicular recording at high densities," says John C. Mallinson, director of the University of California, San Diego's Center for Magnetic Recording Research.

Potter and Lanx began chasing a market for 8-in. perpendicularly recorded media in 1981; in 1983, he switched his focus to the newly hot 5¼-in. market. Using miniature composite heads, he produced vertically recorded media with 20,000 flux changes/in. at 1,000 tracks/in.

Samples of the 5¼-in. disks were shipped, and licenses were sold to Control Data Corp. and National Micronetics Inc. But controller technology was lagging well behind the 10-Mb/s transfer rate needed to fully utilize the technology, and when National Micronetics abandoned the disk business in 1985, Lanx lost its second source. Potter then reoriented his operation and began producing longitudinal 8-in. media, though the company still has an active research interest in perpendicular recording.

"Overall, we see less interest in the U. S. in perpendicular recording," says Richard E. Lavine, marketing manager of vacuum systems at Varian Associates Inc., a Palo Alto manufacturer of vacuum sputtering chambers. "After a flurry of activity two years ago, not much is happening here. And the Japanese seem to be doing less, too. I think the research efforts may be going into magneto-optic."

One way to bump up the areal density is to improve head performance so that the head writes the maximum number of tracks per inch on the medium. In a conventional ring head, this means reducing the width of the head to reduce the fringing field—the active magnetic region that writes a series of flux reversals onto the active layer of the medium. But because the fringing field falls off 50% at a distance comparable with the gap length between the poles of the head, both the thickness of the medium and the head's flying height above the medium must be reduced proportionally.

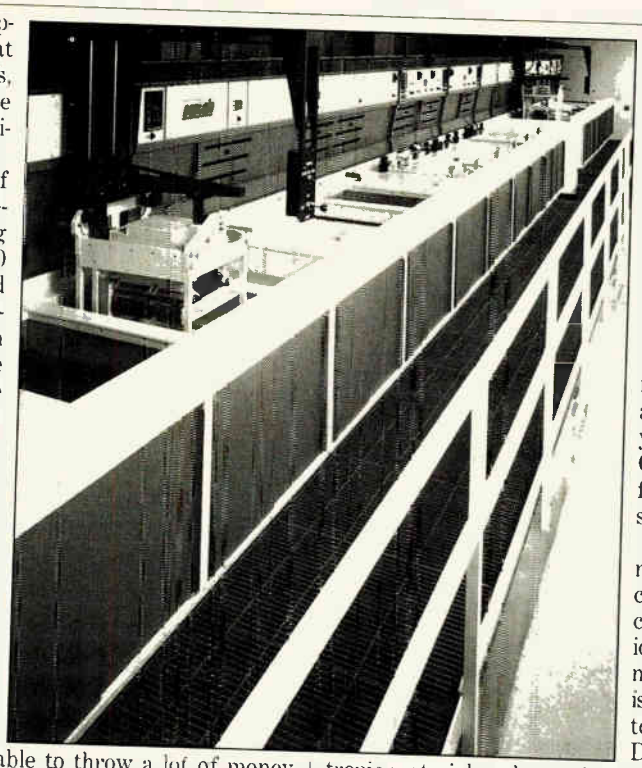
Recording-head technology took its first big leap when the 40- to 45-μin. flying height of the full-sized monolithic head was decreased to 10 to 20 μin., thanks to the introduction of the lower-mass minimonolithic heads and the improved Whitney-type suspension. The lighter minimonolithic heads improved

access times but kept the upward bound of readability at 1,000 tracks/in. Composite heads, which bond a small ferrite core to a ceramic slider, made it possible to get 1,500 tracks/in.

Thin-film heads—the state of the art in head technology because of their smaller fringing field—can write upward of 2,000 tracks/in. They are fabricated using vapor-deposition techniques akin to those used in semiconductor processing. The careful control afforded by the manufacturing process yields finer core geometries, without the constraints imposed by mechanical machining, winding, and assembly of the head that other heads require.

Thin-film heads were first introduced in 1979 by IBM Corp. on its 3370 drive, but they still are not available in volume in the merchant market. The only companies successful with thin-film heads are those large computer companies that have been able to throw a lot of money at the problems. And it even took them quite awhile to perfect their manufacturing techniques to achieve economical yields.

"The only really high-volume manufacturers of thin-film heads are the captives," says Donald C. Collier, director of market analysis for Applied Magnetics Corp., Goleta, Calif., a maker of monolithic, minimonolithic, and composite heads for the disk-drive industry. He estimates that in 1985, thin-film heads accounted for only 17% of worldwide shipments, but almost all were produced for captive consumption by the likes of Control Data, Digital Equipment, Fujitsu, Hitachi, IBM, NEC, Siemens, and StorageTek. Composite heads made up a bare 5% of total worldwide consumption; monolithic and minimonolithic constitute the bulk of shipments.



**1. PROBLEM SOLVER.** Domain Technology, an early leader in sputtering thin metallic films, switched to plating to maintain consistent yields.

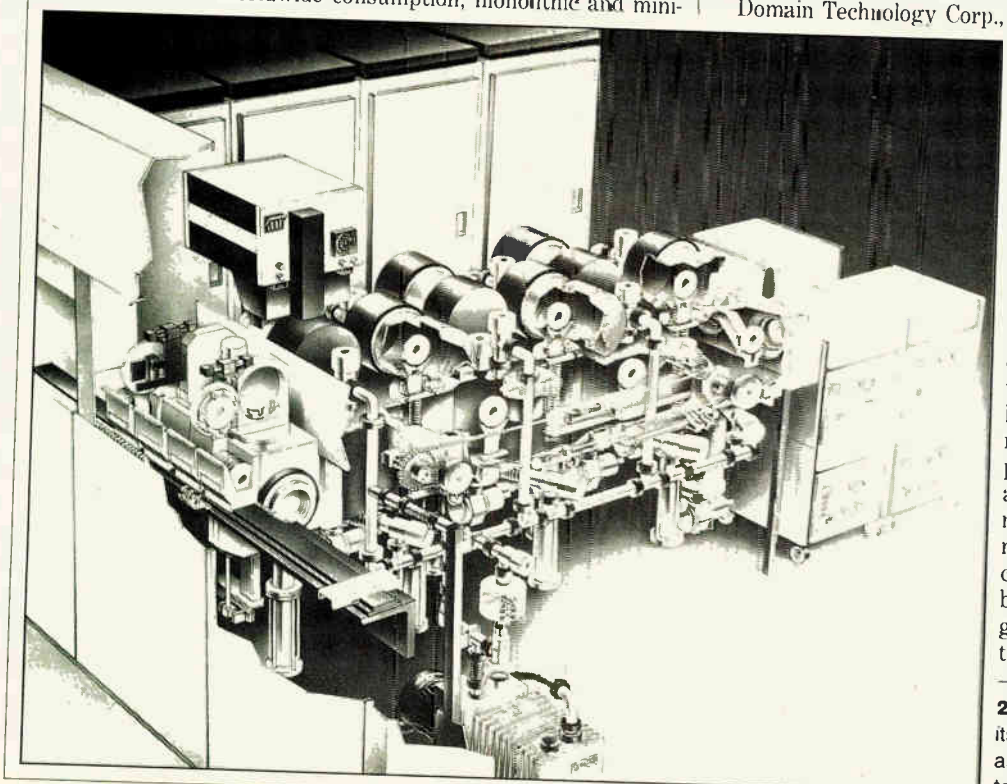
If thin-film-head recording technology has been slow to proliferate beyond the walls of the major systems houses, the opposite is true of thin-film media. Dozens of independent companies were trying to use thin film as a recording medium two years ago [*Electronics Week*, Oct. 29, 1984, p. 55], but to date few have made an unqualified success of it.

The motive to reduce the thickness of the recording medium is compelling. If the thickness of a conventional medium—ferric oxide dispersed in a binder that makes it adhere to a substrate—is reduced too much, the signal-to-noise ratio drops unacceptably. Doping oxides with highly anisotropic material such as cobalt to increase coercivity only partially solves the problem because it must be laid down in a thick layer (35 μin.). But if a continuous thin film consisting of only metallic particles is laid down, the thickness can be reduced to 3 μin. without any appreciable loss in signal amplitude.

Coating a disk with a thin metallic film is a straightforward route to higher areal densities, but successful manufacturing of a thin-film disk has proved elusive. Ampex Corp., San Jose, which made an early splash with its Alar plated thin-film medium, dropped out early this year; other companies that have touted sputtering the metallic film onto the disk have also had their problems.

Domain Technology Corp., Milpitas, Calif., an early leader in sputtering thin films, encountered production problems that drove it to adopt a more conservative manufacturing approach—plating (Fig. 1). In mid-1984, it began ramping up, but it ran into severe process-control problems, yields fell through the floor, and it was forced to shut its doors and go back into research and development.

Today, Domain is producing cobalt-phosphorus thin-film disks with 650, 800, and 950 Oe. Yields have climbed from a 0% to 50% range to over 80%, but this improvement was achieved by adopting electroless plating. Kenneth Lee, vice president of engineering, says Domain remains committed to sputtered thin film, but volume production won't begin till mid-1987. "We are selling the same product created two



**2. BETTER PROCESS.** Varian claims its disk-at-a-time sputtering process assures better modulation characteristics across the disk surface.

years ago, but now we have established the process controls."

Advocates of sputtering maintain that process uniformity is greater than with electroless plating. "Each disk [in a sputtering chamber] sees the same condition as every other disk entering a chamber," explains Varian's Lavine. "This ensures you get good disk-to-disk modulation characteristics" (Fig. 2).

Low modulation—the difference in signal amplitude going around a track—is harder to maintain in an aqueous solution, which is affected by impurities that build up in the bath, Lavine says. Also, the carriers that move the aluminum blank into the bath must be kept uniformly clean, and "repeatability across an entire carrier is hard to maintain," he says. Though he concedes that the plating method has a higher throughput, a sputtering machine's higher quality more than compensates, he maintains. "Throughput of our machine is a little lower, but the important thing is the higher quality of output per month."

Japanese companies are pushing the state of the art in sputtered media. Almost two years ago, Nippon Telegraph & Telephone Corp. reported it had built a sputtered thin-film prototype drive that exceeded the top-of-the-line IBM 3380 drive-storage density by a factor of almost two and beat IBM's data-transfer rate by 50%. The drive, Patty II, was said to have a track density of 1,800 tracks/in. and a linear density of 25,400 bits/in. using conventional ferrite heads. NTT is developing the drive with several partners it declines to name.

Sputtering has also turned in impressive results when used to control the deposition of iron oxide used as a recording medium. Last September, Fujitsu Ltd. reported sputtering an experimental 50,000-flux-changes/in. iron-oxide medium on a substrate (head flying height was 1.97 $\mu$in.). It says the system was merely to show the potential performance of iron-oxide sputtered media. Commercial use of such media will be at an initial density range of 20,000 to 30,000 flux changes/in. at a more practical head flying height, though for now the company has no plans to create a commercial product.

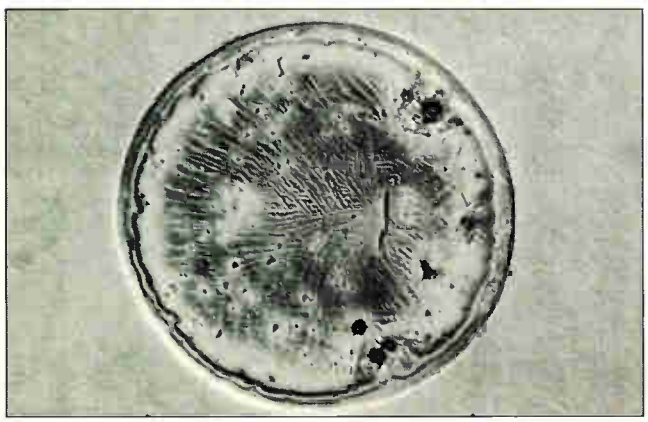
Sputtering thin film may be the wave of the future, but plating is delivering the goods. Stolle Corp., a high-volume producer of blank disks and plated thin-film media in Sidney, Ohio, is trying to increase yields with careful control of the entire manufacturing process.

Starting with the aluminum, Stolle has improved the alloying processes to create a smoother substrate and improve yields (Fig. 3). A common complaint with the blanks is that the particles used to convey strength to the pure aluminum create a surface with too many asperities. Stolle worked out an alloying process that smoothly distributes the magnesium used to alloy the aluminum and creates a homogeneous alloy for oxide-coated disks.

Stolle's next move is to improve the blanks used for thin-film media. Improved yields ultimately depend on rethinking how a substrate is built up, says Ronald L. Schauer, general manager of Stolle's Memory Products Division. "The thin-film industry has been using what has been a process developed to produce oxide disks."

To increase the adherence of the metallic film onto the aluminum blank, the aluminum blank gets a plating of nickel. "When you take a mirror aluminum finish, rough it up with a zincating process, and then plate nickel onto the surface, which must be polished, you are wasting nickel and time in the polishing process," Schauer explains. He and his coworkers are working on a new aluminum alloy, developed especially for thin films, which he hopes will eliminate process steps. He hints it may be ready next year. *–Robert Rosenberg*

**3. SPIT AND POLISH.** Stolle's alloying process produces so smooth a disk that even a drop of saliva creates a major imperfection.



*OPTICAL STORAGE*

## IT MAY BE CLOSE TO CHALLENGING MAGNETICS

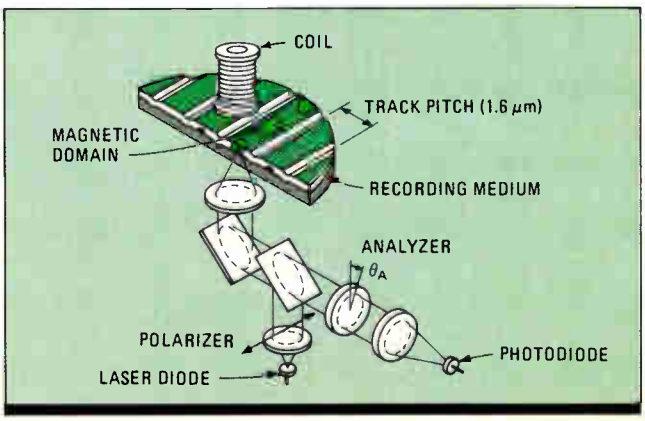
The computer industry has long dreamed of the data storage capacity that erasable optical disk drives could provide, and now the wait for such products may be nearly over. Many companies are now finishing up the development of new media that is the key to a new generation of optical memories. Once that's accomplished, read/write optical disks won't be far behind. Optical disks have one major advantage over magnetic-disk mass storage: tracks can be as close together as bits can be stored in a track.

Optical-disk manufacturers are building on this advantage. They are augmenting write-once media with three types of erasable optical media—magneto-optic, phase-change, and color-change—and are replacing tellurium-based optical media with alternatives that promise longer life expectancy, better operation in severe environments, lower manufacturing costs, and generally improved operating characteristics. And some companies are focusing on write-once media, including Philips, which is developing a medium that, depending on the power of the laser, can be either erasable or write-once. And a small British company, Plasmon Data Systems, has a new write-once medium on the way.

As an example of the optical disk's storage muscle, the LaserDrive 1200 from Optical Storage International, Santa Clara, Calif., stores 14,111 bits per inch and 15,875 tracks/in.; by contrast, IBM Corp.'s 3380 disk drive, the state of the art in magnetic storage, stores 15,240 bits/in. but only 1,600 tracks/in.—one tenth the areal density of the optical-storage device.

Of the three approaches to achieve erasable optical media, the magneto-optic route is favored by many manufacturers of

**1. SPOT DATA.** Lasing a 1-$\mu$m-diameter spot changes its magnetic orientation to write or erase a bit of data.



media and drives. Several companies have shown prototype magneto-optic media: Hitachi, Matsushita Electric, Philips, Sanyo Electric, Sony, 3M, Toshiba, and Verbatim.

In magneto-optic storage drives, writing on a moving disk that has a layer of terbium iron (TbFe), terbium cobalt (TbCo), or cobalt alone—all of which have magnetic flux oriented perpendicular to the plane of disk rotation—is done thermomagnetically. A perpendicular magnetic flux orientation maximizes the transmission and reception of light. The layer has a coercivity of 2,500 Oe and is subjected to a bias magnetic field of about 200 Oe (Fig. 1).

Below the Curie point, the temperature at which the magnetic orientation can be changed, the magnetic field is not enough to change the medium's flux orientation. However, the write laser beam temporarily raises the temperature of a selected 1-$\mu$m-diameter spot on the film. The elevated temperature also reduces the coercivity of magnetic flux there below 200 Oe. Thus the magnetic orientation of flux at this spot can be reversed by the 200-Oe bias field. A "1" is recorded as a spot in which bias magnetization is pointing down, and a "0" is represented by magnetization in the up direction.

In 1980, two media—one of amorphous TbFe and the other of gadolinium terbium and iron—produced a carrier-to-noise ratio of 35 to 40 dB, says Nobutake Imamura of the Kokusai Denshin Denwa (KDD) research and development laboratories in Tokyo. "With improvements in optical heads and storage media, the carrier-to-noise value has been upgraded by about 5 dB a year," he says (chart). A carrier-to-noise ratio of 45 dB or more is necessary for digital data storage.

## IN SEARCH OF A HIGH RATIO

Over the years, the storage medium's composition has been changed to improve the carrier-to-noise ratio. Sony Corp. and KDD worked together to develop a TbFeCo medium. Sony built and installed two prototype 30-cm magneto-optical disks at the KDD lab in October 1984. Though it has a significant jump on every other company, Sony says it will not be close to product development until there is a write-once disk standard.

A TbFeCo combination has been used by Hitachi Ltd.'s Central Research Laboratory in Tokyo to produce a medium that boasts a 57-dB carrier-to-noise ratio. This high figure is made possible by a unique technology that improves the carrier-to-noise ratio of the head and medium by reducing a disk's surface noise.

Other commercial magneto-optic disk makers, such as 3M Co., St. Paul, Minn., now offer 52 to 57 dB, and experimental magneto-optic media have reached a carrier-to-noise ratio as high as 85 dB. Tokyo Sanyo Electric Co. says its magneto-optic recorder still is in development and says it may delay marketing until industry media standards are established.

In contrast to magnetic storage, magneto-optic disk drives cannot write data a bit a time. Instead, an entire track must be completely erased and then rewritten. Two related alternative approaches to erasable optical media are phase-change and color-change media. These have several advantages over magneto-optic media, among them the ability to write a bit at a time, higher carrier-to-noise ratios, longer life, lower manufacturing costs, and faster data-transfer rates.

Of the many research projects under way, two types of phase-change media—one involves amorphous-to-crystalline transformations, the other crystalline-to-crystalline—are commanding a good deal of attention. In the former type, information is stored when a write laser creates a nonreflective, 1-$\mu$m-diameter amorphous (uncrystallized) region in a much more reflective crystalline surface. A read laser can later read the nonreflective amorphous spot. In the crystalline-to-crystalline approach, the write laser hitting a reflective crystalline surface changes a 1-$\mu$m-diameter region to a less reflective crystalline state, which can later be read by a read laser.

An example of amorphous-to-crystalline media in an experimental system is found in the Optical Disc Memory Recorder developed by Matsushita Electric Industrial Co., Tokyo. For recording and playback (Fig. 2), it uses a laser beam with a 0.83-$\mu$m wavelength and an 8-mW incident output power; a 10-mW, 0.78-$\mu$m-wavelength laser is used to erase.

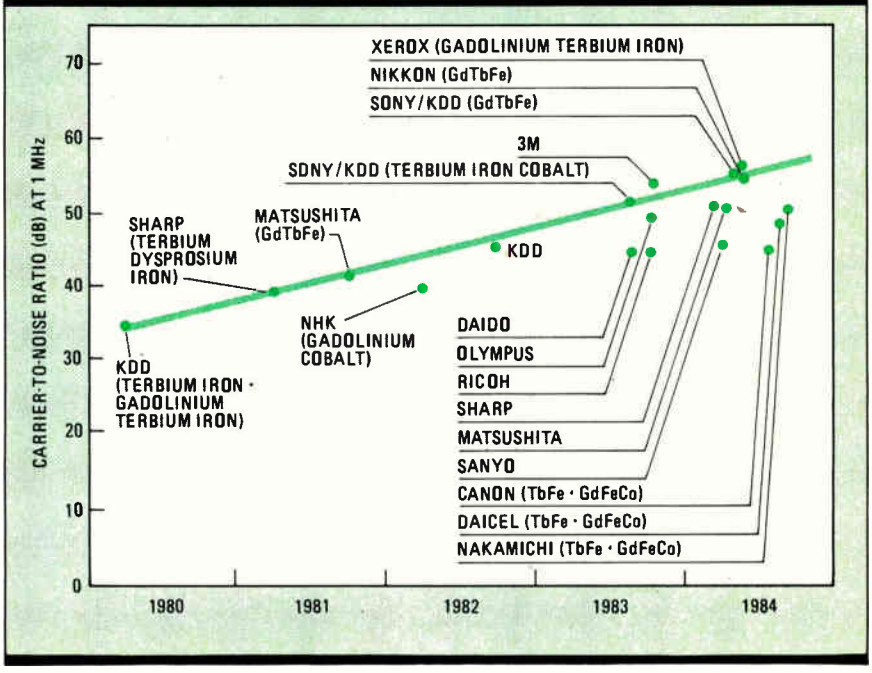
## FAST WORKER

With a single focusing lens serving both read/write and erase lasers, almost simultaneous erasing and recording have been achieved. The Matsushita system is based on patents developed by Energy Conversion Devices Inc. of Troy, Mich. Besides allowing bit-at-a-time recording, amorphous-to-crystalline media offer a difference in reflectivity of the amorphous and crystalline states that is large enough to produce a high carrier-to-noise ratio. Workers at Philips Research Laboratories, Eindhoven, the Netherlands, have reported a carrier-to-noise ratio for amorphous-to-crystalline media on the order of 95 dB, almost high enough to use for high-quality video recording. Philips uses a 0.1-$\mu$m-thick layer of a tellurium–selenium–antimony alloy recording medium.

In spite of these advantages, the medium has drawbacks. One is that the amorphous state tends to be unstable. This problem can be traced to the use of tellurium. This metal, which is attractive because it heats quickly and so allows a rapid change of states, also oxidizes very rapidly in the normal atmosphere, which exacerbates the amorphous-state stability problem. In effect, the entire disk can become nonreflective; this means that all stored data is lost.

To retard corrosion, the medium is sealed in airtight plastic and the metal is alloyed with other metals, notably selenium, for added stability. Fujitsu Laboratories Ltd., Atsugi, Japan, has addressed the amorphous-state stability problem by eliminating tellurium. Its engineers have created a crystalline-to-crystalline medium made of selenium–indium–antimony

*CARRIER-TO-NOISE RATIOS ARE NOW ABOVE 45 dB*



(SeInSb). Company researcher N. Koshino reported that the medium offers sharp contrast of reflection between written and erased states, high sensitivity in writing with a diode laser, and up to 10 million write-erase cycles. The company also found that the life expectancy of the medium is about 10 years.

Writing on the SeInSb medium is accomplished using a 10-mW laser to heat a 1-μm spot for 0.05 to 2 ms. This changes the reflectance of the irradiated spot. Irradiating the same spot with a 5-mW laser for 0.1 to 10 μs returns its reflectance to its original state.

Recently, the Hitachi Research Laboratory, Tokyo, developed alloys that can be used as crystalline-to-crystalline optical-memory media. These include alloys of copper, aluminum, nickel, and zinc in various combinations. Osamu Asai, deputy general manager of the lab, says these alloys have the property of reversibly changing color when exposed to light or heat.

An alloy of silver and zinc assumes different phases with different crystalline structures at high and low temperatures. Each phase assumes a different color. Instead of using differences in light reflectivity to distinguish a "1" or a "0," a difference in color is used.

"When a silver-colored AgZn material is heated to a high-temperature phase region and then cooled, the high-temperature phase stabilizes at room temperature to present a pink appearance," says Asai. After the material is heated to a low-temperature phase region and allowed to cool, it reverts to its silver color. Though the Hitachi medium distinguishes its 1 or 0 state with different colors, the actual storage medium is a metallic layer. It is not a color-change medium, for color-change disks contain an organic dye or dye-binder storage medium. One appeal of organic dye as a storage medium is its low manufacturing cost.

In contrast to other magneto-optic and phase-change media, which are metal films deposited on a glass or plastic substrate using some form of vapor-deposition process, organic dye can be applied using a low-cost spin-coating technique. Another advantage to organic dye is that it can be switched between 1 and 0 states with a relatively low-powered laser.

Mool C. Gupta, a researcher at Eastman Kodak Co., Rochester, N. Y., reports that Kodak has developed a dye-binder system that can be written with a 16-mW laser. The system achieves a carrier-to-noise ratio of 50 dB, comparable to that of magneto-optic media. Significant in the Kodak results is the data-transfer rates the system achieved—5 Mb/s, relatively high for optical systems, which up to now have attained rates of no more than 3 Mb/s. The 5-Mb/s rate also makes it possible for optical media to be competitive with low-end Winchester disk drives, which have the same rate.

All these phase-change and color-change erasable optical media are also being developed as alternatives to conventional metal-film write-once media. In write-once metal-film media, one recording method, called pit-forming, burns a pit permanently into the medium, creating a nonreflective 1-μm-diameter hole in a highly reflective surface. Another recording method, bubble-raising, causes a nonreflective metal surface to bubble into a highly reflective spot 1-μm in diameter.

## TWEAKING THE LASER

Regardless of whether a metal-film, phase-change, or color-change medium is used, laser power is what determines if a medium is to be written and erased repeatedly or written once and thereafter read-only. Typically, laser power between 0.01 and 3 mW can be used to read most optical media. In erasable media, laser power up to 5 mW can be used to erase, and laser power between 10 to 20 mW can be used to record data. Laser power above 20 mW is typically sufficient to ablate the media surface—that is, to create a permanent change in the medium.

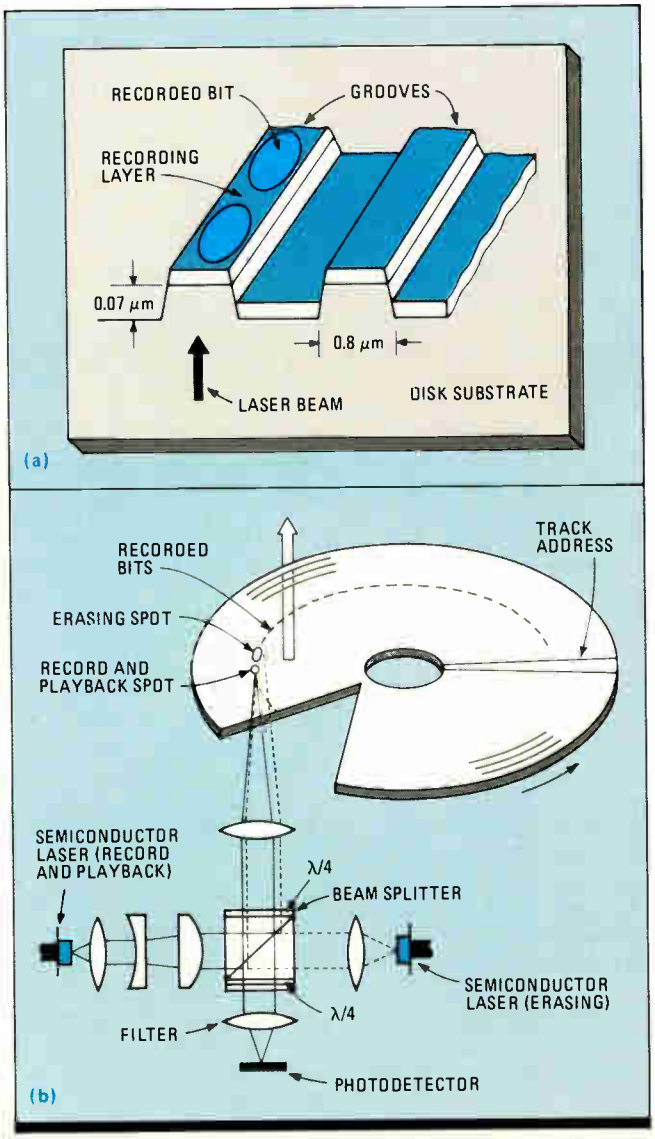
Gary E. Thomas, head of Philips' research labs, says that phase-change media have the advantage over metal-film media of requiring a lower-power laser for recording. Using lower laser power could also help increase the data-transfer rate. He says that phase-change media in write-once applications afford higher resolution, which enables a higher bit density. He reckons that once the phase-change method is perfected, bit density can be increased twofold over conventional pit-forming write-once optical storage.

The Philips labs are developing a tellurium–selenium–antimony phase-change medium that can be constructed as write-once or erasable. During recording in write-once applications, a spot 1 μm in diameter is heated above its melting point. When the laser pulse is completed, the resulting spot is in a permanent metastable amorphous state.

Despite the appeal of dyes and phase-change media in write-once applications, metal films remain the preferred media in most commercial optical-disk products. However, metal-film media cannot tolerate high temperatures, making them unsuitable for military and high-reliability uses. The problem is that almost all such media rely on tellurium alloyed with other metals, which is unstable at high temperatures.

One company has addressed this problem head-on. Plasmon Data Systems, of Melbourn, England, has devised a new medium with no tellurium; instead, it uses a 150-nm-thick layer of platinum, which is sputtered on top of a plastic substrate. The metal heats readily enough for writing but

**2. TWIN LASERS.** A record/playback laser beam (a) and an erase beam work almost simultaneously, allowing bit-at-a-time recording (b).



is thereafter unaffected by temperature.

By itself, platinum would not serve as a good recording medium. The trick is in the fine pattern put into the polycarbonate substrate before the metal is sputtered on. The pattern is a replica of the pattern found in the eye of a moth, which has a very low 15% reflectivity. Company researchers found that the surface of a moth's eye has a fine microcorrugation. The pitch of the corrugation is about 280 nm, much smaller than the wavelength of the laser used to write on the disk surface. To make its medium, Plasmon recreates this pattern on a polycarbonate substrate and sputters a 150-nm-thick layer of platinum evenly over it.

During writing, the micron-wide spot illuminated by the write laser beam produces a temperature of 200°C for 20 ns. Such intense heat even for so short a time is enough to deform the plastic substrate, which removes the fine pattern. The heating also causes the platinum to bubble.

As the bubble forms, the pattern in the platinum is likewise smoothed. As the smoothing occurs, the reflectivity of the metal increases. Once the bubble has been raised, the reflectivity of the spot has been permanently increased from 15% to 50%, thus permanently writing a bit of data. Unlike tellurium, platinum does not easily corrode; therefore, plastic sealing of the media is not as critical, and the life of the medium should be as good or better than existing products. The only other life-shortening factor is deflation of the bubble. This is prevented because both the metal and the substrate deform, and so the bubble could never resume its low-reflectivity state. *–Jonah McLeod*

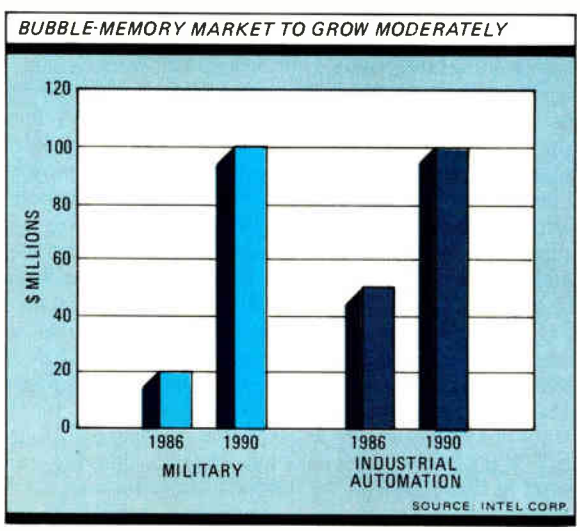
*Additional reporting was provided by Michael Berger in Tokyo and John Gosch in Frankfurt.*

*BUBBLE MEMORIES*

## BLOCH-LINE WORK COULD PULL IT OUT OF NICHE

Magnetic bubble memories were once trumpeted as the next high-volume memory product, thanks to extremely high densities, nonvolatility, and potentially low cost. Then the trumpets went flat: improvements in magnetic disk technology came fast and prices dropped and densities improved more than expected, and bubble memories turned out to be more expensive, difficult to use, and troublesome to design into products than first thought. But these solid-state storage chips are clinging to significant niche markets—notably, ruggedized military equipment and industrial automation. And recent U.S., West German, and highly funded Japanese research in Bloch-line memory—an offshoot of the bubble memory—suggests future densities of several gigabits per square inch—higher than any other storage medium. In fact, Bloch-line memories may propel bubble technology out of its niche.

Although the few players in the bubble-memory business consider it a sizable market, it is far from being large enough to support many vendors. Intel Corp., which has pulled together some figures on market size and growth, estimates the world market for bubble memories at $75 million in 1986, rising to between $150 million and $200 million in 1990. Breaking this down into the two major segments yields $50 million to $55 million for industrial automation (from point-of-sale terminals to process control) and about $20 million for military applications in 1986, and $100 million for industrial automation and $75 million to $100 million for the military in 1990 (chart).




Two Tokyo companies—Fujitsu Ltd. and Hitachi Ltd.—are offering bubble memories. In the U.S., Intel is the only remaining supplier. But research and development continues at these companies and elsewhere; NEC Corp., Tokyo, has development work under way, and there is a bubble-memory startup in the U.S.—Magnesys in San Jose, Calif.

Today's most advanced bubble-memory products are based on 4-Mb technology. Intel has been delivering a variety of 4-Mb products for about two years. Fujitsu will begin volume production of 4-Mb bubble-memory chips this month, and will market board and cassette products with these chips later in the year. Hitachi has developed and is marketing bubble-memory chips with density levels of 6 by 6 μm per cell and capacities of 64 Kb, 256 Kb, 1 Mb, and 4 Mb. The company announced its 4-Mb device nearly two years ago.

Bubble-memory development at Intel's Magnetic Operation in Folsom, Calif., is centered on improving the process technology at the film level—the epitaxial layer on the garnet substrate—for increasing the yields of chips with broader operating temperature ranges. In addition, work is continuing on developing the next step in density—the 16-Mb chip.

Intel is very interested in increasing yields of chips that can operate down to –40°C or –55°C and up to +125°C for a yield level similar to that of 0°C chips. The military market, one of Intel's main targets, needs bubble memories that perform throughout the military operating temperature range of –55°C to +125°C for many of their applications.

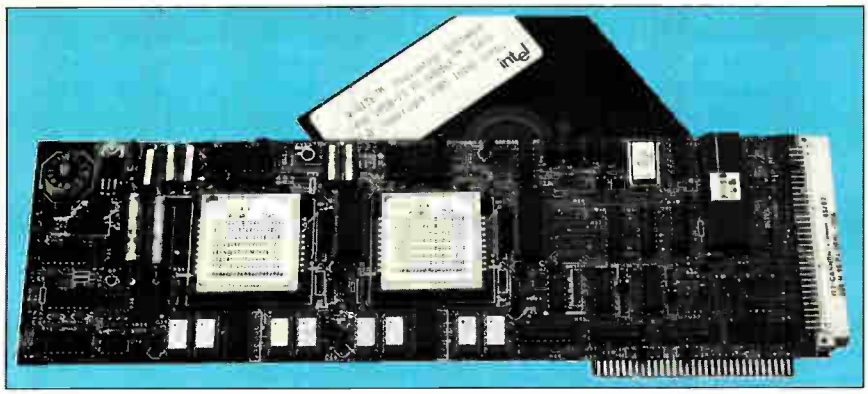
The Air Force Wright Aeronautical Laboratories Avionics Lab at the Wright-Patterson Air Force Base in Ohio awarded Intel a $4.8 million bubble-memory development contract to increase the temperature range of its 4-Mb devices and to decrease the access time to at least 40 ms and potentially to 20 ms. The contract also covers development work on the 16-Mb chip.

By contrast, some Japanese work has focused on other parameters. Fujitsu has improved the data-transfer rate of its 4-Mb chip to 1.6 Mb/s from 100 kb/s in the older 1-Mb memory chips, and the company's engineers have decreased power consumption of bubble-memory systems by using CMOS circuit technology in the support chips.

Hitachi's most recent breakthrough is a new type of packaging—PFC (picture-frame core), so named because the structure uses a magnetic core that resembles a picture frame. The package structure, which is two thirds thinner and has an area one third smaller than a conventional package, also makes it easier to use automated assembly because all parts fit together in layers. Research is under way at Hitachi to develop a 16-Mb chip.

Neither Hitachi nor Intel is releasing target dates for the introduction of 16-Mb chips. "Going from 4 Mb to 16 Mb is a major step in process technology," says Ulmont Smith, Intel's product marketing manager for bubble memories. "It will require perfecting the I2P2 [ion-implantation] processing for the propagation path. Once we get into I2P2, then the sky's the limit—we can go to 64 Mb and up." Fujitsu also is developing a 16-Mb bubble-memory device.

NEC, which has yet to commer-




**PERSONAL BUBBLES.** The Intel PCB-75 bubble-memory board for the IBM Personal Computer and compatibles allows many users to easily evaluate bubble-storage technology.

cialize bubble-memory products, concurs that ion implantation is very promising for fabricating very high-density bubble-memory devices. The company has developed 4-Mb chips with 1-μm diameters using ion-implantation technologies, according to a company spokesman. Its chips also contain cache structures that consist of long data-storage minor loops and very short data-access loops. Average access time for these 4-Mb chips is 0.7 ms under 100-KHz rotating-field conditions.

## BUBBLE STARTUP

The bubble-memory market prospects are attractive enough for at least one new startup, Magnesys, whose aim is to make a subsystem that customers can use right away without having to worry about the details of bubble-memory implementation. The company's founders, veterans of the bubble-memory-component industry, obtained $2.75 million of venture capital last November to finish developing and begin marketing fully integrated systems targeted at end users. Ted Wuerthner, Magnesys' president, says the company has completed its development and has shipped products to beta-test sites on schedule. Magnesys has developed its own advanced bubble process and will be making its own chips but is not ready to reveal any process details. All that Wuerthner will say is that "we are taking bubble technology to its next-generation form.

*The next big step in bubble memories is the 16-Mb chip*

"We are making a solid-state device that is suitable for our kind of system—a complete small-capacity storage subsystem in a small package," he adds. Magnesys is targeting the same two primary market segments as Intel: factory automation and the military. It plans its product introduction for this fall.

Intel is offering a kit for the IBM Corp. Personal Computer that helps users evaluate bubbles (figure). "We are emphasizing the need for higher levels of integration for bubble-memory products," says Smith. "In addition to the PC Bubble product, which has been very successful, we offer boards and cassettes." Smith hints that more highly integrated bubble-memory products will be forthcoming. Current work focuses on lowering the cost of the memories.

Despite general enthusiasm, though, the technology has its detractors. Toshiba engineers, for example, believe they have made the right decision in not pursuing bubble memories. "The memory capacity of semiconductor memories is rapidly increasing, so the need for bubble memories is decreasing," says a company spokesman. Unless the capacity of bubble memories increases tenfold, he says, they won't be useful.

A compelling response to this criticism is the Bloch-line memory, which promises just such an increase in capacity. Bloch-line memory is a new magnetic storage technology that is based on basic bubble technology but far surpasses it in density [*Electronics*, Oct. 14, 1985, p. 16]. Under study and development at Carnegie-Mellon University in Pittsburgh, Kyushu University in Japan, and the Universität GH Wuppertal in West Germany, it uses a magnetic-bubble domain in the form of a stripe within the wall of a magnetic bubble that separates the bubble from the surrounding magnetic material. By encoding many bits within the stripe, one bubble can yield many bits of information instead of only one.

At Carnegie-Mellon, Bloch-line group leader Floyd Humphrey reports great success with the first read/write gate. The group started by building a write gate, and was pleased with the results. After discovering that building a read gate was also easy, Humphrey's team decided to go ahead with a read/write gate, which has now been fabricated and tested. "The results are very encouraging," says Humphrey. "We achieved very good margins—for example, about 2 to 1 in current [for a signal to detect a 1 versus a 0 bit] and nearly the same in time. We expected a much lower margin the first time out." For the first try, the researchers did not attempt to optimize anything—they just wanted to put a read/write gate together to prove they could do it. They were pleasantly surprised that the margins turned out to be so high.

The Carnegie-Mellon team says that success with a read/write gate is important because it allows the start of a Bloch-line memory fabrication process that could reach the high density level promised by the theoretical work and early experiments. A read/write gate means that gates can be put at each end of the loop—read on one side, write on the other—and interleaved. The main question is whether Bloch lines are stable, Humphrey says. "We are ready to start taking data on that now. Then we must learn to define the cells [in the stripe]."

NEC Corp. calls itself "the most aggressive company in the world in Bloch-line memory research." In a joint project with Kyushu University, work is under way to develop chips with densities in the range of 32 to 64 Mb/cm$^2$. But the Kyushu researchers were surprised to learn that it takes much more effort and attention to detail to fabricate Bloch-line chips than they expected, according to an independent industry observer who wishes to remain anonymous. This observer says that the first six chips attempted did not work and that the project has no experimental results yet.

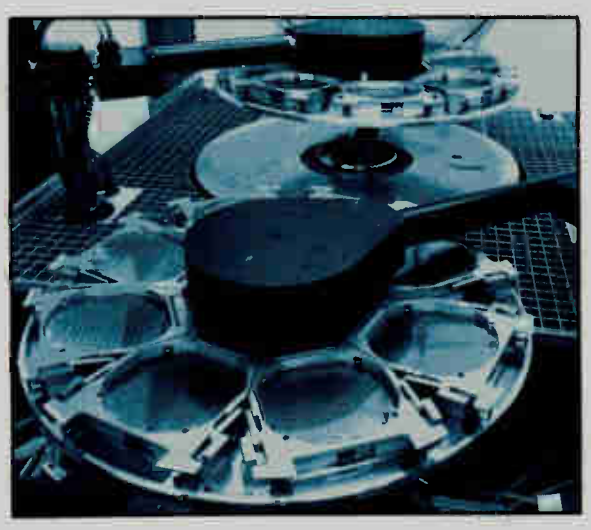
The main Japanese advantage is funding. It is estimated that Bloch-line research in Japan is funded two to three times more heavily than in the U.S. Humphrey says he is unaware of any Bloch-line work in the U.S. other than his research at Carnegie-Mellon. Canon, Hitachi, and Sony have Bloch-line memory projects under way, and Fujitsu says it is considering starting research. In fact, Hitachi has money set aside for Bloch-line work, but it faces a shortage of experienced researchers to get a project started.

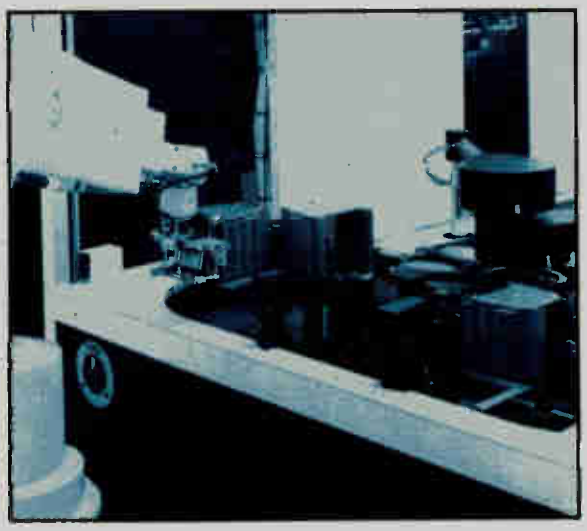
Fujitsu wants to concentrate first on bringing out its 16-Mb bubble chip that uses a hybrid scheme. But the company is interested in Bloch-line technology, on which it expects to start work in about a year. If current Bloch-line research at Kyushu and Carnegie-Mellon does not encounter any major snags in the next year, then Fujitsu is likely to drop its push for a 64-Mb bubble memory and turn its efforts toward developing a Bloch-line product. Though Japan may appear to be a little behind in Bloch-line research, the U.S. effort depends entirely on the work of one lightly funded group. The Japanese, by contrast, have turned some big guns on the challenge. *–Tom Manuel*

*Additional reporting came from Michael Berger in Tokyo.*

Electronics SPECIAL ADVERTISING SECTION

# SEMICONDUCTOR PROCESSING AND MANUFACTURING





# IMPROVING SEMICONDUCTOR SALES AND NEW ADVANCED TECHNOLOGY BOOST PROCESSING EQUIPMENT SALES

The semiconductor-processing segment is feeling the benefits of the recovering demand for integrated circuits. Not only is domestic and foreign consumption up but new production processes are coming on the market, promising to stimulate sales even more.

Demand for semiconductor-production equipment in the U. S., estimated at $2.4 billion in 1985 by the *Electronics* 1986 Market Report, will edge up 2% this year, bringing consumption to $2.5 billion. And the industry is looking for a sustained boost from improving semiconductor sales. Other stimulants include an aggressive drive by U. S. equipment companies into offshore markets, the growing demand for application-specific ICs, and the expected demand for automated production equipment.

Domestic semiconductor and test equipment producers are working hard to expand sales in foreign markets—mainly Japan, Korea, and China, whose IC companies are potential major customers. For some U. S. companies, these efforts are already paying off. A few have even formed joint ventures with their Far Eastern counterparts.

With Japan expected by Perkin-Elmer's Semiconductor Equipment Group to account for 45% of the total worldwide IC consumption by the end of this year, that country has become a particularly desirable market.

While companies are searching for new

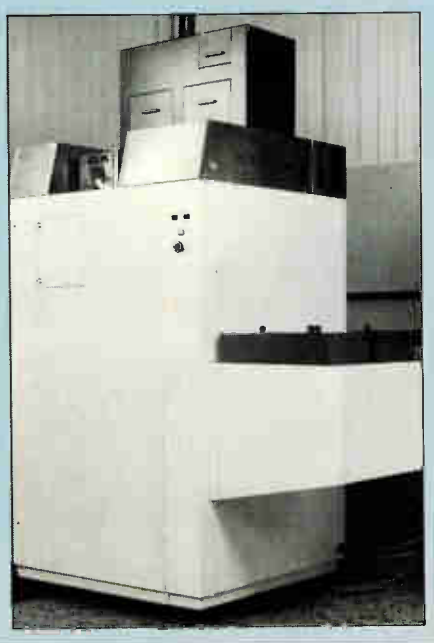
*(Continued on page 40)*

## New-generation wafer stepper available from ASM Lithography

ASM Lithography Inc. is ready to cash in on the growing market for gallium arsenide devices, a critical one for manufacturers of advanced lithography systems with ultrafine-line direct-write capability, says James Alexander, vice president for marketing and sales.

The company recently began marketing two new lithographic systems—a vector-scan electron-beam unit and an automatic wafer stepper. The Beamwriter, an electron-beam system for use in the production of GaAs chips, including microwave FETs, has a 50-kV acceleration voltage for ultrafine-line pattern definition. It was developed by Philips, the Netherlands, which with ASM International established the Tempe, Ariz., company in 1984. Recent customers for the system include Avantek Inc. and Microwave Semiconductor Corp.

ASM Lithography also has started deliveries of the PAS-2500, a fully automatic wafer-stepper system with a 0.9-$\mu$m working resolution and an overlay accuracy of 0.1 $\mu$m. It is used for volume production of submicron very large-scale integrated circuits and of wafers with 6-in. diameters. Its electromagnetically driven stage covers a 1-cm step in 200 ms, about 25% faster than other systems on the market. Typical throughput is seventy-five 6-in. wafers per hour.



The system, the result of a joint development effort between ASM International and Philips, uses a through-the-lens self-compensating laser alignment technique to achieve its overlay accuracy from one layer to another. The technique eliminates drift as well as the need to recalibrate the system.

A Zeiss 46 lens is standard, giving the PAS-2500 an exposure field 20 mm in diameter; a Zeiss 52 lens is optional. The system can accommodate a family of lenses without modification, including higher-resolution lenses now in development.

The PAS-2500 also has a reticle management system that performs a fast exchange of reticles for drop-ins and other application-specific uses.

# INTRODUCING A BREAKTHROUGH IN 600 MIL PRODUCTION


*Delta 6600... an investment in tomorrow that pays off in greatly increased throughput and tester utilization... today.*

The future in totally automated handling systems is here. Delta 6600 is the world's first fully automated production-level test handler. It's designed to revolutionize 600 Mil DIP testing with a fourfold increase in throughput, a threefold improvement in utilization of valuable test equipment and significant bottom line cost-per-part savings.

100% tester utilization alone would make the 6600 a sound investment. It is one handler that will keep valuable VLSI test systems going flat out. And production lines humming.

Fast and fully automated, it works unattended with a minimum of operator involvement. Add extra large storage, input, sort and off-load capacities, and you have the production-level handler of tomorrow. Here, right now.

So, call (619) 292-5000 or circle the reader number and we'll give you the details on the Delta 6600 and a good long look into the future of 600 Mil handler systems. Delta 6600 . . . the production solution.

Delta Design®
A Cohu Company

SEE US AT SEMICON WEST BOOTHS 4761-4764

Circle 75 on reader service card

## Perkin-Elmer delivers its electron-beam lithography system

Perkin-Elmer Corp. has started delivery of the Aeble 150, an electron-beam lithography system that directly writes circuit features as small as 0.5 μm. The system can process over twenty 4-in. wafers per hour, a throughput rate made possible by two features—a vector-scan variable-shaped beam that allows quick customization for the application-specific market and a write-on-the-fly scheme that reduces stage movement overhead. For higher productivity, the system can also expose 5- and 6-in. wafers.

The first two systems are being used to make chips for the Very High Speed Integrated Circuits program, and the Norwalk, Conn., company is trying to ready the system for the commercial market.

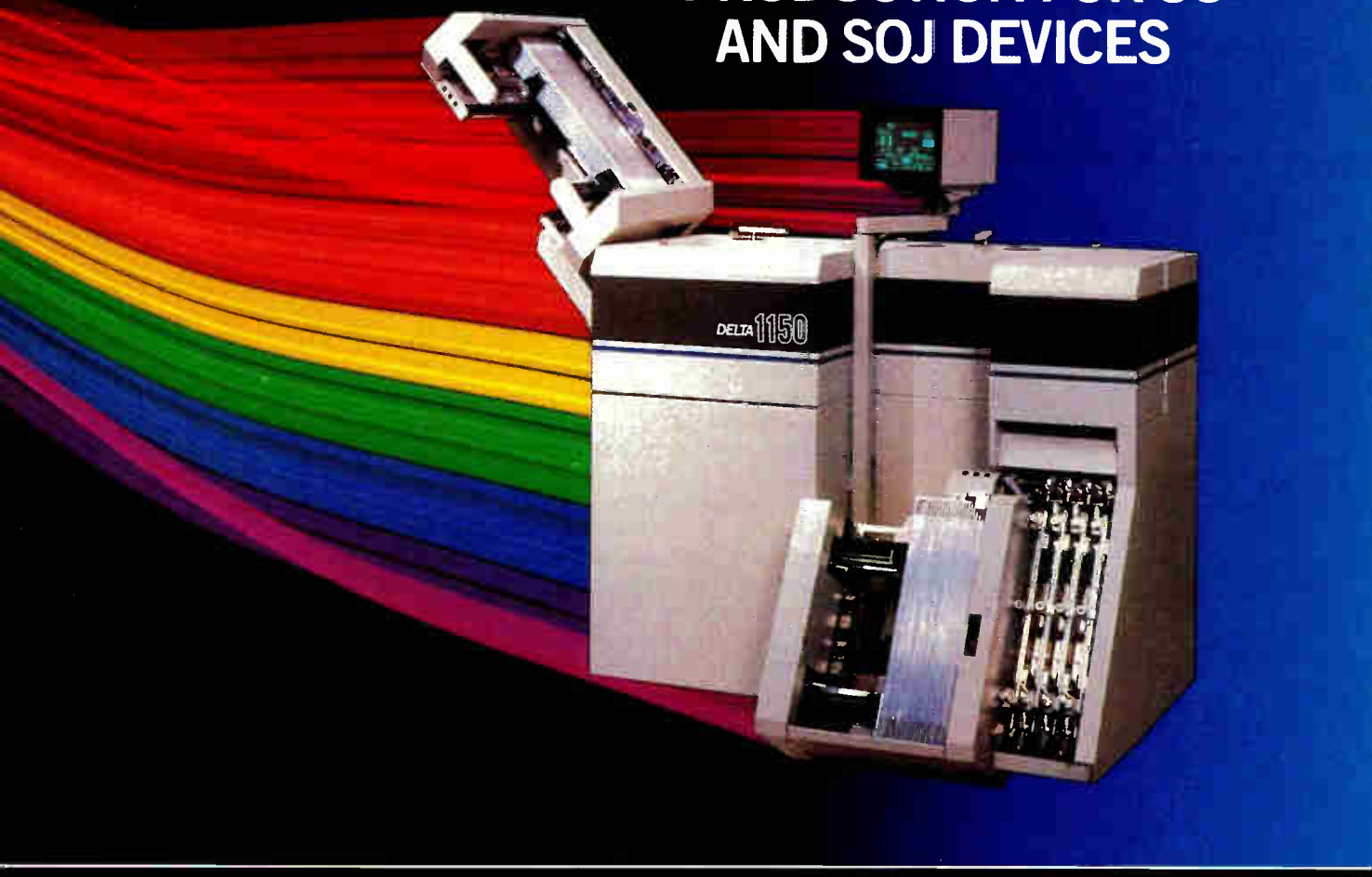
Perkin-Elmer also has been extending its lines of more traditional processing equipment. Among its new offerings are mask aligners, a step-and-repeat system, and a dry-etching system.

The high-end Micralign 600 HT series of projection mask aligners incorporates field-proven optical and automation systems for a machine-to-machine overlay accuracy of ±0.35 μm. Throughput is 100 6-in. or 120 4- or 5-in. wafers per hour, and resolution is from 0.9 to 1.25 μm. The low-end version, the Micralign 600 Delta has an overlay specification of ±0.5 μm and a resolution of 1.5 μm. It handles 100 4- or 5-in. wafers per hour and 85 6-in. wafers per hour. The system can be fully upgraded to the HT in the field.

The SRA-9000 series step-and-repeat alignment system offers submicron resolution at a production throughput of up to 60 wafers per hour with a 0.35 N. A. lens, including alignment and leveling at each exposure field. Using a 0.28 N. A. lens, its throughput is as high as 70 wafers per hour with a working resolution of 1.1 to 1.25 μm. The SRA-9000 has an alignment accuracy of ±0.15 μm in the field-by-field mode and of ±0.35 μm in the optional backup laser stage mode.

The company also offers the Omni-Etch 20000, a dry processing system that handles 6-in. wafers at throughput rates of 40 to 80 wafers per hour. Its pick-and-place wafer-handling system minimizes particulate generation, enabling the system to meet the requirements of a Class 10 clean room.

# INTRODUCING THE KEY TO SMD PRODUCTION FOR SO AND SOJ DEVICES




## *Delta 1150 . . . a totally automated production-level test handler that does 10,000 dph and makes testers work flat out to keep up.*

At last, a solution to the high-speed handling problems that bug small outline device production, and slow it to a crawl.

Delta 1150 makes fast, fully automated, production-level testing of hard to handle SO and SOJ surface mount devices a reality. With advanced hardware and software . . . and an input/output extruded aluminum magazine that makes it possible.

When it comes to real time production performance, plastic sleeves just can't take the heat. That's why precise, reusable aluminum magazines are indispensable to trouble-free automation . . . and are the key to Delta 1150's automated magazine loading and unloading systems.

Unique trackwork, common to both the magazine and handler, captures the parts, ensuring positive control throughout the system. Temperature is independently controlled in the storage chamber and at the test sites, enabling precise thermal control of the DUT. At the test site, two contactors with short lead kelvin contacts, guarantee test integrity.

For more data about Delta 1150, the SMD test handler destined to set new test speed and production records for years to come, call (619) 292-5000 or circle our reader number. Find out what total automation can do for your surface mount small device production. Delta 1150, the production solution.

Delta Design®
A Cohu Company

SEE US AT SEMICON WEST BOOTHS 4761-4764

Circle 39 on reader service card

market opportunities around the world, they also are paying more attention to new product prospects. ASICs are one bright spot for makers of IC-processing equipment, who have a gap to fill where existing production capability falls short.

## Growth in ASICs

The devices already make up a big chunk of the IC market, accounting for an estimated one fifth of all ICs sold and expected to grow 30% annually to become one third of all ICs sold by 1990, according to projections from General Electric Co.'s Microelectronics Center. At that point, ASICs will be a $20 billion market, says GE. Integrated Circuit Engineering, a Scottsdale, Ariz., consulting and research firm, puts compounded annual growth for ASICs at 33% and expects the market to ring up $9 billion in sales by 1990.

The ASIC market is just one reason that manufacturers of chip-processing equipment are continuing to invest in improving the state of their art. Another reason is to meet the needs of semiconductor makers whose IC designs have ever-higher circuit density and greater scale. These designs require increasingly sophisticated production equipment. In addition, technical advances in wafer processing will be necessary to achieve the finer line definitions needed to put up to 1 million logic gates on a single chip—the projected density of an ultralarge-scale IC.

At the same time, new processes will be required to increase throughput and to handle wafers with 6- or 8-in. diameters, as opposed to the 3- to 5-in. wafers common today. Much of the push into ASIC production hardware will come from startups, which have been using laser beams fired directly onto silicon surfaces to tailor semicustom chips.

Manufacturers having to cut costs and improve yields of very large-scale ICs are pushing toward full automation of semiconductor processing, including assembly and testing of ICs. Quality and purity continue to be overriding considerations in the evolution of higher-density VLSI chips, pushing the drive to higher levels of computer control. Future semiconductor production facilities will no doubt be fully automated: the goal is eventually to link all aspects of IC production in a computer-integrated-manufacturing network.

## Big payoff

Developments along these lines are beginning to pay off. In the past year or so, machines have been introduced that accommodate 8-in. wafers, and progress in the field of X-ray lithography is moving that technology from the laboratory to the production floor. Competition to manufacture production X-ray lithography systems is heavy among companies in the U. S., Japan, and West Germany.

And a competing technology is already on the way. A new wave of laser-assisted and laser-based semiconductor-processing systems are nearing the market for applications that require submicron chip geometries and for ASICs. Other efforts are focused on such areas as forming high-resolution diffraction gratings for narrow-band laser diodes, connecting optical-fiber links directly to wafer surfaces, and developing yield-forecasting systems that detect minute defects in compound semiconductor materials.

## Surface mounting

Lasers are also being used to check the solder joints of surface-mounted devices. Surface mounting has become one of the fastest growth areas in the industry, accounting for half of all pc-board assemblies, according to some market researchers, including

(Continued on page 46)

# Introducing stepper technology so advanced few people know what to do with it.

*"We expect our facilities to be the finest wafer fab operation in the world..."*

*"...We evaluated the ASM Lithography system and found it qualifies for our needs."*

*—T.J. Rodgers, President*
*Cypress Semiconductor*

Drop by Semicon West booth #4401 and get acquainted with the company, the technology and the tool that are destined to change the way the entire IC community aligns itself.

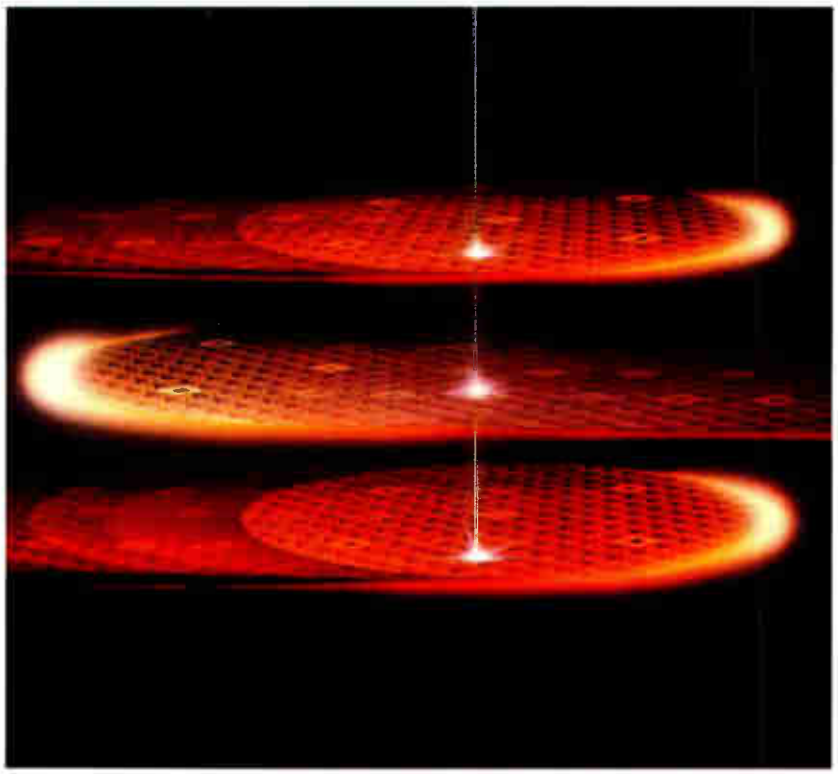
**ASM Lithography**

a joint venture between Philips and ASM International.

ASM Lithography, Inc./P.O. Box 26083/Tempe, AZ 85282/(602) 438-0559
ASM Lithography B.V./P.O. Box 8805/5605 L.V. Eindhoven, The Netherlands/(40) 58 08 00

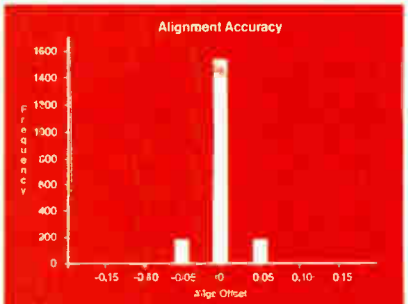
Circle 43 on reader service card

# The SRA-9000 series steps to submicron levels with the industry's highest throughput.



*On axis* *Full field (24 mm dia.)*

*0.9μm wide lines and spaces in 1.15 micrometer 1470 resist (1000 Å $SiO_2$ over Si)*




*Histogram illustrating field-by-field alignment accuracy of 8 consecutively manufactured SRA 5X systems.*

Meet the SRA-9000 series 5X step and repeat alignment system. It offers you submicrometer resolution capability, a fail-safe backup laser stage/global alignment system, 150mm wafer capability...with an impressive production throughput of up to 70 125mm wafers per hour, including alignment and leveling at each exposure field.

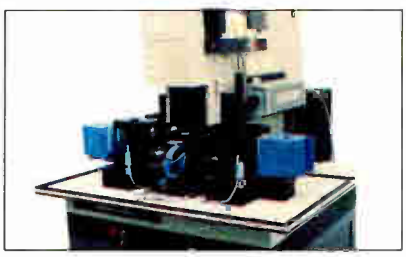
The SRA-9000 series is available with your choice of a 0.28 or 0.35 N.A. lens. Both lenses utilize the mercury h-line for exposure, thus increasing resolution and depth of focus. The 0.35 N.A. lens delivers advanced imaging performance and a large 24mm image field diameter to yield the industry's highest throughput in the submicrometer region.

The new dark-field laser stage/global alignment system operates in conjunction with the standard field-by-field alignment system in a totally automatic drop-in mode. This powerful backup system is automatically engaged if the primary field-by-field alignment signals fall below required levels, thereby maximizing process latitude. Field-by-field alignment accuracy is ±0.15μm; laser stage/global alignment accuracy is ±0.35μm for 98% of the data.

Only the SRA-9000 series offers so many advanced features in a machine that is available today.

To put it to work on your production line, contact Perkin-Elmer, Semiconductor Equipment Group, 761 Main Avenue, Norwalk, CT 06859-0212, (203) 834-6341; or your nearest Perkin-Elmer sales office.

**One Source. Every critical step of the way.**



**SEE YOU AT SEMICON/West '86**
**May 19 through 22 • Hall of Flowers**

**PERKIN-ELMER**

## Delta Design shows gains with surface-mount technology

While some electronics companies foundered last year, Delta Design bettered its past performance. A broad mix of products with a strong emphasis on surface-mount technology helped the Cohu Inc. subsidiary to increase sales and profits.

"Over half our business last year was related to surface-mount technology," says Roger Williams, director of marketing. He also says that over half Delta Design's development budget is dedicated to surface-mount applications.

Among the new products from the San Diego company is the model 6600, a fully automated ambient-hot (to +155°C) production-level handler. It is designed for use in testing 600-mil dual in-line packages that have 24 to 48 leads.

In operation, sleeves of devices placed in the system's input are automatically oriented, emptied, and stored for refilling with tested devices at the end of the handler's cycle. The DIPs travel through a thermal storage area where they are preconditioned and then tested and graded. Once tested, they are sorted and loaded into the sleeves. Throughput, including a 600-ms test time, is 6,000 devices an hour.

Also introduced last year was Delta Design's model 1150, used in testing small-outline surface-mounted devices with 8 to 16 leads.

The 1150 handler, which preconditions small-outline devices and presents them for testing, operates automatically. It works with a computerized test system that analyzes and grades the devices, then releases them into a sort system. Devices are fed into the 1150 by means of a 50-magazine loading system; each of the reusable aluminum magazines holds six sleeves. The handler can run unattended for approximately an hour at a throughput rate of 10,000 devices an hour.

A third new Delta Design system is the model 4200, which handles three types of semiconductor devices: pin grid arrays, flat packs, and hybrids. This handler provides menu-driven operation using a cathode-ray-tube display. A magazine that holds up to 12 plastic or aluminum sleeves feeds devices to the handler. The system sorts up to 12 categories.

Delta Design also makes a variety of temperature chambers for batch testing of electronic components as well as for laboratory use.

Foreign customers are accounting for an increasing percentage of the company's sales, says Williams. "It's not a crunch, exactly, but there's a lot of offshore activity. In some cases, they want day before yesterday delivery. They waited too long before making a commitment to boost capacity."

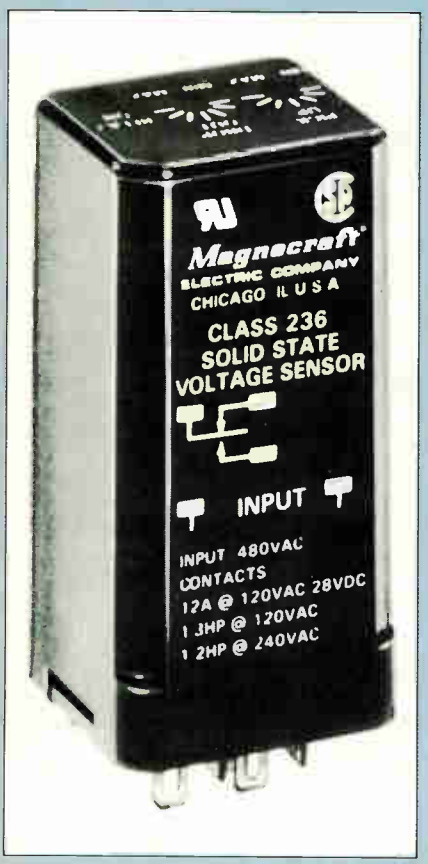
## Magnecraft offers new class of CMOS voltage sensing relay

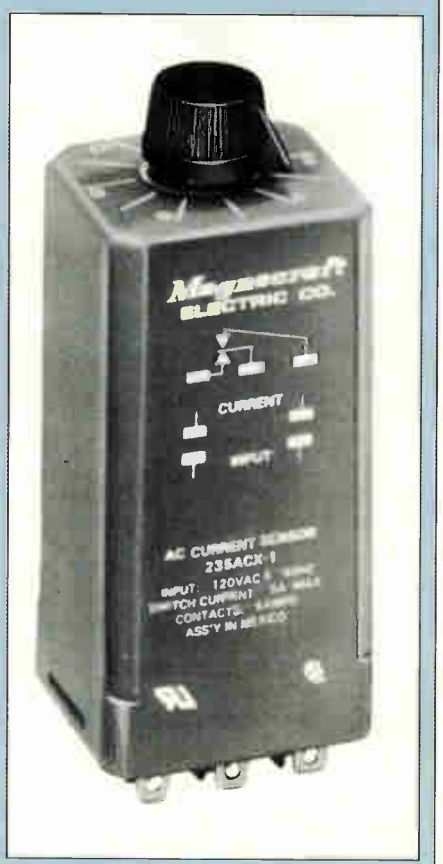
New from Magnecraft Electric Co. is the Class 236 voltage sensing relay, a low-power device that includes a solid-state CMOS sensing circuit. The UL-listed part comes with 120-, 240-, or 480-V ac inputs; the 480-V model operates without use of transformers.

Independent adjustments control pull in and hysteresis (drop out); pickup can be adjusted from 75% to 115% of nominal voltage; hysteresis can be adjusted from 75% to 98% of pickup. Thanks to this broad range, the circuit can be used as either an overvoltage or undervoltage sensor, says the Northbrook, Ill., company.

Magnecraft has moved into a new product area with a field-adjustable device that senses ac electronically. The Class 235 current-sensing relay is a single-pole double-throw device rated at 10 A. In use, connection is through ¼-in. quick connectors and mounting is either with a tapped hole or optional bracket. Socket mountings are available with 0.187 quick connectors. Its current range is 1.5 to 15 A with a 120 V ac coil.

The relay is being used in a variety of applications, according to Ed Rauch, product manager. One application for the part is to monitor current to a motor to determine when an electrical load has been lost. Another is in monitoring inaccessible modes in ovens.




Electronic Trend.

Optical lithography, which is well along in the automation process, is expected to continue to thrive, primarily because the process is continuously upgraded without adding to manufacturing costs. Over the long-term, the markets for semiconductor-production equipment look outstanding, fueled by the rapid pace of technological advancement and the vast potential for continued growth of the semiconductor market. One good indicator of the industry's strength: last year, the membership of the Semiconductor Equipment and Materials Institute rose to over 1,000 corporations, up from approximately 960 companies the previous year. That in itself is a vote of confidence. ■

### FOR MORE INFORMATION

**ASM Lithography Inc.**
P. O. Box 26083
Tempe, Ariz. 85282
(602) 438-0559
Circle 43

**Delta Design Inc.**
5775 Kearny Villa Rd.
San Diego, Calif. 92123-1111
(619) 292-5000
Circle 75
Circle 39

**Magnecraft Electric Co.**
1910 Techny Rd.
Northbrook, Ill. 60062
(312) 564-8800
Circle 40

**Perkin-Elmer Corp.**
**Semiconductor Equipment Group**
761 Main Ave.
Norwalk, Conn. 06859-0212
(203) 834-6341
Circle 44

ANORAD
THE POSITIONING SPECIALISTS

# High Accuracy Positioning Systems *Custom Engineered From Standard Components*

**TYPICAL TURNKEY SYSTEMS**

5 Axis Machining Center

Automatic Vision Inspection System

## MULTI-AXIS SYSTEMS

Tuning Robot: XYZθ vision

ANOGLIDE™ air bearing system

## CONTROLS

ANOMATIC™ CNC Controller

ANOTRONIC™ custom controller

## POSITIONING TABLES

ANORIDE™ X-Y positioning table

ANORAIL™ high speed & long travel

ANOROUND™ rotary tilt option

## POSITIONING COMPONENTS

Encoder

Vision Camera

Intelligent Axis Card

At Anorad, we specialize in understanding your positioning requirements, and translating those needs into custom engineered solutions using our standard, pre-engineered products. Leading manufacturers rely on Anorad for cost-effective positioning solutions for some of their most demanding applications.

Standard, high precision linear and rotary positioning tables form the foundation of our building block approach to system design. Our ANORIDE™ tables employ an extremely reliable crossed roller design while ANOGLIDE™ tables incorporate precision air bearings for friction-free motion. The ANORAIL™ series is utilized for very high speed, long travel applications and features ANOLINE™ linear DC servo motors.

What's more, all of our positioning tables are easily configured into multi-axis, custom engineered positioning systems.

Control can be provided by Anorad's ANOMATIC™ CNC controller, an Intelligent Axis Interface to a host computer, or a controller specially designed for the application. Depending upon the application, sensors, vision systems and work performing devices can be incorporated to provide turnkey systems.

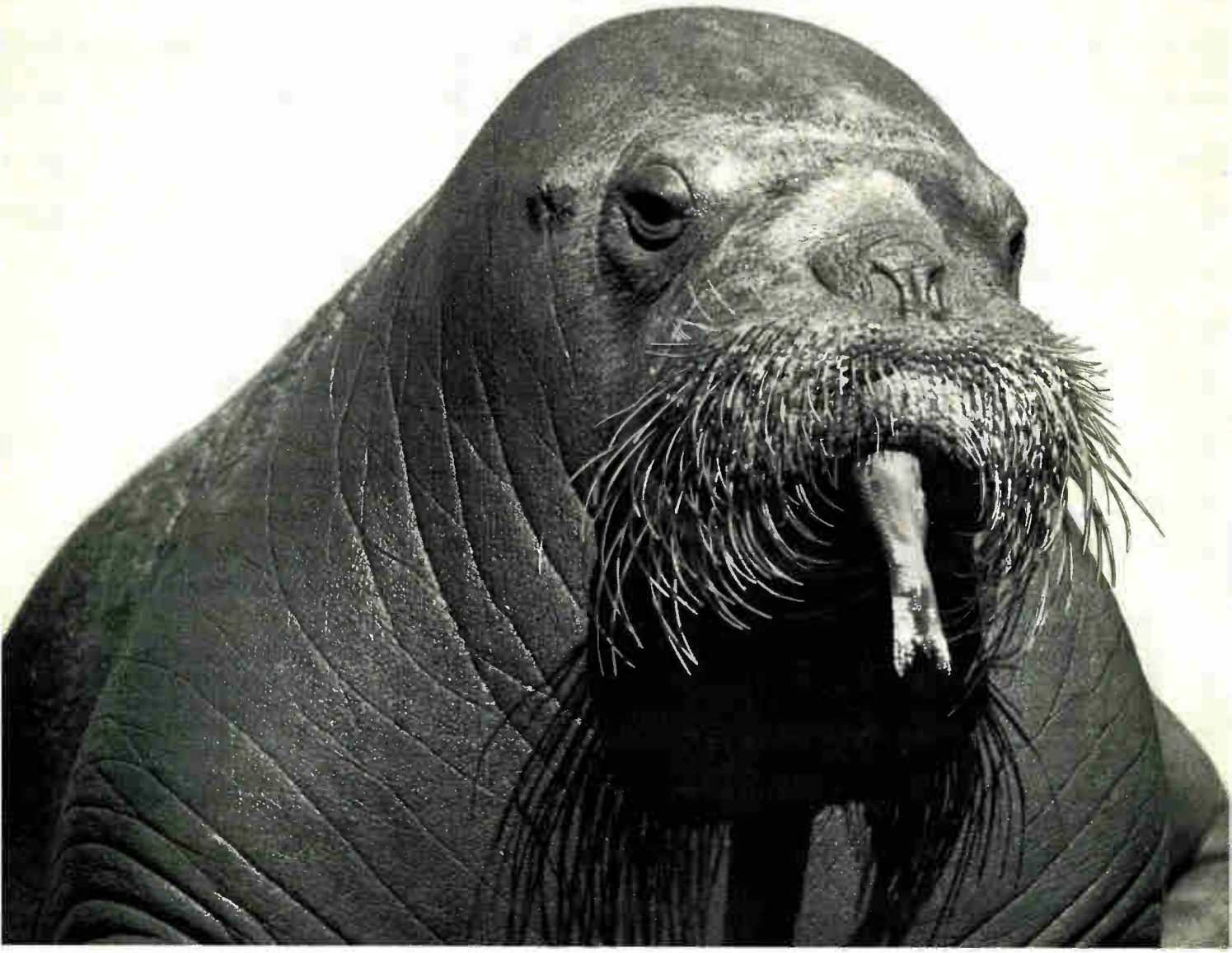
Call an Anorad Application Engineer today to discuss your individual requirement. We will consult, layout, propose, firm bid and deliver a positioning system custom engineered to your specific applications.

**ANORAD** CORPORATION
110 Oser Avenue, Hauppauge, New York 11788 (516) 231-1995 TWX: 510-227-9894

ANORAD Number 1 in precision positioning tables.

**Self-satisfied competitors may believe:**

# "Philips VMEbus offensive? We thought market shares are established."



## Philips is convinced:

market shares are not established as long as there are suppliers who claim to offer more. The background of a multi-discipline concern and large R&D resources dedicated to VMEbus are the basis for the long-term product strategy of Philips, which ensures we offer more. Let the best win!

For more informations:

Building HKF 49
5600 MD Eindhoven,
The Netherlands,
Tx: 35000 PHTC (NL)

AUSTRALIA 02-8888222
AUSTRIA 0222-629141/740
BELGIUM/LUXEMBURG 02-5256646
FRANCE 01-8301111
HONG KONG 05-283298
INDIA 022-4921500
ITALY 039-363507
NETHERLANDS 040-783076
NEW ZEALAND 09-894160
NORDIC 08-7821091 (Sweden)
PORTUGAL 01-683121
SINGAPORE 2538811
SPAIN 01-4042200
SWITZERLAND 01-4882403
U.K. 0223-358866
U.S.A./CANADA (800)-227-1817 ext. 957 d
WEST GERMANY 0211-361640

PHILIPS

**Industrial Automation**

Circle 48 on reader service card

**PHILIPS**

# HOW GENRAD'S NEW TESTER COPES WITH VHSIC CHIPS

## IT WILL HANDLE CHIPS WITH UP TO 288 PINS AT A 120-MHZ CLOCK RATE

The Very High Speed Integrated Circuits program presents some uncommonly difficult challenges to test equipment. These 100-MHz chips, which are being developed with 0.5-μm design rules for the Department of Defense, will be made up of more than a half million gates of random and sequential logic as well as read-only and random-access memory. All this has to be tested in one pass and in a reasonable amount of time. Another testing problem is high input/output pin count—VHSIC chips with 120 to 240 pins are now under development, and parts with even higher pin counts can be expected later.

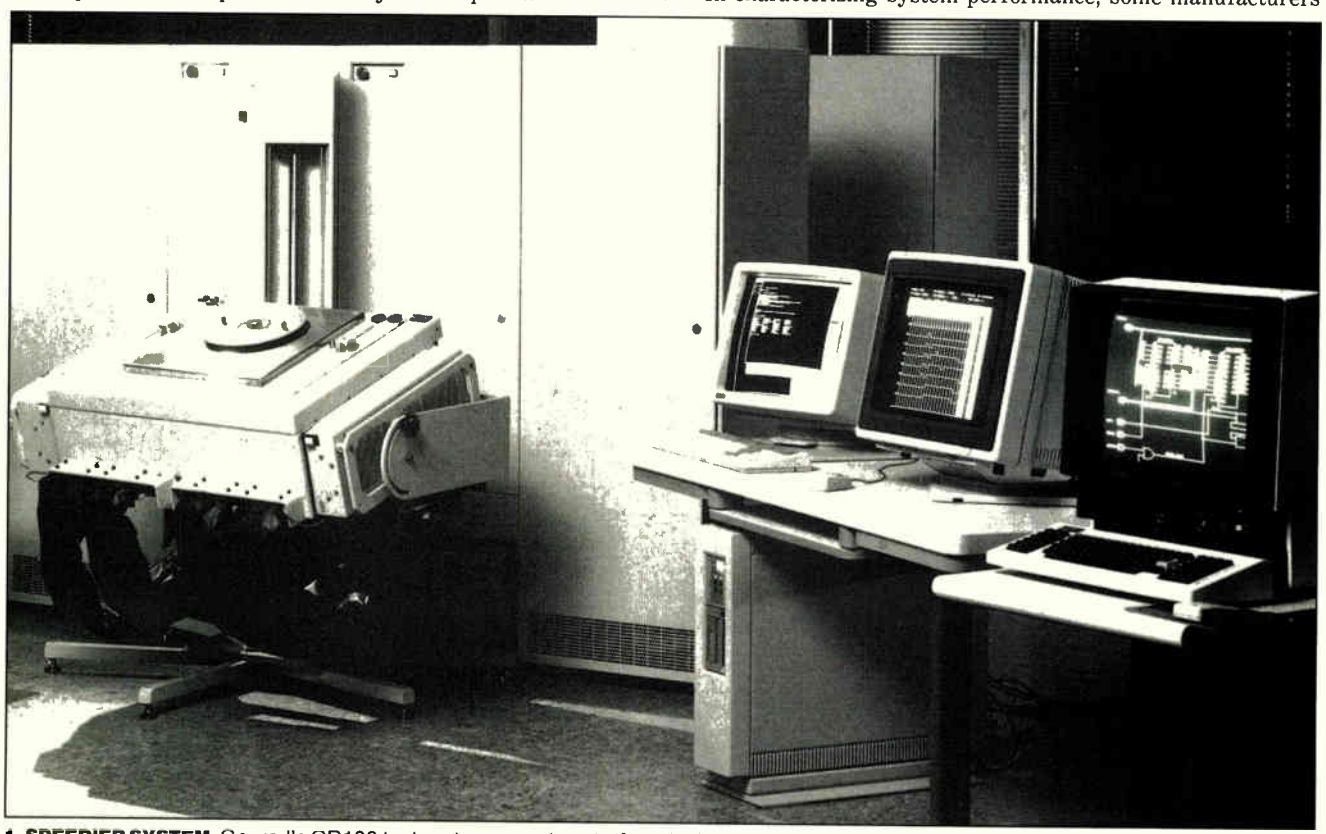
Now Genrad Semiconductor Test Inc. has come up with what it says is the answer to such a momentous challenge. The company aims to meet the demanding VHSIC requirements with its new GR180 test system (Fig. 1), which comes with a 120-MHz clock that provides the basic timing for the device under test. Up to now, 80 MHz was the fastest clock found on test systems. And the GR180's test head contains 288 test pins, twice as many as most existing testers. The tester provides a variety of input stimuli to test the different types of logic found on a VHSIC chip. And test patterns derived during chip design can be used to test sequential and random logic, while additional test-pattern generators can produce sequential address and "walking" 1 and 0 patterns for testing RAM. Prices will begin at about $950,000 for the system.

To achieve its high operating speed, the 120-MHz clock chip inside the system's test head is fabricated in gallium arsenide. "GaAs is used to meet the need for fast rise time," says Roger Ball, Genrad's director of product development operations in Milpitas, Calif. He notes that the GR180's speed is also suited to testing high-speed commercial logic chips such as the 100K emitter-coupled logic arrays supplied by Fujitsu, Motorola, and NEC. These arrays operate at clock speeds up to 100 MHz and can contain as many as 8,000 gates with over 200 I/O pins. "Some ECL devices have specifications calling for an output to occur 1.5 ns after an input," says Ball. "For a tester to confirm performance under this specification, it must be able to position its clock pulse edges very accurately."

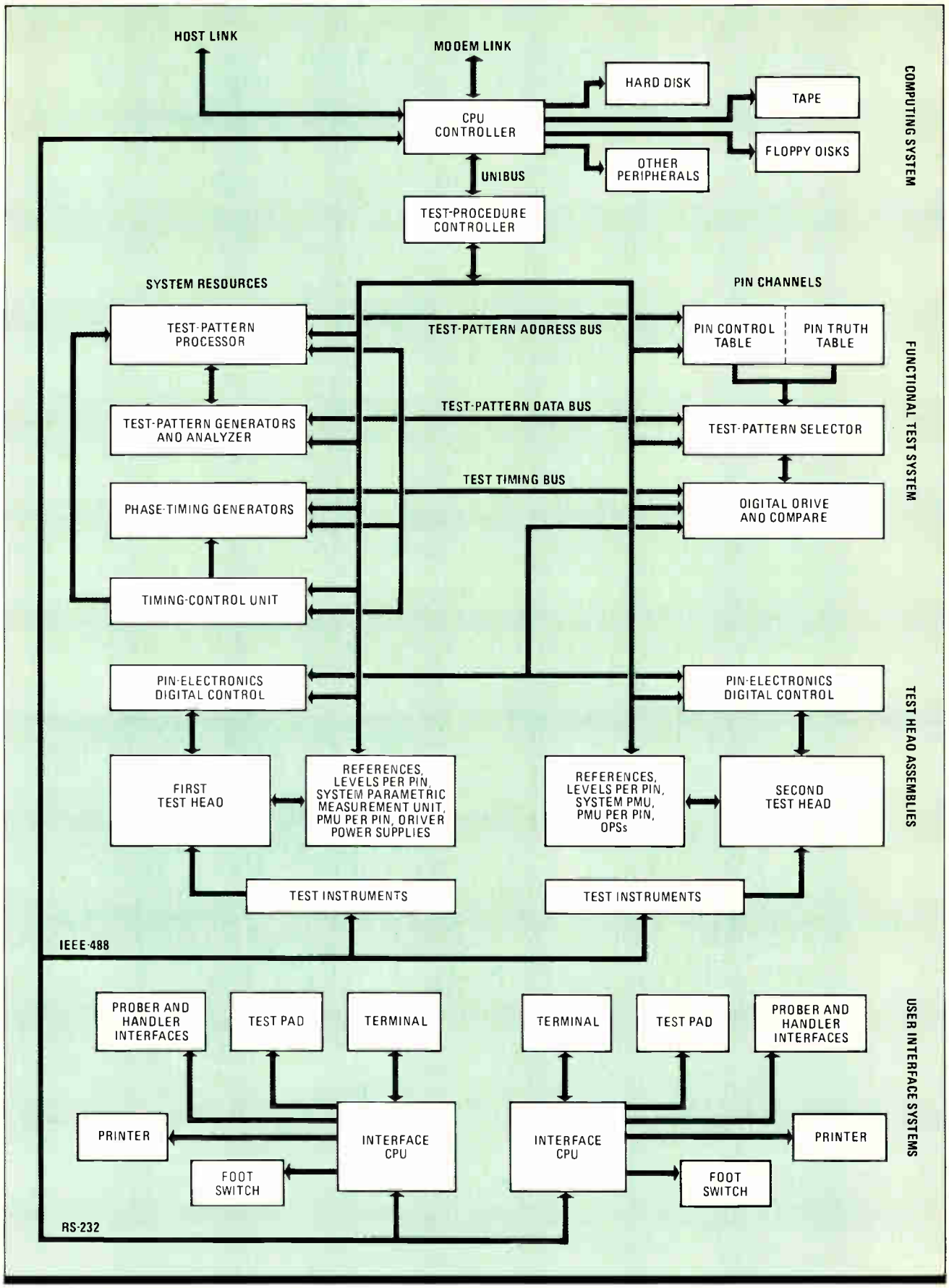
The GR180 system's accuracy is rated at 750 ps. This figure takes in three error components: pin skew on the input pins, accumulated error through the system, and pin skew on the output comparator pins. Input-driver pin skew on the Genrad system is 300 ps; skew on the output comparators is another 300 ps. The remaining 150 ps is accumulated error through the test system.

In characterizing system performance, some manufacturers

TECHNOLOGY TO WATCH *is a regular feature of* Electronics *that provides readers with exclusive, in-depth reports on important technical innovations from companies around the world. It covers significant technology, processes, and developments incorporated in major new products.*



**1. SPEEDIER SYSTEM.** Genrad's GR180 test system operates at a fast clock speed of 120 MHz and provides a variety of stimuli to test 288-pin VHSIC-class chips that contain random and sequential logic as well as on-board ROM and RAM.




**2. FUNCTIONAL ORGANIZATION.** High-speed dynamic testing in the GR180 is done by the functional test system, which has such resources as test-pattern generators and analyzers and large pin-truth-table memory for storing up to 260,000 test vectors.

use input-pin skew alone as a measure of overall system accuracy. "Accuracy is to be distinguished from pin skew," warns Ball. Skew specifies the amount of time that the leading edge of the 1 pulse on one pin can lead or lag the leading edge of any other pin receiving a 1 pulse at the same time.

The test program for the system is developed on a Digital Equipment Corp. VAX work station connected to the tester by means of an Ethernet local-area network operating with Decnet software (Fig. 2). Test programs can also be developed locally on the test system's central processing unit, a DEC PDP-11. Test vectors can also be derived from the work station used to create the VHSIC design. Currently, the GR180 can download test patterns through the Ethernet using Genrad's own Hilo logic simulator.

## WRITING TEST PATTERNS

In the past, the test patterns developed on a logic simulator to verify chip design could not be automatically transferred to engineers for production testing. The GR180 makes this transfer easy. Test programs are generally written on the VAX and transferred to the tester. Having an Ethernet network means that the tester can be linked to other VAX computers and work stations, such as those from Daisy Systems Corp. Through this connection, the simulator test-vector file derived when designing the VHSIC chips on these work stations can be accessed and routed to the test system.

In the design environment (Fig. 3), the engineer creates a circuit model on the Genrad Hilo simulator using a hardware-description language. He also specifies a set of circuit stimuli with Hilo's waveform-description language. Applying the waveform to the circuit model during simulation results in an ASCII-format data-capture file.

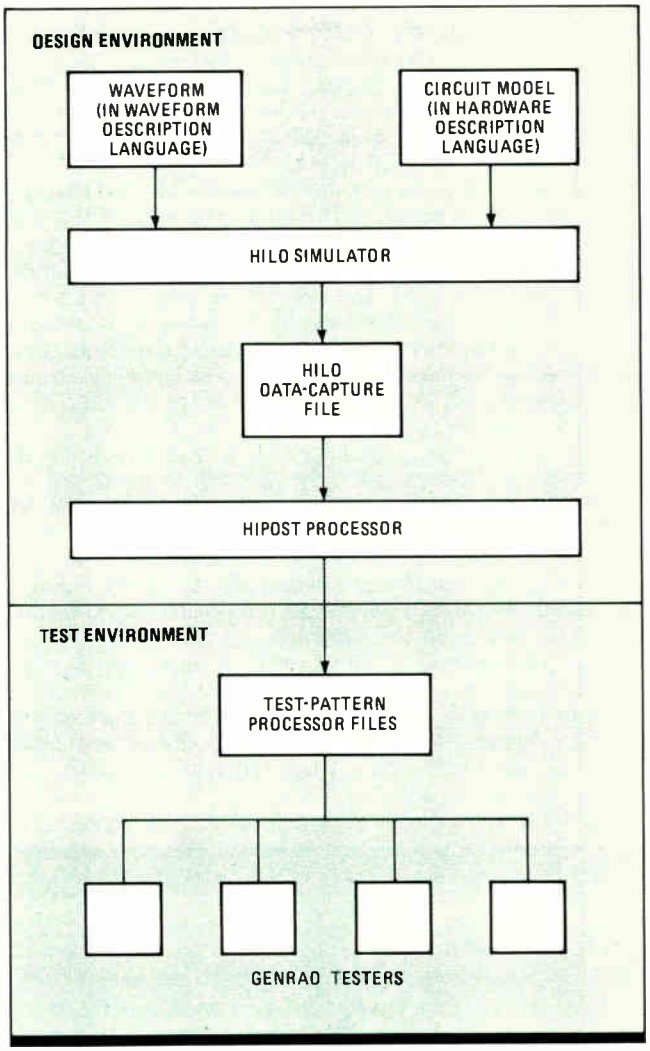
Genrad offers a postprocessor software product called Hipost that runs on the VAX work station, converting the Hilo simulator's data-capture file into the test-pattern-processor file format used by the test system. The test-pattern processor is called by the tester program to apply functional vectors to the device under test. Other versions of Hipost are available to run on a Daisy Logician or Megalogician to generate test vectors that can be transferred to the VAX work station.

Before testing begins, the test program is sent to the test-procedure controller inside the tester. A test program is loaded into the controller in its entirety. Having the test program in high-speed memory assures that no time is wasted by accessing a test pattern from a slow disk drive or other mass-storage device.

"With a capacity of 4 million 32-bit words, or 400,000 test vectors, the test-procedure controller is larger than that on Genrad's previous-generation tester, the GR18, which contains 1 million 32-bit words, or 100,000 test vectors," Ball says. "The larger number of test vectors is required because of the complexity of the VHSIC circuits to be tested." The test-procedure controller's output is sent to an ECL-compatible bus, which moves the test patterns at high speed to the pin truth table and pin control table.

The pin truth table is a sequential memory containing as many as 260,000 vectors. Test patterns from the simulator are stored here and are applied sequentially to the unit under test. The ability to store so many test patterns is an asset in testing complex chips requiring a large number of test vectors because the entire set of test patterns is loaded into memory only once. If the memory were smaller, only part of the test pattern set could be loaded and run, and afterwards the memory would have to be reloaded with the remainder. The large truth-table memory improves test throughput. A unique capability of this tester is that the fixed set of test patterns in the pin truth table can be applied to the unit under test in one part of a test run.

Smaller test patterns paged into the pin control table from the test-procedure controller can be selectively applied to the unit before or after the pin truth table patterns are applied. "Smaller sets of test patterns in the pin control table developed by the test programmer are useful, for example, in setting a device under test into some initial condition," Ball says. "When power is applied to a chip for the first time, the logic of the circuit is in some unknown state. Before testing can begin, the chip must be exercised until it reaches some known state."




**3. TWO TONGUES.** Users model a circuit with hardware-description language and specify stimuli with waveform-description language.

The pin control table loops through a given test pattern, repeatedly applying the same pattern to the device under test. At the same time, the tester's chip driver and comparison function monitors the output of the unit under test, looking for some known state to occur. Once this output state has been reached, the pin control table breaks the loop and directs the pin truth table to apply its 260,000 or so vectors to the IC.

## CHANGES ON THE FLY

Because the contents of the memory inside the pin control table are randomly addressable, the test-pattern processor can direct the pin control table to change the test flow on the fly. It might perform a test in a tight loop, jump from one set of test vectors to another, and so on. The test-pattern selector chooses which of the various test-pattern generators to use in testing a device. It can choose from the pin truth table, pin control table, or from various generators inside the test-pattern generators and analyzers.

The test-pattern generators and analyzers also contain a serial-data generator for performing level-sensitive scan-de-

sign testing, a technique developed at IBM Corp. that involves building extra registers into complex chips to aid testing. It would be impossible to test a large VHSIC chip that is filled with random logic by applying test patterns at the chip's inputs and checking response patterns at its outputs. To simplify the testing of such chips, the IC designer must break the logic into smaller discrete sections.

At the beginning and end of each discrete block, the designer inserts a shift register. The parallel output of the shift register at the beginning of the logic forms the test patterns that stimulate that section of the random logic. The stimulus pattern works its way through the random logic and is strobed in parallel to the register at the end of the logic block. The test patterns set the individual stages of the output register. Once the response to the test pattern has been strobed into the second of the two registers, it is serially shifted out to the test system for analysis.

"One of the features of the serial-data generators inside the test-pattern generators and analyzers is the ability to define a 1, 0, high-impedance state, or a 'don't care' [ignore the bit] state," Ball says. "The tester can select from any of these options on a per-pin basis at high test speed." The stimulus for each pin can be changed selectively on the fly during a test and the serial-data generators can produce a test-pattern bit stream that is up to 2 Mb long.

"The real strength of this system is that complex test-pattern switching can be done in a single pass," says Gene Roth, marketing manager at Genrad. "The designer doesn't have to generate a test pattern to test one chip function, then come out and go through a whole different test pattern for another chip function."

Usually, a tester checks ac parameters after it has tested dc parameters. To perform dc parametric tests, the GR180 has an independent set of reference supplies on each of the 288 test pins for driver voltage high, driver voltage low, comparator voltage high, comparator voltage low, load current low, load current high, load voltage switch, and parametric measurement unit.

The test head's parametric measurement unit can be connected to a pin to force a value on the pin to make a measurement. The unit checks such characteristics as input-pin leakage and output level on each pin.

Other systems have a parametric go/no-go test per pin and establish a reference voltage level against which they grade the pin voltage on a pass/fail basis. This type of system does not provide absolute pin voltage values, a useful capability for characterizing VLSI chips. The Genrad system does. Having independent supplies on each pin enables the test engineer to stimulate each pin on the unit under test uniquely and concurrently. This capability is particularly useful in testing hybrid circuits, which may carry different forms of circuitry requiring varied supplies.

The 288-pin test head of the GR180 can be used as a single head or as two 144-pin heads for testing two devices concurrently. Furthermore, in the two-head configuration, the system can perform a high-speed dynamic test on one head, while running a static dc parametric test on the other—an effective way of increasing throughput.

"We have also provided a number of interfaces for the tester," says Roth. "There is a new GP300 test-head interface that provides interfaces to probers with a 300-pin probe card and to handlers." Unique in this interface is the ability to mate with a prober with a 300-pin probe card; it was not possible to match an overhead prober previously. □

## VHSIC TESTER TOOK MAINFRAME AND MARKETING SAVVY

**In late 1984,** Roger Ball left Manchester in his native England for Milpitas, Calif. About the same time, Gene Roth was preparing to leave the outskirts of Boston for the same destination. Both men were off to begin work on Genrad Semiconductor Test Inc.'s next-generation very large-scale-integration test-system family, the high end of which would become the GR180.

"I came to California to take on strategic planning, market research, and product specification," Roth says. A designer turned marketer, he spent 12 years in engineering before taking an MBA. Ball, a graduate of Cambridge University with an MA in mechanical and electrical engineering, became engineering director.

Genrad saw a need for a VHSIC tester in three areas. One is in the manufacture of military and aerospace systems. A second market is systems integrators, the buyers of these chips. A third takes in captive operations making high-speed, high pin-count chips.

"My research showed there was a market for high-performance testers among captive semiconductor manufacturers," Roth says. "They set up the operation because they can't find the technology in the open market or there is something proprietary about a design that must be kept inside the company to retain a competitive advantage."

Genrad's work for the Very High Speed Integrated Circuits program was well under way when Ball arrived. He began looking at ways to incorporate the technology into a commercial product. Ball was an obvious choice to head the engineering effort. He spent a total of 16 years with International Computers Ltd., where he was design manager of the company's 2980 large mainframe developments. "That's where I got my experience on dealing with large amounts of logic," he says. "Built out of emitter-coupled logic, the 2980 had 400 different board types. I learned to deal with problems in large testers."

Ball left ICL to cofound Cirrus Designs, a consulting company that did applications for board testing, board test programs, and related work. Cirrus did some design work for Genrad and built the test-pattern processor in Genrad's first chip testers. "The test-pattern processor was credited with taking the test system from 30 to 40 MHz," Ball says.

"We also designed one of the pattern generators and serial-data generators in the first-generation test system." In 1983, Cirrus became a wholly owned subsidiary of Genrad and Ball has the job of coordinating the developments in the UK.

When Ball isn't working, he can be found skiing and swimming—two pastimes he has acquired since moving to California. His one regret is that he no longer frequents the theater. "In Manchester, we had three good theaters, all within 25 minutes of where we lived," he says. "I've not gotten around to finding the theaters in this area."

Gene Roth has no regrets about moving. In his spare time he does woodworking, and he is an avid jogger and tennis player. But his special passion is boating.

**TEST MARKET.** Gene Roth (left) identified the GR180's audience and Roger Ball delivered the goods.

# Guess Who's Backing Engineers with Free Power Discretes?

Most suppliers sell their power discretes. SGS is willing to give them away to prove a point: We're not just one of the biggest suppliers of power devices, we're the friendliest.

We mean business. Just send us your card and a note explaining how your company uses power discretes. If you qualify, we'll send you a free $100-value 9-drawer Power Pak case containing 60 of the industry's most popular power discretes.

Better hurry! We've got thousands of Power Paks, but they'll go fast.

Pre-qual programs, indepth tech notes, nationwide distributors and Reps, free power discretes -- SGS is backing engineers with everything it takes to make your job easier. That's why we're known as The Friendly Power.

The Friendly Power™

SGS®

FREE

**SGS SEMICONDUCTOR CORPORATION**
1000 East Bell Road, Phoenix, AZ 85022 (602) 867-6100

_____ Send me your Free Power Pak Sample Case, plus technical info. I have enclosed my business card and a note explaining how I use power devices.

_____ Have a Friendly Power Rep call.

Name _____

Title _____ Phone _____

Company _____

Address _____

City _____ State _____ Zip _____

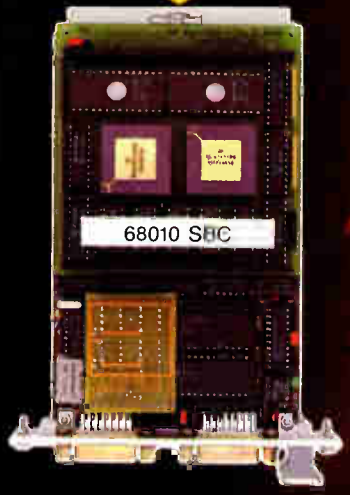
5/19/86

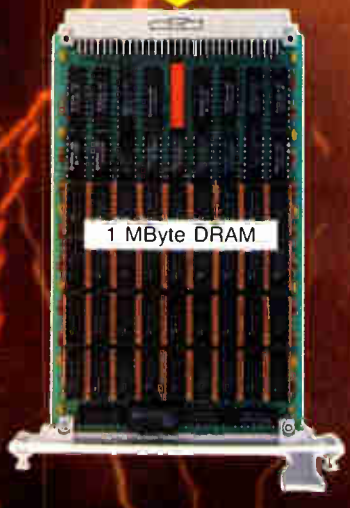
# How we tailor VMEbus solutions to your industrial applications

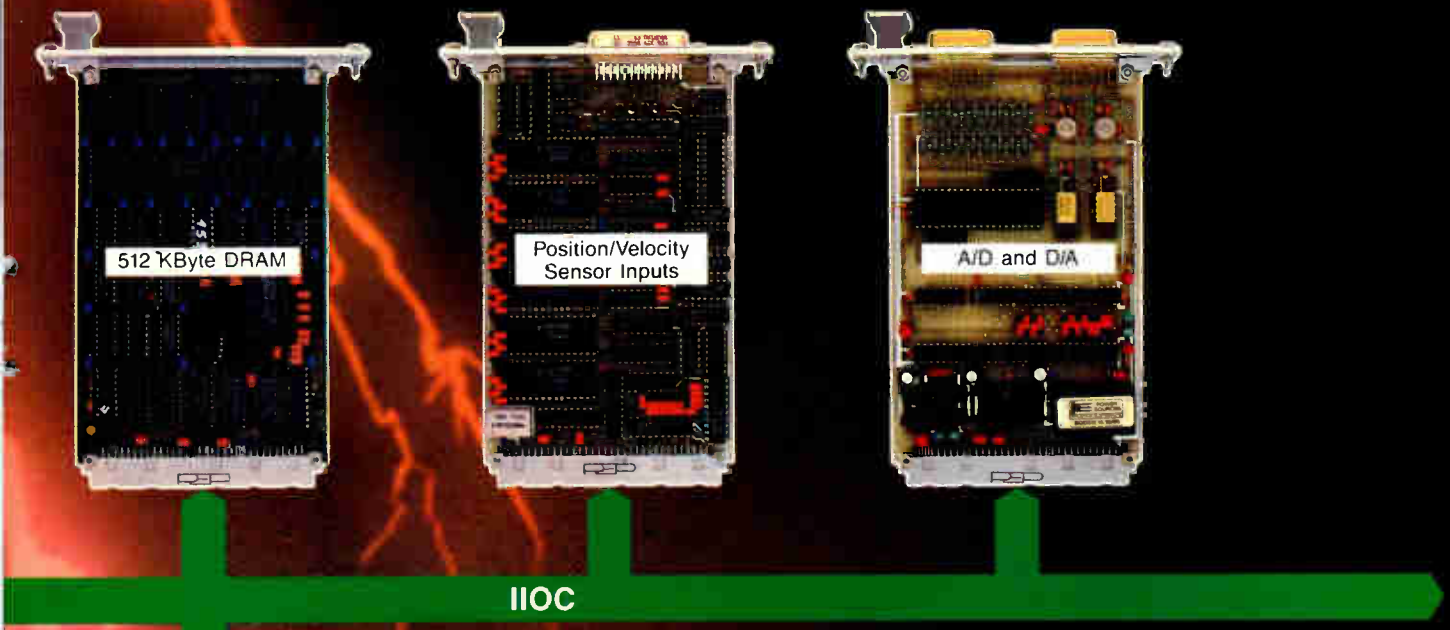

## VMEbus and Intelligent I/O Channel...

With the VMEbus finding overwhelming acceptance worldwide, PEP is now enhancing VMEbus versatility with the Intelligent I/O Channel (IIOC). The IIOC provides you with lower cost interface modules typically used in industrial applications. It can also be furnished with its own CPU which can execute tasks locally, offloading the VMEbus master CPU. The IIOC can also be used stand alone. With or without CPU, the IIOC is accessed transparently (as a 64 Kbyte memory mapped space), eliminating the need for complex multiprocessor operating systems. Furthermore, there is no limitation in the number of IIOC's on the VMEbus other than for physical space.


**VMEbus**





## . . . all in Single Height format

PEP delivers both VMEbus and VME Related Products on the IIOC modules in a consistent, single height format. This gives you the physical and functional configuration flexibility ideally suited for industrial applications. In addition, single height modules are more reliable in harsh environments because of greater resistance to vibration, torsion and shock.

PEP Modular Computers, Inc., 600 North Bell Avenue, Pittsburgh, PA 15106
Phone: (412) 279-6661, (Tollfree): 1-800-228-1737 (outside PA),
1-800-255-1737 (inside PA), Telex 6711521, Telefax 412-279-6860

PEP Elektronik Systeme GmbH, Am Klosterwald 4, D-8950 Kaufbeuren
Phone: (08341) 8974, Telex 541233, Telefax (08341) 4022

**Modular Computers®**

Circle 55 on reader service card

# Harris technology explodes inflated boards.

## Low-cost, space-saving, channel selectable op amps simplify system designs.

In analog design, the goal is not bigger boards but better ones. And nothing accomplishes this goal like Harris channel selectable op amps.

The HA-2400 family combines the functions of an analog multiplexer and a high-performance quad op amp on one chip. Each device features four op amp inputs which can be individually connected to one output stage.

The result: improved system reliability, uncommon design versatility and dramatic savings in board space, design time and system costs.

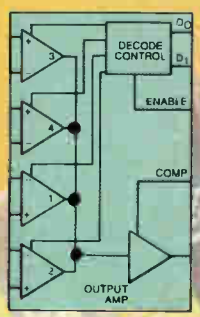
The 2400 family utilizes our proven Dielectric Isolation technology to deliver some impressive specs:

- 30 V/$\mu$s slew rate
- 40 MHz gain bandwidth product
- 110 dB crosstalk rejection
- Digital channel selection - TTL compatible

The HA-2400 family is available in military (HA-2400), industrial (HA-2404), and commercial grades (HA-2405 and HA-2406). The new HA-2406 features the lowest cost. Use them to select and condition different input signals. Or choose different op amp functions to be performed on a single input signal.

That design versatility makes these devices the perfect low-cost components in literally thousands of applications — from missile guidance, communications and avionics, to industrial process controls, test equipment and computer peripherals.

For all the details, call 1-800-4-HARRIS, Ext. 1724 (in Canada, 1-800-344-2444, Ext. 1724). Or write: Harris Semiconductor Products Division, P.O. Box 883, MS 53-035, Melbourne, Florida 32902-0883.




HARRIS

Harris Semiconductor: Analog - CMOS Digital
Gallium Arsenide - Semicustom - Custom - Hybrids

# For your information, our name is Harris.

Circle 56 on reader service card

# INTEL DESIGNS A GRAPHICS CHIP FOR BOTH CAD AND BUSINESS USE

## LOOSELY COUPLED PARALLEL ARCHITECTURE IS KEY TO PERFORMANCE

Two completely different kinds of end customers seem to be fueling the embryonic graphics chip market: the personal computer user in business, who primarily is interested in manipulating text but wants to include more sophisticated graphics, and the designer on a work station, who demands more sophisticated graphics but increasingly wants text-handling capabilities. Intel Corp., long reported to be developing a graphics-oriented microprocessor, is finally announcing its 82786 graphics coprocessor for both applications. It tailored its graphics chip to meet most needs of both the computer-aided-design market as well as of the business and high-end personal computer markets.

The requirements of the two markets are not that different, according to Mark Olson, Intel's product manager. "Both require the ability to perform high-quality graphics and text chores as well as the ability to merge the two in the same display," he says. "And both applications require a high degree of multitasking—the ability to perform two or more complex tasks at the same time and to shift back and forth between them virtually simultaneously."

Users in both markets are also demanding productivity, he says. "What this translates to in the real world of business and engineering is, no waiting." To meet these requirements, Intel designed the 82786 with a loosely coupled parallel architecture that combines flexibility with high speed and sophisticated graphics manipulation as well as powerful text-processing capabilities.

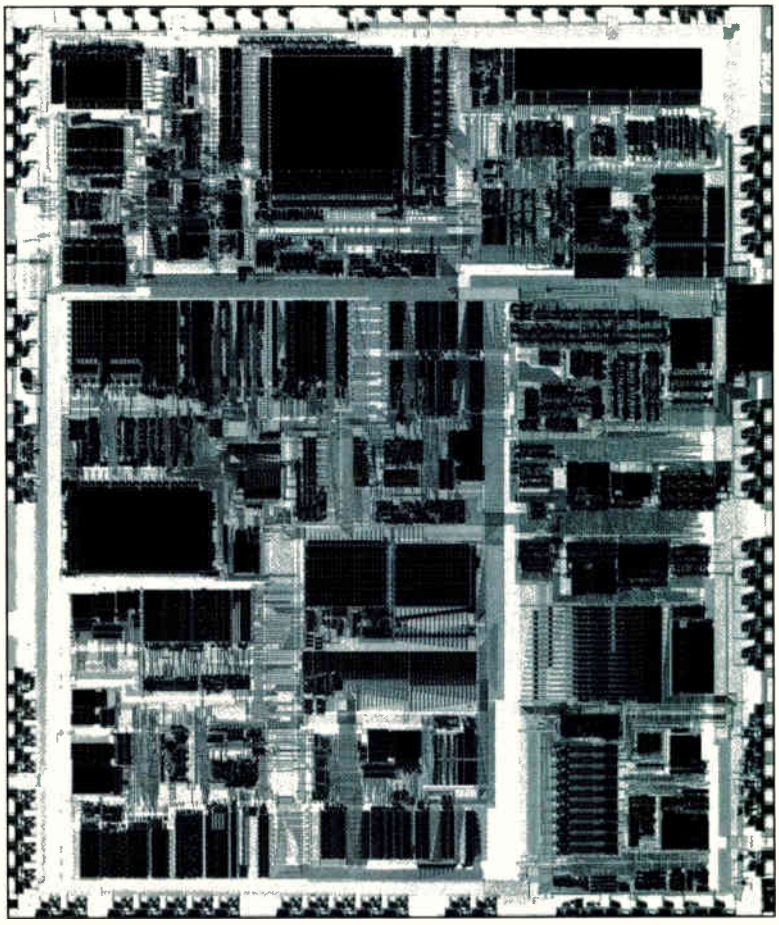
The 82786 is flexible enough to let a designer choose from a wide range of system central processing units—from the 16-bit 8086 to the 32-bit 80386—as well as graphics memories and displays, depending on the cost and performance requirements of the application. And it is designed to run applications based on the American National Standards Institute's Video Device Interface and Graphics Kernel System, as well as those written for the de facto standard IBM Corp. Color Graphics Adapter for the Personal Computer. Such programs can be run simultaneously, each displayed within its own window on the same screen.

Its performance is equally impressive. The 82786 offers almost instantaneous screen updates. It can draw single-window screens in less than 0.1 second, or 400 ns per pixel. The 82786 can draw all the standard primitives—lines, circles, polylines, polygons, and others—at extremely high rates: lines take 2.5 million pixels per second, circles 2 million pixels/s at 8 bits per pixel. As a text processor, it can simultaneously support multiple character sets and create text at a nominal rate of 25,000 characters per second.

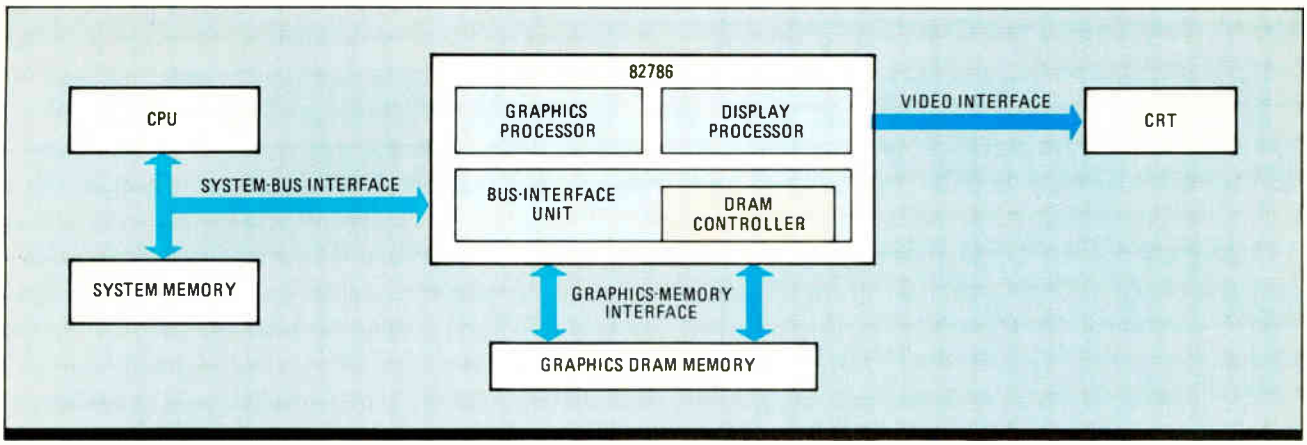
Fabricated using the company's 1.5-$\mu$m CHMOS-III process, the graphics chip (Fig. 1) uses either standard dynamic random-access memories for medium-performance, lower-cost applications, or video RAMs for high-resolution systems. It supports display resolution of 640 by 480 pixels using ordinary memories, as well as up to 256 colors for illustration. For dedicated document creation, the 82786 also supports 1,000-by-1,000-pixel monochrome systems with four gray scales, or colors for denser pages. When the 82786 is used with dual-port VRAMs and high-resolution displays, resolution can reach 2,048 by 1,536 pixels with 8 bits per pixel. Higher resolutions and more colors can be achieved by using multiple 82786s.

Demand for multiple-windowing capability is on the rise, especially for multitasking chores in the office environment. The 82786 implements this capability in hardware. Each application can have its text and graphics drawn into separate regions of memory, which are then combined within windows of the same display. Large amounts of overhead associated with graphics tasks can be offloaded from the main system CPU by storing more text and graphics information in memory than is shown in the display.

The 82786 achieves this performance through a loosely coupled architecture consisting of four independent modules (Fig. 2) organized to operate in parallel: a graphics processor, a display processor module, a bus-interface unit, and a DRAM controller. Applications programs use the graphics processor to draw bit maps that create objects in memory. The window-



**1. GRAPHICS COPROCESSOR.** Intel's 82786 graphics coprocessor supports its family of 16- and 32-bit central processing units.




**2. PARALLEL PROCESSOR.** In Intel's 82786, four modules—graphics, display, bus-interface, and memory-control—operate in parallel.

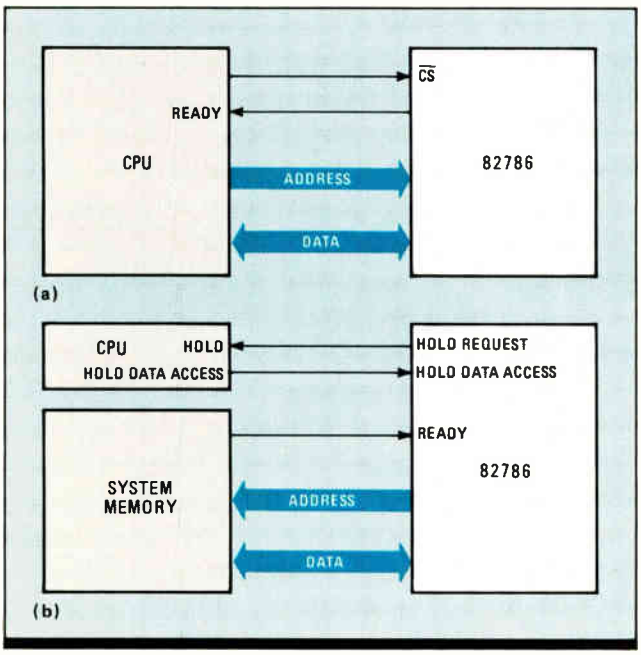
manager software uses the display processor to control display contents. The bus interface and DRAM control modules are invisible to the CPU software after initialization. These two modules permit parallel processing of simultaneous tasks for graphics functions.

New graphics may be drawn into memory at the same time that existing portions of memory are being displayed on a monitor. This separation of functions is what makes possible the high performance of the 82786.

## ASYNCHRONOUS COMMUNICATION

The modules communicate over a built-in asynchronous bus. When the graphics processor module receives a list of commands from the CPU, it sequentially executes them and draws into one or more bit maps, regardless of what is currently being displayed on the screen. The bus-interface unit arbitrates graphics-memory requests to maintain the integrity of the display contents. The DRAM control module directly handles up to 4 megabytes of graphics memory while providing full refresh. Virtually any size or configuration of DRAM, either standard or video and up to 1 Mb, is supported. Static column and fast page modes are directly supported for serial access of memory blocks.

The most common configuration allows the CPU access to the system while the 82786 accesses its dedicated graphics memory. The CPU can also access graphics memory and the 82786 can access the system memory, although not at the same time. If direct memory access is also provided in the system, it interfaces to the 82786 exactly as the CPU does.




**3. SLAVE OR MASTER.** The graphics coprocessor can work with Intel 16- and 32-bit microprocessors in either slave (a) or master (b) modes.

The 82786 works with the CPU in two ways. In the slave mode—that is, when the CPU accesses the 82786—the graphics chip looks to the CPU like an intelligent DRAM controller (Fig. 3a). The CPU generates a chip-select signal, which the 82786 acknowledges when the cycle is complete by generating a Ready signal to the CPU. In the master mode (Fig. 3b), the 82786 looks like a second CPU controlling the local bus. When the CPU receives a signal from the 82786 to request control of the system bus, the graphics coprocessor takes over the bus. When it is finished, it sends a signal to the CPU, which takes back control of the bus.

## FLEXIBLE GRAPHICS PROCESSING

The graphics processor module is powerful enough to handle a wide range of tasks. It accepts commands that allow it to maintain multiple bit maps in memory, to draw the text and graphics objects, to copy images from one piece of memory to another, and to fill the objects. The programming interface supports subroutines and the use of a stack for nesting these subroutines. Registers can be dumped to and reloaded from memory to allow switching between applications tasks. Applications need only assign as much memory to a bit map as is necessary for color support because bit maps do not all need to have the same bit-per-pixel depth.

Key to its power and flexibility is a set of on-chip graphics-oriented commands for primitives—including point, line, polyline, polygon, rectangle, circle, and arc—to relieve the CPU of the chore of creating these figures from scratch. To be displayed on the screen, each figure requires only a single 16-bit request from the CPU incorporating the unique parameters of the graphics primitive, as well as one point of reference, called the current drawing point, to be used as the starting point. For example, a circle's critical parameter is the radius, and a rectangle's the diagonally opposite point. With these two reference points, the graphics processor is intelligent enough to complete the drawing.

For more specialized drawing functions, the graphics processor also includes such commands as Bit-Block Transfer, Incremental Point, and Fill. When the CPU requests it, the 82786 can perform a bit-block transfer (Fig. 4) from one portion of a bit map to another, either within the same bit map or in another bit map, at a rate of 24 Mb/s. Using the Bit-Block Transfer mode, pictures can be composed quickly on the screen by copying portions of those figures currently resident in the display's bit-map memory, including other portions of the picture currently being composed.

An Incremental Point command can draw virtually any complex figure, such as a logo, for example. In such an operation, the pixels to be drawn are listed as displacements in the X and Y directions. On receiving an incremental-point list from the CPU describing the figure's shape, the graphics processor module draws the figure at a rate of 2 million pixels/s, taking into account all currently active drawing attributes such as the texture, bits per pixel, and masking of bits.

## GRAPHICS MODES

The 82786 hardware incorporates a number of graphics modes that other graphics processors usually handle in software. These include clipping, a pick mode to support mouse operations, bit-plane masking, logical operations, and virtually unlimited character-set support.

With the clipping mode, the 82786 can draw partial sections of complete figures such as lines, circles, and more complex objects without generating all of the pixels needed for the complete figure. During execution of drawing commands by the graphics processor module, the CPU calculates addresses of all the pixels to be altered that fall within an area called the clipping rectangle.

To pick an object on the screen with the mouse, the graphics processor module is given a command list to execute, which describes the same picture as that on the screen. The graphics processor goes through the calculations for the drawing, but does not update any of the pixels. Instead, it generates an interrupt if any attempt to select a particular object is made within the currently defined clipping rectangle. This mode reduces considerably the CPU overhead spent on picking up or selecting objects on the screen because the 82786 does all the processing and the CPU is interrupted only when the picked object is identified.

At the same time that the 82786's graphics processor module performs bit-block transfers, it can do such on-the-fly operations as bit-plane masking and logical operations. The first allows copying of the original picture into only selected bit planes without touching others. It can also write text with special fonts, where the writing involves doing bit-block transfers from the location where the character font is stored to the writing location.

Logical operations permit figures to be copied in a bit-complemented mode—that is, if a figure is displayed in a white-on-black background, logical operations allow the figure to be copied in the reverse video, black on white. Using the Fill command, the 82786's graphics processor module can fill in any shape with horizontal lines. The figure's shape is given as a set of parameters, each specifying the beginning point on the X axis and the fill length on the Y axis.

The 82786 supports an unlimited range of character sets, all stored in the display RAM. The number is determined by the amount of memory, and any set can be activated by a single command. Proportional spacing is built into each character set, with the height and width of each character defined independently from 1 to 16 pixels. Not only can the spacing between characters vary, it can also be negative—that is, characters can be positioned to overlap one another, useful for effects such as kerning, that is, squeezing or stretching character spacing.

To manage the screen contents—particularly the tricky task of windowing—Intel designers built a display processor module into the 82786. The module is designed to operate independently of the graphics processor module. The display processor gets its commands from the CPU and has no knowledge of what the graphics processor is drawing.

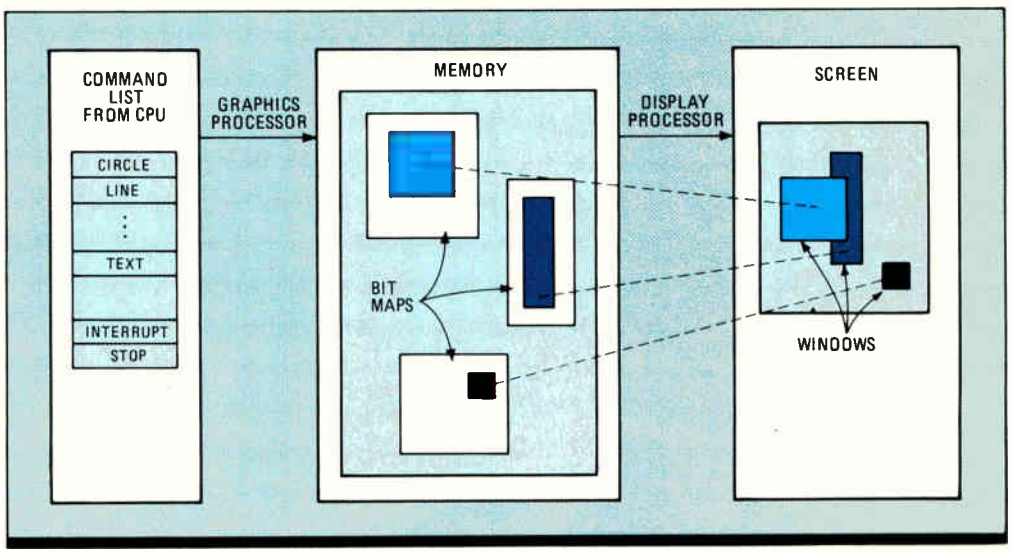
The display processor uses its instruction list to retrieve pixel information from multiple bit maps in memory and place the contents at precise screen locations. Bit maps that contain fewer than 8 bits per pixel are automatically padded to achieve full color. The display processor adds a hardware cursor, zooms the indicated bit-map contents, and provides colored borders around the windows. This produces rapid display changes with minimum system overhead because the windows can be moved a pixel at a time; all the CPU does is manipulate pointers within the instruction list in memory.

The display processor module can create an almost unlimited number of windows on the screen. It works from a configuration list supplied by the main CPU specifying the window map for the screen and what portions of which bit maps are to be shown in each window. The module then constructs the windows for every frame during the scan operation. This is done in real time, giving the illusion of moving windows and allowing the contents of any window to be panned or scrolled in any direction.

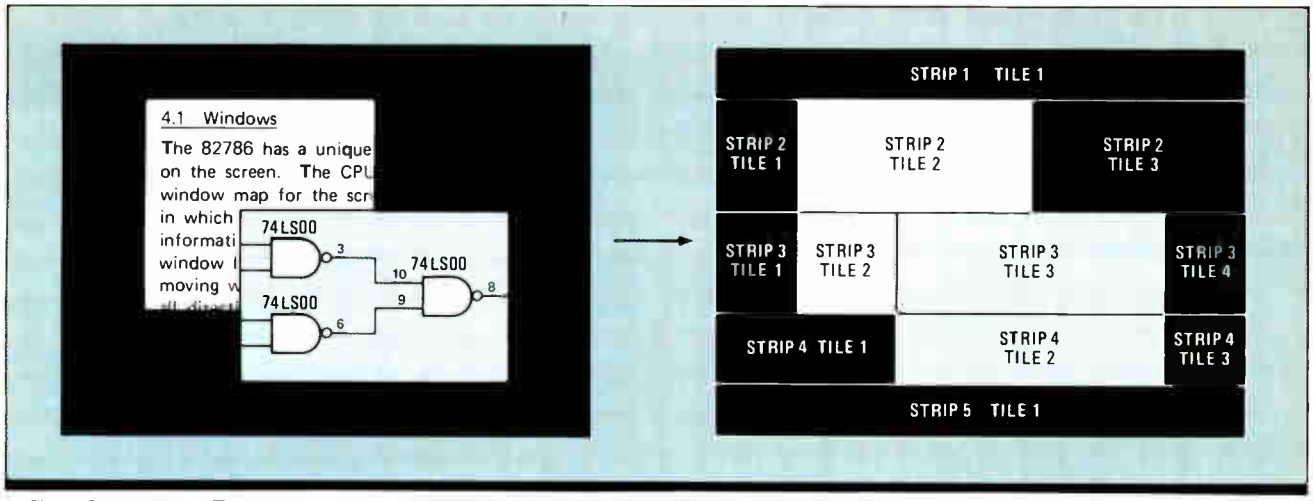
## STRIPS AND TILES

To do this, the display processor module divides the screen into strips and tiles (Fig. 5). Each strip is divided into one or more tiles, dividing the screen into a mosaic of tiles, with each window a collection of tiles. For a given screen, the main CPU provides a screen descriptor list to the 82786's display processor. This consists of a set of strip descriptors specifying the number of scan lines and the number of tiles in each strip, and a set of tile descriptors specifying the width, contents, and attributes associated with the objects being displayed.

Screens are constructed in real time, without the delay usually involved in reading out the contents of a bit map located in memory and reproducing it on the screen. It does this by reading the strip and tile descriptors and filling an on-chip first-in first-out cache with pixel data from the bit maps in the tile descriptors. The FIFO cache is then emptied onto the video screen. The contents of up to 16 tile descriptors can be cached on the chip. As a result, when it is necessary to move a window or windows or to scroll the contents of a




**4. INDEPENDENT MODULES.** Operating independently, 82786 graphics and display modules manage bit maps and windows on screen as commanded by the CPU.




**5. STRIPS AND TILES.** The 82786 handles an unlimited number of windows by manipulating a mosaic of strips and tiles as directed by the CPU.

window, only the strip and tile descriptors need to be changed; the bit-map contents need not be touched.

Speed and performance of the 82786 also derive from the integration of all the DRAM control logic to handle either standard or video DRAMs. By incorporating this function on chip, says Olson, no cycles are lost between the various subunits, and very fast read-modify-write cycles are possible for pixel writing, eliminating the need for two separate cycles for read and write. In the standard configuration, the chip can control up to 32 DRAMs directly. "Even the damping resistors normally needed to suppress ringing are integrated," says Olson. In the full configuration, the DRAMs are organized in four rows and two ranks.

When higher performance is required, the 82786 can support video RAMs, which are DRAMs with an extra serial port through which an entire row of the DRAM can be shifted in or out. While a row is being shifted out, the VRAM is accessible through the parallel port. Although more expensive than the standard page-mode or static-column DRAMs, VRAMs provide several advantages to the 82786.

"First, since the data to the monitor goes directly from the serial port of the VRAM, the display-processing module doesn't use any memory bandwidth," Olson says. "This means that almost 100% of the memory bandwidth is available to the graphics-processing module, giving it much more time to draw, and resulting in faster speeds." Second, much higher resolutions are possible. For example, using thirty-two 64-K-by-4-bit VRAMs results in a resolution of 2,000 by 2,000 pixels at 2 bits per pixel or 1,000 by 1,000 pixels at 8 bits per pixel. □

## INTEL'S FLOATING CRAP GAME

**The design effort** involved in the development of Intel Corp.'s 82786 graphics coprocessor resembled a floating crap game in which one or two main players stay in the game continuously, joined at various times by other participants who come and go as the rules and the goals change.

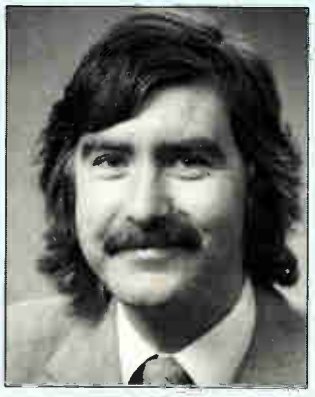
The two main players were 29-year-old Martin Randall, design manager for Intel's next-generation graphics products group, and 30-year-old Richard Hansen, project manager for the 82786. Randall, with a BSc from the University of Southampton in England, was principal architect and design engineer of the 82786. Hansen, who graduated from the State University of New York at Stony Brook with a BSEE, was principal architect of the bus-interface unit on the chip.

In addition to Randall and Hansen, working on the project at any one time was a revolving group of 5 to 10 engineers whose mix of disciplines changed as the product moved through the various stages of development.

According to Randall, the flexibility and free-form nature of the team reflected the basic architecture of the internal bus, which was designed to allow various functions to be loosely coupled, just as it allows the modules to operate independently.

"Once we had defined the overall structure of the device," says Randall, "the features we wanted and how to partition the functions, all that was necessary was to assign design teams to each module and send them on their way, without worrying about how it would interconnect with the other modules."

**RICHARD HANSEN**



**MARTIN RANDALL**

As the interface between the various groups, Randall and Hansen ensured that each of the modules met the handshaking protocols for the internal bus.

In addition to the architecture, Randall claims that the 82786 incorporates several conceptual breakthroughs. One is in the way it handles windows. Rather than use frame-buffer logic, the 82786 uses a display processor to manage the windows. Another is an internal programmable prioritization scheme that allows the system designer to rearrange the communications-processing priorities of the modules to optimize the chip for an application.

Although Intel is marketing the 82786 mainly as a sophisticated graphics coprocessor for use with its 16- and 32-bit central processing units, Randall claims it can be adapted easily to work with the company's 8-bit designs as well. "The resolution may not be anything to write home about compared to a high-end system, but it sure can do windows."

# NCR AIMS ITS GRAPHICS CHIPS AT PC INSTEAD OF WORK STATION

## COST OF MANUFACTURE IS DRIVING FORCE BEHIND 3.75-MIPS CHIP SET

Most graphics controllers and processors have been aimed at the high-performance—and higher-cost—business and engineering work-station end of the market. But NCR Corp. figured that the vast middle ground, the lower-cost but higher-volume personal computer market, was ready for a sophisticated graphics processor that could meet the market's demands at a reasonable cost. The vehicle for its strategy is a two-chip graphics-controller set—the NCR 7300 color graphics controller and 7301 memory interface controller.

"The trend in graphics is to load more and more software into hardware," says Alan Loftus, director of logic products at NCR's Microelectronics Division in Colorado Springs. "The more you can make chip-resident, the more powerful the controller or processor will be and the faster it will work. But it must be implemented with ultimate costs in mind." The company's solution was a two-chip implementation with a parallel architecture that handles color, windowing, and sophisticated text handling. "A picture may be worth a thousand words, but if you don't have 10 or 20 lines of text to describe what's going on, it won't be worth anything," says Loftus.

NCR combined standard approaches to graphics implementation such as frame buffering and presenting text in a graphics representation with innovative techniques such as a dual-text mode that allows generation of standard ASCII text, a variable memory-word width, a cache-memory drawing technique, and a two-stage color-lookup table. It also based its strategy on a stricter adherence to emerging graphics standards than many graphics processors currently on the market.

The 7300/7301 graphics chip set is fabricated using a 2-μm dual polysilicon n-MOS process. Despite the conservative design rules, it operates at an impressive 3.75 million instructions per second and can drive displays at rates up to 30 MHz, and it performs bit-block screen transfers at rates up to 2 million pixels per second.

The set's parallel architecture varies memory word width as the number of supported bit planes varies. This architecture uses memory more efficiently and allows the system to be expanded and upgraded easily.

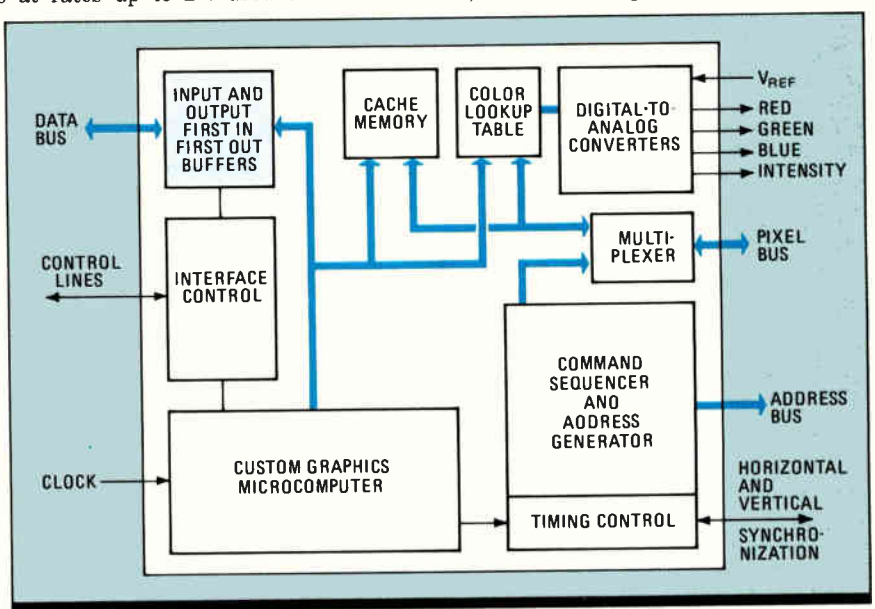
The system's variable word width and a cache-memory drawing method create high-performance graphics and the ability to use commercially available dynamic random-access memories, according to Loftus. The cache-memory drawing method uses an on-chip sequencer to refresh the display, while the drawing processor draws images to the cache memory. During display blanking intervals, the images in the cache memory are downloaded to the frame buffer. This approach draws images quickly without producing flashes on the display and allows the use of commercial DRAMs.

The 7300 color graphics controller (Fig. 1) contains a high-performance graphics processor that takes over many of the tasks usually performed by the host processor. It contains independent input and output first-in first-out registers, each 16 bits by 16 words deep. Although it has an 8-bit internal architecture, the interface logic works equally well for 8- or 16-bit processors. The FIFO registers are used for transferring commands and pixel data. The command register is utilized to specify the data bus width (8 or 16 bits), to handle resets, and to initialize handshake signals for DMA transfers. The status register holds FIFO-register status indicating when the output-FIFO register is empty. The Ready line signals input-FIFO-register status during write operations and output-FIFO-register status during reads.

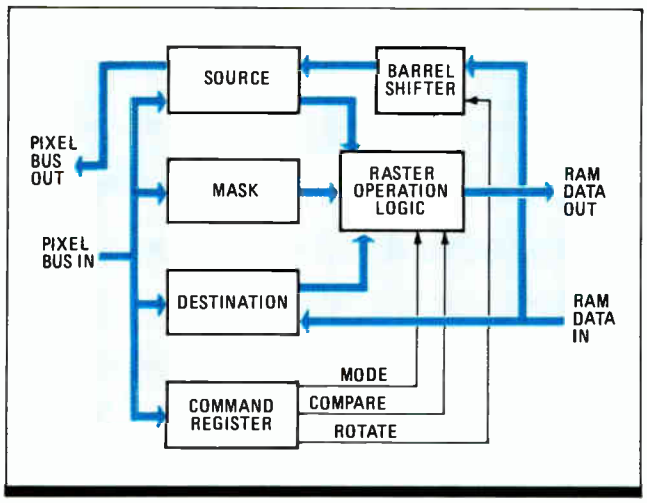
The cache memory is the key to a system that can produce video rates of up to 30 MHz while using standard commmercial DRAMs for the frame buffer. While the graphics microcomputer is drawing to the cache memory, a hardware sequencer performs the display refresh. The image in the cache is downloaded to the frame buffer. This design approach was chosen over an interleaved memory access, which would have required a higher memory bandwidth and faster, more expensive DRAMs.

A frame buffer of up to 1,024 by 1,024 pixels with 8 bits per pixel can be supported. The 7300 provides 8-bit row and column address strobes as well as read/write, $CAS_1$, and $CAS_2$ signals. The RAMs are automatically refreshed by a RAS-type refresh controller. The frame buffer uses absolute—that is, X-Y—addressing, which eliminates linear-address-to-screen-address conversions, a common technique that, however, slows the system and screen response time.

Because the 7300 can support up to 8 bits per pixel, NCR decided to divide the color lookup table into two four-bit subtables—a hue lookup table and an intensity table—for greater flexibility. Bit planes 0 to 3 are called the hue address and are used to select 16 of 4,096 hues. Bit planes 4 to 7 are the




**1. MIGHTY MIX.** The 7300 graphics controller combines a 16-bit graphics processor with cache memory, lookup tables, and logic. It performs many tasks usually done by the host.




**2. MEMORY INTERFACE.** Operating in parallel with the 7300, the 7301 memory interface circuit supervises memory-access operations.

intensity address and are used to select 16 of 32 intensity levels. When the hue data is decoded in the lookup table, one of 16 words is selected. These words are 12 bits wide and contain 4 bits each of red, green, and blue values. Each of these values is then multiplied by the intensity and converted to an analog output signal. In combination, the hue and intensity can provide 256 colors from a palette of about 60-K distinguishable colors.

## GKS COMMAND SET

Strict adherence to a graphics standard was one of the major design goals for the 7300. A high-level command language simplifies and speeds the work of the systems programmer. Adherence to a graphics standard means that subsequent design changes are much less likely to force a major rewrite of system software.

Of the various graphics standards proposed (see p. 64), the NCR designers chose the American National Standards Institute's Graphics Kernel System standard. The 7300's on-board instruction set holds 25 GKS-compatible graphics, timing, and control commands. The advantages of using a GKS-based instruction set are device-independent software and portability of software among systems that run GKS, according to Loftus. In addition, many of the functions supported by the standard adopted by IBM Corp. in its Personal Computers are directly implemented in hardware by the 7300/7301. This increases execution speed because it is not necessary to perform a software emulation of the functions.

But the main advantage, says Loftus, is reduced software-development costs. For example, if the application program is used to create slide presentations, these can be plotted using equipment from a number of manufacturers without changing any of the software. All that is needed is a device driver for the particular equipment. The 7300 driver provides immediate compatibility with a wide base of applications including those run under MS-DOS, PC-DOS, and Unix.

## TEXT HANDLER

A limitation of most existing graphics-controller and -processor chips, even some of the most advanced, has been the inability to handle text efficiently, Loftus points out. Although powerful drawing features are useful, in practice most applications for graphics systems are still very text-intensive. The 7300 was designed to facilitate this common task.

A typical solution is to use an external character generator. The 7300, however, has the on-chip capability to generate a character set and store it in a portion of the frame buffer that is not being displayed. The size of the characters—both width and height—are defined by the user, and up to 256 characters can be defined in a set. Two full character sets can be active at one time, provided sufficient memory exists in the frame buffer. The bit-mapped character images are then accessed with 8-bit codes, which eliminates the usual bottleneck of passing images between the host processor and the graphics controller every time they are needed for display.

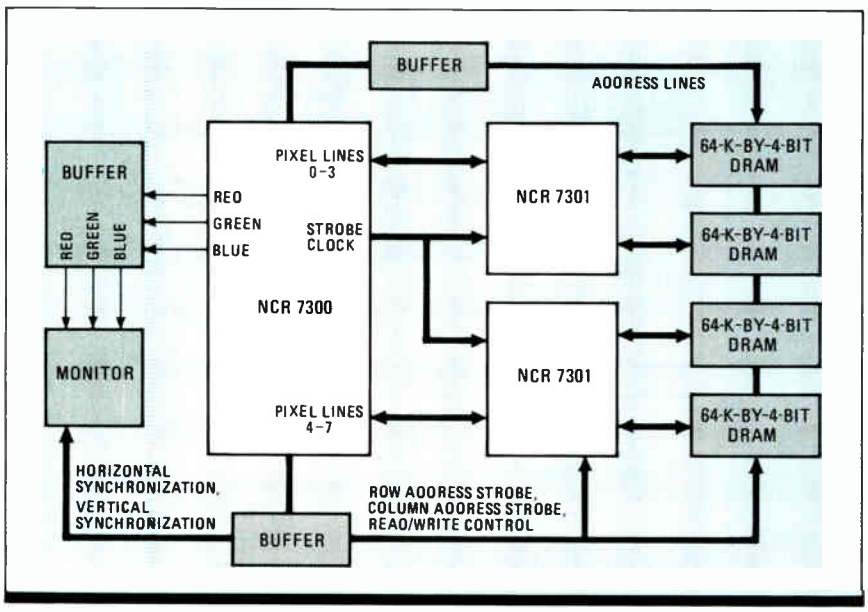
Dual text modes give the 7300 an added level of flexibility. In the Fastext mode, the 7300 generates standard ASCII-type text characters with user-selectable foreground and background colors. The graphics text mode provides proportionately spaced text drawn in any of four directions—up, down, right, or left—using a read-modify-write cycle. In this mode, the characters appear to be stenciled over the existing background.

Several text-handling features incorporated into the 7300/7301 chip set are especially useful for personal computer text-handling applications. These features are soft fonts and automatic lookup tables. The built-in soft-font capability permits the user to customize character sets by size and content and incorporate them into the text, and thus tailor the text to the application without using external character generators.

The auto lookup feature eliminates the bottleneck of passing bit-mapped images between the host and graphics processor every time a character is drawn. Instead, bit-mapped character images are stored in the frame buffer and are accessed with 8-bit codes.

The chip set allows display of up to eight full-width windows, plus viewports, says Loftus, making possible many of the window- and icon-management capabilities now done in software on most personal computers. Included in the chip's command set is a Move Viewport instruction, which allows block-copy transfers of more than 2 million pixels/s.

A feature not usually found on other graphics controllers and processors is the 7300's on-chip programmable color lookup table with overlay mode. This allows the user to display images in multicolors, or




**3. LOW CHIP COUNT.** With the 7300/7301 chip set, a 16-color display system having a 1,024- by 512-pixel frame buffer requires less than a dozen integrated circuits.

in a combination of colors and shades as the application warrants. The overlay mode provides a prioritized plane display in which images on higher-priority planes appear in front of images on lower-priority planes. Planes can be selectively written and displayed, enhancing windowing-type display formats. Animation is produced by writing different values to the lookup table.

For the display of 256 colors simultaneously from an on-chip palette of 64-K colors, the 7300 incorporates a 4-bit multiplying digital-to-analog converter with four analog outputs. An external buffer is necessary to provide isolation from the monitor's high-voltage environment and provide the TTL levels or 5-Ω drive for the monitor. Pixel rates to 30 MHz are supported, providing crisp, flicker-free displays.

The display formats and monitor timings on the 7300 are software defined, allowing the same hardware design to be used in a variety of applications. In addition, the 7300 provides a software clock option so that the graphics processor operates with a double-frequency clock for applications with a low video rate, increasing system performance.

The 7300's dual independent 16-bit-wide, 16-word-deep input and output FIFO registers provide an asynchronous interface to 8- and 16-bit processors. The 7300 occupies two locations within the host processor's address space. One location is used to read and write from the FIFO registers, the other is used to read the status register and to write to the command register. Handshake signals are provided for DMA transfers and a ready line can be used to insert wait states during I/O operations.

Though the NCR team managed to incorporate an impressive number of features on the color graphics controller, it faced a critical decision over the memory function. According to Loftus, system-cost and cost/performance considerations, rather than high density and high performance for their own sakes, dictated the development of a separate memory-interface controller. "Similar functions could have been achieved using TTL shift registers and associated glue logic, but the result would have been lower performance and higher cost," he says. "On the other hand, integrating the two circuits into one would have also increased performance, but only at the cost of going to a higher-density and higher-cost process."

The memory-interface controller is designed to serve as a master supervisory processor and as a memory multiplexer/demultiplexer, allowing the use of generic low-cost DRAMs. The 7300 controls operation of the 7301, which is transparent to the user.

To achieve high performance, a graphics system must be able to quickly transfer blocks of data within the frame buffer. Central to the performance of the NCR system is the ability to perform fast block transfers of data within the frame buffer, as well as block moves of data to and from the 7300's cache memory (Fig. 2). Pixel data can be shifted, masked, and overlaid or exclusive OR'd with existing pixels. Each 7301 supports two bit planes.

A 16-color system with a 1,024-by-512-frame buffer (Fig. 3) uses the 7300 color graphics controller, two 7301 memory-interface controllers, eight 64-K-by-4-bit RAMs, and two TTL buffers for the RAM address and control signals. A two-transistor buffer for each analog output is also needed.

This system can be configured to serve multiple application environments, says Loftus. The time, the number of lines displayed and the number of pixels per line are all software programmable. The only limitation is the maximum size of the frame buffer, which is 1,024 by 1,024 by 8 bits, and the maximum video rate of 30 MHz. Within these boundaries, this system could be used for a variety of display formats, including 640 by 200, 640 by 400, 640 by 480, 800 by 400, and 960 by 350 pixels, all noninterlaced with a 60-Hz refresh rate. With the maximum 1-megabyte frame buffer, it can also support a large interlaced display, such as 1,000 by 700 pixels.

Although NCR has implemented its graphics processor in two chips, it plans eventually to integrate most of the functions of the 7300 and 7301 in a single-chip graphics controller, which will further improve chip count in systems, says Loftus. The company will fabricate the chip using a sub-2-μm CMOS process. The single-chip version is expected to be available during 1987. □

## A THREE-YEAR EFFORT BY THE NCR DESIGN TEAM

**Development** of the 7300/7301 graphics chip set at NCR can justifiably be called a group effort. It involved six engineers and designers who for the most part have been with the project from its inception three years ago.

The team was headed by 39-year-old Dave Henderson, an alumnus of Texas Instruments Inc. who has been at NCR for six years. Working with him were senior topology manager Dan Hackney, who was responsible for implementing the design of the company's computer-aided design tools; Brian Herbert, who as applications leader and technical coordinator worked with Henderson in analyzing the market and defining the product; Steve Johnson, who was responsible for the design of the color graphics chip; Mike Lahey, responsible for the 7301 design; and James Robbins, who worked with Johnson and Lahey on both chips.

According to Henderson, the toughest part of the project was the definition phase. He and Herbert had to analyze the marketplace, recommend to the company which direction to go in as a follow-on to its earlier CRT controller products, then define the basic architecture.

"It became clear after about six to nine months of study that certain trends were emerging: color graphics, multitasking, windowing, sophisticated text and character management, and the ability to merge the two in the same display," says Henderson. "The problem was in determining what mix of these features to implement."

Although the temptation was there to design a high-end chip, with all the bells and whistles, decision making was simplified when the company determined to go after the largest part of the market, based on units sold—the medium-performance segment typified by many personal computer designs.

"Unlike the high end of the graphics market, such as engineering and scientific work stations, where the name of the game is performance no matter what the cost, the rules are somewhat different in the medium-perfomance segment," says Henderson. "There the goal is cost-effective performance—that is, users want as much performance as they can get but only within specific price parameters."

With that perception, definition and eventual design of the chip set were relatively straightforward. The NCR design team focused on achieving reasonably good color graphics, but not at the cost of text display and management; multitasking and windowing, but not at the cost of overall performance or system cost; and integration of as many functions as possible on as few chips as possible, but not to the point of pushing the process technology beyond its density and reliability limits.

**GRAPHICS TEAM.** NCR's Robbins, Herbert, Henderson, Hackney, Lahey, and Johnson, from left.

PROBING THE NEWS

# THE SCRAMBLE TO WIN IN GRAPHICS CHIPS

## INTEL AND NCR ARE THE LATEST TO ENTER THIS HOT NEW MARKET

*by J. Robert Lineback*

**DALLAS**

The race for the lead in the graphics chip business is turning into a stampede. Two more contenders galloped into the fray this week: Intel Corp. with its much-anticipated 82786 graphics coprocessor and NCR Corp. with a two-chip set for color graphics control.

It's still anyone's race for the market that was opened by Hitachi Ltd. and NEC Corp. two years ago. But Texas Instruments Inc. got out of the gate first with the next wave of chips earlier this year when it started shipping samples of its speedy programmable 32-bit graphics microprocessor. Nearly a dozen other new designs are in the works at such chip houses as Advanced Micro Devices, Fujitsu, Honeywell, Inmos, National Semiconductor, Signetics, and Toshiba, plus pioneers Hitachi and NEC.

"The thing that triggered all of this was the dramatic drop in memory prices of a couple of years ago," says Intel's Mark Olson, product manager in the Graphics Component Operation in Santa Cruz, Calif. Inexpensive dynamic random-access memories made RAM-intensive, bit-mapped displays affordable for desktop personal computers. But handling high-resolution color graphics has proven daunting for the microprocessors in today's personal computers.

So chip designers decided to take the opportunity to move this tough graphics-control job out of the CPU and into a special-purpose microprocessor they would come up with for the systems designer. The idea is to send system designers back to the drawing board by giving them far greater power to manipulate video-display pixels independent of a computer's busy host processor. To do this, they are packing the new graphics chips with more intelligence, enhanced embedded drawing algorithms, support for emerging industry interface standards, and bit-mapped display features. Some designs have parallel-processing capabilities, allowing these devices to execute graphics while the host processor applies its muscle to the application.

**GROWING MARKET.** This embryonic market is attracting a crowd of chip makers because of its mind-boggling potential: sockets in every personal computer and many engineering work stations. Estimates from TI show that some 9 million home computers, desktop business models, and work stations worldwide could have used such graphics chips in 1985. And that number is expected to nearly double by 1988 (chart). In addition, graphics chip makers are hungrily eyeing such applications as laser printers, plotters, office copiers, facsimile transmitters, instrument equipment, machine-vision systems, and automotive dashboard displays.

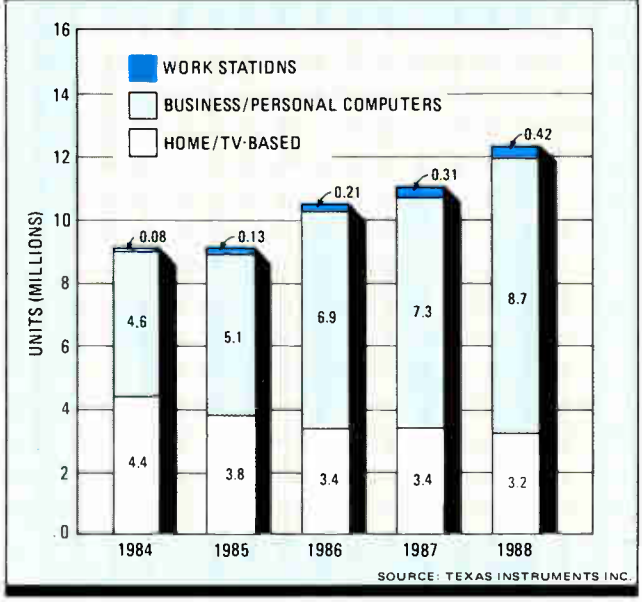
For their part, personal computer makers hope the new chips will enable them to offer fast color displays akin to those of the expensive engineering work stations. Even a few work-station makers are considering the new chips as lower-cost replacements for bipolar bit-slice processors in graphics-display engines. That would help them fight off the onrushing high-end personal computers, such as IBM Corp.'s AT model.

But personal computers will undoubtedly be the first battleground for the competing graphics chips. In fact, NCR sees the market for its new chip set as the lower-cost part of that segment (see story, p. 61). The other newcomer, Intel, is looking to the same market as TI: computer-aided-design and business machines as well as high-end personal computers (see story, p. 57).

The new ICs are getting a hearty welcome from graphics specialists. "I think these chips will revolutionize the DOS market [IBM PCs and compatibles]," says Kim DeWindt, program manager for the Direct Graphics Interface Specification hardware standard proposed by Graphics Software Systems Inc. The Beaverton, Ore., software house worked with both Intel and TI on their chip designs. In return, the two rivals are part of a group of companies endorsing DGIS for the IBM PC market.

Enthusiasm for the chips is also starting to surface at some third-party vendors of graphics boards. "These families of new graphics chips are definitely opening the door for the next-generation products," says Charles Mauro, engineering fellow at Video-7 Inc. The Milpitas, Calif., company is planning to use TI's 34010 graphics processor in a prototype add-on card for IBM PCs and compatibles. "Considering what today's nonintelligent graphics adapters give you in the AT, just imagine what will happen when graphics are offloaded [from the 80286 central processor]," Mauro says. "In many ways it will match or beat the capabilities of today's

*WORLD BUSINESS MARKET MAKES BIGGEST TARGET*



work stations. And that is for plug-in adapters costing under $1,000."

Some customers are discouraged by the popularity of the graphics processor ICs. Take, for example, the experience Vectrix Corp. had with the widely used 7220 chip from NEC. Vectrix was one of the first to design it in, introducing its product at Comdex several years ago. "The next year, we went back and there were 8 million other companies using the 7220," says Larry Addison, director of marketing at the Greensboro, N. C., graphics-subsystem house. As a result, Vectrix is planning to use semicustom and custom chip designs to widen the space between its boards and those from its competition.

Meanwhile, the field will likely become quite crowded before the dust settles. The list of entrants is a veritable directory of the semiconductor business.

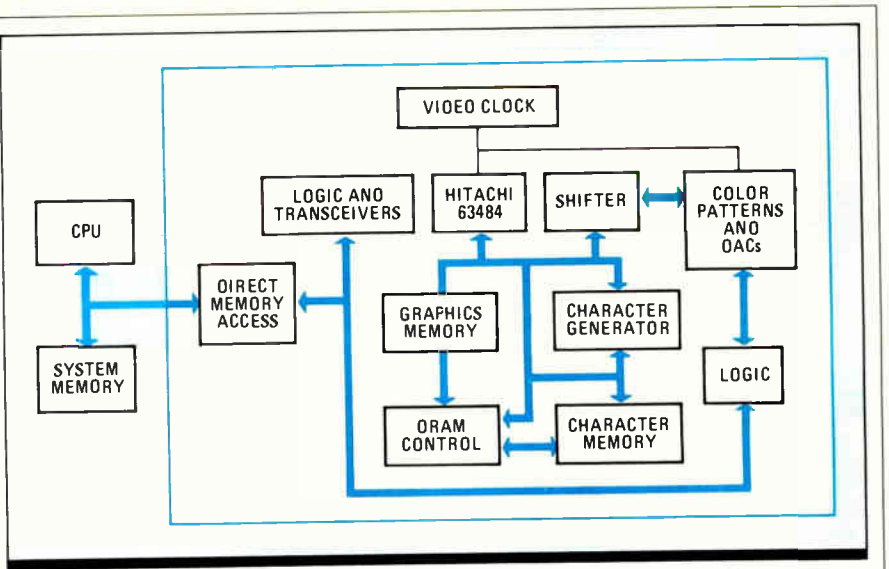
Later this year, for example, National Semiconductor Corp. will start offering samples of its DP8500 raster-graphics processor and the DP8510 bit-block-logic-transfer processor, or BitBLT. The two CMOS processors represent a divide-and-conquer strategy, says Charles Carinalli, director of advanced peripheral and software products in Santa Clara, Calif. The 44-pin BitBLT processor will be an inexpensive slave dedicated to each display plane and operating in parallel with the 68-pin master.

"We've got an SIMD architecture, meaning single-instruction processor and multiple-data manipulators," says Carinalli. "We originally started out doing one processor, but realized we would reach a performance limitation after two or three display planes."

**THIRD QUARTER.** Over in Sunnyvale, Calif., Advanced Micro Devices Inc. is preparing to introduce in the third quarter its Am95C60 quad-pixel data-flow manager, the design of which was influenced by work-station vendors who decided to use AMD's bit-slice products rather than earlier generations of graphics processors.

"We started looking at what the missing pieces were when our customers opted not to use the first graphics engines, like NEC's 7220," says Steve Dines, strategic marketing director of AMD's Logic Products Division. Embedded into the 95C60 are fast BitBLT algorithms along with basic drawing primitives. The chip can paint an average of 40,000 characters per second into a bit-mapped memory.

Others also have designs in the wings. In Japan, Hitachi—which helped start the stampede of graphics processors in 1984 with the introduction of the HD63484—says it is improving the speed of the device and adding support for the Computer Graphics Interface (CGI) standard as well as developing a next-generation chip. Toshiba Corp. and Fujitsu Ltd. both report they are working on high-end graphics introductions.




**A PIONEER.** The Hitachi HD63484 graphics processor, which appeared in 1984, was, along with a chip from NEC, the forerunner of the present generation of graphics processors.

In the U. S., Signetics Corp., which recently began second-sourcing Hitachi's 63484, plans to introduce a coprocessor aimed at boosting windowing capabilities. Dubbed BMAP, the chip translates alphanumerics into bit-mapped graphics. It will be unveiled at Wescon in November. Inmos Ltd., in Colorado Springs, is expected to debut a graphics processor, the G412, based on its transputer architecture. Motorola Inc., which dropped its 68940 raster-graphics processor in January, is developing a new strategy centered on its 32-bit 68020 microprocessor. And Fairchild Semiconductor Corp. is putting together its own plans.

With Intel and TI going head to head, the consensus among third-party board suppliers gives Intel's coprocessor an edge in IBM AT and AT-compatible markets because the 82786 is designed to work with Intel's 80286 host CPU.

**30 FOR INTEL.** "At this point, we've got over 30 solid design wins," claims Intel's Olson. Among software and hardware suppliers that announced this week they will use or support the 82786 are Ashton-Tate, Digital Research, Graphics Software Systems, Lotus Systems, Microsoft, Nova Graphics International, Number Nine Computer, and Reuters.

The 82786 coprocessor's introductory price is $81.25 each in 10,000-piece quantities. In 1,000-piece lots, the chip will cost just under $100. Samples are now available and volume deliveries will start in the fourth quarter.

Still, many observers believe the race between Intel and TI is far from over. Unlike Intel's device, TI's programmable processor—the 68-pin 34010—is a general-purpose 32-bit microprocessor containing a graphics-oriented reduced-instruction-set computer. "I think [the differences between the TI and Intel chips] could be traced back to the culture of the companies," says Kevin McDonough, graphics product manager at TI, Houston. "If you are a host-processor-oriented company—such as Intel—you are not about to create a new general programmable element into the system. The controller peripheral is going to be built around your own host."

Introduced in the first quarter [*Electronics*, Jan. 27, 1986, p. 15], the TI chip has a sample price of $500 apiece and will also enter volume production in the fourth quarter. It executes 6 million instructions per second, addresses a gigabit of storage, and completes raster-manipulating operations in a single cycle. The 34010 may be programmed in high-level languages such as C.

**HANDY MIX.** TI's chip holds user-programmed drawing algorithms, and McDonough believes the programmable approach will enable companies to mix proprietary graphics algorithms with emerging industry standards, such as CGI or the Graphics Kernel Standard, known as GKS. Intel's chip has hard-wired graphics primitives, which the company believes will prove faster than TI's programmable approach.

"It will be interesting to watch what happens," he adds. "I think you will see a lot of design engineers get excited about programming algorithms in the TI chip, but you'll see a lot of management being more interested in the Intel chip because there is more safety in having all of this hardwired. You don't have to worry about software bugs." □

*Reporting provided by Michael Berger, Clifford Barney, Bernard Conrad Cole, and Debra Michals*

# WHEN A FIGHTER FLIES ITSELF IN A LOW-ALTITUDE ATTACK

## TESTS FIRM UP DESIGN OF ELECTRONIC SYSTEMS FOR NEW FIGHTERS

*by Wesley R. Iversen*

**DAYTON, OHIO**

The advanced electronic air-combat systems of the future are now going through their paces over the California desert near Edwards Air Force Base. There a specially fitted-out F-16 fighter is testing the Automated Maneuvering Attack System, or AMAS, the second phase of the program known as AFTI/F-16: Advanced Fighter Technology Integration.

The F-16 is showing how it can approach a target at extremely low altitude, pop up from behind a hill or valley, lock onto the target, and deliver its weapons under computer control—all during a screaming 5-g turn. The entire attack, including a low-altitude escape, typically takes 30 seconds or less. And it would be risky without the help of lasers, sensors, triply redundant computers, voice recognition and synthesis, and other highly advanced technologies.

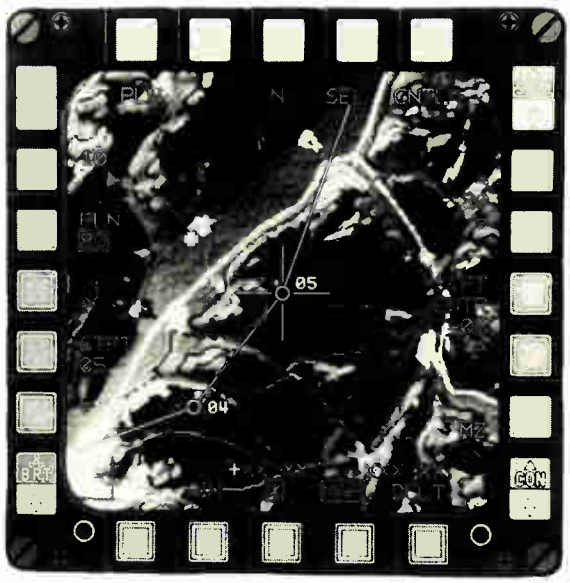
All that and more is involved in the Phase II flight tests. At the altitudes used—down to 200 ft—an already overworked pilot might be distracted long enough to crash his airplane. What's more, with the plane under manual control, the pilot would be hard-pressed to deliver bombs accurately during a high-degree bank.

"Today's low-altitude missions are typically a wings-level, straight-in type of delivery," says Lt. Col. Donald H. Ross, manager of the AFTI/F-16 program at Wright-Patterson Air Force Base, near Dayton. "Our objective is to put maneuverability back into the weapon delivery and, therefore, get better combat effectiveness and survivability."

The importance of AFTI, which so far has cost $72 million, can be judged from the fact that no less than 16 papers on the program are scheduled at this week's National Aerospace & Electronics Conference (Naecon) in Dayton. They are likely to draw heavy attention because the AFTI effort aims to develop, integrate, and flight-test the technologies of future warplanes.

Sponsored jointly by the three services and the National Aeronautics and Space Administration, the AFTI test-bed jet is flying out of the NASA Ames-Dryden Research Facility at Edwards. Phase I tests in 1982 and 1983 focused on development of the multimode Digital Flight Control System [*Electronics*, July 28, 1982, p. 50].

Phase II testing began in September 1984 and is to end this December. It aims to explore advanced forms of aircraft combat automation through the extensive integration of fire control and other avionics systems with the digital flight-control capability established in Phase I. Technologies proven under Phase I are already beginning to show up in plans for U.S. warplanes.




**GROUND PICTURE.** AFTI's cockpit display shows a digital terrain map encompassing 20 nautical miles. It includes landmarks as well as turning points in the pilot's flight plan.

The Naecon sessions on AFTI will lay out results of Phase II AMAS tests to date. With AMAS, a pilot can rely on the airplane to automatically fly itself and deliver weapons in a collision-free, precision flight path during low-altitude dynamic maneuvers that would tax the limits of a pilot's capabilities.

AMAS gets its smarts predominantly from software modifications made by F-16 builder General Dynamics Corp., Fort Worth, Texas, that integrate the plane's fire-control computer with its triply redundant flight-control system. But one key new hardware element of the system is an infrared laser sensor/tracker supplied by Westinghouse Defense and Electronics Center, Baltimore. The closed-loop AMAS control system uses ranging data from the sensor/tracker during the automatic attack mode.

Though AMAS is designed for both air-to-air and air-to-ground combat, tests so far have concentrated primarily on the low-altitude air-to-ground mode, says Ross. Unlike similar IR or radar sensors on conventional modern aircraft that are mounted on the belly, the 350-lb Westinghouse sensor unit is mounted conformally in the AFTI jet's right wing strake, with a counterbalancing dummy pod in the left wing. That gives the AFTI jet the "look-up" capability necessary to stay locked on a target during a high-degree bank, Ross points out. Conventional belly-mounted sensors can only look down and look back.

When beginning a low-altitude bombing run, the AFTI pilot relies on a digital electronic map generator supplied by Harris Corp., Melbourne, Fla. Using a central cockpit-mounted 5-in. multimode color display from Bendix Corp., Teterboro, N.J., the map generator ties into Inertial Terrain-Aided Navigation software supplied by Sandia National Laboratories, Albuquerque, N.M.

With the system, terrain information stored in the map is compared with real-time radar altimeter data to precisely locate the aircraft within the map field. Inertial navigation systems used in commercial aircraft can be off by as much as a nautical mile, Ross says. But the Sandia software can provide autonomous navigation to within 100 meters.

**HILL HOPPING.** Thanks to the new terrain-following capability, the pilot can use ground features to mask himself from the target on the ground until the last possible moment. When the plane pops from behind the terrain to within sight of the target, the sensor/tracker has already been directed in the general target direction based on data from the system. The pilot then must do the final aiming to lock the sensor onto the tar-

get, select the weapon delivery range, and activate the AMAS system.

When the AMAS system is activated, the plane's fire-control computer uses data from the sensor/tracker to calculate the maneuver needed to deliver the weapon. The pilot receives predictive information on the attack, including projected flight trajectory and the weapon release point, through symbols on the head-up display.

When the AMAS exercise commences, the pilot authorizes weapons fire by pressing a button on his sidestick controller and rides through the maneuver. During the attack, system guidance is provided by the fire-control computer based on data from the sensor/tracker, which is integrated with the digital flight-control computer to automatically fly the plane.

The AMAS system builds upon a less sophisticated technology known as Integrated Fire Flight Control that has already been proven on F-15 fighter tests, Ross says. AMAS uses the same basic algorithm (provided by General Electric Co.) for fire and flight control as that employed in the IFFC/F-15 program. But the AFTI technology goes beyond it by more fully automating the attack maneuver and by integrating system safety features needed for the low-altitude AFTI runs, Ross says.

**IN THE SWIM.** Indeed, a major part of the AMAS integration effort involved the development of what is called SWIM software (for System-Wide Integrity Management). SWIM development "was one of the primary research objectives" for the AFTI Phase II effort, Ross says. "Our goal was to be able to deliver weapons as low as 200 ft in a 5-g turn, and to get that, we had to have protection at these low altitudes. The pilot was not going to be able to confidently go down there and ride through the maneuver unless the safety factor was built into the flight-control system."

Another technology under test in Phase II AFTI flights is voice synthesis and recognition, using competing systems provided by Lear Siegler Inc., Grand Rapids, Mich., and Texas Instruments Inc., Dallas. Phase I AFTI tests using the Lear Siegler system established the feasibility of voice for use in noisy, high-g cockpit environments, says AFTI/F-16 deputy program manager Frank R. Swortzel.

Phase II aims to improve recognition accuracy and evaluate the best potential uses. Systems from each vendor currently incorporate 250-word vocabularies for both recognition and synthesis. The Lear Siegler system can handle connected-phrase recognition, but the TI unit is an isolated-word system. A version of the TI system incorporating an advanced connected speech algorithm is expected late this year.

A voice feature that warns the pilot of danger plays a role in an AFTI automatic-recovery system designed to prevent loss of aircraft and crews due to either spatial disorientation or pilot blackout, which the Air Force calls gravity-induced loss of consciousness. As aircraft capabilities have increased, loss of consciousness has become an increasingly serious problem, with 10 aircraft lost because of it during the last four years, military sources say.

But Ross notes that one beauty of the AFTI automatic-recovery system is that it does not rely on detection of pilot blackout. "There are situations where the pilot is not blacked out, but loses awareness. He may be preoccupied with his map or he could be diving at the ground while looking back over his shoulder at the guy who's attacking him, and he doesn't realize that he's about to get himself into an unrecoverable situation," the AFTI program director explains. In fact, over the past 15 years, mishaps attributable to such disorientation have wiped out more than 50 U. S. airplanes.

With the AFTI automatic-recovery system, the pilot is warned both verbally and by visual display of impending disaster. If he doesn't respond, the system automatically levels off the plane and takes over flight control until the pilot regains consciousness or awareness and takes control of the plane himself.

**COMING SOON.** Some AFTI systems are already earmarked for future craft. For example, an advanced digital flight-control system that draws heavily on AFTI work will be incorporated in a version of the F-16C/D fighter scheduled for 1988 operation, while the F-15E will also incorporate some digital flight control elements during the same timeframe. Though Ross can't make specific predictions, he says that some automated flight-control features perfected in Phase II testing—including the system for automatic recovery during pilot blackout—will be naturals for early use on aircraft.

Remaining Phase II tests will focus more heavily on tests of air-to-air AMAS combat. AFTI officials are now looking ahead to a possible Phase III. Though not yet approved for funding, that effort would focus on developing even more sophisticated automatic terrain-avoidance capabilities, says Swortzel.

One aim would be to improve the current Phase II ground-collision-avoidance system, which does not account for terrain features stored in the digital map and assumes a maximum 2% grade change in the AMAS attack arena, says Swortzel. This forces the pilot to make his own assessment of terrain features that might cause a crash.

But future flight-technology programs will likely integrate additional sensor data from the airplane to create what Swortzel calls an "all-terrain automated combat" capability. With that, a pilot could confidently put the plane in an automatic low-altitude attack mode no matter what the surrounding terrain. "Whether we [AFTI program management] do it or somebody else does it, we believe it's the next logical step from the technology we're working on today," Swortzel concludes. □


**POD ON THE PLANE.** Westinghouse's laser sensor/tracker pod mounts where the wing meets the fuselage on the F-16 test plane.

# THE TOUGHEST FIGHT YET FOR MONOLITHIC MEMORIES

## DRAWN BY MMI's SUCCESS IN PROGRAMMABLE LOGIC DEVICES, THE COMMODITY SUPPLIERS JUMP INTO ITS NICHE

**NEW YORK**

It may be in the midst of the toughest fight in its seven year existence, but Monolithic Memories Inc. is like the boxer that boasts "they hardly laid a glove on me." The Santa Clara, Calif., pioneer of the market for programmable logic devices is a classic example of a company that has exploited its niche so successfully that it has drawn the big guys into the business. Now MMI is preparing to slug it out with the giant semiconductor houses.

Company executives are confident MMI is well positioned to maintain its dominance despite a dismal profit picture in the past 18 months. "We're going to fight like hell to keep our share of the market," says president Irwin Federman. "We'll build upon our base and extend our reach."

Having pioneered the PLD market with its patented programmable array logic (PAL) products, MMI is now facing competition from the likes of Advanced Micro Devices, Fairchild, National Semiconductor, Signetics, and Texas Instruments. These companies all want a piece of a lucrative business. MMI so far is successfully beating them back with its bipolar PALs, while planning for new growth with CMOS products such as gate arrays.

It's a battle worth fighting. "The whole programmable-logic market is a good growth market and a good place to be," says semiconductor analyst James L. Barlage of Smith Barney Harris Upham Inc., New York. "That's why everyone wants to get into the market." According to market researcher Dataquest Inc., the industry will reach $280 million in 1986, up from $240 million in 1985. By 1990, says Andy Prophet, an analyst with the San Jose, Calif., company, the market will hit $1 billion. And, he says, MMI is "the major player in the market right now, with revenues of $120 million to $122 million in programmable logic devices."

The PLD market is being driven by two factors, Prophet says. On the one hand, as the semiconductor business increases in general, PLDs "are getting their share of the increase." Second, PLDs can be customized by the user quickly and cheaply. "Some of the money [formerly] being spent on gate arrays now is going to PLDs," he says.

That's why MMI plans to stick with this market and build on the clout it has achieved, says Federman. "One can build a very significant company on programmable logic arrays, and we want to be that company. We also want to capitalize on the [other] opportunities that we can without diluting our efforts in PLAs," such as moving into the larger gate-array market.

**SALES UPS AND DOWNS.** Founded in 1969, MMI scored sales of $187.3 million and earnings of $26.9 million in the chip industry boom year of 1984. But sales slipped 6% in fiscal 1985, which ended September 30, to $177.7 million, while earnings plunged 61% to $10.5 million. In the first half of fiscal 1986, sales are running 7% behind the same period last year, and earnings are off 84%. But Federman says MMI's bookings and backlog have improved significantly in recent weeks, so he agrees with Wall Street analysts' predictions that things will be looking up in the third quarter.

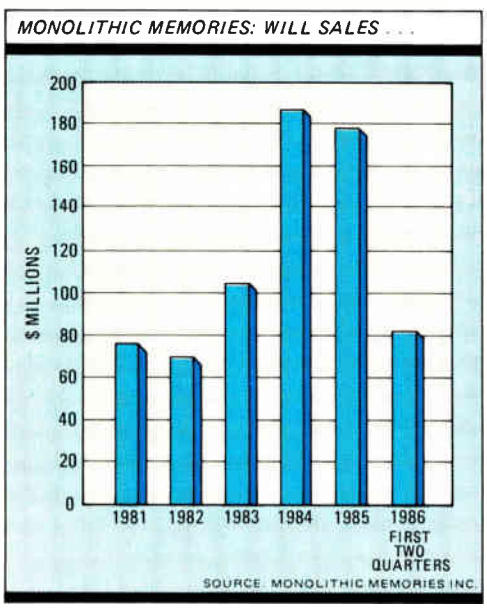
As for the future, Federman says, "We need the computer business to pick up as the year progresses for the fourth quarter to show a gain." About 70% of MMI's sales go to computer makers, and "unless that [pickup] happens, the fourth quarter won't be better than the third quarter. But even if it's not worse than the third quarter, that represents a gain over the fourth quarter last year," he notes.

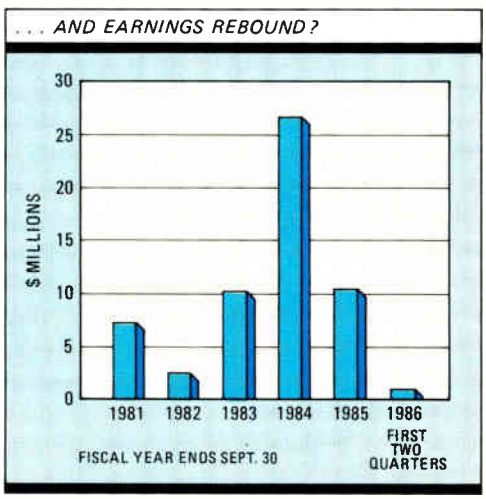
An accountant by training, Federman is credited by industry observers with MMI's success, turning it into a business that he calls "noticeable and in competition with the major companies. If we're not in the big leagues, we're certainly in the Triple-A league."

That management skill will be tested as MMI continues to fight the challenge of such big suppliers as TI, which has ignited a price war since it entered the PLD market in the summer of 1984. But if TI has generated a cloud over MMI's horizon, it's one with a silver lining, says Michael Kubiak, an analyst with Kidder Peabody & Co., San Francisco. "TI's entry has caused prices to go down, but it also increased the size of the business. TI took market share from other suppliers," including National Semiconductor and AMD, but not from MMI, he asserts.

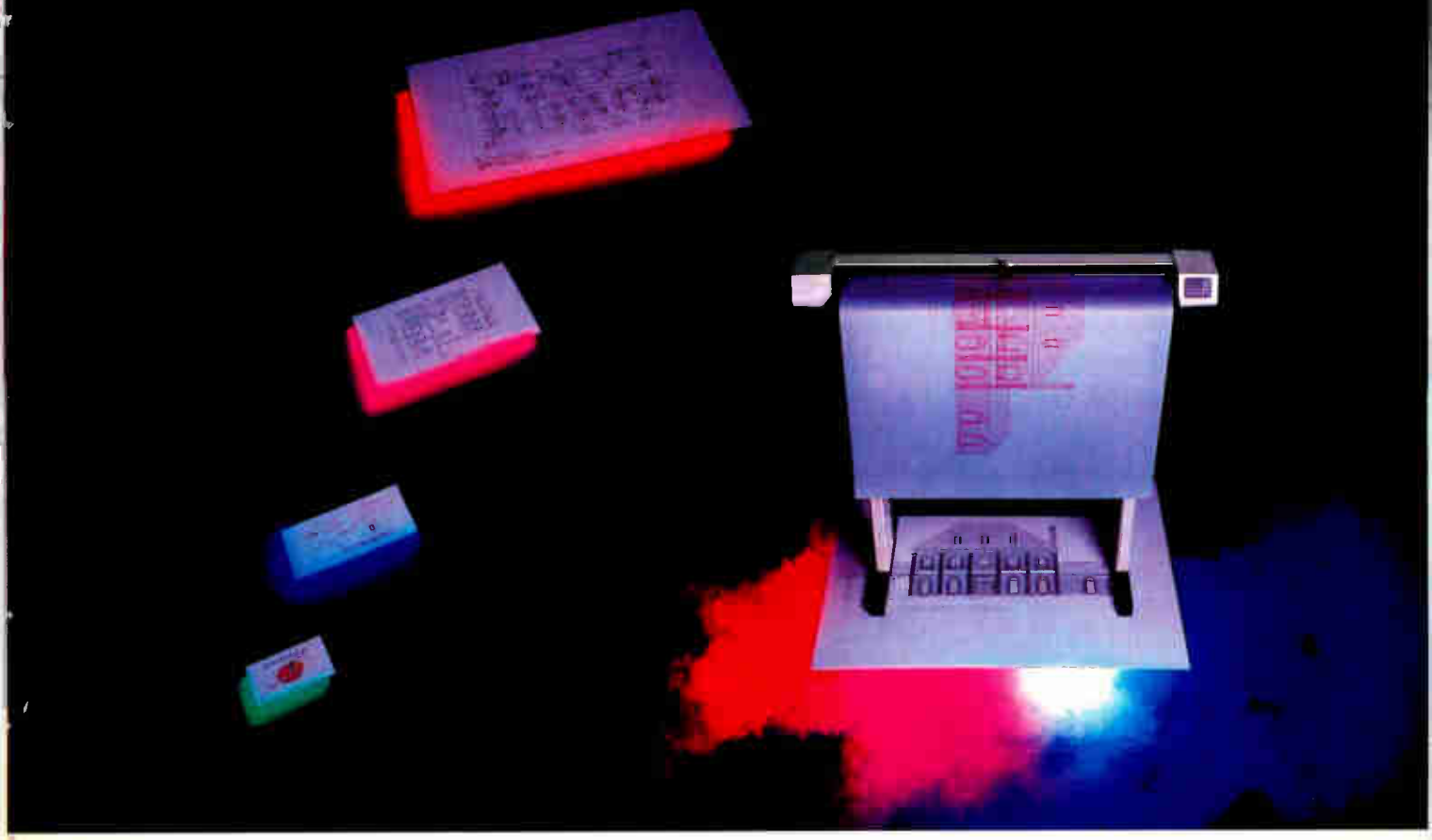
Federman, meanwhile, is sticking to his guns in the

**FEDERMAN:** MMI's president is confident his company can beat back new competitors.



# STEP UP TO E SIZE



Houston Instrument's new E size DMP-56 delivers the precision, throughput, and reliability you require from a drafting-intensive plotter. The DMP-56 also gives you the flexibility to handle 18 different drawing format sizes ranging from 8½ × 11 inches to 36 × 48 inches.

The DMP-56 was designed for any application calling for crisp, clean graphics—whether it's architectural floorplans, mechanical designs, electrical schematics, or overhead transparencies. Because of its media-size adjustment mechanism and automatic media-size sensing feature, the DMP-56 quickly and efficiently responds to your changing format requirements. This high-performance plotter can produce standard (A through E), metric (A4 through A0), oversize (A4 through A0), and Architectural C, D, and E drawings.

The DMP-56 is a professional drafting plotter that draws on the established track record of Houston Instrument's very successful DMP-51/52 and DMP-51/52 MP plotters—plotters that redefined the standard for price, performance, and quality.

Immediately compatible with hundreds of computer-aided design and graphics software packages through our powerful DM/PL™ command language, the DMP-56 also gives you a precise resolution of .001 inch and a maximum plotting speed of 17 inches per second. And, because it uses a standard RS-232-C compatible interface, the DMP-56 can operate with virtually any computer on the market.

The DMP-56 also delivers features you'd expect only from more expensive* plotters—such as quiet servo drive, and an easy-to-use front-panel control. Combine these standard features with the well-known Houston Instrument reliability and support and you have a superior plotter at a reasonable price.

In terms of throughput, performance, price, and quality the DMP-56 is the professional graphics tool you need. For more information, call 1-800-531-5205 (512-835-0900 if in Texas), or write Houston Instrument, 8500 Cameron Road, Austin, Texas 78753. In Europe, contact Houston Instrument, Belgium NV., Rochesterlaan 6, 8240 Gistel, Belgium. Tel.: 32-(0)59-277445. Tlx.: 846-81399.

*U.S. suggested retail price is $5,995. Pricing subject to change.
DM/PL is a trademark of Houston Instrument.

**houston instrument**

A Division of AMETEK

Circle 69 on reader service card

The evidence is in, and it's incontrovertible. When it comes to light, Anritsu runs second to the sun.

True, Anritsu's little laser diodes *are* powerful enough to raise more than a few eyebrows.

And Anritsu optical attenuators can cut *almost* any light source down to size.

And Anritsu optical power meters can take anything a *normal* fiber optic system can dish out.

But none of them can hold a candle to the sun, with its $900 \times 10^{23}$-or-so calories every second and 10-billion-year MTBF.

Still, if you take a closer look, you'll see a bright side to this story.

For instance, let's talk technology: does the sun have anything like Anritsu's laser-accurate outside diameter measuring system for optical fiber production?

In sophistication, Anritsu also has a clear edge. With optical time domain reflectometers and optical spectrum analyzers that give a clear, accurate picture of an entire fiber optics network.

And in terms of visibility, the Anritsu name has become almost an industry standard.

Thanks to a dazzling range of measuring

instruments and light sources for all facets of fiber optic communications.
What about versatility? Simply no competition: Anritsu has more than 11,000 products and systems, and these extend to areas far beyond light. To rugged radio and telecommunications equipment. To public telephones, computers and data processing equipment. To measuring instruments for communications. The list goes on and on.
The sun is still safely #1 for now.
But we're on the move.

Circle 71 on reader service card

Anritsu

**WE'RE ON THE MOVE. WORLDWIDE.**

ANRITSU CORPORATION
10-27, Minamiazabu 5-chome, Minato-ku, Tokyo 106, Japan.
Phone: Tokyo 03-446-1111, Telex: 0-242-2353 ANRITU J

***As of October 1, 1985, Anritsu Electric Co., Ltd. became Anritsu Corporation.***

fight and is committing 16% of MMI's fiscal 1986 revenue to total company research and development. He expects to lose some share in the PLD market—"it's impossible not to lose share, given the quality of the competition." But he foresees a healthy 45% to 50% of MMI's revenue derived from PLDs by 1989 or 1990, compared with 75% in fiscal 1985.

**MOVING TO CMOS.** The company will also diversify its product line by moving to CMOS technology. Through a just-ended agreement with Cypress Semiconductor Corp., a startup chip maker in San Jose, MMI has learned about CMOS technology (although skeptical observers say Cypress may have learned more about PAL technology than MMI learned about building in CMOS).

*'A host of CMOS products' is next*

MMI is "spending a lot of money on CMOS," Federman says, and "presenting a broad array of CMOS products" is the company's No. 1 technological challenge. He says MMI will introduce "a host of CMOS products later this year," including a CMOS gate array, a controller for 1-Mb dynamic random-access memories, and other memory-support chips.

"MMI had a late start in CMOS," notes Kubiak, "and they are working hard to correct it." However, he adds, "I don't see CMOS making a significant contribution to MMI's business until the second half of calendar 1986. By the first half of 1987, it could account for 10% of MMI's business," but that figure is optimistic.

The big plank in the company's CMOS strategy, though, is gate arrays. "It makes sense for them to go to gate arrays," notes Smith Barney's Barlage, because "it moves them one level higher" in chip integration and gives MMI's customers a good migration path for higher integration.

However, he notes, "the biggest challenge they face over the next three years is maintaining their position in PLDs. I'm not worried about their meeting the challenge of the gate-array people but the commodity guys who want to buy their way in."

Counters a confident Federman: "We're the best guy out there and we'll be able to do well. It will be a battle for any competitor to knock us out of a socket." *–Robert J. Kozma*

## BOTTOM LINES

### GROWTH SLOWS IN MILITARY ELECTRONICS

U.S. production of military electronics equipment will grow only 8%, to $49.6 billion, in 1986, a little better than half last year's 15.7% rate, says Henderson Ventures. The Los Altos, Calif., researcher characterizes this year as "a period of unprecedented uncertainty for military electronics suppliers." The decline is due to a combination of spending cutbacks brought about by Congressional legislation and a dramatic slowdown in the international arms market as a result of lower OPEC oil revenue. Production in 1987 will advance even less—3.9%, to $51.5 billion.

### MARKET FIGHT LOOMS IN POWER MOS FETs

Falling prices and a restructuring of the market will result in a closer competition among the players in the power MOS FET market that are vying for the top spots as vendors fight for market share this year, says HTE Management Inc., a Scotts Valley, Calif., market researcher. International Rectifier Corp., still the field's clear leader, will get a stronger challenge from No. 2 Motorola Inc. HTE Management also sees third-ranked Siliconix Inc. improving its position. The market, which totaled $168 million in 1985, will see a shift in sales from military buyers to industrial customers, which are increasing their use of the product. Industrial accounts, which made up 42% of 1985's market, will increase to 57% by 1990. The military segment will shrink from 28% in 1985 to 8% by 1990, when the total MOS FET market will reach $725 million.

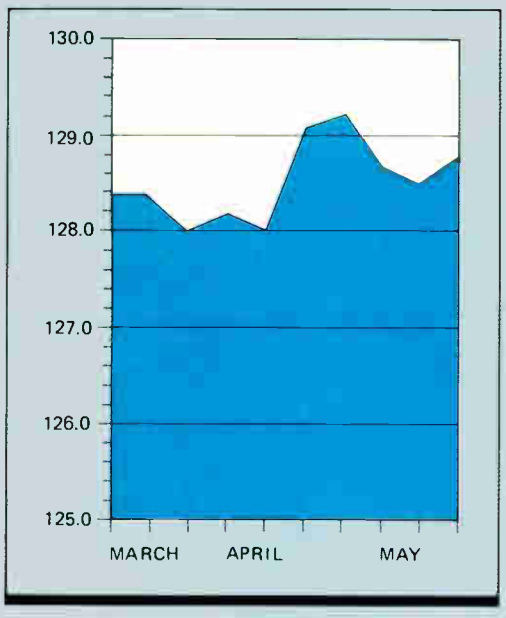
### AI MARKET TO HIT $1 BILLION IN 1986

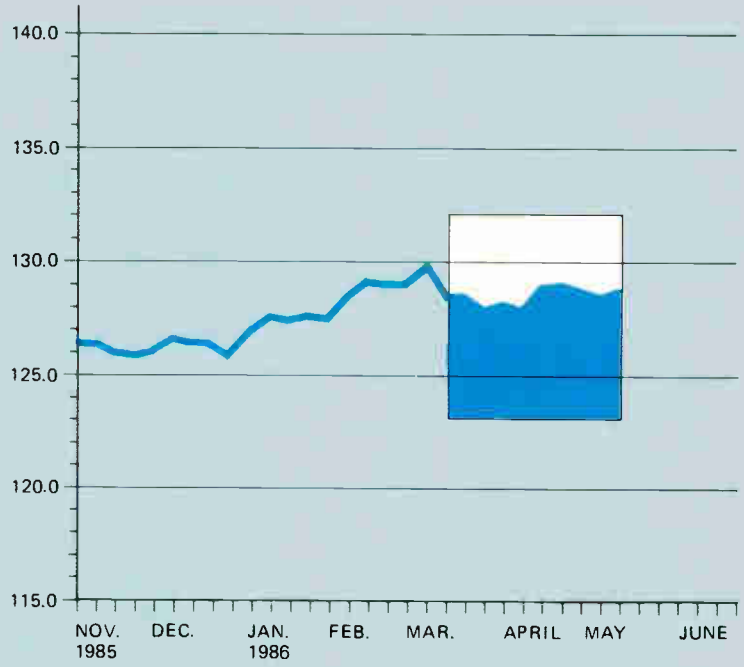
The market for artificial-intelligence products will reach $1 billion this year, estimates DM Data Inc. The Scottsdale, Ariz., market watcher says the biggest part of the AI market is computer hardware, with 49% of the dollar volume. Artificial vision systems have 25%, followed by expert systems with 13%, natural language programs with 6%, voice recognition with 4%, and AI languages with 3%.

### VEECO TO BUY MODULAR POWER

Veeco Instruments Inc. has agreed to acquire Modular Power Systems Inc. for an undisclosed amount of cash. Veeco, Melville, N.Y., says the Austin, Texas, maker of power supplies for the military will become part of its Lambda Group, which also makes power supplies.

## ELECTRONICS INDEX




| | |
|---|---|
| THIS WEEK | = 128.8 |
| LAST WEEK | = 128.5 |
| YEAR AGO | = 127.1 |
| 1982 | = 100.0 |

The *Electronics* Index, a seasonally adjusted measure of the U.S. electronics industry's health, is a weighted average of various indicators. Different indicators will appear from week to week.

## U. S. ELECTRONICS SHIPMENTS

| Shipments ($ billions) | March 1986 | February 1986 | March 1985 |
|---|---|---|---|
| Communications equipment | 5.503 | 5.427 | 5.222 |
| Radio and TV receiving equipment | 1.063 | 1.014 | 0.948 |
| Electronic and electrical instruments | 4.620 | 4.696 | 4.692 |
| Components | 3.432 | 3.263 | 3.475 |

## U. S. GENERAL ECONOMIC INDICATORS

| | March 1986 | February 1986 | March 1985 |
|---|---|---|---|
| Index of leading economic indicators | 176.6 | 175.7 | 167.6 |
| Budgeted outlays of the federal government ($ billions) | 79.700 | 77.950 | 78.852 |
| Budgeted outlays of the Department of Defense ($ billions) | 24.002 | 21.268 | 21.782 |
| Operating rate of all industries (% capacity) | 77.4 | 77.9 | 79.1 |
| Industrial-production index | 125.1 | 125.7 | 124.0 |
| Total housing starts (annual rate in thousands) | 1,949 | 1,997 | 1,849 |

The seesaw performance of the U. S. electronics industry continued in March with news that industry shipments rose 1.5% after employment and production dropped in February [*Electronics*, May 5, 1986, p. 53, and May 12, 1986, p. 57]. Though not overly vigorous, the increase came on the heels of a 5.2% gain in February and could indicate a firming trend for the industry. In fact, total electronics shipments have increased four out of the last five months, and industry sales have risen almost 5% from last October's level. The March overall increase in industry shipments pushed the *Electronics* Index up 0.3 of a point—or 0.2%—last week.

March's sales gains were spread throughout the industry. The only decline was a 1.6% drop in instrument shipments. A strong recovery in the components sector appears to be under way: March's 5.2% jump in shipments brought component sales to their highest level in 12 months. The month's increase essentially equaled February's 5.3% gain.

Shipments of radio and TV equipment were up 4.8% for the month, and those of communications equipment rose 1.4% in March.

# SCANLON IS ITCHING TO STEAL A MARCH ON IBM

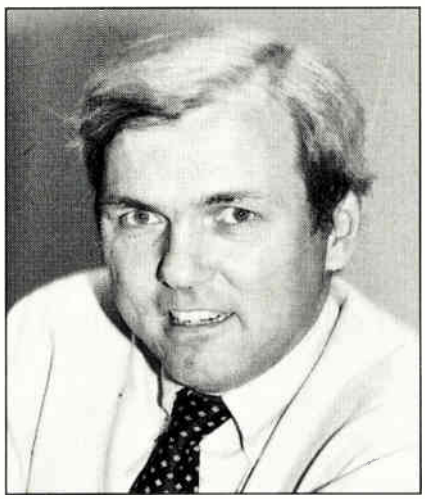
**WESTBORO, MASS.**

John Scanlon has taken his first step toward cashing in on a major market opportunity. But now the director of Data General Corp.'s Product Marketing Division is having a tough time taking the second one. His first step came when he began shipping Data General's new work stations and minicomputers, including the high-end Eclipse MV/20,000 superminicomputer, all of which were announced last November.

But now that he has the products, Scanlon is waiting for improved computer sales, which remain locked in an industrywide holding pattern. This is particularly frustrating for Scanlon because he believes minicomputer companies can cash in big on IBM Corp.'s failure to offer a workable departmental computer.

"The minicomputer companies have got to benefit from this," Scanlon says. He cites widespread customer complaints that IBM's System 36 minicomputers are just not powerful enough. "I don't believe there's anything in the near term [IBM] can do to reconfigure the System 36 to compete with the minicomputer" company offerings.

Scanlon, 41, has been in the business long enough to recognize that opportunities to steal a march on IBM are rare. Having earned an electrical engineering degree from Rensselaer Polytechnic Institute, he began his career at Data General with a summer marketing job while studying for an MBA at Harvard University in 1972. The following year, he returned as a salesman. Then came a succession of positions, including manager of product marketing, European market director, and market director for the Technical Products Division.



**JOHN SCANLON:** The opportunity for Data General is there, but the market's on hold.

After a year as chief of staff for Frank Silkman, senior vice president, and later for Robert Miller, also a senior vice president, Scanlon became director of the company's software development for three years. He assumed his present post in November.

All that experience isn't helping move products now, however. "We're getting mixed signals," Scanlon says. "We're not losing major opportunities, but we're not closing them either. The major opportunity list has the same names on it as six months ago. It's just not moving."

**REASSESSMENT.** What is keeping things on hold, says Scanlon, is that major companies are rethinking their approach to vendor selection. He maintains that the personal computer boom took place as a relatively unorganized buying pattern within corporations. Some of the purchases led to a quick payoff for users through their facility for spreadsheets and word processing, says Scanlon. The question now, he says, "is how can they get these computers channeled into some kind of a plausible workgroup-computing solution."

Beyond tying together the personal computers themselves, companies want to tie them to existing data-processing or management-information-system operations, says Scanlon. He says that customers are also considering how to create links to engineering departments and computers in factories.

Scanlon believes customers also want to reduce the number of vendors they deal with and develop a system architecture template that works across all computing operations. "They just haven't sorted these out yet," he says. "And until they sort them out, they're going to be very reluctant to choose a particular point solution from any particular vendor." *–Craig D. Rose*

## PEOPLE ON THE MOVE

**DONALD R. SORCHYCH**

☐ General Instrument Corp., New York, has named Donald R. Sorchych president and chief executive officer of a wholly owned subsidiary to be formed out of the company's Microelectronics Division. The new company, which will include all GI's microelectronics operations in Chandler, Ariz., and Kaohsiung, Taiwan, is still unnamed. Sorchych comes from Medicomp Inc., a medical products company he founded and headed since 1981.

**KEVIN J. KELLEY**

☐ The new chief of the Federal Communications Commission's Mobile Services Division of the Common Carrier Bureau, Kevin J. Kelley, is moving up from his position as the deputy chief of the Domestic Facilities Division. Kelley joined the FCC in 1980. Before that, he was manager of the blue-green laser communications satellite program at the Naval Ocean Systems Center, San Diego, where he also helped develop the Navy's ultrahigh-frequency satellite communications system.

**C. RICHARD MOORE**

☐ Excelan Inc., the San Jose, Calif., maker of hardware and software products that allow computer systems to communicate over Ethernet local-area networks, has named C. Richard Moore president, chief executive officer, and a member of the board of directors. Moore, 51, previously was president and chief operating officer of Valid Logic Systems Inc., San Jose, and spent 23 years at Hewlett-Packard Co.

**KEIICHI NAKAMURA**

☐ A former engineer and executive with Sony Corp., Keiichi Nakamura is now president of Nippon Fairchild Corp. Nakamura, 58, most recently adviser to Fuji Electric Co., replaces Ronald C. Norris, who had worn two hats as Nippon Fairchild president and head of Fairchild Semiconductor Asia Inc. Norris remains in the latter post, based in Tokyo; Nakamura will oversee Fairchild's Japanese operations.

**EARL J. CLAIRE**

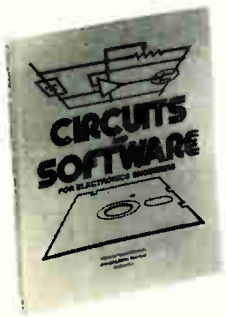
☐ E-Systems Inc. has appointed a director of strategic planning for its ECI Division in St. Petersburg, Fla. Earl J. Claire, 45, will oversee business planning, including the coordination of research and development programs. He will also serve as chairman of the division's patent committee. Prior to joining E-Systems, Claire was president and chief executive officer of Lely Electronics Inc. and Lely Independent Manufacturing Inc., both in Naples, Fla.

**JACK C. DAVIS**

☐ Dataproducts Corp., Woodland Hills, Calif., has appointed Jack C. Davis as chairman and chief executive officer. He succeeds Graham Tyson, who is retiring. Before joining Dataproducts, Davis had been senior vice president in charge of Harris Corp.'s Information Systems Sector since 1982.

## DESIGN PROBLEMS?

**CIRCUITS AND SOFTWARE FOR ELECTRONICS ENGINEERS focuses strictly on design problems!**




Access stimulating, clever approaches that can speed your creative design concepts.

This indispensable source contains hundreds of circuit schematics, block diagrams and computer programs that are conveniently organized into 25 vital categories by function.

**Design** appropriate circuitry to meet challenging specifications.

**Save time** by adapting proven circuits and software to a wide range of applications.

**Save money** and increase productivity by avoiding costly design errors.

Don't take the chance of being less than on top of the latest circuitry developments.

ORDER YOUR COPY NOW!

**Electronics Magazine Books**
P.O. Box 541
Hightstown, NJ 08520

or

**McGraw-Hill Int'l. Pub. Co.**
Attn: ECC
McGraw-Hill House
Maidenhead, Berkshire SL6 2QL
England

Send me _____ copy (copies) of R370 for $19.95 each
- ☐ Payment enclosed
- ☐ Send proforma invoice

Name _____

Company _____

Street Address _____

City _____ State _____ Zip _____

Allow 4-6 weeks for delivery.

## POSITIONS VACANT

**Murkett Associates — Technical Mgmt** placement with national affiliates-fee paid Box 527, Montgomery, AL 36101.

## POSITIONS WANTED

**Electronic Expert For Hire. I do Micro**processor hardware/software, assembly language. Analog, digital design in my N.Y. lab or worldwide. Project rates. Mr. Barry Masel (718) 476-1516.

## SPECIAL SERVICES

**We Buy and Sell all kinds of surplus inventory** — electronics, computers, OEM, etc. (718) 639-2872.

**IBM PC based Automated Test Equipment.** Turnkey ATE can result in significant cost savings either in high volume production, testing of modules & subassy's or low volume complex measurements. NP&A represents a network of electromechanical and software engineers in the N. Calif. area who provide low cost, custom built, fully documented test equipment for R&D or prod'n. req'mts. based upon customer's PC or Hewlett Packard GPIB controllers. Contact Neuman Potter & Assoc., (707) 874-2918, 12154 Occidental Road, Sebastopol, CA 95472.

## HOT LINE

To place your

**Computer Software Ad**

in

**Electronics**

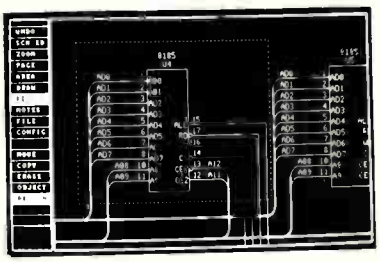
call Ilene Fader

at

**212/512-2984**

# COMPUTER SOFTWARE

## FREE DEMO DISK



**SCHEMA** is a complete, integrated schematic drawing software package for IBM Personal Computers. Use **SCHEMA** with your PC to draw schematics and automatically generate design documentation such as Wire and Net Lists, Bills of Materials, Design Rule Checks, etc. **SCHEMA** is $495 and supports most common PC hardware configurations. Call or write today for a free demo disk and brochure.

**OMATION, INC.**
1701 N. Greenville Ave., Suite 809
Richardson, TX 75081
(214) 231-5167

OMATION

*SPICE* up your *PC*

Z/SPICE professional circuit simulation
Full version $245 Student version $79
ZTEC box 737, college place, wa 99362 (509)-529-7025

## POSITIONS VACANT

**Electric Motor Repairman — Sarasota,** Florida Company has an opening for above position. Salary of $9.00 per hour based on a 40 hour work week. Must have a minimum 2 years of electrical experience. Specialized work requiring the ability to repair and maintain electric equipment. Included will be rewinding and repairing of pumps, PC boards, examining and replacing defective chord connections. Applicants apply to: Job Service of Florida, 2312 Golf-2-Bay Blvd., Clearwater, Florida 33575-8696; Att: Pat Ganno. Job Order #5462649. EOE M/F/H/V.

# NEW PRODUCTS

## GAS INJECTION GIVES CVD SYSTEM THE SPEED AND YIELD FOR ULSI

### FOCUS F1000 CAN PROCESS 70 WAFERS AN HOUR WITH +/–2% UNIFORMITY

Focus Semiconductor Systems believes its F1000 solves the three major problems associated with existing chemical-vapor deposition systems—low throughput, low yield, and large footprints. The F1000 is an automated, low-pressure CVD system with a multiplexed single-wafer reactor module. It processes 70 wafers per hour—18 at a time—and offers a film-thickness uniformity to within ±2% on wafers up to 8 in. in diameter.

Conventional wafer-deposition systems use diffusion tubes, bell jars, and radiant heating. The F1000 replaces these with a proprietary gas injection system that optimizes gas dynamics by exploiting forced-convection flux—hence the name of what the company calls the "focused flow" deposition process.

**FAST.** Focus's CVD system deposits film at up to 2,500 Å/min.

The injection system provides a higher degree of control over the flow of gases to the wafer surface. The company contends that faster, high-yield CVD systems such as the F1000 are necessary for the coming move to ultralarge-scale integration—chips with more than 100,000 transistors and device geometries scaled to submicron size.

**AGING TECHNOLOGY.** Until very recently, most manufacturers of semiconductor-processing equipment met CVD requirements by making process and system updates, the company says. Most have modified 10- to 20-year-old reactor and diffusion-tube configurations in their deposition tools without regard for efficient use of floor space and materials consumption. The F1000's modular design has a footprint of 22 ft².

Compared with 100 to 300 Å/min in conventional quartz-based systems, the Focus system delivers deposition rates of 1,000 to 2,500 Å/min. The high deposition rates improve not only throughput but also yield. Wafers spend a shorter time at temperature, thus reducing surface imperfections and, consequently, unusable lots. In addition, total process times are as low as 15 min. compared with typical cycles of more than 1 hour.

The F1000's high wafer throughput comes from the use of 18 single-wafer reactor chambers. Each chamber is isolated and crosstalk between chambers is prevented, keeping film quality high.

Film uniformity is twice the industry average, says Focus. Wafer yield and reliability are thus maintained, and the high deposition rates translate into high throughput. Users can easily upgrade their systems to 8-in. wafers with minimum retooling and expense.

The F1000 currently produces low-temperature oxide films and will offer capability for *in situ* doped polysilicon, silicon nitride, and other films later this year. Efforts are under way to develop processes for such films as low-temperature epitaxial silicon, low-temperature nitride, and aluminum.

The F1000 consists of three primary system modules for the integrated deposition module, the computer control module, and the vacuum pump module. The deposition module houses the wafer loading and unloading mechanism, the CVD reactor module, gas-flow control, and control systems for pressure and temperature.

The control module uses a Motorola 68000 and incorporates the operator keyboard, 15-in. monochrome graphics monitor, one floppy disk, and a 20-megabyte hard disk used to store program and process data. The vacuum pump module is designed to be placed outside the clean room in either an adjacent service area or basement.

The F1000 is available now for about $400,000. *–Jonah McLeod*

Focus Semiconductor Systems Inc., 570 Maude Ct., Sunnyvale, Calif. 94086. Phone (408) 738-0600 [Circle reader service number 338]

## LETTING A TEST ENGINEER BE TWO PLACES AT ONCE

Teradyne's Automated Remote Control software is designed to solve the problems of setting up, operating, and troubleshooting remote test systems.

These tasks, difficult and time-consuming under the best circumstances, can be made even harder by the geographical distance between the system and the engineer and by language barriers between the engineer and the equipment operators. For example, before a system can go into operation, on-scene operators must manually perform multiple setup functions—and if they make a mistake, the system will likely malfunction. When problems occur, the test floor may have to be shut down until a test engineer arrives—sometimes from halfway around the globe.

Teradyne predicts that its package will improve this situation and lead to substantial savings. It permits an engineer to set up, monitor, and troubleshoot A300-Series analog large-scale-integration test systems located anywhere in the world from a terminal of the test system director—the host computer of the Teranet automatic-test-equipment networking system.

The software's virtual terminal capa-

bility enables any A300-Series system on the Teranet network to be accessed from any terminal on the network, and it lets test engineers be in two places at once. Owners of A300-Series testers can use the ARC software to increase the productivity of test engineers, production operators, and test systems, according to Teradyne, thereby reducing the user's test-floor costs.

From a test-system-director terminal, a test engineer can load, set up, run, and debug test programs, as well as send summary sheets to a line printer and calibrate a tester. The engineer's productivity increases because he can troubleshoot from anywhere, and test-system productivity rises because downtime is reduced. Once the engineer creates tester setups and other tester-command sequences, they can be automatically transmitted to the tester for later execution. This eliminates typing errors and simplifies test-floor operation.

**SIMPLE COMMANDS.** With a few keystrokes, complicated job-plan setups can be executed by either the remote supervisor at a test-system-director terminal or the operator at the site. Simple operations, such as sending a summary sheet to the line printer, are made even simpler and executed more quickly than could be done manually.

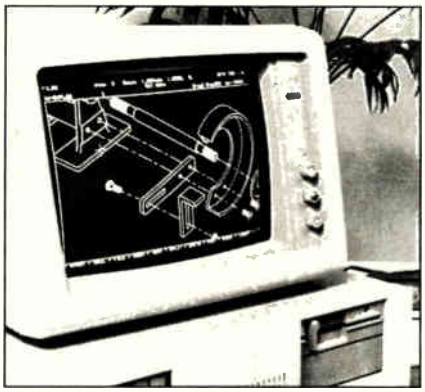
ARC software also allows test-floor managers to customize operator interfaces in their native languages; this cuts training costs and leads to standardized and simplified test-floor procedures. Using ARC software, programs can be run and data collected automatically. For example, self-test can be run on all testers every night and the data analyzed for drift or failure.

ARC software runs on Digital Equipment Corp.'s PDP-11/44 and 11/84 minicomputers, which act as test-system directors. It is priced at $30,000. ARC software to run on additional test-system directors under the same system manager is priced at $20,000 per host computer. Shipments will begin in June. *–Jonah McLeod*

Teradyne Inc., 321 Harrison Ave., Boston, Mass. 02118.
Phone (617) 482-2700 [Circle 339]

## CADAM SOFTWARE MOVES ONTO PC AT

Micro Cadam computer-aided design and manufacturing software brings many features of the Cadam mainframe software package to the desktop. The entry-level program, which runs on an IBM Corp. Personal Computer AT, provides automatic three-dimensional representations, mathematically accurate construc-



tion planes, and automatic dimensioning. Geometry grouping allows any geometry and related text to be grouped together and erased, moved, or modified without affecting other parts of the drawing.

The system requires a PC AT with 640-K of RAM, an 80287 math coprocessor, and a 20-megabyte hard disk. The program can run on remote terminals—away from restricted areas—and factory-floor viewers. It is completely compatible with both the mainframe and the 32-bit work-station versions, so subcontractors can swap files with corporate clients.

Micro Cadam's integrated management functions allow text, descriptions, and other related information to be attached to any element in a drawing. This lets managers track data for generating bills of materials, inventory reports, and other documentation.

The package, which includes software, a function-key box with interface card, and a three-button mouse, sells for $8,000. It is available now.
Cadam Inc., 1935 N. Buena Vista St., Burbank, Calif. 91504.
Phone (818) 841-9470 [Circle 370]

## STILL-VIDEO RECORDER CAPTURES 50 FIELDS

The ProMavica industrial video recorder captures 50 fields or 25 frames on reusable Mavipak still-video floppy disks. The system, an alternative to instant film and slides, creates picture, title, and graphics files; images can be created and displayed immediately on a monitor, with a projector, or as hard copy. Presentations can also be coordinated with other media.

The system is compatible with composite-video and analog or digital red-

green-blue signals from most popular makes of video cameras, recorders, video disks, and TV tuners. An RS-232-C port gives the user external computer control of the ProMavica.

A system consists of the recorder ($3,400), 10 video floppy disks ($100), and a program-editing controller ($1,200). A remote-control unit ($150) and video copy stand with camera ($9,850) will be offered as options with the ProMavica, which will be available in July.
Sony Corp. of America, Sony Communications, 1 Sony Dr., Park Ridge, N. J. 07656.
Phone (201) 930-1000 [Circle 372]

## FILM CAPACITOR SUITS SURFACE MOUNTING

The Inter-Technical Group's metalized plastic film capacitors, which were first introduced in chip form in 1983, are now available in surface-mountable packages. The MKS 01-SMD's electrical characteristics suit it for uses where multilayer ceramic capacitors cannot be used. The entire end surface is used as the soldering contact, and the dimensions correspond to size code 2225 for ceramic chip capacitors. Capacitance values range from 0.01 to 0.1 $\mu$F for rated voltages of 50 V. Maximum rise time is 7.5 V/$\mu$s for pulses equal to the rated voltage. The insulation resistance at +20°C is better than 3,750 M$\Omega$.

Delivery time for the MKS 01-SMD is 12 weeks and the unit price is about 10¢, depending on capacitance.
Inter-Technical Group Inc., Wima Division, P. O. Box 23, Irvington, N. Y.
Phone (914) 591-8822 [Circle 371]

## MOS FET ARRAYS SAVE SPACE

With a nominal surface area of 0.23 by 0.41 in. and a height of 0.07 in., the VN01A NE series of surface-mountable power MOS FET arrays takes up a minimal amount of space on a pc board. And because a single package holds four devices, board-insertion costs are low.

The NE series is designed for industrial and high-reliability designs that warrant the use of ceramic packages. These include display, memory, and relay driving, as well as a variety of general-purpose line-driver applications.

The arrays offer a maximum on-resistance of 3 $\Omega$ and breakdown voltages of 60 and 90 V, the latter intended for military applications. For quantities of 100 to 999, unit prices are $11.35 and $12.04 for the 60- and 90-V models, respectively. Delivery time is within eight weeks.
Supertex Inc., 1225 Bordeaux Dr., P. O. Box 3607, Sunnyvale, Calif. 94088.
Phone (408) 744-0100 [Circle 362]

*MEETINGS*

## THE ISDN TO BE CENTER STAGE AT THE ICC

The International Conference on Communications, June 22-25 in Toronto, is expanding from its traditional 48 sessions to 60, largely as a result of increasing interest in the integrated services digital networks, according to Tas Venetsanopoulos, technical chairman of the ICC.

Fourteen sessions cover ISDN, with such topics as quality assurance, satellite transmission, packet switching, reliability standards, and switching architectures. ISDN now requires "different kinds of demands for different kinds of signals," because of the advent of voice and image transmission, says Venetsanopoulos, professor of electrical engineering at the University of Toronto. Several ISDN papers will discuss approaches to technical problems, and a separate session will deal with the latest advances in image and speech processing.

Six sessions are devoted to signal processing, with one on different aspects of channel modeling. Interest in quality assurance, which had fallen off in recent years, Venetsanopoulos says, has picked up this year.

ICC organizers also experienced a disappointment, Venetsanopoulos reveals. A widely anticipated six-paper session on gallium arsenide very large-scale integrated circuits was scratched at the last minute because the companies and organizations involved would not allow the presentations. No reasons were given, he says.

Venetsanopoulos expects 1,500 to 2,000 attendees, most from the U.S., but says there will be more participants than last year from Europe and Asia.

**NCC '86:** National Computer Conference, IEEE *et al.* (NCC '86, American Federation of Information Processing Societies, 1899 Preston White Dr., Reston, Va. 22091), Convention Center, Las Vegas, June 16-19.

**Compeuro '86,** IEEE Computer Society, (1730 Massachusetts Ave., N. W., Washington, D. C. 20036-1903), Congress Center, Hamburg, West Germany, June 16-20.

**ICC '86:** International Conference on Communications, IEEE (Hugh J. Swain, Andrew Antenna Ltd., 606 Beech St., Whitby, Ont., Canada L1N 5S2), Sheraton Centre, Toronto, June 22-25.

**Computer Vision and Pattern Recognition,** IEEE Computer Society (1730 Massachusetts Ave., N. W., Washington, D. C. 20036-1903), Fontainebleau Hilton Hotel, Miami Beach, Fla., June 22-26.

**94th American Society for Engineering Education Conference,** ASEE (11 Dupont Circle, Suite 200, Washington, D. C. 20036), Clarion Hotel, Cincinnati, June 22-26.

**ATE East '86**: Automatic Test Equipment Conference, Morgan-Grampian Expositions Group (1050 Commonwealth Ave., Boston, Mass. 02215), World Trade Center, Boston, June 23-26.

**CPEM '86:** Conference on Precision Electromagnetic Measurements, National Bureau of Standards, IEEE, and Union Radio Scientifique Internationale (Norman B. Belecki, National Bureau of Standards, NBS Building, Gaithersburg, Md. 20899), NBS Building, Gaithersburg, June 23-27.

**EFOC/LAN 86:** European Fiber Optics Communications & Local Area Networks Exhibition and Conference, Information Gatekeepers Inc. (Joan Barry, Information Gatekeepers, 214 Harvard Ave., Boston, Mass., 02134), International Congrescentrum Rai, Amsterdam, June 23-27.

**1986 Power Electronics Specialists Conference,** IEEE (William Dunford, Department of Electrical Engineering, University of British Columbia, Vancouver, B. C., Canada V6T 1W5), University of British Columbia, Vancouver, June 23-27.

**Advanced Manufacturing Systems Conference,** Cahners Exposition Group (1350 E. Touhy Ave., Des Plaines, Ill. 60017-5060), McCormick Place, Chicago, June 24-26.

**Military Microwaves,** Microwave Exhibitions Ltd. (43 Dudley Rd., Turnbridge Wells, Kent TN1 1LE, England), Metropole Hotel, Brighton, England, June 24-26.

**Symposium on Electromagnetic Compatibility,** Minister of Posts and Telecommunications of the Polish People's Republic (EMC Symposium, 51-645 Warsaw 12, Box 2141, Poland), Technical University of Warsaw, Warsaw, June 24-26.

**Westex '86,** IEEE (Russell Bennett, P. O. Box 2111, Fullerton, Calif. 92633-0111), Grand Hotel, Anaheim, Calif., June 24-26.

**28th Electronic Materials Conference,** Metallurgical Society (B. W. Wessels, Technological Institute, Northwestern University, Evanston, Ill. 60201), University of Massachusetts, Amherst, Mass., June 25-27.

**Design Automation Conference,** IEEE (J. D. Nash, Raytheon Co., Bedford, Mass. 01730), Las Vegas Hilton, Las Vegas, June 29-July 2.

# Advertisers Index



## Classified and employment advertising



■ For more information of complete product line see advertisement in the latest Electronics Buyers Guide
* Advertisers in Electronics International
‡ Advertisers in Electronics domestic edition
□ Advertisers in Special DC-DC Converters Advertising Section





Circle 79 on reader service card

# ELECTRONICS WEEK

## COATING DISKS FOR LONGER WEAR

A Santa Clara, Calif., company says it has come up with an advance in thin-film memory-disk manufacture that promises longer wear and a 10% to 15% improvement in all parametric values at a lower cost than with vacuum sputtering techniques. The company, Information Memories Corp., calls its new process K-2-S. With it, the plated disk receives a protective layer by means of a wet-chemical treatment.

## TELECOM SWITCH DROPPED BY DSC

DSC Communications Corp. of Plano, Texas, has suddenly canceled development efforts aimed at capturing business in the market for advanced digital central-office switches. DSC launched its DEX 5 central-office switch last year after spending $25 million over the past two years to develop it. But now it says the market is dramatically changing, and the central-office-switch market will ultimately be replaced "by a nodal and adjunct-structured network, featuring simplified end-office switches and sophisticated network-control devices."

## MATSUSHITA SHOWS LCD POCKET TV

Matsushita Electric Industrial Co., Tokyo, is the latest of a number of Japanese entries into the liquid-crystal-display pocket TV market. Matsushita's color model has a 3-in. screen, the largest so far in that market, and will be available in July for $374 in Japan. Casio Computer recently introduced a 2.6-in. color LCD model priced at $249, and Hattori Seiko and Epson Hanbai, both Seiko group members, have 2.5-in. color models priced at $330 at current exchange rates. Those three, plus Citizen Watch, also market monochrome models priced at about $125. Casio estimates the world market for pocket TVs was 1 million sets last year and expects sales to double in 1986. Three other makers—Toshiba, Sanyo Electric, and Sharp—are expected to announce color LCD pocket TVs by the end of the year. All will be priced at about $350.

## CONCURRENT IN JAPANESE DEAL

Concurrent Corp. is teaming with Nippon Steel Corp. of Tokyo to set up a subsidiary to sell Concurrent superminicomputers in the $1 billion Japanese market. The Holmdel, N.J., subsidiary of Perkin-Elmer Corp. will own 60% of the venture, called Concurrent Nippon Corp., to be formed this month. In the first stage of operations, Concurrent Nippon will import and market only, but the venture expects to construct a Japanese plant later to manufacture the computers.

## PACT SPEEDS WAY TO VHSIC-LIKE ICs

Military and aerospace companies developing integrated circuits equivalent to those developed under Phase 1 of the Defense Department's Very High Speed Integrated Circuits program can now do so faster, thanks to an agreement between Minneapolis chip maker VTC Inc. and San Jose-based Silicon Compilers Inc. VTC will make its 1.6- and 1-$\mu$m double-level metal CMOS technologies available for Silicon Compilers' Genesil turnkey chip-development system. The companies say the arrangement will speed up insertion of VHSIC-class chips by cutting by one fourth the time usually required for layout and design.

## PIXAR GOES OEM ROUTE

Pixar, the maker of an advanced graphics computer developed to make movie special effects for the *Star Wars* movies, will broaden its focus to include a variety of image-processing markets, including medical and geophysical imaging and military applications. Last week, the company announced its first two contracts with original-equipment manufacturers Symbolics Inc., Cambridge, Mass., maker of an advanced artificial-intelligence computer, and Philips Medical Systems Inc., the Shelton, Conn., subsidiary of North American Philips Co. Pixar, of San Rafael, Calif., was purchased from Lucasfilm Ltd. by Apple Computer Inc. founder Steven P. Jobs and its own employees three months ago.

## IBM OPENS NEW CHIP OPERATION

IBM Corp. has opened one of the most advanced semiconductor plants in the world. The 648,000-ft$^2$ building, at the company's East Fishkill, N.Y., General Technology Division site, is distinguished by its stringent clean-room design and special construction to reduce the effects of vibration. That is accomplished by, in effect, making the middle of its three floors a building within a building, supported independently of the top and bottom floors.

## NASA LOSES 2ND JAPANESE LAUNCH

A second Japanese satellite communications company has switched its launching plans from the National Aeronautics and Space Administration to Europe's Arianespace. Japan Communications Satellite Co., a joint venture among Hughes Communications and two Japanese trading houses, Mitsui and C. Itoh, has canceled its plans for a December 1987 launch with NASA. It will go two months later, from Arianespace's site in French Guiana, instead. A second launch scheduled for April 1988 will still be carried out with NASA.

## 1985 ROBOT SALES SET U.S. RECORD

A strong fourth quarter helped push sales by U.S. robot suppliers to a record $442.7 million last year, reports the Robotic Industries Association, a trade group based in Ann Arbor, Mich. That's up by 33% over 1984, when robot sales totaled $332.5 million. Unit sales in 1985 were up by 21%, going from 5,136 in 1984 to 6,209 last year, the association says. Almost a third of the 1985 U.S. robot dollar volume came in the fourth quarter, when sales totaled 1,656 units worth $142.8 million. At year end, the backlog of unfilled orders totaled 2,287 units valued at $247 million.

## LAN GEAR MAKER IN VMEBUS DEAL

Communication Machinery Corp. has announced a contract with Convergent Technologies of San Jose, Calif., involving $1 million worth of ENP-10 VMEbus interfaces. Communication Machinery, a Santa Barbara, Calif., company, shipped its first local-area-network products about 30 months ago. The Convergent deal was the latest in a series of 17 in the last six months, which have totaled more than $20 million. The company specializes in LAN products that interconnect varied computer equipment.

## NATIONAL BEEFS UP SINGAPORE PLANT

National Semiconductor Corp. will invest $24 million in its Singapore plant over the next three years to increase capacity and introduce advanced packaging, software, and design. Charles Sporck, National's president, says $13 million of the total will be used for equipment to increase the 7-year-old plant's capacity 40% by 1989. Forty engineers and 150 other workers will be added to the 1,700-person workforce.

# How To Stay On Top Of The Charts.

One thing is certain. You have to present a quality image. And you have to maintain it with absolute consistency.

That's why you should look into the new Seiko Hardcopier. You can get a variety of output sizes. With strong vibrant colors and clear, sharp lines on both paper and transparency.

Plus you can get those copies in as little as 45 seconds each. For a lot less money than you thought possible.

The Seiko Hardcopier can make a hundred copies for you off-line. Because its frame buffer holds the image data and frees your terminal. You just set the quantity you want and go on working.

You even get independent image control at the hardcopier. You can change colors without changing the image on the screen. And get hardcopy or overheads that look great even if the colors on the display aren't quite right for presentation purposes.

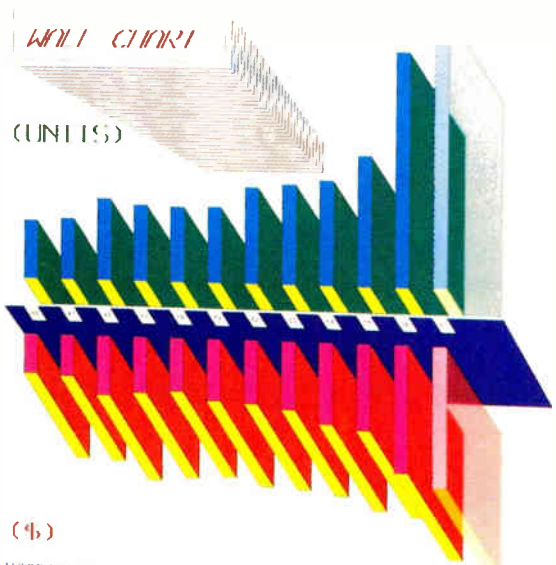
So make one phone call. We'll present you with the whole quality story. And make sure you have the hardcopier that will keep you on top of the charts.

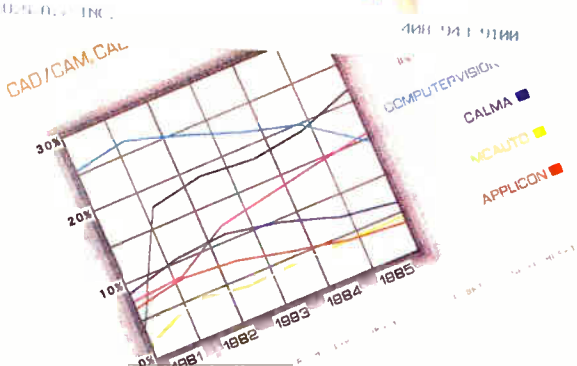
**Call Martin Nelson at (408) 943-9100 today.**

SEIKO INSTRUMENTS



Circle 901 on reader service card

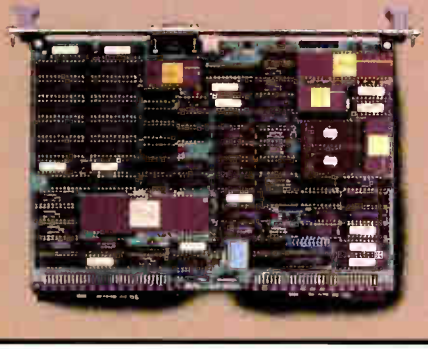




# MASTERSTROKE.

## Powerful, single board imaging and graphics systems for the VMEbus.

A requirement for high performance graphics or imaging is no longer a limitation for designers who are building on strengths of the VMEbus. Matrox has brought its video board expertise to the VMEbus with two powerful new single board products. You'll know them as the masterstroke. Call us, and you'll understand why.



### VG-640 Color Display Processor

- Versatile high level 2D/3D command set
- 640 × 480 × 8 bit resolution
- 256 colors from a palette of 262,144
- 32/16-bit display list processor
- 35,000 vectors/second drawing speed
- single VME dual height board

### VIP-1024 Real-Time Image Digitizer

- Single board input, output, storage
- 1024 × 1024 × 8 bit frame buffer
- 512 × 512 × 8 bit display resolution
- Internal or gen-lock sync capability
- 8 bit flash frame grabber
- 256 colors from a palette of 16.7 million

matrox

1055 St. Régis,
Dorval, Quebec, Canada H9P 2T4
Tel.: (514) 685-2630 Telex: 05-822798
Toll-free no.: 1-800-361-4903

Circle 902 on reader service card