WHY SILICON COMPILERS ARE STARTING TO TAKE OFF/72

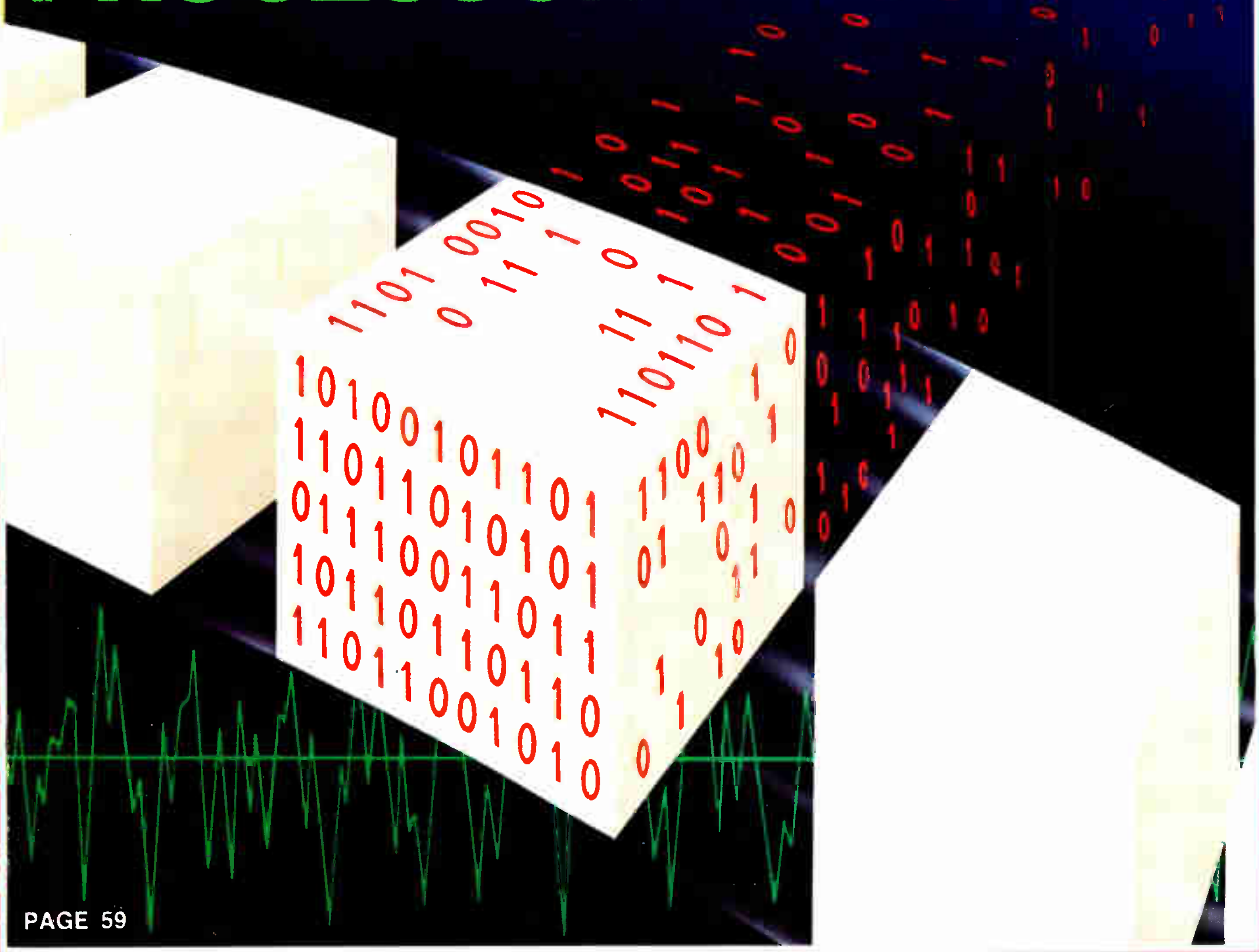
CAN TOSHIBA MAKE IT BIG IN INFORMATION SYSTEMS?/109

A McGRAW-HILL PUBLICATION SIX DOLLARS JULY 24, 1986

Electronics

A NEW CLASS OF DSP CHIP:

THE VECTOR SIGNAL PROCESSOR



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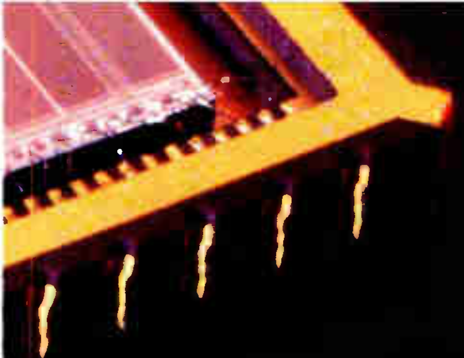

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If you're building high-speed cache or control stores, our 25ns 4Kx4 (the SR16K4, or output-enabled SR16E4) is the fastest part you can buy today. And later this year, you can upgrade to our 'A' version 64K family, offering 25ns across all organizations. We've got you covered!

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Your density-upgrade path is covered, too, with Lattice's CMOS SR256KX family. We'll have samples later this year of our 35ns SR256K1, SR256K4, and SR256K8 – matching the speed of today's products while quadrupling densities. Call us, and you'll be convinced Lattice is fast on its way to becoming your No. 1 high-speed CMOS static RAM source.

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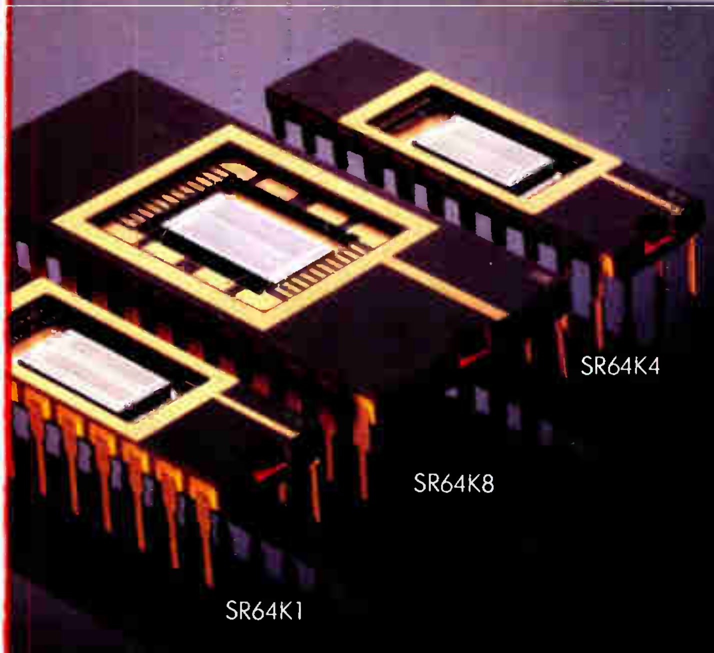
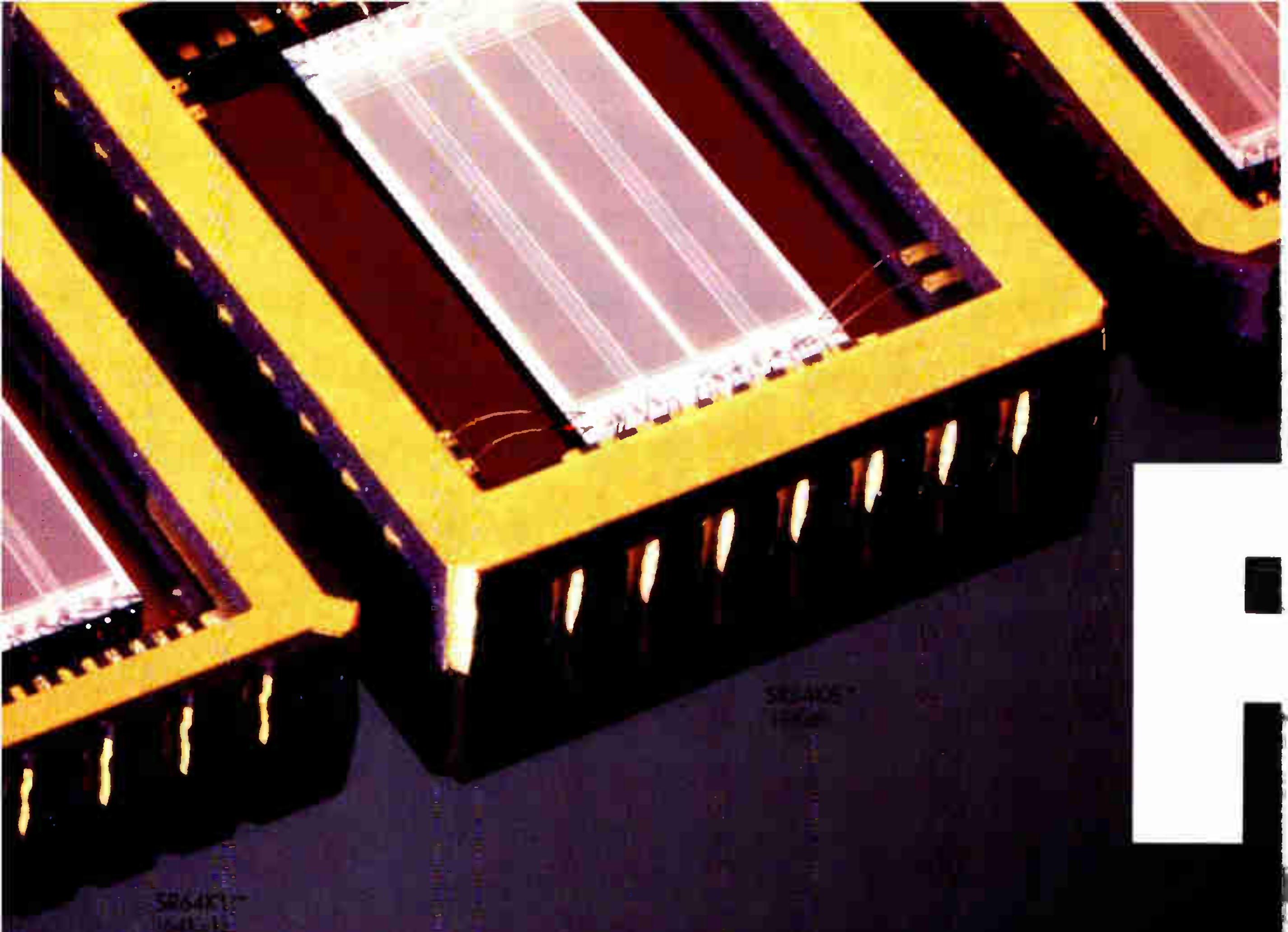


First Again.

Now…



Fast 64K

Unsurpassed Quality and Reliability
Lattice is the most experienced producer of high-performance 35ns 64K static RAMs, with more than 1,000,000 device-hours of accumulated data. That means we're the source of the most reliable product you can count on. And when it comes to quality, Lattice Quality Assurance meets or exceeds all product-assurance program requirements of MIL-M-38510, and all inspection-system requirements per MIL-I-45208. So you can be assured of the highest-quality, most reliable static RAMs available.

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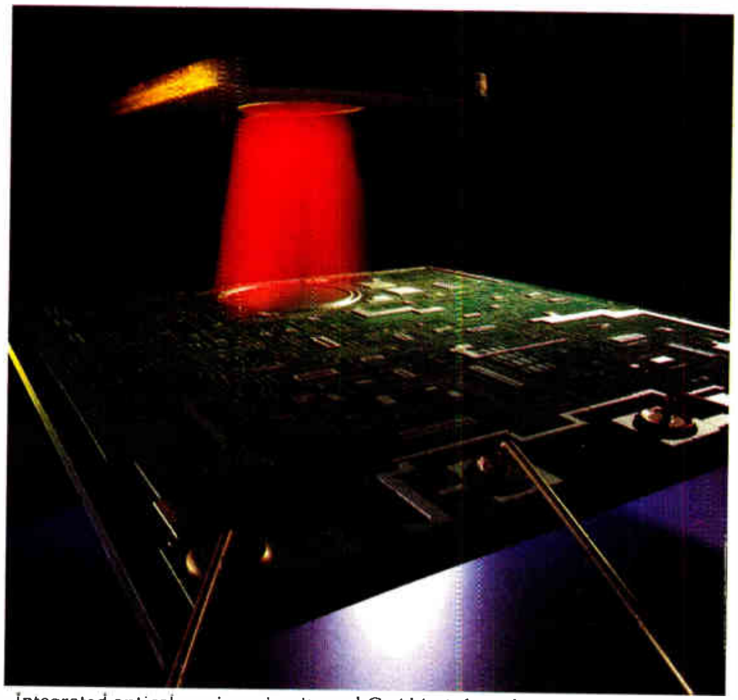
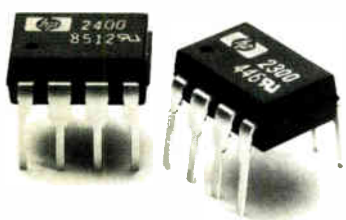
The World's Fastest Optocoupler.
HP's newest optocoupler, the HCPL-2400 with guaranteed 20 MBaud performance, brightens your future by bringing the advantages of optical isolation to today's high speed communication interfaces and local area networks. Data integrity is assured with 10,000 V/μs typical common-mode noise-immunity, and .25 mA of differential input-current hysteresis.



Integrated optical receiver circuits and GaAlAs infrared emitters within the optocoupler provide solutions for high data rate and low power applications.



Cost Saving Features.
A logic-compatible, three-state output, eliminates a pull-up resistor and permits direct drive of data busses. High power-supply noise-immunity saves cost by eliminating a bypass capacitor.

New Low Current Optocoupler.
HP's HCPL-2300 takes advantage of the high speed efficiency of GaAlAs LED's to deliver guaranteed 5 MBaud performance at only 0.5 mA drive current. In-line receiver applications and longer distances are possible due to reduced forward voltage drop across these new LED's. The HCPL-2300 is the right choice where low power and high speed are required.

Free Samples.
Just complete the coupon and HP will send you free samples of both the HCPL-2400 and HCPL-2300. For pricing and delivery information, contact your local Hewlett-Packard authorized components distributor. In the U.S., call Hallmark, Hamilton/Avnet or Schweber. In Canada, call Hamilton/Avnet or Zentronics.

For more information, call your local HP sales office. Look in the white pages of your telephone directory and ask for the Components Department.

Yes! Let me see how HP's new optocouplers can brighten my design future.
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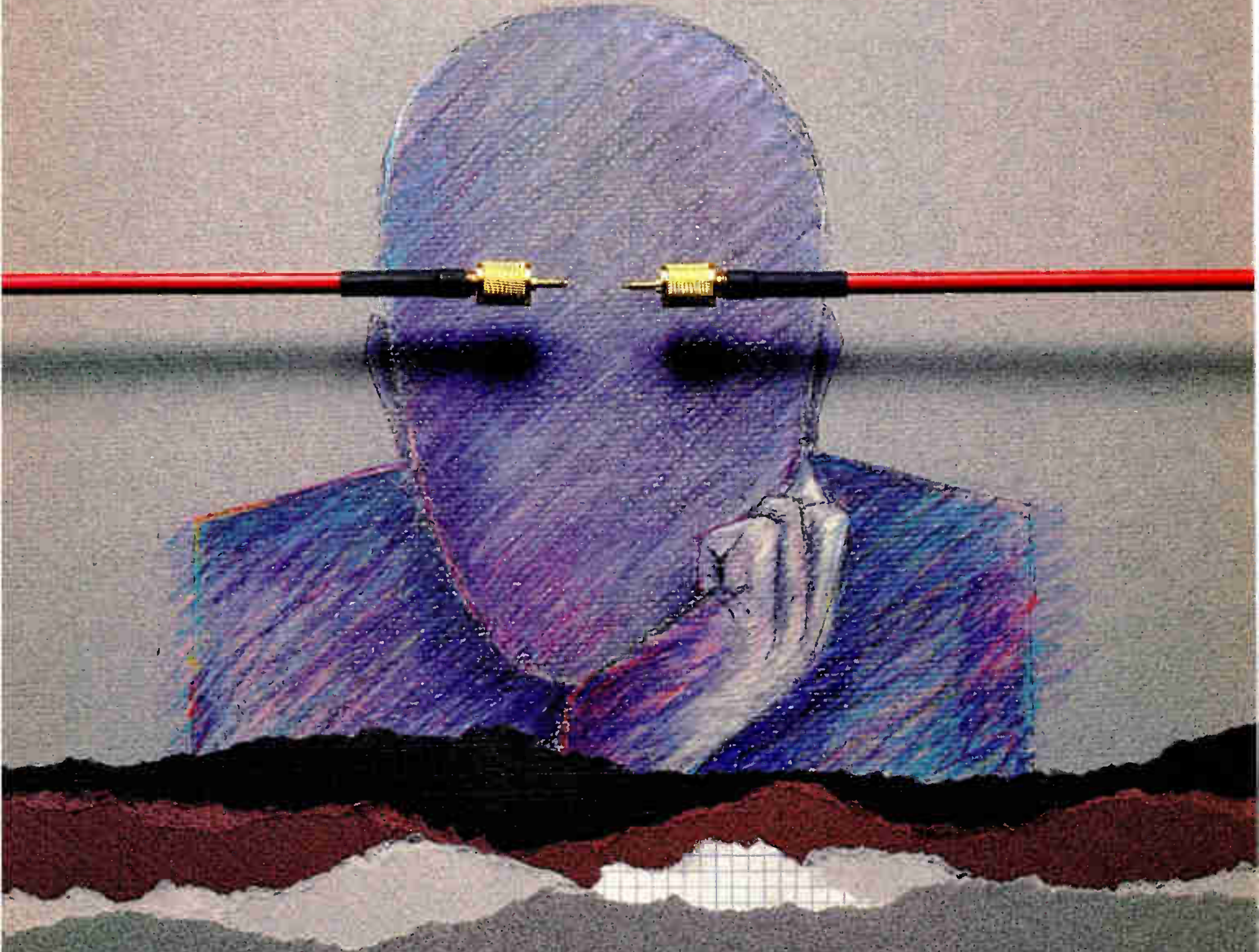

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Superior technology created to solve tomorrow's toughest interconnect problems.
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Electronics

Sometimes it pays to listen to experience. That's what Steve Zollo, our New Products editor, says, referring to his roundup on smart power appearing on p. 97.

ZOLLO: Finds the activity in smart power is overwhelming.

"When [executive editor] Sam Weber assigned the smart-power report to me, I approached it with trepidation. My reasoning was that nothing could be new—after all, we had covered the subject thoroughly less than a year ago. Well, I was wrong, and in reporting and writing the piece, I learned two things. One is that smart power is one of the most active areas in electronics today—ranking right up there with 32-bit microprocessors, digital signal-processing chips, and parallel computing. The other is to trust Sam's judgment.

"I was overwhelmed by all the activity: fully two thirds of all the companies participating in smart power have new products coming out this month or in the next couple of months." And the others have recently released new parts, he adds.

Despite all the ferment in the industry, there were some news-gathering problems. "The most frustrating thing was getting any market figures that are useful to our readers," Steve laments. "The figures varied so widely that they would have been of no help." Part of the problem, Zollo reasons, is that each company has its own definition of just what smart power is.

When Zollo isn't busy at the magazine—he also contributed four new-product stories to this issue—he takes to the skies. Zollo, a 30-year-old native of Orange, N. J., is an avid aviator who has had his pilot's license for six months. He recently completed one of his first extended flying trips, a week-long tour of New York, Vermont, and New Hampshire. "Lake Winnipesaukee [N. H.] is an absolutely breathtaking sight from the air," he says. Steve has found that "flying is like any other athletic endeavor—it takes a good balance of mental acuity and physical dexterity."

Zollo, who earned a BA in English literature from Old Dominion University in Norfolk, Va., recently bought a Cessna 152 and leases it to the Morristown, N. J., flying school where he earned his license at the end of January. "Leasing back the plane keeps my own flying very economical," Steve says.

He finds a strong similarity between flying and engineering. "As with engineering, every aviation problem involves multiple variables. Since I've learned to fly, I've gained an appreciation for the engineering discipline," he says. His next aviation challenge is to engineer a flight to Oshkosh, Wis., next month for the country's premier air show.

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Electronics

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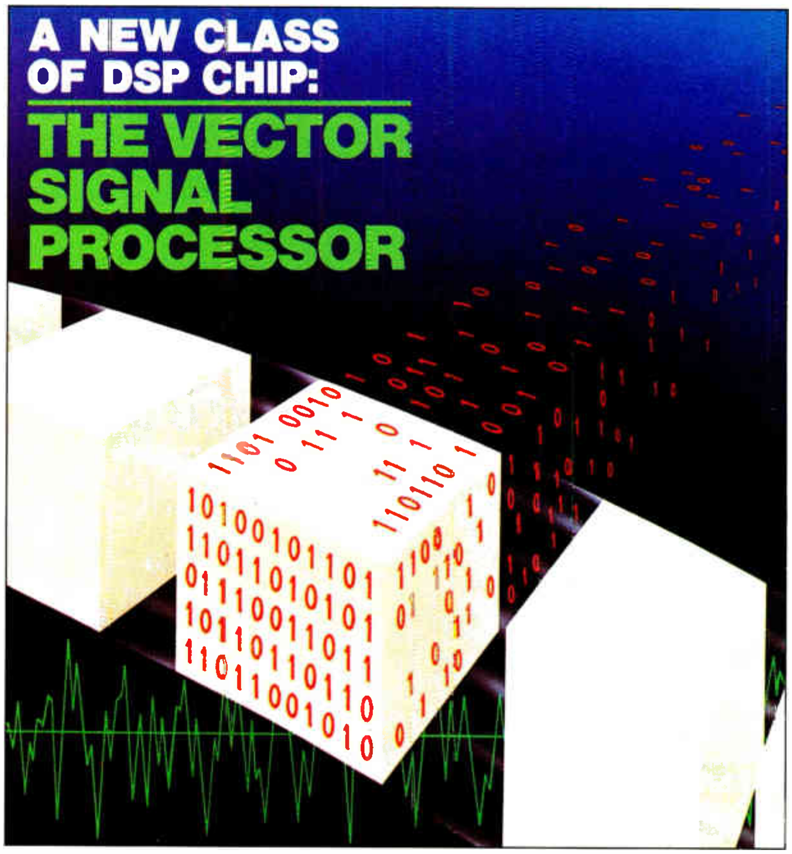

NEW PRODUCTS

DEPARTMENTS

WEEK 40

At last there's a microprocessor that's an arch conservative when it comes to power issues and a flaming liberal when it comes to high performance: AMD's Am29C117 16-bit CMOS Microprocessor. It's fast, but it only uses a frugal 25% of the power of the bipolar Am29117.

Am29C117

Cross party lines.

Get ready to save a lot of time if you're designing a pipeline system. The Am29C117 has two separate I/O ports for simplified timing, so you can achieve up to a 15% increase in throughput on a system basis over an Am29C116. A 16-bit barrel shifter allows you to shift or rotate a word up to 15 positions in a single instruction cycle.

That means you don't have to worry about extra parts or using valuable board space. It's plug compatible with the Am29117 and uses the same instruction set.

It has a 125ns microcycle time. Or an 8mHz data rate.

It's really a very simple concept. When parties cooperate, everybody wins.

Circle 151 on reader service card

WEEK 41

Usually there are lots of IC sources. With a new chip, though, there may be only one place to find it.

Until today, that's been the case with NCR's 5380 SCSI Peripheral Interface. Not anymore. Introducing AMD's 5380 SCSI Peripheral Interface. Strangely enough, it's just like NCR's. As a matter of fact, it's a plug-in replacement. (NCR's meets the ANSI Standard Committee X3T9.2. So does ours.)

5380

To have and have not.

But AMD's 5380 comes with something no one else can offer: It's the International Standard of Quality. It makes a very big promise that we keep with the 5380 and every other IC we sell. We guarantee a 0.05% AQL on all electric parameters, AC and DC, over the entire operating range. Because we think it's no use having the 5380 or any other part if it doesn't come with a promise that means something.

The 5380 with INT•STD•500. Only from AMD.

Circle 152 on reader service card

WEEK 42

AMD not only lets you beat the clock. It lets you program it your way. From delay lines to system timing. All with one very timely device: AMD's new Am2971 Programmable Event Generator.

You'll have your choice of twelve independent registered output waveforms. You'll be able to set, stop and start functions. You can schedule events down to 10ns.

Am2971

Beat the clock.

And here's your chance to stop hassling with delay lines. The Am2971 is a programmable solid state substitute. And all its functions are programmed as easily as a PROM.

To keep everything in sync, the Am2971 lets you set your own system clock, too. For accuracy, there's a multiplying phase-locked-loop oscillator. Or clock it from an external source.

When you set the timings just the way you want, you can make your system perform better. That's why we made the Am2971. Because at AMD, we know that timing is everything.

Circle 153 on reader service card

WEEK 43

Don't get us wrong. TRW's bipolar 12 X 12-Bit Multiplier Accumulator is a very serviceable product.

But when AMD decided to become a second source for the TRW TDC1009J we started by doing all the usual stuff. The Am29C509 is a plug-in replacement for the TDC1009J. Both have the same multiplier and adder in one space saving package. Both have Round Control as well as 27-Bit Product Accumulation Result to give you the luxury of extra headroom.

Am29C509

How to make a silk purse out of a sow's ear.

The similarities end there. We designed the Am29C509 in CMOS so it doesn't hog power. In fact, power needs are cut by 85%. And it gives twice the performance. Our multiply accumulation time is 70ns.

The moral to the story is that the best TDC1009J is our Am29C509; the silk purse with the built-in sow's ear.

Advanced Micro Devices has broken the game wide open.

After building a comfortable lead with a new product a week, every week—on the shelf, in volume—we called in the heavy hitters:

ISDN. CMOS. 32-bit microprocessor chip set. High-speed RAMs. Modems.

The International Standard of Quality guarantees a 0.05% AQL on all electrical parameters, AC and DC, over the entire operating range.

INT·STD·500

No one who follows the game closely is the least bit surprised. This team puts more dollars into R&D, as a percent of sales, than anyone else in the business.

If you like the sound of extra bases, call Advanced Micro Devices.

Advanced Micro Devices

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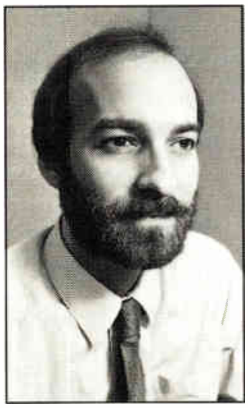
FYI

Many proponents of Ada are touting it as the solution to all software-development ills, but it takes more than a good programming language to write a program



Although I haven't written a line of code in over two years, I'm quite fond of the Ada programming language. Today Ada is speeding the development of million-line programs to process radar returns, guide missiles, or control satellite communications.

Yet when I was a software engineer, I was perfectly happy working with less advanced programming languages. That's because I believed that the skill of the individual programmer, rather than the types of languages and tools he or she used, was the key ingredient in creating well-designed programs.

In contrast, many proponents of Ada are touting it as the key ingredient to any and all problems in the software-development cycle. Indeed, when used properly, Ada can produce code that is well structured and as bug-free as is technically possible. But I still believe that, in the quest for reliable code, the answer lies not in our software but in ourselves.

Whatever the project, whatever the programming language, software engineers must learn how to cope with an environment that is often more concerned with getting a job done quickly than with getting it done right. In an ideal world, engineers and management would work to find a happy medium. Or we could simply tell the customer to wait.

Fortunately for real-world engineers, an alternative solution does seem to be on the way. It comes in the form of leading-edge software technologies. Right now, dozens of companies are pouring millions of dollars into developing advanced productivity-enhancement tools that will make it easier for software engineers to do the quality job they want to do.

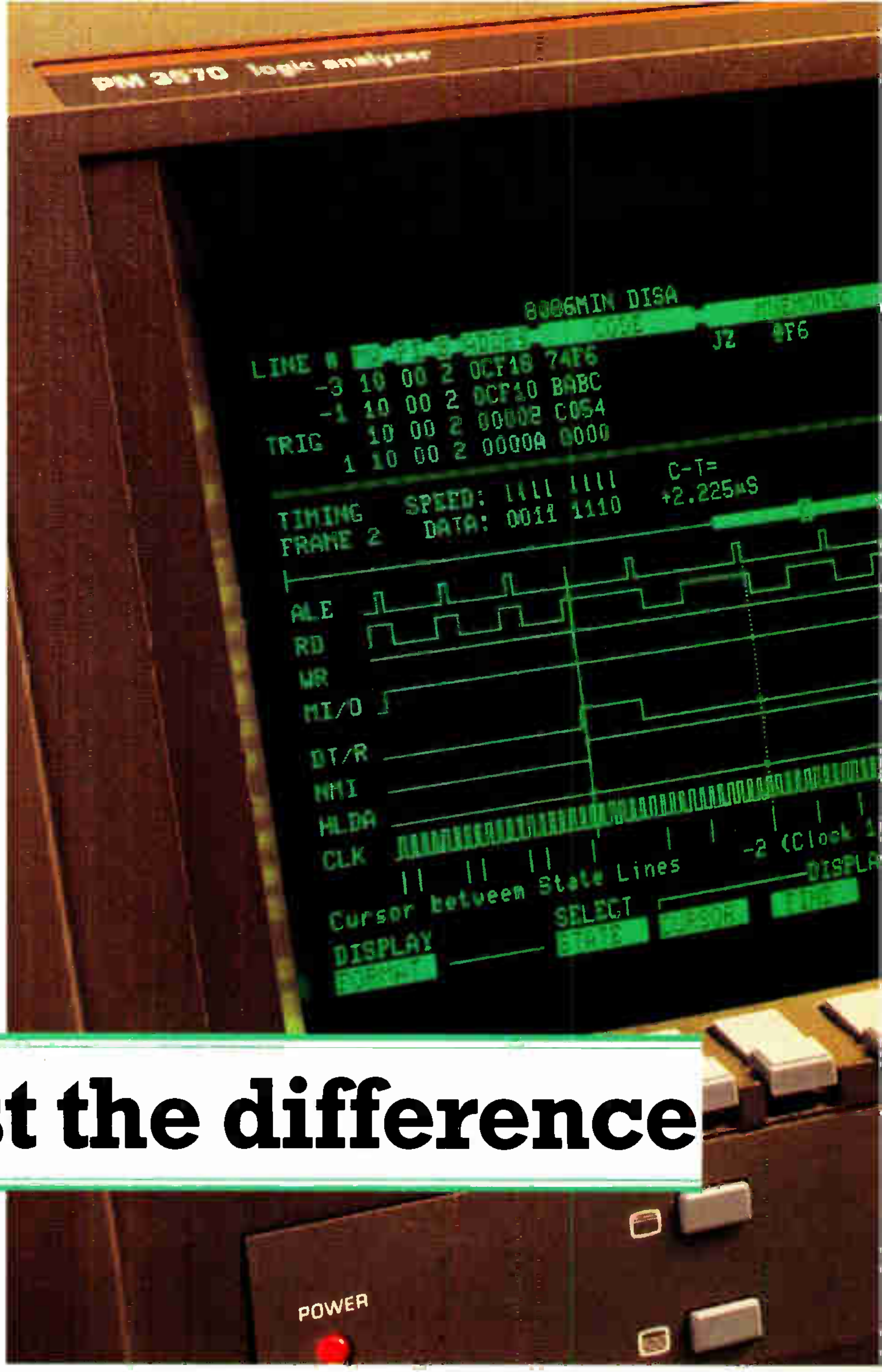
In these efforts, which make for some of the most interesting software stories *Electronics* has covered, Ada is playing a big part. No, Ada is not perfect—occasionally, assembly language is better suited to the job. But any language that is both improving the quality of our software *and* relieving some of the productivity pressure on the software engineers is itself a standard well worth settling on. **ALEXANDER WOLFE**

Software editor Alex Wolfe replaces vacationing editor-in-chief Bob Henkel as FYI author.

Double your logic analysis capability!

The new PM 3570 Logic Analyzer featuring a dual screen display, allows you to perform time-correlated state and timing analysis simultaneously, configurable to 115 channels. Built in performance analysis permits system optimization. Other special features include:

- **83 state and 32 transitional timing channels** for simultaneous, time-correlated acquisition at speeds up to 400 MHz! Or you can combine them for an unprecedented 115 channels of state acquisition.
- **Microprocessor support** for 8, 16 and 32 bit analysis plus a wide range of adaptors including: 40-, 48- and 64-pin dual-in-line (DIL) as well as 68- and 114-pin grid array and 68-pin leadless chip carrier (LCC) versions.
- **Softkey operational simplicity** for step-by-step entry, and non-volatile memory for storage of instrument set-ups and measurement data.
- **A simpler configuration** the PM 3565, handles up to 75 channels including 59 state and 16 transitional timing channels with speeds up to 300 MHz.



Test the difference

- **Product credibility** in technology, technique, quality and service is assured, because the PM 3570 is backed by the corporate resources of one of the world's largest electronics companies.

PHILIPS **Test & Measurement**

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"This is great, it's supporting their entire office."

"Like we said, our one printer would replace four of their old daisywheels."

"And do it with the same wordprocessing software they've already installed."

"Funny to think where we were just a year ago, isn't it?"

"And that we would still be there...if it hadn't been for the Series 32000."

Only one 32-bit microprocessor could deliver the performance Dataproducts needed for their new laser printer. National's Series 32000 family.

Dataproducts needed a powerful product to fill an important market.

They wanted to introduce laser-printer speeds into daisywheel environments. So they developed the LZR-2630. It prints up to 26 pages a minute, a full page at a time, on demand. Yet it's fully compatible with the enormous installed base of wordprocessing software.

The secret of such speed and flexibility is National's Series 32000* family.

The Series 32000 performs *three times faster* than its nearest competitor in this application. So Dataproducts got the throughput they needed for their ultra-fast printer's engine.

They also got a powerful set of development tools, comprehensive diagnostic systems, full applications support, and the corporate-wide commitment of National Semiconductor.

So Dataproducts met the market demand for a high-performance cost-efficient solution.

Which means the Series 32000 is not only the right *engineering* decision for today, it's also the right *business* decision for tomorrow.

Find out how you can build the future into your own 32-bit design. Contact National Semiconductor today.

National Series 32000, MS 23-200
P.O. Box 58090
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Circle 11 on reader service card

National Semiconductor

MEETINGS

30th International Technical Symposium on Optical and Optoelectronic Engineering, Society of Photo-Optical Instrumentation Engineers (P. O. Box 10, Bellingham, Wash. 98227-0010), Town and Country Hotel, San Diego, Aug. 17-22.

Siggraph '86, Association for Computing Machinery and IEEE (Siggraph Conference Management, 111 E. Wacker Dr., Chicago, Ill. 60601), Dallas Convention Center, Dallas, Aug. 18-22.

International Conference on Parallel Processing, IEEE Computer Society and Pennsylvania State University (IEEE Computer Society, 1730 Massachusetts Ave. N. W., Washington, D. C. 20036-1903), Pheasant Run Resort, St. Charles, Ill., Aug. 19-22.

3rd International Congress on Advances in Non-Impact Printing Technologies, Society of Photographic Scientists and Engineers (Samuel W. Ing, Xerox Corp., 800 Phillips Rd., Webster, N. Y. 14580), Fairmont Hotel, San Francisco, Aug. 24-28.

Interconnect '86, United States Telecommunications Suppliers Association (333 N. Michigan Ave., Suite 1618, Chicago, Ill. 60601), San Mateo Expo Center, San Mateo, Calif., Aug. 26-28.

IFIP Congress '86, International Federation for Information Processing (Philip H. Dorn, Dorn Computer Consultants Inc., 25 E. 86th St., New York, N. Y. 10028), Trinity College, Dublin, Sept. 1-5.

NCC-Telecommunications Conference, IEEE Computer Society *et al.* (Mike Sherman, 1899 Preston White Dr., Reston, Va. 22091), Civic Center, Philadelphia, Sept. 8-10.

International Test Conference, IEEE *et al.* (Peter Bottorff, International Test Conference, P. O. Box 264, Mt. Freedom, N. J.), Sheraton Washington Hotel, Washington, Sept. 8-11.

16th European Microwave Conference, Royal Irish Academy *et al.* (Microwave Exhibitions & Publishers Ltd., Convex House, 43 Dudley Rd., Tunbridge Wells, Kent TN1 1LE, England), National Concert Hall, Dublin, Sept. 8-11.

Symposium on Optical Fiber Measurements, IEEE and Optical Society of America (D. L. Franzen, National Bureau of Standards, Division 724.02, 325 Broadway, Boulder, Colo. 80303), NBS Laboratories, Boulder, Sept. 9-10.

Swissdata '86, Swiss Industries Fair (Secretariat, Swissdata 86, Postfach CH-4021, Basel, Switzerland), Fairgrounds, Basel, Sept. 9-13.

Symposium on Optical Communication Primary Standards, EIA (G. P. Watkins, Corning Glass Works MP-BH-03, Corning, N. Y. 14831), National Bureau of Standards Laboratories, Boulder, Colo., Sept. 11.

Midcon 86, IEEE *et al.* (Electronic Conventions Management, 8110 Airport Blvd., Los Angeles, Calif. 90045), Dallas Convention Center, Dallas, Sept. 9-11.

Intercomm '86: International Communications Exposition and Conference for Science and Technology, Cahners Exposition Group (CEG, P. O. Box 70007, Washington, D. C. 20088), Exposition Center, Beijing, China, Sept. 15-20.

IEEE International Symposium on Electromagnetic Compatibility, IEEE (George Ufen, GRU Associates, 1105 E. Commonwealth Ave., Fullerton, Calif. 92631), Town and Country Hotel, San Diego, Sept. 16-18.

International Broadcasting Convention, Electronic Engineering Association *et al.* (IBC Secretariat, Institution of Electrical Engineers, Savoy Place, London WC2R 0BL, England), Metropole Conference and Exhibition Centre, Brighton, England, Sept. 19-23.

Electronics and Aerospace Systems Conference '86, IEEE (Dr. Arvid G. Larson, vice president, Analytic Disciplines Inc., Suite 400, 2070 Chain Bridge Rd., Vienna, Va. 22180), Shoreham Hotel, Washington, D. C., Sept. 22-24.

Nepcon Southwest, Cahners Exposition Group (CEG, 1350 E. Touhy Ave., Des Plaines, Ill. 60017-5060), Infomart, Dallas, Sept. 23-24.

EOS/ESD Symposium: Electrical Overstress/Electrostatic Discharge Symposium (Michael E. Martin, 2111 W. Braker Lane, Austin, Texas 78769-2963), Riviera Hotel, Las Vegas, Sept. 23-25.

International Videotex Industry Exposition and Conference, Videotex Industry Association (Cahners Exposition Group, 999 Summer St., Stamford, Conn. 06906), Jacob Javits Convention Center, New York, Sept. 23-25.

IECON '86: International Industrial Electronics Conference, IEEE (Dr. Richard C. Born, Rexnord Inc., 5101 W. Beloit Rd., Milwaukee, Wis. 53214), Hyatt Regency Hotel, Milwaukee, Sept. 28-Oct. 3.

1986 Applied Superconductivity Conference, IEEE (Ms. Lahni N. Blohm, executive administrator, ASC86, Code 6630C, Naval Research Laboratory, Washington, D. C. 20375), Hyatt Regency On the Harbor, Baltimore, Md., Sept. 28-Oct. 3.

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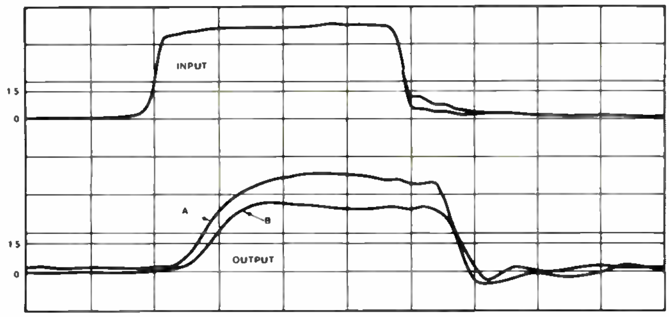
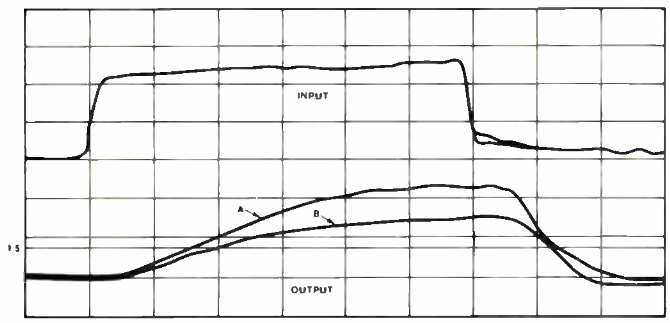


A = Performance's CMOS octal transceivers   B = Advanced Schottky TTL bipolar



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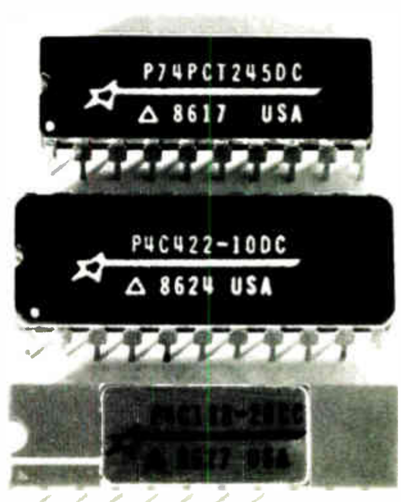

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THE MIDWEST IS THE NEXT HOT SPOT, SAYS CONWAY

CONWAY: "We may see a new breed of hackers creating mechanical, electronically controlled machines."

ANN ARBOR, MICH.

Lynn Conway has a vision about the Midwest that may ruffle some feathers in Silicon Valley and other U.S. high-technology centers. "This is just sort of personal intuition. But something is happening here that's different," says Conway, an associate dean of engineering and professor of electrical engineering and computer science at the University of Michigan.

Specifically, Conway sees the region of southeast Michigan centered in the Ann Arbor-Detroit area as the probable birthplace over the next five to ten years of what she says will amount to "a new, higher technology." Her vision, which involves machine intelligence, is based on the assumption that the Midwest—whose traditional "low-tech" mechanical-engineering image contrasts with such electronics and computer hot spots as California's Silicon Valley and the Boston area's Route 128—is now in the best position to make the concept come alive. The result, says Conway, will be a new breed of automated machinery.

IMPROVING. Silicon Valley has become "preoccupied with a dynamic but relatively narrow set of technologies—predominantly in chip design, digital design, programming—and the companies, products, and markets that you can make out of that," says Conway. By contrast, the Midwest, with its heavy manufacturing base, has been importing computer and electronics technology to improve its traditionally low-technology production techniques, design methodologies, and products.

She feels the process has now broadened to the point where the integration of electronics with mechanical technologies makes the Midwest "the region where a really new form of technology will appear and propagate quickly, as opposed to the things that might appear and propagate in the Bay Area or around Route 128."

Given the 48-year-old Conway's current position, that might at first be seen as regional puffery. But one look at her credentials as a high-technology seer, educator, and mover and shaker establishes her quickly as one whose ideas bear examination. For example, she and California Institute of Technology professor Carver Mead wrote *Introduction to VLSI Systems*, the seminal work that helped launch a revolution in very large-scale-integration design techniques. It earned them the 1981 *Electronics* Achievement Award.

Conway, who holds bachelor's and master's degrees from Columbia University's School of Engineering and Applied Science, actually began her association with Michigan while still living in Silicon Valley. In 1982, during the final stages of a 10-year stint as a system designer at Xerox Corp.'s Palo Alto Research Center, she joined the National Advisory Committee at Michigan's College of Engineering. She left Xerox in 1983 for two years with the Defense Advanced Research Projects Agency in Washington, where she was chief scientist and assistant director for the Strategic Computing Initiative.

COMMINGLING. Conway's job includes improving the school's ties with various federal and state funding agencies and with industry. Under her guidance, the university last year established a new Center for Machine Intelligence, with funding from the state, General Motors Corp.'s Electronic Data Systems, and elsewhere. And Conway says the groundwork is being laid for a significant new kind of interdisciplinary technology in the future: the commingling of disciplines such as machine vision, machine cognition, and artificial intelligence with mechanical action involving robotics that incorporate end-effectors and transducers of various new kinds.

On the academic side, too, Conway is working to help consummate the dream. She is collaborating with other faculty members in mechanical engineering, aerospace engineering, and industrial design to create what she calls a new kind of industrial design course.

A prototype version of the course was taught for the first time last fall. "Our hope is that we'll begin to produce students who can in fact do both mechanical and VLSI chip design. We may start to see a new breed of hackers who will be creating all sorts of weird mechanical, electronically controlled machines," she predicts. *–Wesley R. Iversen*

INTEGRATING AVIONICS IS A STRUGGLE, SAYS RADANT

EL SEGUNDO, CALIF.

The top item on Milton E. Radant's wish list surely reflects the priorities of most of his peers on the airborne side of military electronics. "The single thing that's most on my mind is integrated electronics," says the top technology executive at Hughes Aircraft Co.'s Radar Systems Group.

Like competing U.S. companies in this field, Hughes Radar engineers are working to blend various avionics systems such as radar, electronic warfare, and weapons control into a simplified and smaller unit with higher performance. Although the technologies involved—primarily advanced signal processing, computing, and sensing devices—are at hand, the integration challenge is daunting, notes Radant, a veteran engineer who is now the group's vice president and director of technology. "It's several years away yet," he says.

Hughes failed to nab the premier project in this field—the Phase 1B risk-reduction contracts for the Air Force/Navy Integrated Electronics Warfare System that went to TRW-Westinghouse and General Electric-Sanders Associates in late June. But the effort has spurred a research involvement that must continue, says Radant.

Radant, 54, joined the company in 1954 with his shiny new BSEE degree from the University of Illinois and has since added an MSEE from the University of California, Los Angeles. After starting in general engineering, he worked in computer design and signal

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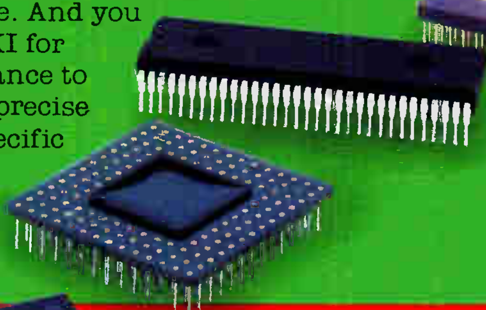

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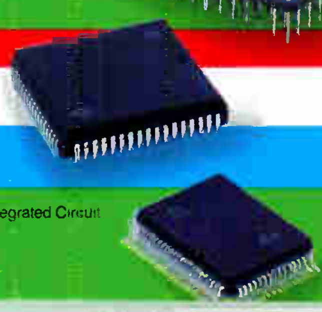

TURN THE PAGE FOR FAST ACTION.

*Customer-Specific Integrated Circuit

RADANT: He aims to make Hughes Radar a major player in airborne EW.

analysis and processing for missiles and radar before turning full attention to the Radar Division (it was not then a group) in 1969.

He rose rapidly to the uppermost levels at Hughes Radar, a group now made up of seven divisions that do well over a total of $1 billion of business a year. Among his earlier posts were manager of the signal-processing laboratory and associate manager of the Advanced Products Division.

MODULAR SOLUTION. The focus of internal research and development today is to improve digital signal processing, which is central to the radar product line. Not only is the group going for ever-faster processing speed, but it is also looking to package the hardware to fit into existing radar equipment for upgrading. A new modular signal processor, whose successful development was guided by Radant, fills this bill on both counts. At full throttle, it operates at up to 50 million complex operations per second (mcops), or it can be used in smaller modular chunks. By comparison, earlier DSP systems worked at 7 mcops.

Radant was named in April to his new post, which carries widened responsibilities for long-range planning. He is working to establish the Hughes operation as a major player in airborne electronic-warfare equipment. Building such units as jammers and countermeasures pods requires DSP and analog-to-digital conversion technologies that Hughes employs in radar work.

"We see these as the key to making more effective EW systems," he says. And he is confident that a number of update programs "are ripe for application of these technologies."

Like many dedicated engineers who are promoted to executive posts, Radant misses the hands-on work. But, he says, the heavy technical content of his job "still keeps me in pretty close touch with the technology." *–Larry Waller*

ELECTRONICS NEWSLETTER

TI FIRES FIRST SHOTS IN A WAR OVER ADVANCED CMOS LOGIC PINOUTS

A pitched battle over pinouts for advanced CMOS logic is in the offing. Texas Instruments Inc., which has allied itself with Dutch giant Philips and its U. S. chip-making subsidiary, Signetics Corp., has fired the first shots by adopting a new pin layout for its forthcoming 1-mm chips. Rejecting the pinout that has been an industry standard for two decades, the Dallas company has adopted a design that moves the ground and V_{cc} from the ends and puts all the outputs on one side of the package with ground pins at the center, and all the inputs on the opposite side surrounding the V_{cc} pins. What's more, ground and V_{cc} pins have been doubled up for some chips. TI says the layout holds down the noise-voltage spikes that occur when multiple outputs are switched simultaneously in fast-running logic. Already strong opposition to the proposal has surfaced. Peyton Cole, corporate director for strategic marketing at Fairchild Semiconductor Corp., Cupertino, Calif., insists that the cost of redesigning boards for the new pinout would be too high for the speed advantage the 3-ns TI chips offer. He adds that TI's pinout alterations "in no way change what happens [with noise spikes] at board level." Fairchild has started delivering its own FACT line of advanced CMOS logic with the standard pinout.☐

STARTUP DANA TO DEBUT A 6-MEGAFLOPS DESKTOP NUMBER CRUNCHER

A work station under development at Dana Computer Inc., the six-month-old startup directed by Convergent Technologies founder Allen H. Michels, will be a massive number cruncher capable of near-Cray performance on a single-user desktop. Insiders say the new Titan will contain three or more processors, each consisting of a scalar and a vector chip plus cache memory. It is designed to perform at 6 megaflops on the double-precision Linpack benchmark tests developed at Argonne National Laboratories. Scalar performance will be from 10 to 30 mips. The Titan will have a radically new architecture in which the 50-million-pixel/s display is integrated with the central processor unit. The scalar engine will be a new 16-MHz reduced-instruction-set-computer chip from MIPS Computer Inc., San Jose, Calif. All the chips—both gate arrays and full custom designs—will be CMOS. The Titan will have from 8 to 128 Mbytes of memory, accessible at 200 Mbytes/s. The Sunnyvale, Calif., company will begin shipping the Titan in the fourth quarter of 1987, with a basic version selling for $75,000. ☐

CHIP SNAFU LEAVES ETA^{10} A LTTLE SHORT

A semiconductor glitch may make some versions of the ETA^{10} supercomputer from ETA Systems Inc., St. Paul, Minn., look more like an ETA^{7}. The name ETA^{10} refers to the projected peak operating rate of 10 gigaflops per second. But timing problems in some of the machine's 20,000-gate CMOS arrays mean that early versions will have a peak of about 7 gigaflops for a full eight-processor machine. ETA says the blame does not lie with chip supplier Honeywell Inc., but rather is the result of overly aggressive original specifications. The first unit will be delivered around year-end. ☐

TI BORROWS DRAM TECHNIQUE TO REDUCE SRAM CELL SIZE

Texas Instruments Inc., one of the staunchest proponents of silicon technology driven by dynamic RAMs, is taking its time entering the crowded race for the fastest CMOS static random-access memories. In fact, a product is at least a year away, but the wait may be worth it. Using a titanium silicide process borrowed from TI's 1-μm DRAM process, researchers say they can reduce the size of six-transistor cells to roughly that of the less reliable four-transistor cells. ☐

ELECTRONICS NEWSLETTER

HALF-INCH TAPE CARTRIDGES CLOSING IN ON REEL DRIVES

Cartridge drives using half-inch magnetic tape have been gaining on the reel drives that for years have been a mainstay storage medium for big computers. Now a crossover is in sight, says the authoritative magnetic-tape industry watcher, the Freeman Report. By 1988, more cartridge units than reel drives will be shipped, and by 1990 the total value of the cartridges shipped will surpass that of the drives, the report says. Worldwide market value for the cartridges in 1990 will exceed $1 billion at prices paid by original-equipment manufacturers; for reel drives the figure will be $696 million. That means a compounded annual growth rate of 31% from 1985's sales of $279 million, notes the report, published annually by Freeman Associates Inc., Santa Barbara, Calif. □

THE UPGRADE TREND CONTINUES IN PARALLEL COMPUTING

Parallel computing is entering its next generation of performance, as many manufacturers upgrade individual central processing units with faster processors and memories that have increased capacities. Flexible Computer Corp. of Dallas and Sequent Computer Systems Inc. of Beaverton, Ore., have already doubled the performance of their systems; now Elxsi, the San Jose, Calif., subsidiary of Trilogy Ltd., is weighing in with a major performance increase in its 6400 minisupercomputer. A new high-speed processor can double the performance of the system, which now runs at 4 to 40 mips depending on the number of processors, and internal memory can be quadrupled to a maximum of 768 megabytes. Shipments of the System 6400 machines with the new parallel-processing configuration will begin in October; the price ranges from $399,000 to $3 million. □

VOICE TRANSMISSION HITCHES A RIDE ON METEOR TRAILS

Engineers long ago figured out how to use the ionized trails left by meteors for Morse-code communication by bouncing signals off them. But for years, they have been stymied in efforts to use the narrowband meteor trails—which can send signals over the horizon and are difficult to jam or intercept—for wideband digitized voice. Now GTE Corp. reports that by transmitting the speech signals in tightly compressed bursts, it has demonstrated what it calls the first meteor-trail transmission and reception of voice radio signals. The Strategic Systems Division in Westboro, Mass., has compressed digitized voice data from 4 Kb to 16 bits by using an artificial-intelligence waveform-recognition matching approach and then assigning numbers to the words in the matching dictionary. The trails last for periods of a few milliseconds up to 2 seconds and typically occur at intervals of several seconds to a few minutes. GTE reports transmitting about 600 words in a single trail. □

BOOK-TO-BILL IS DOWN BUT OUTLOOK IS UP, SAYS GNOSTIC

Despite precipitous losses in earnings for leading chip makers and a book-to-bill ratio that fell last month to its lowest level since January, Gnostic Concepts Inc., a San Mateo, Calif., market researcher, detects a hint of rose in the semiconductor future. The book-to-bill fell from 1.10 in May to 1.07, the second monthly decline in a row. But Gnostic says that by itself, the ratio is an inadequate predictor; its own industry supply/demand curve derived from a host of macroeconomic factors continues to show an upturn. "The outlook for semiconductor billings and the industry in general shows strong signs of improvement," says Gnostic analyst Terry Wong. That's good news for chip makers Intel Corp. and Advanced Micro Devices Inc., both of which suffered losses in the second quarter (see story, p. 154). □

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IMS1600 64K x 1	45,55,70	440	77 CMOS	CMOS
IMS1620 16K x 4	45,55,70	440	77 CMOS	CMOS

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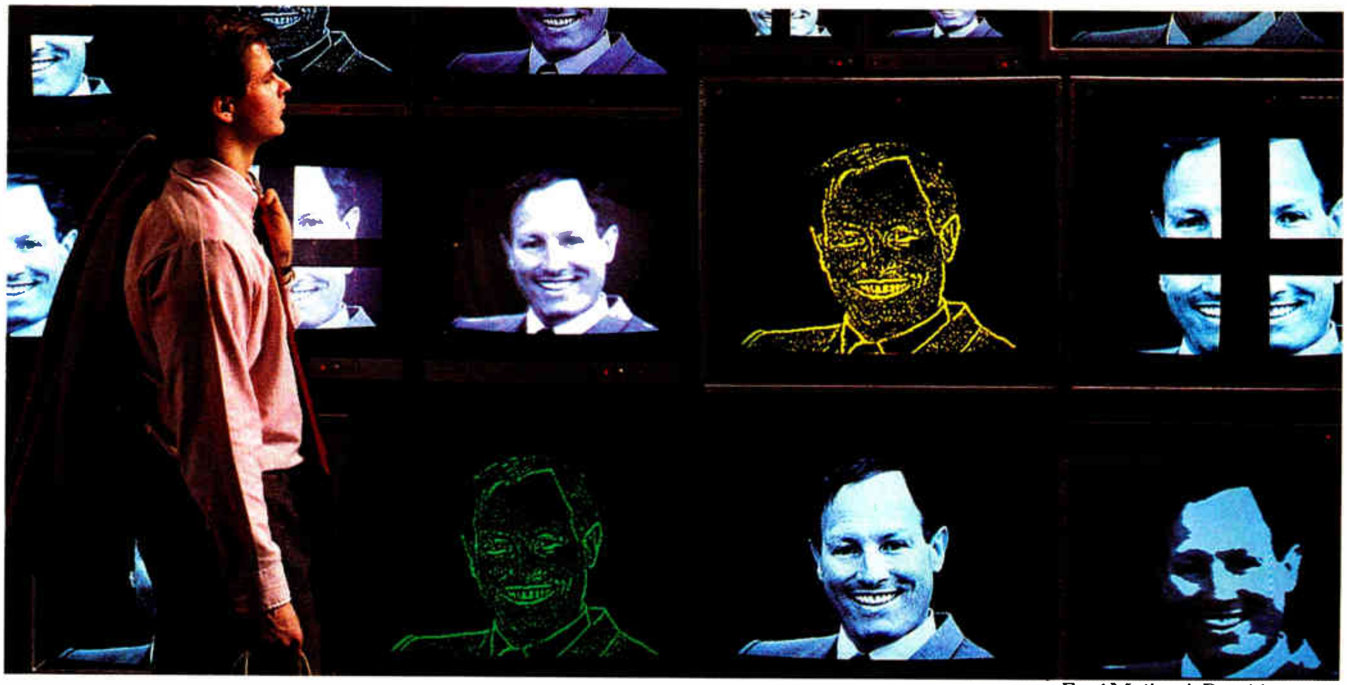

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DT2851 + DT2858 High Resolution Frame Grabber and Auxiliary Frame Processor	IBM PC AT	512x512	256			Yes	8*			2 buffers, 512x512x8 each (512 Kbytes), and 1 buffer, 512x512x16 (512 Kbytes)	Yes	Yes	Yes	Yes	DT-IRIS	DT2851 $2995 DT2858 $1695
DT2603 Low Cost Frame Grabber	MicroVAX II	256x256	64				4			1 buffer 256x256x8 (64 Kbytes)					DT-IRIS	$1895
DT2651 + DT2658 High Resolution Frame Grabber and Auxiliary Frame Processor	MicroVAX II	512x512	256			Yes	4			2 buffers, 512x512x8 each (512 Kbytes), and 1 buffer, 512x512x16 (512 Kbytes)	Yes	Yes	Yes	Yes	DT-IRIS	DT2651 $2995 DT2658 $1895

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PRODUCTS NEWSLETTER

INFERENCE BOOSTS PERFORMANCE OF ITS EXPERT SYSTEM . . .

Los Angeles-based Inference Corp. has a new set of enhancements that speed and enrich its Automated Reasoning Tool, an integrated set of software development tools for expert systems. Version 3.0, which comes out this week, reduces the amount of memory-management overhead, combines object-oriented and rule-based programming, and allows compilation of the source files of rules. Lisp, the language in which ART 3.0 is written, handles memory management, and so an application program will pause while the memory-management routines do garbage collection—tossing out stale data to free up memory. Inference has figured out a way to reduce garbage-collection time by 99%, but it will not give details. ART 3.0 also integrates rule-based methods and object-oriented programming, so users can now do object-oriented programming using both rules and procedures. To speed up expert systems built with ART 3.0, the Inference engineers enriched the rule-joining mechanism to allow rule joins from the right as well as from the traditional left. In addition, they boosted run-time performance by allowing source-rule files to be compiled into binary files that do not have to be compiled every time they are loaded. Preliminary tests show that ART 3.0 performs up to three times faster than ART 2.0. □

. . . AND ADDS VERSIONS FOR SUN AND DEC MACHINES

Inference also is making ART 3.0 available on Sun Microsystems Inc.'s Sun-3 work station and Digital Equipment Corp.'s VAX family. Until now, ART has been available only for use on Lisp-based machines from Lisp Machines, Symbolics, and Texas Instruments. The Sun version of ART will run under Sun Common Lisp, with a special front-end graphics interface that supports windowing and drawing. ART 3.0 for Lisp-based computers can be licensed for $65,000; for Sun and DEC computers, the price is $45,000. All versions are available now. □

VMEBUS CARD FROM XYLOGICS HOLDS SIXTEEN 9.6-KB/S I/O PORTS

Xylogics Inc. is jumping into the market for VMEbus communications controllers with a device that boasts a full 32-bit data path and the ability to support 16 full-duplex asynchronous ports at 9.6 kb/s or 8 ports at 19.2 kb/s. The Xylogics 780 controller can also emulate teletype systems, reducing the amount of character I/O processing that the host system must perform. Contained on a dual-height Eurocard, the 780's serial I/O processor connects the ports to a multiuser VMEbus-based host computer. All drivers and receivers are located on the 780 card, allowing the use of any type of distribution panel. The Burlington, Mass., company will also provide software for both Unix 4.2bsd and System V. Available now, the controller sells for $2,485 in single units. □

ADDS TERMINAL HAS 70-Hz REFRESH RATE TO REDUCE FLICKER

Applied Digital Data Systems Inc.'s 2020 ASCII terminal comes with green, amber, or white phosphors and boasts a 70-Hz refresh rate. That's 10 Hz higher than competitive terminals and helps reduce flicker and keep the picture sharp in the reverse-video mode, in which amber and white screens operate. The Hauppauge, N. Y., company's smart 14-in. terminal includes such features as 480 bits of RAM for each of 16 programmable keys, a pop-up calculator, and an optional DIN connector that lets it be used with keyboards from personal computers. ADDS says the reduced flicker should boost demand for the soft white displays, which have black characters on a white background. The 2020 is available in sample quantities for $695. □

PRODUCTS NEWSLETTER

HP'S VECTRA PERSONAL COMPUTER WILL GO INTO THE FACTORY

Look this fall for Hewlett-Packard Co. to introduce a version of its Vectra computer that can withstand harsh industrial environments. The Palo Alto company says more than 50 manufacturing software packages have already been tested on the IBM Corp. Personal Computer AT-compatible Vectra. Because AT&T Bell Laboratories' Unix operating system is gaining ground in factory automation, the new Vectra will also support Xenix, the popular Microsoft Corp. version of Unix. The Intel Corp. 80286 microprocessor, heart of the Vectra, supports both PC-DOS and Unix. The ruggedized machine will sell for around $6,300, about twice the price of the office version. A factory-grade enhanced graphics display will also be available for the computer. □

FAST COMPARATOR AIDS LINEAR SIGNAL PROCESSING

A comparator from VTC Inc.—the fastest yet to hit the market, the company claims—will make it easier to design systems that require high-speed linear signal processing. The Bloomington, Minn., company's VC7695 features guaranteed propagation delays of 1.9 ns from 0°C to 75°C and 2 ns for its military-grade parts. VTC specifies typical delays as 1.4 ns, in contrast to such competing parts as the AD9685 from Analog Devices Inc., which has 2.2-ns delays at 25°C. The VC7695 owes its speed to a 2-μm ECL process that jacks up the transistor transition frequency (f_t) to 6 GHz. The VC7695 is available now for $10.25 each in lots of 100. □

TI'S 24-PIN FAST PALs DON'T SACRIFICE POWER FOR SPEED

Texas Instruments Inc. is introducing four 15-ns, 24-pin programmable-array-logic devices that don't sacrifice low power consumption for the fast switching speeds. The PALs, with typical propagation delays of 10 ns, are fabricated in TI's 2-μm oxide-isolation bipolar technology, known as Impact. The TIBPAL20 series of devices is compatible with 15-ns PAL parts from Monolithic Memories Inc. But at 180 mA, the TI chips have a power dissipation that is 30 mA lower than MMI devices. The chips cost $6.50 each in 1,000-piece quantities. □

EMULEX TARGETS DEC USERS WITH ITS 1.2-GIGABYTE OPTICAL DISK DRIVE

Users of Digital Equipment Corp. computers with the VMS operating system can boost their system's storage capacities with an optical disk drive from Emulex Corp. A single 1.2-gigabyte optical platter is equivalent to about 26 magnetic tapes, according to the Costa Mesa, Calif., company. The LX400 optical drive connects to the DEC Q-bus and Unibus systems using Emulex's host adapters for the Small Computer System Interface. The optical drive is microprocessor-controlled, boasts a sustained data-transfer rate of 250-K bytes/s, and comes with software to serve as a disk file system. Prices range from $17,000 to $31,000. □

CIMLINC SLASHES THE ENTRY-LEVEL COST OF CIM

Cimlinc Inc. next week will introduce a modular work station that will slash by two thirds the price of entry for a complete computer-integrated-manufacturing system. The 68020-based Power Cim work station from the Elk Grove Village, Ill., company sells for $15,995 and comes equipped with a 19-in. monitor, 4 megabytes of RAM, an 86-megabyte disk drive, and Cim Cad, the company's computer-aided-design software. Power Cim is available immediately. Additional software for complete communications and design-to-factory-floor CIM capability is priced from $1,495 to $12,495. □

Electronics

REVIVED TRANSISTOR STRUCTURE LOWERS COST OF BIPOLAR VLSI

BENEFITS INCLUDE HIGHER DENSITY AND GREATER REPRODUCIBILITY

FREIBURG, WEST GERMANY

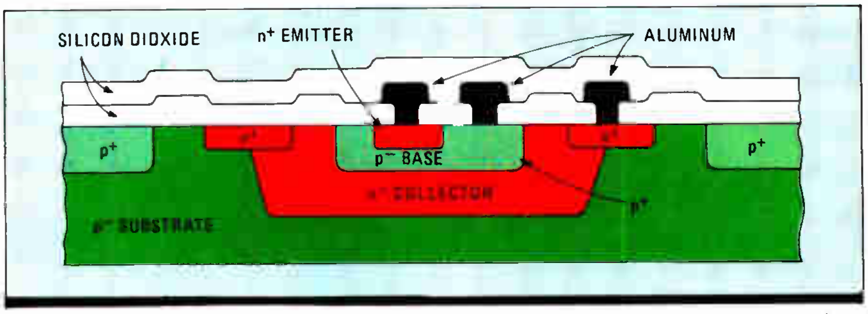
Intermetall GmbH has successfully dusted off a quarter-century-old, almost forgotten technology. Intermetall's new approach builds a device resembling one made by the old method, which diffused an npn transistor's collector region into a boron-doped substrate. It departs from the old diffusion process by using collector implantation (CI). The company says it can make high-performance bipolar integrated circuits cheap enough to use in high-volume consumer products.

Though simple, the old technology did not go far in the late 1950s because it was difficult to control the diffusion processes, explains Lothar Blossfeld, manager of the company's bipolar R&D Laboratories. That translated into poor transistor performance, a result of parasitics, latchup effects, and high collector series resistances. Implantation techniques that could have produced better devices were unknown when diffusion-based transistors were developed.

It is just such implantation that Blossfeld's team is applying to rescue the scheme, which was developed and used by Fairchild, TRW, and other manufacturers for a short time before epitaxial methods for transistor fabrication appeared on the scene in the early 1960s. Intermetall's method is a fully implanted process using only five masking steps and one surface-protection mask. This simplicity lowers fabrication costs.

GOOD FOR VLSI. The CI process lends itself to very large-scale integration of digital and analog functions on the same chip. Particularly easy to integrate, Blossfeld says, are high-speed analog-to-digital and digital-to-analog converters, low-noise operational amplifiers, fast logic chips, and temperature-stable voltage references. Intermetall has already added such CI-based circuits to video recorders, TV sets, and video codecs.

Compared with conventional bipolar techniques, the CI process builds circuits with higher packing densities, lower defect rates, and greater reproducibility. Reproducibility is especially important for obtaining the matched transistor pairs needed to make flash ADCs.



BACK AGAIN. Modern implantation techniques have made a 25-year-old npn transistor structure practical to fabricate. Transistor characteristics are highly reproducible.

Synchronous and identical transistor behavior is crucial for achieving high resolution at a given voltage variation of the input signal for such circuits.

CI-based parts can boast lower noise and higher speed than MOS devices. Intermetall has already made devices with 1.5-GHz transition frequencies, which makes possible the design of logic circuits that run at up to 500 MHz. Another advantage is lower logic levels, which means less switching noise.

The Freiburg division of the ITT Semiconductors Group is not alone in using the CI process. A similar one has been developed by TRW Inc., which calls its process 3D, for triple-diffused. But these parts are said to be expensive and therefore limited to military and other special applications.

Intermetall's fab process starts by implanting phosphorus ions into a boron-doped silicon substrate to form the collector zone. Next, a boron double-implantation step creates the base—the first implantation serving to adjust the transistor's current gain and the second to improve its dc performance. Then the emitter and the collector contact are formed through arsenic implantation. Finally, the contacts are opened and the metalization and surface-protection layers applied.

BLOSSFELD: VLSI chips are easy to integrate with CI process.

The implantation steps eliminate the need for the high-temperature processes typically used in bipolar techniques for collector-zone isolation. Thus the CI process precludes crystal defects, wafer distortion, and high defect rates. That, in turn, spells good fabrication yields.

The penetration depths of the pn junctions are very small—0.3, 0.5, and 2.5 μm for the emitter, base, and collector, respectively. Therefore, the lateral spacings of the transistors may also be small, if high voltages are not required.

SMALL AREA. The transistor's surface area is roughly 20 by 30 μm, about 1/14th that of conventional bipolar transistor structures. That means up to 600 gates can be integrated on 1 mm^2 of silicon. The emitter is 4.8 μm wide, and the contacts measure only 2 by 2 μm.

Because the emitter is highly doped with arsenic, the transistor produces an extremely linear current-gain curve. The device can operate over a current range of more than six orders of magnitude—for example, from 1 mA to 1 nA—without a change in dc current gain. This behavior is important for the accuracy of current sources in DACs operating in binary gradations.

The arsenic emitter also makes for low internal transistor noise, the noise factor being as small as that of specially selected low-noise discrete transistors. Furthermore, the transistor has no burst noise. Its thin base region and small emitter geometry make the device very fast—it can operate at up to 600 MHz.

Digital emitter-coupled logic gates with a power-delay product of 0.3 to 0.5 pJ are possible. The offset voltage varies by only ±0.25 mV over 25°C to 175°C and over a current range of more than six orders of magnitude.

Blossfeld expects that within a few years, VLSI circuits that can handle frequencies as high as 1 GHz will be on the market. In fact, his team is already working on small-geometry devices with transition frequencies approaching 5 GHz. *–John Gosch*

ARTIFICIAL INTELLIGENCE

CHILDREN'S COMPUTER BRINGS AI INTO THE HOME

TOKYO

Recent advances in logic-programming languages and processor and peripheral chips are making artificial-intelligence applications practical in the low-end home computer market. The first product that will seek to prove this point is the AI Computer, which Sega Enterprises Ltd. of Tokyo will start selling in Japan next month for $547.

The Sega AI Computer is built to run programs written in the Prolog AI language. It is strongly oriented toward computer-aided-instruction, especially for children, rather than the catchall hobbyist-to-professional target of other home computers. Perhaps its simplest AI application is a personal diary program that can be used two ways: in a simple word-processing mode for children with some writing facility and in a prompt mode.

In the prompt mode, the child is asked about his or her activities during the day and replies with one- and two-word answers. The computer program then writes a grammatically correct diary entry based on those replies.

In more advanced CAI applications, the computer is more flexible than previous systems. It can parse a user's natural-language inputs and evaluate the person's ability level. It can then proceed to material of appropriate difficulty, rather than simply advancing one level at a time.

The success of the AI Computer will depend almost totally on the software available for it, and Sega has already forged ties with the educational community to develop courseware for 3- to 8-year-olds. Its partner in this endeavor is general trader Marubeni Corp.'s Visual Information Section, Corporate Development Department, Tokyo, which is working with various educational organizations to create the programs.

Sega plans to work also with Linguaphone Institute (Japan) Ltd., Tokyo, to develop English-language instruction programs. Courseware in English should be ready next year, and the Sega AI machine then will be introduced in the U.S.

Rather than employing the Basic-language interpreters of most personal computers, Sega's AI machine uses a run-time Prolog-language interpreter residing in 128-K bytes of read-only memory. The Prolog interpreter is for running applications only—it cannot be used for programming. The company chose the Prolog AI language because of its ability to handle unformatted input and to parse natural-language input. Prolog is not especially suitable for driving displays and controlling peripherals, so Prolog functions call up fast, efficient assembly-language subroutines for these tasks.

AI FOR THE MASSES. Sega's AI Computer will run computer-aided-instruction software written in Prolog.

ENHANCED MATH. Sega Prolog was developed jointly with CSK Research Institute, the AI lab of software house Computer Services Corp., Tokyo. In addition to the assembly-language calls, the language's mathematical performance was enhanced for the AI Computer.

The computer's hardware is designed for high performance at low cost. It is built under contract by Nippon Gakki Co., Shizuoka, a leading maker of MSX-compatible computers and electronic musical instruments. The microprocessor is NEC Corp.'s V-20, an enhanced version of the Intel 8088 implemented in CMOS. The Prolog interpreter is stored in 128-K bytes of read-only memory, and main memory is 128-K bytes of dynamic random-access memory. Video memory is 64-K bytes of DRAM, expandable to 128-K bytes. A Centronics-compatible printer interface is standard. The system's power supply has sufficient capacity to run an optional 3½-in. floppy-disk drive. The machine also comes with a tape recorder for digital input or natural-language audio output, and an eight-direction cursor controller.

The Sega AI Computer has a tablet on its sloping upper surface that takes overlays for various applications. One that will be used in many children's programs is a Japanese-language touchpad, which includes all phonetic-syllabary characters along with variations annotated with one of two standard marks. The technique was designed to meet the needs of young users, who might not be adept at using a traditional Japanese keyboard where the operator strikes character and mark-only keys in succession to obtain the desired syllable.

For older children and adults, the computer also provides the new Japanese industrial-standard keyboard, which fits on top of the tablet to save desk space. Applications programs are usually supplied as plug-in ROM cards with a capacity of up to 128-K bytes, although the built-in cassette tape recorder and optional 3½-in. floppy disk drive can also be used.

ROM versions of Basic and Logo are available for users who want to write programs in those languages. A 128-K RAM expansion kit and a 128-K RAM card are available for disk-based applications or languages that require extra memory. *–Charles L. Cohen*

IMAGING

HOW IMAGE ENHANCEMENT IS TAKING A GIANT LEAP

PASADENA, CALIF.

Image-enhancement processing—the sharpening of fuzzy video images using digital manipulation—has come a long way since the days when scientists at the Jet Propulsion Laboratory in Pasadena, Calif., first developed techniques to study the images relayed from unmanned moon landings in the 1960s. Now image enhancement is taking a giant leap in efficiency as it moves from software to much faster very large-scale integrated circuits designed for the purpose.

Image-processing pioneer Robert Nathan, a JPL staff scientist, has developed a large-array VLSI filter that performs about 800 million multiply-and-add operations/s. First demonstrated earlier this year when it enhanced images the Voyager 2 spacecraft transmitted as it passed the planet Uranus, it employs 245 complex ICs, packaged in seven-chip hybrid kernels and carrying five multiplier-adders per chip.

The five-board filter runs 60 times faster than JPL's previous mainframe-based image-processing systems—without chewing up nearly so much computer power. And it's about five times faster than the latest commercial graphics-processing boards equipped with digital signal processors. Such speed is especially useful in space communications as an aid in overcoming bandwidth limitations that restrict the volume of data that can be sent.

The JPL filter gets speed from its architecture, which pipelines multipliers and drastically cuts the repetition of a key multiplication element in the image-processing algorithm implemented on board, Nathan explains. At the same time, pipelining holds input data-stream access requirements to a minimum—each pixel needs to be accessed only once. The pixel data is then multiplied by a weighting factor—on-chip calibration information JPL imaging scientists have refined over the years to correct distortion created by high-frequency transmission falloff.

In the filter, "data fed only once to the first chip snakes its way through the rest of them," Nathan explains. The JPL filter thus achieves "true concurrency, running full out, all the time."

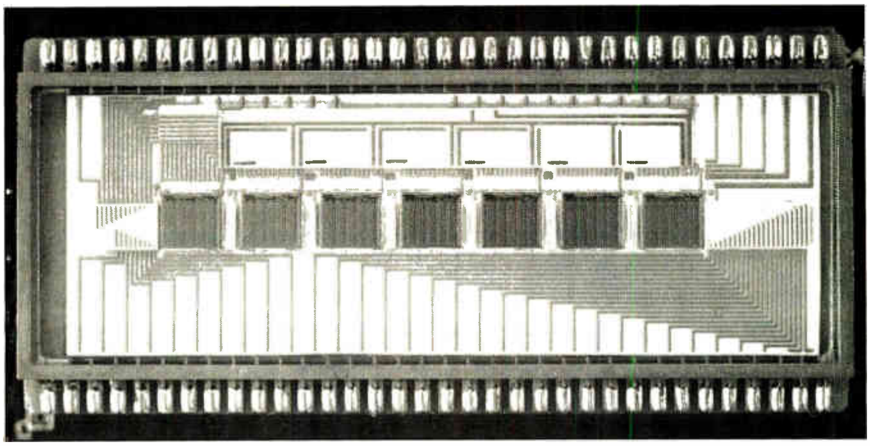


IMAGE ENGINE. Each image-enhancer IC on a JPL hybrid carries five multiplier-adders.

SAVINGS. Because a typical image consists of 1,000 by 1,000 pixels and a 35-by-35-element weighting mask, Nathan calculates that the system offers a 1,225-to-1 savings in accessing steps when compared with the previous software-controlled enhancement processes.

As it stands now, the JPL image enhancer is a plug-in box that depends on a Digital Equipment Corp. VAX-11/780 computer for general processing. To get further improvements, adding chip-based general-purpose processing is the goal, and Nathan hopes to build a 32-bit processor into the next round of chips.

The JPL scientist therefore is proposing an advanced enhancer as an on-board analysis unit for microscope images. It would be carried by the unmanned Rover vehicle intended to roam the surface of Mars and other planets in the 1990s. But the National Aeronautics and Space Administration has not yet approved these missions.

With upgraded processing speed and reliability, the proposed unit could reduce voluminous amounts of data with new algorithms for pattern recognition and extraction. "It should be possible to analyze and even preselect images containing new information for transmission," Nathan predicts. *–Larry Waller*

MICROPROCESSORS

MOTOROLA TARGETS MS-DOS MARKETS

AUSTIN, TEXAS

Recent months have constituted some of the worst of times for chip makers. But they have also been the best of times for microprocessor sales, says Motorola Inc., which is reporting financial results that run against the recessionary grain of the still-sluggish semiconductor industry (see story, p. 154). Somewhat unexpectedly, Motorola reports that an all-time-high demand for its microprocessors helped push semiconductor operating profits sharply higher in the second quarter.

Motorola officials in Austin are now preparing to quicken the pace further with major moves aimed at solidifying and expanding the company's early lead in 32-bit sales over archrival Intel Corp. The Motorola Microprocessor Products Group is expected soon to take its 32-bit 68020 to its highest planned speed grade, a 25-MHz version. A totally new 32-bit design, the widely rumored 68030, waits in the wings for a fall introduction as the heir to the high end of the 68000 series. (Company representatives decline to discuss details on the 68030.)

Motorola is also hoping to exploit what it sees as a window of opportunity to break Intel Corp.'s firm grip on the office market for personal computers. Since the introduction of IBM Corp.'s Personal Computer nearly five years ago, Motorola and other chip competitors have found little success in office markets that have clung to Big Blue's PC standards, which are based on Intel iAPX 86 processors and Microsoft Corp.'s MS-DOS operating system.

But a new version of MS-DOS (numbered 5.0) on the horizon will require the rewriting of software to unleash the full power of the 286 and 386 processors. If the right software standards can be set up before the rewriting starts, Motorola reasons, new program versions will be able to run on Motorola processors as well as those made by other companies.

Such standards are under development at Hunter Systems, a small software house in Palo Alto. Known as XDOS, the effort seeks to establish standard function calls for programs written in the C language to use in interfacing them with MS-DOS 5.0. The calls will also define an interface with the IBM PC's basic input/output system and with the portion of memory reserved for video data.

Programs conforming to the XDOS standard could thus fulfill the original promise of C—they could be ported to any processor architecture simply through recompilation, given an XDOS-compatible operating system written for that processor. Colin Hunter, president of Hunter Systems, says his six-month-old company is now talking with a dozen hardware and software vendors to set up the C standard.

68000 XDOS. Still under development, an XDOS-based operating system for Motorola's 68000 family is expected to be introduced by year end. The 68000 XDOS packages will be available in several versions, one of which will be a stand-alone operating system.

Another version will be offered as a library and kernel that runs atop Unix. This package will enable a 68000-family processor running under Unix to execute XDOS-compatible applications.

In addition to Motorola, Hunter is meeting with microprocessor manufacturers Fairchild Semiconductor Corp. and National Semiconductor Corp., and other companies he declines to identify. "We are saying as long as you are rewriting programs [for MS-DOS 5.0], let's standardize C in such a way that applications can be ported across architectures," says Hunter. He emphasizes that negotiations to set the definitions are still under way. *–J. Robert Lineback*

COMPUTERS

ICs OUTSPEED SOFTWARE IN DOING TEXT SEARCHES

RESEARCH TRIANGLE PARK, N.C.

An easy-to-search electronic file cabinet from General Electric Co. can perform search and retrieval operations faster than software search techniques. GE is teaming two new special-purpose processor chips—a text array processor and a logic-resolution processor—with a Digital Equipment Corp. MicroVAX II to produce its Gefile.

Implementing software procedures and algorithms in hardware for vastly increased performance is not new—floating-point and graphics processors have been around for some time. But now the idea is spreading to applications such as business and office automation; in fact, GE has at least one competitor—Proximity Technology Inc.—in the text-searching chip business.

The chips that make Gefile possible stem from GE's belief that what very large-scale integration has done for general-purpose microprocessors, it can do for special-purpose processors as well. So GE created the Silicon Systems Technology Department in Research Triangle Park to pursue this business.

Designers in the Silicon Systems Technology Department develop special-purpose processors to implement functions in hardware typically done in software, and then develop products based on those processors. The department's first product was the Graphicon 700 processor, a chip set for very high-speed three-dimensional graphics [*Electronics*, April 21, 1986, p. 18].

Work on the text array processor began at GE's Space Systems Division and was transferred to Silicon Systems when the new department was formed. The processor performs sequential searching and retrieval of text at 5 million comparisons/s. Software searching is not directly comparable: it varies by application. A text editor, for example, could hit 2,500 characters/s for a sequential search.

By adding the logic-resolution processor, which resolves Boolean, proximity, and combinatorial logic in search requests, GE has created an efficient sequential-searching engine. Reams of text can be searched and matched in a straightforward, sequential pass without having to create and maintain an index.

Proximity Technology, a small company in Fort Lauderdale, Fla., took a similar tack some 30 months ago when it introduced a special-purpose processor for text searching, the PF474, which searches text at 400,000 characters/s [*Electronics*, Dec. 1, 1983, p. 113]. The PF474 can match and correlate file items without requiring exact matches—it recognizes whether an imprecise inquiry is similar or a close match to information in a file, for example.

Proximity has been marketing the PF474 in a variety of products combining software and hardware. One is Cleanmail, a program that eliminates duplicate entries from a personal computer's data base even if they are not exact duplicates. Cleanmail calculates the degree of similarity between records and presents similar records to the user for comparison and elimination.

Now Proximity is readying the PF-474C Proximity Search, a faster, more power-efficient CMOS version of the chip. The company has designed a non-numerical supercomputer with 8,192 of the new chips running in parallel. "It's a project we want to build," says Peter N. Yianilos, president of Proximity. "We are talking to some of the biggest computer users in the world about a capability to economically deal with very large amounts of inexact data."

The project, as currently conceived, will use a massively parallel architecture, 256 megabytes of random-access memory, and a high-speed local-area network to access the large data bases of IBM Corp. mainframes. This special-purpose engine will give large computers the ability to search data bases of millions or billions of items and very quickly measure similarity. This approximate-pattern-matching ability, a prominent feature of human intelligence, will now be available in computer hardware.

100 CABINETS. GE's Gefile electronic-filing-cabinet product is available now. A much less ambitious product than Proximity's proposed PSP-8000, GE's compact turnkey system is about the size of a two-drawer filing cabinet.

It is a stand-alone filing computer with up to 1 gigabyte of filing storage and a powerful general-purpose computer, the MicroVAX, that can run existing VAX VMS programs and the filing application. Gefile stores up to 500,000 text pages—the equivalent of 100 four-drawer file cabinets—that can be filled up from a variety of sources, such as text scanners, word-processing systems, and electronic mail—and very rapidly searched.

"The system can be used to store office memos, letters, and reports, which often are misfiled and lost in standard filing cabinets," says William F. Geiger, GE's marketing manager.

There are three term-matching processors (GE's Text Array Processor) in the basic $64,900 Gefile system. All Gefile systems, including the 50,000-page starter system, offer multiple simultaneous searches and serve multiple users. *–Tom Manuel*

FILING CABINET. General Electric's Gefile system uses special-purpose VLSI processors to search through a text data base at much higher speeds than software-based systems can.

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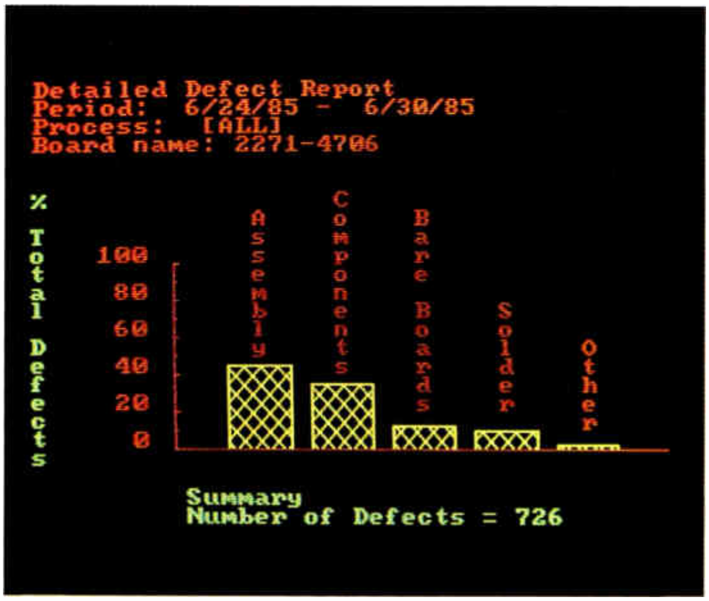

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MIT ICE DETECTOR TAXIS FOR TAKEOFF

CHICAGO

Researchers at the Massachusetts Institute of Technology are turning to ultrasonics for a new way of detecting and measuring ice buildup on aircraft wings. Icing experts say the ultrasonic technique promises greater accuracy than do present detectors. That means it could form the basis for automatic, electronically controlled systems that could make aircraft safer and more efficient.

Current ice-detection systems rely on probes that must be mounted—on the fuselage and the engine inlets—in such a way that they protrude into the airstream. By contrast, the ultrasonic detector developed at MIT can be flush-mounted. This means the unit could be placed directly on the leading edge of a wing and other airfoils, directly measuring the ice on critical surfaces.

"With the probes that we've used for a number of years, we've always had to install them on the side of an airplane. That means you have to extrapolate out to the wing, and that always creates anomalies," notes Douglas E. Cozby, an icing-detection engineer at Boeing Commercial Airplane Co., Seattle. "We'd like to be able to put the detectors on the surfaces we're protecting."

TWO TYPES OF PROBES. Today's commercial transport planes generally use one of two types of external ice detectors, notes Robert J. (Joe) Shaw, deputy chief of the icing research office at the National Aeronautics and Space Administration's Lewis Research Center, Cleveland. One relies on a vibrating rod, with ice buildup detected by changes in the rod's vibration frequency. The second relies on a beam of light that is obscured as ice builds up.

By contrast, the technique developed at MIT uses a piezoelectric crystal transducer/receiver mounted in a housing flush with an airfoil surface. When the piezoelectric element is pulsed with a voltage, it emits a compressive wave. The wave travels through any accreted ice, is reflected at the ice-air interface, and then returns to the transducer as an echo signal (see figure). The elapsed time between the original pulse and the return of the echo is then used to measure the thickness of the ice. The system uses a second, later echo to detect the presence of water on the surface during wet ice buildup.

According to NASA's Shaw, the ultrasonic technique not only detects ice on an airfoil's leading edge but also appears to measure ice growth rates much more accurately than can competing techniques; this property is useful for icing research. NASA has already funded two years of research using the Lewis Icing Research Tunnel and actual aircraft. Shaw says the agency is negotiating to extend that work, which is being done by the MIT inventors of the technique, John Hansman, assistant professor of aeronautics and astronautics, and graduate student Mark S. Kirby. The current contract is up in October.

Meanwhile, MIT is negotiating a final agreement with Simmonds Precision Products Inc., Vergennes, Vt., which is being awarded an exclusive license to market the technology. Simmonds is already working with Boeing, which plans to begin icing-tunnel tests on a prototype ultrasonic unit next month.

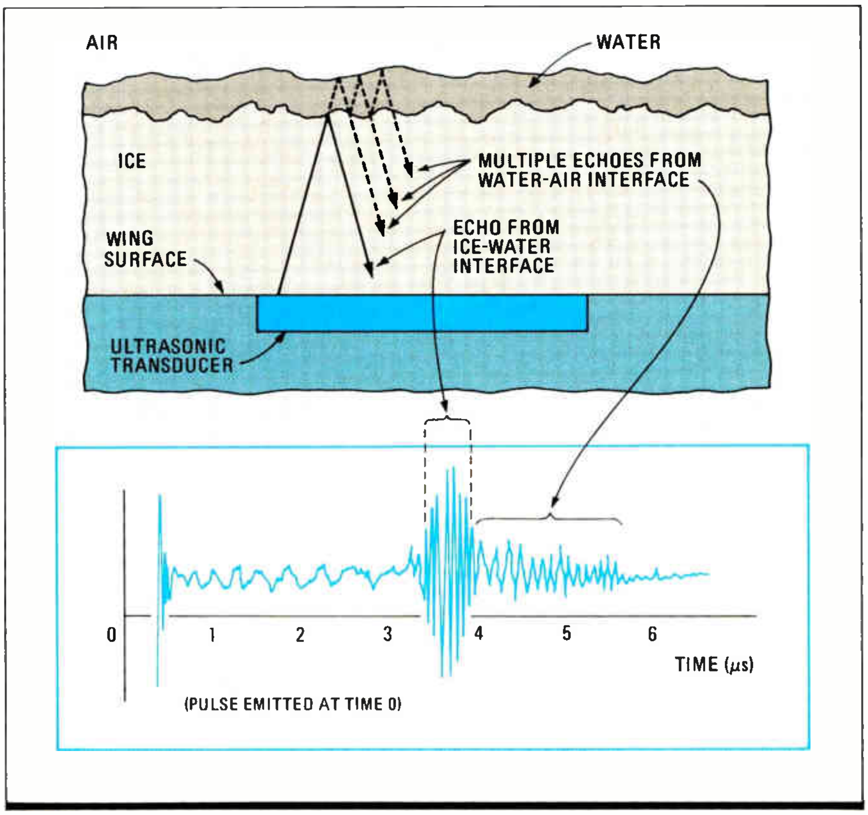
Boeing also plans tests on four other types of detectors, says Cozby, who is heading up the work. Three are probe-type detectors, and the fourth is a surface version of a vibratory device developed by Minneapolis-based Rosemount Inc., Cozby says. The goal of the Boeing tests is to develop an ice-detection and de-icing system for the 7J7, a next-generation short- to medium-haul transport that will take advantage of new propfan designs developed by NASA.

Cozby says Boeing is particularly interested in the surface-mountability of ice detectors. "We intend to use the detector to automatically control the ice-protection system without crew interference, so we want a more direct measurement" of icing on critical surface airfoils, he explains.

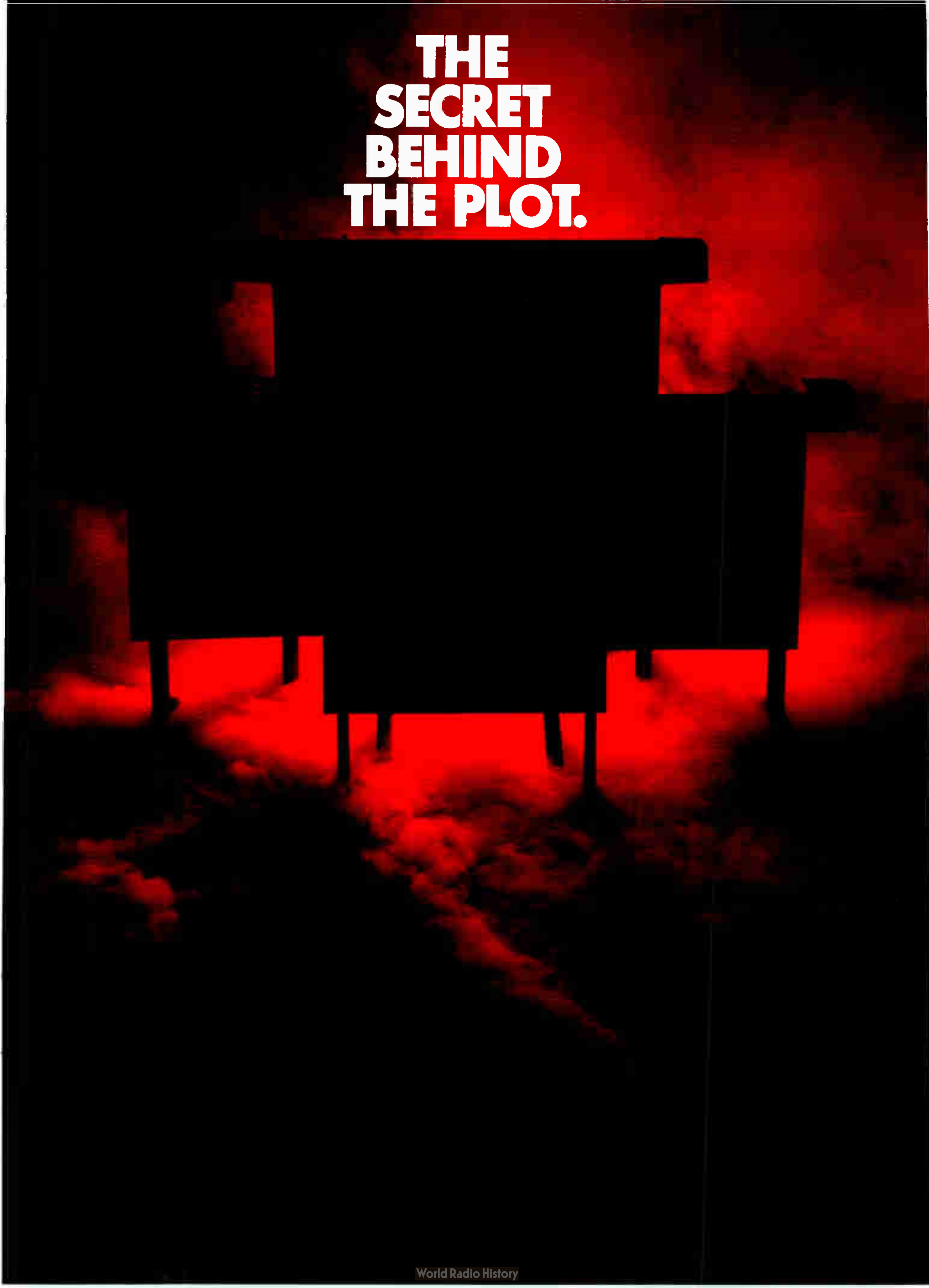
In contrast to current-generation planes, all of which require the pilot to manually control the de-icing system, an aircraft with an automatic system would be more efficient, Cozby says. "Quite often, a pilot has to anticipate when he's going to hit icing" and thus activates the system sooner than necessary, he explains.

De-icing systems flown today include those that direct hot gases from the engine onto critical airfoils and others that mechanically flex the wing surfaces to break up ice. All types in current use exact a penalty in aircraft efficiency, so the less they are used, the better it is for efficiency.

At Simmonds, advanced development marketing manager Douglas E. Stuart says that ice-detection systems based on the MIT technique could be ready for market within two to three years. Systems using multiple flush-mounted ultrasonic sensors in a wing foil under multiplexed microprocessor control are



THIN ICE. An ultrasonic transducer developed by MIT researchers detects and measures the thickness of ice on an airplane's skin by timing an echo returning after a pulse is sent.


THE
SECRET
BEHIND
THE PLOT.

likely, he says, depending on the requirements of aircraft manufacturers. He notes that commercial aircraft makers represent the largest likely near-term market opportunities for the new system.

Hansman at MIT believes that the invention will have a sizable impact on aircraft ice-detection techniques. Although "only about 1% of [aircraft-related] fatalities today are due to icing," Hansman says, use of the ultrasonic technology could help cut that number even lower. *–Wesley R. Iversen*

GRAPHICS

PC-BASED GRAPHICS TAKE ON WORK STATIONS

HUDSON, N. H.

A small graphics company has squeezed the power of a dedicated graphics work station into a pair of boards for IBM Corp.'s Personal Computer AT, RT PC, and compatibles. Not only do the boards offer high-resolution display—1,280 by 1,024 pixels—but the processing power is there to redraw screens at high speed.

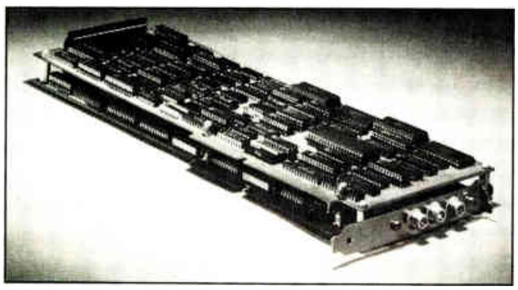
There are a number of graphics cards for PCs that offer the resolution of the $4,500 Clipper Graphics card set from Pixelworks, but few that can approach it in processing clout. It draws vectors at 10 million pixels/s and fills areas at 60 million pixels/s. Such graphics muscle makes a big difference for professional engineering or architectural applications for computer-aided design.

Many industry observers think that the PC marketplace is not ready to support such expensive high-end graphics. Some believe that IBM must clear the trail, establishing a high-end standard before a market will develop. But Pixelworks stands ready to pioneer a market that it thinks fulfills engineering needs not being met by current PC products.

MANY PALs. The Clipper Graphics subsystem offers "the architecture of a mainframe" in an AT environment, says Rattan Dahr, vice president of marketing and sales. The card carries separate special-purpose processors—built using 26 programmable-array logic chips—for interfacing with the system bus and memory, display-list traversal, two- and three-dimensional image transforms, line drawing, and clipping (dealing with elements outside the screen area).

The PC's 80286 microprocessor is left to deal with system input/output tasks and higher-level application functions. Other graphics systems for the PC have chips that relieve the 286 of line drawing and clipping, but Pixelworks believes these chips, such as the Intel 82786, do not give the speed the engineer demands for CAD applications.

"Other companies like Number Nine and Vectrix offer equally high resolution on their boards, but they draw lines using slow, predesigned chips. Their display speed cannot match ours," says Gerard J. Dwyer, the senior hardware engineer on the Clipper project.



FAST CLIP. The Clipper Graphics boards give the engineer's PC AT the power needed for CAD applications.

Using an adapted version of Auto-Cad software, for example, the Clipper zooms in without sacrificing resolution. Maintaining the high resolution, Dwyer says, is vital for the engineer, who works with minute detail.

Pixelworks, an offshoot of Small System Design Inc., a Hudson design and consulting firm, entered the market expecting to sell internationally in six to eight months, but Dahr says the response from the overseas market has been so great that they will begin sooner.

Competitor Microfield Graphics Inc. of Beaverton, Ore., uses a bit-slice processor to achieve a relatively high drawing speed—at least 2 million pixels/s. Microfield claims the bit-slice architecture helps minimize size and power consumption. The $3,200 T4 card achieves speeds of 100 million pixels/s in area fill and 7.4 million pixels/s for random vectors. "The advantage of our system is the programmability of the bit-slice architecture. This allows us to work with each of our clients in designing a system to suit their needs," says Ron Wilson, director of marketing and sales for Microfield.

When a user buys such a graphics system, he must also obtain a high-resolution monitor costing about $1,000. "Can these graphics companies justify the cost? So far the high end of the market has been relatively soft," points out David N. Smith, the products sales manager for Aydin Corp.'s Controls Division, Fort Washington, Pa., which makes such monitors. "Everyone will ooh and ahh at first, but the dollars may not be there."

In fact, PC-based systems don't save much money, claims Jack Morehouse, marketing manager for the Graphics Terminal Division of Tektronix Inc., Beaverton, Ore. "The price of a whole advanced PC graphics set is not as reasonable as some think. It is important to remember that there is less price differential between the specialized graphics PC and the graphics terminals now."

Other makers of PC graphics systems see the direction Pixelworks has taken as the way to go—in time. "Eventually, EGA [IBM's enhanced graphics adapter] will be the bottom of the line in graphics, and the professional systems will be standard," says Michael Dannon, graphics sales manager for Tseng Laboratories Inc., Newtown, Pa. Tseng will move toward top-of-the-line graphics, he says. But "we're going to wait and see about the announcement by IBM about Super EGA [a new graphics expansion for the PC]. No matter how good you are in this market, you still must move with IBM." *–David Rubinger*

PERIPHERALS

A NEW COST CONTENDER IN TOUCH-SENSITIVE SCREENS

WOBURN, MASS.

A strong contender has never left the technological competition to lower the cost of touch screens: analog capacitive touch systems. MicroTouch Systems Inc. is reporting several manufacturing improvements that have substantially lowered costs for analog capacitive technology, which previously had been more expensive than other interactive touch-screen approaches.

Among the advances reported by MicroTouch are a flexible method of building touch sensors for cathode-ray tubes of various shapes and sizes and the development of a narrower electrode pattern that fits out of sight behind most standard CRT bezels. The electrodes are applied to the edges of the touch-sensitive layer of glass that is mounted in front of the CRT.

Thanks in part to computer-aided-design software used to modify the electrode patterns for different screen sizes,

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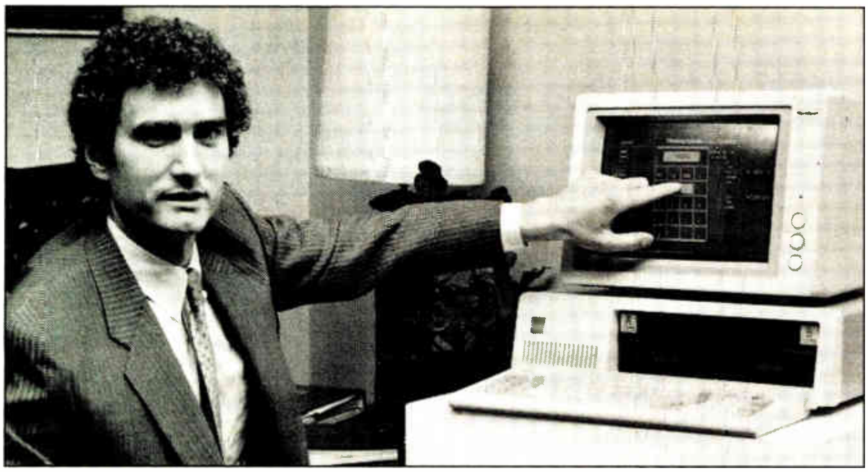

FLEXIBLE. MicroTouch adapts electrode patterns for different screen sizes, says Logan.

turnaround times for new designs have been shortened. It is now possible to retrofit a screen with touch capability in as soon as one week, says Jim Logan, MicroTouch president. Costs have also been reduced by about 30%.

Other touch-screen manufacturers are moving to offer a variety of technologies or to enhance software-development tools to ease the integration of touch-screen technology into designs. Touch-screen advocates generally consider lowering costs and smoothing software as critical to expanding their relatively small markets.

Until now, three major technologies have fought for touch-screen dominance: infrared, resistive membrane, and analog capacitive. Using IR diodes and detectors, a finger or other pointer blocks light projected across the face of the screen. Resistive membranes require mechanical compression of an overlay.

Analog capacitive touch screens use a thin sheet of glass coated with a thin layer of metallic oxide and exploit the capacitance of the human hand. Electrodes along the edges of the glass sheet have an ac signal applied to them. A finger's capacitance changes the signal received on one side of the screen so that the finger's location can be pinpointed.

STILL DEVELOPING. Of the three technologies, analog capacitive technology has traveled the shortest distance along the development curve; it is the most recent of the three to be used commercially. The capacitive approach has also been limited by a relatively large electrode pattern that was not hidden from sight by many standard bezels. Now MicroTouch says it can manufacture the electrodes to stricter tolerances and thereby reduce their size. The company has also partly automated the placement of the electrodes onto the glass.

For quantities in excess of 1,000 units, MicroTouch has cut the price for a 13-in. screen from $500 per unit to $350, including controllers.

While these price cuts bring analog capacitive technology to roughly the level of competitive resistive membrane touch screens and somewhat below the cost of IR screens, Logan believes capacitive technology can be pushed further. He thinks capacitive types will eventually be the lowest in cost.

Meanwhile, the acknowledged installed-base leader in touch screens, Carroll Touch Inc., Round Rock, Texas, will offer a resistive touch screen for the first time next month. Until now, the subsidiary of Amp Inc. has concentrated on IR touch screens. Quantity prices for 13-in. IR screens are around $415 each, the company says.

Elo Graphics Inc. in Oak Ridge, Tenn., is pressing on the software front. The company, a subsidiary of Raychem Corp. of Menlo Park, Calif., will introduce a software development system at Siggraph '86 in Dallas next month.

All these are attempts to build a market that until now has been restricted to narrow niches such as public information displays. Most in the business believe cost has been a major roadblock. "If the price came down by half, you'd probably quadruple the market," says Logan of MicroTouch.

Analysts are generally skeptical, however, about the growth potential for touch-screen markets. Peter Kibbler, a senior consultant with International Resource Development Inc. in Norwalk, Conn., says, "I don't think people like to touch screens."

But touch-screen advocates say markets in areas such as point-of-sale and training devices will provide significant growth for their products. They generally concede that significant penetration of the office market is not feasible now, but they argue that this market could open up as the number of intermittent computer users grows. *–Craig D. Rose*

PERSONAL COMPUTERS

NOW IT'S EASY TO PROCESS CHINESE CHARACTERS

NEW YORK

Within the Great Wall of China lies the greatest market opportunity for computer makers the world over, but tapping that potential has not been easy. With more than 6,000 distinct characters in its alphabet, generating Chinese text is so laborious that China's computers have so far been limited to crunching numbers. But now a system for Chinese text generation called Tian Ma (Chinese for "flying horse") is trying to leap the language barrier and make Chinese computer-compatible.

Drawing on artificial-intelligence techniques to automatically transliterate Pinyin (Chinese spelled out phonetically using the Roman alphabet) into Hanzi (traditional Chinese ideographic characters), Tian Ma may be the most advanced system of its kind. Unlike earlier solutions to Chinese word processing, the add-on boards for IBM Corp. Personal Computers generate Hanzi text in real time, without requiring the user to take part in the transliteration process.

The biggest roadblock to making China computer-literate is making the Chinese language computer-compatible, says Peter Liembigler, director of the Computer Linguistics Group at International Geosystems Corp., Vancouver, B. C. "We have built the bridge between spoken and written Chinese."

Tian Ma uses a context-based approach to choose the right Hanzi character for each Pinyin word, a difficult task because hundreds of Chinese Hanzi characters can be represented by the same sound and Pinyin spelling. There are 120 distinct Hanzi characters that can be pronounced "he," for example, and more than 200 homonyms for "yi." Although intonation is semantically significant in spoken Chinese, the context-based approach compensates for this missing information.

Grammar-school children in the People's Republic of China are now taught to read and write in Pinyin before they learn to use the Hanzi character set, and some of the biggest names in computing—IBM, Wang, and Xerox—now offer products capable of converting Pinyin into Hanzi. But none offers the automatic 99% accuracy that Interna-

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HEWLETT PACKARD

DS15603

Circle 43 on reader service card

tional Geosystems claims for Tian Ma, which was developed after the company, a specialist in computerized mining applications, found it was having trouble corresponding with Chinese clients. Now the company is hoping to expand its presence in China, Liembigler says. "This is the type of system we think will help in technology transfer."

The challenge in translating from Pinyin to Hanzi is in sorting out the appropriate character without slowing down the typist, says Jerry Kambeitz, Tian Ma project director. In other systems, the typist is burdened with choosing the most appropriate ideogram from a computer-generated list, as is necessary with the Xerox 6085 work station, configurable in about 30 languages.

The 6085 halts every time it confronts a choice of which Hanzi character is intended by a given Pinyin word; it offers the user a list of homonyms from which to choose. This can happen as often as every fifth to tenth word, says Deborah Phillips, manager of multilingual markets at Xerox Corp.'s Information Systems Division, Sunnyvale, Calif.

ALMOST ALWAYS RIGHT. In contrast, Tian Ma will get 99 Hanzi characters out of 100 right when using common language, says Liembigler. Where technical terminology is involved, the system's data base must be expanded.

Unlike Xerox's product—a complete system costing between $8,000 and $10,000 configured for Chinese—Tian Ma resides on an add-on board for the IBM PC and compatibles. The board, with 1.2 megabytes of read-only memory and a Z80B processor, costs about $1,200 and can be easily incorporated into word-processing and desktop publishing systems.

International Geosystems plans to build between 50,000 and 60,000 of the boards in the next 18 months, says chairman Joseph Mason. Negotiations are under way for distribution rights, and, Mason says, "we can sell everything we make."

But the company's strategy is to sell only some of the boards through distributors. "We prefer not to make commitments with distributors that would prohibit better commitments from IBM and Wang," says Mason. Discussions with both computer makers are ongoing.

Just how much impact Tian Ma can have in China is still unclear; estimates of China's installed base of microcomputers range from 150,000 to 600,000. And word processing ranks low on the Chinese list of priorities, says Dick Bloss, an independent consultant and project director for market researcher Frost & Sullivan Inc., New York. "At the moment, there's not much of a market for it. Their computer revolution is just starting. They're not going to start out where we are now, they're going to start where we were in 1955. And no one ever heard of word processing back then."

Undaunted, International Geosystems is already talking about developing a low-cost Chinese word processor and using the Tian Ma algorithm in a Japanese-language system. And Kambeitz indicates that talks with IBM may result in the combination of Tian Ma with a voice-recognition system that would allow direct translation of spoken Chinese into Hanzi text. *–Tobias Naegele*

COMPONENTS

FILM CUTS COST UP TO 90% FOR CAPACITIVE KEYBOARD

MONTAUBON, FRANCE

France is about to get its first native entry in one of the least glamorous but fastest growing niches of the data-processing industry.

This autumn, Mors SA of Montaubon will begin producing full-travel capacitive keyboards that replace the internal printed-circuit board with a polyester film carrying printed silver traces. Company executives figure this original technology will give them a competitive edge in cost—they expect to be able to manufacture a keyboard for between 10% and 20% of the cost of capacitive units built with pc-board technology.

Mors, a company that splits its annual $100 million sales between military and professional systems and components such as relays and switches, has a clear motive for entering the market. Company estimates put the world market for full-travel keyboards, whose keys move a minimum of 4 mm when pressed, at some $500 million and rising at an annual rate of 30%. Some 25% to 30% of that total is made up of capacitive keyboards, which are far more reliable than their resistive-technology counterparts.

EASY TOUCH. A polyester film layer makes Mors's capacitive keyboard less expensive than pc-board-based competition.

BIG PLANS. Being the only native manufacturer should put Mors in a particularly strong position to grab a substantial piece of the French keyboard market, which Mors sees reaching a little more than $21 million this year and expanding at a rate of 25%. The company predicts the French full-travel keyboard market will reach $50 million by 1990.

Full-travel keyboards based on resistive-contact technology are less expensive than capacitive types. Mors believes its capacitive product will be as inexpensive to produce as resistive keyboards, while offering all the advantages of expensive capacitive models.

Resistive keyboards use a conventional electrical switch contact; their operation is easily degraded by ambient dust and other contaminants. In capacitive keyboards, the switch contact of each key is replaced by a capacitor with one electrode mounted on the key itself and the other inside the keyboard housing. Depressing the key brings the two electrodes closer without letting them touch and causes a rise in capacitance.

When the capacitance passes above a set threshold, the condition is decoded as a key having been pressed. In existing capacitive keyboards, a pc board forms the pattern of internal electrodes.

Mors replaces the pc board with a polyester film mounted on a metal substrate for rigidity. On the film are printed successive layers of silver and varnish, as conductor and dielectric, respectively, to form the internal electrodes and the connections to them.

Each key contains a plunger to which is attached a block of synthetic foam mounted with an electrode. The foam cushions the action of the key to give the keyboard a pleasant touch and to make operation nearly silent. An integrated dish-shaped spring returns keys to their original position.

A very few standard electronic components form an interactive interface between the keys and the associated data-processing system. Mors holds patents on both the polyester film layer and the interface electronics.

Keyboards based on this technology are suited to mass production—computer-aided manufacturing can easily handle design variations. Mors executives reckon the company can make changes in half a day. *–Robert T. Gallagher*

Circle 45 on reader service card

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INTERNATIONAL NEWSLETTER

BATTERED AIWA BRACES FOR $24 MILLION LOSS FOR YEAR

The balmy days of uncontested supremacy for Japanese consumer electronics companies are a memory: they are taking a pounding from the rising yen and strong Korean competition. The latest producer to show the effects of the struggle is Aiwa Co. The Sony Corp. subsidiary is soaking in red ink, with a loss of more than $13 million for the six months ended May 31 and an anticipated loss of $24 million for the full fiscal year ending Nov. 31. The Tokyo-based audio and video equipment manufacturer blames more than the strong yen and Korean competition. It notes that orders for Sony's private-label production of Beta video cassette recorders were halved as demand for that format dried up, and 8-mm VCR sales did not pick up as rapidly as expected. So Aiwa will seek to cut its losses by shutting down one of its three plants in Japan, transferring some of the production to Singapore, and eliminating about 700 of its 3,200 employees. The company also plans to combine its four operating divisions, now scattered around Tokyo. □

WEST GERMANS PUT COMPUTER VISION BEHIND THE WHEEL

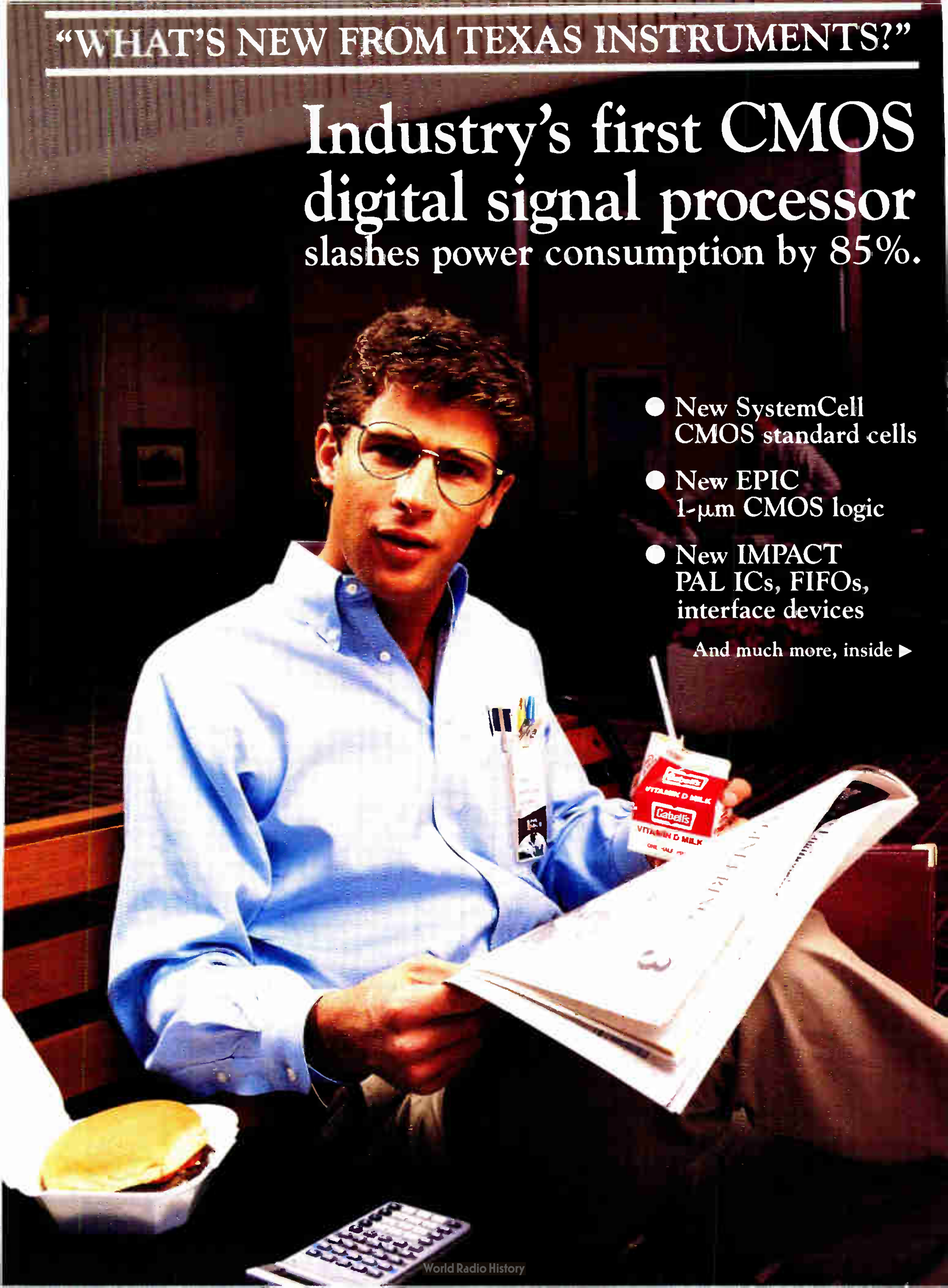
Researchers at West Germany's Armed Forces University in Munich say the "Autonomobile" they have been developing for the past five years under a government grant will be ready for a workout on a private test track next year. The research team, headed by Ernst D. Dickmanns, a professor for control engineering at the university's Aerospace Department, already has proved out the basic gear for the autonomous vehicle—a computer-controlled vision and guidance system plus an automatic throttle control and brake control. Using a Mercedes test van from Daimler-Benz AG with a human driver, the initial tests, which only partly exercised the autopilot, were run at speeds up to 40 mph on country roads and up to 60 mph on the Autobahn, Germany's network of superhighways. "We are not seeking to replace the driver," Dickmanns emphasizes. The goal, he says, is a kind of control that can take over from the human driver just as an aircraft's autopilot does in situations when the pilot's full attention is not necessary. The Munich machine relies on standard chips, unlike the U. S.'s Autonomous Land Vehicle program sponsored by the Defense Advanced Research Projects Agency, which is based on new computer architectures and yet-to-be-developed hardware. □

MESSERSCHMITT GOES AFTER BIGGEST FOREIGN STAR WARS AWARD

The biggest Strategic Defense Initiative contract slated for a non-U. S. company is the lure for Messerschmitt-Bölkow-Blohm GmbH, West Germany's largest aerospace company. Messerschmitt has a $4 million order for predevelopment work on an infrared sensing system that space vehicles would use to identify enemy-launched missiles in flight by their heat waves. If the Messerschmitt system passes muster, its reward will be a $35 million contract to follow through with development. □

JAPANESE TO LET U. S. SCIENTISTS INTO FIFTH-GENERATION PROJECT

Computer scientists from the U. S. will gain access to Japan's fifth-generation computer project under a new agreement between the National Science Foundation and the Tokyo-based Institute for New Generation Computer Technology group. The agreement, to take effect next year, will bring up to three U. S. researchers per year into the Japanese project, for six months to a year each. The American visitors will be treated as regular staff members, with the right to work on their own personal research or contribute to the Japanese project's objectives. All results will be published in general scientific literature. □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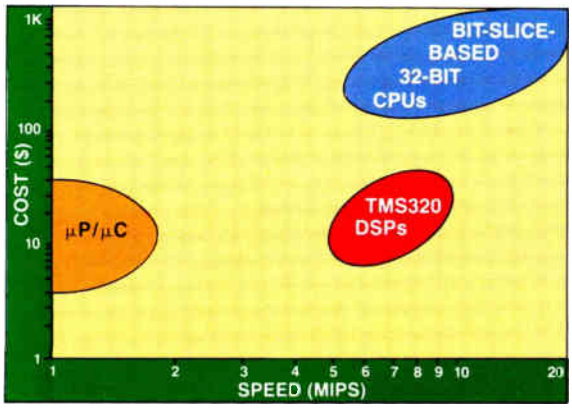
Processing five million instructions per second, TI's new CMOS TMS320C10 programmable DSP can, in many applications, give you the performance of a bit-slice processor at the price of a microcontroller. And it dissipates only 125 mW — just 15% of the power of the industry-standard TMS32010.

While the design of the new TMS320C10 has been optimized for DSP, it can serve equally well as a high-speed microprocessor in a broad range of computation-intensive applications: Telecommunications. High-speed control. Consumer goods. Computers. And with its low power consumption and high inherent noise immunity, TI's TMS320C10 is also ideal for use in portable equipment and for control applications in electrically noisy environments.

TI's TMS320 DSP FAMILY MEETS COST/PERFORMANCE NEEDS



High performance at lower cost distinguishes TI's TMS320 family. In many applications, TMS320 devices can give you speed comparable to bit-slice processors at prices on a par with much slower dedicated microcontrollers.

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TI's new CMOS TMS320C10 is plug-in compatible with the industry-standard TMS32010. It utilizes the same Harvard architecture and the same advanced instruction set. It gives you the same 16 × 16-bit hardware multiplier with 32-bit precision — that multiplies as fast as it adds. And it communicates with off-chip memory at full speed.

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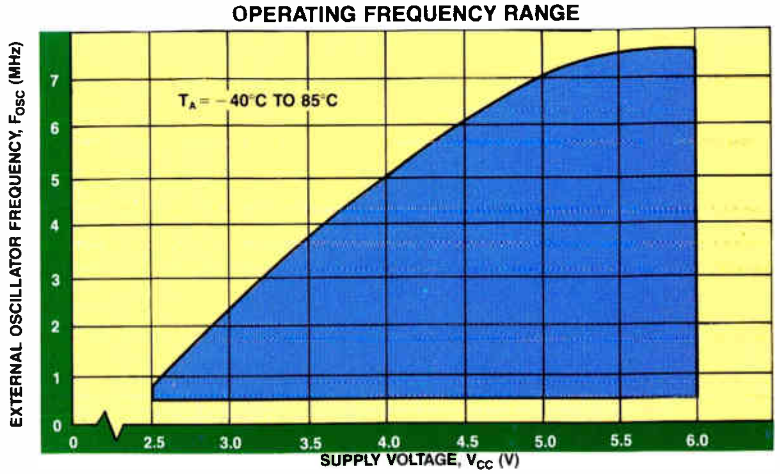
1

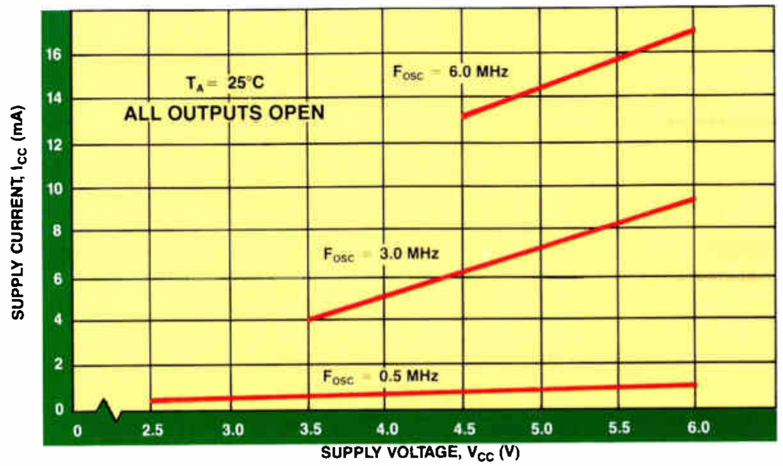
New CMOS microcomputer helps cut system costs.

TI's TMS70C42 CMOS 8-bit microcomputer is designed to help lower your system costs across a broad spectrum of realtime control applications and a wide range of operating characteristics (*see graphs*). Both the TMS70C42, with its 4K bytes of on-board ROM and 256 bytes of RAM, and its ROM-less TMS70C02 counterpart have features designed to reduce system cost: Two high-resolution 16-bit timers with 5-bit prescale and pulse-width-modulation output. Fully programmable interrupt enable and interface. Integrated hardware UART with baud-rate generator.

And to help get your product to market quickly and economically, these extremely flexible devices are supported by an extensive array of inexpensive development tools.

TMS70C42 MICROCOMPUTER





2

IMPACT PAL ICs are world's fastest, at 12 ns maximum.

TI's exclusive 2-µm IMPACT technology makes possible extremely dense and fast programmable-array-logic (PAL) circuits. Now four new PAL ICs (TIBPAL16XX-12 series) from TI cut propagation delay to an unprecedented 12 ns. And maximum clock-to-output time to only 10 ns. For the first time, you can design in programmable logic that is faster than that provided by high-speed discrete logic products like the 74AS and 74F families.

TI's new IMPACT PAL ICs provide for cost-effective implementation of a wide range of circuits formerly based on SSI/MSI components: Minicomputers, superminis, professional computers, industrial controls, high-end graphics processors — wherever super speed and programmability are important design criteria.

Military IMPACT PAL family continues to grow

For manufacturers of military products, TI now offers a family of 16 PAL circuits which comply fully with the requirements of MIL-STD-883C, Class B. Included are standard and half-power devices with propagation-delay times of 30 and 40 ns, drawing 185 and 95 mA, respectively.

Where power limitations are tight or *super* speed is vital, TI's unique IMPACT PAL ICs can make the difference — whether for retrofitting an existing design or starting from scratch. Because they dissipate significantly less power for the same high-speed performance (30 ns for 105 mA, maximum). Or for approximately the same power (200 mA, maximum), they can give you 20-ns speed (*see table*).

CHARACTERISTICS OF TI MILITARY PAL ICs

Type	T_{pd} (ns)	I_{CC} (mA)	F_{max} (MHz)
Standard (16XXA)	30	185	25
Low-power (16XXA-2)	40	95	16
High-speed IMPACT (16XX-20)	20	200	40
Lower-power IMPACT (16XX-30)	30	105	25

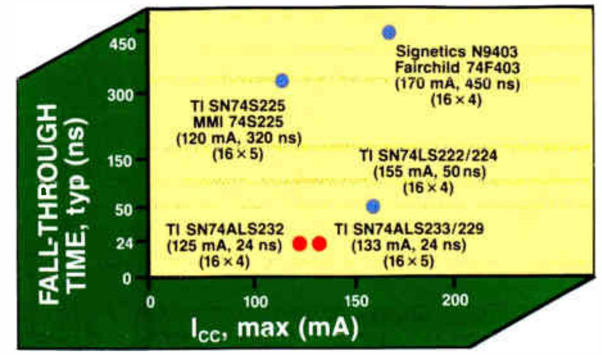
3

TI's IMPACT FIFOs: 50% faster than any others.

TI's new "zero-fall-through" 16 × 4 and 16 × 5 IMPACT FIFO memories are a full 50% faster than any others. And operate at a low 133 mA.

The SN75ALS232/233/229 asynchronous FIFOs feature dual-port-RAM architecture, so there are no ripple-through delays, no address generation required. Their 0- to 30-MHz speed gives you increased system throughput for long data streams. Full/empty status flags may be used as clock-enable signals to control asynchronous timing.

TI's IMPACT FIFOs SET THE PERFORMANCE PACE



New industry leaders: TI's IMPACT FIFOs offer a 50% improvement in fall-through time.

4

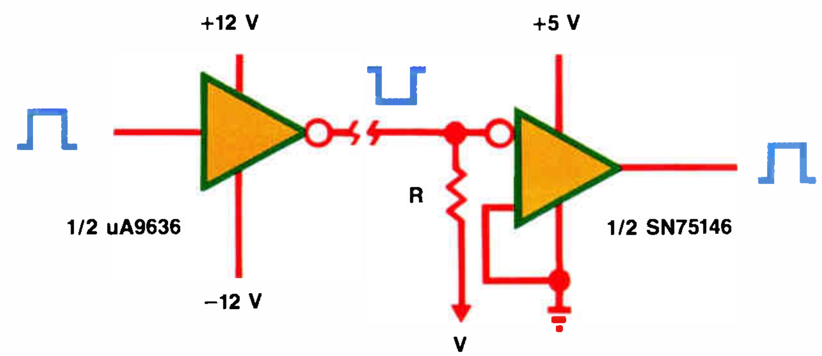
High-speed, low-power IMPACT line drivers and receivers.

Now Texas Instruments utilizes the IMPACT process for the first time in line-interface devices. For high speed and low power.

TI's SN75ALS126 quadruple line driver, designed to meet IBM 360/370 specifications, provides for faster switching with lower power dissipation than the SN75126 and MC3481 drivers for which they are direct replacements.

A new dual differential line receiver, SN75146, is compatible with either single-ended or differential-line systems, to meet both RS-422-A and RS-423-A EIA Standards. With one external resistor, it also meets the requirements of RS-232-C (*see diagram*). Similar to the uA9639, TI's SN75146 includes additional input filtering, making it ideal for noise-sensitive single-ended applications.

RS-232-C SYSTEM APPLICATIONS, SN75146



Unique new TI line receiver meets RS-422-A and RS-423-A standards. And with a single external resistor (R) it also satisfies the requirements of EIA Standard RS-232-C.

5

High-speed signal conditioners for wide-bandwidth applications.

For compatibility with digital processors, signals from magnetic mass memories and video imaging arrays must be amplified and shaped by circuits capable of very high data rates. Now Texas Instruments introduces five such circuits: Three differential video amplifiers and two differential comparators.

The TL592B is a low-noise, high-gain amplifier with a 50-MHz bandwidth and only 3 µV of broad-band noise. For applications that require automatic gain control, the TL026 and TL027 amplifiers offer a selection of peak gains with 50-MHz bandwidth and 50 dB of AGC.

And TI's new TL712 and TL721 high-speed comparators provide the signal shaping necessary for compatibility with TTL or ECL logic circuits, with propagation delays that can be less than 12 ns.

TYPICAL SIGNAL-CONDITIONING APPLICATION

For more information ...

about any of the new products from Texas Instruments described here, just check the appropriate squares on the reply card and return it to TI today.

1-μm EPIC process enhances TI's CMOS logic circuits.

Enhanced Performance Implanted CMOS (EPIC™) logic, a unique development of Texas Instruments, will bring to silicon-gate CMOS logic the speed of FAST™ high-speed advanced bipolar devices — and 24-mA sink/source current — while retaining the inherently low power characteristics of the CMOS process.

The 1-μm EPIC process is a direct outgrowth of TI's 1-Mb DRAM technology. In fact, the cell design of TI's 1-Mb DRAM was itself strongly influenced by the desire to devise a technology equally applicable to the fabrication flow of high-performance logic.

The outcome is a universal 1-μm flow in which the steps for making DRAM-cell capacitors can be easily skipped when processing logic ICs. This unifying technology is helping TI to respond quickly, sensitively — and economically — to your changing needs.

EPIC products optimized for high quality and reliability

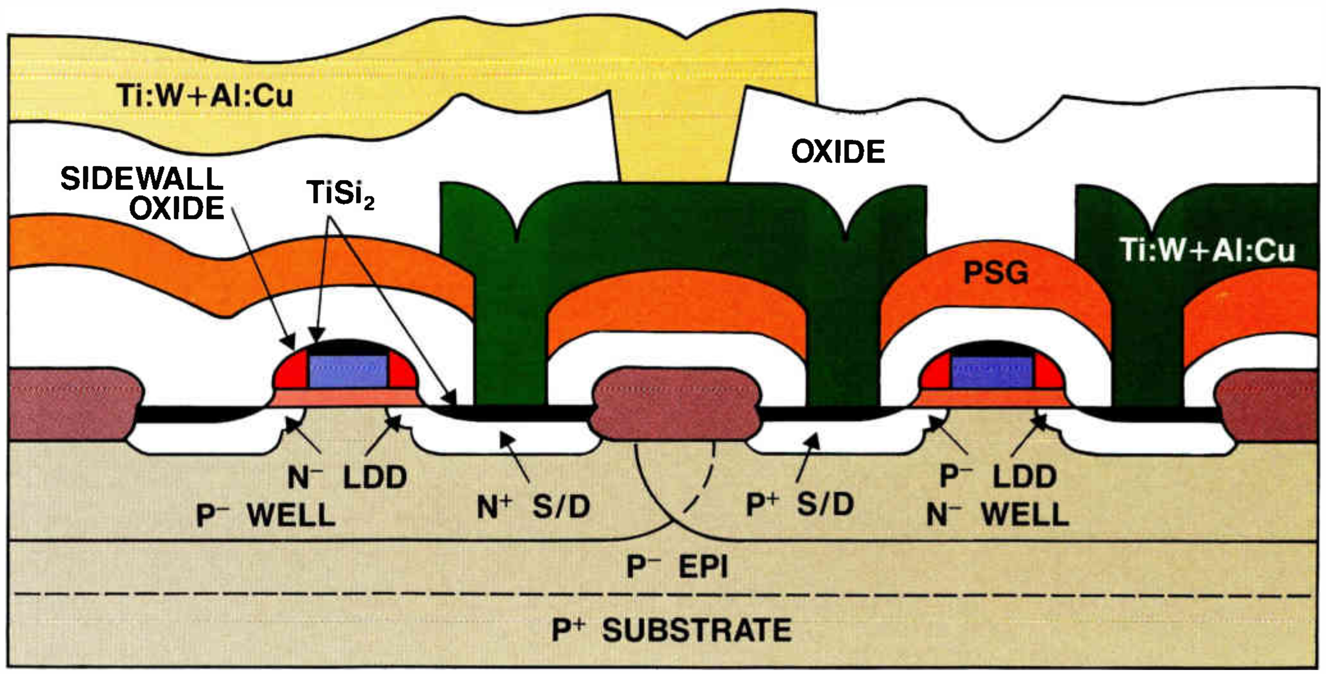
Fundamental physical limitations become critical in the design and fabrication of structures as small as 1 μm: Quantum-mechanical tunneling through thin oxides. High-intensity fields due to hot-electron effects. Latch-up in high-density CMOS circuits. All have been brought under effective control by TI's new 1-μm EPIC design.

Among the features that contribute to optimal reliability in TI's new EPIC CMOS devices: Input and output structures that protect against electrostatic discharge up to ±6 kV, well above the ±2 kV specified by MIL-STD-883. Copper-doped aluminum metal improves reliability by effectively preventing electromigration. The process also features an epitaxial substrate layer for outstanding latch-up suppression *(see diagram)*.

A broad family of devices soon to come

With the perfection of TI's 1-μm EPIC processing, a whole new family of advanced CMOS logic (ACL) devices is on the horizon. It is expected to include SSI and simple and complex MSI parts. The 1-μm gate lengths in EPIC devices will permit average propagation delays of less than 3 ns, with subnanosecond internal-gate performance.

Watch for introductions of TI's high-speed EPIC ACL devices. They're coming soon.



Superior switching time and 24-mA output drive are achieved in TI's new ACL family through 1-μm EPIC CMOS technology. The process is an outgrowth of the CMOS technology developed by TI to support its 1-Mb DRAM.

Texas Instruments quality and service cut your costs.

You can cut your costs of incoming inspection and testing. Diminish lead times and inventories. Reduce board and systems repair and warranty replacements. And make substantial savings, because these expenses may drive the ultimate cost of your components as high as two or even five times what you paid your supplier for them.

At Texas Instruments, we recognize this problem, and we're doing something about it.

TI is committed to improvements in quality and service that can cut your total "cost of ownership" for the components we manufacture. By stressing on-time delivery, so you can shorten lead times and slash inventories. And by delivering only products conforming to the highest standards of quality and reliability, so you may choose to reduce or eliminate incoming inspection and minimize repair and replacement.

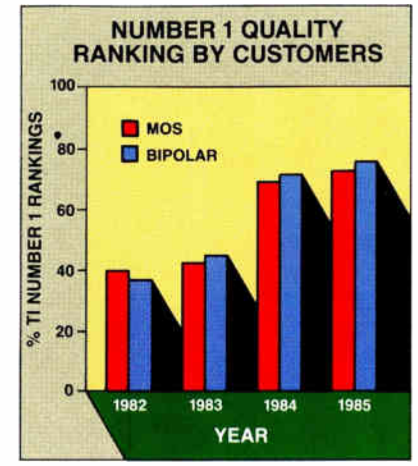
Service partnership with TI makes you the winner

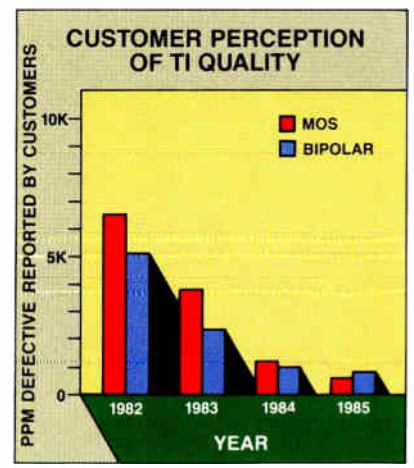
Central to TI's approach is our conviction that supplying semiconductors is more than producing commodities: It is a service that you depend on us for. In order to provide that service, we must establish an appropriate, responsible partnership with you.

To make that partnership work to your advantage, we must provide leadership technology in all areas of your needs — on time. And that is exactly the direction Texas Instruments is moving, to give our customers every benefit of leading-edge technology — including the technology of quality and service.

Quality and reliability: TI's commitment to you

In the era of megabit-class technologies, quality and reliability are increasingly critical. And at TI the bottom line of our quality-improvement program is lower cost of ownership for you. In partnership with our customers, we are making it work. As measured and reported by customers participating in an ongoing feedback program, TI quality — in terms of parts per million (ppm) defective — has reached levels unheard of just a few years ago *(see bar graph below)*.





Among those TI customers taking part in another continuing survey, the number who rank TI's quality first among their semiconductor suppliers shows an impressive and steady increase *(see bar graph above)*. Since 1984 customers in the U.S., Europe, and Japan have presented TI with more than 50 awards for outstanding quality and service achievements.

A record to be proud of? Yes. And we are. But the real payoff from TI's giant steps in innovative technology and service is increased profits and market share for you.

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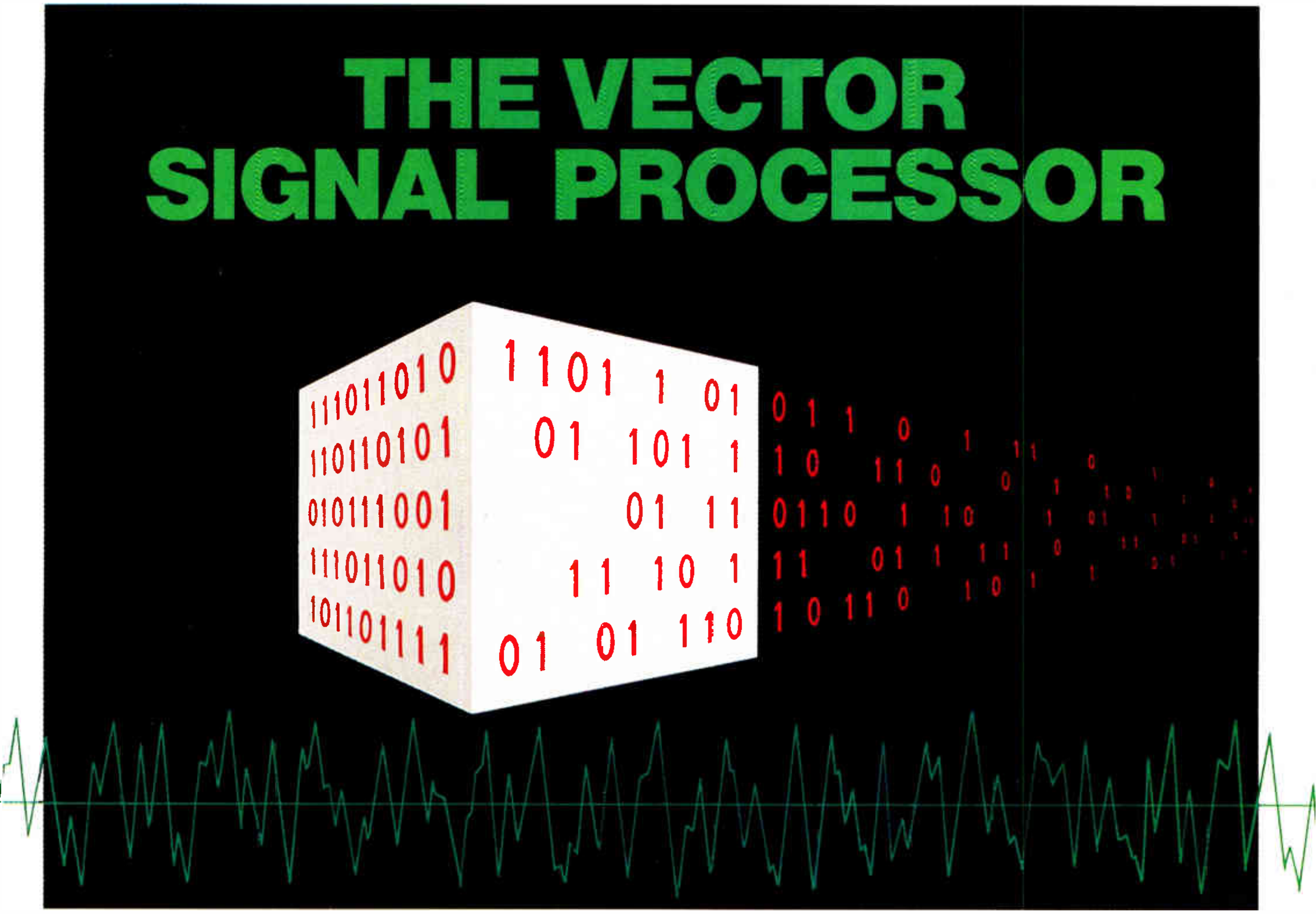
INSIDE TECHNOLOGY

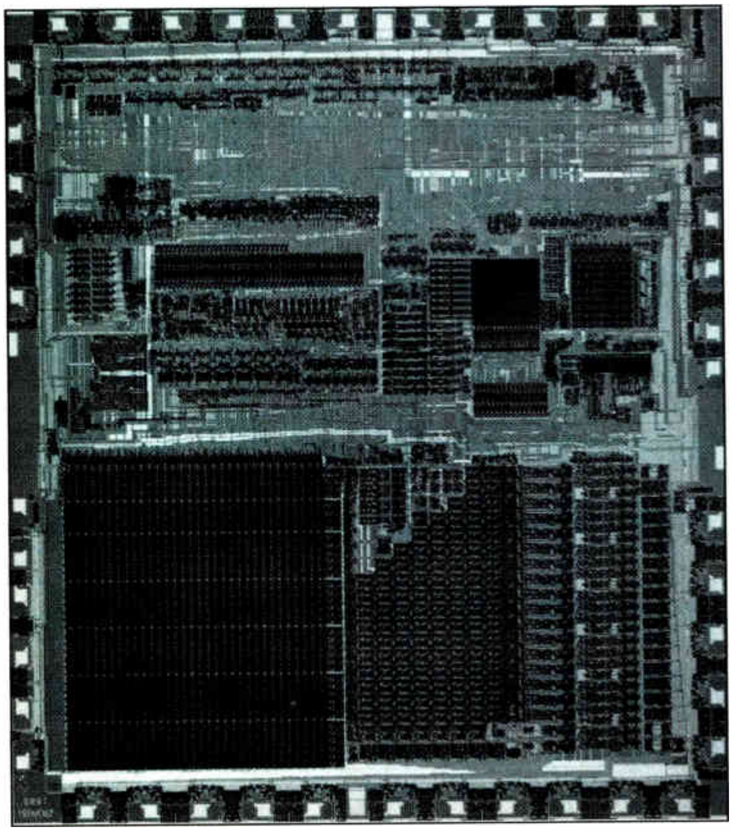
A NEW CLASS OF DSP CHIP:



A speedy new single-chip contender is getting set to make a splash in digital signal processing. Zoran Corp.'s ZR34161 uses vector-handling techniques to gulp down blocks of data, rather than picking off a single data input at a time as scalar processors do. Vector processing alone is a big speed booster, and Zoran enhances it with embedded signal-processing algorithms that radically pare down system overhead. The embedded algorithms also make it much easier to incorporate the new vector signal processor into a system: the designer uses high-level instructions rather than writing many lines of machine code. The result is a chip that can execute a fast Fourier transform with only three instructions. What's more, it operates at throughputs high enough for real-time image processing: 2.5 ms for an FFT.

The Santa Clara, Calif., company's 16-bit CMOS VSP (Fig. 1) is the first monolithic signal processor to utilize the powerful vector-handling techniques employed for scientific data processing in large vector computers and minicomputer array processors (see "Grabbing data by the block," opposite). The ZR34161 [*Electronics*, July 10, 1986, p. 19] would also work nicely as a coprocessor for personal computers, according to the company. Despite its high performance, the chip contains only 70,000 transistors, so it is not large by today's signal-processor standards. It is made in 2-μm, double-layer-metal CMOS technology.

The ZR34161 handles vectors as long as 128 complex words rather than one input at a time (scalars). It uses high-level instructions to execute embedded algorithms, has an architecture optimized for processing in the frequency domain with the embedded algorithms, and uses block floating-point arithmetic. All new to monolithic signal processors, these features minimize data handling, eliminate hundreds of lines of instruction code and fetches, and add efficiency.



The embedment technique is a proprietary combination of hardwiring and microcoding that enables the processor to interpret the instruction tailoring.

The chip's architecture stems from a decision by Zoran's founders (Levy Gerzberg, executive vice president and chief technical officer, and Yuval Almog, senior vice president) to pursue what the company calls its Systems Processors concept—that is, to give priority to system integration and performance rather than single-function components such as multipliers and multiplier-accumulators. So instead of becoming a scalar machine using low-level instructions, the ZR-34161 evolved into a vector processor using high-level instructions and embedded algorithms, onboard rather than external direct memory access, and a DSP-driven instruction set instead of general-purpose instructions.

VECTOR HEAVEN

"Open any textbook on digital signal processing and you'll see sigmas scattered throughout the text," notes Gerzberg. "All those sigmas represent vectors, so why not simply process them as vectors?" Vector-processing programs require very few memory accesses other than DMA transfers. "Even a very complex mathematical operation like the FFT is simplified. It takes just three instructions: load vector, execute FFT, store results. Done!"

Further, he notes, programs can exploit the VSP's 20-MHz clock rate because, with no memory fetches and bus contentions to add overhead, the embedded algorithms actually run that fast. Moreover, the algorithms provide the math expertise previously needed to write signal-processing programs.

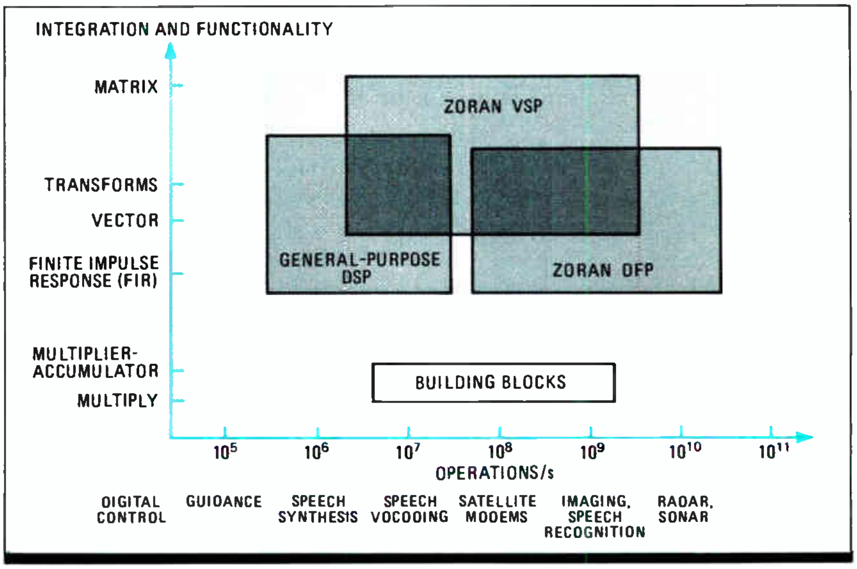
"Yet users can differentiate their products by using different algorithms and in different order," Gerzberg says. "For instance, in two-dimensional image processing, designers may use various types of transforms, do filtering before or after transformations, compress the data with proprietary tricks, and so forth. With this kind of processor, a designer can be more innovative because he can now afford very complex algorithmic schemes.

"One of the nice things is that you can concentrate on the key system concept, rather than the fine details of the mathematics," he continues. "With a general-purpose device, signal-processing experts are needed to write the math into the program correctly. But with our approach, an engineer need only decide what algorithms to use. An engineer fresh out of college can write DSP software with relative ease."

Despite the FFT's popularity in the DSP community, designers often avoid incorporating the

1. MONOLITHIC VSP. Zoran's vector digital-signal-processing chip with 70,000 transistors requires only three instructions to do a 1,024-point fast Fourier transform in 2.4 ms.

function into their products because it requires a lot of hardware or software to implement, according to Almog. He says Zoran chose the FFT as the core algorithm of the VSP because it can be used throughout a very broad range of applications, provided that system throughput and cost targets are met. "Fast Fourier transforms could not be executed easily with only multiplier-accumulator building blocks," Almog says. "So we viewed this as an opportunity to provide a needed function that previously demanded too much software or hardware." He adds that Zoran has also integrated system-simulation capabilities into the Vector Signal Processor Simulator (VSPS) to minimize up-front investment in software and algorithm development.



2. WIDE RANGING. Zoran's Systems Processors extend the range of monolithic DSP applications to the high end of the telecommunications spectrum.

With the VSPS, a system designer can take a good look at systems with up to eight VSPs running simultaneously simply by embedding the signal-processing programs in the C-language simulator program. The designer can also describe external devices and look at how the VSPs interact with them. Alternatively, the designer can use any C-callable language, including Fortran.

In this environment, users can compare alternate system designs, determine arithmetic precision, time program executions, and monitor bus usage. After the program has been debugged, the simulation package generates VSP object code that can be embedded into a host-system program. A $5,000 simulation package runs on Digital Equipment Corp. VAX computers under both VMS and AT&T Bell Laboratories' Unix operating systems, and a $3,000 package runs on an IBM Corp. Personal Computer AT under Microsoft Corp.'s MS-DOS. The PC AT becomes an applications development system with its simulator and a $3,000 applications development board. Also available are a VSP evaluation board, an assembler package, and one-day and three-day hands-on training courses.

The company is also introducing a family of companion chips called digital filter processors (DFPs). These processors also use the embedded-algorithm technology, but they incorporate a more specialized set of algorithms that allows the DFP to operate in optional, hardwirable modes instead of under software control.

By combining the DFP with the VSP, system designers can implement a wide range of complex signal-processing applications with relatively little concern about the mathematical aspects of the design. These DFPs are multitap, multicell processors for such vector operations as finite-impulse-response (FIR) filtering and convolutions. The DFPs do not execute instructions; however, with different coefficients and hardwiring schemes, they can perform a large

GRABBING DATA BY THE BLOCK

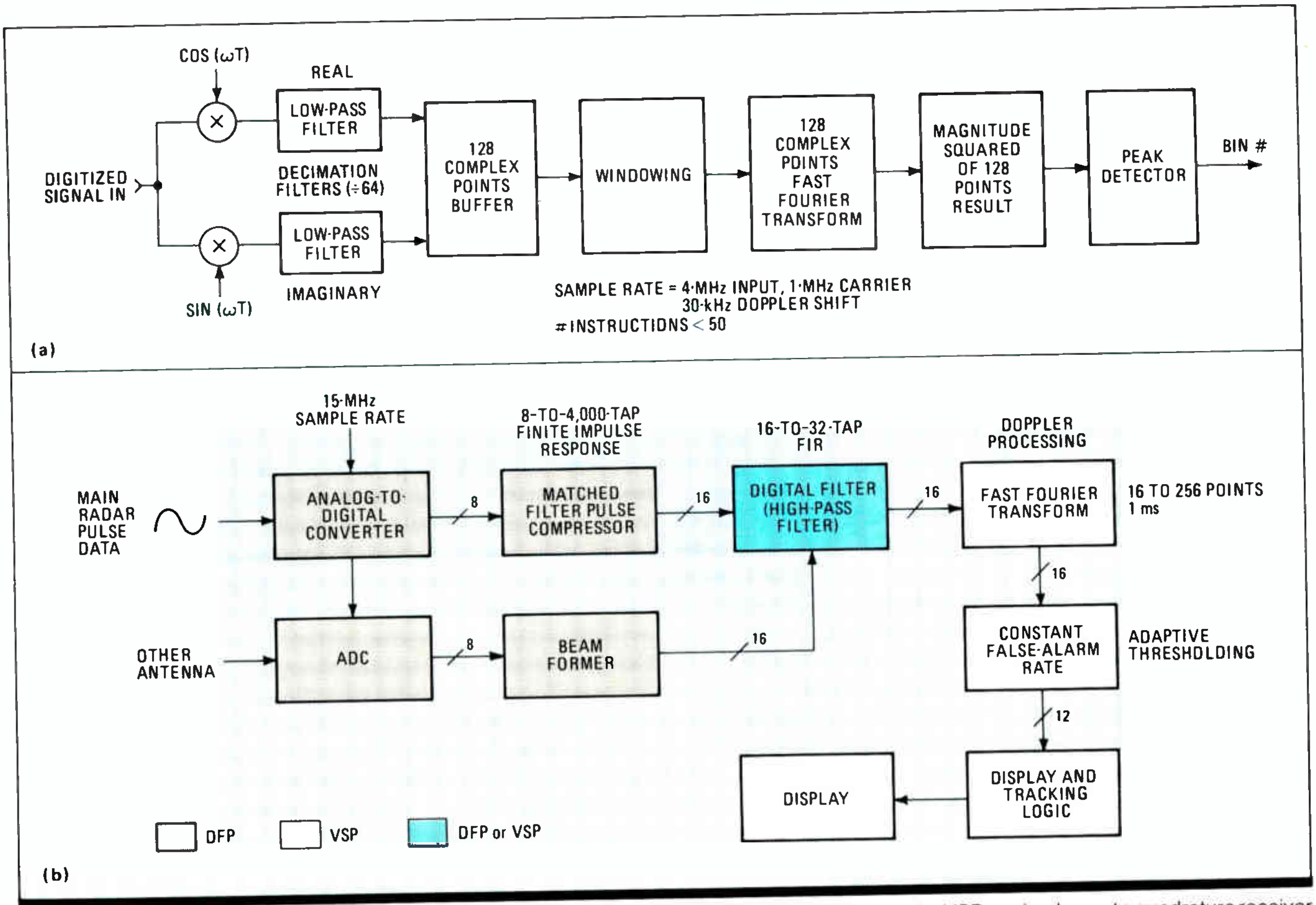
Vector processing speeds up processing of data streams by operating on blocks of data, called vectors, instead of on one data input at a time, as in scalar processing. In signal processing, the vectors may be sets of samples representing analog signals, but they can also be other types of signal information or such digital signals as the output of a charge-coupled-device video camera.

Conventional digital signal processors handle one input at a time. So if an application calls for processing data in sets, blocks, or continuous streams, a vector processor will usually be more efficient. Large-scale vector computers, for instance, are often used to process weather-forecasting data and to enhance video images transmitted by space satellites and planetary probes.

Vector processors really shine when two signal vectors must be processed together. For instance, a vector representing an incoming signal may be processed with a previously stored reference signal to detect differences between the two signals, or it may be processed with coefficients in a filtering application. With a vector processor, whole blocks can be operated on at once, but with a conventional digital signal processor, successive pairs of signals, called couples or scalars, must be multiplied, accumulated, and stored. All these operations involve memory accesses and other system overhead.

Vector processors also simplify windowing, another form of signal processing. For instance, a processor operating faster than real time can process overlapping blocks of signal samples. This windowing technique prevents discontinuities in the output data and in any analog signal outputs produced by digital-to-analog converters.

Each point in a window can represent a weight or a sample. So if two vectors are processed, one can be a filter and the other a block of samples. By weighting points differently, for example, a designer can control filter shapes in the frequency domain. Other tricks of the windowing trade include magnifying parts of an image.



3. BEYOND BENCHMARKS. Systems Processors handle a range of signal processing: (a) a VSP can implement a quadrature receiver Doppler-shift measurement system; (b) complex systems such as radar processors can use both the VSP and DFP.

variety of signal-processing functions.

One 8-tap DFP, the ZR33881, has a throughput of 340 Mb/s at an input data rate of 20 MHz—up to 10 times the speed of conventional general-purpose DSPs. The throughput is more than required for convolving 256-by-256-pixel images at a rate of 60 frames per second. But because it contains one processor per tap, a DFP can also be used in much more complex applications. Its specifications include a guarantee that it can calculate up to more than 1,024 taps with no overflow. In addition, the DFP family is fully cascadable, so multiple processors can be implemented in a system.

BRAINS AND BRAWN

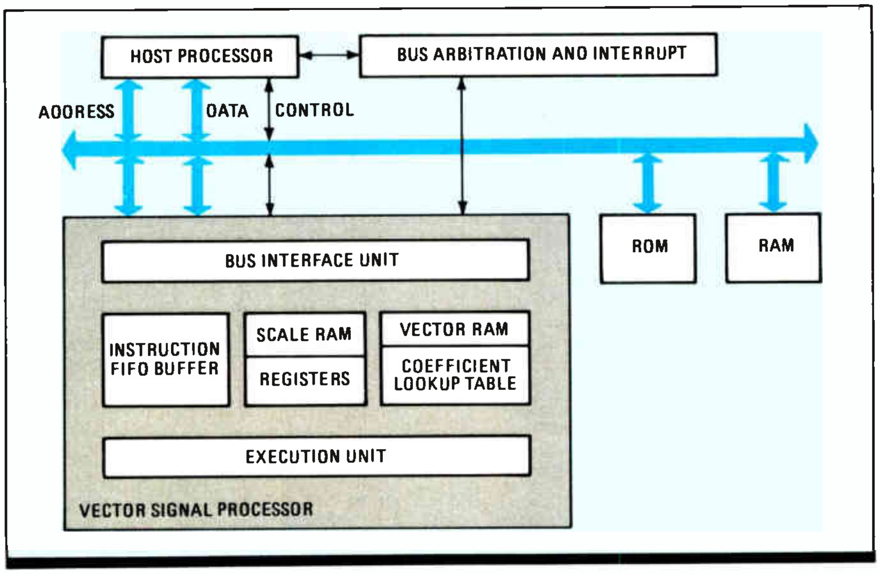
Together, the VSP and DFP cover an applications range that previously required signal-processing systems built with multipliers, accumulators, and other building blocks (Fig. 2). Alternatives were systems built with bit-slice bipolar processors and building blocks, and even array processors. A range of systems can be built with a single VSP and with both devices (Fig. 3). In such complex and high-performance systems as TV modems (image-compression and -transmission systems for teleconferencing), speech recognition, X-ray image processing, and radar-beam steering, the VSP provides the frequency-domain brains and the DFP supplies the time-domain brawn.

Zoran says multiprocessor configurations are practical with the VSP because the device contains a DMA channel as well as embedded algorithms. These overcome the system-bus loading and contention problems that would be created if each processor had to execute large amounts of code at high speed. In addition, a dual-processor architecture (a microprocessor-style bus interface unit and an execution unit that operate concurrently) allows the VSP to perform several different functions concurrently with the efficiency of a concurrent processor.

Even though Zoran developed the VSP for the high-performance market, the company envisions a proliferation of vector processing in much broader fields; combinations of the DFP and VSP map well into such applications as image compression and radar processing, but the VSP can also be used as a stand-alone processor in many applications.

For instance, single-processor designs similar to a Doppler measurement system could be used in a portable blood-flow meter, a police radar, or a digital FM receiver. Zoran says that although other monolithic digital signal processors can perform the same functions, not even the advanced devices reported at this year's International Solid State Circuits Conference can perform them at a high enough frequency. So there's considerable logic behind Zoran's expectation that its Systems Processors also herald the next era in low-cost digital signal processing.

As Zoran executives put it, they've lowered the system overhead instead of waiting for submicron CMOS to raise the speed. In addition, there's a comparable reduction in system-development time. For instance, instead of encoding the mathematical operations of an FFT, the designer simply specifies the parameters in a high-level instruction. This approach also leverages the vector processor's block floating-point capability for added dynamic range. In the block floating-point mode, the relative dynamic range is 96 dB; in the fixed-point mode, the absolute dynamic range is 96 dB.



4. LOOSELY COUPLED. With a built-in direct-memory-access channel, the VSP can operate as a loosely coupled peripheral to a host processor.

With the price/performance barrier broken, digital signal-processing technology will indeed become pervasive, predicts John A. Ekiss, Zoran's president and chief executive officer. "At today's prices, a high-end-system manufacturer can replace a $20,000 box with a $2,000 board" by using Zoran's chips. "But as costs come down, a board will cost $200 and perhaps eventually $20." It was that prospect that impelled Ekiss to quit his job as vice president of Intel Corp. to join Zoran last year (see "For Zoran, systems before silicon," p. 65). At present, the ZR34161 VSP costs $700, the 4-tap ZR33481 DFP costs $275, and the 8-tap ZR33881 DFP costs $490 in low quantities off the shelf.

Unlike a conventional digital signal processor, the VSP is optimized for certain tasks, as is the DFP. Instead of assembly-language instructions that allow the designer to program any kind of operation, the VSP has a small set of 23 high-level instructions comparable to commands for intelligent peripherals. It excels in executing certain algorithms, including FFT, magnitude square/accumulate, cross multiply/accumulate, complex conjugate, and the like. It processes signal vectors best. Obviously, scalars could be processed as vectors with a length of one.

ALGORITHMS DICTATE ARCHITECTURE

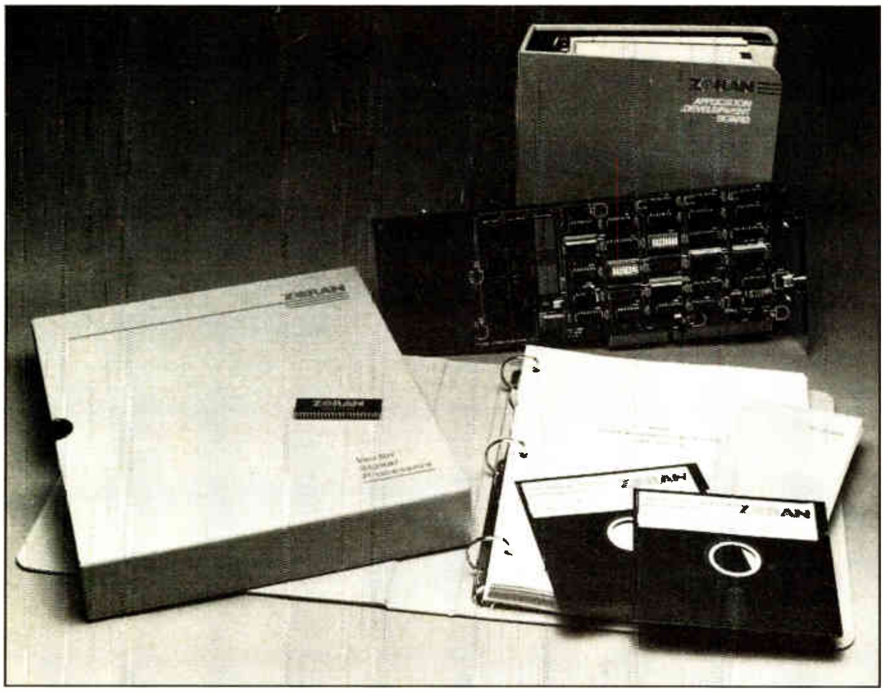
These specializations enabled Zoran's designers to optimize the VSP's architecture for real-time processing in the frequency domain. The architecture favors the FFT most, but like the other algorithms, its use is a designer's choice. "There is no magic architecture," says Almog. "That was precisely the problem we wanted to solve. Each algorithm dictates its own architecture."

The ZR34161 was designed for frequency-domain processing with the FFT as its core. In contrast, the DFPs were optimized for such vector functions as FIR filtering in the time domain, so their architecture relies on parallel processing and pipelining for speed. The VSP has a unique, vertically integrated architecture that includes all the functions needed to execute its algorithms, including vector-handling features, DMA controller, read-only-memory coefficients for 1,024 FFT points, data random-access memory, and a first-in first-out buffer for instructions.

The ZR34161 has a microprocessor-style bus interface unit and an execution unit that operate concurrently. The bus interface unit buffers addresses and data, stores up to four instructions in a FIFO buffer, and controls the bus and DMA channel (Fig. 4). It can operate either independently of the execution unit or in conjunction with it to support arithmetic logic operations requiring data. It can be either a bus master fetching its own data and instructions at clock rates to 10 MHz, or a bus slave receiving instructions and data from a host. But it always requests the bus from a host before using it, so the host remains the bus arbiter and can preempt the VSP if it needs the bus.

The VSP is designed for processing in the frequency domain; the digital filter processors perform such vector functions as FIR filtering in the time domain

All this allows the execution unit to operate as



5. Helpmates. Zoran offers application-development tools for its vector signal processor, including a simulator and an evaluation board.

a stand-alone signal-processing system with only an external input/output data buffer, to operate with larger program and data memories under the control of such devices as programmable logic arrays, and to operate as a loosely coupled coprocessor with standard microprocessors.

In the execution unit, the data RAM holds a data vector for arithmetic operations. The RAM stores 128 38-bit complex words, allowing the block floating-point FFT algorithm to use 19-bit real and imaginary values. Or the RAM may be partitioned into two complex 64-word sections for overlapped I/O and computation. After a vector is stored, it flows through a 17-by-17-bit multiplier with 25-bit real and imaginary accumulators designed for butterfly execution.

VSPs can be linked in parallel with a shared memory architecture, or they can be lined in an interlaced architecture with each chip having its own memory

Because the architecture favors frequency-domain processing, facilities to support the FFT abound in the execution unit. For instance, to support the processing of 1,024-point FFTs, the coefficient lookup table stores 256 16-bit coefficient values and generates up to 1,024 complex sine/cosine values. However, modulate and demodulate instructions can use the table, too. FFT scaling is fixed or automatic.

A key vector-processing element is the VSP's built-in block floating-point capability. If the programmer doesn't specify fixed-point operation, the architecture selects block floating-point operation. The block floating-point arithmetic associates an exponent with a vector, and the corresponding FFT scale values generate the scale value. Data vectors are rescaled using the scale parameter in the FFT instruction. This is analogous to adjusting exponents on two floating-point numbers before addition. A vector can be scaled as a complete vector or as equal-sized blocks.

Speeds for 1,024-point complex FFTs are 2.4 ms in fixed-point and 3.3 ms in block floating-point. These times can be cut by more than half by paralleling VSPs. For instance, if four VSPs operate in parallel in a system with shared memory architecture, a 1,024-point complex FFT can be performed in only 1.3 ms. With an interlaced architecture (each VSP with its own memory), throughput improvements grow almost linearly. Fixed-point operation gains speed at the expense of dynamic range. That is, the VSP's relative dynamic range of 96 dB in the block floating-point mode becomes an absolute dynamic range of 96 dB in the fixed-point mode. In some cases, a relative dynamic range of 96 dB is equal to an absolute dynamic range greater than 190 dB, Zoran points out.

The 23 high-level instructions range in size from 1 to 3 words. Because overlapping improves FFT execution speed, instructions executed by the ALU can overlap with the bus-interface-unit memory I/O or partially overlap, and the bus interface unit shares the internal RAM bus with the ALU. The memory instructions handle vector on- and off-processor transfers.

Eleven instructions use only internal memory. Besides the FFT, they include:

- Magnitude square/accumulate.
- Modulate.
- Demodulate.
- Cross multiply/accumulate.
- Complex conjugate.
- Accumulate real.
- Accumulate imaginary.
- Absolute value.
- Scale.
- Scale literal.

Vector multiply real/accumulate, vector add real, and vector add complex can all use external memory. In addition, there are the usual control instructions: jump halt and no operation.

A DFP contains four or eight filter cells, each a processor built around an 8-by-8-bit multiplier, decimation registers, related logic, and a 26-bit accumulator. The output stage contains an additional accumulator for adding and shifting cell outputs. The multipliers operate on data bytes and coefficient bytes. These don't need instructions. Nor are the DFPs generic digital filters; they have embedded algorithms (FIRs and convolutions). But they can perform a large variety of functions in different configurations.

The basic mode is a 1-d FIR filter, but a DFP can also serve as a 2-d FIR filter for digital video, machine vision, and other imaging applications. The DFPs can also be used for such functions as adaptive filters, butterfly computers, and complex multiply-adders. Major options include correlation/convolution, decimation, and interpolation. For instance, two 20-MHz 4-tap chips connected to a multiplexer comprise an interpolation-by-two FIR filter with an output rate of 40 MHz. DFP tools include a $995 design system that runs on an IBM PC AT computer (a package for the VAX computer is also available for $1,495), a $2,000 hardware development system, and a training course. □

FOR ZORAN, SYSTEMS BEFORE SILICON

Zoran Corp. was destined to become a semiconductor company—after all, *zoran* means "silicon" in Hebrew—when it was founded in December 1981. More than four years elapsed before the Santa Clara, Calif., company had a manufacturing plant of its own, yet when Zoran did start up a wafer-fabrication line to produce its initial family of vector signal-processing circuits, the company was already one of the largest manufacturers dedicated to digital signal processors.

This unusual history can be explained by the fact that Zoran began by defining its mission—seeking new ways to solve system problems—and then establishing a semiconductor technology. It is almost taken for granted in Silicon Valley that new semiconductor processes lead to new products, but Zoran's founders viewed that as putting the cart before the horse.

"Because we decided to focus primarily on architectural solutions to performance problems, we did not need our own wafer-fabrication line until later on," explains Levy Gerzberg, executive vice president and chief technical officer. "We worked on system issues and applications issues instead of putting resources into production facilities."

One reason Zoran delayed wafer fabrication, Gerzberg says, is that "we are convinced that vertical integration takes the right technology at the right time. Companies develop their own cultures, and if you build a semiconductor company first, if you make components not aimed at specific systems problems, you may build up too much inertia in the wrong direction. It's hard to attract systems engineers into a semiconductor company—they must be convinced you have a systems viewpoint."

Gerzberg and cofounder Yuval Almog, senior vice president, did not start out with the idea of developing vector signal processors. Gerzberg, 41, and Almog, 36, met in California shortly before they agreed to form Zoran Corp. The two men had followed very different career paths but realized that their experiences were complementary.

At the time, Gerzberg was associate director and senior research associate of the Stanford University Electronics Laboratories in Palo Alto. He has more than 15 years of experience in semiconductor technology, systems, and digital signal processing. He holds a doctorate in electrical engineering from Stanford and degrees in electrical engineering and medical electronics from the Technion Israel Institute of Technology. Gerzberg was president of Zoran until last year, when John Ekiss joined the company as president and chief executive officer.

Almog, in contrast, had worked on product planning and analysis at Raychem Corp., Menlo Park, Calif., and was Raychem's military electronics marketing manager when he cofounded Zoran. He also served eight years in the Israeli Air Force as a pilot, systems officer, and electronics instructor. He has bachelor's degrees in mathematics and computer science from the University of Alabama and a master's degree in management from the Massachusetts Institute of Technology. Almog is senior vice president for business strategy.

Ekiss, 51, holds a master's degree in electrical engineering from Carnegie-Mellon University, Pittsburgh. He has more than 27 years of experience in semiconductor engineering, manufacturing, and general management. Formerly a vice president of Intel Corp. and general manager of Intel's Arizona-based Special Components Division, Ekiss previously held positions at Motorola, Philco/Ford, and RCA.

In late April 1982, the embryonic company won the backing of two venture capitalists—Adler & Co. of New York

THE TEAM. Zoran's management team consists of (left to right) Levy Gerzberg, executive vice president; Yuval Almog, senior vice president; and John Ekiss, president and CEO.

and Elron Electronics Industries Ltd. of Israel—on the strength of a 10-page document describing their ideas. But to clinch the deal, they had to draft a business plan, and the plan began with their first choice: a DSP product line.

For almost a year, Zoran operated out of Almog's garage in Palo Alto. Almog, who had quit his job at Raychem, worked full-time on product planning and definition and on a detailed model of how the company should grow, while Gerzberg, who was still engaged in other research at Stanford, worked part-time at other facilities on the underlying semiconductor and DSP technology.

"We started to integrate VLSI expertise into the company by hiring the right people," Gerzberg says. "We focused a small team on system issues, architecture, microprocessor-related considerations, and interconnection technology. In the VLSI area, we concentrated on interconnections. We saw interconnections as the major limitation on chip performance. So instead of becoming experts in growing very thin oxide, we left that to the big guys. Even at 2-μm density, a lot of companies are still fighting problems with contacts and double-layer metalization."

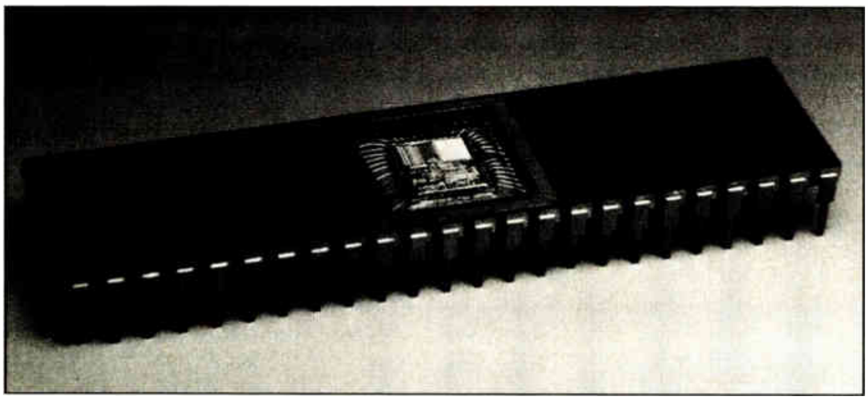
The buildup began in the first half of 1983, when Zoran began hiring technology specialists to work with Gerzberg. Early in 1983, the firm opened a design center in Sunnyvale, Calif., for its system engineers, and soon afterward opened a second design center in Haifa, Israel. The Haifa center was started up by Rafi Retter, now director of product development. Retter, architect of the ZR34161 VSP (vector signal processor), had been with Intel Corp.'s design center in Haifa.

By the end of 1984, Zoran had about 75 employees in the two design centers. Almog was getting favorable feedback on product concepts from leading manufacturers of signal-processing systems, and the founders were convinced that Zoran had both the potential and the opportunity to become a leading manufacturer of DSP circuits. During that phase, Almog says, he met again and again with about 120 potential customers. Those discussions led not to one product definition but to a whole array of potential product lines and families. "We were sure then that we were on the right track," Almog says.

Because of the growing interest in emerging applications for monolithic signal processors, DSP market projections were climbing well beyond a billion dollars a year. Integrated Circuit Engineering, a Scottsdale, Ariz., consulting company, recently estimated that chip sales could grow as much as 400%—to over \$3 billion by 1990.

"We knew from reports on experimental circuits that we could enter the high-end market with a clear technical lead," Gerzberg says. High-end applications are abundant in any of Zoran's key market segments—telecommunications, medical electronics, military electronics, instrumentation, industrial automation, digital audio/video, and such computer products as array processors.

In 1984, Zoran began searching for a semiconductor industry executive to head the company's transition into production. Once again, the founders tapped Intel. Ekiss was a vice president of Intel and general manager of the Special Components Division, which produces microcontroller, telecommunications, automotive, military, and custom products (among other signal-processing products, the division made the venerable 2920, the first monolithic signal processor). The founders approached Ekiss, and in February 1985 he joined Zoran.



PROCESSOR PACKAGE. Zoran's ZR34161 VSP in a 48-pin DIP handles vectors as long as 128 complex words and uses high-level instructions to execute embedded algorithms.

Ekiss recalls his first discussions with Gerzberg and Almog. "After a three-hour meeting one night, I told my wife, 'If these guys can execute what they have, this will be fantastic,' " he says. "The more they revealed, the more I became convinced that this was a major opportunity to build not just a company but a very significant company that could position itself really well against the major companies."

Ekiss' first task was raising more capital to fund manufacturing, finish developing the initial products, develop simulators and other design tools, hire more people, and start up a marketing department. The third round of financing, completed in October 1985, brought in more than \$22 million—a record for Silicon Valley, if not the world. All told, investors have put \$27 million into Zoran since it was founded. In addition to Adler and Elron, there are 17 other investors, including Concord Partners (Dillon Read); Grace Ventures; Investment Advisors; Kleiner Perkins Caufield & Byers; Mitsui; Montgomery Securities; Vista Ventures; and Welsh, Carson, Anderson & Stowe.

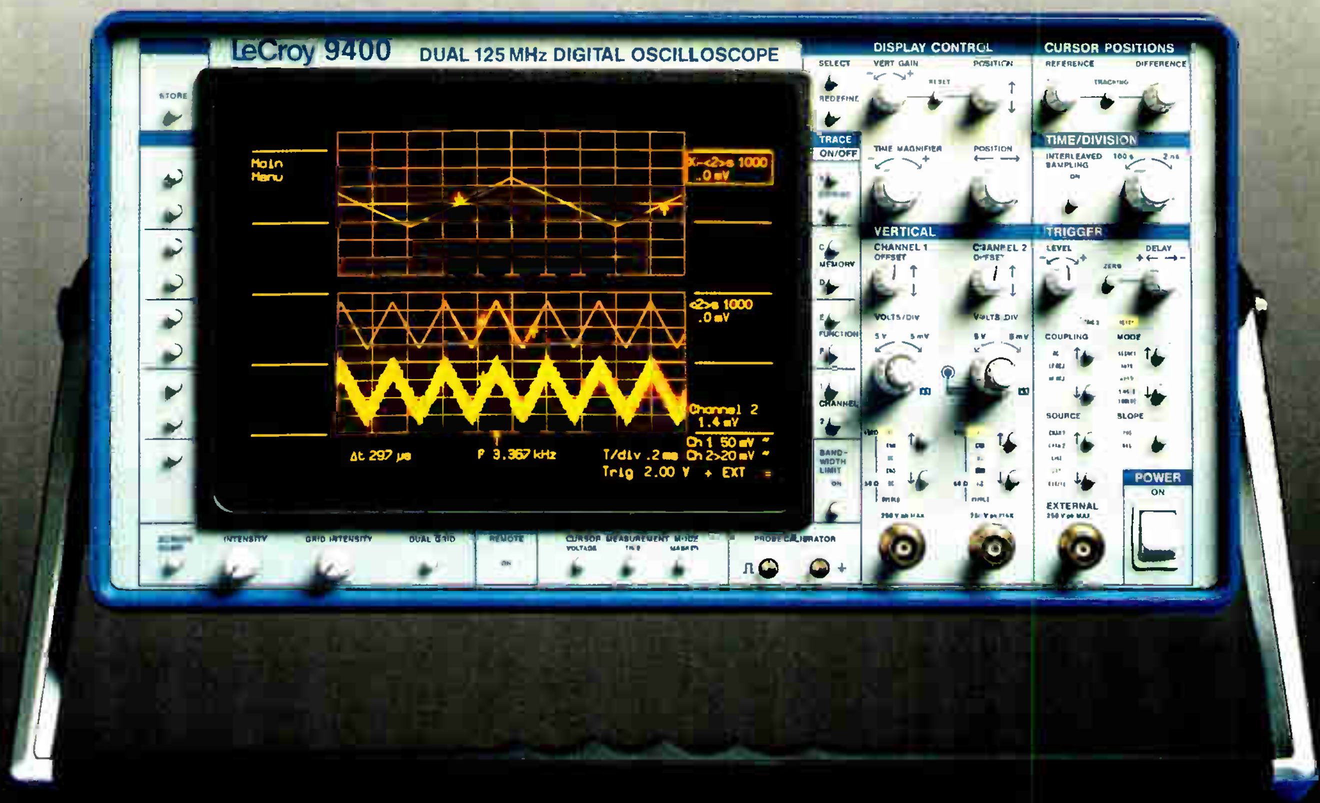
Zoran had already identified a suitable plant, complete with an advanced fabrication line for 4-in. CMOS wafers. It was an almost-new plant, built by Storage Technology Corp. before it ran into severe financial difficulties. Last August, Zoran bought the fab line for about 25¢ on the dollar, and finally became a semiconductor manufacturer.

In December, the first working product—a digital filter processor—came off the line and went to key customers. One customer wrote, after evaluating the processor, that the device would enable him to replace 10 boards with a single board of equal performance or, conversely, build a system 10 times as powerful with 10 boards.

Zoran now employs more than 100 people. "We are probably the world's largest dedicated DSP manufacturer now," Ekiss says. As for the future, he adds, "It's important to remember that Zoran started from scratch with systems expertise. Zoran does not have to go through that transition later on. It will not be easy for larger companies to get systems expertise and integrate it with their company. Every semiconductor company has its own charter, and I believe that the way Zoran grew will give us a significant advantage." □

THE BEST.

...... in signal processing



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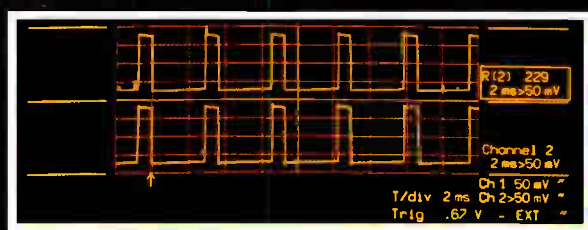

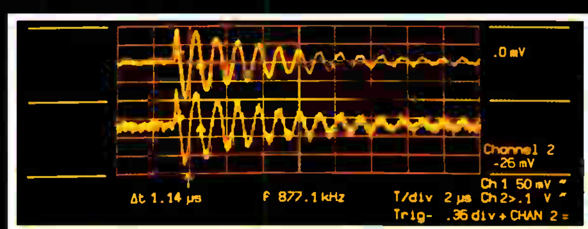

Top: Summation averaging over 1,000 waveforms, expansion and high resolution frequency measurement all shown in one display.

Middle: Extrema Mode shows glitches in digital circuitry, logged over 229 acquired waveforms.

Below: Digital filtering with a 9-point filter smooths noisy transient.

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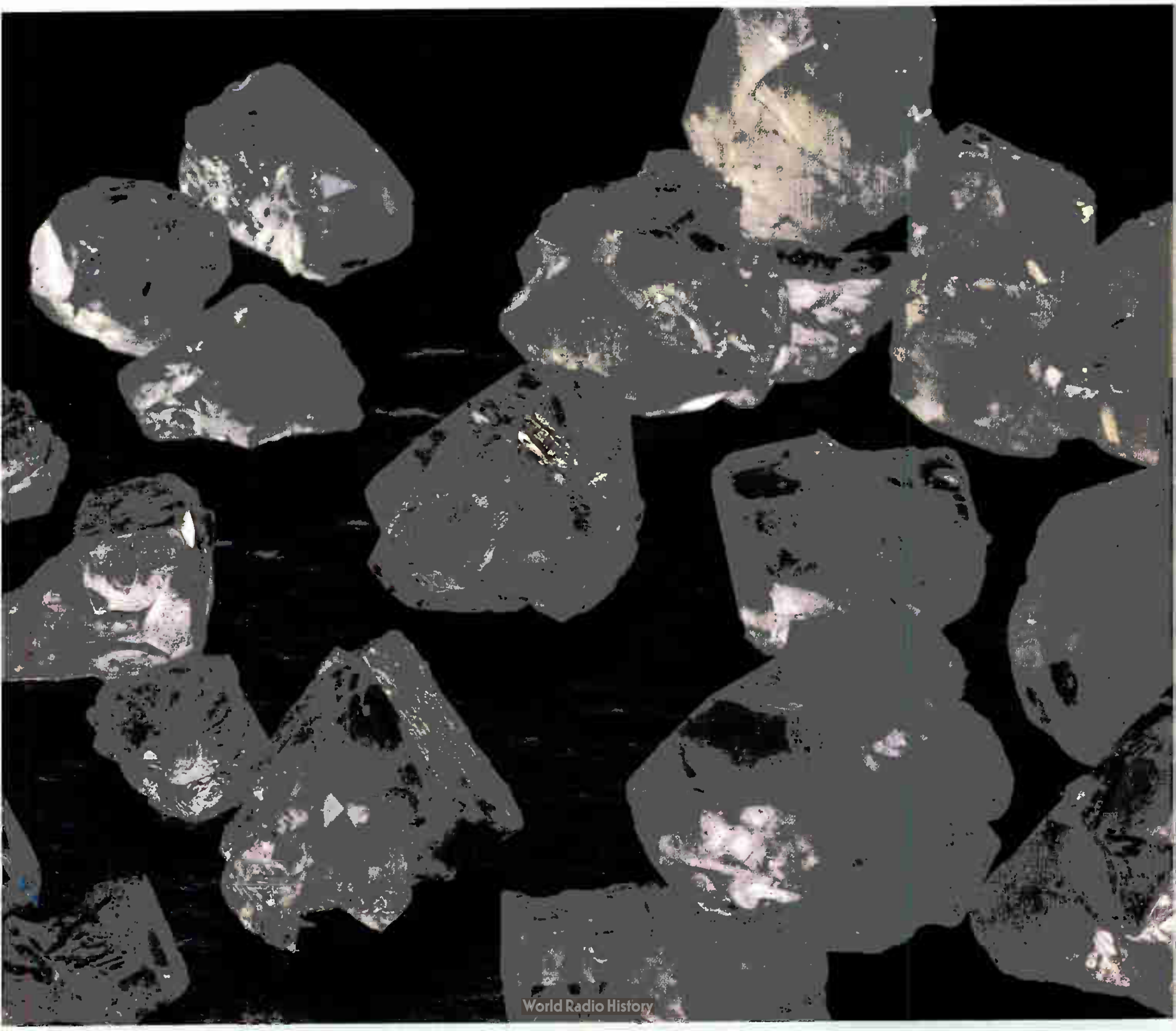
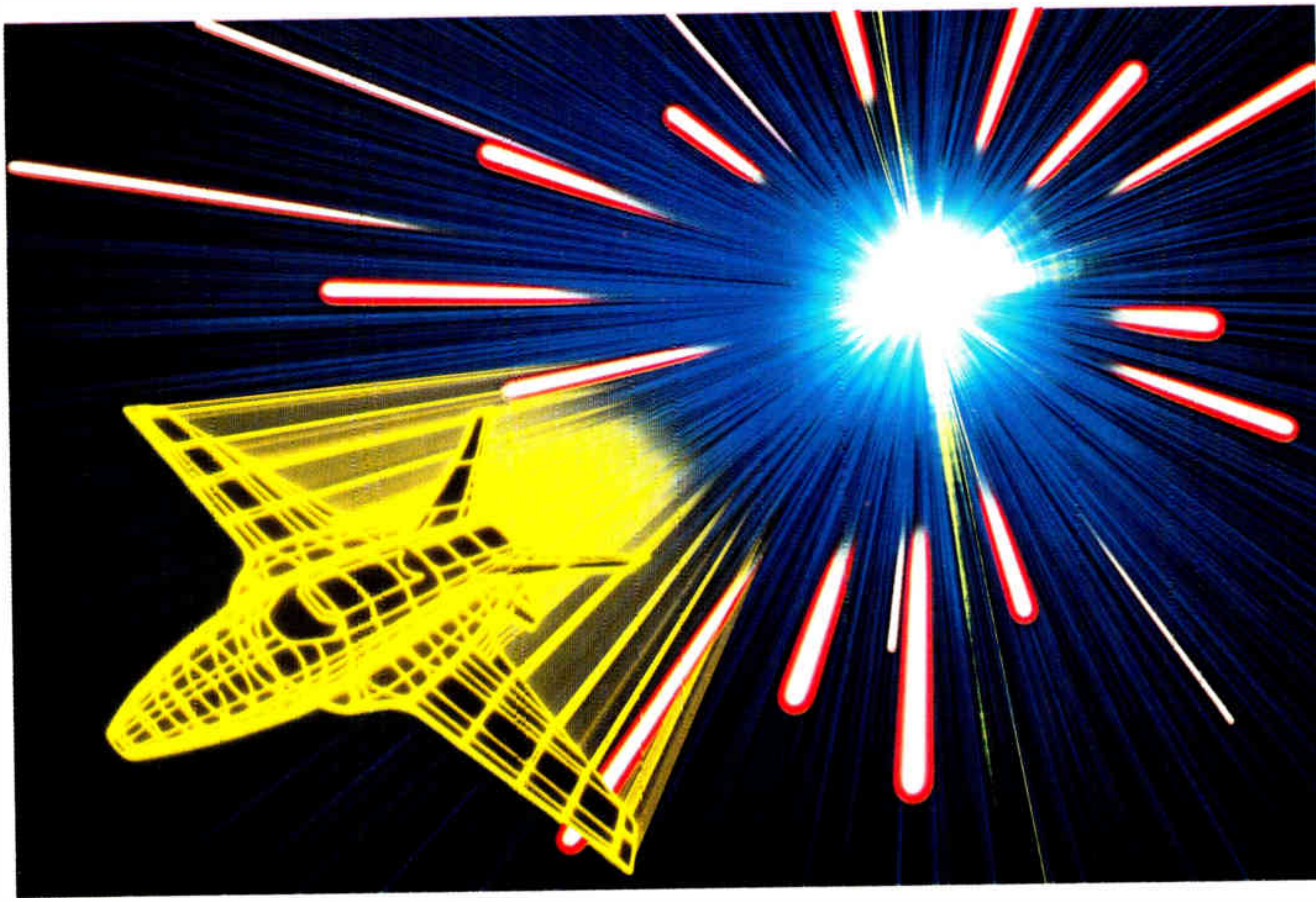
Circle 67 For Demonstration

Circle 143 For Information





NEC INTRODUCES WORLD'S FASTEST FLOATING-POINT SIGNAL PROCESSOR.

Our μPD77230 Advanced Signal Processor breaks the floating-point barrier in digital signal processing (DSP) with unprecedented speed and accuracy.

The new single-chip CMOS DSP races through 32-bit full floating-point arithmetic at 13.4 MFLOPS. It executes up to 6 concurrent operations, including multiply and accumulate, in a 150ns cycle.

With 32-bit floating-point precision, our advanced signal processor eliminates problems with round-off error, quantization noise, scaling, limit cycles and over/underflow. It is unique in offering a 55-bit multiplier result (8-bit exponent, 47-bit mantissa), with eight 55-bit registers, 47-bit ALU and barrel shifter.

In addition to its large internal memory blocks (512 × 32 × 2 data RAM, 2K × 32 program ROM and 1K × 32 data ROM), the 77230 provides external expansion up to 4K of program RAM and 8K of data RAM. Serial and parallel I/O also add flexibility. The serial interface allows cascading, links with codecs and AD converters while the parallel interface supports master- and slave-mode operations.

The 77230 is ideal for image processing, graphics workstations, telecom and other applications requiring high speed and high precision.

NUMBER 135

NEW ZEALAND GOES DIGITAL WITH NEW FOTS AND NEAX61.

Plans for a nationwide Integrated Digital Network (IDN) in New Zealand, where the telephone ownership rate is among the highest in the world, are rapidly taking shape.

The New Zealand Post Office selected NEC to supply state-of-the-art 140MB fiber optic transmission systems (FOTS) and digital switches that will bring the digital future clearly into view.

NEC will provide all the necessary optical terminal and repeater equipment for the fiber optic systems to be installed in links covering Wellington, Auckland, and other major cities.

NEC's 140MB FOTS provides high-quality communications paths equivalent to 1,920 telephone channels. High-performance optical devices enable long repeater span. It also features in-service system monitoring functions, low power consumption and compact size. A slim rack, measuring 2.75m(H) × 0.12m(W) × 0.225m(D), accommodates three terminal systems.

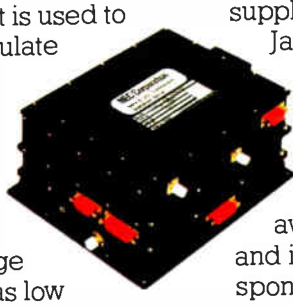
For the development of its ISDN, the New Zealand Post Office selected NEC's enhanced NEAX61 digital switching system with ISDN capability. Nearly 100 systems, including toll and international switches, are to be supplied within a five-year period.

NEAX61 digital switches with an aggregate total of 5 million lines are now in service in 36 countries.

NEC TRANSPONDERS SELECTED FOR INMARSAT-2.

NEC satellite transponders will play a key role in INMARSAT-2, the second generation of international maritime communications satellites.

NEC was recently awarded a contract from British Aerospace Public Limited Company to supply TT&C C-band transponders. This technology-intensive equipment is used to receive and demodulate telecommand signals, to transmit telemetry signals, and for ranging.



The transponder design will include various leading-edge technologies such as low noise amplifiers (Noise figure: 2.5dB), SAW filters to achieve excellent band-rejection performance (60dB min. ±2MHz from center frequency), threshold extension FM demodulation to achieve high sensitivity, and hybrid microwave ICs to minimize equipment size and weight, plus high-efficiency high-power amplifiers (RF output: 6W min.).

As one of the world's leading suppliers of satellite transponders, NEC has contributed to a number of international programs, supplying hundreds of advanced transponders for INTELSAT-IV, IV-A and VI series of communications satellites.

NEC has also integrated and supplied all the transponders for Japan's communications satellites, including the world's first two Ka-band satellites, and various TT&C (tracking, telemetry and command) transponders.

Additionally, NEC was awarded a contract to develop and integrate high reliability transponders for BS-3a and -3b, Japan's next generation of direct broadcasting satellites.

ALL-SOLID-STATE UHF TV TRANSMITTERS.

The latest 30kW UHF TV transmitter from NEC sets a new standard for high output power in all-solid-state design.

The 30kW transmitter incorporates many enhancements including high-performance exciters, powerful transistor power amplifiers, low-loss RF combiners and high-efficiency switching regulators.

The 1.2kW transistor power amplifier, utilizing reliable, high-power and high-gain (120W typical and 7dB min. at 860MHz) bipolar transistors which were developed in-house, features a remarkably reduced component count—only 1.7 times larger than the conventional 300W PA.

Compared to tube types, the new transmitter features greatly enhanced economy and reliability. Safety and maintainability are also improved, while power consumption is reduced by approximately half.

NEC's new all-solid-state UHF TV transmitter series includes 15kW, 10kW, 5kW and 3kW models. A 30kW system is already in satisfactory operation.

NEC

WHY SILICON COMPILERS ARE STARTING TO TAKE OFF

Today's compilers vastly speed up the job of creating complex integrated circuits, but mostly for those engineers who are already skilled in design methodology

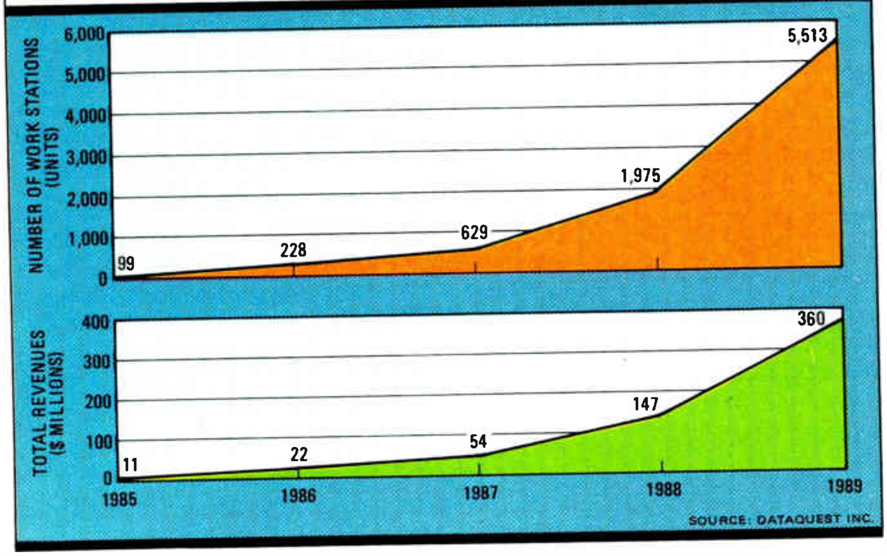
by Jonah McLeod

Five years after silicon compilation was introduced to the chip-design community, it is finally gaining acceptance. Silicon compilation promises to automatically synthesize the design of integrated circuits and therefore move IC design into the hands of system designers. Today's compilers haven't fulfilled that promise because they still require extensive knowledge of chip-design methodology. However, IC designers are welcoming them with open arms because they greatly reduce the effort required to create complex circuits.

One prediction of the growth of silicon compilation comes from Dataquest Inc. The San Jose, Calif., market research firm says a mere 99 work stations with silicon-compilation capability were shipped in 1985, at an average selling price of $110,000 per system (see chart). That converted into only $11 million in revenue last year. Dataquest expects the unit shipments and revenue to more than double in 1986 and again in 1987. Moreover, 1988 and 1989 should nearly treble each previous year's shipments and revenue.

A major impediment to the acceptance of silicon compilation has been the lack of enthusiastic support from silicon foundries. Because a generic silicon compiler produces the same layout regardless of the fab line that produces the final chip, the foundry becomes a commodity supplier of silicon with no way to differentiate its product from that of the competition. But now foundries are beginning to develop their own silicon compilers. The makers of silicon compilers are ramping up operations too, and companies selling compilation tools to foundries are springing up.

SILICON COMPILERS ARE POISED TO TAKE OFF



One healthy trend is a new emphasis on accountability, with foundries and compiler makers striving to pinpoint the problems that result in a faulty design. Moreover, compilation technology is making significant strides forward, with system-level simulation and new compaction techniques starting to appear. Over the horizon are new departures: compilers that produce the equivalent of hand-design circuits and compilers that work solely from functional descriptions.

Silicon compilation, like gate arrays and standard cells, was developed to shorten chip-design cycles, which are often longer than the lifetime of the product in which they are used. However, standard cells and gate arrays do not let a designer work at a system-design level of abstraction to produce very large-scale implementations. As an alternative, compilation is most effective when the designs contain several complex macrocells, such as microprocessors, multipliers, random-access and read-only memories, and programmable logic arrays. Gate arrays and standard cells do not offer the number of logic functions needed to implement this level of design complexity: typical compiled chips contain upward of 50,000 transistors.

In the silicon-compilation design process, the designer enters a circuit description of components he needs to implement his final design, and the description is translated into a layout on silicon. The high-level description is first broken down into smaller functional block descriptions: arithmetic logic unit, PLA, RAM, ROM, etc. They, in turn, are broken down into smaller logical components, such as AND and OR gates. Next, the gates are translated into a basic circuit configuration, using such components as transistors, wires, and contacts. These circuit elements are then laid out on silicon. Up to this point, compilation is independent of process technology, but the layout changes with each process: n-MOS, CMOS, bipolar, or gallium arsenide.

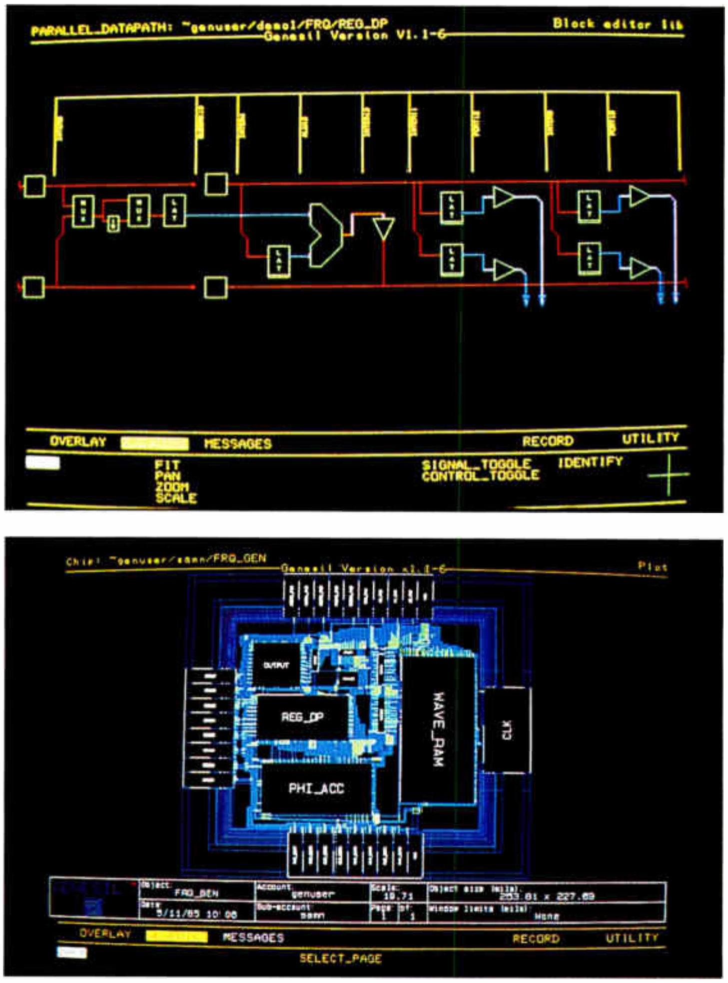
FACILITATING DESIGN CHANGES

At each level of the compilation hierarchy—functional, logical, circuit, and topological—a silicon compiler synthesizes models of the circuit (Fig. 1). At each level, it can provide functional simulation, timing models, timing simulation, power estimates, test vectors, and layouts. A designer can take a snapshot of any or all of these six aspects of his design at any point in the compilation sequence.

"As a design grows in detail, the ability to obtain a variety of estimates about size, power, and performance lets a designer make incremental mid-course changes instead of waiting until the design is complete," says Steven C. Johnson, vice president of engineering at Silicon Compilers Inc., a San Jose seller of compilation systems. "In this way, a designer has a 'what-if' capability in the design process." Johnson argues that only design tools with such a capability are true silicon compilers (see p. 77).

A silicon compiler operates from stored sets of rules from which it can synthesize complex building blocks. "The designer may want a multiplexer with seven data inputs having two control lines and three output lines," says Philip Rosenbaum, vice president of marketing at Silicon Design Laboratories Inc., a Liberty Corner, N. J., maker of compilation tools for foundries. "The compiler creates this circuit from an input description, and it is uniquely configured for that design requirement."

One problem with silicon compilation comes when the designer tries to implement a circuit in the different silicon processes of various found-



1. NO HANDS. After the designer enters a schematic (a), Silicon Compiler's software automatically produces a chip layout (b).

ries. Most compilers use a technique called lambda design rules in order to approximate each foundry's design rules. They perform a linear shrink of their own primitive design rules to fit the different foundry processes. So to convert a circuit implemented in a 2-μm CMOS process into 1.2-μm CMOS, the compiler performs a linear shrink of the basic cells. But in hand optimization, the 1.2-μm CMOS cells will typically undergo a nonlinear reduction. In contrast, the compiler using lambda design rules is a less-than-optimum approximation of any new process technology.

Problems arise when a designer using a lambda-rule compiler tries out a design in different foundries' processes. "It is not really reasonable or fair to make the comparison" in this way, "but everyone using the compilers will do so," says Larry Jack, military strategic marketing manager at Honeywell Inc.'s Digital Product Center in Colorado Springs. If the designer performed a hand design using each foundry's individual design rules, the comparison would be much better.

The ability of silicon compilers to lay out and re-lay out a design quickly has created somewhat of a dilemma for silicon foundries. If, for

STEVEN C. JOHNSON of Silicon Compilers says silicon compilation lets designers do a "what-if" analysis on a chip design.

instance, three competing foundries each provide its design rules to a generic silicon-compiler vendor, a designer can compile his circuit for each of the three foundries and from the results make a choice of which to use.

"The problem to this approach is that it takes away all the proprietary advantage of the foundry," explains Rosenbaum. "The foundry has a proprietary expertise in IC process technology—its ability to create a three-input NAND gate in the smallest geometry possible, for example—which it wants to protect. It does not want to share that."

THE ROLE OF COMPETITION

Sam Brown of compiler maker Seattle Silicon Technology Inc. disagrees. "There is too much competition for any one foundry to believe it can significantly differentiate its foundry capability and to effectively supply a customer by itself," says the executive vice president of the Seattle-based company. "Customers will always want a second source to be able to fab the product at other foundries." In addition, Brown points out, there is too much competition among foundries for any one to cut off a potential avenue of business. Thus, it is in a foundry's best interest to support silicon-compilation companies by providing their process rules.

At least one foundry executive agrees. "Our business is to sell silicon," says Terry Walthers, applications manager at Gould AMI Semiconductors Inc., Santa Clara, Calif. "We support libraries of components on computer-aided-engineering work stations for designers who want to develop a design and give it to us to lay out. We also support third-party silicon-compiler companies. We want to maximize the number of designs we do. We don't care which system it comes off of."

But foundries are changing the way they support silicon compilation. Instead of providing their design rules to third-party compiler vendors, they are beginning to write their own compilers.

One foundry that has long provided its own silicon compilers is VLSI Technologies Inc. "We were the earliest to market silicon compilers to our customers," says Andy Haines, the San Jose company's ASIC strategic marketing manager. VTI provides schematic capture, simulation, and layout models with a set of general-purpose compilers: RAM, ROM, PLA, and random logic. In addition, the company also provides compilers for a 2901 bit-slice microprocessor and an N-by-N multiplier for special-purpose applications.

MORE ON THE WAY

These are third-generation compilers implemented for 2-μm double-metal CMOS. The company plans a future generation of compilers based on 1.5-μm double-metal CMOS. "Existing designs can be converted and will receive the full benefit of the new technology," says Haines.

VTI is in the fortunate position of having a two-to-three-year head start on other foundries in developing a compiler tool kit. Moreover, its compilers were all generated internally, whereas other foundries have had to go to outside sources for their tools. And, addressing the second-source concerns of its customers, VTI's data base can be run at other foundries that have process compatibility. These include Sierra Semiconductor Corp. and Zilog Corp., both of San Jose, and Rockwell International Corp.'s Semiconductor Products Division in Newport Beach, Calif.

In spite of its openness to third-party compilers, Gould sees the value of a foundry-offered compiler and is developing its own. Terry Walthers says "Gould Research Laboratories in Rolling Meadows, Ill., is developing its own programming language to create the compiler."

Two makers of silicon-compilation tools, Silicon Design Labs and SDA Systems Inc., Santa Clara, were the first to recognize that foundries competing with VTI could benefit from offering silicon compilers optimized for their own processing technologies. "We decided to provide the foundries the tools to create their own compilers so they could support them and then go out and support the system designer," Rosenbaum explains. The foundry can differentiate itself by offering its own compilers optimized to its fabrication facility.

Other foundries are beginning to jump onto the compiler bandwagon. For example, NCR Corp. of Dayton, Ohio, announced at the Design Automation Conference in Las Vegas early this month that it was using Silicon Design Labs' tools to write compilers for most of its macrocell library.

SDA Systems has a similar agreement with Harris Semiconductor. And Motorola is going to use Silicon Compiler's software tools to develop compilers of its macrocell library.

Foundry-originated compilers help solve the finger-pointing problem that can occur when a system designer brings to a foundry a design that has been compiled with a third party's software tools. Who's at fault if a design does not work once it has been implemented in silicon: the system designer, the foundry, or the software vendor? "When the foundry provides a turnkey system for the system designer, one potential source of error, the third-party software vendor, is eliminated," says Honeywell's Jack.

PHIL ROSENBAUM of Silicon Design Labs says foundries that write their own compilers can better support the system designer.

From the designer's point of view, dealing directly with the foundry helps reduce the finger-pointing problem considerably. "The quality of the output from the compiler is what needs to be controlled," says Jack. "How accurately does it create silicon designs that match what can be built? How exhaustively was the design simulated? Was the simulator capable of catching all the critical problems?"

In a typical design project, the system designer comes to the foundry support staff with questions such as: How producible is the part? How is the designer going to package the chip? How fast is the design expected to operate? In answering these questions, the foundry is working with the designer to provide a critical design review before he provides a tape to generate a chip.

The makers of silicon-compiler systems are very much aware of the finger-pointing problem, too. They have increasingly begun shouldering the responsibility for ensuring that the system designer's circuit implemented with their compilers do work. Silicon Compilers and Seattle Silicon Technology both offer brokerage services that act as middlemen between the designer and the foundry.

However, guaranteeing that the prototype circuit from the foundry conforms to the specifications is only part of the problem. Often the silicon part is exactly what the designer specifies, but in the overall system design of which the silicon chip is only one of many components, the designer might make an error in connecting the chip with other system elements, interchanging input and output pins, and so on. Whether the foundry, compiler vendor, or designer makes the mistake, the result is the same: the designer becomes disenchanted with silicon compilation.

Silicon Compilers has taken steps to eliminate designer error as a source of problems in the total design process. It has developed a system-level simulator, which extends the simulation capability used in evaluating the IC. The simulator accepts behavioral descriptions of components external to the chip. The description is written in a Lisp-like behavioral modeling language called Genesil Interface Extensions, or Genie. With the language, complex systems can be described in less than a few hundred lines of code. "We have seen the language used to simulate entire video display terminals and complete minicomputer systems," says Johnson.

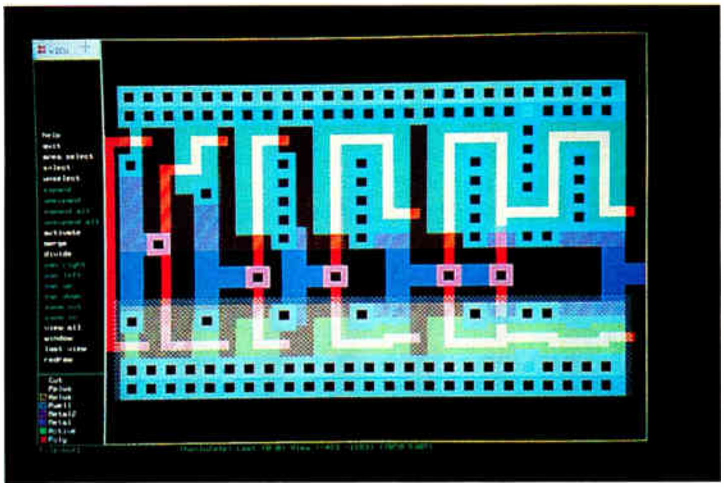
In addition, the simulator helps exercise the IC design at the system level. It can be used to create test vectors that stimulate the chip as if it were in its final system environment. The designer can program test vectors using the Genie language, or he can write microinstructions in a microcode assembler. With the microcode, the designer can store data in RAM or program code in ROM to simulate the final application.

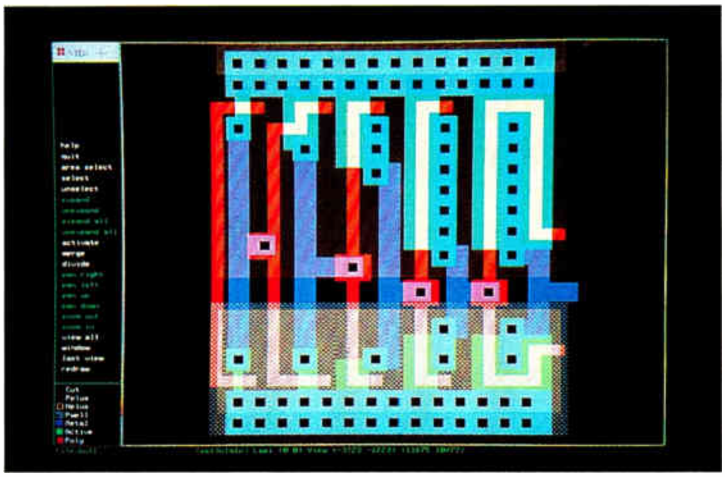
Using the Genie language, the designer can program test-vector-generation algorithms instead of programming 50,000 individual test vectors. With the algorithms, the simulator can simulate the behavior and function of a given circuit.

Dynamic compaction shrinks compiled designs much as a designer would, so it avoids the problems that occur in an across-the-board linear shrink

A real advantage of silicon compilation is the ability to transfer designs to denser processes: from 2-μm to 1.5-μm CMOS, for example. Thus, as process technology improves, existing designs can take advantage of the improvements in subsequent versions.

Seattle Silicon Technology has pioneered a technique called dynamic compaction that overcomes the problems of shrinking designs found in lambda-rule compilation. The technique automatically compiles a circuit that is compacted close to what can be accomplished by the layout designer doing the job by hand. It is unlike a linear shrink, in which the entire geometry of the circuit is reduced in size to the point where the design rules for the new process are not





2. SQUEEZE. Dynamic compaction reduces the interior geometry (a) of the cell to ensure the greatest possible reduction (b).

violated. Rather, dynamic compaction actually changes the interior geometry of the cell, says Seattle Silicon's Sam Brown.

This means a buffer that's rectangular in shape in one process could become square in the newer technology (Fig. 2). "Besides the aspect ratio being different, the interior layout of the cell can be different too," says Brown. "For example, the number of loops of poly wire can change."

In dynamic compaction, a module is defined in terms of the rules for the process—not in terms of a physical shape. So if one rule results in a greater shrink than another, the compaction process can accommodate the difference and shrink each device feature accordingly. That means it can map into individual design rules of different foundries much more effectively.

An even more attractive capability is being able to migrate from n-MOS to CMOS to emitter-coupled logic, GaAs, or silicon on sapphire. "We've been experimenting with GaAs and SOS compilers," says Dick Oettel, chief scientist for Seattle Silicon. "A circuit can be fabricated in low-cost CMOS in order to ensure it works, and then actually implemented in SOS or GaAs."

All the silicon compilers now in use are structured systems: the designer defines his chip in terms of building blocks such as ROM, RAM, PLAs, and N-by-N multipilers. Some three or four years away is the next step, an optimizing compiler that automatically lays out a circuit in the most optimum fashion possible. It would produce the equivalent of hand-designed circuits.

SOME CHANGES COMING

Gould AMI Semiconductors has taken steps in this direction already. The company has developed a system called Score, which allows Gould engineers to automatically generate the data for new standard cells based on customer-defined performance requirements. Score works with the basic transistor structures, just as a layout designer does.

"Score takes all the learning that layout designers use in laying out a design on silicon," says Terry Walthers at Gould. "It takes geometric tricks such as turning a transistor 90°, splitting transistors, and putting contacts down the center. All of this knowledge has been put into Score." Now a designer can specify, say, a J-K flip-flop with synchronous or asynchronous reset on it to be 250 μm high on the chip. Score lays out a flip-flop meeting these requirements.

Another parameter that can be specified is timing; for example, the J-K flip-flop must be able to switch in 3 ns. Score computes transistor sizes required to reach this timing specification. "The software sizes the transistor for the speed specified and lays it out physically," says Walthers. "This is what is now known in the industry as a cell compiler."

The main difference between a cell compiler such as Score and silicon compilers is that the foundry uses a cell compiler to replicate the IC layout designer's expertise. As such, the cell compiler is unavailable to the system designer, who simply provides a net list description to the foundry, which in turn lays out the design. By contrast, designers can use a silicon compiler to produce a physical layout that the foundry builds exactly as the compiler has specified. Eventually, however, cell compilers will be part of a general-purpose silicon compiler and so will be available to designers outside of foundries.

Ultimately, the design engineer will use behavioral compilers, which will work solely from functional descriptions. "The ideal silicon compiler will allow the designer to talk to it in a high-level language," says Walthers. "The designer might ask for a counter that counts to 63 bits, resets to 15 bits, adds number A to number B, and stores the result in an accumulator."

In other words, the designer give a high-level functional description of a circuit. In response, the compiler generates a circuit that behaves in that fashion. The software evaluates the circuit-design alternatives as an engineer would and then creates an IC using the best alternative. □

OPINION

SILICON COMPILATION IS NO HYPE

Silicon compilation has been in the news for the past two years, and some of the recent articles have questioned its viability. The interest at the recent Design Automation Conference leaves little doubt that this important technology has indeed taken root. But hype and confusion remain in the market; often design tools purporting to be silicon compilers are not worthy of the name.

Few people can define silicon compilation accurately; even fewer know what really makes it important. Let's remedy that:

Silicon compilation is a VLSI design methodology that provides designers timely feedback of all information needed to make reasonable design tradeoffs. It provides this feedback and foundry-independent, quality production tooling directly from abstract, system-level design inputs. It guarantees that the circuits so produced will operate in accordance with the feedback data provided.

Designers are constantly striving to find the safest and most cost-effective solution to their system design problem. If the feedback is comprehensive, accurate, and timely, then the designer can test alternative strategies and zero in on an optimal design quickly. This total feedback capability is found only in true silicon compilers.

Comprehensive feedback means all information necessary for design tradeoffs is available. For VLSI, this includes power, timing, die size, die cost, functionality, pinout, testability, and logical design-rule information. It also includes feedback from the data base as to the "currency" of all portions of the design.

Accurate feedback means power and timing feedback with all required data, such as critical paths, cycle time, or setup and hold times, based on the actual layout of all transistors and interconnections, not upon some stored macro. Also, accuracy demands functional simulation feedback that remains correct over all operating conditions and manufacturing processes.

What is timely feedback? Regardless of the circuit's complexity, the designer needs to see the impact of any change quickly; the quicker the feedback, the more variations can be explored.

It is the unique, simultaneous combination of all of these forms of feedback, coupled with abstract system-level design input, that defines silicon compilation and makes it important.

My table compares the features available in various design systems, with compilation requirements shown shaded. The section labeled "Hybrid" describes features found when layout compilers and work stations are combined.

Steven C. Johnson is vice president of engineering at Silicon Compilers Inc.

Silicon compilation is not simply layout compilation, as many believe. We're all getting pretty good at layout compilation. All silicon compiler vendors have synthesized module layouts at densities of 0.5 to 1.75 mil^2 per transistor (2-μm CMOS process), and chips at densities of 0.8 to 4.0 mil^2 per transistor, depending upon function; and all but one of us support multiple processes and IC manufacturers.

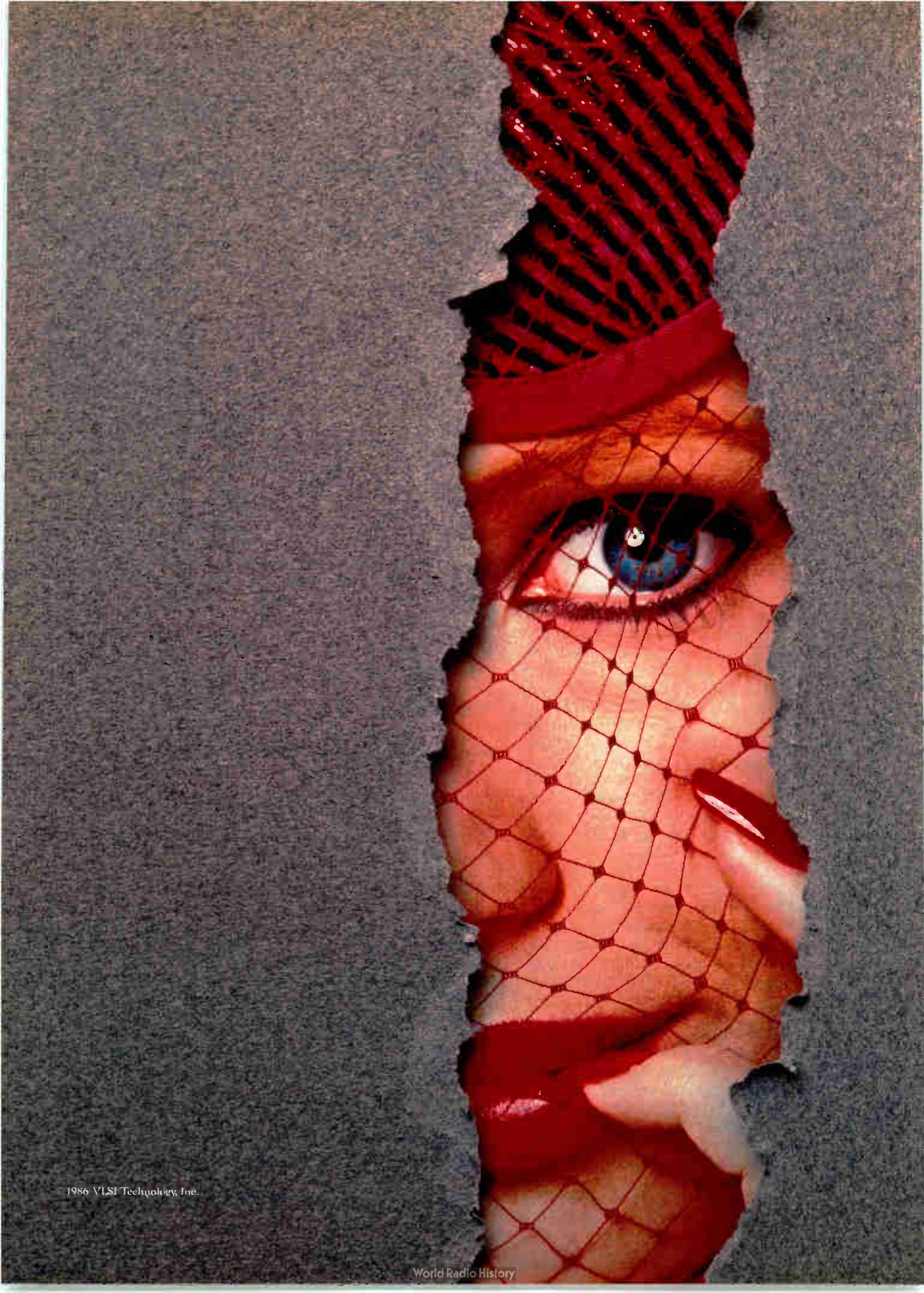
The metamorphosis to true silicon compilation depends on two additional (currently proprietary) technologies—static timing analysis and power syndrome analysis—and the abandonment of classical gate- or switch-level simulation and timing verification, commonly found on CAE work stations ("Estimated timing" in the table).

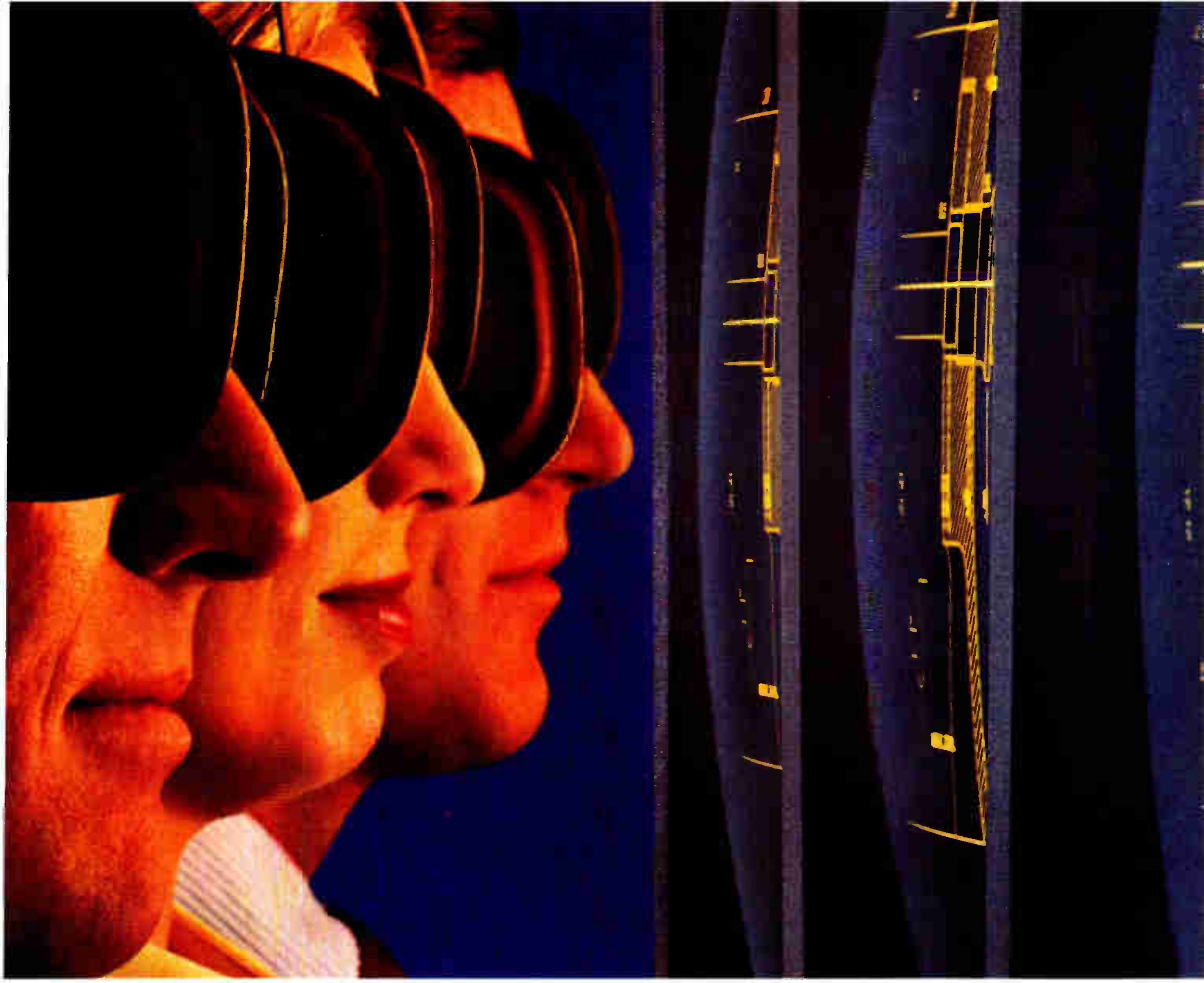
Silicon compilation in a year went from a few courageous beta test sites to a large number of major programs; and silicon has been flowing out—fully functional—ever since. This says that there are exciting years ahead once everyone understands what silicon compilation really is.□

WHAT DIFFERENT VENDORS OFFER

	Compiler design features	VTI	SCI	SST	SDL	LLL
Silicon compiler	System engineer's module library	•	•	•		•
	User-extendible library	•	•	•	•	•
	Module layout synthesis	•	•	•	•	•
	Chip layout synthesis	•	•	•	•	•
	Accurate timing feedback		•			
	Accurate power feedback		•			
	Accurate size feedback	•	•	•	•	•
	Chip functional verification	•	•	•	•	•
	System-level verification	•	•	•	•	
	Functional-level design entry	•	•	•	•	•
	Logical (semantic) rule checks		•			
	Foundry (process) independent		•	•	•	•
	User calibratible for process		•		•	
	Automatic test generation					
	Integrated data base manager	•	•	•	•	
	Currency checking		•			
Hybrid	Estimated timing	•		•		
	Estimated power	•		•		
	Foundry (process) dependent	•				
Extras	Schematic synthesis		•		•	
	Schematic input (for netlists)	•	•	•	•	•

VTI = VLSI Technology Inc.
SCI = Silicon Compilers Inc.
SST = Seattle Silicon Technology Inc.
SDL = Silicon Design Laboratories Inc.
LLL = Lattice Logic Ltd.





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VLSI DENSITY COMES TO POWER MOS FETs

Advanced photolithography, plasma etching, and rapid thermal annealing combine to produce chips with nearly 3 million cells per square inch

Engineers at Fairchild Semiconductor Corp. borrowed a trio of processing techniques from very large-scale integration to breed a new generation of power MOS FETs that pack 2.8 million cells into 1 square inch. That's about three times the density of current-generation parts and twice that of devices still in development by competitive companies, says Karl A. Sassaman, manager of power device design at Fairchild's Discrete Division in San Rafael, Calif.

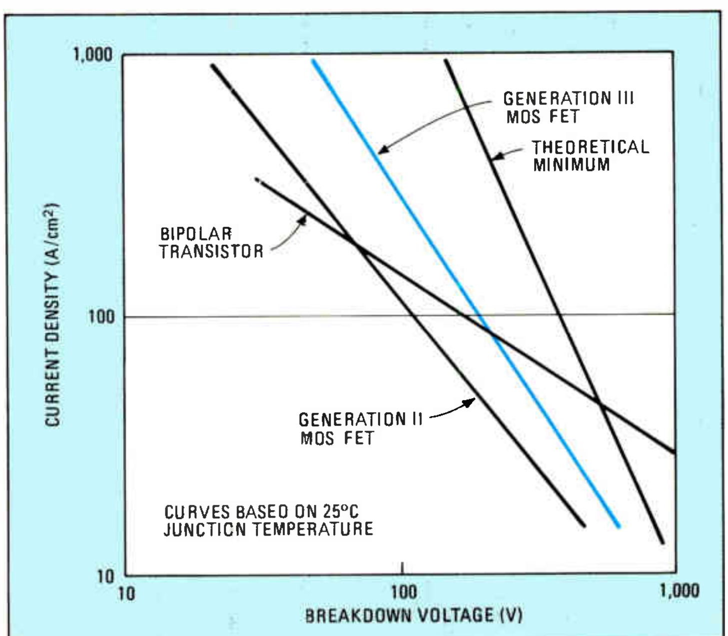
Fairchild's Generation III uses projection photolithography, plasma etching of contact windows, and rapid thermal annealing to produce very shallow junctions. GEN III pushes power MOS FET on-resistances about as close to the theoretical minimum—the intrinsic conductivity of the silicon epitaxial layer—as is possible with current technology, says Sassaman. "Compared with current power-MOS FET technology, we can fabricate devices with lower on-resistances, higher speeds, with smaller dice, and at lower cost.

"At the 100-V level, we have raised current density by a factor of three and raised the crossover point at which a power MOS FET can compete with bipolar on a current-density basis from 60 to 200 V" (Fig. 1). Economically, the technology will raise the limit at which MOS FETs can compete with bipolar parts to 600 V, he says.

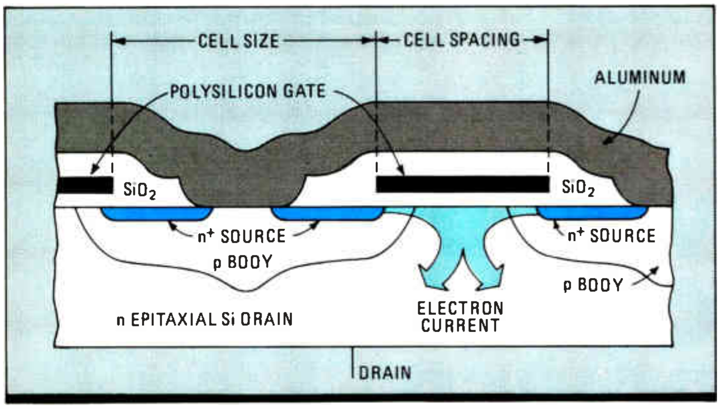
The use of MOS FETs for power conversion has grown tremendously, replacing bipolar transistors in many applications. Power MOS FETs are faster, more rugged, and have simpler gate-drive requirements, but their relatively high on-state resistance (R_{on}) and higher cost have hampered faster penetration into bipolar turf.

It has long been apparent that to overcome these limitations vis-à-vis bipolar power devices requires reducing the resistance per unit area, the parasitic capacitance, and the amount of gate charge, says Neil Wylie, senior process development engineer. "To attain these goals requires a shift from the archaic methods now used to fabricate such devices and a move to more advanced techniques similar to those used in the production of VLSI memory and logic circuits," he says.

Specifically, says senior design engineer Steve Sapp, if power MOS FETs are to continue to gain market share from bipolar devices, their on-resistance must be decreased to reduce power consumption and to minimize voltage drops for low-voltage applications. In addition, it will be necessary to reduce the amount of gate charge for



1. MOS vs. BIPOLAR. VLSI-type processing lets Fairchild's GEN III power MOS FETs rival bipolar current densities up to 200 V.



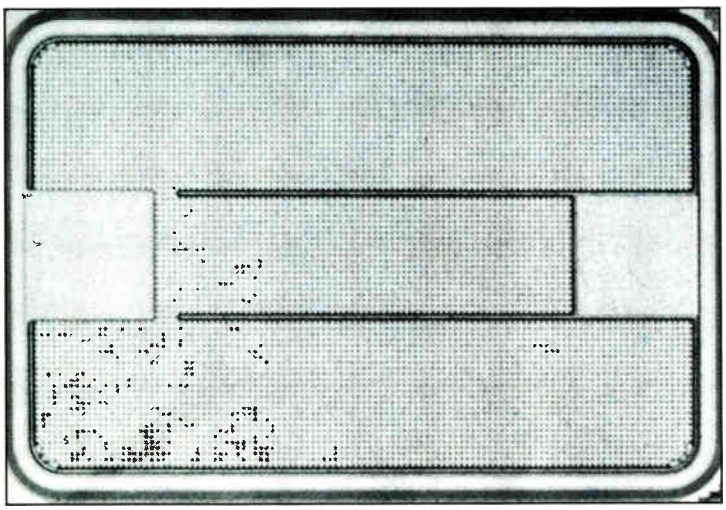
2. DMOS. Key to the current- and voltage-handling abilities of power MOS FETs is a double-diffused self-aligned structure.

switching. "Lower charge reduces current demands on the gate drivers, resulting in faster switching for plug-in replacements in present applications," Sapp says.

The basic power MOS FET is a vertical structure (Fig. 2), formed using a double-diffused MOS process. The p body and the n+ source diffusions are both self-aligned to the edge of the polysilicon gate electrode. Current starts to flow when a channel forms in the p body in response to a positive gate voltage, first horizontally through the channel and then vertically through the n- epitaxial drain region.

Unlike bipolar power devices, achieving higher power handling capability in MOS FETs is not a matter of building bigger structures. Rather, as in memory circuits, the solution is to pack ever-increasing numbers of MOS FET cells into smaller die areas. They are linked in parallel, creating a grid-like pattern (Fig. 3). The cumulative effect of the linked cells is the summation of the combined capabilities of each. So achieving better performance is basically a matter of increasing the number of individual MOS FET cells per square inch, says Wylie.

Cell size and cell spacing are the two critical parameters in achieving greater density per square inch, and thus greater on-resistance. The first is defined by the edges of the window in the poly gate, the latter is the distance between adjacent poly windows. The smaller the cell, the lower the on-resistance, because the available channel area increases on a per-cell basis in proportion to the total cell size.


3. MOS FET GRID. To match the performance of bipolar transistors, millions of MOS FET cells are linked in parallel to form a grid.

Unfortunately, says Sapp, the rules for shrinking the dimensions of power MOS FETs are not quite as straightforward and linear as those for digital and memory chips, particularly with respect to cell spacing. Although the on-resistance does lessen as cell spacing is decreased, the effect bottoms out at about 9 to 10 μm and starts to increase again (Fig. 4). Cells placed too closely together have higher resistance because the current flow is restricted as it flows vertically. As a result, present efforts to hike cell densities in power MOS FETS focus on decreasing the basic transistor geometries, much more so than in a digital or memory circuit.

PROJECTION PRINTING

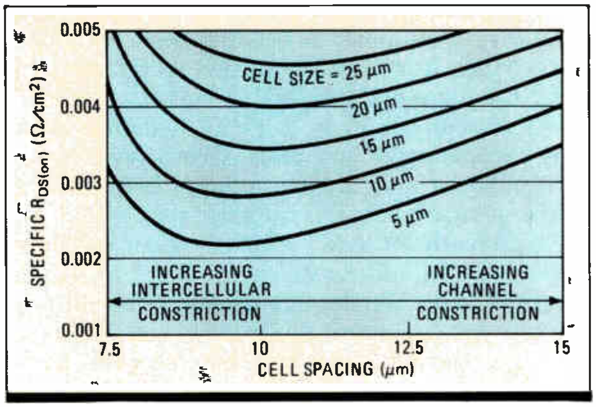
The first step in increasing cell density, says Wylie, was relatively straightforward—a shift from the commonly used proximity photolithographic techniques to projection printing. This technique alone, he says, resulted in pushing minimum feature size from 4 to 2 μm.

To achieve further improvements, he says, Fairchild abandoned standard wet etching in favor of plasma etching. In wet etching, wafers with a resist pattern are immersed in a temperature-controlled chemical etchant for a fixed period of time. The amount of exposed material removed is a function of time, with the etch rate determined by the strength of the etchant, the temperature, and the material being etched.

"The major problem with wet etching is that it is isotropic," says Wylie. "That is, as the chemical etches down through the material, it also etches laterally by about the same amount."

Moreover, DMOS-based power MOS FETs need a thick layer to increase power and voltage handling capability, and that produces a large undercut. "To overcome this in power MOS FETs, as in integrated circuits, it is usually necessary to design your devices with the undercut in mind," says Wylie. "You do this in one of two ways. One alternative is to design the DMOS structure with thinner layers. The other is to design with more conservative rules, larger geometries. The end result is the same—a lower voltage-handling ability and a higher on-resistance, due in the first case to the thinner layers and in the second to fewer cells per square inch."

To resolve this problem, the Fairchild engineers turned to plasma etching. Plasma provides vertical etching through the thicker layers of the DMOS structure with nearly zero lateral undercutting from the photoresist opening. The etching is achieved through the use of ionized gases



4. BALANCING ACT. To cut on-resistance and boost density of power MOS FETs, size and spacing of cells must be considered.

rendered chemically active by a radio-frequency-generated plasma. This allows very precise control of both the vertical dimension and the amount of undercutting, because when the energy source is shut off, etching ceases almost immediately. Though some lateral etching does take place, the amount is small relative to the amount of vertical etching.

In the GEN III parts, the shift to plasma etching resulted in a reduction of the contact window's minimum size to almost 1/50th and photoresist undercut to 1/5, from 0.25 to 0.05 µm. The result: it is possible to build power MOS FETs with both higher cell densities and higher voltage- and current-handling capabilities.

The third and final improvement, says Wylie, was a shift to rapid thermal annealing of the various impurity implants, particularly phosphorus. As in VLSI chips, precise control of both dose and depth of implanted dopants is critical to the performance of power MOS FETs with densities in excess of 1 million cells per square inch.

However, the resultant impurity profiles depend upon both the initial implant and the subsequent thermal processing necessary to heal, or anneal, the silicon damaged by implantation. When a high-energy ion-implantation beam enters the perfect crystal below the wafer surface, it knocks atoms out of the lattice, damaging the first few thousand angstroms of silicon—rendering it amorphous. This radically changes the electrical properties of these areas, in essence rendering them useless.

ANNEALING TO HEAL

It is possible to heal some or all of this damage by annealing the semiconductor with an appropriate combination of time and temperature, says Wylie. Theoretically, complete recovery of lifetime, mobility, and carrier activation should occur. In practice, however, thermal annealing techniques fall short of the ideal.

Using furnace annealing, the highest practical temperature is about 1,000°C, requiring about 20 to 30 minutes to bring the silicon back to a reasonable level of repair. The problem, says Wylie, is that the longer the wafer is treated, the greater the degree of diffusion, both vertically and laterally.

"The ideal with rapid thermal annealing is to use a focused source of heat, such as a laser, and subject the material to temperatures approaching 5,000° or 6,000° for extremely short periods—no more than a few milliseconds or nanoseconds," says Wylie. "Because of the short duration, profiles of implanted materials can be annealed without appreciable diffusion."

TWO-THIRDS CELL REDUCTION

In the Fairchild power MOS FETs, the use of rapid thermal annealing reduced phosphorus junction depths from 0.8 to 0.4 µm, which has the effect of reducing lateral diffusion of the p body, allowing an overall reduction in the cell size of about two thirds. But the most important benefit was that the transistor was reduced by almost two thirds in the lateral direction.

The result of these improvements is a reduction in the pitch—cell size plus cell spacing—from 28 to 15 µm, and an increase in packing density from about 900,000 or 1.0 million to 2.8 million cells per square inch. Less directly visible are the reductions in critical electrical parameters. For example, on-resistance per unit area decreased by about 50% on average. And because the chip area is reduced for a particular value of on-resistance, both the parasitic capacitance and the gate charge shrink by the same amount, making switching speeds faster.

The effects of these improvements are best illustrated by looking at their impact on power MOS FETs with 50- and 500-V breakdown voltages, says Sapp. "For example, at 50 V, if the on-resistance is held constant at 0.025 Ω, the die area of a device employing these techniques can be reduced by 59%, from 38,000 to 16,000 mils^2."

GEN III cuts on-resistance per unit area by 50%, and because it halves parasitic capacitance and gate charge, switching speeds are faster for power MOS FETs

And because capacitances tend to track area, the critical measures in this area—the common-source short-circuit input, reverse-transfer, and output capacitances—are decreased by a like amount: from 2,350 to 1,030, 250 to 110, and 920 to 390 pF, respectively. The gate charge to turn on the device also decreased by a factor of two, from 40 to 20 nanocoulombs. Most significantly, the 135-A controllable current per square centimeter almost doubled to 253 A.

On the other hand, if the chip is kept at about the same size as 50-V power MOS FETs with densities of 900,000 to 1 million cells per square inch, on-resistance can be reduced by 56%, from 0.025

to 0.011 Ω, and the controllable current increased by a like amount. But because the gate charge increases only marginally, from about 40 to 45 nC, switching speed is unaffected.

At higher breakdown voltages the relative reduction in on-resistance decreases, says Wylie. This is because channel resistance is a smaller contributor on high-voltage parts than on low-voltage ones. Nonetheless, the impact of these new fabrication techniques is still significant at high voltages.

At 500-V breakdowns, die size shrinks by 45%, from 21,700 to 12,000 mils^2. On-resistance remains about 1.2 Ω. And although reverse-transfer capacitance more than doubles, the other two contributors to internal capacitance remain about the same. Moreover, the controllable current increases by 56%, from 26.1 to 40.7 A/cm^2.

For equivalent 21,700-mils^2 dies, a 500-V power MOS FET fabricated with the GEN III process will have a 43% lower on-resistance, from 1.2 to 0.68 Ω. Rated current-handling capability will increase 33%, from 26.1 to 34.7 A/cm^2.

Fairchild is now building prototypes of a wide variety of devices with up to 600-V breakdowns. Making plans to be in production by the fourth quarter, Fairchild marketers are developing two product strategies to take advantage of the GEN III breakthrough, says Sassaman.

The first would be to offer devices with the same on-resistance but with substantially smaller die and package sizes for the same function. "This approach would lower device costs substantially," Sassaman says. "But just as important is that it will allow faster switching with about the same gate drives as current devices."

The second option is to retain existing packages and die sizes and offer devices with lower on-resistances and higher voltage- and current-handling capabilities. Assuming that equal advances have been made with transformer cores, copper wiring, and Schottky rectifiers to handle the additional current, this approach would provide a great deal more flexibility. "First of all, if we lower the on-resistance but keep the same thermal resistance of previous offerings, the controllable current level is increased," says Sassaman. "On the other hand, by keeping the current levels the same, power dissipation is reduced, thereby improving device efficiency."

The GEN III technology will break power MOS FETs out of the packaging constraints imposed by bipolar transistors, he believes. "Despite its shortcomings, the workhorse of power-transistor packaging has been the TO-3 metal can. One reason it has survived is its low cost of manufacture."

With the smaller die sizes possible in GEN III, says Sassaman, lower-cost packages are now feasible. Currently in development at Fairchild is a version of the TO-247. Besides lower cost, the plastic package offers technical advantages over the TO-3, among them a lower thermal resistance because of an all-copper header, rather than a combination of steel and copper. □

'GREENHORNS' TAKE A FRESH APPROACH TO POWER MOS FETs

If the GEN III family is totally unlike any other MOS FET line, it should come as no suprise. The design team approached the density problem with a clean slate, technologically speaking.

When the time came to organize the power MOS FET project, Fairchild Semiconductor Corp. decided to assemble a group of greenhorns, says Karl Sassaman, manager of power device design in San Rafael, Calif. "We looked for engineers whose experience in other areas of process development and circuit design might result in new perspectives."

The old man of the group is senior design engineer Steven Sapp. The principal designer of Fairchild's previous-generation GEN II power MOS FETS, he joined the company in 1980 as a failure-analysis engineer after graduation from Whitworth College in Spokane, Wash., with a BS in physics.

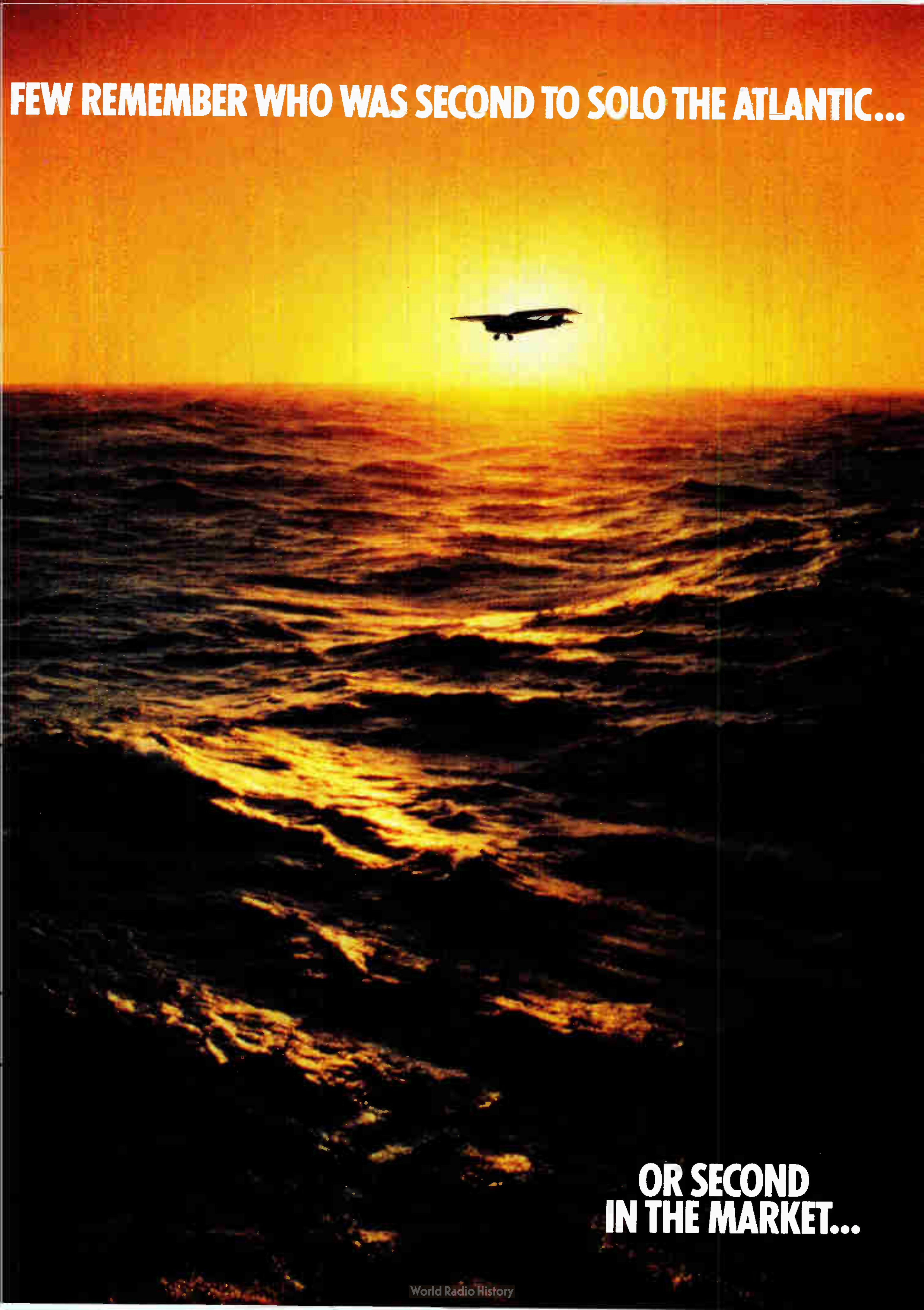
Carmel McShera is the senior process engineer responsible for the ion-implantation and diffusion areas of wafer fabrication. She graduated from the National University of Ireland in 1982 with BS and MS degrees in physics. Before joining Fairchild, and the design team, in 1984, McShera worked for two years at Analog Devices BV in Ireland.

Senior process-development engineer Neil Wylie is a 1980 graduate of the University of Sheffield, England, with a bachelor of engineering degree in electronics. Before joining the GEN III team in 1983, he worked for three years at National Semiconductor (U.K.) Ltd. Involved from the very beginning with the startup of the company's power-chip fab line, he defined the design rules and processes for GEN III.

EXPERIENCE NOT NECESSARY. Watching Rich Zelenka, seated, are (left to right) Sapp, McShera, Wylie.

Senior process engineer Richard Zelenka joined Fairchild in 1983 and is responsible for photolithography and metalization on GEN III. A graduate of the University of Wyoming with a BS in chemical engineering, he is currently completing his doctoral studies at the University of California at Berkeley.

Fairchild was able to come up with a power MOS FET design of such high cell density because "we had the advantage of no preconceived notions, no bad habits to overcome," says Sassaman. Rather than try to extend old technologies to higher densities, he says, "we looked at it as basically a matter of developing a very large-scale-integration-level circuit that had the additional requirements of high-voltage and -current handling."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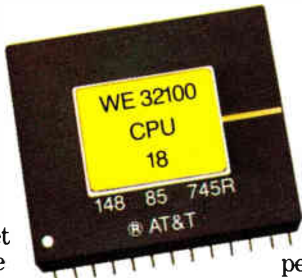

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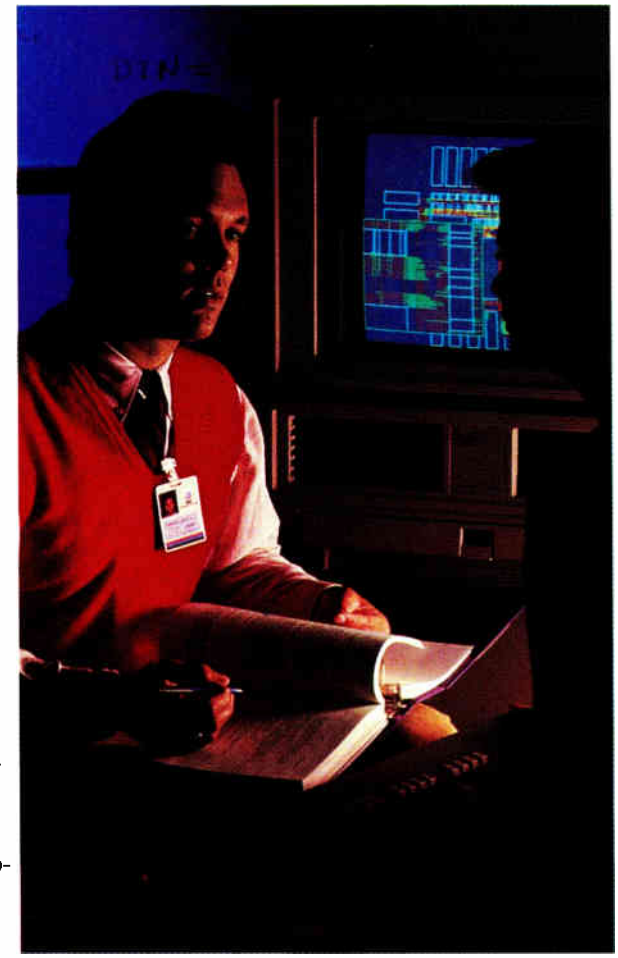

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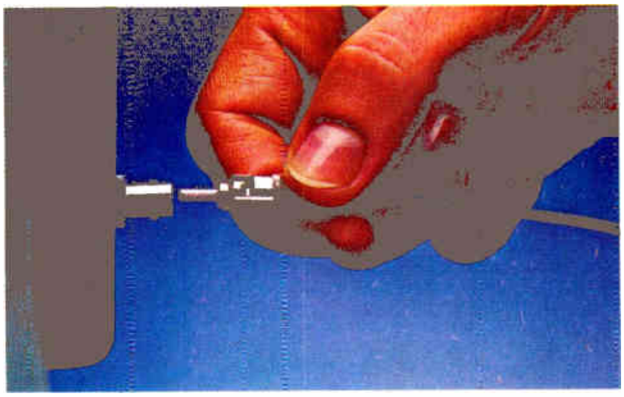

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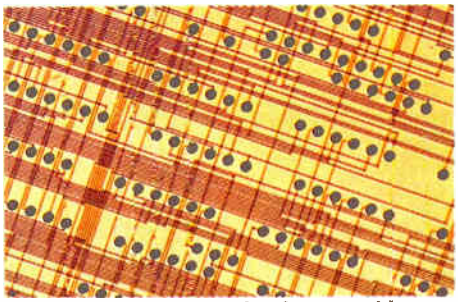

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AT LAST, IT'S EASY TO DESIGN RS-232-C MODEMS

A single CMOS chip generates all the voltage levels necessary for an RS-232-C interface; the key is a dual-charge pump for both positive and negative voltages

The easy-to-design RS-232-C modem is finally here, thanks to a new chip that generates all the interface voltage levels. Making this chip possible is a dual-charge-pump design that generates both positive- and negative-going voltages.

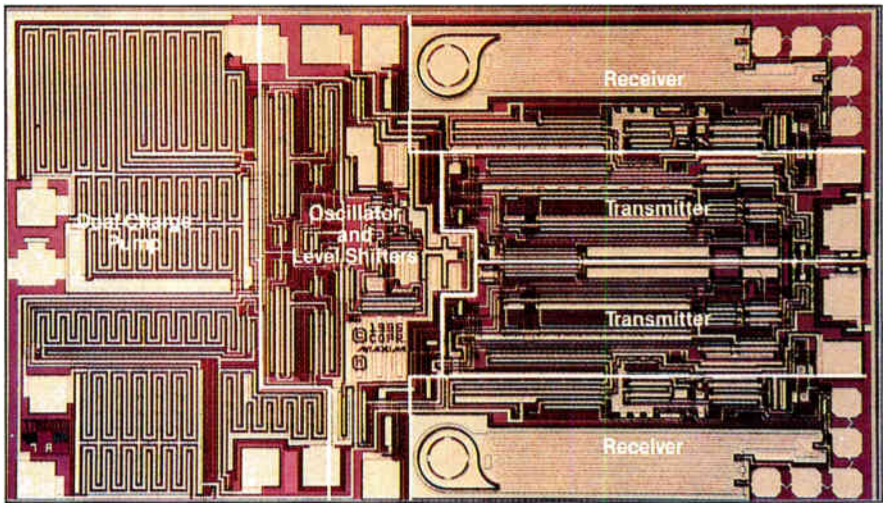
"When you look at a modem board, you see an extraordinarily high level of integration—except for the RS-232-C interface which requires anywhere from 15 to 20 components," says David Fullagar, vice president of research and development for Maxim Integrated Products Inc. "But the more important factor to many systems designers is the additional cost of generating the positive and negative supply voltages, which can increase the cost of the system by $20 to $30."

The Sunnyvale, Calif., company's single-chip solution to the problem of generating multiple voltages at the RS-232-C interface, the MAX232 (Fig. 1), reduces both the chip count and cost by 95%, says Brian Gillings, Maxim's director of strategic planning and application engineering. The company also is extending the use of monolithic dc-to-dc converters to generate necessary voltage levels locally and is introducing a number of cousins of the MAX232 to serve as on-board voltage converters.

The RS-232-C standard (table, p. 90) calls for 2-V logic noise margins. This means the transmitters must deliver at least ±5-V swings, while the receivers must respond to signals that swing no more than ±3 V. The slew rate is specified to a maximum of 30 V/ms to reduce ringing and reflection; the receiver input impedance is between 3 kΩ and 7 kΩ to provide a known terminating impedance.

The MAX232 voltage converter interface meets all these specs. Fabricated in the company's 3-μm metal-gate CMOS process, it is organized into three sections: two charge-pump converters, dual RS-232-C transmitters, and dual RS-232-C receivers. One of the converters changes +5 V to +10 V, and the other changes +10 V to −10 V.

Until Maxim developed the 16-pin MAX232, the system designer of a



1. DUAL INTERFACE. All RS-232-C interface requirements are provided on Maxim's MAX232 with a dual-charge pump that generates both positive- and negative-going voltages.

RS-232-C STANDARDS CALL FOR MIXED VOLTAGES	
Output swing, 3-kΩ load	+/− 5 V min
Output swing, open circuit	+/− 15 V max
Slew rate	30 V/µs max
Input threshold	+/− 3 V max
Input voltage	+/− 25 V max
Input resistance	3 to 7 kΩ

+5-V powered system had limited options for powering an RS-232-C output, says senior scientist David Bingham. "He could 'cheat' and send 0- to 5-V signals and hope that it worked. Or he could use an expensive and bulky hybrid dc-to-dc converter module, run power buses around the board, and power a simple receiver/transmitter IC from ±12 V. He could even use one or more single-chip, stand-alone charge-pump inverters, but this would require that he build his own level translators." The MAX232 supplants these techniques and requires only four external components: low-cost 22-mF capacitors (Fig. 2).

The transmitters of the MAX232 are CMOS inverters powered from the ±10-V internally generated supplies. The transmitter inputs are TTL- and CMOS-compatible, with logic functions set at 1.3 V for 5-V supply levels. In addition, says Bingham, the inputs have internal pull-up resistors that force the output of an unused RS-232-C transmitter low when the input is not connected.

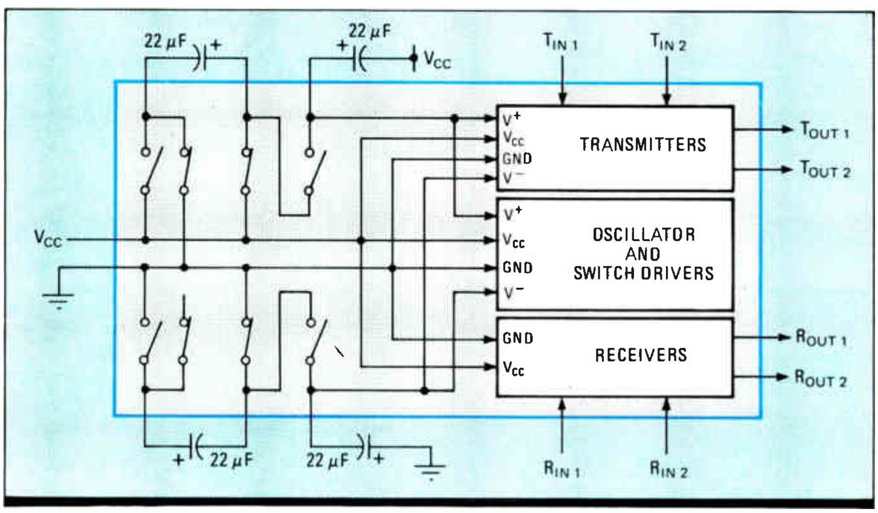
The unloaded RS-232-C output swing of the MAX232 is from –10 V to 0.6 V below the +10-V level. The slew rate of the outputs is limited to less than 30 V/ms, eliminating external slew-rate-limiting capacitors. The on-chip receivers also conform to the RS-232-C specs, with inputs that can withstand ±30 V even when the device has no power applied. The input receivers have 500 mV of hysteresis to improve noise rejection.

At the heart of the MAX232 is a dual-charge-pump circuit developed by Bingham that generates output voltages both more positive and more negative than the +5-V supply. Similar to ac doublers and triplers, charge pumps are most common in strictly digital designs such as memory circuits. Charge-pump circuits generate the appropriate voltage by charging a capacitor to an input voltage and then adding, subtracting, or inverting the voltage on the capacitor's positive or negative input-voltage terminal, transferring this charge to a holding capacitor.

"The problem to be solved with the MAX232's charge-pumping scheme was that the RS-232-C interface made it necessary to generate a –5-V signal from a +5-V signal, as well as to generate a +10- to +12-V signal and then invert it to generate a –10- to –12-V signal as well," says Bingham. "Current technology makes it possible to build voltage doublers and voltage inverters, but most of these devices have been limited to generating such signals in a negative-going direction." The MAX232 combines both functions in a single device, as well as simultaneously generating positive- and negative-going signals.

TWO CLOCK PHASES

The circuit scheme implemented on the MAX232 to generate the necessary voltage doubling and inversion in both the negative- and positive-going directions is done on two phases of an internally generated clock, says Bingham. During phase 1 (Fig. 3a), capacitor C_1 is charged to the V_{cc} supply voltage through switches S_2 and S_3. During phase 2 (Fig. 3b), the voltage on C_1 is then added to V_{cc} through switches S_1 and S_4 , producing a signal across capacitor C_2 equal to twice V_{cc}. At the same time, capacitor C_3 is charged to a similar level through switches S_5 and S_7 and then inverted with respect to ground through S_6 and S_8 to produce a negative voltage twice V_{cc} during phase 1. The switches are turned on and off at a 16-kHz rate by the internal clock and arranged to break before make so that no charge is lost from capacitors C_2 and C_4 during each phase.



2. FEWER ICs. A single-chip MAX232 voltage-converter interface and four capacitors can replace 15 to 20 parts to provide RS-232-C voltage levels.

Though the MAX232's circuit scheme is simple to conceptualize, there is considerable difficulty in implementing it in CMOS, especially when combined with a number of other components on the same chip, says Bingham. "Conventional wisdom says that you should not be able to build such a dual-charge pump structure with CMOS devices without going into latchup," he says. "This is because it is necessary to forward-bias the CMOS transistor structures. However, this goes against all conventional wisdom. When you forward bias, it is very easy to go into latchup, if care is not taken in designing the circuit, because of the inherent silicon-controlled-rectifier diode structure present in all CMOS devices."

To allow forward biasing of the MAX232 without going into latchup, Maxim surrounds each diode with serial collectors that tie back to the cathode of the diode. These collectors trap most of the minority carriers injected into the substrate when the diode is forward-biased. "It is important to collect as many of these carriers as possible, because if they diffuse far enough, they will be collected by the base of the equivalent npn transistor in the SCR structure, causing latchup," he says. The key is to position the collectors close enough to the emitter of this npn transistor so that at least 99% of the injected minority carriers are collected and put back into the cathode of the diode.

The MAX232 also represents a different approach to distributing voltages around a board and through a system by using numerous small monolithic CMOS dc-dc converters. "The standard approach has been to use a relatively large switching power supply and a number of relatively bulky discrete bipolar transistor-based hybrid dc-dc converter modules and channel the necessary voltages throughout the system and boards via special signal buses," Fullagar says.

Distributed power conversion using monolithic devices is somewhat akin to the distributed processing that unburdens a computer from servicing peripheral systems, he says. It accommodates a variety of local supply requirements without demanding that the main power source deliver the required voltages or regulation.

So Maxim has extended the distributed approach to voltage generation using monolithic dc-dc converters from the 0.5-mW range—the MAX232—up to the 5-mW range with the MAX 630 series of monolithic CMOS dc-dc converters. Now in the works, says Fullagar, is the MAX640 series of CMOS dc-dc converters, which extends the distributed approach up to 10 W.

"As large as the market is, the MAX232 is a specific solution to a narrowly defined subset of local generation of dc signals," he says. "The monolithic CMOS MAX630 and 640 series are more generalized solutions to the same problem and as a result can be applied across a much broader range of systems."

Fabricated using the same 3-μm metal-gate CMOS process used in the MAX232, the 630 and 640 series combine a 1.31-V bandgap reference, an oscillator, a voltage comparator, and a 1.3-V trip-point comparator into a single eight-pin package. The 630 and 640 series of devices require at most no more than three additional external components—an inductor and capacitor for the positive converters and an additional current diode for the negative converters. They operate in a somewhat different manner from the MAX232, since their task is to generate a regulated output voltage rather than the multiple voltages, both positive and negative, required to satisfy the RS-232-C interface requirements.

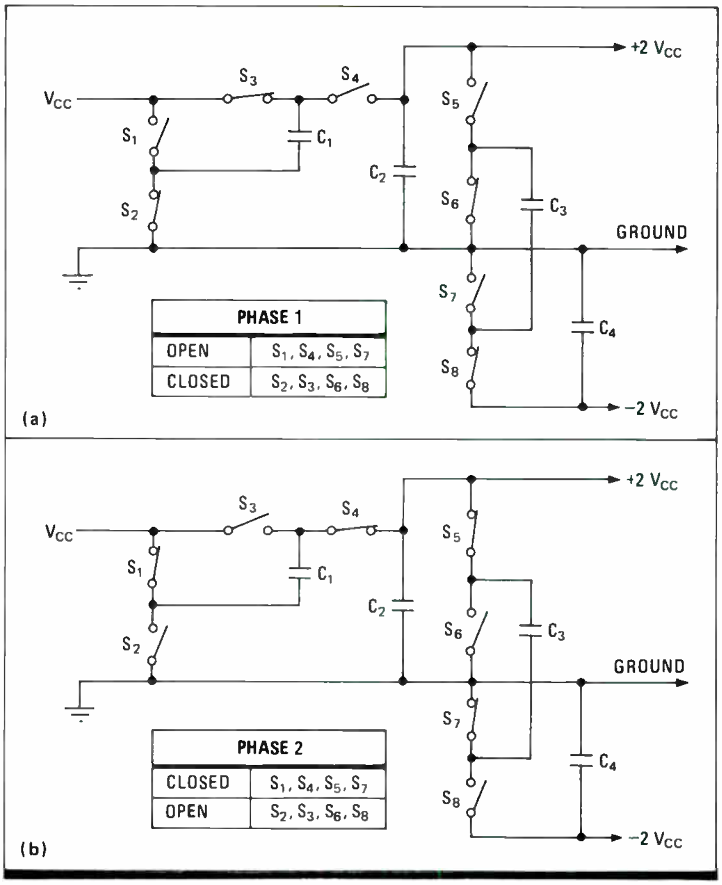
To do this, these devices use a set of internal resistors to divide the output and compare it to the 1.31-V internal reference with the comparator. Whenever the output is below the programmed voltage, the comparator output will switch on and off at the frequency of the internal oscillator. When the output is on, the current

Single-chip dc-to-dc converters also can be used for distributed voltage generation, supplying regulated outputs wherever necessary in a system

through the external inductor rises linearly, storing energy in the magnetic field of the inductor. When the output switches off, this magnetic field collapses, creating an inductive kickback at a higher voltage, which is delivered to the output capacitor through the internal catch diode.

When the output voltage reaches the desired level, the comparator inhibits the output until the load has discharged the output capacitor below the desired voltage level. This cycle repeats, keeping the output capacitor charged to the desired output voltage.

The MAX630 and 640 series use pulse-frequen-



3. TWO PHASES. The dual-charge pump generates positive and negative voltage doubling and inversion in two phases (a) and (b).

cy modulation rather than the more commonly used pulse-width modulation. Both pwm and pfm circuits control the output voltage by varying the duty cycle, says Fullagar. In the pwm approach, the frequency is held constant and the width of each pulse is varied. In the pfm circuit, the pulse width is held constant and the duty cycle is controlled by changing the pulse repetition rate. The advantage of the pfm approach, says Fullagar, is that it operates at a much higher efficiency—about 50% to 60%.

Maxim has refined the pfm technique with an on-chip constant-frequency oscillator. The output MOS FETs are switched on when the oscillator is high and when the actual voltage is lower than desired. If the output voltage is higher than desired, the MOS FET is disabled by that oscillator cycle. This "pulse skipping," as Fullagar calls it, varies the average duty cycle and thereby controls the output voltage.

Unlike pwm devices, which use an op amp as the control element, the Maxim dc-dc converters use a comparator to compare the output voltage to an on-board reference voltage. "This reduces die size, the number of external components, and the operating current," says Fullagar.

Key features of these ICs are a large n-channel MOS FET on the output for positive converters and a p-channel MOS FET for negative converters. Using MOS FETs rather than bipolar transistors gives a higher switching speed, which reduces switching losses and allows the use of smaller, lighter, and less costly magnetic components, says Fullagar. Even more important for high efficiency, low-power dc-dc converters, MOS FETs do not require a base current—unlike bipolar transistors, which use a portion of the input power as a base-current drive. Where the input power of an equivalent bipolar output circuit with a 2-mA current drive would, for example, increase by a factor of 10 between no load and full load, in the MAX630/640 series it increases by only 1 μA/kHz.

The introduction of monolithic dc-dc conversion devices such as the MAX232 and the MAX630/640 series presages the eventual removal of ac voltages from inside most electronic systems altogether, says Fullagar. "A computer, for example, could be supplied with a moderately regulated 24 V dc from an outside supply. Then monolithic dc-dc converters on the internal boards could develop all the proper operating voltages and provide the extra measure of regulation required by voltage-sensitive circuits." □

BEHIND THE MAX232 IC: A MAN WHO WON'T TAKE NO FOR AN ANSWER

For David Bingham, senior scientist at Maxim Integrated Products, the MAX-232 is only the latest in a long series of ground-breaking chips he has designed. He participated in the design of the first monolithic dual-slope analog-to-digital converter, the ICL7106, and was the chief designer of the CAZ AMP, the first ultra-low-offset voltage amplifiers using commutating auto-zeroing techniques. He also designed the popular ICL7660 voltage inverter, as well as Maxim's MAX610, an ac-to-dc regulator.

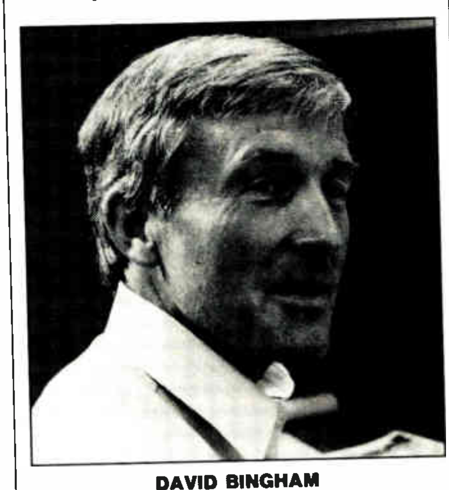
The 47-year old Bingham started as a designer of bipolar analog circuits at SGS Semiconductor, Milan, Italy, after graduating from the University of London with a degree in electrical engineering. He moved to the U.S. to work at Fairchild Camera & Instrument Corp. and then Cermetek Inc. before joining Intersil Inc. in 1970.

Intersil was fabricating solid-state circuits for watches, and some of Bingham's first designs there combined bipolar and thin-film technologies. As CMOS technology matured, he moved his watch circuits to that process. Then he began devoting his attention to analog CMOS technology.

Bingham explains his creativity by saying he doesn't like to take no for an answer: "I become very stubborn when someone tells me there is something that can't be done. I immediately begin looking for ways it can be done."

The design of the MAX232 was a case in point. "When it was first considered, the idea of generating all those voltages on the same chip did not seem possible," he says. "After thinking about it for a while, it seemed to me that if it was at all possible, it would have to involve some sort of dual-charge-pump scheme, to generate both positive- as well as negative-going voltages."

However, designers have avoided that sort of structure in CMOS designs, Bingham says, "because it involves doing exactly what the textbooks tell you to avoid at all costs to prevent latchup: forward-biasing the circuits."



DAVID BINGHAM

There is a good side as well as a bad side to forward-biasing, he says. "There is always an opportunity to use bad effects of CMOS to advantage. The key is careful planning and attention to detail."

By careful placement of components and collection of minority carriers, he says, it is possible to achieve virtually every conceivable structure—including npn and pnp transistors, diode structures and bridge rectifiers—and function, both analog and digital, as well as a variety of power and voltage supply functions. "I like CMOS because you never feel as if you are pushing its limits," says Bingham. "Even when it appears as if you are, there is always the potential that by diddling a little here and diddling a little there, what was previously impossible is now possible."

Bingham also has a fondness—indeed, an enthusiasm—for the more mature 2-, 3-, and 4-μm CMOS processes. "The advantage of a relatively mature process, aside from low cost, is that it is well-understood; its capabilities and limitations are clearly defined," he says. And with understanding comes the ability to adapt the process to perform almost anything a designer might want to do.

WHICH BAND IS RIGHT FOR BYPASS SATELLITES?

The C and K_u band each have advantages for network designers and managers, and it takes a careful analysis to determine which one to choose

Bypass satellite networks have emerged as a promising alternative to terrestrial leased-line networks. Based on 1.2-meter satellite dishes known as very small aperture terminals or VSATs, these networks offer the potential of increased system reliability and performance while substantially lowering the cost of data transmission. According to one study, VSAT networks can reduce the corporate data communications bill by as much as 25% to 50% over leased lines. That's a real plus for telecommunications managers, considering the steady rise in private-line tariffs.

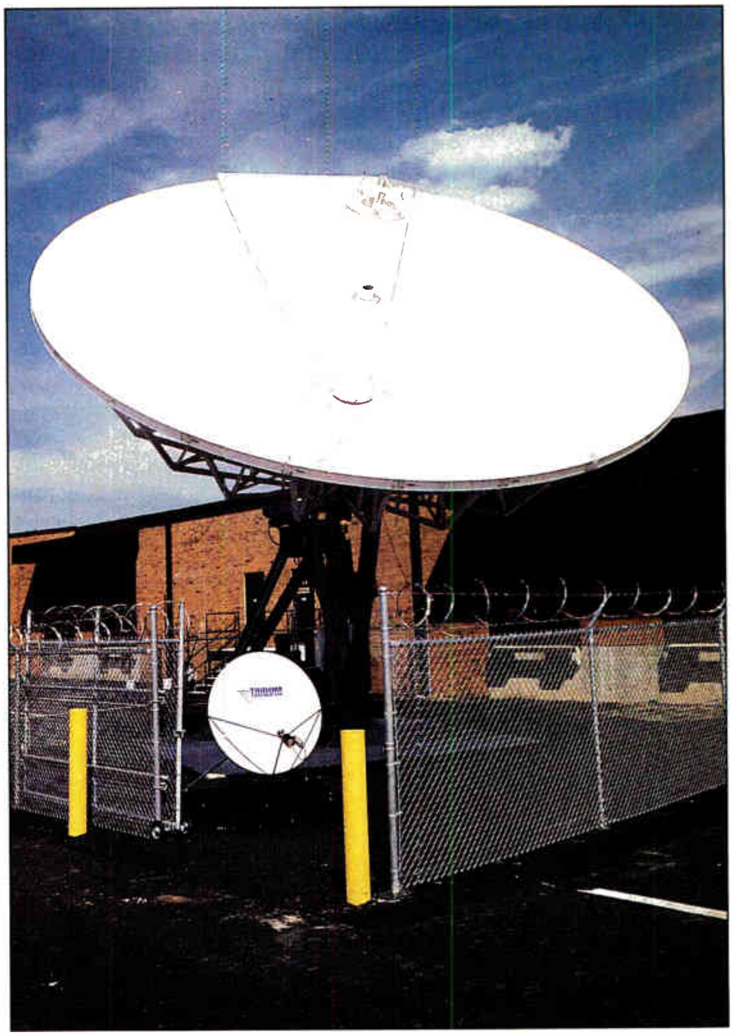
The coupling of the compact radio-frequency technology associated with the 1.2-m dishes in a topology that is insensitive to distance frees network managers to add or delete nodes from a network without worrying about local and long-distance tariffs. But choosing the right VSAT for a private satellite network involves careful evaluation of the tradeoffs associated with the two leading transmission frequency bands.

The C and K_u bands are the only practical choices allowed by the Federal Communications Commission for commercial satellite systems. Because a satellite acts as little more than a microwave relay station in space, separate frequency bands are used for its transmitter (downlink) and receiver (uplink) paths to prevent interference. The C- and K_u-band frequencies are in different sections of the microwave spectrum, and the K_u band's position causes a different response to atmospheric conditions.

THE TWO CHOICES

The bands are each 500 MHz in bandwidth. By using the signal-separating properties of vertical and horizontal antenna alignment, each path is usually divided into 24 overlapping channels, or transponders, which are about 36 MHz wide. The C-band satellite can transmit at 3.7 to 4.2 GHz. The earth station can transmit at 5.925 to 6.425 GHz. The frequencies for K_u satellite and earth-station transmitters are 11.7 to 12.2 GHz and 14 to 14.5 GHz, respectively.

"C-band or K_u-band satellite networks each have advantages," says Alan McBride, chief scientist and cofounder of Tridom Corp., the Marietta, Ga., satellite network builder. Tridom believes K_u-band VSATs are the clear choice for most business applications, while conceding that C band is better for rural areas or applications where availability must be maintained regardless



1. RIGHT CHOICE. The 10-meter C band and 1.2-m K_u band each have their appropriate applications.

CHOOSING THE CORRECT VSAT	
C BAND	Ku BAND
Advantages	
• Lower susceptibility to rain-induced fading phenomena • Less-costly hardware in near term	• Higher satellite power provides higher performance and lower cost • Frequency band not used by other communications devices. Site selection and licensing simpler
Disadvantages	
• Terrestrial interference makes site selection and licensing more costly and blocks some locations entirely • Larger antenna needed for similar data rates (spread-spectrum operation narrows this difference)	• Higher susceptibility to rain-induced fading phenomena. (This disadvantage can be eliminated with a nonstop architecture) • Higher-cost hardware in the near term

of weather and cost of implementation (Fig. 1).

"The big attraction of the C band is that it is relatively unaffected by weather conditions," McBride says. "Its major drawback is that its frequency range is also used by the common carriers to implement their terrestrial microwave-based voice transmission facilities. So in heavily urbanized areas there is a distinct likelihood that a new C-band installation could interfere with an existing network." For that reason, considerable time and money are often required to prevent interference and acquire the necessary license for a C-band network, he says.

By contrast, few terrestrial communications systems use K_u-band frequencies. "Since interference with an existing network is remote, the licensing requirements for K_u usually require little time or expense—a real plus in accommodating both initial installations and ongoing office relocations," McBride says.

K_u-band satellite networks operate with higher power budgets than C-band systems, which means that substantially higher data rates can be supported on the small dishes. But K_u is not without its constraints. Its biggest drawback is that its signal level is subject to attenuation by heavy rainfall—a problem in areas with heavy annual rainfall, such as those states bordering the Gulf of Mexico (table). Much of the rainfall effect can be overcome, however.

The choice of C- or K_u-band should follow the application's requirements, says McBride. "The major issues in selecting any data communications system—satellite or otherwise—are performance and operational capabilities that meet both initial and future requirements," he says.

Both satellite systems meet certain basic requirements. They are available at least 99.5% of the time, and a better grade of service can be engineered. Both provide sufficient response time to meet interactive applications demands, and hardware configuration is flexible enough to accommodate future applications growth.

McBride applies another set of parameters to judge the suitability of C versus K_u VSAT technology: whether there are initial location restrictions in implementing a particular technology; determining total long-term system costs, including capital plus recurring costs; and the system's flexibility—whether future relocation and associated costs will be low.

Frequently cited as the biggest obstacle facing K_u VSATs is rain fade, the statistically predictable amount that microwave signals will attenuate whenever there is precipitation along the signal path. "Rain fade is not a total loss of signal, and it rarely interferes with the availability of a properly designed system," McBride says. "When a major rainstorm hits, a short-term [2- to 10-min duration] increase in the signal path's bit-error rate can be corrected by stepping up the transmitted power, using larger receiver antennas, or providing nonstop backup to recover bursts received with errors."

The National Aeronautics and Space Administration has compiled statistics on rain fade by region, so K_u system designers can predict the amount of attenuation expected in any location (Fig. 2). In fact, using backup capability and increased power margins, K_u systems can provide better than 99.9% rain-fade availability.

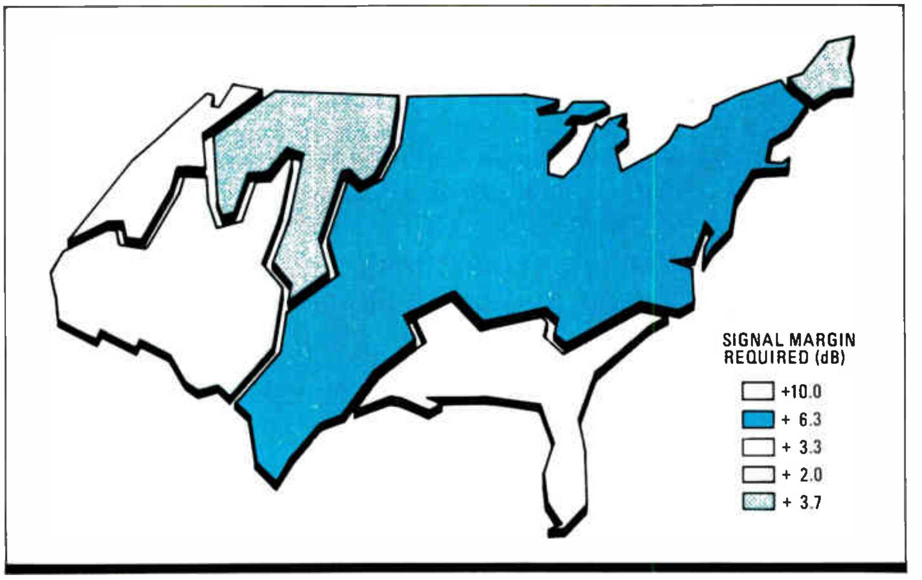
FIGHTING RAIN FADE

Transmitting at high power levels in the K_u band is one way to blast through the rain-fade problem, but there are more economical solutions, McBride says. "If rain fade impacts your location during certain months, then an automatically activated dial-up terrestrial service can be used as a short-term, low-cost backup to the satellite system during the critical period." This has the double advantage of backing up both rain fade and catastrophic equipment failures. McBride says the cost of backup will be considerably less than having the entire network on terrestrial lines or a C-band system.

Another way to overcome rain fade in K_u-band networks is to use a single master station to operate hundreds of remote VSAT units. The master station, equipped with a large antenna and powerful rf amplifier, compensates for rain attenuation by increasing signal amplification. The diameters of master-station antennas range from 6 to 9 m. Their hub amplifiers are 300 to 600 W, compared with 1 or 2 W typical on the smaller dishes. Or the size of the remote VSAT can be increased from 1.2 to 1.8 m, though this would boost installation costs.

"Rain fade has not proved a serious drawback to K_u-band operations," says McBride. "Look at IBM's Satellite Business Systems or the NBC television network. They are examples of established nationwide networks that have years of experience operating in the K_u band. Minimum downtime is critically important to their businesses, and all have been successful in achieving their goal of availability in the rain-fade environment."

C-band systems are nearly immune to rain-fade. However, they suffer from a set of problems brought on by their potential for interference with terrestrial microwave transmissions. Telephone company microwave transmissions use the same range of frequencies, so they are susceptible to interference from C-band data network transmissions on the downlink path. To minimize this problem, the FCC limits the amount of power a C-band satellite transponder can broadcast to 35 dBW. K_u-band users have no such restrictions. Recent satellites have been launched with 45-dBW K_u-band transponders aboard.



2. NO PROBLEM. By increasing signal power margins in a Ku-band satellite system, the problem of rain-fade attenuation can be effectively eliminated.

Tridom recommends that prospective users of C-band technology first investigate the possibility of interference at essential locations. "Particularly in large cities, it may not always be possible to prevent interference by the usual methods, such as shielding the C-band antenna or locating it out of the path of interference," says McBride. "In general, if several nodes are slated for large metroplitan areas, the user can anticipate some number of unavailable sites, greater licensing costs, and longer waiting time gaining FCC approvals."

McBride says considerable time is needed to gain telephone company and FCC action on a C-band application. He also notes that of all installations, only about 80% do not conflict with existing microwave facilities. In an average mix of rural and urban installations, an estimated 15% to 18% require some kind of construction or special frequency coordination to avert possible interference with existing C-band microwave links. In the remaining 2% of cases, there is simply no way to engineer an installation.

Once interference studies have been completed, the next step is to compare total costs of C- or K_u-band systems in terms of one-time capital expenses as well as recurring monthly charges. The factors include equipment costs, licensing services, site construction costs, future relicensing because of moves and additions, site construction as a result of relocation, and satellite charges.

The major factors affecting equipment costs are complexity of channel-modulation techniques, antenna size, and the amplifier required. Over the last few years, prices for K_u-band rf components have dropped considerably and are nearly as low as those for C band, McBride says. For example, the power availability of C and K_u bands shows that for comparable performance, the lower cost of smaller K_u band antennas offsets most of C band's advantage of lower-cost rf components.

OVERCOMING INTERFERENCE

Expensive channel-modulation techniques such as the spread-spectrum method are often used to overcome C-band interference with and from other systems. The digital hardware necessary to implement spread spectrum and its attendant Code Division Multiple Access (CDMA) channel-access method in C-band systems adds complexity and somewhat diminishes the equipment cost advantage of C-band, says McBride.

The relative costs associated with licensing also can be a factor in choosing between C and K_u band. Individual VSAT earth stations must be licensed if they use C band, but the FCC allows a blanket license covering all sites under a single K_u application. Also, C-band frequency-coordination studies must be conducted to prove there will be no interference to existing services.

McBride says that in general, the K_u-band licensing process is faster, less complex, and hence less expensive than the C-band process. With C-band applications, the legal fees, frequency searches, and engineering studies can run into many thousands of dollars—not counting added construction costs for shielding and other kinds of interference protection.

Shielding is often used to alleviate C-band signal interference. Because microwave signals radiate in a straight line of sight, a conductive barrier, usually made of copper mesh in concrete, can be placed in the transmission path to attenuate the interfering signal. The cost ranges from $100 to $10,000 or more, depending on location. It may be altogether impossible if weight loading exceeds the roof's structural capacity or if the landlord or local planning commission objects to the larger installation.

USING EXISTING STRUCTURES

In some cases a penthouse, cooling tower, adjacent building, or other existing structure can be used as a shield. However, shielding should never interfere with positioning along the orbital arc since it often becomes necessary to change to another satellite because of technical, legal, interference, or economic reasons. Using a building as a C-band shield usually requires mounting the antenna on the ground rather than the roof. Ground mounts entail the added cost of cutting pavement, digging a trench, laying conduit, and recovering the pavement.

It may be possible to find another nearby site that is out of the path of interfering microwave signals. However, if the distance exceeds the system's specified maximum length of the intrafacility link cable, then the cost of additional equipment such as line amplifiers, short-haul modems, and the added cable itself must be considered. What's more, there is always the possibility that constructing a new site may cost more than building the original site.

Accommodating physical relocations and additions are ongoing in any major network operation. Business statistics on office-space turnover suggest that the typical company changes 20% of its office locations each year. With a K_u-band network, an office can be relocated on short notice with service installed at the new location over a weekend. This contrasts with the typical 45- to 90-day ordering times for leased lines and C-band licensing and shield construction, Tridom maintains.

If the branch offices in a C-band network are occasionally relocated, the ongoing added costs of barrier construction and FCC relicensing must be added to the system cost. Interference may preclude a critical relocation altogether or require a prohibitive cost for construction work.

"We have found that for a majority of business applications, K_u-band operation offers significant current operational benefits and, importantly, long-term flexibility and growth capabilities that make it a clear choice over C-band," McBride says. "K_u is superior in applications that typically require high data rates, a need to add multiple applications, limited voice or audio teleconferencing capabilities, and substantial metropolitan area locations.

"The ideal C-band applications are those which require an extremely high degree of availability but need only low data rates. Additionally, these networks usually have a large percentage of sites outside of metropolitan areas and many in the Gulf Coast states, where rain fade is troublesome."

VSATs can provide substantial operational and long-term cost advantages over terrestrial networks, but careful consideration of installation and operational factors is the key to success. □

IT TAKES PLENTY OF C-BAND EXPERIENCE TO APPRECIATE K_u

Alan McBride, Tridom Corp.'s founder and chief scientist, is no newcomer to satellite communications. His K_u-band zeal owes to a long association with the more established C-band networks.

In the early 1960s, during a stint with Rockwell International Corp.'s Collins Radio Division in Dallas, McBride helped design the Public Broadcasting Service, the first national broadcast satellite network. "I was an engineering manager for the initial deployment," he says. "We were using 10-m dishes, and each receive-only earth station cost $80,000 to $100,000. Now we could do the same thing with K_u-band technology for about $7,500 apiece."

The 53-year-old University of Oklahoma alumnus recalls that, "because this was the first national satellite network, they designed the heck out of it. They [the design engineers] were scared, but they did a hell of a job because it still works 10 years later."

SATELLITE VET. Alan McBride, flanked by Jim Stratigos and Steve Chaddick, has 20 years of experience in both satellite networks.

In the early 1980s, McBride went to Scientific Atlanta Inc. to work on digital audio communications for the major broadcast networks. He left in 1983 to form Encom Systems Inc. with six Scientific Atlanta colleagues. A builder of head-end installations for cable-TV companies, Encom was quickly gobbled up by Byers Communications Systems, also of Atlanta, about a year later. But Byers ran into trouble, so McBride and five staff members launched Tridom.

Steve Chaddick directs RF and communications engineering at the Marietta, Ga., company. Besides building 1.2- and 1.8-m receive and transmit earth stations, Tridom provides software for end-to-end communications coverage. Handling this end is Jim Stratigos, director of digital and software engineering.

THE BOOM STARTS IN SMART POWER PRODUCTS

The mushrooming smart-power industry is unveiling a host of new devices that replace electromechanical parts in industrial and consumer applications

by Steve Zollo

This could be the year that smart power makes it big. Thanks to the growing number of participants in the field, the smart power industry is mushrooming with new process technologies and new products for both industrial and consumer applications.

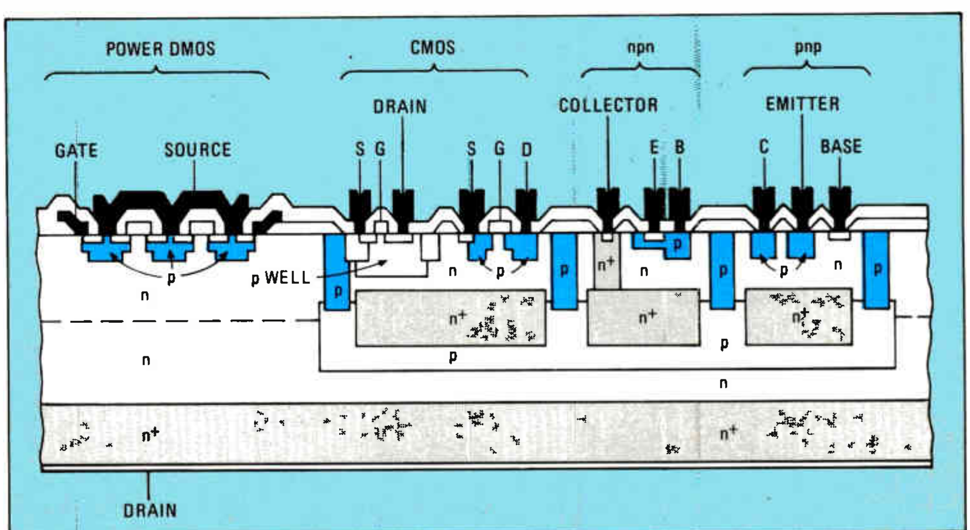
Smart power, in its broadest definition as the interface between logic and load (see "What is smart power?" p. 99), is busy at work in products today. But the electronics world is just beginning to feel the benefits of smart power, which opens up entirely new applications for transistorized control of electric power in areas where, until now, electromechanical relays, solenoids, switches, gears, pulleys, hydraulics, and other cumbersome devices have been used.

For example, a microprocessor could accept inputs from infrared and photo sensors to spot a person's entry to a room and to measure the amount of light in the room. The processor would direct a smart power device to start up or shut down heating and air conditioning systems and to dim or brighten lighting.

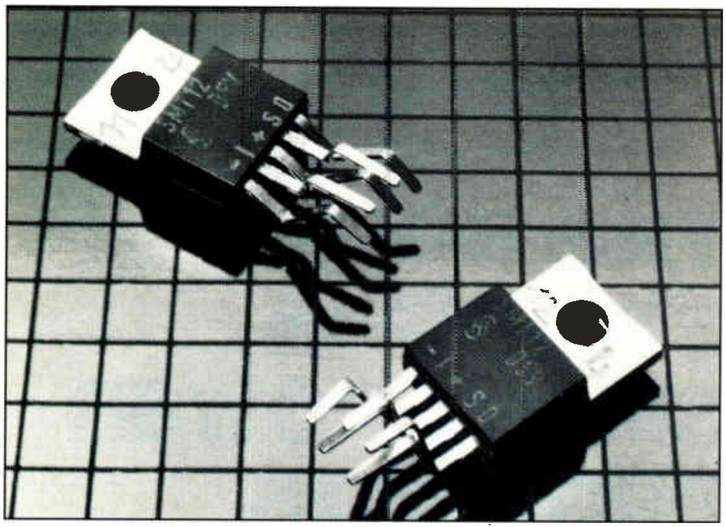
In automobiles, the wiring harness, now roughly 50 lb of wiring, could be cut in half. A single wire would be run around the perimeter of the car, and power modules to control lights, seats, power windows, and the air conditioner would be clipped on where needed. Also in automobiles, the 9-lb hydraulic power steering unit could be replaced by a 3-lb motor controlled by a single smart power device. The automobile industry will be a great market booster for smart power, since each car will require about 30 smart power devices.

In the future, home appliances would be modernized by smart power. Air conditioners, washing machines, and dryers all use ac motors, which are expensive to vary according to load. A properly isolated smart power IC would be able to vary the speed of the appliance's motor, making it more efficient and cutting power consumption dramatically.

SGS Semiconductor, Phoenix, Ariz., is making a big assault on the smart power industry this year, introduc-



1. HIGH POWER. The power device on SGS' VIPower chip can have a voltage capability up to 1,200 V and a current capability up to 20 A.



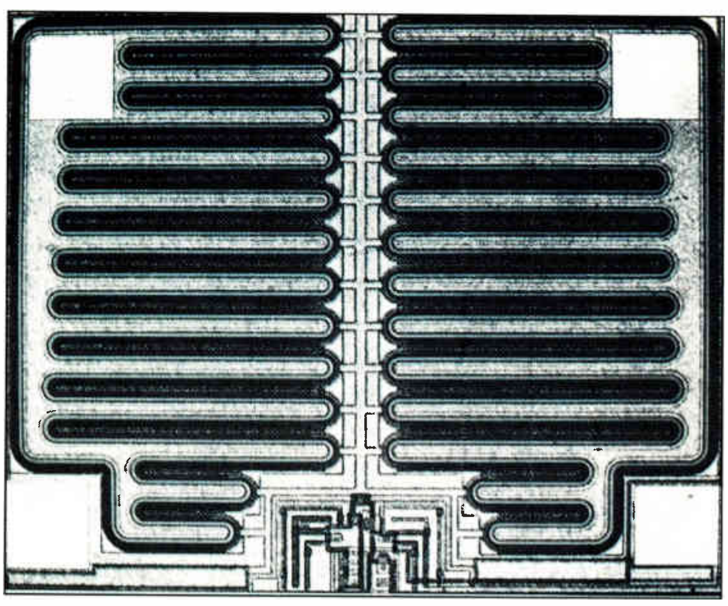
2. TAKING NOTES. Customer comments helped Siemens come up with the BTS 412, a 50-V, 12-A SIPMOS smart power chip.

ing a new technology and a couple of new products in its basic Multipower-BCD process [*Electronics Week*, Dec. 10, 1984, p. 28]. Multipower-BCD combines bipolar linear, CMOS, and DMOS devices on the same chip with maximum supply voltages of 60 V. Subsequent parts now in development will be rated at 250 and 450 V, sufficient for some off-line switching supplies, solid-state relays, and fluorescent-display drivers.

While the Multipower process has many advantages, it cannot compete with vertical power processes in terms of voltage and current. So SGS adapted two new pure bipolar vertical power processes for a smart power process that is called VIPower, for Vertical Intelligent Power (Fig. 1).

The VIPower family will offer voltage capability up to 1,200 V and current capability up to 20 A. Moreover, the power transistor can be npn bipolar or DMOS, and a mixture of CMOS and bipolar drive circuits can be included. The first products being designed will be general-purpose 400-V 10-A high-speed switches with logic-level inputs and full protection circuitry incorporating diagnostic outputs. The typical applications for VIPower will be in high-voltage off-line power supplies, controller/drivers of automotive ignition coils, motor controllers in robotics systems, and CRT deflection.

3. BIDIRECTIONAL. International Rectifier's BOS FET switches bidirectionally and can handle up to 300 V.



SGS is expanding the Multipower-BCD process with a 10-A dc-to-dc converter, a 100-W class D audio amplifier, and intelligent switches for multiplexed wiring systems. In the near future, it will use Multipower-BCD to build specialized peripheral driver circuits with optimized power and control sections for each load type.

West Germany's Siemens AG first tested the power IC waters by introducing a part using its Smart Sipmos process in the fall of 1985 [*Electronics*, Sept. 2, 1985, p. 51]. Designated the SMT 12, the device was a technical demonstration product provided in engineering samples. After comments from prospective customers, Siemens went back to the labs and emerged with an enhanced device, now called the BTS 412.

VERSATILE SWITCH

The BTS 412 (Fig. 2) is designed to switch every type of power load and is compatible with TTL or CMOS logic. The device works in a voltage range between 7 and 50 V and can be used in both 12- and 24-V applications. The maximum load current is 12 A. It is equipped with two essential protective functions: in case of a short circuit, the current is switched off after 220 μs; in the event of an overload condition, the temperature sensor will switch off the component when the junction temperature exceeds 150°C.

In addition to the Sipmos output transistor, the chip includes 5-V CMOS logic circuits, bipolar components, and high-voltage CMOS circuits. Smart Sipmos technology integrates 5-V CMOS, high-voltage CMOS, and bipolar structures with vertical power MOS FETs without junction or dielectric isolation. George Fodor, marketing manager for the Siemens Power Semiconductor Division of Broomfield, Colo., says that the isolation technique is proprietary and won't give out any further details.

Sipmos does not require more than the simple epitaxial base material of a normal Sipmos transistor. This makes Smart Sipmos a cost-effective solution for industrial and automotive electronics, Siemens claims.

The next Smart Sipmos part, due sometime in the third quarter, will incorporate thermal protection. "The device takes the worry of thermal protection off the designer. You can't kill the device by overheating it," Fodor says.

International Rectifier Corp. is adding a monolithic member to its family of hybrid parts. The

Crydom division of the El Segundo, Calif., company is bringing out a bidirectional power IC (Fig. 3) that has the dc output characteristics associated with transistors but can provide ac outputs as a triac would. The device, called a BOS FET, contains a bidirectional (ac or dc) n-channel power MOS FET output structure derived by fabricating two of the company's HEXFETs in inverse series, along with input circuitry for fast turn-off and gate protection. The BF series comprises 100-V and 300-V models.

The BOS FET is the same device that is part of Crydom's PhotoVoltaic Relay hybrid series, but it has not been available separately until now. The monolithic BOS FET is fabricated in a high-voltage process similar to the n-well CMOS that integrates high-voltage lateral DMOS transistors with a variety of low-voltage control components.

The BF series, available in 8-pin dual-in-line packages, has a supply voltage range of 3 to 10 V, a gate current range of 0.3 to 3 μA, and an input impedance of more than 8 MΩ. Output characteristics when used as an ac/dc switch are a drain supply blocking voltage of 100 or 300 V peak, an on-resistance of 4 or 24 Ω, and an on-state drain current of 250 or 125 mA. The output terminals can be reconfigured to operate unidirectionally (dc), and the on-resistance can thereby be decreased by a factor of four. Crydom is targeting the devices at applications in general-purpose control of analog signals in low-power instrumentation and in information processing.

Motorola Semiconductor Products Inc. of Phoenix, Ariz., uses a C/DMOS process to attract the automotive, industrial power supply, microprocessor support, and motor control markets. Motorola's SMARTpower products are low-to-medium-voltage, high-current parts. Roger Janikowski, marketing manager, says Motorola does not offer low-current, high-voltage parts such as display drivers.

VERTICAL DMOS

Motorola's smart-power process is a combination of CMOS logic and its proprietary TMOS power structures on a single chip (Fig. 4). TMOS is a vertical implementation of DMOS. The first products to use the C/DMOS process were the MPC2000 family of overvoltage and temperature protection circuits [*Electronics*, Oct. 7, 1985, p. 65].

Motorola is readying a new family of devices using this technology. The first of these, the MPC1500, is a 16-A device and has an n-channel output power MOS FET. The intelligence on the chip includes the charge-pump circuitry, which can generate the proper gate drive. The 1500 also has pulse-width-modulation circuitry to control the inrush current to a lamp (like a head-

WHAT IS SMART POWER?

The precise definition of "smart power" is the subject of debate. But most agree that, functionally, the role of a smart power circuit is to interface between digital control logic and a power load. For example, a power transistor that is driving a relay or motor and can limit current, provide thermal protection, and send status messages back to a microprocessor is a smart power part.

A dozen or so companies make smart-power products. While most refer to their offerings generically as smart power devices, SMARTpower—as one word—is a Motorola trademark.

Broadly speaking, smart-power products include high-voltage, high-current devices, low-voltage, high-current parts, and high-voltage, low-current devices. Some companies say only monolithic circuits can be smart power devices; others maintain that hybrid parts can be included as well.

A quick look at what's available shows that the only widely used product that can be deemed a true smart power integrated circuit is the flat-panel display driver. Smart motor drivers are also beginning to make their way into the market. But no true monolithic high-voltage, high-current smart power chip yet exists.

At Sprague Electric Co., Brad Marshall defines a power IC as a single-chip monolithic part that operates at 1 A and 1 W or more—that has been the traditional line of demarcation between a transistor and a power transistor. Marshall, who is director of marketing and product development at the Worcester, Mass., company, says that a smart power IC must contain logic circuitry in such processes as CMOS or integrated injection logic.

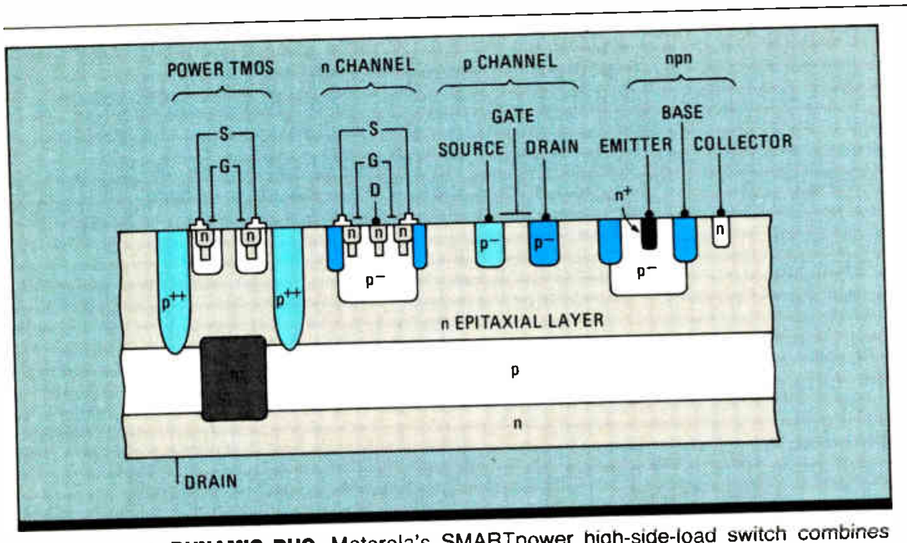
Others, however, take exception to the argument that a smart power transistor must be monolithic. Alexander Lidow, executive vice president of manufacturing and technology at International Rectifier Corp., says a smart power device is any part that "is the interface between control and a load that requires greater than 1 W of power." Lidow likes to call the devices power interface circuits, which encompasses the hybrid solutions that the El Segundo, Calif., company and its Crydom subsidiary proffer.

"In the world of power interface, the user cares about performance, reliability, and cost," Lidow says. So the user doesn't care if the part is a hybrid or monolithic solution, he maintains.

Bill Numann, marketing manager of Siliconix Inc., concurs. "Siliconix analyzes the application and determines the more feasible approach, single or multichip solutions," he says. Whatever is most cost-effective is the route the Santa Clara, Calif., company takes.

To those who say monolithic solutions are more reliable, Lidow points out that by putting power and logic on the same chip, a manufacturer is localizing the heat. That localization can subject the logic—which is usually designed to run under 80°C—to the temperatures to which power is usually subjected, 150°C.

As for economy, a monolithic solution may not always be the less costly approach. Numann asks why someone would want to take the relatively simple and inexpensive task of creating power transistors and construct them with the multiple number of masks required in logic circuits. The biggest obstacle to widespread acceptance of power interface circuits is the misconception that hybrids are not smart power. "It's a macho thing to put it all on the same chip," Lidow quips.



4. DYNAMIC DUO. Motorola's SMARTpower high-side-load switch combines vertical output devices and low-level control elements on one chip.

light), says Dan Artuis, Motorola's manager of strategic marketing for discrete products.

The third smart attribute of the 1500 is fault detection. For example, there is an output that indicates if the lamp is burned out or has a short circuit. That information is a logic-level signal that is applied to the higher levels of control back to the host controller. The MPC1510 is similar to the 1500 but does not have the pwm circuitry. Therefore, it is targeted at applications that do not have to deal with large inrush currents. This part can handle 10 to 15 A.

Another series coming down the pike is targeted at motor-control applications. The first device will be the MPC1700, which is a controller for the unidirectional permanent-magnet motors found in air conditioners and fuel pumps. Motorola will start offering samples in the fall.

ROUNDING OUT A LINE

Supertex Inc. of Sunnyvale, Calif., is rounding out its line of electroluminescent-display drivers with 32-channel column and row drivers. The HV51 and HV52 are monolithic serial-to-parallel converters with open-drain outputs for driving the rows. The pair has outputs of up to 225 V and a sink current of 100 mA. The internal shift registers operate at 8 MHz. The 8-MHz column drivers, the HV53 and HV54, have output voltages as high as 80 V and a source or sink current minimum of 20 mA.

Supertex builds its chips in a proprietary high-voltage CMOS process that combines high-voltage DMOS output capabilities with low-power, high-speed silicon-gate CMOS logic. In addition to use in electroluminescent displays, the chips can be used for nonimpact printers, facsimile machines, and in automatic test equipment.

Sprague Electric Co. applies its BiMOS process to two areas: flat-panel-display drivers, characterized by high-voltage, low-current devices; and motor driver ICs, characterized by medium-voltage, medium-current devices. The latter makes up 90% of the market, estimates Sprague's Brad Marshall, director of marketing and product development. The Worcester, Mass., company's BiMOS process, a fusion of bipolar and CMOS, offers output breakdown voltages of up to 100 V, output current ratings as high as 600 mA, and a logic input voltage range of 5 to 15 V. Logic switching speeds of up to 1 MHz at 5 V and up to 2 MHz at 12 V can be accommodated. Among the advantages of BiMOS are microprocessor compatibility, low-power logic, a wide logic-supply range, bipolar output capability, CMOS noise immunity, and space-saving integration.

Sprague's four new BiMOS products are high-current bipolar Darlington power drivers for microprocessor-based applications with relays, solenoids, stepper motors, LEDs, or other high-power loads up to 480 W. The UCN-5813B and UCN-5814B will sink up to 1.5 A per channel and include transient suppression diodes. The 5813B and 5814B are rated for 50-V operation, while the 5813B-1 and 5814B-1 are rated for 80-V operation.

A MOSTEK ENTRY

A new entrant into the smart power market is Thomson Components Mostek Corp. [*Electronics*, June 23, 1986, p. 21]. The company is taking a two-pronged approach into smart power with a high-side load power IC, the MK5501, and a line of flat-panel-display drivers second-sourced from Supertex. The MK5501, which is slated to be ready for volume production in the first months of 1987, is made in a high-yielding 5-μm process. This conservative approach to process technology is critical to keeping the parts in the right price range, says Steve Whipple, director of power products operations for the Carrollton, Texas, company. Such automotive power ICs eventually will have to sell for less than $1, he says.

Mostek is combining bipolar and CMOS on the chip, along with vertical DMOS. It claims to have a patentable process that yields small FETs by reducing the number of masking steps. Since the part is 60% to 70% MOS FET, reduction of that area is more important to the die size than using fine geometries in the logic and analog portion of the device, Whipple says. The MK5501 is a 10-A, 60-V intelligent power switch. It is housed in a TO-3 package with eight pins, and it will be housed in a five-pin TO-222 plastic package when ready for volume production next year.

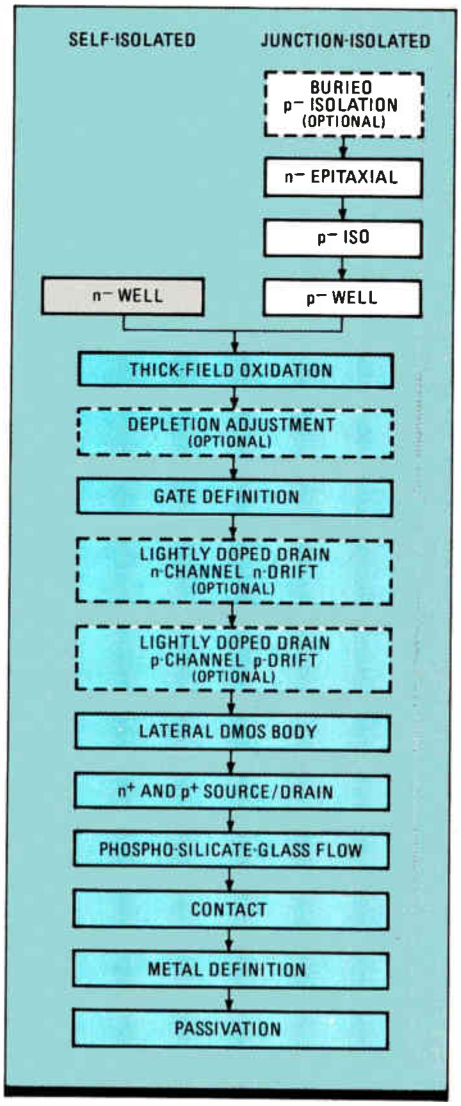
Whipple says Mostek is within a couple of months of offering samples of EL display drivers that are mask-compatible with HV03-HV06 parts from Supertex. Mostek's parts, the 5563-5566, are 64-line row and column drivers. Volume production will start sometime in the third quarter.

Another new entrant into the market is a Scottish company, Integrated Power Semiconductors Ltd., with U. S. headquarters in Santa Clara, Calif. The company is readying chips aimed at power supplies, motor controls, and solenoid drivers.

A number of other companies, which do not have new products at this moment, are competing for the smart power dollars. Among them are Siliconix, GE, TI, Unitrode, and Telmos.

Siliconix Inc., Santa Clara, uses two related processes to fabricate its line of smart power devices (Fig. 5). The self-isolated D/CMOS is a modification of a conventional n-well self-aligned CMOS process. The modification allows the fabrication of n-channel lateral DMOS transistors, in addition to both n-channel and p-channel MOS devices.

The process sequence is capable of any combination of low-voltage CMOS, high-voltage n-channel enhancement- or depletion-mode lateral DMOS and high-voltage PMOS. In December, Siliconix expects to ship a single-chip 1-W switching power supply fabricated in this process. The Si9100 has a single-ended 120-V device with a low on-resistance and an n-channel output. In this circuit, high-voltage PMOS devices are not required, simplifying the process implementation. Siliconix also uses its self-isolated process to make EL-display drivers that contain 90-V push-pull output devices.



5. COMMON THREAD. Siliconix has two similar processes for building smart power devices.

JUNCTION ISOLATION

The second Siliconix process, a junction-isolated D/CMOS process, is a modification of a combined bipolar p-well self-aligned CMOS process. This modification allows the fabrication of pnp and npn bipolar transistors as well as high-voltage n-channel lateral DMOS transistors and both n- and p-channel devices. The n-channel lateral DMOS transistors can be used exclusively for high-voltage requirements.

Unlike self-isolated devices, each lateral n-channel DMOS drain or vertical npn collector must be enclosed by a p+ isolation diffusion to isolate adjacent devices from one another. Since it takes a lot of silicon area to isolate each n-channel logic device, low-voltage CMOS circuitry is implemented using conventional n-MOS devices fabricated in a p− well.

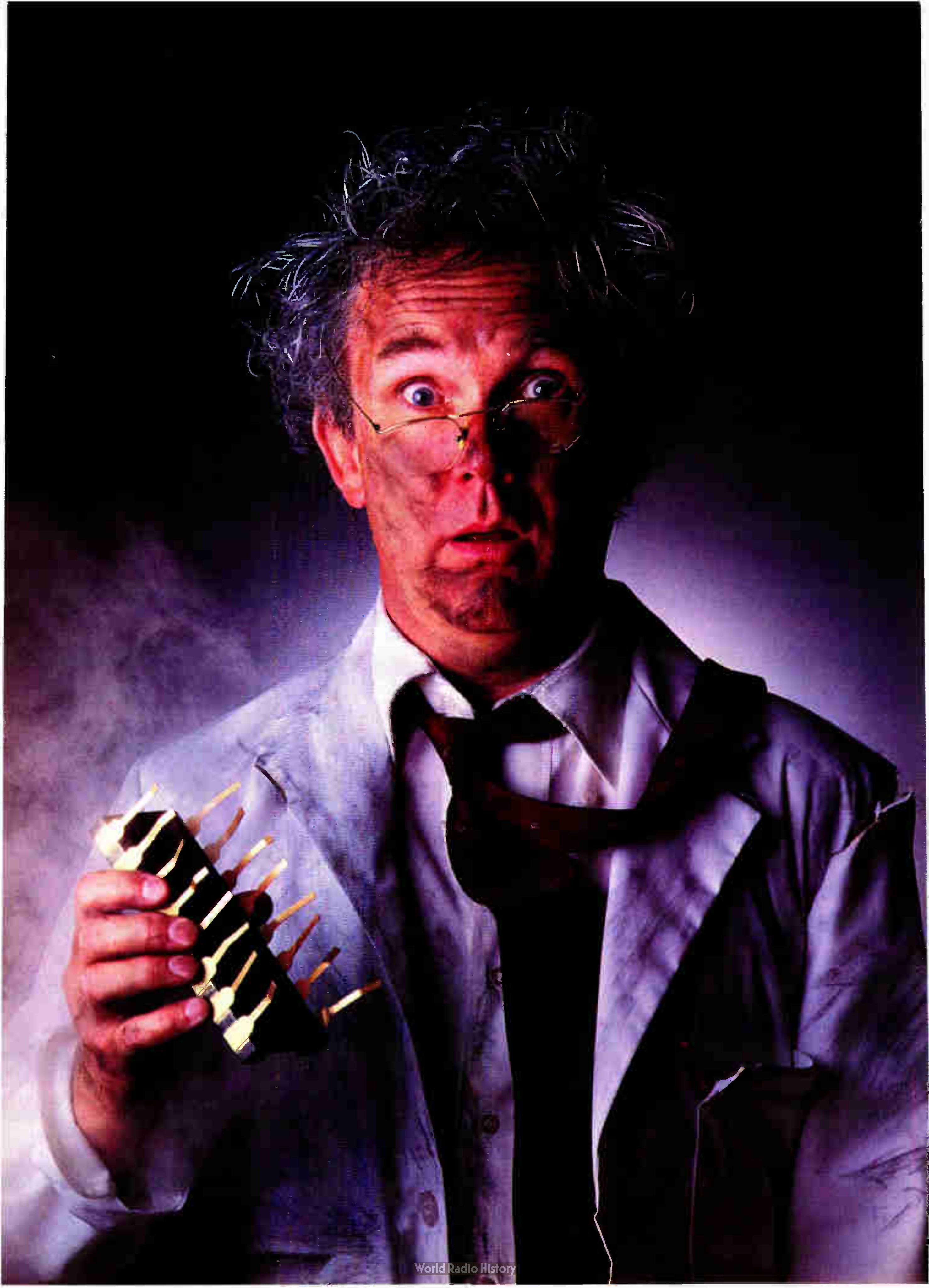
The most significant characteristic of junction-isolated D/CMOS is its compatibility with circuit applications that require bipolar supply operation or ground-referenced high-voltage ac operation. One example of such a part is the DG568 eight-channel multiplexer, which is designed for high-voltage applications in microprocessor-based instrumentation and process control.

General Electric Co. takes a semicustom approach to smart power. To show off the capabilities of GE-Smart technology, late last year the Power Electronics Semiconductor Department in Research Triangle Park, N. C., introduced an off-the-shelf motor driver circuit. The GS1E10MA control circuit, for fractional-horsepower electric motors, is rated at 500 V with the potential of switching up to 10 A in less than 1 μs. The GS1E10MA contains two power MOS insulated-gate transistors, two fast-recovery flyback diodes, and a high-voltage IC optimized for half-bridge pwm motor-drive applications.

Texas Instruments Inc. makes flat-panel-display drivers in its junction-isolated Bid-FET process. CMOS logic controls DMOS power devices, which drive bipolar power transistors. The Dallas company's process handles the 200-V levels that are required for EL displays.

Unitrode Corp. uses a combination bipolar-CMOS process similar to Sprague's to fabricate drivers for stepper motors, piezo elements, and relays. For example, the Lexington, Mass., company's UC3717 stepper-motor driver combines a low-power Schottky-TTL input, a current sensor, and an output stage with built-in Schottky diodes for thermal protection.

Telmos Inc. gets 500-V capability in its smart power devices by combining a 500-V n-channel, 500-V p-channel, and 500-V insulated gate thyristor on a chip that also has conventional low-voltage CMOS transistors. The Sunnyvale company's chips control ink-jet and electrostatic printers and work in telecommunications. □



REMEMBER WHEN THE CHIPS WERE DOWN?

Your system, or maybe even your entire line, was down. The chips you ordered didn't meet spec, quantities were insufficient, or maybe they weren't produced at all. It's a hair-raising experience.

INMOS understands how you feel. That's why we're dedicated to the highest standards of quality and reliability, without compromising performance in any of our products: SRAMs, DRAMs, Microcomputer products or ASICs.

For example, our CMOS Static RAMs have quality levels better than 300ppm and reliability levels below 50 fits. This means with 16 of our 16K SRAMs, your cache memory should have better than 100 years of failure-free performance.

We know the stakes are high. At INMOS, you get products you can depend on from a company you can depend on.

16K CMOS SRAMs	
Device	Access Times
IMS1403 (x1)	20, 25, 35, 45ns
IMS1423 (x4)	23, 35, 45ns

64K CMOS SRAMs	
Device	Access Times
IMS1600 (x1)	35, 45, 55ns
IMS1620 (x4)	35, 45, 55ns
IMS1624 (OE, x4)	35, 45, 55ns
IMS1630 (x8)	45, 55, 70ns

LOW POWER DATA RETENTION CMOS SRAMs		
Device	Access Times	Idr*
IMS1403L (x1)	25, 35, 45ns	0.5µA
IMS1601L (x1)	45, 55, 70ns	10µA
IMS1620L (x4)	45, 55, 70ns	10µA
IMS1624L (OE, x4)	45, 55, 70ns	10µA

All above products are available in MIL-STD-883C *Idr = Typical Icc at 2V at 25° centigrade.

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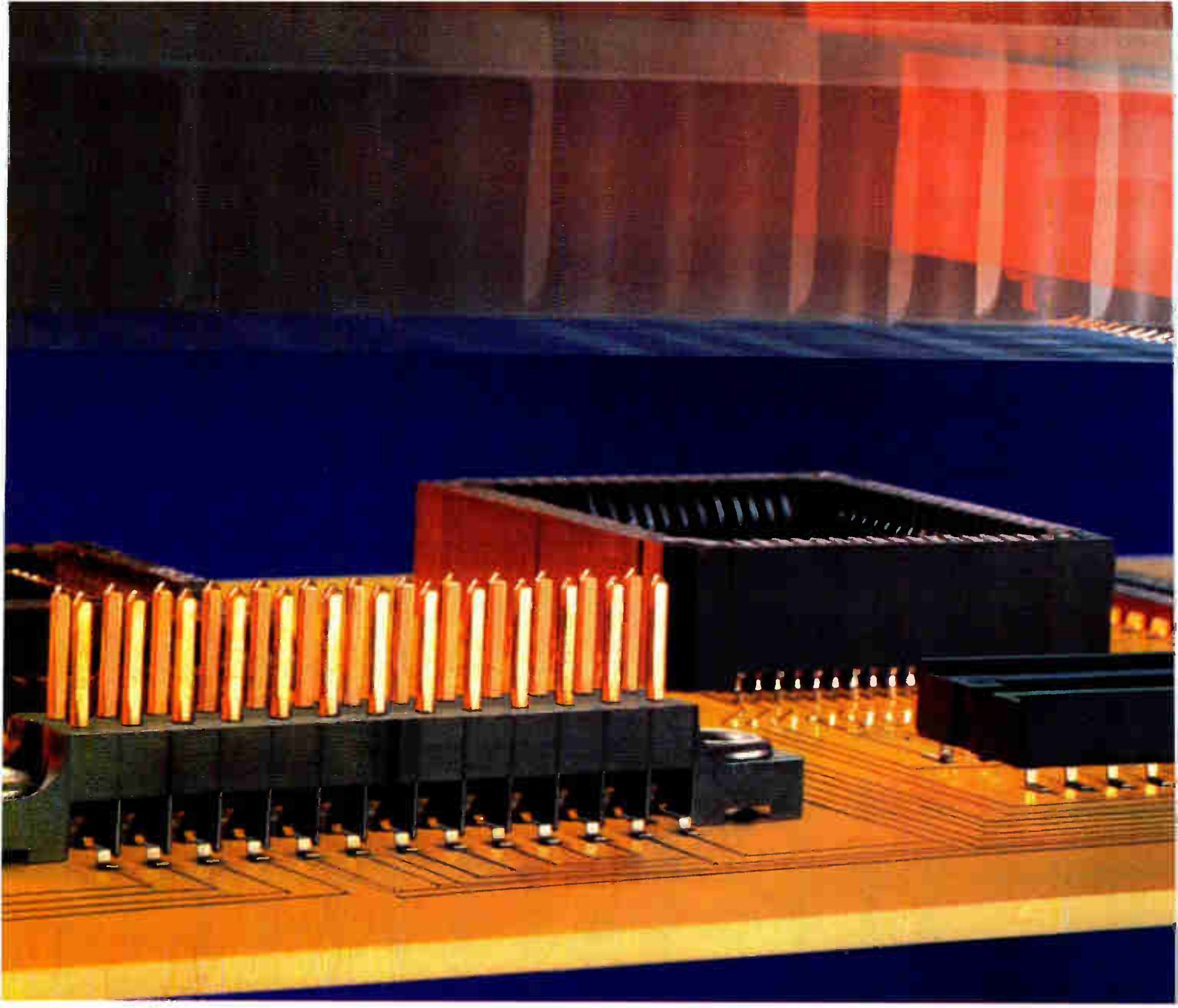
Circle 103 on reader service card



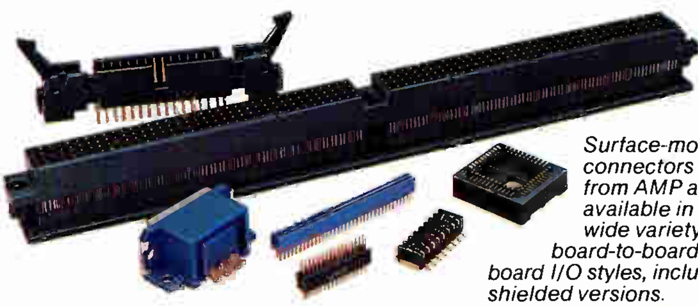
How AMP adds depth to

Technologies expand—and pay off—when they get in-depth support.

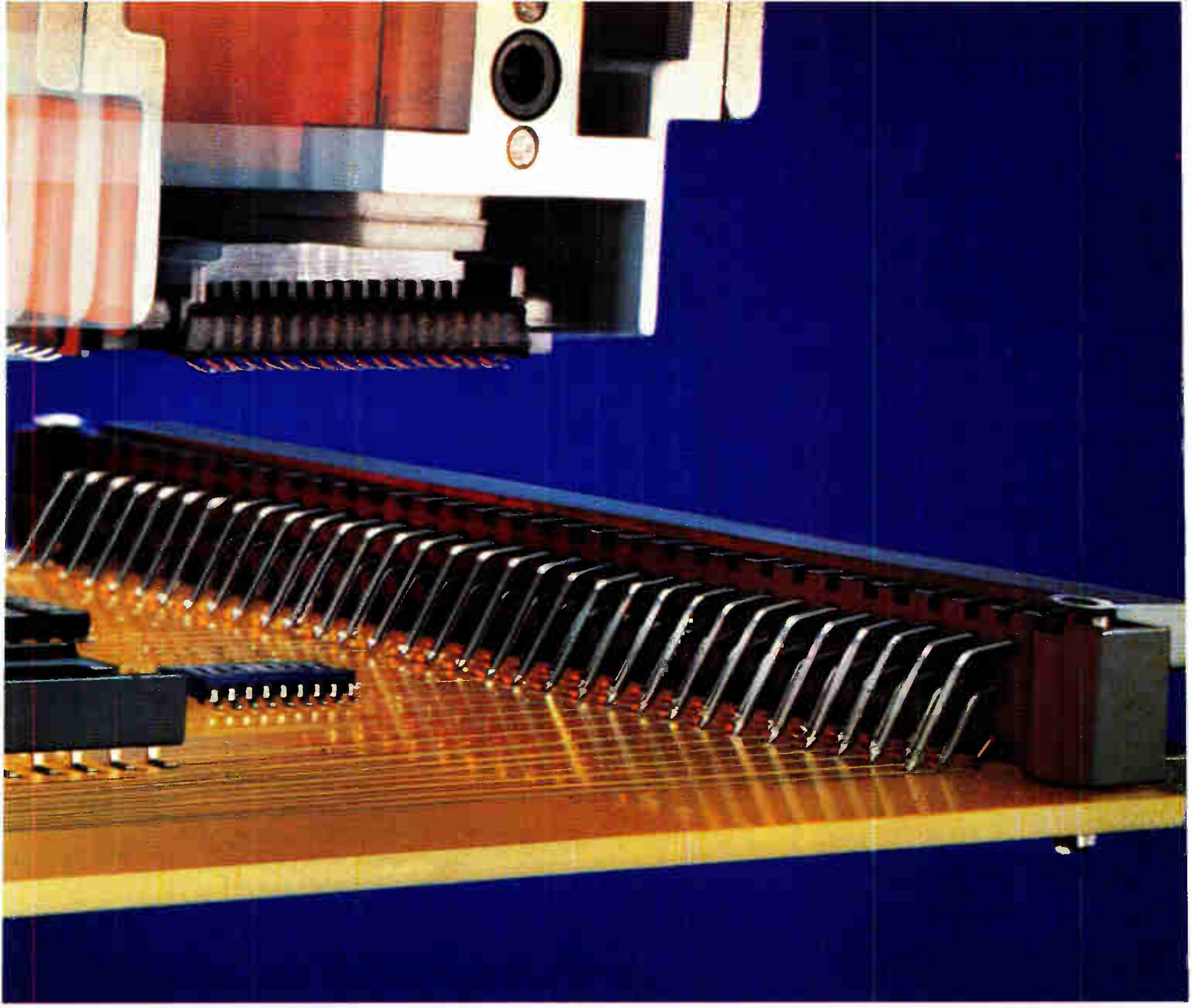
Many popular AMP connectors and sockets are already available in surface-mount styles. With more being developed every day. The depth? In the design, and in the usual for us—the technological backing to make a product both practical and affordable.

For instance, many of our SURMOUNT products are designed for flexible automation. Robotic systems offer fast production changeover via programming control. And we offer what you need to make it work: feeder and positioning equipment, and a variety of compatible packages, from tape and single tubes to stacking, multi-track trays.

All SURMOUNT products are in tested materials, naturally. Plastics and platings developed to withstand the process conditions of surface mounting. Because the technology is developing,



Surface-mount connectors from AMP are available in a wide variety of board-to-board and board I/O styles, including shielded versions.



EMERGING COMPUTER TOOLS SPEED UP SOFTWARE DESIGN

Structured design and analysis tools help design program modules faster and with less bugs; moreover, they cover all seven phases of the software development cycle

by Alexander Wolfe and Jonah McLeod

Software engineers are bootstrapping their expertise to create a whole new class of structured design and analysis tools. These tools make up a framework called CASE, for computer-aided software engineering, and help design program modules faster and with fewer bugs.

As such, they are serving a steadily growing market. Developers of embedded systems spent $395 million on off-the-shelf and in-house CASE tools in 1985, estimates Tektronix Inc. By 1990, the company says, that figure could rise to $1.4 billion.

CASE's time is certainly at hand. The Department of Defense projects that the need for new software will increase 12% a year compounded. Measured another way, the DOD calculates that software accounted for only 5% of a typical system five years ago. Today, that figure is 50%—and in five years, it will be 95%.

In CASE, the software development cycle is broken down into seven phases: analysis, design, prototyping, coding, testing, integration, and maintenance. Three broad classes of design tools serve these seven phases. These tools typically run on superminicomputers such as Digital Equipment Corp.'s VAX family and, increasingly, on work stations.

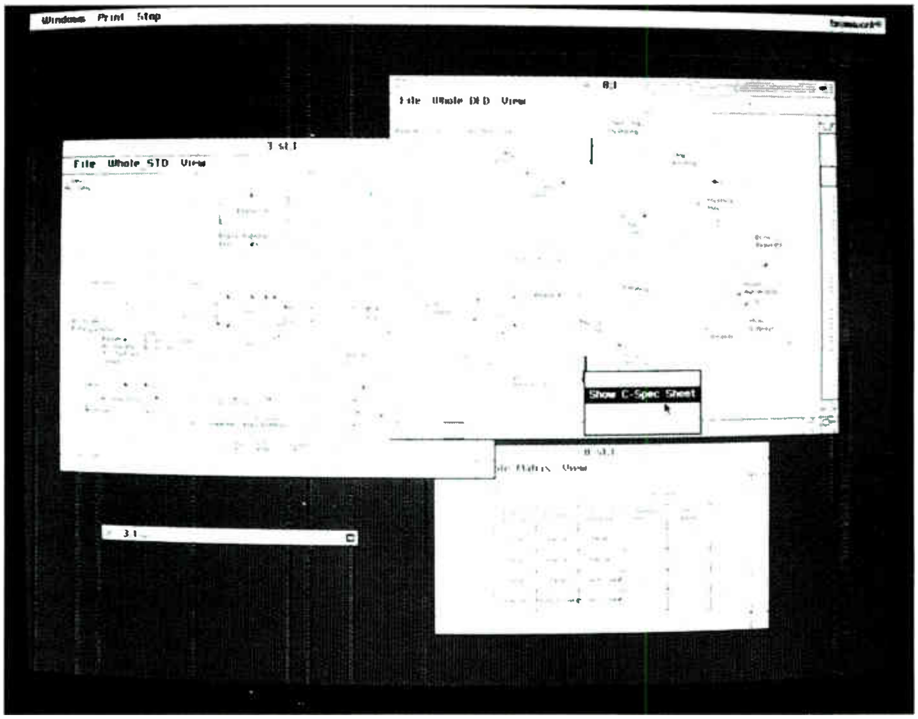
Design tools encompass the analysis and design phases. Dominating this class are structured design and structured analysis products. Implementation tools, enveloping the code and test phases, make up the second category. Here, compilers are the main CASE product. (Prototyping tools straddle both the design and implementation categories.) Finally, the integration-tool class covers the integration and maintenance phase. Symbolic debuggers and hardware emulators are key integration tools.

All three classes will grow rapidly for the rest of the decade. A breakdown of the CASE market by

BRANCHING OUT. Tektronix Inc.'s graphics modeling tool now can run on Apollo Domain work stations and IBM's PC AT and PC/XT.

Tektronix shows that design tools stood at $100 million in 1985, with only 25% of that spent on off-the-shelf products. Total consumption, including tools developed in-house, will rise to $588 million by 1990. Sales of implementation tools were $138 million in 1985, $411 million predicted by 1990. Textronix estimates integration tools will rise from $157 million in 1985 to $441 million in 1990—but these figures cover only Motorola Inc.'s 8-, 16-, and 32-bit microprocessors and Intel Corp.'s 32-bit microprocessors, so the total integration market should be larger.

Tektronix intensified its interest in the market last month by unveiling new systems at the Design Automation Conference in Las Vegas, as did Hewlett-Packard Co., Palo Alto.



ONE FOR ALL. Hewlett-Packard's Teamwork/Structured Analysis features a project library that is the central data base for everyone working on a project.

Tektronix' Software Development Products Division in Beaverton, Ore., introduced a host of real-time development aids. The company announced that its Structured Analysis Tools—the graphics modeling aid for system specifications—is now available for Apollo Domain work stations and IBM Corp.'s Personal Computer AT and PC/XT. In addition, it unveiled Lands, for language-development system, and a universal microprocessor development system that runs on VAX and MicroVAX computers under the VMS or Unix operating systems.

HP, a relative newcomer to the CASE business, introduced HP Teamwork/Structured Analysis, a tool that provides computer-aided support for the specification phase. Its strength lies in its project library, which serves as the central data base for everyone working on a specific project and includes data-flow diagrams, data dictionaries, process specifications, annotations, and project-management data.

As the new CASE tools debut, established systems are being updated. For example, Cadre Technologies Inc. is increasing the sophistication of its graphical software development aids. The two-year-old Providence, R. I., company has added real-time capabilities to its Teamwork/SA structured analysis product with Teamwork/RT [*Electronics*, May 26, 1986, p. 13].

Following the flow of control and data in a real-time program is difficult, so Cadre used a real-time structured-analysis methodology from the Instrument Division of Lear-Siegler Inc., Santa Monica, Calif. It, in turn, is based on one developed by Tom De Marco and Ed Yourdon, founders of Yourdon Inc. of New York, a CASE tool developer.

Teamwork/RT graphically displays control-flow diagrams to provide a high-level view of the system's requirements. Control specifications show how output responses evolve from input data in combination with timing, sequence, and control requirements.

The control specifications can be represented by state-transition diagrams, state/event matrices, or process-activation tables. A data dictionary lists the definitions of data flows, data stores, and control flows used in the system.

Diagrams have been a problem, notes Cadre president Louis J. Mazzucchelli. Much real-time software development is done for the Pentagon, whose rigid specifications did not take into consideration flow diagrams generated by structured analysis systems. But the Pentagon is moving with the times, and that's no longer a problem. "A lot of people are now generating structured design diagrams and inserting them into MIL-STD-2167 documentation," he says.

END TO GUESSWORK

Intel Corp. recently introduced iPAT, a real-time software-analysis tool that works with the Hillsboro, Ore., Development System Operation's in-circuit emulation products. The product's ability to analyze performance and code coverage helps in the integration and evaluation phases.

Previously, software developers could only guess at which sections of program code to improve to speed total system performance. With iPAT, they can isolate slow or untested codes. The product monitors all microprocessor execution addresses in real time, and displays cumulative, average, minimum, and maximum time. ☐

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PROBING THE NEWS

CAN TOSHIBA MAKE IT BIG IN INFORMATION SYSTEMS?

IT'S PINNING ITS HOPES ON COMBINING COMMUNICATIONS AND COMPUTERS

by Michael Berger

TOKYO

Close by Tokyo Bay stands a 40-story silver-gray skyscraper that symbolizes the future of an electronics giant. Toshiba Corp.'s new headquarters, located on the very site where the $14 billion conglomerate began as a small engineering office in 1875, has been designed for the future. It is equipped with fiber-optic lines, local-area networks, and all the equipment that Toshiba hopes is the basis for its future growth.

Toshiba sees its future in information systems—the combination of communications systems and computers that will dominate the office- and factory-automation markets—and the company is fashioning a global strategy intended to put it at the center of these markets. It is a strategy bent on synergizing the strength of Toshiba's diverse technological know-how and forging a series of technical and marketing links with foreign companies (see "Two years of deals fill the niches," p. 112) to create the products and systems it needs to penetrate those key markets. Expansion of overseas operations is another facet of the strategy, and the company plans to build up its already impressive research and development efforts, with one thrust focusing on its leading-edge CMOS semiconductor technology.

The new skyscraper is intended as a showcase for Toshiba's thrust into information systems. To some observers, however, the new building and its electronic infrastructure are symbols of unfulfilled potential. Computers adorn the desks of all Toshiba division executives, but as one admits, "I rarely use it—no time."

The critics say that Toshiba suffers from a reputation as a company that too often is first to market with a product but last to cash in on it. In 1979, for example, Toshiba was the first Japanese company to produce a word processor. But just as marketing got under way, a key executive who had masterminded the project was suddenly switched to another division, and the marketing effort soon lost steam. Toshiba then watched as Fujitsu Ltd., NEC Corp., and its other rivals moved in to dominate the market. Toshiba later made a comeback, but it's the first fumble that most people remember.

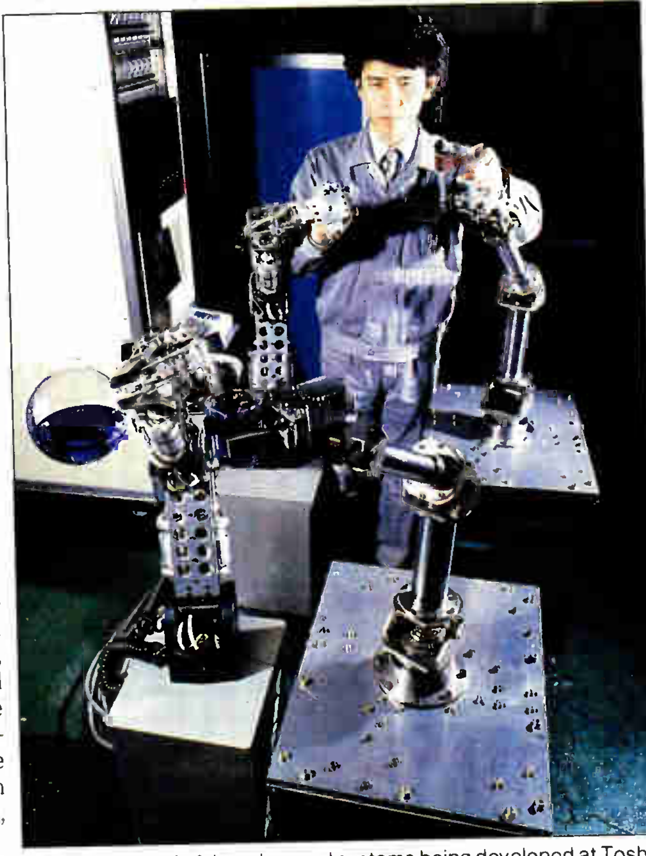
But a number of industry executives and analysts believe that the clear signs of change at Toshiba, above and beyond its gleaming new building, make it a company to watch. "The sleeping elephant is now awake," commented the respected economics journal *Nikkei Business*.

"Toshiba has strong CMOS technology, [a technology] which clearly is going to be dominant in the future," says analyst David Keller of James Capel & Co.'s Tokyo office. "They've also got the kind of know-how to create superior production or communications systems inside the factory or office. But the question is: can they put it all together?"

The answer, say company insiders, rests on the success or failure of a master plan that Toshiba cryptically calls Project I.

"It stands for 'integration and information,'" says the new president and chief executive officer, Sugiichiro Watari, a small and energetic man with a reputation as a hard-driving, efficient manager. Watari's major task is to carry through the basic changes that began under his predecessor, Shoichi Saba, who is now chairman of the board. Project I, his first major undertaking, is designed, he says, "to integrate our strengths—all our Toshiba divisions—to focus our talent and technology on the key markets of the future, which we believe will be communications-related."

The company once known as Tokyo Shibaura Electric Co. also is undergoing a radical shift in the weight of its sales. Just seven years ago, the annual sales of its industrial electronics and components division were 25% of the consolidated total. The division's $4.8 billion in sales last year were 33% of the $14 billion total. By 1988, the company plans to increase that ratio to 44%, and by 1995 it expects the division to account for a full 60% of sales. The division should dominate the company's sales be-



HELPER. Typical of the advanced systems being developed at Toshiba's laboratories is this robot for sites too hazardous for humans.

cause it is the center of Toshiba's effort in information systems.

The most obvious competitor in the race for a strong position in information systems is not an American or European manufacturer, but a company just across town: Hitachi Ltd. "Hitachi is a natural target for Toshiba," says analyst Peter Rawle of W. I. Carr & Sons (Overseas), "because it is the industry leader in those areas where Toshiba is strong: factory systems, heavy industrial machinery, and industrial electronics." And Hitachi, like Fujitsu and NEC, is strong in the mainframe market, where Toshiba doesn't even compete. But Rawle and other industry sources note that coming markets may be characterized by smaller-scale office and factory systems based on micro- or even minicomputers rather than traditional mainframes. "If that turns out to be true," Rawle says, "Toshiba could be in a very good position, because it's already strong in those products and now it's trying to integrate them."

Moreover, Toshiba executives and engineers like to emphasize that they're "willing to shake hands with anyone" to design systems to customer needs. "They've built business computer systems which are IBM-compatible," notes James Capel analyst Keller. "They've got a venture with NEC [NEC-Toshiba Information Systems Co.] which produces office computer systems, and they've built still other systems around Fujitsu or Hitachi operating systems. They're very flexible."

VAST POTENTIAL. That flexibility, if fused with Toshiba's diverse customer base, adds up to enormous sales potential. For the fiscal year ending last March 31, Toshiba reported $1.42 billion in machine tools and new materials; $3.68 billion in heavy-machinery sales; and $4.43 billion in consumer electronics; as well as the $4.80 billion in industrial electronics and components. (All currency conversions in this article use a rate of 235 yen = $1.) If Toshiba can, as it boldly predicts, build systems for anyone, it could draw upon hundreds of customers in each of its various divisions.

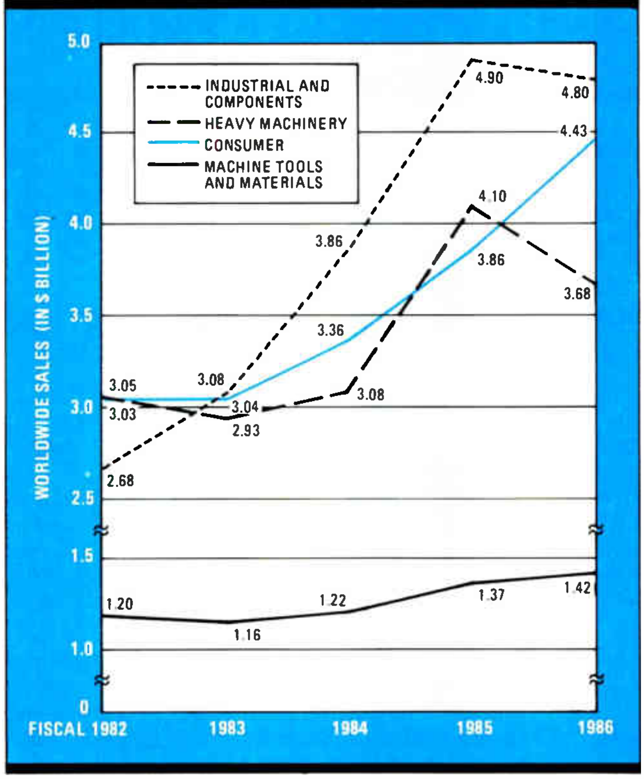
The company recently reported a 31% drop in net income for the last fiscal year, but every Japanese electronics maker is reporting similar drops these days because of last year's worldwide semiconductor market slump and the ravaging effects of the yen's 40% appreciation. Hitachi, for example, reported a 29% drop in profits, and NEC's results were off a staggering 59.5%.

This year, Toshiba predicts an increase in sales to $15.5 billion but a drop in net income to about $204 million, as the company adjusts to the new dollar-yen levels. Analyst Rawle of W. I. Carr, however, predicts that total sales will move from a modest 7% growth in the current fiscal year to 11% in fiscal 1987 (ending March 31, 1988). What's more, he holds that net income—which will drop 11% this fiscal year—will rebound spectacularly to 57% growth in 1987.

"We feel that the combination of fairly strong 3% growth in the U. S. economy during the second half of this year and the effects of Toshiba's adjustments to the stronger yen mean a very strong fiscal 1987 for them, especially in computer-related products and semiconductors," Rawle says.

Toshiba boldly predicts that it can build systems for any user

TOSHIBA'S STRENGTH IS ITS DIVERSE CUSTOMER BASE



Analyst Keller of James Capel disagrees—for the short term. "We feel that it's highly probable that the yen could strengthen to 240 by the end of this year," he says. "That would put not only Toshiba but every other Japanese electronics major against the wall in terms of their international competitiveness."

Such a crisis, he contends, would lead to a greatly strengthened South Korean presence over the long run and force Japanese companies to come up with new information systems to keep their technological edge. Under these conditions, Keller says, "Toshiba could be in a very strong position long term. Of all the major Japanese electronics makers, it is the most aggressive in seeking to enter information-distribution markets."

One reason for Toshiba's new aggressiveness is Watari. He has been president less than three months, but Toshiba insiders say they see changes already. For example, in an effort to keep ideas flowing, meetings of departmental engineers now take place weekly instead of monthly. "We have to improve our ability to bring up good ideas from the bottom of the company to the top and get them to the market as fast as possible," Watari says.

"We clearly see the rising demand for systems for process control in heavy industry, communications systems for the office," the president goes on. "We need strong horizontal communication among our divisions, but we have not always had good communication in the past."

His style is intense, says semiconductor group executive Tsuyoshi Kawanishi, adding that "I am going to visit a major customer tomorrow, and president Watari is taking me in his car. I not only get extra time to talk with him, but I can use him to improve relations with customers."

Although Project I specifies integration and information, it might also stand for industrial electronics. This division, which has grown at an annual rate of 20% for the last five years, includes most of the products that are central to Toshiba's strategy—electronic components, office automation equipment, and telecommunications. The newly appointed executive vice president in charge of the division, Joichi Aoi, is also one of the architects of Project I.

As another part of the integration

FOREIGN SALES PLAY GROWING ROLE AT TOSHIBA

Fiscal year	$ billions		% of total
	Sales	Overseas sales	
1982	9.97	2.68	26.80
1983	10.21	2.61	25.56
1984	11.51	3.14	27.28
1985	14.22	4.44	31.22
1986	14.34	4.48	31.24

SOURCE: TOSHIBA CORP.

BIG LEAP. At the VLSI Laboratory, the main work is on the difficult leap from 4-to 16-Mb memories. Toshiba is increasing its R&D.

strategy, former Industrial Electronics Division director Jun Kobayashi has been named president of Toshiba's largest subsidiary, Tokyo Electric Co. Tokyo Electric has seen its business slump because of overdependence on exports—they represent 50% of sales—and overexposure in low-margin products such as printers and electronic typewriters. Kobayashi's main target is to turn Tokyo Electric into a systems-oriented producer to revitalize its still prosperous point-of-sale business and add more sophisticated products to its line.

Other companies in the Toshiba Group have been reorganized or expressly created to implement Project I. Toshiba Information Equipment Co., formed in 1984, is in charge of marketing all office-automation products and software. Toshiba Systems Development Co., founded the same year, has one task only: creating software for customers. It now has eight branches nationwide.

Last year, a new development laboratory focusing exclusively on communications products was established at Hino, a Tokyo suburb, and this year Toshiba founded another unit to work with the Ministry of Posts and Telecommunications in product development.

Even in Toshiba's traditional fields, such as nuclear energy and plant process control, the emphasis is on integrating divisional strengths. Since its research laboratories were combined under one roof in Toshiba's giant R&D Center in Kawasaki, "communication between our division and others has noticeably improved," says Takao Uchida, managing director of the Heavy Electrical Apparatus Group. Even though sales of nuclear plants slumped last year and will be adversely affected this year and next by the Chernobyl disaster, Uchida sees plenty of room for the development of new products, especially in a number of projects devoted to fuel-cell research, where Toshiba has a leading role.

Project I is overseen by a special task force, the Information and Communication Systems Business Group, which crosses product and division lines. Its senior manager, Ufo Mohri, is one of Toshiba's major strategists, a man who says his company must deal with two basic realities. "My view of the 21st Century," Mohri says, "is one of 'information imperialism'—that is, the continuing dominance of IBM in computers and AT&T in communications."

Because of its weakness in these two sectors, Toshiba's strategy is to work with the giants hand in hand, rather than to compete with them. For example, industry watchers expect that Toshiba and AT&T Co. will announce a deal in which the Japanese company will become an original-equipment manufacturer for the communications giant.

Simultaneously, Toshiba is building a new relationship with Nippon Telegraph & Telephone Corp. Before NTT went private last year, it dealt almost exclusively with a cozy family of suppliers. Now, former outsiders such as Toshiba have a shot at its business. The latest example is Toshiba's involvement in an NTT-backed five-year research project to develop a modular type of private branch exchange system capable of handling 500 lines or more.

As for IBM Corp., "We want to be a problem-solver, a systems provider, and we're willing to work with anybody," says Shigenori Matsushita, chief engineering officer of the Information Systems Business Group. "We're stronger than IBM in some areas, including image-printing, optical-character reading. We think we can offer them some advantages." He indicates that Toshiba and IBM already are working together on product development, but he would not provide details.

PORTABLES. The product line Matsushita likes to talk about most is Toshiba's new T-Series of IBM-compatible portable computers, which hit the U. S. market just this year. The push into the U. S. personal computer market is just the latest in a series of moves overseas, both in manufacturing and marketing. Toshiba has more than 10,000 workers at overseas plants and will add another 1,000 this year in the U. S. alone, where its subsidiary, Toshiba Corp. USA, is expanding. (Toshiba will not divulge sales figures for its foreign enterprises.)

Reacting to both trade pressure and

WATARI: Toshiba's president and CEO is pinning his hopes on Project I.

KAWANISHI: Head of the semiconductor group likes Watari's intense style.

the appreciation of the yen, Toshiba has moved quickly to establish more overseas production bases in a variety of products. Two months ago in Dallas, it opened its third semiconductor design center in the U. S. and plans to build three more in Boca Raton, Fla., Chicago, and Los Angeles. This fall, another new $44 million plant in Irvine, Calif., will begin producing X-ray diagnostic and computer-axial-tomography equipment as well as key telephones.

Nor is overseas expansion confined to the U. S. Toshiba has formed two companies in Europe in the last six months, one in Britain and one in France, and plans to open a West German operation in 1987. Toshiba Information Systems UK will market office automation products and Toshiba Systemès (France) SA, a joint venture with Rhône-Poulenc SA, will begin producing portable computers by the end of the year. The West German venture is a videocassette recorder plant, Toshiba Consumer Products (Germany) GmbH.

To buttress these overseas operations, Toshiba is making a big investment in R&D. Semiconductor R&D is clearly a key area, for Toshiba keenly wants to follow up its success in 1-Mb RAMs. The hub of research at the VLSI Laboratory is laying the groundwork for what Kawanishi calls "the much more difficult leap, from 4- to 16-Mb products." Toshiba, which spent $425 million in semiconductor R&D from 1983 through 1985, is accelerating its research program this year. "We have budgeted $454.5 million for VLSI research," says president Watari, "and it will go mostly for developing technology in new markets such as semicustom and custom semiconductors."

Researchers last year announced development of an excimer (xenon chloride gas) laser etching process with the potential to meet the required 0.5-μm design rules for 16-Mb chips. Toshiba pushed to the forefront of the world CMOS market with its earlier investments, and it was the first to enter the 1-Mb random-access memory market last year. It currently produces about 300,000 of the 1-Mb chips a month and plans to increase that to 1 million a month by October. Production is aided by the company's earlier development of 5:1 wafer steppers, which allow Toshiba to produce 256-K and 1-Mb products on the same lines.

Another Toshiba research project involves the production of more cost-effective gallium arsenide ingots. It recently announced a new process that the company says should cut the cost of producing GaAs wafers by one-third [*Electronics*, May 19, 1986, p. 9]. Once again, its technological prowess was proved, but it still remains to be seen is how effectively Toshiba can turn this work into products and profits.

Toshiba is accelerating its spending in semiconductor R&D

Other research teams already have had impact in a traditional Toshiba strong suit, consumer electronics. Its inverter system technology has given Toshiba a strong market position in Japan's all-season air-conditioner market. And in the competitive but growing pocket television market, Toshiba this autumn will market a back-lit, 4-in. color model, the largest screen size available. The company also has announced development of a 10-in. liquid-crystal display, also the largest in the market, for computer display use.

Recovering another of its fumbles, Toshiba last year switched its videocasette production to the more popular VHS format, after hanging in with the Beta format (for too long, say most analysts). Nonetheless, the division began making money last year, and the new factory in West Germany is evidence that demand is strong.

The company's most ambitious long-range research of all is in a totally new area—biotechnology. Toshiba will spend about $55 million this year in research directed toward developing biotech processes for use in the production of components for future artificial-intelligence systems. "The most important product for the information age is going to be AI," says planner Mohri, "and we have more ways than any other company to put that knowledge to use. I know we're headed in the right direction; I hope we're moving fast enough." □

TWO YEARS OF DEALS FILL THE NICHES

For the last two years, Toshiba Corp. has been making acquisitions and putting joint ventures together like the missing pieces of a puzzle, with nearly every deal designed to eliminate a Toshiba weak spot.

- To get into the increasingly lucrative custom semiconductor markets, the company tied up with LSI Logic Corp. of Milpitas, Calif., in gate arrays and with Siemens AG in standard cells.
- To shore up its computer and software know-how, it took control of Sord Computer Corp., a Tokyo venture firm with money and marketing problems [*Electronics*, April 7, 1986, p. 48].
- To strengthen its telecommunications business, Toshiba sought and got marketing arrangements with AT&T for its DX-2000 Datakit digital switches, and this month further announced it would market AT&T's System 75 digital private branch exchange in Japan. Toshiba also markets a packet-switching system made by the Belgian affiliate of International Telephone & Telegraph Corp.

The AT&T connection includes Ing. C. Olivetti & Co., of which AT&T has a minority share. Last year, Toshiba acquired a 20% equity in Olivetti Corp. of Japan, for which it has been an original equipment manufacturer of computer peripherals.

- To bolster its presence in the computer-aided-design work station business, Toshiba made another marketing agreement, this one with Sun Microsystems Inc. of Sunnyvale, Calif.

The most tantalizing venture of all, however, didn't come off. Earlier this year, Toshiba and Motorola Corp. reportedly held talks about a possible production and marketing relationship, but there was no agreement. *–M.B.*

SUDDENLY, THE RULES CHANGE FOR EUROPE'S TELECOM BUSINESS

THE ITT-CGE DEAL WILL FORCE SWEEPING REALIGNMENT

by Robert Gallagher

PARIS

The winds of change blowing through the European telecommunications industry are reaching gale force. The recently announced accord on the sale by ITT Corp. of the major interest in its telecommunications and office-automation activities to the French nationalized Compagnie Générale d'Electricité (CGE) may be only the latest in the series of mergers and consolidations that are reshaping the telecommunications landscape. But it promises to dwarf the others and to force sweeping realignment of the players.

French government approval is still required to confirm the deal [*Electronics*, July 10, 1986, p. 42] and there are factions in the government that are fighting it. But both government officials and executives of the nationalized CGE emphasize that the original announcement could not have been made without government sanction, though this means only that the forces favoring the deal have the upper hand for now. Should the accord be blocked for some reason, Canada's Northern Telecom is waiting in the wings to take up negotiations with ITT.

Another complication could be the conservative government's plan to denationalize 65 companies, including CGE. But it is unlikely that many of them will be privatized. For one thing, the socialists of President François Mitterrand are opposed—he says he will not sign nationalization decrees. Also, French capital markets are unlikely to be able to absorb the sale of the companies.

In any event, the stage is set for intense and possibly drawn-out wrangling across Europe as native and foreign makers of telecommunications equipment jockey for position to stake out pieces of the various national markets, particularly in public switching equipment. And in a related development, an accord between CGE and AT&T Co. [*Electronics*, Feb. 17, 1986, p. 16], also awaiting French government approval, is threatened by fallout from the more comprehensive agreement between the French company and ITT.

The trigger for the latest deal is the decision by U. S.-based ITT to cede control of its European telecommunications business. The company's decision may come as a surprise in many quarters, but it can be viewed as the latest, and most spectacular, step in a shakeout that the European telecommunications business has been undergoing since digital switching systems began replacing electromechanical switches.

The shakeout began as early as 1980, when Dutch multinational Philips began negotiating to merge its public switching activities with those of a competitor. After talks with several suitors, Philips teamed up with AT&T Co. in the creation of AT&T and Philips Telecommunications BV, a move that marked the exit of Philips from the manufacture of switches.

In 1982, French giant Thomson turned its telecommunications activities over to CGE, where they were merged with the latter's Alcatel subsidiary. And in England, a merger of the switching activities of General Electric Co. Ltd. and Plessey plc has been under discussion for nearly two years. No decision has yet been made, but some rationalization under the umbrella of one or the other of the companies is inevitable.

That ITT is the next casualty comes as a surprise because the company appeared to be one of those with the critical mass of market share necessary to succeed in the world of public telecommunications.

But the giant conglomerate's back appears to have been broken by its troubles with the System 12 digital exchange. Software problems put deliveries of the switch far behind in nearly every market being served by ITT's four principal European subsidiaries [*Electronics*, February 15, 1986, p. 15]. The result was a fall in profits which, added to the monumental development costs for the highly advanced switch, became a drain on the parent company. As if troubles overseas weren't enough, ITT threw in the towel on adapting System 12 for the U. S. market after spending a hefty $1 billion on the effort [*Electronics*, Feb. 24, 1986, p. 29].

The deal hammered out by ITT president Rand Araskog and CGE chief executive officer Georges Pébereau would create a joint venture bringing together the European subsidiaries of ITT and Alcatel, CGE's principal subsidiary. ITT would receive $1.5 billion in cash, and the joint venture would assume $350 million in debt.

The resulting $4.2 billion company

ARASKOG: ITT's president would give up control of the company's European telecom business.

PÉBEREAU: CGE's chief executive would run the second biggest telecom company in the world.

would be controlled 30% by ITT and 70% by a new European consortium. CGE would take a controlling interest in the consortium, ranging between 51% and 60%. The rest would be held by other European partners. Belgian and Spanish interests have already signed up for 10% shares, and CGE is recruiting others.

At first glance, the joint venture would have impressive credentials: with total sales of some $9.6 billion, it would be second only to AT&T and would control some 35% of the European telecommunications market (chart, p. 114). It would boast production facilities in some 16 countries and commercial operations in 75 countries.

But it will take more than impressive credentials for the new French-run company to solve two fundamental problems. The first is whether CGE will be able to achieve the goal that has escaped ITT: getting System 12 operating to the satisfaction of customers. Should the French firm have the same bad luck as ITT, its attempt at becoming the world's No. 2 telecommunications gear manufacturer could well turn into a costly nightmare.

TWO VIEWPOINTS. Industry observers are divided into two groups. There are those who figure that if ITT were close to fixing System 12's glitches, it would never have decided to sell its telecom activities. The others feel that System 12's problems can be resolved and its market share saved.

"It looks to me like ITT is just trying to bail out before it's too late," asserts one European telecommunications executive. "Look at it this way. You have a company which has spent a ten-figure amount on the development of a digital telephone exchange; and just at the time when you're supposed to be getting your problems ironed out, you sell the business to a competitor so that he can reap the profits. That scenario just doesn't make sense."

Other observers think that it was business prospects, not the System 12's problems, that fueled ITT's move. "ITT is in the process of divesting a lot of its holdings, and this is just another example," argues one executive close to the CGE-ITT negotiations. "They can expect to make a return on investment of no more than 5% on their European telecommunications activities. While that could look pretty good for a European company, U. S. firms are under pressure to do a lot better than that.

"Araskog has no choice but to beef up his bottom line, and getting rid of European telecommunications is a very efficient way of doing that," the executive reasons. "Just look at what happened to ITT stock when the deal with CGE was announced." The company's shares on the New York Stock Exchange shot up nearly 10% on the day of the announcement.

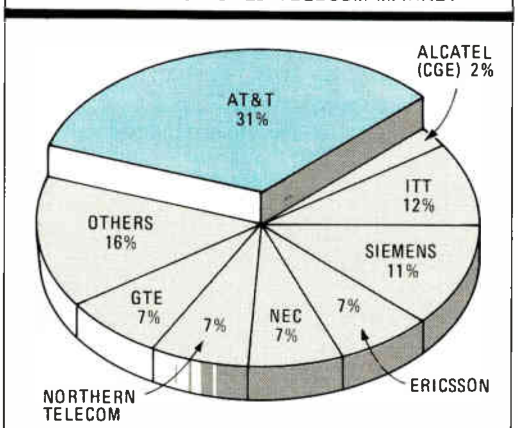
CGE executives, moreover, are confident that System 12 can be put into shape. They are reported to have sent some of their own engineers to evaluate the switch that is in operation at ITT's laboratories, and they are convinced that the question now is simply how long it will take to get the exchange operating properly, rather than whether or not it will ever meet its specifications. They admit, however, that two years ago the situation looked so bleak that they would have balked at making the same kind of deal.

CGE executives believe System 12 can be shaped up

Even if System 12 does finally measure up to expectations, the new joint venture will have another hurdle to clear in keeping its market share. Putting ITT's interests under French control is a signal to competitors that they should be jockeying for position to grab a piece of the System 12's business.

CGE has tried to preempt any such attempt in Belgium and Spain, two of the major European markets where ITT supplies System 12. It is recruiting Telefonica SA, the company that operates the national telephone network in Spain, and Société Générale de Belgique, an influential Belgian banking group, as shareholders in the new joint venture. But maintaining market share in the more important Italian and West German markets will be far more difficult.

AT&T DOMINATES WORLD TELECOM MARKET



SOURCE: NORTHERN BUSINESS INFORMATION

In Italy, the telephone company already uses three suppliers: national flagship Italtel SpA; Fatme SpA, a subsidiary of Sweden's L M Ericsson AB; and ITT subsidiary Face Standard SpA. There is general agreement that three suppliers are one too many, and Italtel chief executive officer Marisa Bellisario has been lobbying for years to get her company's 50% share of the market increased significantly. That would put Italtel on equal footing with the national suppliers in other European countries. So the company is sure to use the passing of Face Standard to French control as ammunition.

In West Germany, Siemens AG, a company that entered the digital switching business late, feels that it has some catching up to do in serving its domestic digital exchange business. It is sure to try to influence the Bundespost to increase its share of the German digital market at the expense of ITT subsidiary Standard Elektrik Lorenz AG.

That Siemens is looking at the CGE-ITT accord as an opportunity is clear from overtures it is making to the French government. Shortly after the two companies made their announcement, Siemens announced that it wants to take control of the Compagnie Générale des Constructions Téléphoniques. CGCT, the now nationalized former ITT subsidiary, holds 16% of the French market with MT-20 and MT-25 switches produced under license from CGE. According to government officials, Siemens is arguing that it deserves a piece of the French market if the French are to control a substantial piece of the German business.

LOOKING AT CGCT. Siemens is not alone in thinking that CGCT is a good target. Both Ericsson and Northern Telecom are also negotiating with the French for the right to serve the CGCT's portion of the French market. They would accomplish this by buying an interest in the French company, which would then produce the purchasing company's switch under license. The fact that they think CGCT is up for grabs is a sign that a complex deal among CGCT, CGE, the French government, and AT&T is in jeopardy. Under the terms of the deal, AT&T would have taken an interest in CGCT, which would discard its MT switches for AT&T's 5ESS-PRX system. In return, AT&T would have placed a $200 million order with CGE's Alcatel subsidiary for microwave transmission gear and would have helped Alcatel introduce its E-10 switch on the U. S. market.

CGE executives vigorously deny that there is any conflict between the two agreements. But they do admit that if the ITT deal goes through, they would redirect their strategy from attacking the U. S. switching market—previously a top priority—in favor of concentrating on European and third-world markets. That redirection would inevitably devalue the AT&T accord for CGE and could cause it to fall through the cracks. □

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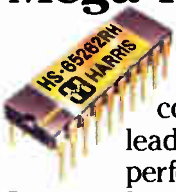

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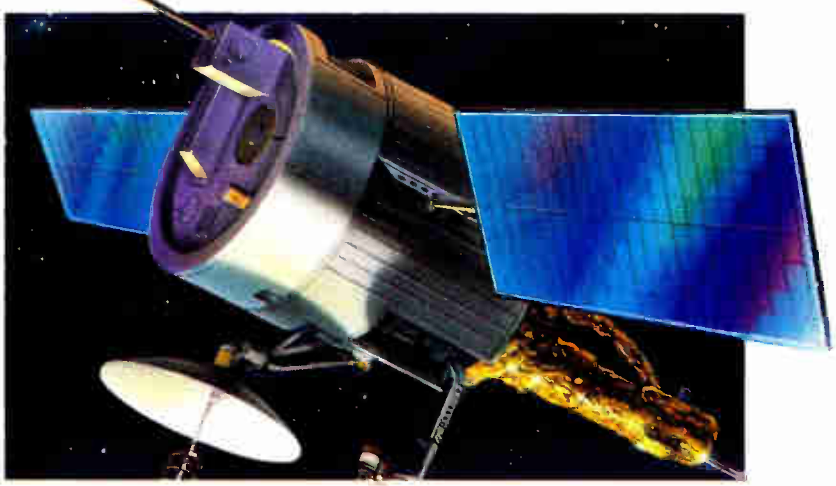

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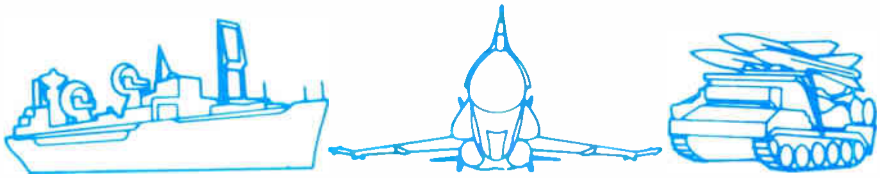

MILITARY ELECTRONICS

SPECIAL ADVERTISING SECTION

A MIDDLING TWO YEARS, THEN A SURGE IN THE MARKET

U. S. production of military electronics will be up only slightly this year. But at $50 billion, it's still a very big target. Among the Pentagon's better-funded projects are the Strategic Defense Initiative, the Very High Speed Integrated Circuits program, Defense Advanced Research Program Agency efforts, and the more mundane office-technology projects spread out among the various military agencies.

A noticeable change could be coming in the way the military does business with the electronics industry, as it begins to look more seriously at increasing competition, prototyping weapons before they're actually purchased, and buying more hardware and software off the shelf.

As part of its effort to improve efficiency, hold down costs, and still meet its office technology needs, the Department of Defense has also begun to work more closely with systems integrators, who will operate as prime contractors—working with multiple vendors to merge hardware, software, and communications.

The Pentagon is continuing to emphasize security in its computer and data-communications acquisitions, has expanded its requirement for data-encryption devices, and, along with the National Security Agency, has developed a series of programs to help industry vendors meet its needs in these areas.

Military electronics suppliers are arming themselves for a variety of high-technology development and major weapons-system programs. Though projections for defense electronics spending are essentially flat this year and next, there's a continuing emphasis on highly sophisticated systems and weapons program upgrades.

U. S. production of military electronics equipment will grow 8%, to $49.6 billion, in 1986, which is only slightly better than half last year's 15.7% rate, according to Henderson Ventures, Los Gatos, Calif. The market research and consulting company attributes the decline to cutbacks in several programs, brought about by Congress as well as by the dramatic downturn in the international arms market in the wake of lower OPEC oil revenue. Henderson sees production of military electronics in 1987 advancing a meager 3.9%, to $51.5 billion.

Some of the bigger projects in terms of spending are the Defense Advanced Research Program Agency (Darpa), the Strategic Defense Initiative (nicknamed Star Wars), and the Very High Speed Integrated Circuits program. Together, they cover a raft of electronic technologies and account for several billion dollars in research and development. Other major targets for R&D dollars are microwave systems and artificial intelligence.

On the comparatively low-tech side, the DOD is becoming a big buyer of microcomputers for its administrative operations.

A surge in connectors

Among other areas that remain strong are power supplies and connectors. The military represents a billion-dollar market for power supplies, mainly for aircraft and communications equipment. And this year, it managed to edge out the computer industry as the top buyer of connectors for the first time.

With the military demanding faster and smarter chips, Darpa has a major program under way to produce gallium arsenide 32-bit reduced-instruction-set computer chip sets. Prototypes should be delivered by mid-1988, but several spinoffs are expected from the program before then. Among them are CMOS chip versions and software, including an Ada compiler and elements of AI programming.

Pentagon spending on GaAs is now in the $5 million range. At least 23 companies are vying for a piece of the program. Darpa's plan is to supply the chips on boards to systems and software contractors that submit winning proposals for use in RISC processors.

Besides a contract, participants in the GaAs program will get a leg up on what should develop into a huge commercial market. A recent Henderson Electronic Market Forecast indicates just how big the GaAs market could become: Henderson estimates that consumption of GaAs products will grow to $5 billion in 1996 from its current $240 million. One of the biggest opportunities for electronic companies remains the Strategic Defense Initiative, with a $2.7 billion budget for fiscal year 1986 and an expected budget of $3.4 billion for fiscal 1987. Much of the program is research, but an increasing portion will be going for actual hardware and software procurement. More than half the funding for Star Wars is directed toward surveillance, tracking and kill assessment, and directed-energy weapons. These categories include signal-processing and infrared technologies, terminal imaging radar, and airborne optical systems.

Another big chunk is designated for kinetic-energy weapons. Part of the remainder is earmarked for computer systems and battle management, the rest for key support technology and management.

However, Congressional cuts in funds for the Star Wars program from next year's budget could delay the government's decision on the feasibility of a space shield by as much as a year, according to a recently released government report. Comparable cuts in 1985 and 1986 have already forced program managers to drop some of their projects.

In addition, the Soviet Union is asking for a total ban on all antimissile research as part of the Geneva arms talks. As a result, the fate of ongoing Star Wars research and development may be tied to international negotiations.

VHSIC production

The DOD's 10-year VHSIC program is going strong and shows no signs of slowing. Program participants are ready to begin producing 1.25-μm ICs, with expectations that they will be able to begin volume production by the end of this year. These Phase 1 VHSIC chips already have been designed into several DOD systems.

Like the GaAs program, the VHSIC project should have many commercial applications. Six contractors have pilot programs under way using Phase 1 chips, and the DOD has set aside approximately $200 million to encourage systems designers to incorporate VHSIC technology into military hardware. Another $75 million

Miltope wins contracts for printer, Winchester drive, and bubble memory

Miltope Corp.'s use of state-of-the-art technology in military and other ruggedized products is paying off. Both its RDS-1500 series of militarized 5¼-in. Winchester disk drives and its TP-3000 thermal printer will become part of the message-processing system aboard the Air Force's E4-B Advanced Airborne Command Post. To date, the Melville, N. Y., manufacturer has delivered over 2,500 Winchester disk systems to the government.

In addition, the company recently won a contract worth $500,000 from General Electric Co.'s Simulation and Controls Division to supply its MIL-E-16400 bubble memory for the U. S. Navy DDG-51 Patrol Frigate Program. The fully militarized, dual-cartridge-based system will be interfaced to a Navy standard AN/UYK central processor.

Several other of Miltope's militarized products have recently come on the market, among them an IBM PC AT-compatible computer, a cartridge tape drive, and a miniature airborne printer.

The Tiger Rugged 1, a flat-panel PC AT-compatible, is based on Hewlett-Packard's Vectra. It is designed for all-weather field use.

The M480 high-performance cartridge tape drive is both format- and cartridge-compatible with IBM's 3480 system. Miltope has scheduled customer shipments of this device for the first quarter of 1987. A full Mil-Spec version will be available in the second quarter of 1987.

The company's new miniature airborne printer is designed for operation in severe tactical aircraft applications. It measures 5 in. wide by 4 in. high by 7.41 in. deep and offers printouts in two formats: 20 to 24 columns or 32 columns. The printer features a self-contained power supply, a 4-K buffer, and a MIL-STD-1553 interface. It is also nuclear hardened.

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Joe Angleton, assistant laboratory manager for VLSI design at the Missiles System Group, is a primary originator of Hughes gate array efforts.

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Circle 119 on reader service card

New triple-output supplies beef up Abbott's military lines

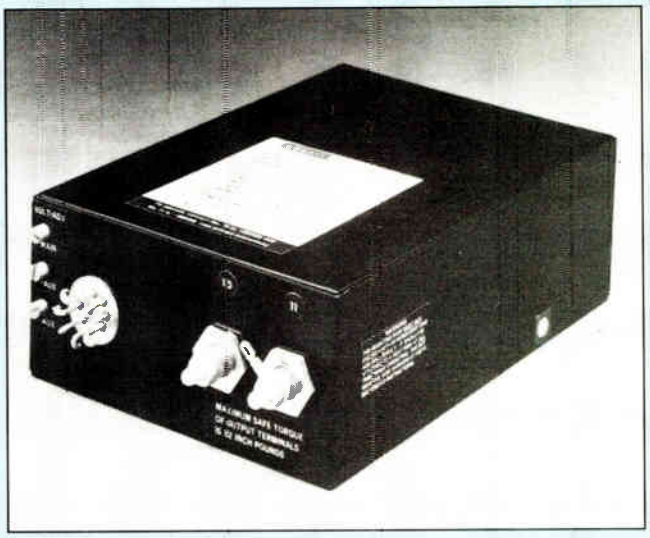
The Power Supply Division of Abbott Transistor Laboratories Inc. is building up its lines of triple-output switching supplies with three new models for the military market. All deliver 5 V ±12 V or 5 V ±15 V and have a ripple and noise rating of 100 mV peak to peak. In addition, they meet a slew of military specifications.

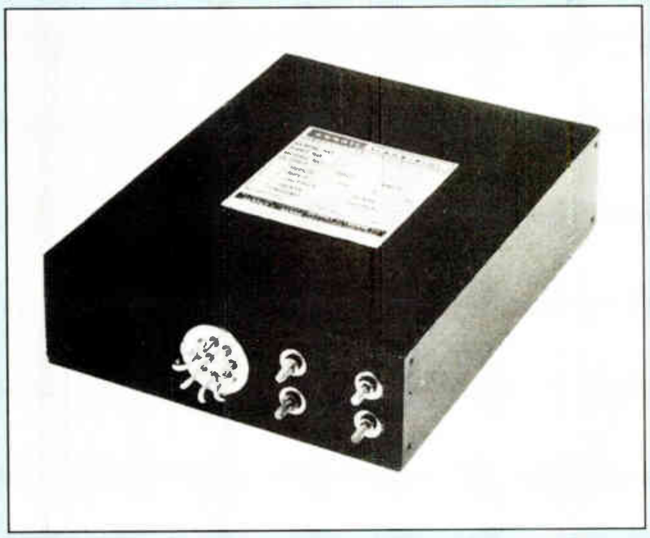
The M300T is designed for use in naval sonar and radar, communications, ground support for airborne systems, and electronic countermeasure equipment. It accepts 115 V ac at 47 to 440 Hz and delivers 300 W with a density of 2.1 W/cubic inch (per Navmat guidelines).

Enclosed in a hermetically sealed package, the M300T measures 3 by 6 by 8 in. and meets the environmental requirements of MIL-STD-810C. Its specifications include line and load regulation of 0.2%, protection from electromagnetic interference (meeting MIL-STD-461B), input protection (meeting MIL-STD-1399), and a hold-up time of 10 ms. Options include special connectors, three-phase input, a wider input-voltage range, and a wider operating-temperature range.

Also new from the Los Angeles company is the BC200, a 200-W dc-dc converter that operates at 100 kHz and accepts an input voltage of 22 to 32 V dc. In addition, it dissipates enough heat to keep junction temperature below 110°C. The supply meets the requirements of MIL-STD-461B for EMI protection; its low-profile, hermetically sealed package measures 1.875 by 5.75 by 8 in.

The third of Abbott's recent introductions is the 100T-series. These switchers come in two versions: the MB100T operates at 47 to 65 Hz; the WM100T operates 320 to 480 Hz. Both models accept 115 V ac and supply 100 W. They also meet EMI requirements for MIL-STD-461B and applicable environmental specifications. The MB100T's input circuit is protected against transients and surges in accordance with MIL-STD-1399, the WM100T's in accordance with MIL-STD-704. Both have a typical mean time between failures of 100,000 hours.





has been earmarked for development of VHSIC design-automation systems. Phase 2, already well under way, calls for the development of 0.5-μm devices and the establishment of a pilot production facility by the fall of 1988.

Surveillance, acquisition, and tracking are among the major program elements in the DOD's R&D budget. Thus the military market for microwave systems and for microwave components should continue to grow, fueled by ongoing requirements to refine airborne, shipboard, and ground-based electronic warfare systems for the three services. Frost & Sullivan, a New York market researcher, puts the total military market for microwave components—both active and passive—at over $3.1 billion in 1988, an increase of 174% from 1982.

Future system requirements will emerge for both electronic warfare and satellite communications applications, on-board guidance for air-launched and other tactical missiles, and the development of ballistic missile defense. The military's activity in ballistic missile defense systems will eventually have a major impact on the microwave components market, Frost & Sullivan says.

Another area of major interest to all military services is AI. Darpa reportedly accounts for 72% of the total U. S. AI market, or approximately $68 million of the $95 million budgeted for AI by the DOD this fiscal year. And these figures do not take into account military funding of AI research and development programs for in-house government labs, government-


AEG

sponsored university research, and other contract work.

Most of the AI funding will go to purchase symbolic processors and software, expert-system development, tools, and training.

Excluding the Darpa and Star Wars programs, the Air Force currently funds about half the military's AI programs, mainly in avionic applications. The Navy's interests in artificial intelligence are confined primarily to mission planning, target acquisition, and combat control. The Army continues to focus much of its AI activities on the development of battle management programs.

The Air Force has also been busy with the recently completed Forecast II, a formal program aimed at identifying emerging technologies and evaluating their impact. Seventy proposals have been selected for implementation by the Air Force Research Laboratories. Among them: the National Aerospace Plane, a military version of the space shuttle that could take on a variety of military missions from earth orbit; a highly automated "super cockpit," which would take over many tasks handled by the pilot; and a study on new concepts in satellite deployment.

Back on the ground, the DOD is making a run on the microcomputer market, and purchases of microcomputers could surpass those of all other computer technologies.

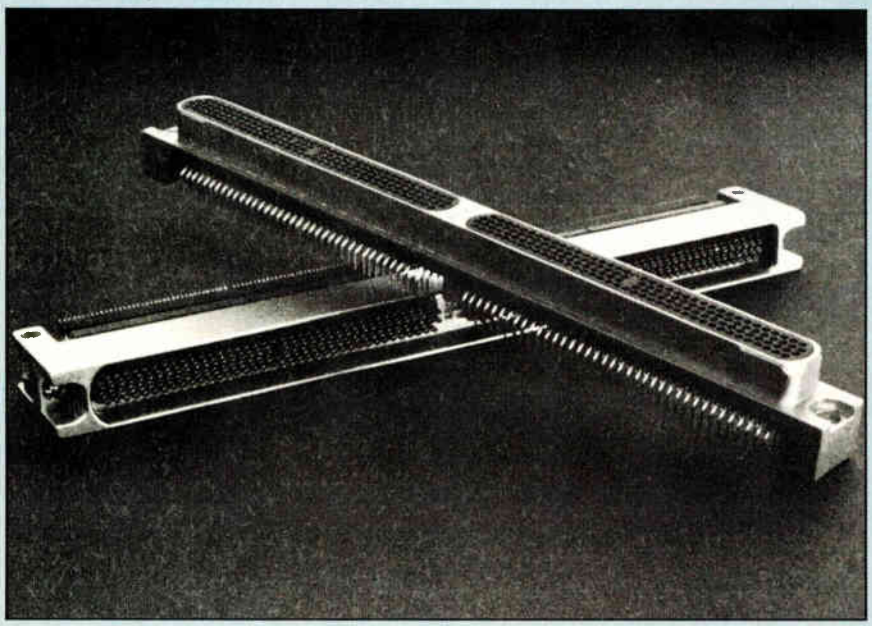
Each service has its special microcomputer requirements. The Air Force is developing a service-wide network of 32-bit work stations. The Army is automating its technical-publishing activities, a program valued in the hundreds of millions of dollars. Also, the DOD hopes to automate all its hospitals.

In virtually every case, computer vendors will work with systems integrators who will operate as prime contractors, merging hardware, software, and communications. Indeed,

High-density connectors are hot items from Microdot companies

Malco and Connector Industries of America, two Microdot Inc. companies, have new connectors ready to go. In response to the military's call for standardized parts, Malco is packaging a line of connectors in high-density standard modules. These HDSM connectors, which the company developed for Texas Instruments Inc., are designed for systems that require increased pin-outs in a smaller board area. Each HDSM connector has up to 304 high-reliability twist-pin contacts placed on 0.05-in. centers in four rows. Board area measures 4.6 by 0.36 in. For increased circuit density, the connectors can be surface mounted on both the daughter and the motherboard.

The South Pasadena, Calif., company now has high-density D connectors in its MCK and MCD lines that meet the requirements of MIL-C-83513. These devices, whose pins exhibit an engaging force of 4 oz typical and 5 oz maximum, are designed for use in miniaturized airborne and space electronics, computers and test equipment.



Several lines from Connector Industries of America are winning places on the Qualified Products List. One of them is the MIL-C-81703 series 1 hermetic receptacles. Designated the D series, these quick-disconnect push-pull couplers utilize a piece of vitreous glass for sealing; they have a flat fluorosilicone seal for positive mating.

The Cincinnati, Ohio, company has also completed qualification testing on the MIL-C-38999 series 3 hermetic connectors and expects them to be on the QPL by midsummer. Thanks to their high-density insertion designs, these connectors have twice the number of contacts than devices with similar shell sizes. They are scoop proof and have a quick-disconnect triple-start thread to maintain electrical continuity between mating shells prior to pin and socket engagement and during disconnection. The plug shells have grounding fingers for shielding from electromagnetic radiation and radio-frequency interference.

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Efficiency	60% minimum
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Line regulation	0.2% or 25 mV
Load regulation	0.2% or 25 mV
EMI	Meets MIL-STD-461B**
Environment	Meets MIL-STD-810C, MIL-S-901C
Input protection	Per MIL-STD-1399
Operating temperature range	0°C to +71°C
Storage temperature range	−55°C to +85°C
MTBF* (Ground benign)	60,000 Hrs.
ER option	134,228 Hrs.
MTBF* (Naval sheltered)	11,000 Hrs.
ER option	28,000 Hrs

*MIL-HDBK-217D (50°C baseplate temp.)
**Refer to spec sheet for applicable levels.

Circle 123 on reader service card

Thin LCDs, color CRTs join AEG's Mil-Spec lines

Advanced-technology displays for military equipment, automobile dashboards, information systems, and measuring instruments are the ticket at AEG Corp. Now available from the Somerville, N. J., company are an extremely thin, lightweight LCD incorporating chip-on-glass technology for military and other rugged applications as well as a color CRT for avionic displays.

Because the LCD's driving circuitry is on the same substrate as the liquid crystal and a pc board is not needed, the LCD is only 3 mm thick. It requires a drive voltage of 5 to 10 V. The twisted-nematic display, which is shock and vibration resistant, operates in the temperature range of −54°C (with a back heater) to +85°C.

Customers can order the LCD as a reflective display for ambient light operation, as a transflective display for ambient or backlight use, or as a transmissive display for rear illumination. The company also offers colored illumination without filters to intensify contrast.

A new addition to AEG's line of CRTs is the M18-E851, a high-brightness avionic display for use in the cockpits of high-performance aircraft. For high resolution, the 5-by-5-in. display has a fine, 0.2-mm-pitch shadow mask and a ruggedized in-line electron gun. It also has a self-converging deflection system, static color purity with convergence correction, and a contrast enhancement filter—all geared to ensure that the display meets military requirements. Display modes include raster scan, stroke write, and hybrid.

with some projects involving up to 20 vendors and 50 or more turnkey systems, the systems integrator's role is growing in military/government computer installations.

Four areas of concern

As part of the acquisition process, the DOD has identified four main areas of concern: computer security, microcomputer acquisition, microcomputer decision-support systems, and project management using microcomputer support.

The military's interest in computer security is reflected in the growing number of microcomputer vendors that are designing their products to meet the guidelines of the Pentagon's Tempest security standard.

The number of products developed under the Defense Department's Tempest security standard guidelines has grown to well over 200. To qualify under the Tempest program, these products are required to eliminate electromagnetic emissions, which may be monitored by unauthorized personnel trying to collect data from agency computers or other electronic equipment.

Several programs are under way to promote the development of secure products and assist vendors in designing data-encryption and related systems. At the same time, each defense agency has formed its own security team to deal with new issues and technologies as they evolve.

Given all the programs the DOD funds and the vast sums in its budget, it recently set up a separate program to help it control costs. And it expects to save about $500 million a year through this program, which will change the way in which semiconductors for the military's electronic systems are purchased.

Standard numbers

Scheduled to be in place by Oct. 1, the program calls for the Defense Electronics Supply Center to assign a standard number to every semiconductor used in electronic military hardware. According to the

Continued on page 128

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A Division of Amstar Technical Products Company, Inc

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Circle 125 on reader service card

Amp puts emphasis on EMP protection

There is no military specification yet for electromagnetic phenomenon, but Amp Inc. is developing a line of EMP-protected connectors that meets the current needs of military original-equipment manufacturers. The Harrisburg, Pa., company is putting considerable effort into reaching the production stage with products that are protected from an extremely large pulse of energy, such as that created by a nuclear explosion.

For now, Amp's EMP research and development effort is focused primarily on the Air Force's Milstar military satellite program. The company is also pursuing EMP programs for the Navy and Army, which have begun to develop their own requirements.

Connectors that Amp developed for an EMP environment are already being designed into several military programs, according to a company representative.

"The desire is to develop a standard, but the government hasn't reached that stage yet," he says. "There are still some compromises," with OEMs essentially dictating system requirements as a standard begins to evolve.

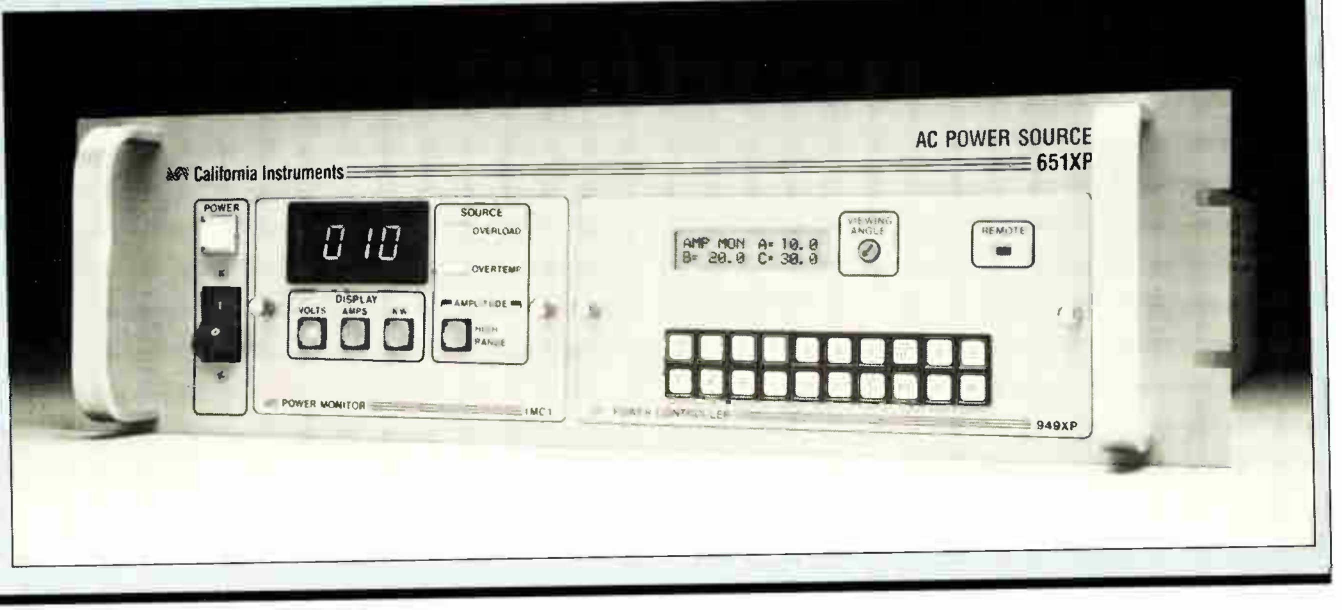
California Instruments offers MATE-certified power sources

California Instruments believes it has a jump on other power-source suppliers now that the Air Force has stipulated Modular Automatic Test Equipment (MATE) as the standard acquisition system for defining, acquiring, and supporting automatic test equipment. The San Diego, Calif., company, a division of Amstar Technical Products Co., is already manufacturing ac power sources with MATE certification, and its XP series is the ac power system in Sperry Corp.'s A10 ATE program for the Air Force, says Leonard G. Roberts, marketing manager.

"In addition to being able to control all the ac power parameters, the XP series also provides the user with complete power-monitoring capabilities," says Roberts. "A MATE version of the XP series is being evaluated in a number of Air Force programs."

The modular series consists of three main components: rack-mountable power amplifiers with front-panel cutouts, controllers, and monitors. Any of the modules can be used with any of the power amplifiers, so the power source can be structured to suit such specialized applications as dc power-supply testing and evaluation, avionic and robotic testing, and gyro testing. The series can also be used as a bench ac supply and as a burn-in power source. Over 60 different configurations are possible.

Features of the XP series include a General Purpose Interface Bus for transmission of actual measured values of volts, amperes, watts, and power factors; reduced panel height and high power density; programmable voltage range change; automatic remote calibration; and an integral elapsed time display.



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AMP Interconnecting ideas

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Senate Armed Services Committee, approximately 40% of the semiconductors purchased for the military are procured using so-called source/specification control drawings. Under the new system, contractors will produce these drawings only if militarized versions of the required semiconductors have not already been developed.

Recent studies indicate that once the new semiconductor buying method is adopted, only one out of eight of the source/specification control drawings now produced will be required.

The Defense Electronics Supply Center will also be responsible for the acquisition of new data-processing equipment. Pentagon officials expect the new procedure to greatly reduce paperwork and time.

Additional changes are likely as the result of a 113-page report recently completed by President Reagan's Blue Ribbon Commission on Defense Management, headed by David Packard, a former deputy secretary of defense and chairman of Hewlett-Packard Co.

Among the panel's recommendations is that contractors develop and test prototypes of weapons systems before the Defense Department makes any commitments to purchase. In addition, the Packard commission has called for increased competition for military contracts, a reduction in the number of people that are involved in selecting contractors, and a general reorganization in the management of the military's procurement system.

According to the commission, if its key recommendations are adopted, the time that it takes to develop and field

Harris's rad-hard CMOS meets military needs

Harris Semiconductor Corp.'s Custom Integrated Circuits Division can claim more than two decades of experience in the development of radiation-hardened products. The Melbourne, Fla., division recently began to ship samples of a library of semicustom and custom rad-hard CMOS ICs, including gate arrays and standard cells. Like the company's other rad-hard products, these ICs are all latchup free and able to withstand a total dose of 1×10^5 rad (Si). Now the company is about to release several more rad-hard products, among them the HS-65262RH, a 16-K-by-1-bit rad-hard asynchronous CMOS static RAM.

The HS-65262RH is designed primarily for satellite systems where high speed and low power consumption are a must. It has a typical access time of less than 100 ns and, thanks to its static configuration, consumes a minimum of power under all conditions. In addition, the circuit is TTL compatible and comes with three-state outputs.

By the end of this year, the Custom Integrated Circuits Division expects to begin shipping samples of several other rad-hard ICs, including a CMOS programmable interval timer (HS-82C54RH), 512-K-by-8-bit and 2-K-by-8-bit CMOS PROMS (HS-6641RH and HS-6616RH), and a 2-K-by-8-bit asynchronous CMOS memory (HS-65162RH). It is also readying samples of a 16-bit CMOS microprocessor, the HS-80C86RH, for shipment in the third quarter of the year. The rad-hard device, which is compatible with the Intel 8086, operates at 0 to 5 MHz off a 5-V power supply. It provides 1 megabyte of direct addressing capability. Samples of the HS-80C85RH, an 8-bit microprocessor compatible with the Intel 8085, are available now.

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RDS1720	172 Mbytes	5¼″	172 to 688 Mbytes
RDS1600	160 Mbytes	8″	160 to 320 Mbytes
RDS2340	234 Mbytes	8″	234 to 468 Mbytes
RDS3500	350 Mbytes	8″	350 to 700 Mbytes

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weapons would be halved. This process now requires approximately 15 years, on average.

Much of the Packard study has been published in a series of interim reports, and Congress has already begun to clear the way for the adoption into law of some of its provisions. The Reagan administration supports most of the commission's proposals. ■

IMC brings out line of vaneaxial cooling fans

IMC Magnetics Corp. has been producing military products—including blowers and thermal products for ground and airborne communication systems, radar systems, transponders, electronic countermeasure equipment, and aircraft landing systems—since it was established in 1951. Its motors and fans have been used to cool computer and other electronic equipment on every U. S. space flight since the Mercury program.

IMC Magnetics' Eastern Division, Westbury, N. Y., supplies the cooling fan for the AN/UGC-136AX, a Tempest-qualified military teleprinter approved by the Navy for shipboard use. Another, even smaller fan is used in the digital radar warning system designed for several military helicopters.

The new big seller in the military line from IMC Magnetics' Eastern Division is a series of vaneaxial cooling systems designed primarily for cooling tracked vehicles, inflatable shelters, and other applications requiring a large volume of air. Ranging from 17 to 24 in. in diameter, these vaneaxials deliver air at a rate of 10,000 to 15,000 CFM. Air delivery curves are plotted using static pressure in inches of water versus airflow in cubic feet per minute.

In addition to the Eastern Division, which supplies mostly blowers and fans and produces most of IMC Magnetics' military products, the company's Florida Division in Miami Lakes supplies power supplies; its New Hampshire Division in Rochester is a major manufacturer of tubeaxial fans; and its Thermal Products Group in Jericho, N. Y., makes heat dissipators. Another subsidiary, Universal Magnetics Corp. in Chatsworth, Calif., produces dc motors and motor/encoders.

Datum finds new applications for time and frequency monitor

On-site time and frequency reference that is precise enough to use for calibration and synchronization has become a necessity for many installations involved in deep-space tracking, communications, navigation, and electronic intelligence. And Datum Inc.'s 9390 GPS time and frequency monitor is designed to provide a time transfer accuracy better than ± 100 ns of the coordinated universal time scale and a frequency resolution to 5×10^{-12}. To do this, it uses code transmissions from satellites in the Navstar Global Positioning System.

Completely self-contained except for a separate antenna and preamplifier assembly, the 9390 can be mounted in a standard 19-in. rack. A 16-button keyboard controls operating modes and data entry. The two-line alphanumeric display provides activity messages, menu choices, and the results of measurements and computations. A printer or a remote-control device can be hooked up through the system's RS-232 port.

The Global Positioning System is a satellite-based radio navigation and positioning system under development by the Department of Defense. Scheduled for completion in 1988, the system will contain 21 orbiting satellites equipped to provide continuous velocity, timing, and three-dimensional positioning information on a global basis. For the time being, five or six satellites are providing several hours per day of worldwide coverage, depending on the receiver's position.

Besides the Defense Department, such U. S. government agencies as the Federal Aviation Agency and NATO as well as a number of commercial customers are using the 9390, says Don Mitchell, range systems manager at the Anaheim, Calif., company. Calibration laboratories, both governmental and commercial, have developed several applications for the 9390, he says. In addition, survey organizations are using the device to develop positioning data, and several large data-communications agencies and companies are using it as a time and frequency source.

FOR MORE INFORMATION

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Continued on page 134

IMC VANEAXIAL FANS

Three IMC vaneaxial fans are at work in the Army's M109A2, 155 MM self-propelled howitzer, ventilating the crew's compartment, cooling the radiator and supporting the air cleaner system. IMC airmovers hold a prominent place in cooling military ordnance. For best results, let the IMC engineering staff solve your air moving problems.

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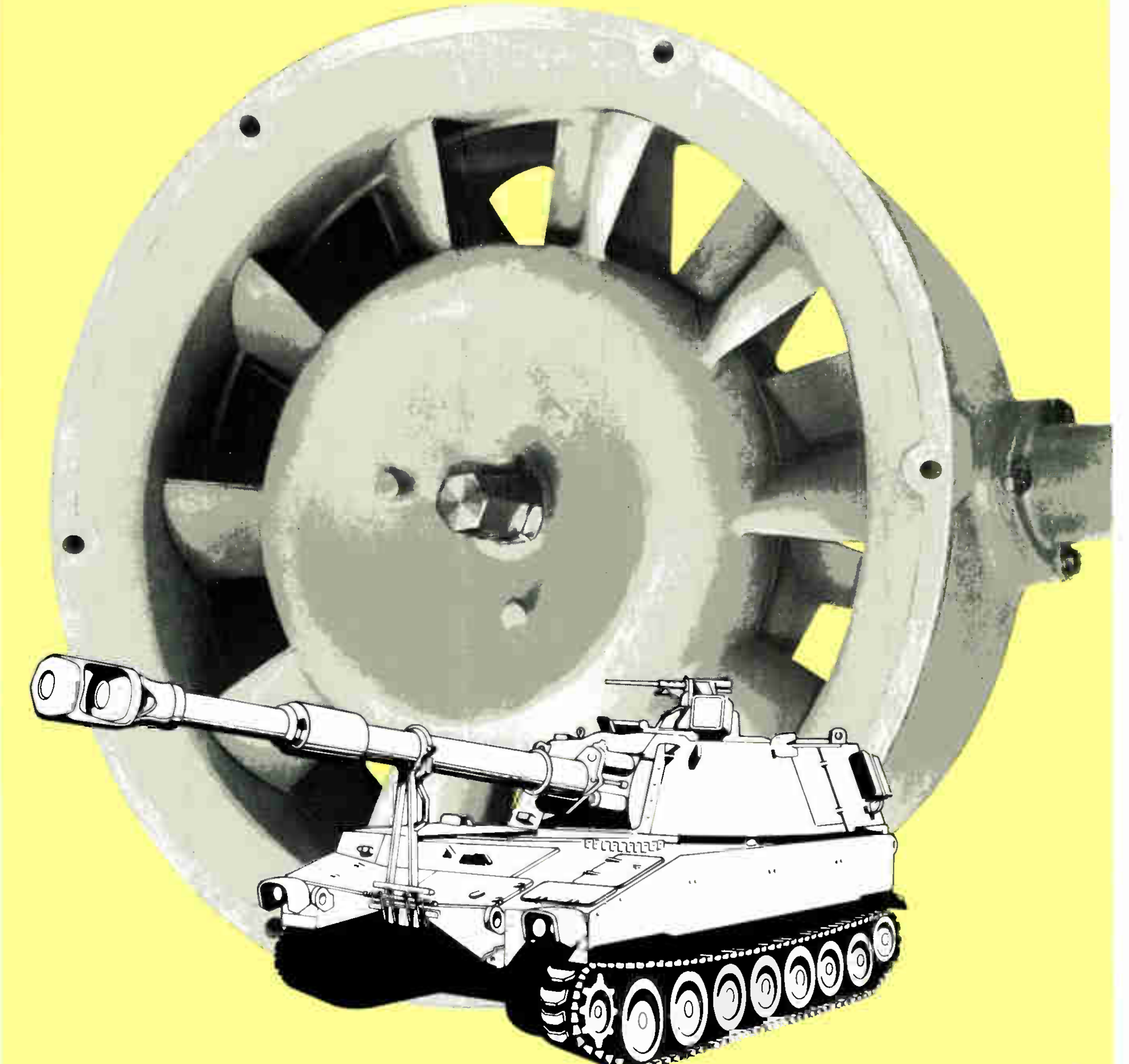

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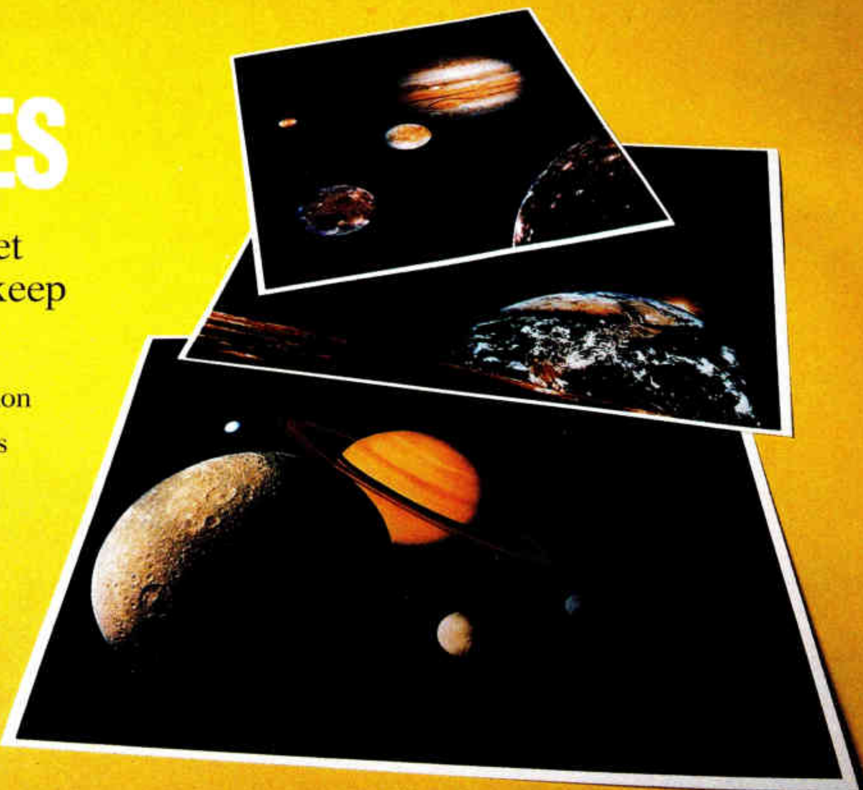


NEW PRODUCTS

WORK STATION BEATS SUPERMINIS IN CONTINUOUS SIMULATIONS

PC AT-BASED SYSTEM ALSO COSTS FAR LESS

Until recently, continuous simulation required superminicomputers with the resultant hefty expenditures. But now Xanalog Corp. has developed a work station, based on a modified IBM Corp. Personal Computer AT, that packs significantly more power for continuous simulation yet costs substantially less than a supermini. And Xanalog's XA-100 is much simpler to use because simulations are programmed graphically, rather than by writing algebraic equations.

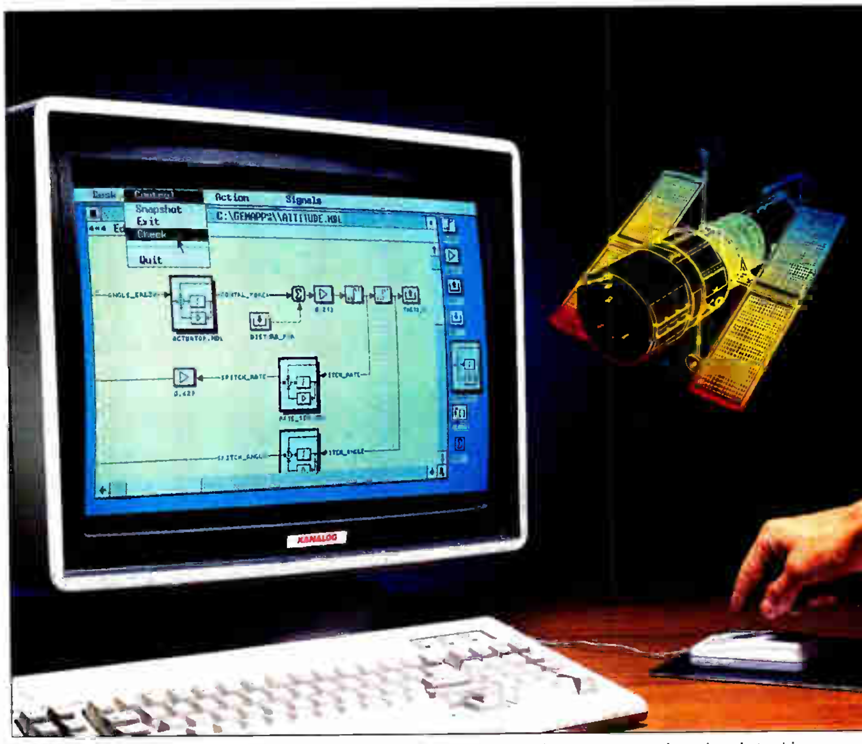
The XA-100 will be unveiled at the Summer Simulation Conference in Reno, Nev., beginning July 27. Designed for satellite-system, aerospace, and other simulation applications, the work station includes a parallel arithmetic unit that relegates the PC AT to functioning only as a task-level supervisor.

SPEEDIER. Xanalog claims the XA-100's computational speed in simulation applications is three to ten times faster than that of the more costly Digital Equipment Corp. VAX-11/780. But XA-100 systems will be priced beginning at just $60,000. Key to this performance level, says Martin Schrage, a cofounder of Xanalog, is the system's software.

The XA-100 allows a user to enter a model graphically by creating a simulation block-diagram model from icons presented on the unit's color screen. The icons represent standard simulation operations such as integration, summation, multiplication, and table lookup. A full range of transcendental and logical functions is also available.

The system comes with a mouse, used for overall control of symbol positioning and pull-down menus. This allows the flow of the simulation and algorithms to be established with purely graphical interactions. By contrast, other simulation software requires the user to program in a continuous simulation language using typed-in algebra and English. The result with the XA-100 system is that block diagram of the model and the simulation program are the same.

The system's block-diagram editor has an error-checking function. Detected errors are flagged in color and continue to flash until the user corrects them. Through use of a hierarchical structure, the XA-100 simulation block diagrams can contain icons representing submodels, which can themselves contain submodels. And a library of submodels can be built up and shared among members of a department.



DYNAMIC SIMULATION. Dynamic systems such as satellites can now be simulated inexpensively with a PC AT-based system. Users write programs by creating block diagrams.

The compiler at the heart of the system is largely responsible for the computational speed, which Xanalog claims is anywhere from 50 to 100 times that of an unmodified PC AT running off-the-shelf simulation software. The compiler developed for the XA-100 does complex scheduling and partitions tasks among the two processors. It is designed for the relatively short vectors and open code with little looping found in continuous-simulation programs.

The compiler has a graphic language analyzer that uses the block diagrams to do simulation checking not possible with algebraic languages. The analyzer accepts the user's block diagrams and from them generates the same intermediate language as would a Fortran compiler. The compiler also checks feedback paths for sources of instability and alerts the programmer by highlighting problem areas on screen.

Most of the software development work for the XA-100 was done at a facility in Reading, England. The software effort was led by Damian McArdle, a Xanalog founder and also a founder and director of Systems Software Factors, a scientific-software house in the UK.

The boards that beef up the PC AT are a 24-bit integer processor and a 32-bit floating-point processor, each with its own programming memory and capable of accessing up to 32 megabytes of data. The parallel processor is tightly coupled to the PC AT and shares memory with it, avoiding the delays introduced by direct-memory access transfers.

In total, the additional processors provide the capability of executing 6 million floating-point operations/s in parallel with 6 million integer instructions/s. Memory for storing programs can be up to 32-K words, sufficient to contain 5,000 lines of compiled Fortran code. The 5,000 lines can be executed in 5.12 ms, Xanalog says.

The additional hardware will be made for Xanalog by Fast Firmware Technologies Ltd., Southampton, UK. Initially, the XA-100 will be offered with a 640-by-350-pixel color graphics monitor. Later, the company says an optional 1,024-by-768-pixel display will be available. Delivery is scheduled to begin sometime in October. *–Craig D. Rose*

Xanalog Corp., 215 Salem St., Woburn, Mass. 01801. Phone (617) 938-8722 [Circle reader service number 380]

LOGIC ANALYZER LEAVES PREDECESSOR IN THE DUST

ASICs TOO. One version of Tektronix' DAS 9200 helps design and test ASICs.

Tektronix, the company that pioneered modular logic-analysis systems, is coming out with a second-generation system that far outperforms its predecessor and moves into new application areas as well. In addition, the DAS 9200 Digital Analysis System can be expanded in three ways, whereas the DAS 9100 could be expanded only one way.

Depending on how the user configures the DAS 9200 mainframe with plug-in cards, it can acquire up to 540 channels at 20 MHz with 32-K-deep memory, 432 channels at 200 MHz with 4-K-deep memory, 160 channels at 2 GHz with 8-K memory, and up to 1,008 stimulus channels at 50 MHz with 8-K memory. By comparison, the 9100 system has a maximum of 104 acquisition channels with synchronous acquisition to 330 MHz and asynchronous acquisition to 660 MHz.

MULTITASKING. In addition to the plug-in cards, the 9200 can be expanded by adding up to three additional mainframes for a total of 28 instrument slots. The third way to expand the system is through software, because it runs under a multitasking operating system. The only expansion mode for the 9100 was plug-in cards. Unlike the 9100, which has its own screen and keyboard, the 9200 requires a dedicated terminal.

The system's speed and flexibility permit engineers to do things with the 9200 that they never could before with a logic analyzer. For example, the 500-ps sampling resolution is fast enough to observe critical timing problems such as metastable states, spurious clock signals, race conditions, and propagation delays that today's logic analyzers with 2-ns resolution cannot capture.

Also, with today's analyzers a user has to trade off speed for increased channel count when doing state analysis. This makes it difficult to debug fast, microcoded state machines. But one configuration of the 9200 requires no tradeoff, allowing 5-ns speed across the full channel width, which can range from 16 to 96 channels.

The 9200 addresses microprocessor and software analysis and debugging, system integration, high-speed state and timing analysis, functional verification of application-specific IC prototypes, board function test, and general-purpose logic analysis applications.

A variety of instrument modules that offer several choices in sample and stimulus rates, memory depth, and channel width can be combined with special-purpose software packages to create a large number of possible system configurations. And the manufacturer is using an open architecture in the system so that it—and users—can tailor software to better suit specific applications.

A 68010-based system controller that comes with 2 megabytes of RAM and runs under a multitasking operating system provides the computing resources for the DAS 9200. Also housed in the mainframe are two disk drives: a 10-megabyte hard-disk drive, used for storage of standard software, set-up information, acquired data, and user files; and a 360-K-byte floppy-disk drive, used to load application software onto and back up the hard disk.

A 156-line high-speed application bus transfers information within and between instrument modules. Bus lines are capable of 250-MHz event transfers, 1-ns edge speeds, and 800-ps propagation delays.

Interactions and combinations of instrument modules within the 9200 system can be redefined through the user interfaces. Software-controlled interactions among modules allow the user to quickly isolate complex problems in both hardware and software.

LINKABLE MODULES. Unlike the 9100, modules in the 9200 can be linked to trigger one another. Module interactions include time correlation, real-time state machine interactions, and acquisition/pattern-generation interactivity. Cluster configuration of modules, even those residing in expansion mainframes, is possible under the system's control software.

Currently, Tektronix has three plug-in acquisition instrument cards, one add-on digitizing module, and two pattern generation modules for the 9200. The 92A16 acquisition card is 16 channels wide. With a 4-K-word memory, it is capable of 200-MHz acquisition speeds in both synchronous and asynchronous modes. Glitch-storage speeds of 100 MHz are possible, with a 2-K memory. The card is designed for medium-speed hardware analysis and high-speed state analysis. Multiple cards can be combined into a module of 96 channels at full speed or 432 channels at lesser speeds.

Designed primarily for microprocessor support and software performance analysis, the 92A60 and 92A90 acquisition modules provide 60 and 90 channels, respectively, with 32-K bits of memory behind each channel. The modules can be clocked at up to 40 MHz, and they can acquire data at rates up to 20 MHz. The 92A60 is for 8- and 16-bit processors and the 92A90 is for 32-bit processors. In maximum configuration, the 92A60 and 92A90 can be combined for up to 540 channels.

As an example of the module interaction, several 92A60s and 92A90s can be precisely time-correlated with each other using a time-stand feature. They also can be correlated with the 92A16 to provide time-aligned displays of any type of activity in the system being measured.

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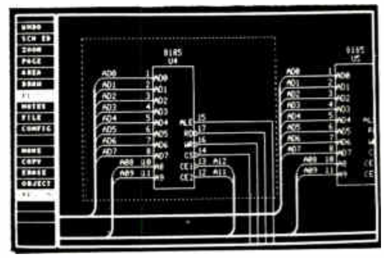

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For really high-speed hardware analysis and high-resolution timing analysis, the 92HS8, a stand-alone unit that plugs into the mainframe, is capable of 2-GHz asynchronous sampling for 500-ps resolution and 1.5-ns glitch detection and capture. The 92SH8 can be combined to deliver 32 channels with 8-K memory using only two card slots and up to 160 channels per system-wide configuration.

For pattern generation, Tektronix has a 50-MHz 18-channel card that generates vectors sequentially or algorithmically. The 92S16 can be used alone or in conjunction with up to seven 92S32 cards, yielding up to 270 channels. Memory depth is 1-K words on each channel. The 50-MHz 36-channel 92S32 can put out stored patterns sequentially, or it can be controlled by a 92S16. Memory on the 92S32 is 8-K per channel.

The DAS 9200 can be custom configured by combining individual cards, or customers can select from many preconfigured systems. The basic system, including the terminal, sells for $11,425.

The price for a general-purpose unit, working with 8- and 16-bit microprocessors, that has 200-MHz timing and 50-MHz pattern generation is $38,450. A system containing 256 stimulus and 256 acquisition channels costs $150,000. Delivery takes from four to 16 weeks after ordering. *–Steve Zollo*

Tektronix Inc., P. O. Box 500, Beaverton, Ore. 97077.
Phone (503) 644-0161 [Circle 381]

PROGRAMMER SUITS ALL LOGIC TYPES

The explosive growth in the number of field-programmable logic types is putting device programmers to the test. Now, Data I/O Corp. has a flexible and easy-to-use universal device programmer that readily handles the challenge.

Sophisticated pin-driver electronics enable the UniSite 40 to program all available programmable parts, including PROMs, EPROMs, EEPROMs, and EEPROM-based programmable logic devices, programmable logic arrays, programmable-array logic, integrated fuse logic, and programmable microcontrollers. Unlike competing universal programmers, the UniSite 40 requires no special hardware adapter for each device type.

TWELVEFOLD GROWTH. The number of programmable device types has mushroomed from about 100 in 1973 to more than 1,200 today. To add further confusion to the situation, they are becoming more complex and are being offered in a variety of new package types. And there is no standard pin-out configuration for pin-grid arrays yet.

"The UniSite 40 grew out of the rapidly changing programmable-device market," says Leo Nikora, marketing manager for Data I/O's Design Automation Division. "Flexibility and ease of use are important since designers do not spend a lot of time in front of a programmer."

A single socket module supports all devices in 40-pin DIPs, and a single module for surface-mountable packages includes six sockets for 20-, 28-, 32-, 44-, 52-, and 68-pin plastic leaded and leadless chip carriers. A small-outline IC socket supports 20-, 22-, 24-, and 28-pin parts.

To support a specific device, the UniSite 40 reassigns pin functions as required. A built-in functional test feature ensures that each pin driver operates properly.

NO FUSS. Users of Data I/O's universal programmer don't have to keep special device adapters in stock.

Pin-driver electronics is key to the system's flexibility. The software-intensive system maps the device-specific functions—for example, the manufacturer's pin assignments—to the universal pin-driver electronics.

"We've incorporated some very sophisticated technology into our pin-driver card, making full use of two semicustom application-specific ICs, a 16-bit microprocessor, high-speed RAM, and a large number of surface-mount devices that help put universal device support into a compact package," says Nikora.

SMART PORT. The UniSite 40's SmartPort, a self-configuring serial interface, reduces the need for special cabling to connect it to the host computer. The programmer can be linked between the host computer and a terminal, so that it has access to the design files. Data rates are selectable from 300 to 19,200 bits/s. The instrument also runs with personal computers operating in the terminal-emulation mode.

Algorithm updates for new parts are loaded from a 3½-in. floppy disk, so designers can quickly begin using new types of devices as they come to market. The disk also provides an alternative for quickly downloading data files from the remote host.

To make the system easy to use for both experienced and novice users, Data I/O chose to use a spreadsheet-like user interface. Users can have their choice of walking through prompting menus or zooming directly to the desired operation. In the latter case, the user selects the command's first letter as well as special commands, such as macros, to tailor the programming process. For example, parameters for 10 devices can be saved for instant recall at the touch of a single keystroke. Pricing for the UniSite 40 starts at $11,000. Delivery takes six weeks. *–Steve Zollo*

Data I/O Corp., 10525 Willows Rd. N. E., Redmond, Wash. 98073.
Phone (206) 881-6444 [Circle 382]

STD-BUS CARD PAVES PATH TO IEEE-488

The STD-488-2 is an STD-bus card that provides an interface to the IEEE-488 instrument bus. The board supports complete IEEE-488 talker, listener, and controller functions. An on-board direct-memory-access controller offloads the task of transferring data along the IEEE-488 bus from the main CPU.

Applications for the STD-488-2 include test-instrument clusters, automatic test-system control, and data collection and storage. Its capabilities include normal or DMA transfers at data rates of up to 1 megabyte/s; Z80 mode 2 interrupt generation; and three on-board counter-timers. Options are an I/O cable for a standard IEEE-488 connector, assembly-language and Forth software drivers, and a remote-address-switch cable.

Priced at $645 Canadian, the STD-bus board will be shipped in six to eight weeks' time.

Seimac Ltd., 1378 Bedford Hwy., Bedford, Nova Scotia, Canada B4A 1E2.
Phone (902) 835-9686 [Circle 369]

CPU CARDS ARE THREE TIMES FASTER THAN PC AT

ADVANCED COMPUTER SOLUTIONS BOOSTS SPEED BY ADDING 12-MHz PROCESSORS AND 100-NS DYNAMIC RAMs

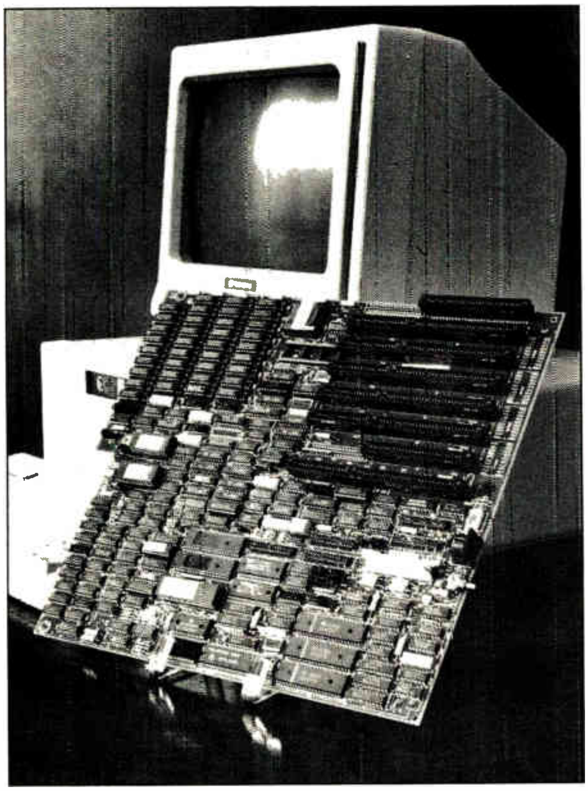
A series of fast motherboards compatible with the 16-bit CPU of IBM Corp.'s Personal Computer AT offers a choice of 80286 microprocessors clocked at 10 or 12 MHz, compared with the 8-MHz clock driving the fastest PC AT. The motherboards, from Advanced Computer Solutions International Inc., carry up to 4 megabytes of RAM on a pc board fitting the AT form factor.

The combination of the fast processors and 100-ns dynamic RAMs gives the ET 286 Plus motherboards processing speeds two to three times that of standard ATs, says president Om P. Singla. The boards represent a classic example of a small systems house aiming to outdo IBM's PCs. "Hindsight is better, since you can incorporate the most recent technology. And being small, we can afford to be more aggressive" about using the latest advances, says Singla.

MEGABIT DRAMs. The ET 286 Plus has sockets that accommodate either 256-K or 1-Mb DRAMs. The board is an eight-layer unit with heavy ground and power lines to help ensure high signal-to-noise protection, Singla says.

The company has engineered the motherboard to compensate for slower plug-in peripheral cards not designed for bus speeds of 10 and 12 MHz. Extra wait states can be used to resolve differences between the fast CPU and slower memories on expansion cards.

To use newly available 12-MHz 286s, the company designed a set of proprietary peripheral components, which include a clock generator and a high-speed bus controller. These devices, plus an optional 80287 floating-point math coprocessor, reside on a piggyback daughter card attached to the 12-MHz motherboard. The 10-MHz board uses standard peripheral chips.



DOUBLE UP. The ET 286 Plus CPU board can carry a daughterboard with an 80287 coprocessor and fast peripherals.

The 12-MHz board is forced to generate one wait-state cycle when accessing memory, even with the relatively fast 100-ns DRAM chips. When the 10-MHz CPU board is loaded with 100-ns DRAMs, however, it can run without wait states. The manufacturer also sells a 10-MHz board stocked with 150-ns DRAMs; it also runs with one wait state. All three configurations are available with either 1 megabyte of DRAM, using 256-K chips, or 4 megabytes, with 1-Mb n-MOS parts from Toshiba Corp. Both RAM sizes are available in 100- and 150-ns versions.

The 12-MHz board with 1 megabyte of DRAM sells for $1,045 each in 500- to 1,000-piece quantities. The 10-MHz zero-wait-state system, with 1 megabyte of memory, sells for $945 each in quantities of more than 500 pieces. Expanding memory to 4 megabytes adds $2,000 per board. The 10-MHz one-wait-state board sells for $795 with 1 megabyte and $2,595 with 4 megabytes. The 80287 coprocessor is an additional $450. All versions are available now.

Each ET 286 Plus motherboard features standard AT-compatible I/O ports, system bus, keyboard interface, and slots for eight expansion cards. Systems integrators can use the boards to complete the assembly of a fully functional AT-compatible computer for about $1,500 to $1,600, Singla says. *–J. Robert Lineback*

ACS International Inc., 2105 Luna Rd., Suite 330, Carrollton, Texas 75006. Phone (214) 247-5151 [Circle reader service number 340]

GRAPHICS CARDS SUIT IBM PC FOR CAD

Systems integrators wishing to turn a member of the IBM Corp. Personal Computer line into a computer-aided design and engineering work station can now boost the machine's graphics resolution with cards from Pronto Computers Inc. The HR-1200 series boasts resolutions up to 1,280 by 1,024 pixels with up to 256 simultaneously displayable colors. IBM's highest resolution card supports 640 by 400 pixels, which is insufficient for CAD systems.

"There is an increasing demand for high-resolution graphics capabilities at the PC-based work-station level," says David Ingstad, vice president of marketing and sales at Pronto Computers. The boards, which have been under development for over a year, have been successfully benchmarked by customers of Computer Sciences Corp.'s Defense Systems Division.

The HR-1200 series of boards provides flicker-free graphics on 60-Hz noninterlaced monitors. In addition to the 256-color 1,280-by-1,024-pixel card, Pronto offers one with the same resolution and just 16 colors, which can be displayed from a palette of 4,096. Two other cards support 1,024-by-768-pixel displays with either 256 or 16 simultaneous colors.

Users can draw such graphics primitives as vectors, rectangles, arcs, circles, ellipses, and polygons at speeds of up to 1.3 million pixels/s. The board also provides commands for area fills, paint, pattern, and direct-memory-access modification at speeds up to 2.6 million pixels/s. Zoom, pan, copy, and color-replacement commands are also supported by the hardware, which employs dual-port video-speed RAM chips to optimize performance.

The high-performance boards include a 256-by-12-bit color lookup table, three high-speed digital-to-analog converters, and a 1.5-megabyte memory for the screen image. The boards also have memory for storing fonts and special characters. They can handle either an 8- or 16-bit data path to maintain compatibility with the full spectrum of IBM PCs and compatible machines.

EYE ON THE FUTURE. Use of the PC in the design, manufacturing, and engineering procedure will show steady and exponential growth over the next decade, Ingstad says, so there will be a demand for products that maximize the performance of engineering systems built around the microcomputer. With the new cards, an engineer or designer can equip his PC-based system with more powerful display terminals and more complex software products. CAD performance will grow to include activities previously performed only on minicomputers and mainframes, the company says.

The graphics engines' performance is credited to the use of a graphics processor from Hitachi Ltd. and DACs from Brooktree Corp. The Hitachi graphics processor contains 38 commands for complete geometric flexibility. This chip provides more functions and speed than any other now available, enabling Pronto to package all functions on a one-card slot, Pronto says.

Graphics software currently supported includes AutoCAD, ComputerVision's Personal Designer Series, Graphics Kernel Systems, Virtual Device Interface, and other popular packages. C-language drivers are also available for customized application development.

The 1,280-by-1,024-pixel version with 256 simultaneous color display costs $3,495 each, and the 1,280-by-1,024-pixel board with 16-color capability sells for $2,795. The 1,024-by-768-pixel card with 256 color capability sells for $2,895, and the 16-color 1,024-by-768 board is $2,195. All are available now. *–Ellie Aguilar*

Pronto Computers Inc., 3730 Skypark Dr., Torrance, Calif. 90505.
Phone (213) 539-6400 [Circle 342]

CARD LETS PC AT EMULATE MILITARY COMPUTERS

An interface card that lets a personal computer emulate expensive tactical computers and peripherals takes a big bite out of development costs for many military projects. Developed by Sabtech Industries, the PC-NTDS (for Navy Tactical Data Systems) plugs into the IBM Corp. Personal Computer, PC/XT, PC AT, and compatible machines.

Called a 32-bit bridge, the board provides full-duplex 32-bit I/O support for parallel communications with 32-bit tactical computers carrying the standard Navy AN/UYK designation. "The board converts the communications protocol of the IBM PC into the protocol of the militarized computer," says Sabtech president Rahim Sabadia. The adapter costs $2,850 for the AT version or $1,600 for the XT-compatible unit. This contrasts favorably with standard military computers, notes Sabadia—they carry tabs of up to $500,000 each.

The product conforms to MIL-STD-1397, which governs NTDS hardware. "The adapter can be set up to operate as an 8-, 16-, or full 32-bit parallel interface and can exceed the transfer rates that are required for the NTDS bus," says Sabadia. The NTDS bus transfers a maximum of 250,000 words/s, each 32 bits wide. Sabtech's board will transfer 3.3 megabytes/s, or about 825,000 such words/s.

The board also carries an RS-422 communications port with outputs that can be set for three-state operation and transmission at 19.2 kb/s. This allows the desktop computer to emulate tactical RS-422-based peripherals.

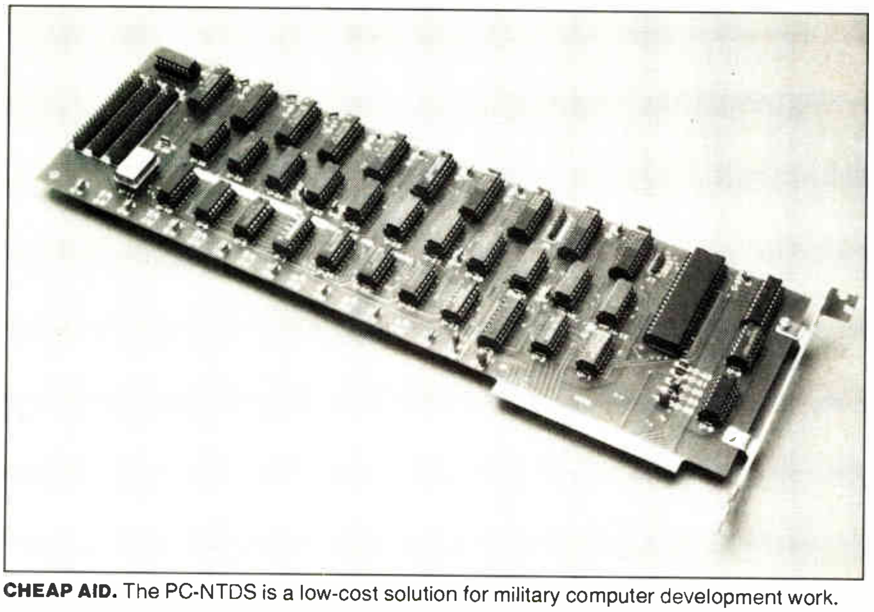
The PC/XT interface card conforms to MIL-STD-1397A, the slower version of the NTDS bus, with optional support for the faster MIL-STD-1397B. The AT-compatible interface supports both standards. Both units perform all types of NTDS transfers—input, output, external function, and external interrupt.

SIMULATION. With the interface installed, a PC can be programmed to simulate an NTDS host computer. Two interface boards can be installed in a single PC to simulate a peripheral device, with one board acting as an output channel and the other as an input channel receiving data from a host.

And because desktop-based development systems do not require temperature-controlled rooms, Sabadia points out, the interface card can be installed in a portable machine such as a Compaq and be carried aboard ships for use as a software-debugging aid.

The Test Message Generator software package provided with each adapter provides a high-level language for controlling the interface. Assembly-language source code for the I/O drivers is included, enabling users to write custom software, as well as diagnostic software and loopback-test cables.

The adapter can also serve as a transparent RS-422-bus analyzer or monitor. The PC can be programmed to inject test stimuli or collect data during execution of tactical software. *–Ellie Aguilar*



CHEAP AID. The PC-NTDS is a low-cost solution for military computer development work.

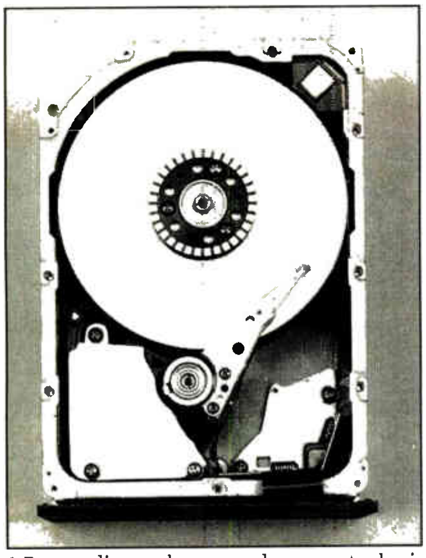
Sabtech Industries, 4091 E. La Palma Ave., Unit P, Anaheim, Calif. 92807.
Phone (714) 630-9335 [Circle 341]

160-MEGABYTE DRIVE HAS SCSI INTERFACE

The Q160, a 160-megabyte (formatted capacity) Winchester disk drive from Quantum Corp., comes with an embedded Small Computer Systems Interface controller. The full-height 5¼-in. Q160's controller is built around a custom disk-drive controller chip.

The Q160 is compatible with the company's earlier 53- and 80-megabyte drives. Therefore, engineers working with the lower-capacity drives can upgrade their systems by simply connecting the Q160 to the SCSI bus.

The drive uses the run-length-limited



1,7 encoding scheme and supports logical block sizes of 512, 1,024, or 2,028 bytes. Data can be transferred at 1.25 megabytes/s. Access time is 30 ms at a maximum and 26 ms typically, including head-settling time.

When available in the fourth quarter, the Q160 will sell for $1,495.

Quantum Corp., 1804 McCarthy Blvd., Milpitas, Calif. 95035.
Phone (408) 262-1100 [Circle 358]

DATA BASE WORKS ON SINGLE PCs OR NETS

A data-base-management system for the IBM Corp. Personal Computer family works either on stand-alone computers or on local-area networks. The R:Base System V enables users to perform ad hoc data management and create programs to automate data-management tasks without having to learn a programming language.

Using R:Base System V's Express System, a software technology that provides access to the data base without programming, users can create customized forms and reports and run applications. Definition Express enables users to create data base structures and to modify existing structures. The Forms Express and Reports Express modules permit the creation of multipage data-entry forms and reports.

The system contains all the software needed for both single-user configurations and multiuser operations on LANs. For example, multiuser features in R:Base System V include automatic row verification to handle simultaneous file accesses and password protection. An unlimited number of work stations can be added without additional cost. The data-base system sells for $700 and is available now.

Microrim, 3925 159th Ave. N. E., P. O. Box 97022, Redmond, Wash. 98073.
Phone (206) 885-2000 [Circle 355]

DRIVE COMES WITH IPI-II INTERFACE

An embedded intelligent peripheral interface (IPI-II) is the boast of the M2333P, the first 8-in. Winchester disk drive to offer this feature, according to the manufacturer. The interface offers 2.5-megabyte/s data streaming, 2-byte parallel data transfers, extended status, and fixed- and variable-block lengths.

Positioning time for the disk drive is 20 ms. The M2333P's disk enclosure measures just 15 by 8½ by 5 in. high. The package houses the disk enclosure and pc boards, including the IPI-II disk drive controller interface.

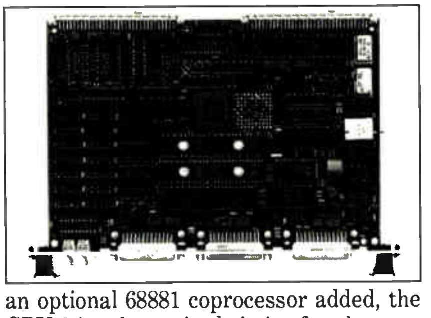
Priced at $4,995 in quantity, the M2333P will be available for evaluation in the third quarter, with production to follow in the fourth quarter.

Fujitsu America Inc., 3055 Orchard Dr., San Jose, Calif. 95134.
Phone (408) 946-8777 [Circle 357]

VMEBUS BOARDS USE NO WAIT STATES

The CPU-6 series of VMEbus boards offers zero-wait-state operation at 8 MHz or one-wait-state operation at 12.5 MHz. There are 512-K bytes of dedicated RAM and four 28-pin EPROM sockets on the single-board subsystem. For multiple interface requirements in process control, three RS-232-C serial ports and one parallel port are also provided.

The price of the board is $1,845. With

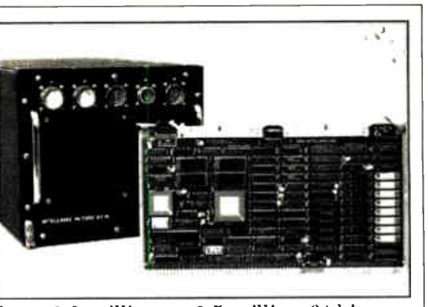


an optional 68881 coprocessor added, the CPU-6 is a low-priced choice for the user who wants to include fast floating-point arithmetic in a test-and-measurement application, the company says. Delivery is from stock.

Force Computers Inc., 727 University Ave., Los Gatos, Calif. 95030.
Phone (408) 354-3410 [Circle 349]

ADA COMPUTER CRUNCHES 2.4 MIPS

A ruggedized Ada multiprocessor computer's processing speed has been tripled by adding a CPU board with a 68020 32-bit processor plus an 68881 floating-point coprocessor. The combination allows the IN/7000 AT/R to process 2.4 million Ada instructions/s or



from 0.3 million to 0.5 million 64-bit-precision floating-point operations/s, the company says.

The CPU board's clock rate is 16.7 MHz with no wait states. It also offers a demand-paged memory-management unit with 12 different resident contexts for multiple processing. The maximum virtual-address space per context is 1 gigabyte.

Also new to the system are a 3-megabyte memory board and a dual-port memory board that can be accessed over either the local or the system bus for enhanced multiprocessor operations. Various combinations of EPROMs and static RAMs can also be configured.

Pricing for an IN/7000 AT/R computer system starts at under $50,000.

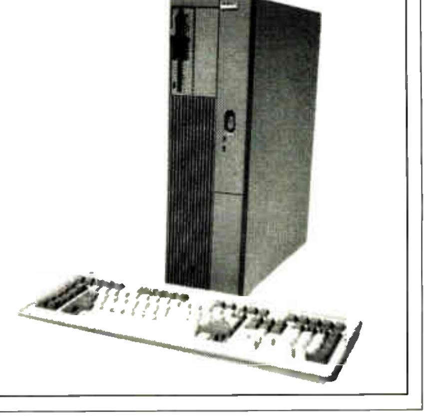
Intellimac Inc., 6001 Montrose Rd., Rockville, Md. 20852.
Phone (301) 984-8000 [Circle 347]

OEM COMPUTER TAKES EIGHT BOARDS

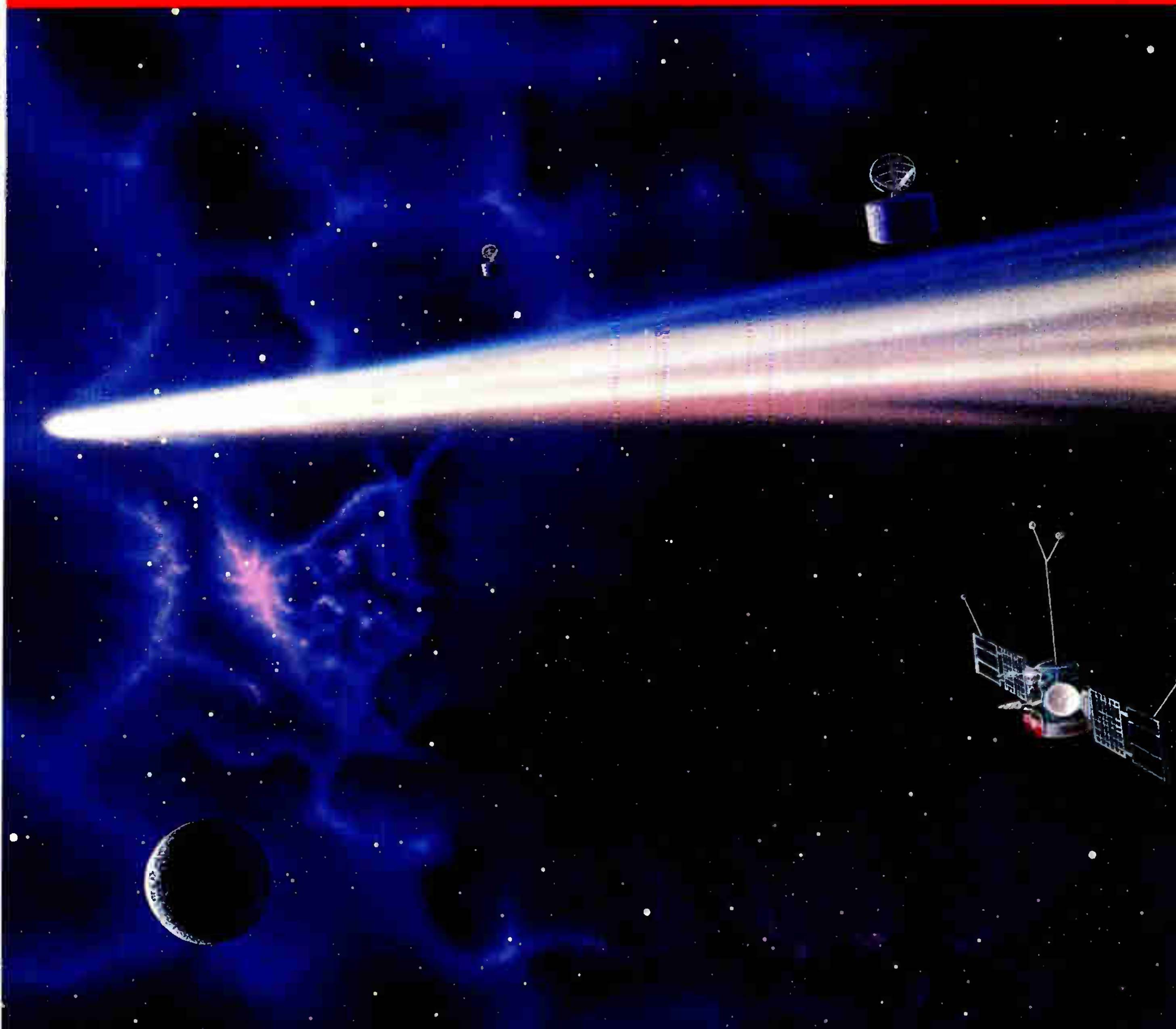
The $2,500 PC8 computer, which is compatible with the IBM Corp. Personal Computer and PC AT, offers eight slots for adding custom features. It is designed for original-equipment manufacturers and value-added resellers who want to build systems using PC-compatible expansion boards and peripherals.

Features include an 80286 processor, MS-DOS, Basic, 512-K bytes of memory expandable to 640-K bytes, a hard-disk drive and two floppies, and keyboard with a number keypad. Systems are available now.

Applied Digital Data Systems Inc., 100 Marcus Blvd., Hauppauge, N. Y. 11788.
Phone (516) 231-5400 [Circle 348]



Pursuing Halley's Comet:



All five satellites on the trail of Halley's Comet rely on RCA High-Rel components.

The world has been waiting 75 years for the magnificent Halley's Comet to reappear and light up the heavens. And this time Earth will send out a welcoming committee.

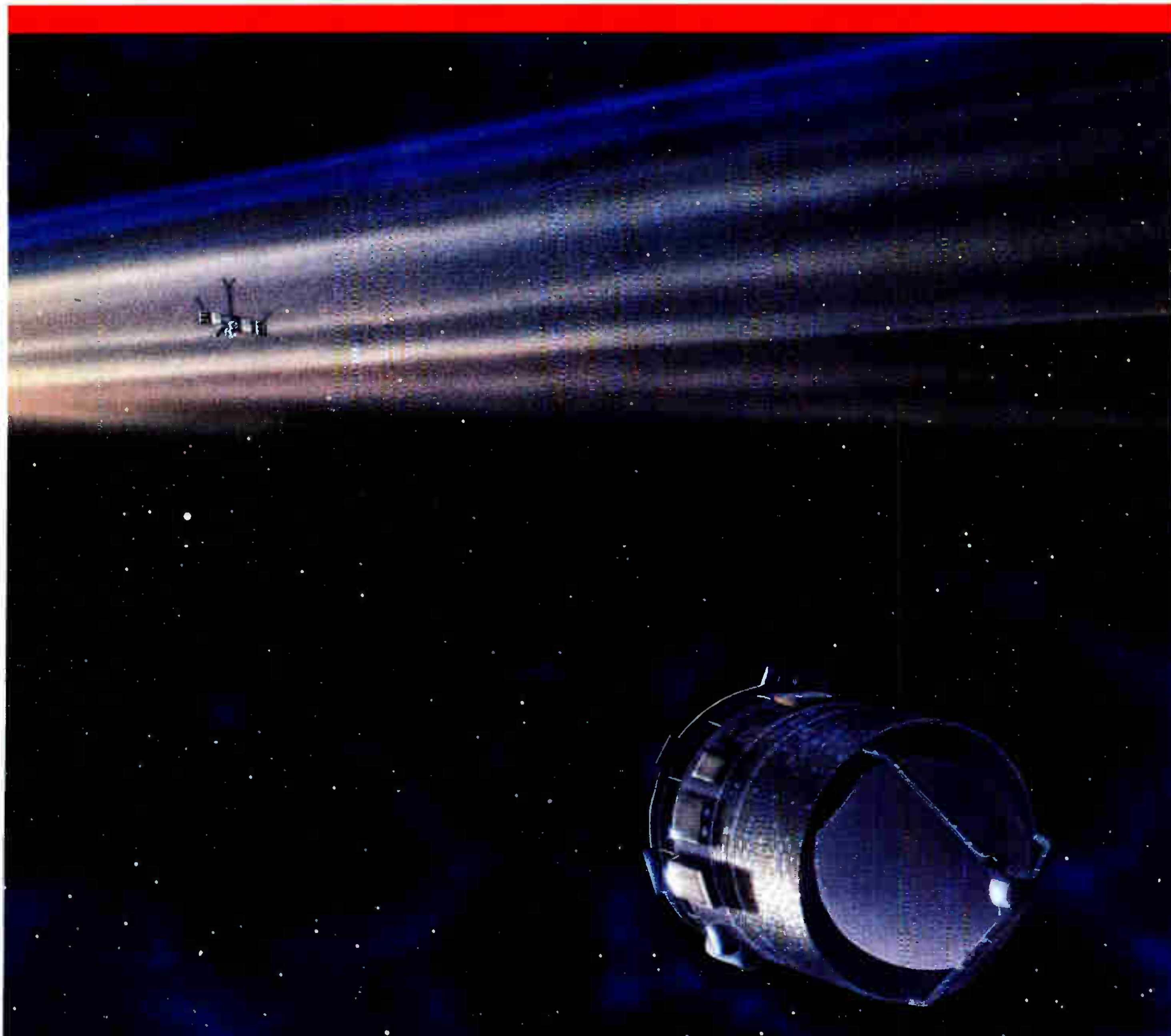
A worldwide effort.

Years ago, governments all over the world agreed to set up a tracking force of five satellites: the European Giotto, Japanese MS-75 and Planet A, and Soviet Vega I and Vega II. Launched into coordinated orbits, they will monitor the path of the comet precisely.

RCA helps make it possible.

All five of these satellites will use High-Rel CMOS devices made by RCA. Devices which

a Mega-chase in space.



have been specially designed to withstand the demands of space travel.

What science hopes to learn:

Scientists will use this data to learn about the origin of Halley's and other comets. They hope to determine the location and nature of the comet's nucleus. On-board instruments will detect particles as small as one-trillionth of a gram. Many scientists believe these particles are samples of matter from the formation of the solar system.

Enjoy the show.

Halley's Comet will appear late in November, 1985, and will be fully visible in late March, 1986, particularly in the southern hemisphere. Don't miss the opportunity to see the splendor...your next chance will be in the year 2060.

If you'd like to know more about our very broad line of High-Rel devices for military, aerospace and scientific designs, contact your RCA sales office or distributor. Or write: RCA Solid State, Box 2900, Somerville, NJ 08876.

Your Mega-partner in High-Rel.

RCA

KEYBOARD PROGRAMS SMART PROCESS MONITOR

MICROPROCESSOR IN ANALOGIC'S CONTROL MASTER LETS USERS KEY IN ALL CALIBRATION, CONFIGURATION

Analogic Corp. is taking the wraps off its Control Master intelligent industrial process monitors and controllers that simplify and expand the capabilities of current offerings. A microprocessor allows all configuration and calibration to be done in software through a front-panel keyboard. Conventional products require hardware programming.

"The significance of this product is that it's all menu-driven, software-driven," says Raymond G. Sansouci, marketing manager for the company's Industrial Products Group. "There are no more analog setpoints, no more hardware. Everything is programmed from the keyboard on the product, making it easier to use and more reliable over time."

The 4½-digit panel meter also has the highest conversion rate available in the industry, Sansouci says. At 20,000 conversions/s, it's 8 to 10 times faster than existing products, he claims. The Control Master uses a 17-bit ADC and thus has a 3:1 resolution ratio of internal

TWO BY TWO. The Control Master accepts two inputs of varying types.

conversion to external display. The display is a vacuum-fluorescent unit with adjustable brightness.

The Control Master series will consist of two products starting at $375 each for a basic configuration, with a range of options forthcoming. The first panel meter, to be available next month, will fit the ⅛ DIN form factor, with the second slated as ¼ DIN size and offering additional capabilities such as more I/O lines.

The initial CM panel meter accepts two input signals at a time. Both primary and secondary inputs can handle signal types including current, frequency, resistance temperature detector, strain gauge, thermistor, thermocouple, and voltage.

Furthermore, the Control Master's standard power supply makes it unnecessary for users to stock both ac- and dc-powered meters. The supply accepts ac power from 80 to 264 V at 47 to 63 Hz or dc from 12 to 48 V.

For controls or alarms, the system has four standard outputs programmed as normally opened or closed. The outputs can be programmed to change state based on one input or on a mathematical combination of the two inputs.

The Control Master comes in a 6-by-2-by-4-in. enclosure and includes a basic single-point serial communications interface. An option allows up to 32 individual Control Masters to be addressed on a multidrop network using RS-422 or RS-485 cabling. The system can also be interfaced to a computer to store and analyze data. *–Debra Michals*

Analogic Corp., 14 Electronics Ave., Danvers, Mass. 01923.
Phone (617) 777-4500 [Circle 460]

SEVEN SENSORS SPEED AUTOMATION

It's easy to build a spanking-new automated factory: it's a matter of starting at the top with the computer and working down to the sensors. But automating existing factories has not been as straightforward. Now, Honeywell's Micro Switch Division has a new strategy and seven new sensor products that should ease that task.

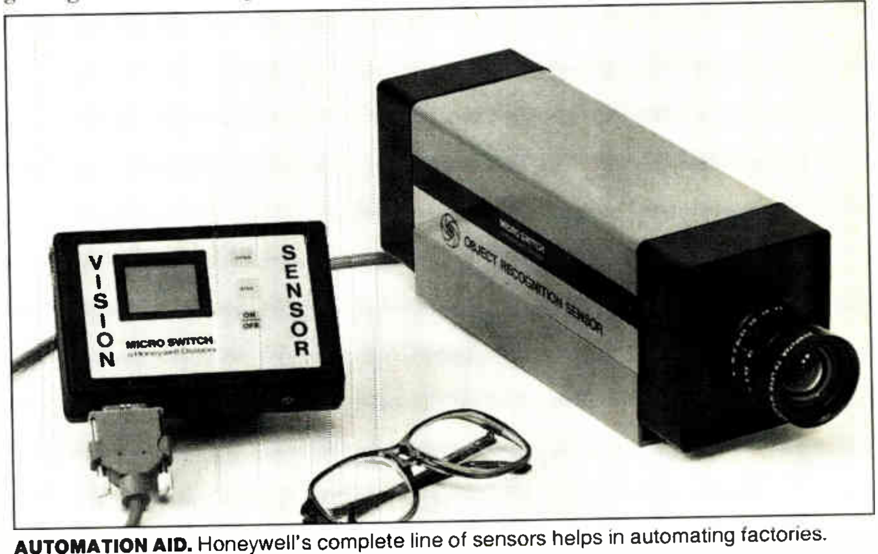
The company's bottom-up approach is based on the belief that many automation efforts will involve manufacturers integrating automation into their existing equipment. At this lowest level of the manufacturing system architecture, the sensor plays a pivotal role.

Honeywell divides sensor requirements into seven functional categories, including presence/absence, positioning, inspection, condition measurement, identification, sensor interface, and man/machine interface. Honeywell has one new product for each category.

By putting sensing and interface needs into functional categories, the user no longer has to know exactly what kind of product he needs, such as a photoelectric control or a pressure sensor. "He needs only to indentify what he wants to do," says Dick Slayton, director of marketing for the Micro Switch Division.

But the company is also looking to sell to companies building completely new factories. "In each case, they can be used just as easily by companies beginning an automation process from the ground up as by companies with sophisticated systems that begin with a supercomputer at the top," says Murray Death, factory-automation products manager at the Micro Switch Division.

The presence/absence sensor Micro Switch has added to its stable is a photoelectric limit switch. The MP series



AUTOMATION AID. Honeywell's complete line of sensors helps in automating factories.

controls are assembled from a modular photoelectric head and a choice of standard plug-in bases. Plug-in logic and replacement lenses are also available. The system can operate in either the retroreflective or the diffuse mode. Scanning distances range from 5 ft for the diffuse head to 22 ft for the retroreflective head. Prices range between $100 and $119, with delivery in eight weeks.

In proximity sensors, which detect the position of any object or material, the company is bringing out a line that employs ultrasonic technology. The 943 and 942 can detect the position of solids, liquids, metals, and substances that are transparent, translucent, or opaque, regardless of color.

ANALOG OR DIGITAL. The 943 is a setpoint version, and the 942 provides a choice between analog and digital outputs. The 943 setpoint sensor has a maximum sensing range of 39 in. without a beam concentrator and up to 47 in. with a concentrator. The range of the 942 is 5.9 to 59 in. Both are available with remote sensors or as integral units.

The 942 ac/dc unit ranges in price from $1,000 to $1,023, and the 943, which is dc only, sells for between $225 and $228. Delivery takes 10 to 12 weeks.

For inspection, the 952 series can be used to detect a part's position, check labels, guide robots, and check the fill level of bottles. The sensors are easy to use and feature a preprogrammed microprocessor. The 952 series can inspect up to 2,000 parts/min. The 952 sensors can detect edge position to within 1%. This is done by sensing a change in brightness or a contrast within the field of view of a pixel array. A choice of outputs is available, including solid-state, analog, RS-232-C, and RS-422. Each station is priced about $2,000.

Micro Switch is adding two new basic current sensors and their holder assemblies for condition measurement. These include a standard industrial output version and an advanced Hall-effect transducer version for applications requiring a higher degree of accuracy.

The standard industrial output versions measure ac or dc current and provide 1- to 5-V or 4- to 20-mA loop linear outputs. Improved null interchangeability and temperature shift characteristics are provided with the advanced linear-output Hall effect transducer current sensors. They can measure either ac or dc current, and sensitivity is adjustable. The current sensor products range from $17.50 to $43.95 with delivery in six to eight weeks.

The 950RS series object-recognition sensor incorporates vision technology in an easy-to-use package. It can analyze four different parts and compare their images with reference images preset in its memory, at line speeds of 600 objects/min. Because the 950RS can detect subtle differences in size, shape, or pattern, it is appropriate for inspection tasks and part identification and orientation. Fourteen part-identification algorithms (such as left edge, right edge, area, and perimeter) are preset in its memory. Scene focusing and illumination algorithms are also factory-programmed to aid in setting the lens focus and aperture.

Menu-driven setup on a hand-held two-key controller simplifies operator training. A complete unit with hand-held programmer, cable, and sensor sells for $5,000.

Micro Switch is using the FactoryLink industrial applications software package from United States Data Corp. to integrate its SID-2000 sensor interface with IBM Corp. Personal Computers. FactoryLink, which is priced between $3,500 and $5,000, turns a PC into a complete operator/management work station when used with real-time monitoring and control equipment such as the Micro Switch SID-2000, which processes the multiple sensor inputs.

A new $49.50 industrial logic and refresh control unit for the company's PDPS programmable display pushbutton strip allows the display to interface with any industrial system, computer, or programmable logic controller. Through the control unit, the host system can be programmed to provide legends and graphics to the user, take appropriate action when one or more of the switches has been activated, and then display a different legend if required. *–Steve Zollo*

Micro Switch, 11 W. Spring St., Freeport, Ill. 61032.
Phone (815) 235-6600 [Circle 461]

MOTOR CONTROLLER HANDLES 12 AXES

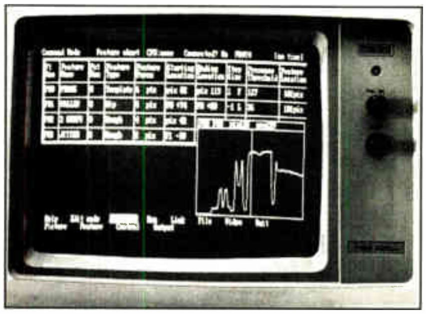
A low-cost programmable stepper motor and machine-site automation controller can run any combination of up to eight axes of linear and up to four axes of circular interpolation, including two simultaneous sequences.

In machine-site and robotic applications, the MAC100 can control such automation-related components as relays, solenoids, and ac motors. An 8031 microprocessor is at the heart of the MAC100, which consists of three STD-bus modules, a stepper-motor driver card, an I/O card, an eight-slot card cage, a power supply, and software. The MAC100 is available now for $2,800 each, with quantity discounts available.

Techno Inc., 2101 Jericho Turnpike, New Hyde Park, N. Y. 11040.
Phone (516) 328-3300 [Circle 465]

MENUS PROGRAM VISION SYSTEMS

A software package from Opcon reduces vision-system programming to a matter of entering a sequence of responses to prompts from a personal computer. Called Pixel Mechanic, the program guides the user through four menu-driven screens that allow him to create the entire sequence of application functions to be performed by the company's Inspector series of vision systems.



The vision system records an image to be used as the benchmark by which the computer compares images. Using this image, the user can tag key visual characteristics of the object and then instruct Pixel Mechanic to record the resulting data as correct for the object. The final program identifies and segregates objects that differ from the benchmark.

Available next month, Pixel Mechanic will sell for $995.

Opcon Inc., 720 80th St. S.W., Everett, Wash. 98203.
Phone (206) 353-0900 [Circle 468]

TIMER/COUNTER DOES 5,000 COUNTS/MIN

The CX200 programmable solid-state timer and counter unit has five time ranges and can count at speeds up to 5,000 counts/min. The time ranges from 19.999 s to 199 h, 59 min. Each of the unit's two count rates will accept and display counts from 1 to 19,999.

Seven miniature rocker switches inside the unit select time or count operation, time range, and standard or reverse start operation. The CX200 line uses memory backed by a 10-year lithium battery and has a keypad lock to prevent unauthorized program changes. The CX200 is available now for $125.

Eagle Signal Controls, 8004 Cameron Rd., Austin, Texas 78753.
Phone (512) 837-8300 [Circle 467]

MAINFRAME SERVER LINKS ETHERNETS TO IBM'S SNA

MITEK CONTROLLER LETS NETWORKED COMPUTERS TAP INTO IBM ENVIRONMENTS WITHOUT CHANGES TO SOFTWARE

Mitek Systems Corp.'s new mainframe network server takes a distributed approach to bridging the differences between Ethernets and the host environment of IBM Corp.'s System Network Architecture.

The Multibus-based M2X30 controller and the software its microprocessor executes handle the most complex portion of protocol conversion between SNA and the Transmission Control Protocol/Internet Protocol that Ethernets use. But the computationally intensive screen-conversion tasks are distributed to Mitek software that runs in each Ethernet TCP/IP work station.

The result is a system that enables Ethernet-attached computers and work stations to tap into the undistributed SNA environment of IBM mainframes without requiring any changes to the SNA or application software residing back at the IBM or IBM-compatible host, explains Cleve V. Graves, technical marketing manager for the company.

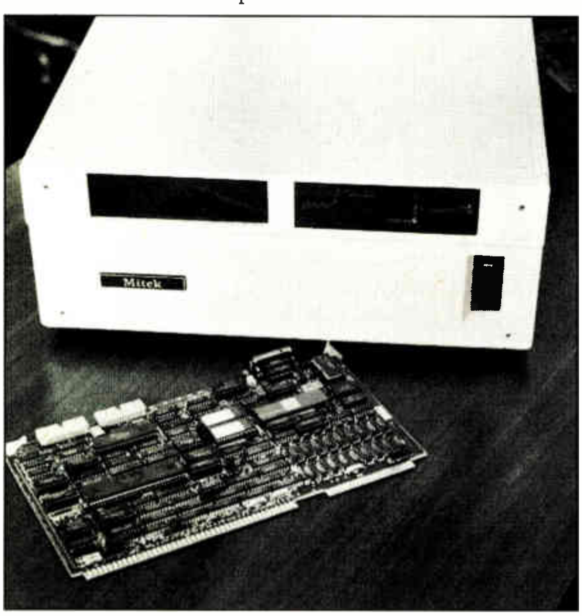
"Companies using IBM mainframes are usually reluctant to change their host environments for the connectivity of local-area networks or non-IBM systems," notes Graves. Mitek's M2X30 SNA Network Servers and presentation services software, which is the software that runs on the networked work stations, combine to provide SNA-to-TCP/IP conversions at the speed of Ethernet.

The M2X30 controller box comes in two versions: the 2030, which contains a 2901 bit-slice-based processor for direct attachment to the high-speed channels of IBM mainframes; and the 2130, for attachment to remote hosts using the Synchronous Data Link Control protocol. The 2030 direct-channel attachment runs at burst rates up to 1.8 megabytes/s. The SDLC remote-mainframe connection runs at up to 64 kb/s over a V.35 link or at 19.2 kb/s using an RS-232-C option.

Mitek's recently introduced controller box, which houses the systems, has six Multibus I card slots [*Electronics*, April 21, 1986, p. 74]. The Multibus-based controller and its software operate at the transport level, implementing the lower five levels of the seven-layer Open Systems Interconnection reference model devised by the International Organization for Standardization.

The top two OSI layers are handled by Mitek's SNA Network Server Presentation Services programs residing inside the networked system, typically a work station running an operating system based on AT&T Co.'s Unix. The SNS/PS software takes about 100-K bytes of the work station's memory.

UNIX PORTABILITY. Presentation services packages have been written in the C language so they can be easily adapted to work stations and computers running Unix. The company is also developing an interface to Microsoft's MS-DOS for personal computers. The SNS presentation services are available in two versions for either SNA 3270 terminal emulation and PC 3270 file transfer or SNA 3770 remote-job-entry emulation.



SHARED WORK. Protocol conversion is divided between the Mitek controller and each work station on the net.

In the IBM mainframe, the final two layers of protocol conversion are routinely handled by the existing virtual-telecommunications-access method, or VTAM, which is the host-access method driving SNA. "Our technology represents a distributed solution in protocol conversion," says Graves. "It is unique in that the most CPU-intensive portion—the conversion to the local screen type—is handled in code distributed across a vast number of computers so there are more compute cycles available. The more complex task of converting layers one through five—which are not as compute-intensive—is centralized in the 68000-based hardware," he explains.

M2X30 systems come in rack-mountable and tabletop configurations. They are powered by 115 V ac or, optionally, 230 V, and operate from 0°C to 70°C. Each unit has a floppy-disk drive for loading the controller's own operating system.

An Ethernet controller card resides on the Multibus. Mitek is outfitting its M2X30 systems with Ethernet controllers from both Excelan Inc., which uses Intel's chip set, and Communication Machinery Corp., which uses Advanced Micro Devices' set.

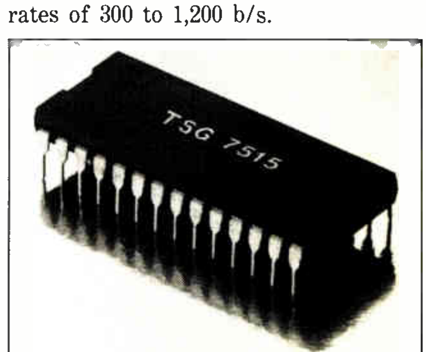
In quantities of one to four, the M2030 channel-attached SNA network server costs $29,500. The M2130 remote-attached server costs $21,000 each in like quantities for the RS-232-C version and $23,500 each for high-speed V.35 configurations. The SNS presentation services software is a licensed software product, costing $4,500 for multiuser versions in quantities of one to five and $750 for single-user systems in lots of fewer than 50. *–J. Robert Lineback*

Mitek Systems Corp., 1303-B March Lane, Carrollton, Texas 75006.
Phone (214) 242-8277 [Circle 440]

MODEM CHIP WORKS IN FULL DUPLEX

A single-chip modem from Mostek transmits and receives data in full-duplex operation while supporting three telephony standards. Depending on how its pins are wired, the TSG7515 CMOS modem can support the Bell 212A, Bell 103, or International Telegraph and Telephone Consultative Committee V22 A-B transmission standards.

The chip will generate and receive both phase-modulated and fm signals. The ability to operate in both signaling methods allows the device to be used in four different modem modes with data rates of 300 to 1,200 b/s.



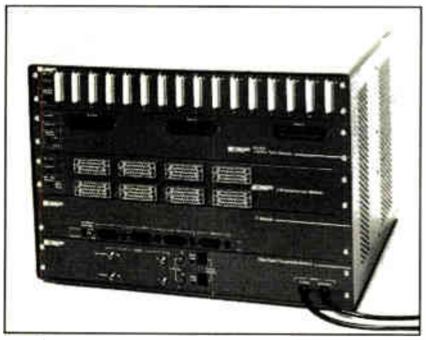
The 7515, which typically consumes 100 mW from a ±5-V power supply, performs phase modulation by differential phase-shift keying. In the frequency-generation mode, on-chip switch capacitor filters are used to reject and demodulate out-of-band noise. The double-polysilicon CMOS modem chip uses a 4.9152-MHz crystal as its internal frequency reference. The 7515 modem sells for $53.80 each in 100-piece quantities.

Thomson Components-Mostek Corp., 1310 Electronics, Carrollton, Texas 75006.
Phone (214) 466-6178 [Circle 445]

MULTIPLEXER USES OPTICAL FIBER

A fiber-optic multiplexer, the model 5510 connects a wide variety of equipment, including minicomputers and data PBXs, to terminal clusters; front-end processors to control units; and PBXs to PBXs or digital microwave radios. The multiplexer can be configured with various I/O modules available with RS-232-C, RS-422, V.35, and T1 interfaces.

All channels are multiplexed into a 28-



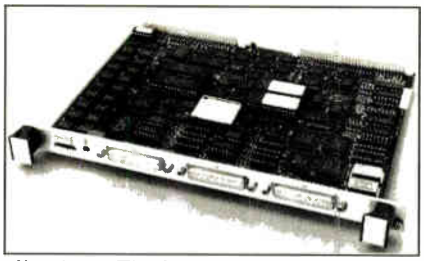
Mb/s aggregate data stream, transmitted over a fiber-optical cable up to distances in excess of 5 km, and finally demultiplexed by a second 5110. The multiplexer comes in a desktop or rack-mountable configuration at prices starting at $3,750. Delivery takes 30 days.

Raycom Systems, 6395 Gunpark Dr., Boulder, Colo. 80301.
Phone (303) 530-1620 [Circle 446]

MULTIPROTOCOL BOARD SUITS VMEBUS

Designers using the VMEbus can equip their systems for communications tasks with the DCP-8820 data-communications processor. It enables the VMEbus computer to operate in a number of popular communications protocols including asynchronous, bisynchronous, Synchronous Data Link Control, High-level Data Link Control, X.25, X.21, and Systems Network Architecture.

The DCP-8820 comes with a real-time multitasking executive and Unix-compatible device drivers to reduce the systems integrators' cost and time in developing custom communication ap-



plications. The board is built around an 8-MHz 80186 processor and includes 512-K bytes of zero-wait-state RAM with parity and 64-K bytes of dual-ported RAM.

In quantities of 100, the DCP-8820 costs $1,680 each. Delivery takes 60 days.

Systech Corp., 6465 Nancy Ridge Dr., San Diego, Calif. 92121.
Phone (619) 453-8970 [Circle 447]

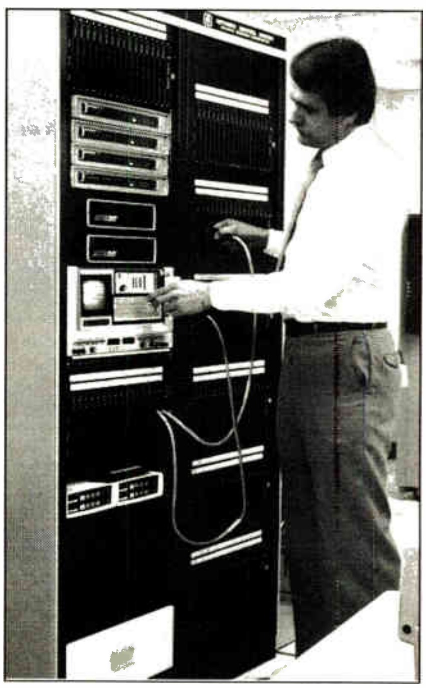
SYSTEM REVIVES FAULTY NETWORKS

The NTS 1000 network restoration and test system speeds fault isolation and service restoration in data-communications networks. The modular system consists of patching, switching, and test equipment.

Audible and visual alarms alert the network operator to a loss of carrier or other selectable digital signal leads. Communication-service restoration is provided by patch, fallback switch, and crossover switch modules.

Pricing varies because each NTS 1000 system is custom configured. The system can be expanded without discarding existing equipment. Delivery takes 30 days after receipt of order.

Atlantic Research Corp., 5390 Cherokee Ave., Alexandria, Va. 22312.
Phone (703) 642-4000 [Circle 448]



MESSAGE ENCRYPTOR MEETS NSA SPECS

The HS3447 Cypher I encryption/decryption device is endorsed by the National Security Agency for applications in which sensitive but unclassified information must be secured. The device is suitable for standard encryption applications or in spread-spectrum communications applications.

The HS3447 is designed to encrypt and decrypt a serial data stream using an NSA-endorsed algorithm. It encrypts a plain-text message using a specified variable to produce ciphered text, which is decrypted at the receiver to produce the original plain text.

The device is suitable for commercial, satellite, mainframe computer systems, banking, and brokerage communications applications. Pricing for the HS3447 is $80 each in lots of 1,000. Production quantities are available now for immediate delivery.

Harris Corp., Semiconductor Sector, P. O. Box 883, Melbourne, Fla. 32901.
Phone (305) 724-7800 [Circle 450]

MODEM HANDLES DATA AND VOICE IN ONE CALL

A 1,200-b/s desktop modem features automatic voice and data switching over the same line during a call. The P212ZX automatic dialing, automatic answering modem is compatible with the Hayes 1,200-b/s Smartmodem as well as with Bell 103 300-b/s standards.

The modem offers full-duplex asynchronous operation over switched telephone networks. It is suited for distributed applications such as electronic mail or access to public information services such as Tymnet and Telenet.

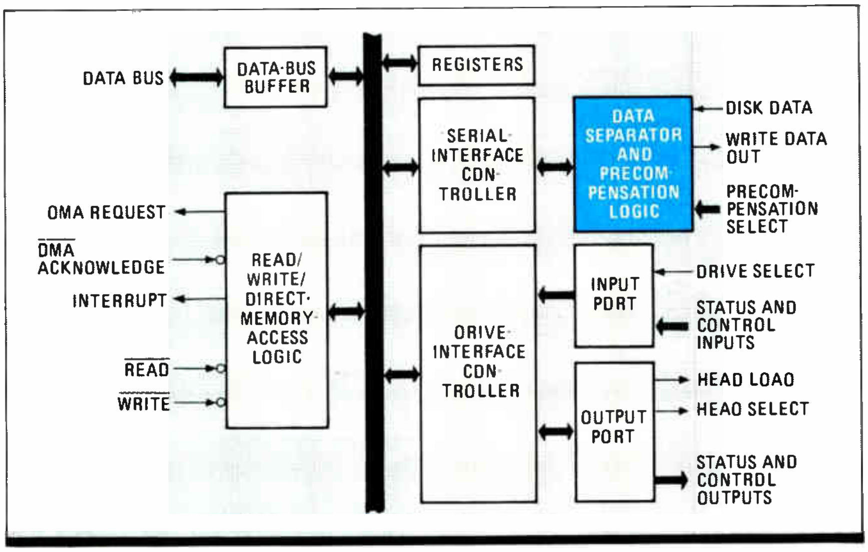
In addition, manual option switches allow the P212ZX to work with smart or dumb terminals. Available now, the modem sells for $325 each.

The company also has a 2,400-b/s version that has the popular Microcom Network Protocol error-correction procedure. It sells for $595 and is also available now for immediate delivery.

Prentice Corp., 266 Caspian Dr., Sunnyvale, Calif. 94088.
Phone (408) 734-9810 [Circle 452]

FLOPPY-DISK CONTROLLER DOES DATA SEPARATION

SMC'S SINGLE CHIP FOR PC AT QUAD-DENSITY DRIVES ALSO HAS PRECOMPENSATION CIRCUITRY



TWO COUNTERS. The FDC9268 uses two counters, one for bit jitter and one for flux events.

Designers of IBM Corp. Personal Computer AT compatibles can get a single-chip solution to building the floppy-disk drive controller. The FDC9268 from Standard Microsystems Corp. incorporates the company's version of NEC Corp.'s 765A, the industry-standard controller IBM uses in the PC AT, as well as functions that IBM does with external circuitry on the AT.

The chip also integrates SMC's FDC-9239 Enhanced Floppy Disk Interface Circuit, which contains circuitry for digital data separation, head-load timing, and write precompensation. The chip enables designers to build the controller on the motherboard rather than on a separate card. With on-chip data separator and precompensation circuitry, the FDC9268 eliminates the need for resistors, capacitors, a voltage-controlled oscillator, and the interface between the separator and the controller.

The chip is for use with AT-compatible 1.2-megabyte quad-density floppy drives, which record 80 tracks/in. of data using modified frequency modulation, but it can also be used with 3½- and 8-in. floppy drives. It also supports single- and double-density drives for 40 tracks/in. of FM and modified FM data, respectively. The chip supports programmable data recording lengths of 128, 256, 512, or 1,024 bytes/sector. Each chip can control up to four drives.

In addition, the company is working on a Small Computer System Interface initiator. This chip will enable disk drive makers to build drives with embedded controllers that can link directly to a computer's SCSI bus.

"IBM does not include digital data separation or precompensation circuitry on the AT's disk-drive controller," says Ronald S. Ethe, marketing manager for rotating memory products. "Yet designers building compatible products using this chip can use sloppy floppies and still get the soft-error rate in their drives to less than 10^{-9}." A 16-bit cell-divide algorithm does the error correction.

There are a number of other benefits, Ethe says. Because of the chip's performance, designers can keep the cost of their systems down by using cheaper drives. The digital data-separation circuitry eliminates the need to tweak every controller on the production line, which saves manufacturing costs. Finally, stocking a single chip reduces inventory costs.

The precompensation circuitry adjusts for variations in spacing between data bits written on the media. These variations result from fluctuating motor speed, called bit jitter, and magnetic flux. The latter spaces 1 and 0 bits closer together or farther apart, especially when there is a continuous stream of the same bit type.

The precompensation circuitry adjusts data writing to ensure that bits are properly spaced and more easily read later. With quad-density drives, the system expects a flux transition every microsecond. Because precompensation helps write data more accurately, reading is accomplished with lower error rates.

Unlike other data separators, the FDC9268 has two registers: one keeps track of bit jitter, the other magnetic-flux events. Standard Microsystems uses a 16-MHz clock frequency rather than a 8-MHz clock of other separators. This increases the window margin and bit-jitter tolerance figures.

The FDC9268's window margin, or the time in which data can be read, is specified at 920 ns for 500-kHz data rate and 1,920 ns for 250 kHz. For bit jitter, the figures are 520 ns for 500-kHz drives and 920 ns for 250-kHz drives.

Samples will be available in the middle of next month, with production-quantity shipments beginning in October. In lots of 25, each chip is priced at less than $20. *–Steve Zollo*

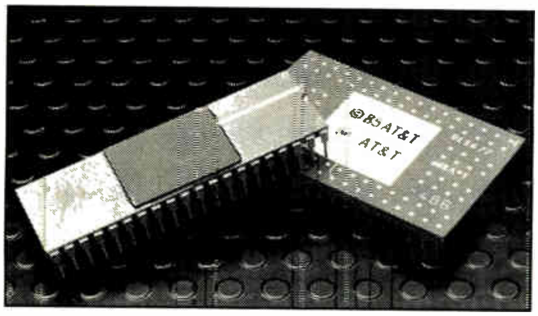
Standard Microsystems Corp., 35 Marcus Blvd., Hauppauge, N. Y. 11788.
Phone (516) 273-3100 [Circle 360]

AT&T MOVES ITS DSP CHIP INTO THE MARKETPLACE

Not every company can come to market with a tried-and-true chip. But AT&T Co.'s Components and Electronic Systems division is joining a growing list of semiconductor giants in the market for monolithic digital signal processors with a chip that it has been using in its own equipment for two years. The WE DSP32 32-bit chip uses floating-point arithmetic to achieve higher bandwidth and better accuracy than competing chips.

What sets this DSP apart from all the others, AT&T says, is that it is the only floating-point single-chip DSP now on the market and ready for delivery. Other companies—notably NEC and Texas Instruments—have announced similar products, but none is commercially available yet. Samples of the DSP32 can be had in four weeks, and production quantities can be delivered in 13 weeks.

"We're not selling futures with this thing," says Ray Pitetti, marketing manager for DSP. "It's here and ready right now. And we've made considerable changes and improvements since we



CHOICE. AT&T's digital signal processor comes in a 40-pin ceramic DIP or a 100-pin grid array.

started using this chip internally."

Just what those changes were, Pitetti isn't saying, but he will talk about some that are in the works. The chip, which now operates on a 16-MHz clock and executes instructions in a 250-ns cycle—about 8 million floating-point operations/s—is due for performance enhancements in the third quarter.

By shrinking its geometries, AT&T anticipates dropping the chip's cycle time to under 150 ns and improving worst-case power consumption from 2.45 W to less than 2 W. None of these changes will have any effect on the architecture, however, so that designers who begin to integrate the DSP into a system now will be able to make an easy chip-for-chip replacement with the enhanced model later, Pitetti says.

System designers will also be helped along by software and hardware development tools. A support software library includes a "C-like" syntax assembler and an architectural simulator, while a one-board development system allows real-time testing, debugging, and evaluation. Fabricated in a single-level metal n-MOS process, the chip incorporates both random-access and read-only memory. The 2-K bytes of ROM and 4-K bytes of RAM can eliminate the need for external memory chips in some applications, Pitetti says. Designed as a general-purpose chip, it is best suited for applications in speech, image, and graphics processing. Floating-point arithmetic is critical in such applications because they require great precision in processing large amounts of data.

The telecommunications systems for which the chip was originally designed demanded higher processing capabilities than one chip could provide, Pitetti says. So AT&T's designers built in capabilities that make it easier to cascade the DSP32 than conventional chips. While most DSPs cannot be interconnected without interface chips to help convert data into a form they can handle, any number of DSP32s can be chained together. "One chip can drive the other in a master/slave configuration," Pitetti says. "You can have multiple DSPs without the 'glue chip' interfaces."

Prices for the WE DSP32 start at $175 apiece, and there is a choice of packages. Users can select between a 40-pin DIP and a 100-pin grid array, both of which offer both serial and parallel I/O capabilities. The PGA provides access to 56-K bytes of external memory over a 32-bit data bus and 14 additional access lines. Development tools—both hardware and software—are also available. *–Tobias Naegele*

AT&T Technology Systems Co., Components and Electronic Systems, 555 Union Blvd., Allentown, Pa. 18103.
Phone (800) 372-2447 [Circle 363]

25-NS SRAMs USE ONLY 100 mW

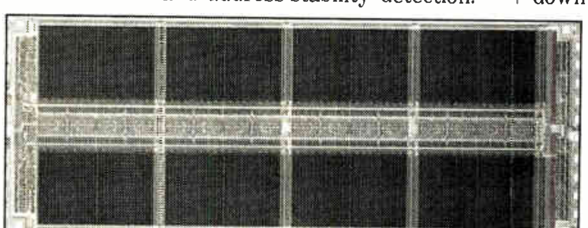
Motorola is entering the competition in high-speed CMOS static RAMs with two 64-K parts and one 16-K. With access times as low as 25 to 45 ns, the 4-K-by-4-bit MCM6268, the 64-K-by-1-bit MCM6287, and the 16-K-by-4-bit MCM-6288 are guaranteed over the full commercial temperature range.

Competitive high-speed CMOS SRAMs are only now reaching the 35-ns level, and they typically dissipate 500 mW at that speed. Motorola's chips can be used without sacrificing active power. Active dc power on all three parts is 100 mW (20 mA at 5 V). Active ac power is 400 mW on the MCM-6268 and MCM6288 and 250 mW on the MCM6287. On all three, standby power is 25 mW.

The balance of speed and very low active power comes from a new block-oriented architecture with extremely short bit lines—each has only 64 cells. The architecture provides high-speed signal development during read instructions and also ensures high data integrity during write operations.

BUFFERS. On the 64-K SRAMs, these low-capacitance bit-lines are decoded into 16 local operational amplifiers that drive four global data lines. To improve immunity against input glitches and false address-float conditions, the SRAMs incorporate an address buffer that combines hysteresis and a semaphore latch.

Motorola's SRAMs stand out from other parts in their ability to operate in a truly asynchronous mode with high skew immunity. The company achieved this by adding a proprietary circuit that can distinguish between address-transition detection and address-stability detection.



FULL SPEED. The 25-ns 64-K-bit SRAM uses just 250 mW.

In the first operation, the address-transition setup signal's rising edge equalizes the array, turns off all word-lines, and shuts down the RAM. This occurs immediately and independently of any previous cycle.

The signal's falling edge is used for true address-stability detection. The falling edge, rather than the rising edge, begins the access cycle, times the turn-on of both the new word-line and amplifiers, and powers down the RAM after a predetermined time.

The SRAMs also have a chip-select speedup circuit that equalizes access times from chip-select and address commands. This circuit remedies the usual delay experienced when chip-deselect shuts down the address buffer's inputs.

Fabricated in 1.5-μm double-polysilicon, double-metal CMOS, the SRAMs use a four-transistor cell occupying only 189 μm^2 with a cell ratio (the ratio of pull-down device to transfer gate size) of 3:1. This allows high data integrity and faster write access.

The two 64-K SRAMs come in 300-mil-wide, 22-pin ceramic side-braze or plastic DIPs and in ceramic leadless chip carriers measuring 290 by 490 mils. All feature the standard Jedec pinout. The 16-K-by-4-bit MCM6288 also comes in a 24-pin version with an output-enable pin. The 4-K-by-4-bit MCM6268 comes in a 300-mil, 20-pin DIP, also with the Jedec pinout.

At 25 ns, the MCM6287 in a 22-pin ceramic package costs $43.40 each. The MCM6288 costs $54.60 each in the same package, and the MCM6268 costs $16.80 in a 20-pin plastic package. Prices are for lots of 100 pieces or more. Samples are available now, with production quantities to follow next month. *–Bernard C. Cole*

Motorola Inc., MOS Memory Products Group, 3501 Ed Bluestein Blvd., Austin, Texas 78762.
Phone (512) 928-7465 [Circle 361]

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3	Mobil	27	Boeing	51	Georgia-Pacific	75	Hewlett-Packard	99	Pfi
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5	IBM	29	Allied	53	W.R. Grace	77	Texas Instruments	101	N
6	Texaco	30	Eastman Kodak	54	Signal Companies	78	LTV	102	Pillsbı
7	E.I. du Pont	31	Unocal	55	Anheuser-Busch	79	American Brands	103	PPG Industr
8	Standard Oil (Ind.)	32	Goodyear	56	Nabisco Brands	80	International Paper	104	Int. Harves
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10	General Electric	34	Westinghouse Elec.	58	Coastal	82	Burroughs	106	Borg-Warı
11	Gulf Oil	35	Philip Morris	59	Raytheon	83	Archer-Daniels-Midland	107	American Cyanar
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18	United Technologies	42	McDonnell Douglas	66	Sperry	90	CPC International	114	Warner Com
19	Tenneco	43	Rockwell Int.	67	Gulf & Western Ind.	91	Time Inc.	115	Owens-Illin
20	ITT	44	PepsiCo	68	Continental Group	92	Deere	116	Carnati
21	Chrysler	45	Ashland Oil	69	Bethlehem Steel	93	Bristol-Myers	117	American C
22	Procter & Gamble	46	General Dynamics	70	Weyerhaeuser	94	Martin Marietta	118	Reynolds Met
23	R.J. Reynolds Ind.	47	3M	71	Ralston Purina	95	Firestone Tire & Rubber	119	Campbell So
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27 million Americans can't read. And guess who pays the price.

While American business is trying to stay competitive with foreign companies, it's paying an added penalty. The penalty of double-digit illiteracy.

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What does illiteracy cost you? Get out your calculator. Illiterate adults make up 50%-75% of our unemployed. Every year they cost us an estimated $237 billion in lost earnings. They swell our welfare costs by $6 billion annually and diminish our tax revenues by $8 billion.

Illiteracy costs you through your community, too. It robs the place where you work and live of its resources. It undermines the potential of the people who make your products and the people who buy them. No dollar figure can be assigned to this. But over the years, this may be the costliest loss of all.

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ELECTRONICS WEEK

IBM REVENUES RISE BUT NET SLIPS 7.7%

IBM Corp. announced some good news and some bad news last week. The good news is that sales were up 7.3% to $12.2 billion for the second quarter, but the bad news could haunt Big Blue for the rest of the year: net earnings were down 7.7% compared with a year ago, indicating extreme pressure on profit margins that could last through 1986. The report took Wall Street by surprise, and IBM stock dropped $3.875 per share the day of the announcement.

MOTOROLA GAINS; INTEL, AMD LOSE

Motorola Inc.'s second-quarter earnings more than doubled to $55 million on sales of $1.5 billion, but other chip makers weren't so fortunate. Intel and Advanced Micro Devices both posted significant losses. Intel Corp., Santa Clara, Calif., reported a $20.4 million loss for the second quarter as revenue plunged to $305.2 million—a 17.9% decline from revenues in the comparable quarter of 1985. Meanwhile, AMD Inc., Sunnyvale, Calif., declared a $28 million loss despite a modest revenue growth of 2.2% that brought total income to $153.9 million.

PC SALES UP IN EUROPE

Europe is escaping the downturn that struck the U.S. personal computer market, says Gordon Curran, director of Intelligent Electronics Europe, in Paris. He estimates that PC volume shipments on the continent will rise from the 1.227 million units sold last year to 1.657 million units in 1986. Curran says European and U.S. suppliers are battling hard for the fast-moving Italian market, where IBM Corp. and Ing. C. Olivetti & Co. dominate. In the first half of 1986, Curran says, Italian businesses have already bought about 200,000 microcomputers. Last year IBM led with a 31.1% market share versus Olivetti's 26.9%, but now the two are so close that it's hard to tell which will emerge the winner.

SWISS MAY RELAX TELECOM RULES...

The Swiss government is drafting new telecommunication regulations relaxing the post office monopoly on telephones and Telex machines. But the government plans to leave the country's communications networks under post office control. The new regulations will be put before parliament for debate and may also be the subject of a referendum before becoming law.

...AS NTT LOSES ITS MONOPOLY

Cracks are appearing in Nippon Telegraph & Telephone Corp.'s telecommunications monopoly, as alternate long-distance phone services will soon be available. Japan Telecom Co., Daini Denden Inc., and Teleway Japan Corp. have received permission to start service. Undercutting NTT's prices by 20% to 30%, the new companies will start operations Aug. 1. with several private-line services for businesses, including telephone, facsimile, data communications, and video teleconferencing.

HP JOINS X/OPEN TO FIGHT IBM

In joining the X/Open Group, Hewlett-Packard Co. is now the third U.S. member firm. X/Open, which also counts seven European members, is a united attempt to keep IBM Corp. from dominating the European minicomputer and work station market. Other U.S. representation comes from the European subsidiaries of Digital Equipment Corp. and Sperry Corp. To keep IBM at bay, the X/Open group is attempting to unite behind AT&T Bell Laboratories' Unix operating system as a standard [*Electronics*, July 10, 1986, p. 121].

WANG WILL DROP 1,600 WORKERS

Despite modest increases in revenue and earnings, Wang Laboratories Inc. is cutting its workforce again. The new 1,600-worker cuts put Wang's employees at 30,000 worldwide. The move comes 13 months after Wang slashed another 1,600 from its payroll during last summer's computer slump. The Lowell, Mass., company hopes to induce 1,400 employees to leave through early retirement and voluntary separation programs, but 220 workers at Wang's plant in Juncos, Puerto Rico, will receive straight layoff notices.

EUROPEANS TARGET AUTO ACCIDENTS

Car makers and traffic authorities in France, West Germany, Italy, Sweden, and Britain are working together on an electronic communication system designed to avoid collisions. Called Prometheus (for Program for European Traffic with Highest Efficiency and Unprecedented Safety), the eight-year project is backed by Europe's Eureka program. The goal is an automatic information exchange among cars and traffic signals to alert drivers to dangerous conditions.

GE TAKES AXE TO RCA/SHARP

General Electric Co. has canceled the RCA/Sharp Microelectronics Inc. joint venture, established last year by RCA Corp., New York, and Sharp Corp., Tokyo. The joint company would have established a shared design facility and foundry in Camus, Wash., but when GE bought RCA late last year for $6.28 billion, the project was put on hold. As part of the agreement to cancel the venture, GE, Fairfield, Conn., and Sharp will study other areas of mutual interest for future cooperation.

GTE LABS SQUEEZES 4 CHANNELS ONTO 1

Researchers at GTE Laboratories Inc., Waltham, Mass., have discovered a way to digitize and compress four voice channels onto one 64-K-bit/s channel without distorting signal quality. GTE has applied for patents on the technology, which could be used commercially by next year.

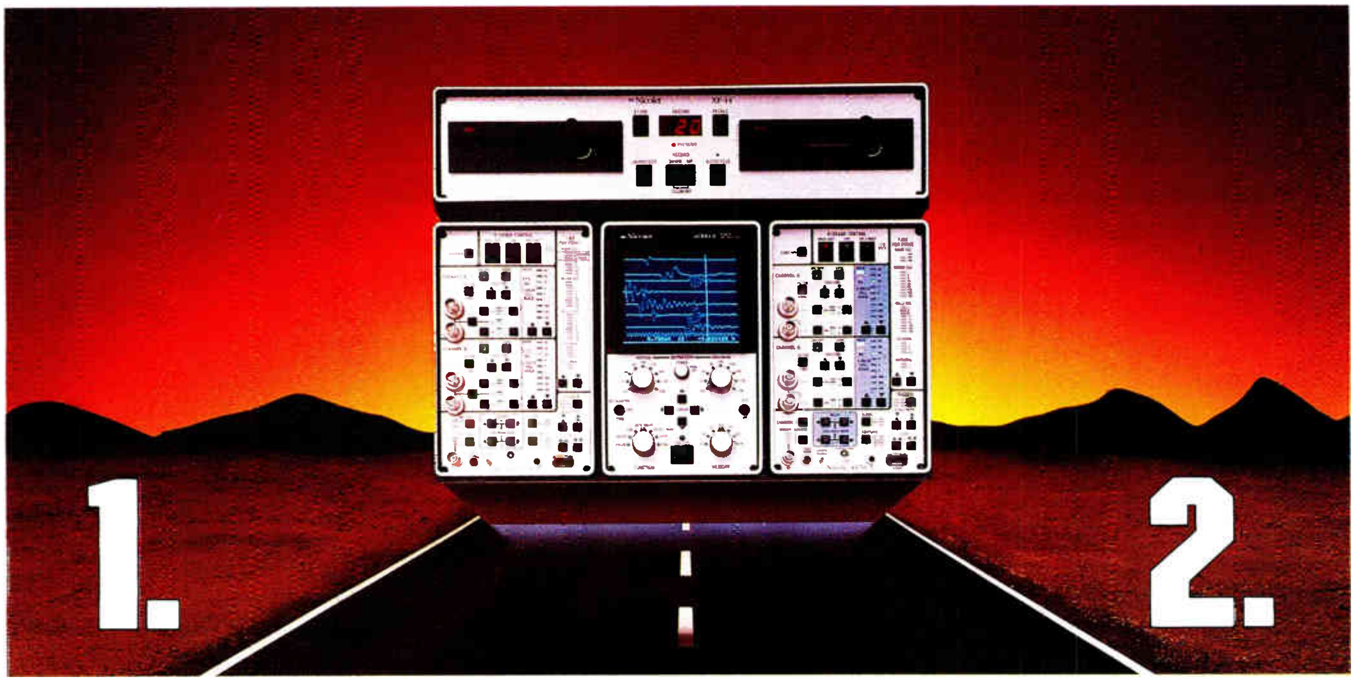
INMOS CLOSES U.S. PRODUCTION LINES

Inmos Corp. is closing its Colorado Springs memory-chip manufacturing lines and laying off 450 of 800 workers. Volume production will now be based in Newport, Wales. But the company will keep research and development and U.S. sales and marketing in Colorado Springs, and is planning a new 1-μm CMOS pilot line for a series of 25-ns static RAMs. Inmos's British-based parent, Thorn EMI, expects capacity throughout the chip industry to exceed demand for the next two to three years.

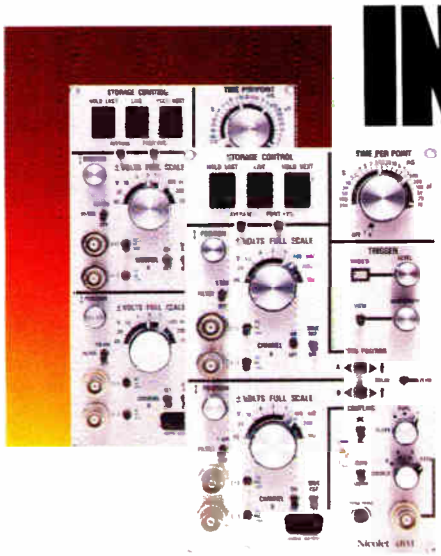
STUDY SAYS MANY AREN'T USING CAE

More than a third of the companies involved in printed-circuit-board and chip design have no significant investment in computer-aided engineering, according to a study sponsored by the Automated Design & Engineering for Electronics conference. The report says 37% of those surveyed either had not begun to purchase CAE or had "made no significant purchase." But where CAE has been installed, it is in heavy demand. The study says a typical work station is shared by 3.9 designers who use it for 13 hours a day.

THE FIRST NAME IN DIGITAL SCOPES



TWO DIGITAL SCOPES IN ONE.



The Acquisition.

With sweep speeds from days to nanoseconds and resolution up to 15 bits, the 4094 digital 'scope can capture the most elusive signals. Every plug-in has 16K of memory, viewable trigger set-up and independent pre- or post-trigger delay on each channel. Signal averaging is standard and our latest 10 MHz/12-bit plug-in even offers real time manipulation of the incoming signals. With two plug-ins the 4094 can record four channels simultaneously. Or even monitor two slow signals and capture high speed glitches at the same time. All under computer control or via manual operation: whatever your application demands.

The Analysis.

Expand and examine any waveform feature in detail. Use the dual cursors and numerics to measure the time or voltage of any point. Compare live or stored waveforms with each other or with pre-recorded references. Store signals on disk manually or automatically. Use pushbutton programs to manipulate the data or send it to your computer via GPIB or RS232 interface. Complete your report with a hardcopy plot using the XY/YT recorder or digital plotter outputs.

First Time, Everytime.

Don't miss important data because of set-up errors. From the World's first in 1973 to the latest models, Nicolet 'scopes are easy to use. Find out how they can be the quickest solution to your signal problems. For more information call 608/273-5008, or write Nicolet Test Instruments Division, P.O. Box 4288, 5225 Verona Road, Madison, WI 53711-0288.

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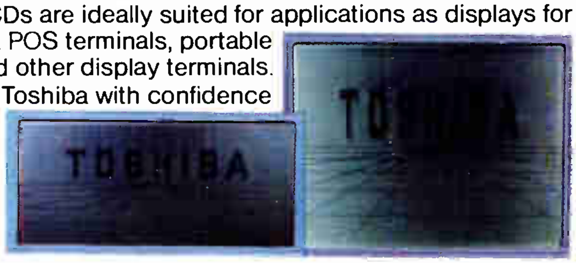
2,000 sharper-than-ever characters all on a portable LCD display.

Toshiba's newest LCD modules give you 640 × 200 dot displays in a choice of two viewing sizes. One is approximately the size of a magazine, and the other about half that size.

Both sizes put an enormous amount of information on view . . . an array of 80 characters × 25 lines. But still bulk and power consumption are at a minimum. Battery powered, these slim modules interface with various systems through LCD controller without renewing software.

Toshiba's advanced technology has also eliminated surface reflection and developed a sharper contrast which gives a brighter and easier to read viewing screen. And for low light or dark viewing an optional backlightable LCD is available.

These versatile LCDs are ideally suited for applications as displays for personal computers, POS terminals, portable word processors and other display terminals. You can also look to Toshiba with confidence for a wide range of sizes and display capacity to suit your LCD requirements.



TLC-363 *TLC-402*

Specifications

		TLC-402	TLC-363B
Display			
Number of Characters		80×25 (2,000 characters)	80×25 (2,000 characters)
Dot Format		8×8, alpha-numeric	8×8, alpha-numeric
Overall Dimensions (W × H × D)		274.8×240.6×17.0 mm	275.0×126.0×15.0 mm
Maximum Ratings			
Storage Temperature		−20° – 70° C	−20° – 70° C
Operating Temperature		0° – 50° C	0° – 50° C
Supply Voltage	V_{DD}	7 V	7 V
	$V_{DD} - V_{EE}$	20 V	20 V
Input Voltage		$0 \leq V_{IN} \leq V_{DD}$	$V_{SS} \leq V_{IN} \leq V_{DD}$
Recommended Operating Conditions			
Supply Voltage	V_{DD}	5±0.25V	5±0.25V
	V_{EE}	−11±3V Var.	−11±3V Var.
Input Voltage	High	V_{DD} − 0.5V min.	V_{DD} − 0.5V min.
	Low	0.5V max.	0.5V max.
Typical Characteristics (25°C)			
Response Time	Turn ON	300 ms	300 ms
	Turn OFF	300 ms	300 ms
Contrast Ratio		3	3
Viewing Angle		15 – 35 degrees	15 – 35 degrees

Design and specifications are subject to change without notice.

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