PROGRAMME ESSDERC

ESSDERC ESSCIRC

35th European Solid-State Device Research Conference

12 - 16 September 2005 - Grenoble, France

Organized by

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AEPI GRENOBLE ISERE

TUESDAY, 13 SEPTEMBER 2005

08:45	Introduction and Paper Award 2004 *(Dauphine)*			
09:15 - 09:55	Joint Plenary Session - R. Cavin *(Dauphine)*			
10:00	ESSDERC Plenary Session - A. Auberton-Hervé, C. Mazuré *(Dauphine)*			
10:40	Coffee Break *(Alpes Congrès - exhibtion area)*			
11:05	SESSION 1.A. : Multi-Gate Devices *(Dauphine)*	SESSION 1.B. : Gate Stack *(Oisans)*	SESSION 1.C. : RF Devices *(Sept Laux)*	SESSION 1.D. : Compact Modeling *(Stendhal)*
12:45	Lunch Break *(Salon les Ecrins)*			
14:15 - 14:55	Joint Plenary Session - E. Yablonovitch *(Dauphine)*			
15:00	2.A. : Nano-Scaled Devices *(Chartreuse)*	2.B. : Dynamic Random Access Memories *(Belle Etoile)*	2.C. : High- and Medium-K Characterisation *(Meije)*	SESSION 2.D. : Nanowires *(Sept Laux)*
16:40	Coffee Break *(Salle de Réception)*			
17:00	RUMP SESSION: Where Will the Revolutionary Solutions Come from: Technology or Design? (Dauphine)			
18:30	End of conference day			
19:00	Welcome Reception *(Musée de Grenoble)*			

WEDNESDAY, 14 SEPTEMBER 2005

09:00 - 09:40	Joint Plenary Session - M. Shur (Dauphine)			
09:45	SESSION 3.A. : RF and Power SOI *(Chartreuse)*	SESSION 3.B. : Nanoscale and Organic Devices *(Sept Laux)*	SESSION 3.C. : Back-End Characterisation and Reliability *(Meije)*	SESSION 3.D. : Transport in Novel Materials *(Belle étoile)*
11:05	Coffee Break *(Salle de Réception)*			
11:25	SESSION 4.A. : Strain Engineering *(Chartreuse)*	SESSION 4.B. : Non-Volatile Memories I *(Belle étoile)*	SESSION 4.C. : Noise and Fluctuations in Nanometer MOSFETs *(Meije)*	
12:45	Lunch Break *(Salon les Ecrins)*			
14:15 - 14:55	Joint Plenary Session - M. Thompson *(Dauphine)*			
15:00	ESSDERC Plenary Session - H.-S. P. Wong *(Dauphine)*			
15:40	Coffee Break *(Alpes Congrès - exhibtion area)*			
16:00	SESSION 5.A. : Biological and Optical Devices *(Stendhal)*	SESSION 5.B. : High-K Dielectrics *(Oisans)*	SESSION 5.C. : Oxide Reliability and ESD *(Dauphine)*	
18:00	End of conference day			
19:00	Gala Dinner			

THURSDAY, 15 SEPTEMBER 2005

09:00 - 09:40	Joint Plenary Session - C. Joachim *(Dauphine)*		
09:45	ESSDERC Plenary Session - L. Risch *(Dauphine)*		
10:25	Coffee Break *(Alpes Congrès - exhibtion area)*		
10:45	SESSION 6.A. : CMOS Technology *(Dauphine)*	SESSION 6.B. : Advanced Process Steps Integration *(Oisans)*	SESSION 6.C. : Power and HV Devices *(Stendhal)*
12:45	Lunch Break *(Salon les Ecrins)*		
14:15	Presentation ESSDERC-ESSCIRC 2006 *(Dauphine)*		
14:25 - 15:05	Joint Plenary Session - H. Stormer *(Dauphine)*		
15:10	SESSION 7.A. : Advanced Numerical Methods *(Chartreuse)*	SESSION 7.B. : Non-Volatile Memories II *(Belle étoile)*	SESSION 7.C. : Strained Si Characterisation and Reliability *(Meije)*
16:30	Coffee Break *(Salle de Réception)*		
16:40	SESSION 8.A. : Carbon Nanotube Devices *(Chartreuse)*	SESSION 8.B. : High-Speed Memories *(Belle étoile)*	SESSION 8.C. : Mobility Extraction *(Meije)*
17:40	Closing Session *(Dauphine)*		
18:00	End of conference day		
19:30	Farewell Party		

WELCOME

The 35th European Solid-State Device Research Conference takes place in Grenoble from Tuesday 13 September to Thursday 15 September 2005. The aim of the conference is to provide an annual European forum for the presentation and discussion of recent advances in semiconductor devices and technologies. ESSDERC 2005 is jointly organized with the 31st European Solid-State Circuits Conference (ESSCIRC). The initiative to merge the two sister conferences was started in 2002, as an incentive to foster the necessary interaction among technologists, device experts, and circuit & system designers. While keeping separate Technical Programme Committees, ESSDERC and ESSCIRC are governed by a single Steering Committee and share plenary keynote presentations, tutorials (September 12) and satellite workshops (September 16) bridging both communities. Participants registered for either conference are encouraged to attend any of the scheduled parallel sessions.

ESSDERC-ESSCIRC is the largest and best quality European meeting related to micro and nano electronics. In order to guarantee the excellence of the scientific level, the Steering Committee has abolished posters and half-time presentations, while imposing a very strict acceptance rate (40%). The evaluation of submitted papers has been improved: enlarged Technical Programme Committee, redesigned sub-committee topics, increased number of reports per paper, new functionalities enabled in the web submission system. A total number of 308 papers were submitted to ESSDERC, representing a tremendous increase (+ 85 papers) compared to 2004 and a record for the last decade. More than 30 countries, from all continents, were represented with substantial participations from Europe, USA, Japan and Korea. Most of the papers originated from strong national (55%) and international (16%) co-operations. Only 123 contributions could be included in the final programme of ESSDERC 2005 which also features outstanding plenary and session invited talks. ESSDERC'05 will especially focus on advanced device concepts, revolutionary transistor architectures, new technologies and process steps related to ITRS road blocks, nanotechnologies, quantum and molecular devices, sensors and displays, etc.

Several innovations are tested or reintroduced this year: a joint panel session, session invited talks, an exhibit, a farewell party and technical visits (Friday September 16). Our conference has a new logo. A Special Issue of Solid-State Electronics will contain selected full-length papers. Grenoble will not miss the opportunity to preserve and develop the tradition of a warm Social Programme: the Welcome Reception at the Museum of Grenoble (Tuesday evening), the Gala Dinner and Show on Wednesday evening and, finally, the Farewell Party (Thursday evening) at the scenic Bastille location which overlooks Grenoble area and mountains. The accompanying persons will enjoy several excursions. Grenoble is a high-tech city, with wonderful surroundings in the heart of the Alps, offering attractive opportunities for an extended stay over the weekend.

We would like to thank the authors for their contributions, the members of the Technical Programme Committee, Steering Committee and Local Organizing Committee for their hard work, Mrs Iris Mazuré our omnipresent conference secretary, and our generous sponsors.

We are looking forward to a successful conference, with exciting scientific contents and rich human interactions. We warmly welcome you and your colleagues to Grenoble.

Sorin Cristoloveanu, *Conference Chair*
Michel Brillouët, *Conference Co-Chair*
Thomas Skotnicki, *ESSDERC Technical Programme Chair*

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ESRF in Grenoble.

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Further information

For further information about the conference please contact the conference secretariat:

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Or visit the web page: **http://www.essderc2005.com**

2005 mm silicon wafers.

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GENERAL INFORMATION

GRENOBLE - An Attractive Destination

Grenoble is the capital of the French Alps, located in a valley surrounded by beautiful mountains. On the touristic side, Grenoble is famous for alpine landscapes, sunshine and snow. Stendhal once wrote that "...there was a mountain at the end of each Grenoble street: Belledonne, Vercors and Chartreuse..."

On the scientific side, Grenoble is often referred to as the place where the Silicon and SOI Valleys merge. Stendhal would certainly write today that "…there is research lab or high-tech place at the corner of each mountain".

A number of advanced R&D centres and leading semiconductor fabs are scattered around Grenoble. Application oriented research is blooming, its roots being the dense network of laboratories dedicated to basic research. World class institutes (European Synchrotron Radiation Facility, CEA, CNRS, High Magnetic Field Laboratory, Neutron ILL reactor, etc) are surrounded by numerous smaller, yet outstanding University and CNRS laboratories.

Grenoble is one of the major university towns in France: over 60 000 students representing about 10% of the population of the greater Grenoble area. Grenoble is understandably proud of its academic and scientific environment, with a long tradition of partnership between research and industry.

Climate

September is usually a sunny month with an average temperature of 20 - 24°C. Since rain showers are possible, light clothing and a raincoat are recommended. However, the organisers have negotiated perfect weather conditions...

Time Zone

Central European summer time (GMT + 2).

Electricity

Standard European type 2 pin round sockets with 220 Volts, 50Hz are used.

Currency and Value Added Tax (VAT)

The French national currency is the Euro. France has a Value Added Tax called T.V.A (19.6 %) that is included in the price of all goods and services. Visitors are entitled to claim this tax back on purchases made over a certain amount, upon or after leaving the country.

Tips

Tips in restaurants, hotels and taxis are not usual; they are included in the cost.

GENERAL INFORMATION

Banks

Banks are usually open from Monday to Friday from 09h00-16h00. Some banks are closed on Monday and some are open on Saturday.

Emergency calls

In case of emergency, dial 18 for Fire/accident and 15 for Medical Help (SAMU).

Visa Requirements

All foreign participants must have a valid passport, except the European Union citizens, who need only an identification card. According to the citizenship, the duration and purpose of the stay in France, a visa may be required. For more information http://www.diplomatie.fr/venir/visas/

Invitation letters to apply for a visa will be sent by the organisers upon request. We advise you to forward your request before 15 July 2005 to:

essderc-esscirc@enserg.fr

clearly indicating the dates of arrival and departure.

Hotel Reservation

ESSDERC-ESSCIRC'05 has blocked hotel rooms for the participants until August 1, 2005. Please note that September is high season for business travellers. It is therefore strongly recommended to complete the reservation of your hotel room as soon as possible.

An updated hotel list is available on:

http://www.essderc2005.com or http://www.esscirc2005.com

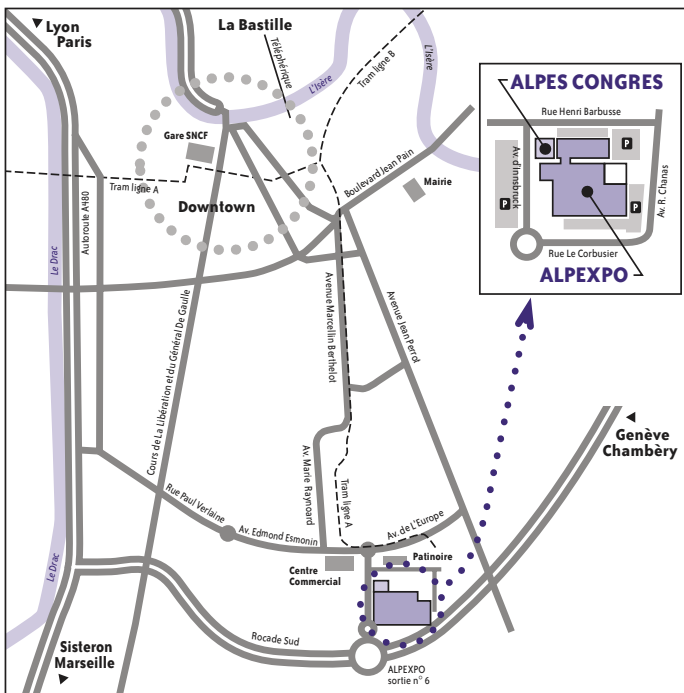Please contact the hotel of your choice and make the reservation directly, mentioning the name of the conference.

The conferences will be held at:

Alpes Congres - Alpexpo
Avenue d'Innsbruck - BP 2408
38034 GRENOBLE - France

Tel. +33 (0) 476 39 66 00
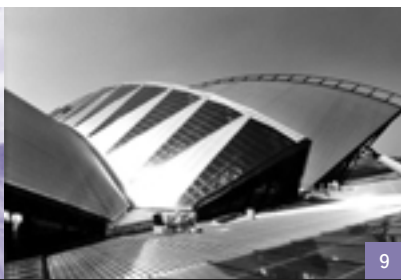

How to get to the conference site

From downtown / Grenoble train station:

▶ Tramway line A, direction Echirolles : Denis Papin, Stop : Pôle Sud.

▶ By car:
  Take Rocade Sud (coming from A48 Lyon-Grenoble or A41 Genève-Chambery-Grenoble), exit number 6: Alpexpo-Grand Place. There is a large car park in front of the Alpes Congrès - Alpexpo conference centre.

CONFERENCE SITE

By plane:

- ▶ Lyon-St. Exupéry airport www.lyon.aeroport.fr : 1 hour drive. Taxi cost : approx. 130 - 140 EUR - Tel. + 33 (0) 826 800 826.

- ▶ Airport shuttle bus SATOBUS www.satobus.com (every hour *hh*.30 from 7.30 am to 21.30 pm direction Grenoble, every hour *hh*.00 from 5.00 am to 20.00 pm direction Lyon-St. Exupéry) - Tel. + 33 (0) 472 68 72 17

- ▶ Airport Genève-Cointrin www.gva.ch : 1.5 - 2 hours drive. Taxi costs : approx. 220 EUR - Tel. + 41 (0) 22 798 20 00
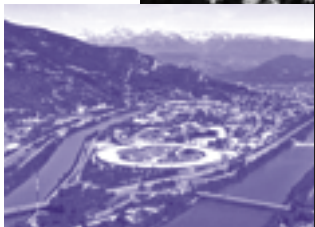
By train:

- ▶ High Speed Train (TGV)
  Grenoble-Paris 3 hours - 7 trains every day
  (other TGV from Lille, Nantes)

Grenoble Gare SNCF :
Tel. + 33 (0)8.92.35.35.35. (reservations) - www.sncf.fr

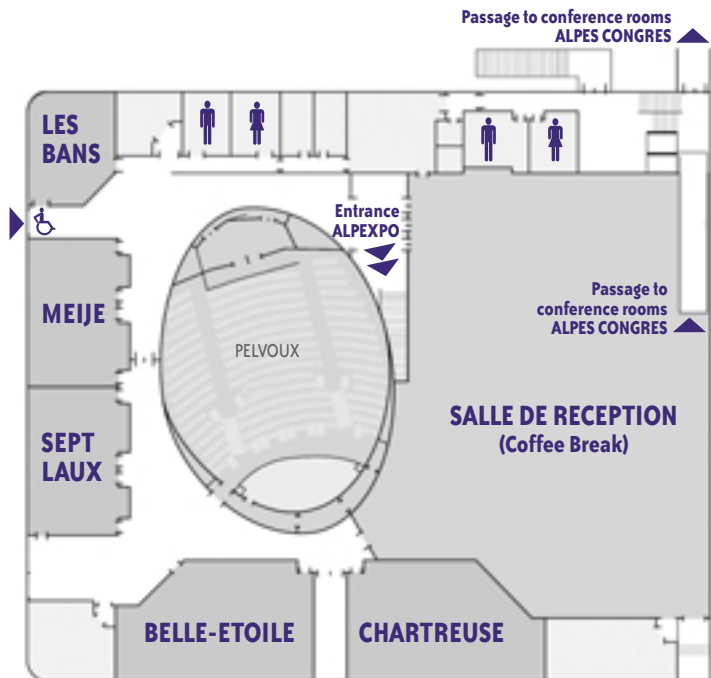**By car - distance from Grenoble:**

- ▶ Lyon: 100 km
- ▶ Geneva: 145 km
- ▶ Torino: 240 km
- ▶ Nice: 330 km
- ▶ Paris: 570 km
- ▶ Barcelona: 625 km
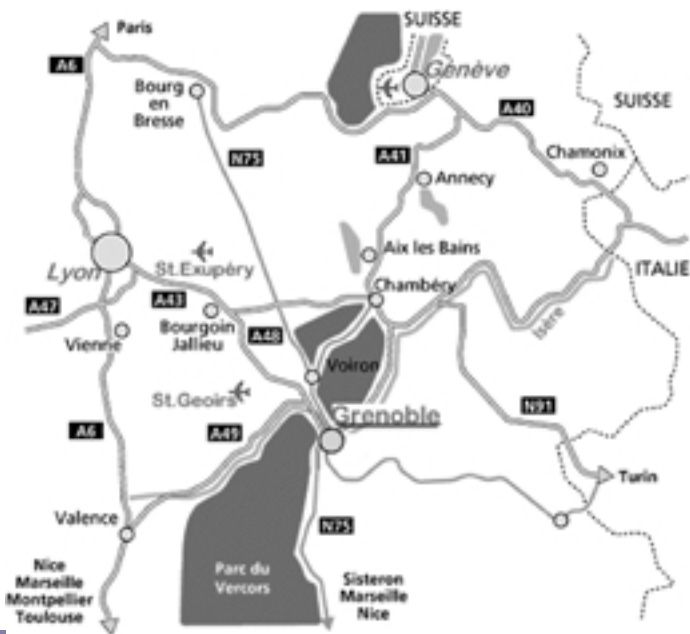
MAP CONFERENCE FACILITIES

Alpes Congres and Alpexpo are connected by an inner passage.

First Floor conference rooms Alpexpo

Passage to conference rooms
ALPES CONGRES ▲

LES BANS

Entrance
ALPEXPO

Passage to
conference rooms
ALPES CONGRES ▲

MEIJE

PELVOUX

SALLE DE RECEPTION
(Coffee Break)

SEPT LAUX

BELLE-ETOILE
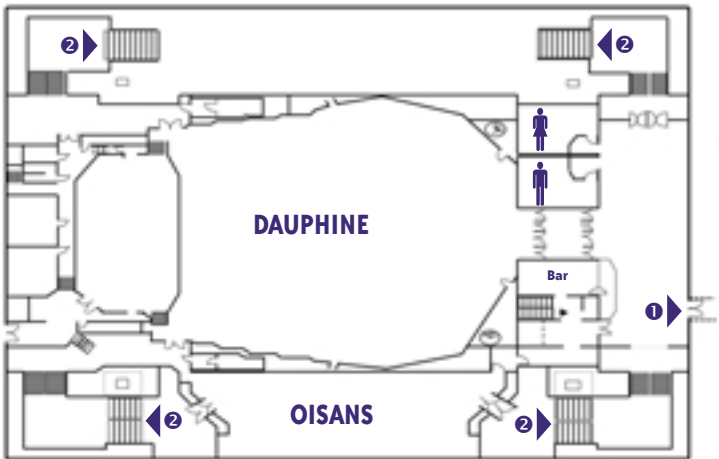
CHARTREUSE

MAP CONFERENCE FACILITIES

Ground Floor conference rooms Alpes Congrès

Main entrance ALPES CONGRES
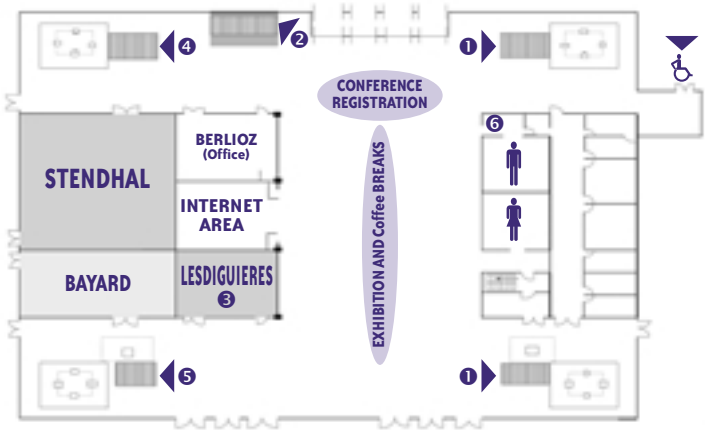
- ❶ To Dauphine and Oisans
- ❷ Downstairs to lunch area (Salon Les Ecrins)
- ❸ Speakers room
- ❹ To Dauphine
- ❺ To Oisans
- ❸ Telephone

First Floor conference rooms Alpes Congrès

- ❶ Passage to Alpexpo
- ❷ Downstairs to Conference Registration, Exhibition & Coffe Break

CONFERENCE REGISTRATION

Please complete the registration form (see annexed A4 sheet) and send it or fax it to:

MCI France / ESSDERC-ESSCIRC
11 rue de Solférino - 75007 Paris - Fax +33 (0)1 53 85 82 83

or register online:

http://www.essderc2005.com or http://www.esscirc2005.com

To take advantage of pre-registration rates, the completed registration form and fee must be received by 12 AUGUST 2005. Early registration is encouraged.

Conference registration fee covers admission to all sessions, the exhibition, the coffee breaks, the welcome reception, the gala dinner, the farewell party, three lunches, a CD and one volume of the proceedings.

Tutorial registration fee covers admission to the tutorial, the coffee breaks, the lunch, the CDROM containing all short courses, and one printed version of the selected short course.

Workshop registration fee covers admission to the workshop, the lunch buffet and the coffee breaks.

Accompanying persons fee includes the welcome reception, the gala dinner and the farewell party.

Conference Registration Fees (Tuesday, 13 – Thursday 15 September, 2005)	BEFORE AUGUST 12, 2005 (Payment must be received before 12.8.2005)	AS FROM August 13, 2005
Regular	590,00 EUR	670,00 EUR
IEEE members (IEEE N° required)	560,00 EUR	640,00 EUR
Students (please provide certificate)	490,00 EUR	570,00 EUR

Tutorials Registration Fees (Monday, 12 September)	BEFORE AUGUST 12, 2005 (Payment must be received before 12.8.2005)	AS FROM August 13, 2005
Tutorial 1 (full day) "New process and device concepts"	200,00 EUR	250,00 EUR
Tutorial 1 (Student)	150,00 EUR	200,00 EUR
Tutorial 2 (full day) "Advanced concepts for SOC and SIP"	200,00 EUR	250,00 EUR
Tutorial 2 (Student)	150,00 EUR	200,00 EUR
Tutorials 3 + 4 (half day each) "Nanoelectronics" + "Emerging Memory Architectures"	200,00 EUR	250,00 EUR
Tutorials 3 + 4 (Student)	150,00 EUR	200,00 EUR

Workshops Registration Fees (Friday, 16 September)	BEFORE AUGUST 12, 2005 (Payment must be received before 12.8.2005)	AS FROM August 13, 2005
1) SDR / Cognitive Radio	110,00 EUR	110,00 EUR
2) MOS-AK	free	free
3) SINANO	free	free
4) MIMOSA	200,00 EUR	200,00 EUR
5) ENIAC	free	free

CONFERENCE REGISTRATION

	BEFORE AUGUST 12, 2005 (Payment must be received before 12.8.2005)	**AS FROM August 13, 2005**
Accompanying persons	110,00 EUR	110,00 EUR
Additional Proceedings of ESSDERC or ESSCIRC	80,00 EUR	80,00 EUR
Technical Visits (Registration before 15 August 2005)		
STMicroelectronics (Friday, 16 September)	30,00 EUR	
SOITEC (Friday, 16 September)	30,00 EUR	
Tours		
V1 – La Chartreuse	23,00 EUR	23,00 EUR
V2 – Grenoble	22,00 EUR	22,00 EUR
V3 – Vercors region	27,00 EUR	27,00 EUR

Payment

▶ By cheque payable in France to the order of ESSDERC-ESSCIRC/ MCI France.

▶ **On line:** accepted credit cards VISA, EURO/MASTER CARD or AMEX.

▶ Payments can also be made by bank transfer to

ESSDERC-ESSCIRC 2005 / MCI France,

11 rue de Solférino, 75007 Paris

Bank : Crédit Lyonnais - Bank code : 30002 - Sort code : 00424 - Account number : 0000008606P - Key : 61 - Bank agency : Paris rue du Bac (00424) - IBAN : FR33 3000 2004 2400 0000 8606 P93 - BIC : CRLYFRPP

Cancellation

All cancellations must be notified in writing (by mail or fax BUT NOT email) to MCI France according to the following conditions. Reimbursement will be processed after the conference.

Up to August 29, 2005 : 80 EUR will be withheld for administrative fee

After August 29, 2005 : No refund

Requests for preregistration refunds must be received no later than 10 working days prior to the first day of the conference.

Name change: a processing fee of 30 EUR will be charged for changes in registration.

Registration desk

Conference registration will be located at

Alpes Congres - Alpexpo

Avenue d'Innsbruck - BP 2408 - 38034 GRENOBLE - France

Tel. +33 (0) 476 39 66 00 (switch board Alpexo)

Opening hours of the registration

12 September: 8 am - 5 pm

13 - 15 September: 8 am - 6 pm

16 September: 8 am - 3 pm

CONFERENCE INFORMATION

Internet services

Computer terminals with internet access will be available for free on the site of the conference during the opening hours.
It will also be possible to use the WIFI network (10 Mbytes/s) of the conference center using your personal laptop. WiFi cards can be purchased at the conference center (2 hours = 9.5 EUR, 24 hours = 29 EUR, 7 days = 99 EUR).

Conference language

The working language for the conference will be English to be used for all presentations and printed material.

Insurance disclaimer

Please arrange your own travel and health care insurance. The organizers will not be held liable for accidents, theft and property damage, nor for delays or any modification of the programme.

Speakers briefing

Authors should meet their chairperson in the session room 20 minutes prior to the beginning of their respective sessions.

Guidelines for Presentations

To ensure a successful presentation, without software compatibility problems, please note the following guidelines:

▷ Your presentation will take **20 minutes** including your introduction by the session chair and a few minutes for questions from the audience.

▷ **Electronic projection** will be used for all presentations (no transparencies or 35mm slides).

▷ Your presentation has to be in **PDF** or **PPT** format on **IBM PC** versions **ONLY**.

▷ Your presentation has to be saved using a file name with the pattern "**S_author_n**.pdf" (or .ppt) where **S** is the session number (see the conference programme), author is the last name of the first author and **n** is the version number of your file. Example: 1A1_Einstein_17.ppt.

▷ Please prepare a **SHORT vita** (5 lines) so that the chairman can introduce you.

▷ The deadline for submission of your presentation is: **September, 2nd 2005**. Details regarding the exact procedure of submissions will be available on the ESSDERC & ESSCIRC web site at the beginning of July.

▷ **No correction of your presentation will be possible** after September 2.

▷ Computers will be available in the **Speaker Preparation Room** to review your file (not to make changes).

▷ Please bring a backup CD or USB key with your presentation just in case.

▷ Despite the fact that the content of electronic presentations is assumed to be placed in the public domain at the time of the conference, ESSDERC-ESSCIRC'05 **will not publish or distribute the presentation files**.

Conference proceedings

All participants will receive a copy of either the ESSDERC or the ESSCIRC Proceedings and a CDROM with both ESSDERC and ESSCIRC accepted papers.

Best paper award

ESSDERC/ESSCIRC offers a "Best Paper" award (for contributed papers only) and a "Young Scientist" award, for the best paper presented by a speaker of less than 28 years old. The recipient will be the speaker himself. The selection is based on: (i) evaluation by the audience and (ii) paper ratings.

SOCIAL PROGRAMME

Tuesday, 13 September at 7 pm

A welcome reception will be offered by the Mayor of Grenoble, Michel DESTOT, at the "Musée de Grenoble", 5, place de Lavalette.

City center, tramway stop "Nôtre Dame - Musée".
Shuttle busses from Alpexpo will be arranged at 6:40 pm for the participants at the Panel Session.

Wednesday, 14 September at 7:30 pm

The Gala dinner will take place at the PRISME Seyssins (89 avenue de Grenoble, 38180 Seyssins).

The shuttle buses will leave from Alpexpo at 7 pm.

☺ A cocktail reception before the dinner will be offered by the Mayor of Seyssins, Didier Migaud.

☹ The morning session on Thursday still starts at 9 am !

Thursday, 15 September at 7:30 pm

Farewell party at the Restaurant du Téléférique, Fort de la Bastille, Grenoble.

To join the restaurant, please take the cable car, the organiser will provide free tickets.

Departure : Téléférique Grenoble-Bastille, Quai Stéphane Jay

The Farewell evening is sponsored by

ACCOMPANYING PERSONS PROGRAMME

All tours will be conducted in English. They will depart and return from and to the Conference Center. The organisers reserve the right to cancel tours with less than 25 participants. Since the excursions have a limited number of participants, please register as soon as possible. Reservations will be made in order of arrival; on-site availability cannot be guaranteed.

V1 - "La Chartreuse"

Tuesday, 13 September 2005 - 1:30pm-6:30pm
Cost: 23 EUR

This is a land of calm with small and pretty villages, peaceful forests, mountain passes crossed by winding roads overhanging torrents. Saint Bruno found refuge here more than 900 years ago to meditate and found the famous Grande Chartreuse Monastery. The monastery is still dedicated to prayer and meditation and part of it can be visited. The tour includes the visit of the distillery in the greatest caves as well as the tasting of the famous Chartreuse liquor.

V2 - "Grenoble"

Wednesday, 14 September 2005 - 09:00am-01:00pm
Cost: 22 EUR

This tour is designed to reveal the city's architectural and cultural treasures such as Saint-André, Notre-Dame and Grenette squares, the palace of justice, Stendhal's home, the city gardens and old private mansions from the 15 and 16 centuries so typical with their Renaissance spiral vaulted stairways. Riding the cable car, you will get to the fortified site of the Bastille to admire an astonishing panorama overlooking Grenoble and the surrounding mountains. In clear days Mont Blanc comes nearby!

V3 - "Vercors region"

Thursday, 15 September 2005 - 08:30am-01h30pm
Cost: 27 EUR

The Vercors seems to be an island surrounded by land. Water has cut deep gorges, magestic cirques, caves and swallow-holes, among the most famous in the Solar System.
Visit of the unforgettable Choranche Caves with its thousands of spaghetti-like stalactites reflected in the inner mountain lake. The sound and light show is spectacular. Stop at Pont-en-Royans at the end of the Bournes Gorges: dominated by rocky edges, this very, very old village is suspended above the bed of the torrent. Picturesque houses overhang the void.

ESSDERC-ESSCIRC
JOINT PLENARY TALKS

Horst Stormer
"Silicon Forever! Really?"

Eli Yablonovitch
"Silicon Nano-Photonics: Where the Photons Meet the Electrons"

Michael Shur
"Terahertz Electronics: Devices, Circuits, and Applications"

Ralph Cavin
"Limits of CMOS Devices and Circuits"

Mike Thompson
"Future of CMOS Technology, Manufacturing and Products"

Christian Joachim
"Towards a Molecule - Computer? "

MINATEC - Under construction.

ESSDERC-INVITED PLENARY TALKS

Carlos Mazuré and André-Jacques Auberton-Hervé
"Engineering Wafers for the Nanotechnology Era "

Nanotechnology starts at the substrate level. Substrate engineering is one of the most important innovations of the nanotechnology era driven by the vanishing boundary between substrate design and device architecture. SOI substrates, the first engineered substrates of its kind, have made possible an efficient optimization of MOSFET current drive while minimizing the leakage and reducing parasitic elements, thus enhancing the overall IC performance. Strained silicon, hybrid orientation SOI, germanium on insulator have added new handles to traditional scaling to further improve device and IC performance. An overview of the advances in Smart Cut engineered substrates and the impact on device performance will be given.

Biographies

André-Jacques Auberton-Hervé co-founded Soitec with Jean-Michel Lamure in 1992, and currently serves as President and CEO, overseeing the strategic, operational and financial activities of the company. Prior to founding Soitec, Dr. Auberton-Hervé managed joint development programs between LETI and Thomson-CSF, the ultimate target of which was the technological transfer from R&D to production. These programs included the transfer of 1.2 μm and 0.8 μm SOI CMOS for space applications. He was also in charge of several projects, which applied SOI to 3D integration, VLSI and ULSI. In 1999, he received the European SEMI Award in recognition of his work on the Smart Cut technology and his contribution to the semiconductor industry. Dr. Auberton-Hervé is a member of the Electrochemical Society and the IEEE. Dr. Auberton-Hervé has a Ph.D. in semiconductor physics and an M.S. in materials science from Ecole Centrale de Lyon (France).

Since 2001, Carlos Mazuré, Chief Technology Officer, has managed Soitecs's strategic Advanced Technology Development organization. He is tasked with identifying the best new breed of engineered substrates and its applications to help define the future business directions for the company. He works closely with Soitec's customers to help support and open new applications for Soitec's Smart Cut technology. Prior to Soitec, Mazuré served as director of business development at Infineon Technologies AG, and was involved with the IBM/Siemens DRAM Development Alliance. His experience also includes work on SOI and BiCMOS high performance devices and technology development at Motorola Corp. Carlos Mazuré holds two doctorates in physics, one from the University of Grenoble, France, and the other from the Technical University of Munich, Germany. Carlos Mazuré is the author of more than 150 technical papers and holds more than 70 patents worldwide.

Lothar Risch
"Pushing CMOS beyond the Roadmap"

The end of CMOS and of Moore's law was already discussed at feature sizes of about 1μm in the eighties. Today, the 90 nm generation is in production and in spite of many roadblocks, the latest ITRS expects that CMOS can be scaled at least down to the 22 nm node with minimum gate lengths of 9 nm. However, for conventional bulk CMOS serious challenges are evident and new transistors with better electrostatic channel control, lower off currents and higher on currents will be needed. Among them multi-gate devices with very thin silicon channels are most promising. Several architectures like FinFET, wafer bonded double-gate and

SON have been demonstrated with good electrical characteristics at gate lengths of 25-10 nm. From quantum mechanical simulations with idealized source drain doping profiles it is predicted that silicon MOSFETs will be functional down to 2 nm gate length with off currents in the μA/μm range. Multi-gate transistors have also been implemented in high density Flash memory cells down to 20 nm. They achieve large Vt shifts, suitable for multi-level storage. Even single electrons can be detected on the storage node. To summarize, it seems very realistic that the device roadmap will not end at the 22 nm node. Provided that manufacturing and cost issues can be fulfilled, CMOS will dominate also in the nanoelectronics era.

Biography

Lothar Risch received the diploma degree in physics from the Technical University of Berlin in 1974 and the doctor degree from the Technical University of Karlsruhe in 1976. He joined Siemens Corporate Research in Munich in 1977. Since then, he has been engaged in Silicon microelectronics especially in DRAM memory cell development from 4 to 256 Mbit, CMOS logic, and Silicon based nanoelectronics. In 1999 he moved to Infineon Technologies, the former Siemens Semiconductor Group. Now, he is a senior director of the department Corporate Research Nano Devices with the main activity on 30 to 10nm CMOS and memory cells. He filed more than 50 patents and he is also a member of several advisory boards and technical program committees.

H.-S. Philip Wong
"Nanoelectronics: Nanotubes, Nanowires, Molecules and Novel Concepts"

As device sizes approach the nanoscale, new opportunities arise from harnessing the physical and chemical properties at the nanoscale. Chemical synthesis, self-assembly, and templated self-assembly promise the precise fabrication of device structures or even the entire functional entity. Quantum phenomena and one-dimensional transport may lead to new functional devices with very different power/performance tradeoffs. New materials with novel electronic, optical, and mechanical properties emerge as a result of the ability to manipulate matter on a nanoscale. It is now feasible to contemplate new nanoelectronic systems based on new devices with completely new system architectures. This paper will give an overview of the materials, technology, and device opportunities in the nanoscale era. The focus of discussion will be on nanotubes, nanowires, molecular devices, and novel device concepts for nanoelectronics.

Biography

H.-S. Philip Wong joined the IBM T. J. Watson Research Center, Yorktown Heights, New York, in 1988. In September, 2004, he joined Stanford University as Professor of Electrical Engineering. While at IBM, he was Senior Manager of the 60-member Department of Nanoscale Materials, Processes, and Devices. He has the responsibility of shaping and executing IBM's strategy on nanoscale science and technology. Prior to this appointment, he was Senior Manager of the Exploratory Devices and Integration Technology Department. His 54-member department was responsible for defining and executing IBM's exploratory devices and technology roadmap for silicon technology. His research interests are in nanoscale science and technology, semiconductor technology, solid state devices, and electronic imaging. He is interested in exploring new materials, novel fabrication techniques, and novel device concepts for future nanoelectronics systems. Novel devices often require new concepts in circuit and system designs. His research also includes explorations into circuits and systems that are device-driven. He is a Fellow of the IEEE. He is a member of the Emerging Research Devices Working Group of the International Technology Roadmap for Semiconductors (ITRS).

The exhibition includes major scientific publishers as well as suppliers of equipments for characterisation, CAD software, test tools and equipment, etc.

Opening hours:
Tuesday 13 September: 12 am - 5 pm
Wednesday 14 September: 9 am - 5 pm
Thursday 15 September: 9 am - 3 pm

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CIRCUIT EXHIBITION

An exhibition of integrated circuits is organised during all the Conference. Three categories of circuits are considered: education, research, industry. All circuits have been fabricated, through different manufacturing services. The circuit exhibition is sponsored by CMP.

Plots of the circuits as well as information on the circuits (function, origin, etc.) are on display on Tuesday, Wednesday and Thursday at the exhibition area. The authors will be present at their posters for discussions and demonstrations during the Coffee Breaks on Tuesday. A catalogue is available.

For more information, please contact:
Bernard Courtois   bernard.courtois@imag.fr
Hubert Delori   hubert.delori@imag.fr

FRINGE MEETINGS

Lunch and Learn Seminar: Pulsed Characterization of Advanced CMOS Technologies

Date: Wednesday, 14 September, 12:45-14:15 (and 18:00 – 19:00)
Room: Bayard

Organised by:
Keithley

For more information please come to our booth at the exhibition area.

Other Fringe Meetings:
The topic and location of the fringe meetings will be announced at the conference site.

MONDAY, 12 SEPTEMBER
SHORT COURSES

Registration from 8:00 am at :

Alpes Congres - Alpexpo
Avenue d'Innsbruck - BP 2408 - 38034 GRENOBLE - France
Tel. +33 (0) 476 39 66 00 (switch board Alpexo)

Organiser:
Simon Deleonibus CEA-LETI, email: sdeleonibus@cea.fr

Short course 1: New process and device concepts

Chair: F. Balestra, IMEP
Room: Chartreuse

8:50-9:00	**Introduction** - F. Balestra, IMEP
9:00-10:30	**Advanced CMOS Devices on Bulk and SOI: Physics, Modeling and Characterisation** - T. Poiroux, CEA LETI
10:30-10:45	Coffee Break
10:45-12:15	**Alternative CMOS Architectures and ITRS Emerging Research Devices** - HS Philip-Wong, University of Stanford
12:15-13:45	Lunch (Sponsored by NANOCMOS)
13:45-14:45	**High-K Gate Dielectrics** - H. Iwai, Tokyo Inst. of Tech
14:45-15:45	**Ion Implantation Damage and Annealing in Silicon** - K. Jones, University of Florida
15:45-16:00	Coffee Break
16:00-17:00	**New Interconnects Schemes: End of Copper, Optical Interconnects?** - S. Laval, IEF, France

Fees:

Regular: 200 EUR (early), 250 EUR (late)
Students: 150 EUR (early), 200 EUR (late)

Short course 2: Advanced concepts for SOC and SIP

Chair: S. Deleonibus, CEA-LETI
Room: Belle étoile

8:50-9:00	**Introduction** - S. Deleonibus CEA-LETI
9:00-10:30	**SOC and SIP for Heterogeneous System Integration** - R. Mertens, IMEC
10:30-10:45	Coffee Break
10:45-12:15	**System-Level Performance Analysis of Advanced CMOS Technologies** - Philip Christie, Philips
12:15-13:45	Lunch (Sponsored by NANOCMOS)

MONDAY, 12 SEPTEMBER

13:45-14:45	**Advanced SiGeC BICMOS Technology for SoC Integration** - A. Chantre, STMicroelectronics
14:45-15:45	**Embedded Memories** - A. Maurelli, STMicroelectronics
15:45-16:00	Coffee Break
16:00-17:00	**Introducing New Devices on Chip: MEMS, Sensors, etc.** - P. Ancey, STMicroelectronics

Fees:

Regular:	200 EUR (early), 250 EUR (late)
Students:	150 EUR (early), 200 EUR (late)

Short course 3: Nanoelectronics - Beyond the roadmap Emerging research devices

Chair:	G. Baccarani, Univ. Bologna
Room:	Meije

8:50-9:00	**Introduction** - G. Baccarani, Univ. Bologna
9:00-10:00	**Molecular Electronics: Self-Assembly and Organisation, Carbon Nanotubes** - J-P. Bourgoin, CEA
10:00-11:00	**Spin Electronics** - C. Chappert, IEF
11:00-11:15	Coffee Break
11:15-12:15	**Quantum Computing in Quantum Dots** - D. Loss, U. Basel
12:15-13:45	Lunch (Sponsored by NANOCMOS)

Short course 4: Emerging Memory Architectures When will the UNIversal Memory be available?

Chair:	R. Bouchakour, Univ. Marseille
Room:	Meije

12:15-13:45	Lunch (Sponsored by NANOCMOS)
13:50-14:00	**Introduction** - R. Bouchakour, Univ. Marseille
14:00-15:00	**Technology and Key Design Issues for New Memory Devices (Embedded and Stand Alone)** - Kinam Kim, Samsung
15:00-16:00	**FeRAM and MRAM Technologies** - Y. Arimoto, Fujitsu
16:00-16:15	Coffee Break
16:15-17:15	**New Memory Concepts: from Silicon Nanocrystal Memories to Molecular Memories** - B. De Salvo, LETI

Fees (short course 3 + 4):

Regular:	200 EUR (early), 250 EUR (late)
Students:	150 EUR (early), 200 EUR (late)

TUESDAY, 13 SEPTEMBER
SCIENTIFIC PROGRAMME

Introduction and Paper Award 2004

Time: 08:45 - 09:15
Location: Dauphine

Joint Plenary Session

Chairs: S. Cristoloveanu, IMEP (France) ; M. Brillouët, CEA-LETI (France)
Time: 09:15 - 09:55
Location: Dauphine

09:15 **Future Devices for Information Processing**
R. Cavin, V. Zhirnov, Semiconductor Research Corporation, USA

ESSDERC Plenary Session

Chairs: S. Cristoloveanu, IMEP (France) ; M. Brillouët, CEA-LETI (France)
Time: 10:00 - 10:40
Location: Dauphine

10:00 **Engineering Wafers for the Nanotechnology Era**
C. Mazuré, A-J. Auberton-Hervé, SOITEC, France

Coffee Break

Time: 10:40 - 11:00
Location: Alpes Congès

SESSION 1.A. : Multi - Gate Devices

Chairs: M. Jurczak, IMEC (Belgium) ; P. Stolk, Philips Crolles (France)
Time: 11:05 - 12:45
Location: Dauphine

1A1
11:05 **3-D Thermal Modeling of FinFET**
R. Joshi, IBM, USA; J. Pascual-Gutiérrez, Purdue University, USA;
K. Chuang, IBM, USA

1A2
11:25 **Immunity to Substrate Effect in Advanced Ω-FET Devices**
R. Ritzenthaler, O. Faynot, C. Jahan, A. Kuriyama, L. Brévard, CEA-LETI,
France; S. Cristoloveanu, IMEP, France; S. Deleonibus, CEA-LETI, France

1A3
11:45 **Specific Features of the Capacitance and Mobility Behaviors in
FinFET Structures**
T. Rudenko, Institute of Semiconductor Physics, National Academy
of Sciences, Ukraine; V. Kilchytska, Universite Catholique de Louvain,
Belgium; N. Collaert, S. Gendt, R. Rooyackers, M. Jurczak,
InterUniversity Microelectronics Center, Belgium; D. Flandre,
Universite Catholique de Louvain, Belgium

1A4
12:05 **Evidence for Reduction of Noise and Radiation Effects in G[4]-FET
Depletion-All-Around Operation**
K. Akarvardar, S. Cristoloveanu, IMEP, France; B. Dufrene, IBM, USA;
P. Gentil, IMEP, France; R. Schrimpf, Vanderbilt University, USA;
B. Blalock, University of Tennessee, USA; J. Chroboczek, IMEP, France;
M. Mojarradi, JPL, USA

1A5

12:25 **Tunneling and Intersubband Coupling in Ultra-Thin Body Double-Gate MOSFETs**

V. Sverdlov, Institute for Microelectronics, TU Vienna, Austria; A. Gehring, AMD Saxony LLC & Co. KG, Germany; H. Kosina, S. Selberherr, Institute for Microelectronics, TU Vienna, Austria

SESSION 1.B. : Gate Stack

Chairs: J. Hooker, Philips Leuven (Belgium) ; R. Beck, Warsaw University of Technology (Poland)

Time: **11:05 - 12:45**

Location: Oisans

1B1

11:05 **Germanium/HfO_2/TiN Gate Stacks for Advanced Nodes: Influence of Surface Preparation on MOS Capacitor Characteristics**

C. Le Royer, X. Garros, C. Tabone, L. Clavelier, CEA-LETI, France; Y. Morand, STMicroelectronics, France; J. Hartmann, CEA-LETI, France; Y. Campidelli, O. Kermarrec, ST Microelectronics, France; V. Loup, E. Martinez, O. Renault, B. Guigues, CEA-LETI, France; V. Cosnier, ST Microelectronics, France; S. Deleonibus, CEA-LETI, France

1B2

11:25 **The Effect of Metal Thickness, Overlayer and High-k Surface Treatment on the Effective Work Function of Metal Electrode**

K. Choi, H. Wen, SEMATECH, USA; H. Alshareef, TI, SEMATECH, USA; R. Harris, P. Lysaght, H. Luan, P. Majhi, B. Lee, SEMATECH, USA

1B3

11:45 **Mixed-Signal and Noise Properties of nMOSFETs with HfSiON/TaN Gate Stacks**

C. Rittersma, Philips Research Leuven, Belgium; E. Simoen, P. Srinivasan, IMEC, Belgium; M. Vertregt, Philips Research, The Netherlands; C. Claeys, IMEC, Belgium

1B4

12:05 **Work Function Control of Metal Gates by Interdiffused Ni-Ta with High Thermal Stability**

T. Matsukawa, Y. Liu, M. Masahara, K. Endo, K. Ishii, H. Yamauchi, E. Sugimata, H. Takashima, E. Suzuki, S. Kanemaru, Nanoeletronics Reseach Inst., AIST, Japan

1B5

12:25 **PLAsma Doping for S/D Extensions: Device Integration, Gate Oxide Reliability and Dynamic Behavior**

B. Dumont, STMicroelectronics, France; A. Pouydebasque, Philips Semiconductors, France; F. Lallement, D. Lenoble, G. Ribes, J. Roux, STMicroelectronics, France; S. Vanbergue, Philips Semiconductors, France; T. Skotnicki, STMicroelectronics, France

SESSION 1.C. : RF Devices

Chairs: P. Ashburn, University of Southampton (United Kingdom) ; S. Decoutere, IMEC (Belgium)

Time: **11:05 - 12:45**

Location: Sept Laux

1C1

11:05 **High-Performance Varactor Diodes Integrated in a Silicon-on-Glass Technology**
K. Buisman, HiTec, Delft University of Technology, The Netherlands; L. Nanver, T. Scholtes, H. Schellevis, ECTM, Delft University of Technology, The Netherlands; L. de Vreede, HiTec, Delft University of Technology, The Netherlands

1C2

11:25 **Three-dimensional 35 nF/mm² MIM Capacitors Integrated in BiCMOS Technology**
A. Bajolet, ST Microelectronics / IMEP-INPG, France; J. Giraudin, C. Rossato, L. Pinzelli, S. Bruyère, S. Crémer, T. Jagueneau, P. Delpech, ST Microelectronics, France; L. Montès, IMEP-INPG, France; G. Ghibaudo, IMEP, France

1C3

11:45 **Comparison of two Types of Lateral DMOSFET Optimized for RF Power Applications**
D. Muller, J. Mourier, A. Perrotin, B. Szelag, A. Monroy, STMicroelectronics, France

1C4

12:05 **Deep Trench Isolation Effect on Self-Heating and RF Performances of SiGeC HBTs**
B. Barbalat, T. Schwartzmann, P. Chevalier, T. Jagueneau, B. Vandelle, L. Rubaldo, F. Saguin, STMicroelectronics, France; F. Aniel, IEF, France; A. Chantre, STMicroelectronics, France

1C5

12:25 **Investigation of Fully- and Partially-Depleted Self-Aligned SiGeC HBTs on Thin Film SOI**
G. Avenier, P. Chevalier, B. Vandelle, D. Lenoble, F. Saguin, STMicroelectronics, France; S. Frégonese, T. Zimmer, IXL Bordeaux, France; A. Chantre, STMicroelectronics, France

SESSION 1.D. : Compact Modeling

Chairs: H. Jaouen, STMicroelectronics Crolles (France) ; K. McCarthy, University College Cork (Ireland)
Time: 11:05 - 12:45
Location: Stendhal

1D1

11:05 **Quantum Short-Channel Compact Modeling of Drain-Current in Double-Gate MOSFET**
D. Munteanu, J. Autran, X. Loussier, L2MP-CNRS, France; S. Harrison, R. Cerutti, T. Skotnicki, ST Microelectronics, France

1D2

11:25 **Compact Modeling of Anomalous High Frequency Behavior of MOSFET's Small-Signal NQS Parameters in Presence of Velocity Saturation**
A. Roy, J. Sallese, EPFL, Switzerland; C. Enz, CSEM, EPFL, Switzerland

1D3

11:45 **Compact Modeling of Electrical, Thermal and Optical LED Behavior**
P. Baureis, University of Applied Sciences, Wuerzburg, Germany

TUESDAY, 13 SEPTEMBER

1D4

12:05 **A Closed-Form Charge-Based Expression for Drain Current in Symmetric and Asymmetric Double Gate MOSFET**
A. Roy, EPFL, Switzerland; J. Sallese, EFPL, Switzerland; C. Enz, CSEM,EPFL, Switzerland

1D5

12:25 **Base-Collector Junction Charge Investigation of Si/SiGe HBT on Thin Film SOI**
S. Frégonese, IXL, France; G. Avenier, STMicroelectronics, France; C. Maneux, IXL, France; A. Chantre, STMicroelectronics, France; T. Zimmer, IXL, France

Lunch

Time: **12:45 - 14:10**
Location: Les Ecrins

Joint Plenary Session

Chairs: M. Steyaert, Katholieke Universiteit Leuven (Belgium) ; W. Redman-White, Philips Semiconductors (UK)
Time: **14:15 - 14:55**
Location: Dauphine

14:15 **Silicon Nano-Photonics: Where the Photons Meet the Electrons**
E. Yablonovitch, Electrical Engineering Department, University of California, USA

SESSION 2.A. : Nano-Scaled Devices

Chairs: G. Iannaccone, University of Pisa (Italy) ; L. Risch, Infineon (Germany)
Time: **15:00 - 16:40**
Location: Chartreuse

2A1

15:00 **Nanotechnology: Potential Challenger to Silicon CMOS? (Invited)**
B. Yu, NASA Ames Reserach Center, USA; M. Meyyappan, NASA Ames Research Center, USA

2A2

15:20 **Quantum-Mechanical Analysis of the Electrostatics in Silicon-Nanowire and Carbon-Nanotube FETs**
E. Gnani, A. Marchi, S. Reggiani, M. Rudan, G. Baccarani, ARCES - University of Bologna, Italy

2A3

15:40 **Trade-off between Electron Velocity and Density of States in Ballistic Nano-MOSFETs**
M. De Michielis, D. Esseni, F. Driussi, DIEGM, Univ. of Udine, Italy

2A4

16:00 **Monte Carlo Simulations of Sub-100 nm InGaAs MOSFETs for Digital Applications**
K. Kalna, University of Glasgow, UK; L. Yang, Cadence Ltd., China; A. Asenov, University of Glasgow, UK

2A5

16:20   **The 65nm Tunneling Field Effect Transistor (TFET) 0.68 μm² 6T Memory Cell and Multi-V$_{th}$ Device**
T. Nirschl, Infineon Technologies, Germany; S. Henzler, J. Fischer, A. Bargagli-Stoffi, M. Fulde, M. Sterkel, Technical University Munich, Germany; U. Schaper, G. Georgakos, Infineon Technologies, Germany; D. Schmitt-Landsiedel, Technical University Munich, Germany

SESSION 2.B. : Dynamic Random Access Memories

Chairs: P. Erratico, STMicroelectronics Agrate (Italy) ; S. Okhonin, Innovative Silicon (Switzerland)

Time: **15:00 - 16:40**

Location: Belle étoile

2B1

15:00   **High-Density Low-Power-Operating DRAM Device Adopting 6F2 Cell Scheme with Novel S-RCAT Structure on 80nm Feature Size**
H. Oh, J. Kim, J. Kim, S. Park, D. Kim, S. Kim, D. Woo, Y. Lee, G. Ha, J. Park, N. Kang, H. Kim, Y. Hwang, B. Kim, D. Kim, Y. Choi, J. Choi, B. Lee, S. Kim, M. Cho, Y. Kim, J. Choi, D. Shin, M. Shim, W. Choi, G. Lee, Y. Park, W. Lee, B. Ryu, Samsung Electronics Co, Korea

2B2

15:20   **Advanced Memory Concepts for DRAM and Nonvolatile Memories (Invited)**
F. Horiguchi, Toyo University, Japan

2B3

15:40   **Data Retention Analysis on Individual Cells of 256Mb DRAM in 110nm Technology**
A. Weber, Infineon Technologies / TU Harburg, Germany; A. Birner, Infineon Technologies, Germany; W. Krautschneider, TU Harburg, Germany

2B4

16:00   **Enhancement of Data Retention Time in DRAM using Step gaTed AsymmetRic (STAR) Cell Transistors**
M. Jang, M. Seo, Y. Kim, S. Cha, S. Park, S. Pyi, J. Jeong, S. Hong, S. Park, Hynix Semiconductor Inc., Korea

2B5

16:20   **Analysis of the NAND-type DRAM-on-SGT for High-Density and Low-Voltage Memory**
H. Nakamura, I. Pesic, H. Sakuraba, F. Masuoka, Research Institute of Electrical Communication, Tohoku University, Japan

SESSION 2.C. : High- and Medium-K Characterisation

Chairs: S. Bengtsson, Chalmers University (Sweden) ; G. Groeseneken, IMEC (Belgium)

Time: **15:00 - 16:20**

Location: Meije

2C1

15:00 **Polarity Dependence of Bias Temperature Instabilities in Hf(x)Si (1-x) ON/TaN Gate Stacks**
M. Aoulaiche, M. Houssa, R. Degraeve, G. Groeseneken, S. De Gendt, M. Heyns, IMEC, Belgium

2C2

15:20 **The Role of Nitrogen Incorporation in Hf-based High-k Dielectrics: Reduction in Electron Charge Traps**
N. Umezawa, National Institute for Materials Science, Japan; K. Shiraishi, Univ. of Tsukuba, Japan; K. Torii, Semiconductor Leading Edge Technology Inc., Japan; T. Chikyow, National Institute for Materials Science, Japan; H. Watanabe, Osaka Univ., Japan; K. Yamabe, Univ. of Tsukuba, Japan; T. Ohno, Institute for Materials Science, Japan; K. Yamada, Waseda Univ., Japan; Y. Nara, Semiconductor Leading Edge Technology Inc., Japan; M. Boero, Univ. of Tsukuba, Japan

2C3

15:40 **Effects of Plasma Nitridation on the Electrical Properties of Nitrided Oxide Gate Dielectric for DRAM Application**
J. Heo, D. Kim, B. Koo, J. Kim, C. Kim, Y. Noh, S. Baek, Y. Shin, U. Chung, Samsung Electronics Co., Korea

2C4

16:00 **A New Method Based on Charge Pumping Technique to Extract the Lateral Profiles of Localized Charge Trapping in Nitride**
H. Pang, L. Pan, L. Sun, Y. Zeng, Z. Zhang, J. Zhu, Institute of Microelectronics, Tsinghua University, China

SESSION 2.D. : Nanowires

Chairs: M. Sanquer, CEA (France) ; O. Engström, Chalmers University (Sweden)
Time: **15:00 - 16:40**
Location: Sept Laux

2D1

15:00 **Analytical Model for Nanowire and Nanotube Transistors Covering both Dissipative and Ballistic Transport**
G. Mugnaini, G. Iannaccone, University of Pisa, Italy

2D2

15:20 **High Performance ZnO Nanowire Field Effect Transistor**
S. Cha, J. Jang, Y. Choi, G. Ho, D. Kang, D. Hasko, M. Welland, G. Amaratunga, University of Cambridge, UK

2D3

15:40 **Impact of Point Defect Location in Nanowire Silicon MOSFETs**
M. Bescond, University of Glasgow, UK; N. Cavassilas, K. Nehari, J. Autran, M. Lannoo, L2MP UMR CNRS 6137, France; A. Asenov, University of Glasgow, UK

2D4

16:00 **Detection of Individual Traps in Silicon Nanowire Transistors**
M. Hofheinz, X. Jehl, M. Sanquer, G. Molas, M. Vinet, S. Deleonibus, CEA Grenoble, France

2D5

16:20 **Influence of Band-Structure on Electron Ballistic Transport in Silicon Nanowire MOSFET's: an Atomistic Study**
K. Nehari, N. Cavassilas, J. Autran, L2MP-CNRS, France; M. Bescond, University of Glasgow, UK; D. Munteanu, M. Lannoo, L2MP-CNRS, France

Coffee Break

Time: **16:40 - 17:00**
Location: Salle de Réception

RUMP SESSION: Where will the revolutionary solutions come from: technology or design?

Time: **17:00 - 18:30**
Location: Dauphine

Moderators : T. Skotnicki (STMicroelectronics, France) , A. Kaiser (IEMN, France)

ESSDERC Panelists :
- Hiroshi IWAI (Tokyo Institute of Technology, Japan)
- Rainer WASER (RWTH-Aachen, Germany)
- Kazunari ISHIMARU (SoC R&D Center, TOSHIBA Corp., Japan)
- Peter ZEITZOFF (SEMATECH, USA)

ESSCIRC Panelists:
- Clive BITTLESTONE (Texas Instruments, USA)
- Georges GIELEN (K.U. Leuven, Belgium)
- Sreedhar NATARAJAN (Emerging Memory Technologies, Canada)
- Yannis TSIVIDIS (Columbia University, USA)

This rump session brings together eight international experts in technology/devices and advanced design. Each panelist represents a different area of the technology or design: from CMOS manufacturing and advanced Si devices to nanoelectronics beyond CMOS, from analog & RF to memory and CAD. Short presentations are given to stimulate questions and comments from the audience. What are the bottlenecks? What are the perspectives for breakthrough solutions? Will they come from the technology/device side, from the design side, or from both?

Welcome Reception at the "Musée de Grenoble"

Time: 19:00

Joint Plenary Session

Chairs: C. Enz, CSEM (Switzerland) ; E. Perea, STMicroelectronics (France)
Time: **09:00 - 09:40**
Location: Dauphine

09:00 **Terahertz Technology: Devices and Applications**
M. Shur, ECSE Department and Broadband Center, Rensselaer Polytechnic Institute, USA

SESSION 3.A. : RF and Power SOI

Chairs: M. Östling, KTH (Sweden) ; J. Burghartz, DIMES (The Netherlands)
Time: **09:45 - 11:05**
Location: Chartreuse

3A1
09:45 **Efficient Crosstalk Reduction Using Very Low Resistivity SOI Substrate**
J. Ankarcrona, L. Vestling, K. Eklund, J. Olsson, Uppsala University, Sweden

3A2
10:05 **SOA Improvement of P-Channel High-Voltage SOI Devices**
S. Schwantes, M. Graf, V. Dudek, Atmel Germany, Germany

3A3
10:25 **SOI CMOS Technology for RF/Analog Applications - Active/Passive Devices and New Crosstalk Isolation Technology (Invited)**
R. Huang, G. Zhang, H. Liao, L. Yang, T. Yan, Y. Zhou, X. Zhang, Y. Wang, Institute of Microelectronics, Peking University, China

3A4
10:45 **Temperature Dependence of Avalanche Multiplication in Submicron Silicon Devices**
D. Massey, J. David, G. Rees, Department of Electronic and Electrical Engineering, University of Sheffield, UK

SESSION 3.B. : Nanoscale and Organic Devices

Chairs: P. Heremans, IMEC (Belgium) ; E. Cantatore, Philips Leuven (Belgium)
Time: **09:45 - 11:05**
Location: Sept Laux

3B1
09:45 **Digital Logic Using Magnetic Nanostructures (Invited)**
R. Cowburn, Imperial College London, Blackett Physics Laboratory, UK

3B2
10:05 **Modelling of Polymer Schottky Diodes for Real Device Applications**
M. Raja, N. Sedghi, B. Eccleston, S. Badriya, S. Higgins, University of Liverpool, UK; G. Lloyd, Merck Chemicals Ltd, UK

3B3

10:25   **High-Speed InP-based Resonant Tunnelling Diode on Silicon Substrate**
W. Prost, V. Khorenko, University Duisburg-Essen, Germany; A. Mofor, A. Bakin, Technical University Braunschweig, Germany; E. Khorenko, S. Ehrich, University Duisburg-Essen, Germany; H. Wehmann, A. Schlachetzki, Technical University Braunschweig, Germany; F. Tegude, University Duisburg-Essen, Germany

3B4

10:45   **Organic CuTCNQ Non-Volatile Memories for Integration in the CMOS Backend-of-Line: Preparation from Gas/Solid Reaction and Downscaling to an Area of 0.25 μm^2**
R. Müller, S. De Jonge, K. Myny, D. Wouters, J. Genoe, P. Heremans, IMEC, Belgium

SESSION 3.C. : Back-End Characterisation and Reliability

Chairs: G. Ghibaudo, IMEP (France) ; J-L. Autran, Université d'Aix-Marseille (France)
Time: **09:45 - 11:05**
Location: Meije

3C1

09:45   **Characterization and Modeling of Al_2O_3 MIM Capacitors: Temperature and Electrical Field Effects**
S. Bécu, S. Crémer, O. Noblanc, ST Microelectronics, France; J. Autran, L2MP, UMR CNRS 6137, France; P. Delpech, ST Microelectronics, France

3C2

10:05   **Precise Analogue Characterization of MIM Capacitors Using an Improved Charge-Based Capacitance Measurement (CBCM) Technique**
Z. Ning, H. Delecourt, L. De Schepper, R. Gillon, M. Tack, AMI Semiconductor, Belgium

3C3

10:25   **Distinction of Intrinsic and Extrinsic Breakdown Failure Modes of Cu/Low-k Interconnects**
N. Hwang, Institute of Microelectronics, Singapore; T. Tan, C. Gan, Nanyang Technological University, Singapore

3C4

10:45   **Magnetic Sensing as Signal Integrity Monitoring in Integrated Circuits**
E. Gutierrez INAOE / INTEL, Mexico; E. Torres, R. Torres, INAOE, Mexico

SESSION 3.D. : Transport in Novel Materials

Chairs: E. Sangiorgi, University of Bologna (Italy) ; G. Le Carval, CEA-LETI (France)
Time: **09:45 - 11:05**
Location: Belle étoile

3D1
09:45 **Strained Si/SiGe MOSFET Capacitance Modeling Based on Band Structure Analysis**
F. Gilibert, STMicroelectronics/L2MP, France; D. Rideau, STMicroelectronics, France; F. Payet, STMicroelectronics/L2MP, France; F. Boeuf, E. Batail, M. Minondo, STMicroelectronics, France; R. Bouchakour, L2MP, France; T. Skotnicki, H. Jaouen, STMicroelectronics, France

3D2
10:05 **Physics and Modeling of Ge-On-Insulator MOSFETs (Invited)**
A. Chin, H. Kao, Y. Tseng, D. Yu, C. Chen, National Chiao-Tung Univ., Taiwan; S. McAlister, National Research Council of Canada, Canada; C. Chi, National Tsing Hua Univ., Taiwan

3D3
10:25 **Variations of Hole Mass in p-MOSFETs under Process-Induced Mechanical Stress**
T. Guillaume, M. Mouis, IMEP, France

3D4
10:45 **A Semi-Empirical Surface Scattering Model for Quantum Corrected Monte Carlo Simulation of Strained Si-nMOSFETs**
A. Pham, C. Nguyen, C. Jungemann, B. Meinerzhagen, NST, TU-Braunschweig, Germany

Coffee Break (Sponsored by Mentor Graphics)
Time: **11:05 - 11:25**
Location: Salle de Réception

SESSION 4.A. : Strain Engineering
Chairs: K. Ishimaru, Toshiba (Japan) ; S. Koester, IBM (USA)
Time: **11:25 - 12:45**
Location: Chartreuse

4A1
11:25 **In-Depth Study of Strained SGOI nMOSFETs down to 30nm Gate Length**
F. Andrieu, T. Ernst, O. Faynot, O. Rozeau, CEA-LETI, France; Y. Bogumilowicz, STMicroelectronics, France; J. Hartmann, L. Brévard, A. Toffoli, D. Lafond, H. Dansas, CEA-LETI, France; B. Ghyselen, SOITEC, France; F. Fournel, CEA-LETI, France; G. Ghibaudo, IMEP, France; S. Deleonibus, CEA-LETI, France

4A2
11:45 **On the Scalability of Source/Drain Current Enhancement in Thin Film sSOI**
E. Augendre, G. Eneman, A. De Keersgieter, V. Simons, I. De Wolf, J. Ramos, IMEC, Belgium; B. Pawlak, Philips Research Leuven, Belgium; L. Fei, MEMC, USA; M. Goodwin, Texas Instruments, USA; S. Brus, S. Severi, F. Leys, E. Sleeckx, S. Locorotondo, M. Ercken, J. de Marneffe, IMEC, Belgium; M. Seacrist, B. Kellerman, MEMC, USA; M. Goodwin, Texas Instruments, USA; K. De Meyer, M. Jurczak, S. Biesemans, IMEC, Belgium

4A3

12:05   **A Highly Robust SiGe Source Drain Technology Realized by Disposable Sidewall Spacer (DSW) for 65nm Node and Beyond**
Y. Kim, T. Mori, Y. Hayami, T. Yamamoto, H. Morioka, H. Kokura, K. Kawamura, Y. Shimamune, A. Katakami, A. Hatada, M. Shima, N. Tamura, H. Ohta, T. Sakuma, M. Kojima, M. Nakaishi, T. Sugii, M. Miyajima, Fujitsu Limited, Japan

4A4

12:25   **High Performance Device Utilizing Ultra-Thick-Strained-Si (UTSS) Grown on Relaxed SiGe**
S. Lee, Y. Kim, Y. Lee, J. Lee, I. Jung, D. Lee, Y. Shin, U. Chung, J. Moon, Samsung Electronics, Korea

SESSION 4.B. : Non-Volatile Memories I

Chairs: S. Hall, University of Liverpool (UK) ; A. Schenk, Integrated Systems Laboratory (Switzerland)
Time: **11:25 - 12:45**
Location: Belle étoile

4B1

11:25   μ **Trench Phase-Change Memory Cell Engineering and Optimization**
A. Pirovano, F. Pellizzer, A. Redaelli, I. Tortorelli, E. Varesi, F. Ottogalli, T. Marangon, A. Lacaita, R. Bez, STMicroelectronics, Italy; M. Tosi, P. Besana, R. Cecchini, R. Piva, M. Magistretti, M. Scaravaggi, G. Mazzone, P. Petruzza, F. Bedeschi, A. Modelli, ST Microelectronics, Italy; D. Ielmini, DEI, Politecnico di Milano, Italy

4B2

11:45   **Gate Current in Stacked Dielectrics for Advanced FLASH EEPROM cells**
F. Driussi, S. Marcuzzi, P. Palestri, L. Selmi, University of Udine, Italy

4B3

12:05   **Anomalous Charge Loss of Reference Cell in MLC Flash Memory Due to Process-Induced Mobile Ion**
S. Sim, W. Kwon, H. Lee, J. Han, S. Jeon, B. Lee, J. Kim, J. Han, B. Yoon, W. Lee, C. Park, K. Kim, Samsung Electronics, Korea

4B4

12:25   **High Work-Function Metal Gate and High-K Dielectrics for Charge Trap Flash Memory Device Applications**
S. Jeon, J. Han, J. Lee, C. Choi, Samsung Advanced Institute of Technology, Korea; S. Choi, H. Hwang, Gwangju Institute of Science and Technology, Korea; C. Kim, Samsung Advanced Institute of Technology, Korea

SESSION 4.C. : Noise and Fluctuations in Nanometer MOSFETs

Chairs: A. De Keersgieter, IMEC (Belgium) ; M. Rudan, University of Bologna (Italy)
Time: **11:25 - 12:45**
Location: Meije

4C1

11:25   **Do Hot Electrons Produce Excess Noise?**
C. Jungemann, B. Meinerzhagen, NST, TU Braunschweig, Germany

4C2

11:45   **A Physics-Based Low Frequency Noise Model for MOSFETs under Periodic Large Signal Excitation**
R. Brederlow, Infineon, Germany; J. Koh, Samsung, Korea; R. Thewes, Infineon, Germany

4C3

12:05   **Simulation of Combined Sources of Intrinsic Parameter Fluctuations in a 'Real' 35 nm MOSFET**
G. Roy, F. Adamu-Lema, A. Brown, S. Roy, A. Asenov, Glasgow University, UK

4C4

12:25   **Convergence of the Legendre Polynomial Expansion of the Boltzmann Equation for Nanoscale Devices**
C. Jungemann, NST, TU Braunschweig, Germany; M. Bollhoefer, TU Berlin, Germany; B. Meinerzhagen, NST, TU Braunschweig, Germany

Lunch

Time: **12:45 - 14:10**
Location: Les Ecrins

Joint Plenary Session

Chairs: H. Iwai, Tokyo Institute of Technology (Japan) ; F. Balestra, IMEP (France)
Time: **14:15 - 14:55**
Location: Dauphine

14:15   **Future of CMOS Technology, Manufacturing and Products**
M. Thompson, STMicroelectronics, France

ESSDERC Plenary Session

Chairs: H. Iwai, Tokyo Institute of Technology (Japan) ; F. Balestra, IMEP (France)
Time: **15:00 - 15:40**
Location: Dauphine

15:00   **Nanoelectronics: Nanotubes, Nanowires, Molecules, and Novel Concepts**
H.-S. P. Wong, Center for Integrated Systems and Department of Electrical Engineering, Stanford University, USA

Coffee Break (Sponsored by Mentor Graphics)

Time: **15:40 - 16:00**
Location: Alpes Congrès

SESSION 5.A. : Biological and Optical Devices

Chairs: R. Thewes, Infineon (Germany) ; R. Mertens, IMEC (Belgium)
Time: **16:00 - 17:40**
Location: Stendhal

5A1

16:00 **BioMEMS in Medicine: Diagnostic and Therapeutic Systems (Invited)**
K. Cheung, P. Renaud, EPFL, Switzerland

5A2

16:20 **Genetically-Engineered Whole-Cell Bioreporters on Integrated Circuits for Very Low-Level Chemical Sensing**
S. Islam, B. Weathers, M. Zhang, B. Blalock, S. Ripp, G. Sayler, S. Terry, S. Caylor, University of Tennessee, USA

5A3

16:40 **Large-Area Avalanche Diodes for Picosecond Time-Correlated Photon Counting**
A. Gulinatti, I. Rech, Politecnico di Milano, Dipartimento di Elettronica e Informazione, Italy; P. Maccagnani, IMM-CNR, Italy; M. Ghioni, S. Cova, Politecnico di Milano, Dipartimento di Elettronica e Informazione, Italy

5A4

17:00 **The Effect of Dislocation Loops on the Light Emission of Silicon LEDs**
T. Hoang, P. Leminh, J. Holleman, J. Schmitz, University of Twente, The Netherlands

5A5

17:20 **Detection of THz Electromagnetic Radiation with Si/SiGe HFET**
S. Richard, N. Zerounian, P. Boucaud, IEF, Université Paris-Sud 11, France; J. Ortega, LURE, Université Paris-Sud 11, France; T. Hackbarth, H. Herzog, DaimlerChrysler Research Center, Germany; F. Aniel, IEF, Université Paris-Sud 11, France

SESSION 5.B. : High-K Dielectrics

Chairs: A. Bauer, FhG, Erlangen (Germany) ; E. Augendre, IMEC (Belgium)
Time: **16:00 - 18:00**
Location: Oisans

5B1

16:00 **Mobility Enhancement of High-k Gate Stacks through Reduced Transient Charging**
P. Kirsch, J. Sim, S. Song, S. Krishnan, J. Peterson, H. Li, M. Quevedo-Lopez, C. Young, R. Choi, N. Moumen, P. Majhi, SEMATECH, USA; Q. Wang, J. Ekerdt, The University of Texas, USA; G. Bersuker, B. Lee, SEMATECH, USA

5B2

16:20 **Investigation on the Compositionally Graded Hf_xAl_yOz Films for TiN Based DRAM Capacitor**
D. Kil, K. Hong, S. Yeom, H. Song, K. Park, J. Roh, N. Kwak, H. Sohn, J. Kim, S. Park, Hynix, Korea

5B3

16:40 **Scalability and Reliability of $TaN/HfN/HfO_2$ Gate Stacks Fabricated by a High Temperature Process**
J. Kang, Peking University, China; H. Yu, IMEC, Belgium; C. Ren, National University of Singapore, Singapore; H. Yang, N. Sa, X. Liu, R. Han, Peking University, China; M. Li, D. Chan, National University of Singapore, Singapore; D. Kwong, The University of Texas, USA

WEDNESDAY, 14 SEPTEMBER

5B4

17:00 **Accurate Investigation of the High-k Soft Phonon Scattering Mechanism in Metal Gate MOSFETs**
O. Weber, M. Cassé, L. Thévenod, CEA-LETI, France; F. Ducroquet, CEA-LETI/CNRS, France; T. Ernst, CEA-LETI, France; B. Guillaumot, STMicroelectronics, France; S. Deleonibus, CEA-LETI, France

5B5

17:20 **Suppression of Chemical Phase Separation in High-k Zirconium an Hafnium Nitro-Silicate and Alumino-Silicate Alloys for CMOS Applications**
G. Lucovsky, NC State University, USA; J. Phillips, Rutgers University, USA; J. Whitten, NC State University, USA

5B6

17:40 **The Effect of Y_2O_3 Buffer Layer for La_2O_3 Gate Dielectric Film**
K. Nakagawa, K. Miyauchi, K. Kakushima, T. Hattori, Frontier Collaborative Research Center, Tokyo Institute of Technology, Japan; K. Tsutsui, Interdisciplinary Graduate School of Sci, and Eng., Tokyo Institute of Technology, Japan; H. Iwai, Frontier Collaborative Research Center, Tokyo Institute of Technology, Japan

SESSION 5.C. : Oxide Reliability and ESD

Chairs: R. Woltjer, Philips Leuven (The Netherlands) ; J. Schmitz, University of Twente (The Netherlands)
Time: 16:00 - 18:00
Location: Dauphine

5C1

16:00 **MOS Gate Current Characteristics and their Implications for Lifetime Area Scaling**
S. Kleff, R. Bottini, G. Ghidini, STMicroelectronics, Italy

5C2

16:20 **Effect of Hot Carrier Stress on the Performance, Trap Densities and Transient Behavior of SLS ELA TFTs**
D. Kouvatsos, Institute of Microelectronics, NCSR Demokritos, Greece; G. Papaioannou, M. Exarchos, L. Michalas, Solid State Section, Physics Department, University of Athens, Greece; A. Voutsas, LCD Process Technology Laboratory, Sharp Labs, USA

5C3

16:40 **New Perspectives on NBTI in Advanced Technologies: Modelling and Characterization**
M. Denais, STMicroelectronics, France; V. Huard, Philips Semiconductors, France; C. Parthasarathy, G. Ribes, STMicroelectronics, France; F. Perrier, Philips semiconductors, France; D. Roy, STMicroelectronics, France; A. Bravaix, L2MP-ISEM, France

5C4

17:00 **Modeling MOSFET and Circuit Degradation through SPICE**
A. Cester, S. Gerardin, A. Paccagnella, University of Padova, Italy; G. Ghidini, ST Microelectronics, Agrate Brianza, Italy

5C5

17:20 **Charge Trapping Effects and Interface State Generation in a 40V Lateral Resurf pDMOS Transistor**

P. Moens, AMI Semiconductor BVBA, Belgium; G. Van den Bosch, IMEC, Belgium; D. Wojciechowski, F. Bauwens, AMI Semiconductor, Belgium; H. De Vleeschouwer, AMI Semiconductor, Bhutan; F. De Pestel, AMI Semiconductor, Belgium

5C6

17:40 **Predictive Device Simulation for ESD Protection Structures Validated with Transient Interferometric Thermal-Mapping Experiments**

S. Reggiani, E. Gnani, M. Rudan, G. Baccarani, ARCES University of Bologna, Italy; S. Bychikhin, J. Kuzmik, D. Pogany, E. Gornik, Inst. for Solid State Electronics- TU Vienna, Austria; M. Denison, N. Jensen, Infineon Technologies AG, Germany; G. Groos, Univ. of the Federal Armed Forces Munich, Germany; M. Stecher, Infineon Technologies AG, Germany

Gala dinner at the PRISME Seyssins

Time: 19:30

(Bus departure from Alpexpo at 19:00)

VILLE DE SEYSSINS

LA **METRO.**

Nodules-based memory for tomorrow…

Joint Plenary Session

Chairs: T. Skotnicki, STMicroelectronics (France) ; A. Ionescu, EPFL (Switzerland)

Time: 09:00 - 09:40

Location: Dauphine

09:00 **Towards a Molecule - Computer? Resources and Technologies to Compute within a Single Molecule**
C. Joachim, NanoSciences Group, CEMES/CNRS, France

ESSDERC Plenary Session

Chairs: T. Skotnicki, STMicroelectronics (France) ; A. Ionescu, EPFL (Switzerland)

Time: 09:45 - 10:25

Location: Dauphine

09:45 **Pushing CMOS beyond the Roadmap**
L. Risch, Infineon Technologies, Germany

Coffee Break

Time: 10:25 - 10:45

Location: Alpes Congrès

SESSION 6.A. : CMOS Technology

Chairs: T. Ernst, CEA-LETI (France) ; E. Dubois, IEMN (France)

Time: 10:45 - 12:45

Location: Dauphine

6A1

10:45 **Interaction of Middle-of-Line (MOL) Temperature and Mechanical Stress on 90nm High-Speed Device Performance and Reliability**
K. Lim, Chartered Semiconductor Manufacturing Ltd, Singapore; V. Chan, R. Rengarajan, H. Lee, N. Rovedo, IBM, USA; E. Lim, Chartered Semiconductor Manufacturing Ltd, Singapore; S. Yang, F. Jamin, P. Nguyen, IBM, USA; W. Lin, C. Lai, Y. Teh, J. Lee, L. Kim, Chartered Semiconductor Manufacturing Ltd, Singapore; Z. Luo, H. Ng, IBM, USA; J. Sudijono, Chartered Semiconductor Manufacturing Ltd, Singapore; C. Wann, IBM, USA; I. Yang, IBM, Singapore

6A2
11:05 **CMOS Integration of Solid Phase Epitaxy for sub-50nm Devices**
A. Pouydebasque, Philips Semiconductors, France; B. Dumont, STMicroelectronics, France; R. El-Farhane, Philips Semiconductors, France; A. Halimaoui, STMicroelectronics, France; C. Laviron, CEA-LETI, France; D. Lenoble, C. Rossato, N. Cassanova, STMicroelectronics, France; V. Carron, CEA-LETI, France; S. Pokrant, Philips Semiconductors, France; T. Skotnicki, STMicroelectronics, France

6A3
11:25 **65nm LP/GP Mix Low Cost Platform for Multi-Media Wireless and Consumer Applications**
B. Tavel, B. Duriez, Philips Semiconductors, France; R. Gwoziecki, CEA-LETI, France; *et al*

6A4
11:45 **Silicidation Induced Strain Phenomena in TOtally SIlicided (TOSI) Gate transistors**
A. Mondot, STMicroelectronics, France; M. Müller, Philips Semiconductor, France; D. Aimé, B. Froment, F. Cacho, A. Talbot, F. Leverd, M. Rivoire, Y. Morand, STMicroelectronics, France; S. Descombes, P. Besson, A. Toffoli, CEA-LETI, France; S. Pokrant, T. Skotnicki, STMicroelectronics, France

6A5
12:05 **Demonstration of High Performance Transistors with PVD Metal Gate**
H. Harris, AMD, USA; H. Wen, K. Choi, SEMATECH, USA; H. Alshareef, TI, USA; H. Luan, Infineon, USA; Y. Senzaki, C. Young, S. Song, SEMATECH, USA; Z. Zhang, TI, USA; G. Bersuker, P. Majhi, B. Lee, Sematech, USA

6A6
12:25 **Insight on Physics of Hf-based Dielectrics Reliability**
G. Ribes, M. Denais, S. Bruyère, D. Roy, F. Monsieur, V. Huard, C. Parthasarathy, STMicroelectronics, France; M. Müller, Philips, France; T. Skotnicki, STMicroelectronics, France; G. Ghibaudo, IMEP, France

SESSION 6.B. : Advanced Process Steps Integration

Chairs: F. Arnaud, STMicroelectronics Crolles (France) ; S. Deleonibus, CEA-LETI (France)
Time: **10:45 - 12:45**
Location: Oisans

6B1
10:45 **Intrinsic Limitations for CMOS with High-k Gate Dielectrics: Electrically-Active Grain Boundary and Oxygen Atom Defect States (Invited)**
G. Lucovsky, NC State University, USA; J. Lüning, Stanford Synchrotron Research Center, USA

6B2
11:05 **Minimization of the MuGFET Contact Resistance by Integration of NiSi Contacts on Epitaxially Raised Source/Drain Regions**
A. Dixit, R. Rooyackers, F. Leys, IMEC, Belgium; M. Kaiser, R. Weemaes, Philips, The Netherlands; I. Ferain, A. De Keersgieter, N. Collaert, K. Anil, IMEC, Belgium; R. Surdeanu, Philips, Belgium; M. Goodwin, Texas Instruments, USA; P. Zimmermann, Intel, USA; R. Loo, M. Caymax, M. Jurczak, S. Biesemans, K. De Meyer, K.U. Leuven, IMEC, Belgium

THURSDAY, 15 SEPTEMBER

6B3
11:25 **Scalability of Strained Nitride Capping Layers for Future CMOS Generations**
G. Eneman, M. Jurczak, P. Verheyen, T. Hoffmann, A. De Keersgieter, K. De Meyer, IMEC, Belgium

6B4
11:45 **CMP-Less Integration of 40nm-Gate TOtally SIlicided (TOSI) Bulk Transistors Using Selective S/D Si Epitaxy and Ultra-Low Gates**
M. Müller, Philips Semiconductors, France; A. Mondot, D. Aimé, B. Froment, A. Talbot, J. Roux, G. Ribes, Y. Morand, T. Skotnicki, S. Descombes, P. Gouraud, F. Leverd, STMicroelectronics, France; A. Toffoli, CEA-LETI, France; S. Pokrant, Philips Semiconductors, France

6B5
12:05 **Schottky Barrier Height Modulation Using Dopant Segregation in Schottky-Barrier SOI-MOSFETs**
M. Zhang, J. Knoch, Q. Zhao, S. Lenk, Institute of Thin Films and Interfaces, ISG-1 IT, Research Center Juelich, Germany; U. Breuer, Zentralabteilung fuer Chemische Analysen, Research Center Juelich, Germany; S. Mantl, Institute of Thin Films and Interfaces, ISG-1 IT, Research Center Juelich, Germany

6B6
12:25 **Base-Contact Proximity Effects in Bipolar Transistors with Nitride-Spacer Technology**
H. van Zeijl, L. Nanver, DIMES, The Netherlands

SESSION 6.C. : Power and HV Devices
Chairs: M. Stoisiek, University of Erlangen (Germany) ; O. Noblanc, STMicroelectronics Crolles (France)
Time: **10:45 - 12:45**
Location: Stendhal

6C1
10:45 **Characterization of Dynamic SOA of Power MOSFETs Limited by Electrothermal Breakdown**
G. Van en Bosch, IMEC, Belgium; D. Wojciechowski, AMI Semiconductor Belgium, Belgium; B. Elattari, IMEC, Belgium; P. Moens, AMI Semiconductor Belgium, Belgium; G. Groeseneken, IMEC, Belgium

6C2
11:05 **LDMOS Modeling for Analog and RF Circuit Design**
A. Canepari, STMicroelectronics, France; G. Bertrand, STMicroelecronics, France; A. Giry, M. Minondo, F. Blanchet, H. Jaouen, B. Reynard, N. Jourdan, STMicroelectronics, France; J. Chante, CEGELY, INSA, France

6C3
11:25 **Monolithic Bidirectional Switch (MBS) - A Novel MOS-Based Power Device**
M. Baus, M. Ali, O. Winkler, B. Spangenberg, Institut fuer Halbleitertechnik, RWTH Aachen University, Germany; M. Lemme, AMICA, AMO GmbH, Germany; H. Kurz, Institut fuer Halbleitertechnik, RWTH Aachen University, Germany

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6C4

11:45 **Low Switching Losses Devices Architectures for Power Management Applications Integrated in a Low Cost 0.13μm CMOS technology**
C. Grelu, ST Crolles/INSA LPM, France; N. Baboux, INSA LPM, France; R. Bianchi, ST Crolles, France; C. Plossu, INSA LPM, France

6C5

12:05 **The Impact of Channel Engineering on the Performance and Reliability of LDMOS Transistors**
N. Mohapatra, K. Ehwald, R. Barth, H. Ruecker, D. Bolze, P. Schley, D. Schmidt, H. Wulf, IHP, Germany

6C6

12:25 **Integration of Substrate-Isolated High Voltage Devices in Junction Isolated Technologies**
S. Pendharkar, Texas Instruments Inc, USA

Lunch

Time: **12:45 - 14:10**
Location: Les Ecrins

Presentation ESSDERC-ESSCIRC 2006

Time: **14:15 - 14:25**
Location: Dauphine

Joint Plenary Session

Chairs: A. Kaiser, IEMN-ISEN (France) ; A. Wild, Freescale (USA)
Time: **14:25 - 15:05**
Location: Dauphine

14:25 **Silicon Forever! Really?**
H. Stormer, Department of Physics and Department of Applied Physics and Applied Mathematics, Columbia University and Bell Labs, Lucent Technologies, USA

SESSION 7.A. : Advanced Numerical Methods

Chairs: R. Clerc, IMEP (France) ; T. Grasser, TU Wien (Austria)
Time: **15:10 - 16:30**
Location: Chartreuse

7A1

15:10 **A New Method to Calculate Leakage Current and its Applications for sub-45nm MOSFETs**
G. Lujan, W. Magnus, B. Sorée, IMEC, Belgium; M. Pourghaderi, IMEC, KU Leuven, Belgium; A. Veloso, IMEC, Belgium; M. van Dal, Philips Research LEuven, Belgium; A. Lauwers, S. Kubicek, IMEC, Belgium; S. De Gendt, IMEC, KU Leuven, Belgium; M. Heyns, IMEC, Belgium; K. De Meyer, IMEC, KU Leuven, Belgium

THURSDAY, 15 SEPTEMBER

7A2

15:30　**Finite Element Simulation of Thermomechanical Stress Evolution in Cu/Low-k Interconnects during Manufacturing and Subsequent Thermal Cycling**
N. Chérault, Centre des Matériaux - ENSMP / STMicroelectronics, France; J. Besson, Centre des Matériaux - ENSMP, France; C. Goldberg, Freescale Semiconductor, France; N. Casanova, STMicroelectronics, France; M. Berger, Centre des Matériaux - ENSMP, France

7A3

15:50　**Simulation and Characterization of High-Frequency Performances of Advanced MIM Capacitors**
J. Piquet, LAHC, France; O. Cueto, CEA, France; F. Charlet, SILVACO, France; M. Thomas, STMicroelectronics, France; C. Bermond, LAHC, France; A. Farcy, J. Torres, STMicroelectronics, France; B. Flechet, LAHC, France

7A4

16:10　**Wavelet-Based Adaptive Mesh Generation for Device Simulation**
L. De Marchi, F. Franze', DEIS-University of Bologna, Italy; E. Baravelli, ARCES-University of Bologna, Italy; N. Speciale, DEIS-University of Bologna, Italy

SESSION 7.B. : Non-Volatile Memories II

Chairs:　G. Baccarani, University of Bologna (Italy) ; R. Bez, STMicroelectronics Agrate (Italy)
Time:　**15:10 - 16:30**
Location:　Belle étoile

7B1

15:10　**AC-SONOS: A Single-Poly, Assist-Charge Induced Source-Side-Injection SONOS Low Power Nonvolatile Memory**
M. Lee, J. Wu, Macronix International Co.,Ltd., Taiwan; M. Kuo, Macronix International Co.,Ltd., Togo; T. Hsu, H. Lung, Macronix International Co.,Ltd., Taiwan; T. Huang, National Chiao Tung University, Taiwan; R. Liu, Macronix International Co.,Ltd., Sudan; C. Lu, Macronix International Co.,Ltd., Taiwan

7B2

15:30　**Experimental and Theoretical Study of Layered Tunnel Barriers for Nonvolatile Memories**
J. Buckley, B. De Salvo, G. Molas, M. Gély, S. Deleonibus, CEA/LETI, France

7B3

15:50　**Advanced Ring Type Contact Technology for High Density Phase Change Memory**
Y. Song, J. Park, S. Lee, J. Park, Y. Hwang, S. Lee, K. Ryoo, S. Ahn, C. Jeong, J. Shin, W. Jeong, K. Koh, G. Jeong, H. Jeong, K. Kim, Samsung Electronics, Korea

7B4

16:10　**Improvement of the Current-Voltage Characteristics of a Tunneling Dielectric by Barrier Engineering by Adopting an Atomic-Layer-Deposited SiN Layer for Flash Memory Applications**
S. Hong, J. Jang, T. Park, D. Jeong, M. Kim, C. Hwang, School of Materials Science and Engineering, Seoul National University, Korea

SESSION 7.C. : Strained Si Characterisation and Reliability

Chairs: J. Mueller, Freescale Crolles (USA) ; H. Brut, STMicroelectronics Crolles (France)

Time: 15:10 - 16:30

Location: Meije

7C1

15:10 **Extraction of Physical Parameters of Strained-Silicon MOSFETs from C-V Measurement**
K. Chandrasekaran, X. Zhou, S. Chiah, W. Shangguan, G. See, Nanyang Technological University, Singapore; L. Bera, N. Balasubramanian, S. Rustagi, Institute of Microelectronics, Singapore

7C2

15:30 **Low Temperature Characterization of Effective Mobility in Uniaxially and Biaxially Strained N-MOSFETs**
F. Lime, IMEP, France; F. Andrieu, LETI-CEA, France; J. Derix, G. Ghibaudo, IMEP, France; F. Boeuf, T. Skotnicki, ST, France

7C3

15:50 **Impact of Strain and Strain-Relaxation on the Low-Frequency Noise of SRB Silicon n-MOSFETs**
E. Simoen, G. Eneman, C. Claeys, P. Verheyen, R. Delhougne, R. Loo, K. De Meyer, IMEC, Belgium

7C4

16:10 **STI-Induced Damage and Hot-Carrier Reliability in the Narrow Width Short Channel NMOSFET Fabricated Using Global Strained-Si Technology**
W. Phua, National University of Singapore, Singapore; D. Ang, Nanyang Technological University, Singapore; C. Ling, K. Chui, National University of Singapore, Singapore

Coffee Break

Time: 16:30 - 16:40

Location: Salle de réception

SESSION 8.A. : Carbon Nanotube Devices

Chairs: M. Macucci, University of Pisa (Italy) ; G. Le Blevennec, CEA (France)

Time: 16:40 - 17:40

Location: Chartreuse

8A1

16:40 **Three-Dimensional Atomistic Simulation of Carbon Nanotube FETs with Realistic Geometry**
G. Fiori, G. Iannaccone, University of Pisa, Italy; M. Lundstrom, G. Klimeck, Purdue University, USA

8A2

17:00 **Improving DC and AC Characteristics of Ohmic Contact Carbon Nanotube Field Effect Transistors**
M. Pourfath, H. Kosina, Institute for Microelectronics, TU-Vienna, Austria; B. Cheong, CSE Lab, SAIT, Korea; W. Park, Materials and Devices Lab, SAIT, Korea; S. Selberherr, Institute for Microelectronics, TU-Vienna, Austria

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8A3

17:20 **Nanoscale Capacitors Base on Metal-Insulator-Carbon Nanotube-Metal (MICNM) Structures**
J. Jang, S. Cha, Y. Choi, D. Kang, D. Hasko, G. Amaratunga, University of Cambridge, UK

SESSION 8.B. : High-Speed Memories

Chairs: R. Brederlow, Infineon (Germany) ; H. Ishiwara, Tokyo Institute of Technology (Japan)
Time: 16:40 - 17:40
Location: Belle étoile

8B1

16:40 **65nm High Performance SRAM Technology with 25F2, 0.16μm² S3 (Stacked Single-Crystal Si) SRAM Cell, and Stacked Peripheral SSTFT for Ultra High Density and High Speed Applications**
H. Lim, S. Jung, Y. Rah, T. Ha, H. Park, C. Chang, W. Cho, J. Park, B. Son, J. Jeong, H. Cho, B. Choi, K. Kim, Samsung Electronics Co. Ltd., Korea

8B2

17:00 **UTB SOI SRAM Cell Stability under the Influence of Intrinsic Parameter Fluctuation**
K. Samsudin, B. Cheng, A. R. Brown, S. Roy, A. Asenov, Glasgow University, UK

8B3

17:20 **A SrRuO₃/IrO₂ Top Electrode FeRAM with Cu BEOL Process for Embedded Memory of 130nm Generation and Beyond**
Y. Kumura, T. Ozaki, I. Kunishima, A. Nitayama, H. Kanaya, O. Hidaka, Y. Shimojo, S. Shuto, Y. Yamada, K. Tomioka, K. Yamakawa, S. Yamazaki, D. Takashima, T. Miyakawa, S. Shiratake, Semiconductor Company, Toshiba Corporation, Japan; S. Ohtsuki, Toshiba Microelectronics Corporation, Japan

SESSION 8.C. : Mobility Extraction

Chairs: H. Przewlocki, ITE Warsow (Poland) ; L. Selmi, University of Udine (Italy)
Time: 16:40 - 17:40
Location: Meije

8C1

16:40 **Influence of Ballistic and Pocket Effects on Electron Mobility in Si MOSFETs**
J. Lusakowski, W. Knap, Y. Meziani, J. Cesso, A. El Fatimy, R. Tauk, N. Dyakonova, Université Montpellier, France; G. Ghibaudo, IMEP, ENSERG, France; F. Boef, ST Microelectronics, France; T. Skotnicki, STMicroelectronics, France

8C2

17:00 **Experimental Validation of a New Analytical Model for the Position-Dependent Hall Voltage in Semiconductor Devices**
M. Rudan, S. Reggiani, E. Gnani, G. Baccarani, ARCES - University of Bologna, Italy; C. Corvasce, D. Barlini, M. Ciappa, W. Fichtner, Integrated Systems Laboratory ETHZ - Zurich, Switzerland; M. Denison, N. Jensen, M. Stecher, Infineon Technologies, Germany; G. Groos, Univ. of the Federal Armed Forces Munich, Germany

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THURSDAY, 15 SEPTEMBER

8C3

17:20 **Magnetoresistance Technique for Mobility Extraction in Short Channel FDSOI Transistors**
W. Chaisantikulwat, M. Mouis, G. Ghibaudo, IMEP, France; C. Gallon, C. Fenouillet-Beranger, STMicroelectronics, France; D. Maude, Grenoble High Magnetic Field Laboratory, France; T. Skotnicki, STMicroelectronics, France; S. Cristoloveanu, IMEP, France

Closing Session

Time: **17:40 - 18:00**
Location: Dauphine

DECON 2005 ECS Satellite Symposium

"Crystalline Defects and Contamination: Their Impact and Control in Device Manufacturing IV"

Thursday, 15 September, 2pm & Friday, 16 September, 9am - 5pm

Room: Sept-Laux

For more information, see *Programme ESSCIRC, pages 40-41 -* **Friday, 16 September.**

Farewell party at the Bastille

Time: 19:30

FRIDAY, 16 SEPTEMBER
WORKSHOPS

See Programme ESSCIRC, pages 40-47.

DECON 2005 ECS Satellite Symposium
"Crystalline Defects and Contamination:
Their Impact and Control in Device Manufacturing IV"

SINANO Workshop
"Nanoscale CMOS and Emerging Post-CMOS Logic and Memory Nanodevices"

MOS-AK Workshop
"Principles and Practice of the Compact Modeling and its Standardisation"

SDR/Cognitive Radio:
"Software Defined Radio : Theory, Design and Applications"

MIMOSA Workshop
"Invisible Electronics for Ambient Intelligence Applications"

ENIAC Workshop
"Nanoelectronics Technologies 2020: a European Strategic Research Agenda"

FRIDAY, 16 SEPTEMBER
TECHNICAL VISITS

ESSDERC-ESSCIRC'05 organises two technical visits exclusively for participants and accompanying persons. The visits consist of a short presentation providing an overview of the companies' activities, followed by a clean room visit. Participants can choose between STMicroelectronics or Soitec. The visits will end with an overlook of the new MINATEC center and the European Synchrotron Radiation Facility in Grenoble.

STMicroelectronics is a global independent semiconductor company and is a leader in developing and delivering semiconductor solutions across the spectrum of microelectronics applications. Crolles1 (STM) and Crolles2 (Alliance between STM, Philips and Freescale) Fabs, located at 20 Km from Grenoble, are well known for the creation and validation of high-level System-on-Chip (SoC) intellectual property (IP) blocks.

Created in 1992 by two researchers, André-Jacques Auberton-Hervé and Jean-Michel Lamure from CEA-LETI, **SOITEC** is an example of a successful move from fundamental lab research to worldwide industrial leadership in the innovative and highly competitive domain of SOI materials.

Please note that for organisation reasons, registration to the technical visits must be completed before 15 August 2005.

Registration fee: 30 EUR (please use registration form)

SOITEC

PROGRAMME ESSCIRC

ESSDERC ESSCIRC

31sh European Solid-State Circuits Conference

12 - 16 September 2005 - Grenoble, France

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TUESDAY, 13 SEPTEMBER 2005

Time			
08:45	Introduction and Paper Award 2004 *(Dauphine)*		
09:15 - 09:55	Joint Plenary Session - R. Cavin *(Dauphine)*		
10:00	SESSION 1.E. : DC/DC Converters *(Chartreuse)*	SESSION 1.F. :Amplifiers beyond 10 GHz *(Belle étoile)*	SESSION 1.G. : Synthesizer Building Blocks *(Meije)*
11:00	Coffee Break *(Salle de Réception)*		
11:25	SESSION 2.E. : Analog Signal Processing *(Chartreuse)*	SESSION 2.F. : Short Range Communications *(Belle étoile)*	SESSION 2.G. : Low Power and High Performance Digital Circuits *(Meije)*
12:45	Lunch Break *(Salon les Ecrins)*		
14:15 - 14:55	Joint Plenary Session - E. Yablonovitch *(Dauphine)*		
15:00	ESSCIRC Plenary Session - L. Larson *(Dauphine)*		
15:40	Coffee Break *(Alpes Congrès - exhibtion area)*		
16:00	SESSION 3.E. : High Resolution Data Converters *(Dauphine)*	SESSION 3.F. : PLLs *(Oisans)*	SESSION 3.G. : Clocking and Synchronisation *(Stendhal)*
17:00	RUMP SESSION: Where will the Revolutionary Solutions come from: Technology or Design? *(Dauphine)*		
18:30	End of conference day		
19:00	Welcome Reception *(Musée de Grenoble)*		

WEDNESDAY, 14 SEPTEMBER 2005

Time			
09:00 - 09:40	Joint Plenary Session - M. Shur *(Dauphine)*		
09:45	ESSCIRC Plenary Session - B. Nauta *(Dauphine)*		
10:25	Coffee Break *(Alpes Congrès - exhibtion area)*		
10:45	SESSION 4.E. : DSP Building Blocks *(Dauphine)*	SESSION 4.F. : RF Circuits *(Oisans)*	SESSION 4.G. : Amplifiers *(Stendhal)*
12:45	Lunch Break *(Salon les Ecrins)*		
14:15 - 14:55	Joint Plenary Session - M. Thompson *(Dauphine)*		
15:00	SESSION 5.E. : Ultra Wide Band *(Chartreuse)*	SESSION 5.F. : Sensor Interfaces *(Belle étoile)*	SESSION 5.G. : Test of Digital Circuits and Memory *(Meije)* — SESSION 5.H. : Linear High Voltage Circuits *(Sept Laux)*
16:00	Coffee Break *(Salle de Réception)*		
16:20	SESSION 6.E. : Continuous Time Filters *(Chartreuse)*	SESSION 6.F. : Sensor Integration *(Belle étoile)*	SESSION 6.G. : Memory Circuits *(Meije)*
18:00	End of conference day		
19:00	Gala Dinner		

THURSDAY, 15 SEPTEMBER 2005

Time			
09:00 - 09:40	Joint Plenary Session - C. Joachim *(Dauphine)*		
09:45	SESSION 7.E. : Analogue Circuits for Communications *(Chartreuse)*	SESSION 7.F. : VCOs *(Belle étoile)*	SESSION 7.G. : Crypto Systems *(Meije)* — SESSION 7.H. : Imagers 1 *(Sept Laux)*
10:45	Coffee Break *(Salle de Réception)*		
11:05	SESSION 8.E. : High Speed Optical Interfaces *(Chartreuse)*	SESSION 8.F. : Oversampled Data Converters *(Belle étoile)*	SESSION 8.G. : Digital Power Supply & Wiring *(Meije)* — SESSION 8.H. : Imagers 2 *(Sept Laux)*
12:45	Lunch Break *(Salon les Ecrins)*		
14:15	Presentation ESSDERC-ESSCIRC 2006 *(Dauphine)*		
14:25 - 15:05	Joint Plenary Session - H. Stormer *(Dauphine)*		
15:10	ESSCIRC Plenary Session - B. Gammel, S. Rüping *(Dauphine)*		
15:50	Coffee Break *(Alpes Congrès - exhibtion area)*		
16:10	SESSION 9.E. : Analog Circuits *(Dauphine)*	SESSION 9.F. : Cellular Communications *(Oisans)*	SESSION 9.G. : High Speed ADCs *(Stendhal)*
17:40	Closing Session *(Dauphine)*		
18:00	End of conference day		
19:30	Farewell Party		

WELCOME

The 31st European Solid-State Circuits Conference takes place in Grenoble from Tuesday 13 September to Thursday 15 September 2005. The aim of the conference is to provide an annual European forum for the presentation and discussion of recent advances in solid-state circuit design and integration. ESSCIRC 2005 is jointly organized with the 35th European Solid-State Device Research Conference (ESSDERC). The initiative to merge the two sister conferences was started in 2002, as an incentive to foster the necessary interaction among technologists, device experts, and circuit & system designers.

While keeping separate Technical Programme Committees, ESSDERC and ESSCIRC are governed by a single Steering Committee and share plenary keynote presentations, tutorials (September 12) and satellite workshops (September 16) bridging both communities. Participants registered for either conference are encouraged to attend any of the scheduled parallel sessions.

ESSDERC-ESSCIRC is the largest and best quality European meeting related to micro and nano electronics. In order to guarantee the excellence of the scientific level, the Steering Committee has imposed a very strict acceptance rate (40%). The evaluation of submitted papers has also been improved and new functionalities enabled in the web submission system. A total number of 288 papers were submitted to ESSCIRC, representing a positive trend. More than 30 countries, from all continents, were represented with substantial participations from Europe, USA, Japan and Korea. The final programme of ESSCIRC 2005 includes 119 contributions with outstanding plenary and session invited talks. ESSCIRC 2005 covers all areas of integrated circuit design: analog and RF circuits, data converters, digital circuits, DSP and memories, mixed-signal circuits, imagers, sensors, systems-on-chip, advanced design concepts and revolutionary architectures.

Several innovations are introduced this year in Grenoble: a joint panel session, session invited talks, paper exchange with DATE, an exhibit and technical visits (Friday September 16). Our conference has a new logo. A Special Issue of the Journal of Solid-State Circuits will contain selected full-length papers. Grenoble will not miss the opportunity to preserve and develop the tradition of a warm Social Programme: the Welcome Reception at the Museum of Grenoble (Tuesday evening), the Gala Dinner and Show on Wednesday evening and, finally, the Farewell Party (Thursday evening) at the scenic Bastille location which overlooks Grenoble area and mountains. The accompanying persons will enjoy several excursions. Grenoble is a high-tech city, with wonderful surroundings in the heart of the Alps, offering attractive opportunities for an extended stay over the weekend.

We would like to thank the authors for their contributions, the members of the Technical Programme Committee, Steering Committee and Local Organizing Committee for their hard work, Mrs Iris Mazuré our omnipresent conference secretary, and our generous sponsors.

We are looking forward to a successful conference, with exciting scientific contents and rich human interactions. We warmly welcome you and your colleagues in Grenoble.

Sorin Cristoloveanu, Conference Chair
Michel Brillouët, Conference Co-Chair
Andreas Kaiser, ESSCIRC Technical Programme Chair

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Further information

For further information about the conference please contact the conference secretariat:

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Or visit the web page: **http://www.esscirc2005.com**

Giant C_{2005}^{09} nanotubes in Grenoble.

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Michael	Moyal	Consultant (D)
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Gérard Ghibaudo	IMEP - INPG (F)
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Frédéric Petrot	TIMA/SLS - INPG (F)
Marc Renaudin	TIMA - INPG (F)
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Patrice Senn	France Telecom R&D (F)

GENERAL INFORMATION

About Grenoble, hotels, visa, ...
See Programme ESSDERC, page 7 and 8

CONFERENCE SITE

How to get there ...
See Programme ESSDERC, page 9 and 10

CONFERENCE REGISTRATION

Fees for the Conference, Tutorials, Workshops, Tours, ...
See Programme ESSDERC, page 13 and 14

CONFERENCE INFORMATION

Guidelines for oral presentations, web service, ...
See Programme ESSDERC, page 15

SOCIAL PROGRAMME

Not to be missed ...
See Programme ESSDERC, page 16

ACCOMPANYING PERSONS PROGRAMME

Three tours available ...
See Programme ESSDERC, page 17

EXHIBITORS

The Exhibition includes major scientific publishers and suppliers of equipment/software.
See Programme ESSDERC, page 21 and 22

TECHNICAL VISITS

Friday, 16 september: STMicroelectronics or SOITEC, MINATEC, etc
See Programme ESSDERC, page 48

MAP CONFERENCE FACILITIES

Alpes Congres and Alpexpo are connected by an inner passage.

First Floor conference rooms Alpexpo
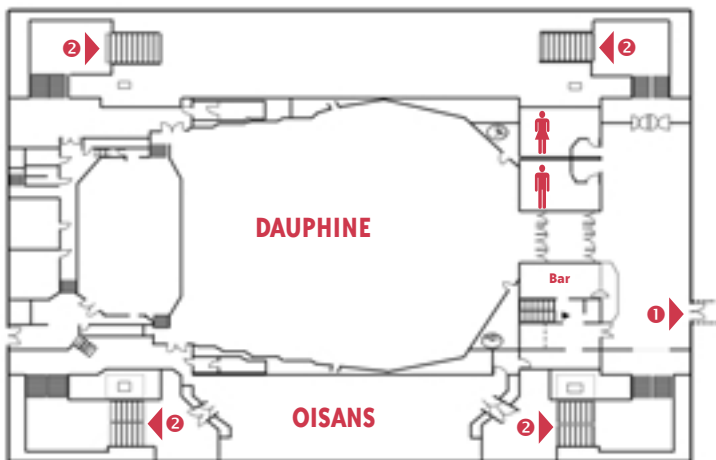

Passage to conference rooms
ALPES CONGRES

LES BANS

Entrance
ALPEXPO

Passage to
conference rooms
ALPES CONGRES

MEIJE

PELVOUX

SALLE DE RECEPTION
(Coffee Break)

SEPT LAUX

BELLE-ETOILE

CHARTREUSE
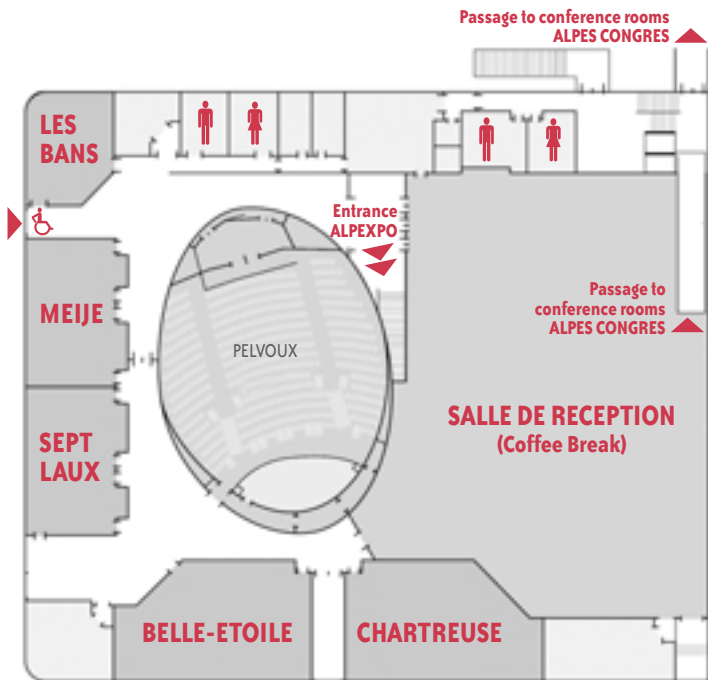
MAP CONFERENCE FACILITIES

Ground Floor conference rooms Alpes Congrès

Main entrance ALPES CONGRES
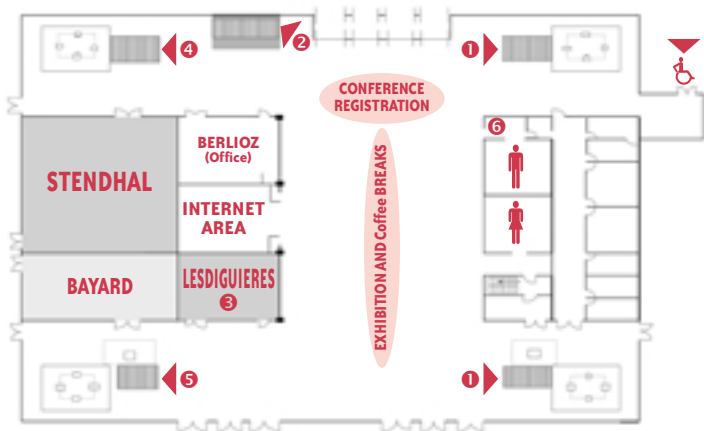
- ❶ To Dauphine and Oisans
- ❷ Downstairs to lunch area (Salon Les Ecrins)
- ❸ Speakers room
- ❹ To Daupine
- ❺ To Oisans
- ❻ Telephone

First Floor conference rooms Alpes Congrès

- ❶ Passage to Alpexpo
- ❷ Downstairs to Conference Registration, Exhibition & Coffe Break

ESSDERC-ESSCIRC
JOINT PLENARY TALKS

Horst Stormer
"Silicon Forever! Really?"

With certainty scaling in silicon is going to hit a wall, technologically or economically. While we don't know exactly when this is going to happen, "approximately a decade from now" is a pretty common guess. Hence it is prudent to imagine and investigate alternative ways to create electronic systems that may have a chance to lead us "beyond silicon". At present there is no clear path at all. Only open-minded and imaginative research has a chance to overcome the foreseeable impasse. One of these "crazy ideas" may just pan out; just like using semiconductors instead of vacuum tubes or the printing of interconnects instead of using copper wires.

Biography

Horst Stormer received his Ph.D. in 1977 from the University of Stuttgart and joined Bell Labs as a postdoc shortly after. From 1983 to 1992 he headed the Semiconductor Physics Research Department and became the Director of the Physical Research Laboratory of AT&T Bell Labs in 1992. In 1997 Stormer moved to Adjunct Physics Director at Bell Labs and became a Professor in the Physics and the Applied Physics Department of Columbia University in New York. Stormer has worked extensively on the properties of lower-dimensional electron systems and is one of the Scientific Directors of the Columbia NSF Nano Center. H. Stormer received the Nobel Prize in Physics in 1998.

Eli Yablonovitch
"Silicon Nano-Photonics: Where the Photons Meet the Electrons"

It has become apparent that silicon technology can provide many of the requirements for nanophotonic integration, including many of the common discrete opto-electronic components. Some of these components are based on photonic crystal designs, but generally electromagnetic design becomes the main research requirement in nano-photonics. The question has always been what is the exact structure that should be fabricated? The era of purely intuitive design may be obsolete.

We must now concentrate more on design software, rational design, and the numerical solution of inverse problems. There are a number of inverse algorithms, including genetic algorithms, the errorpropagation method, and simulated annealing that can contribute to future progress in nanophotonic design.

Biography

Eli Yablonovitch graduated with the Ph.D. degree in Applied Physics from Harvard University in 1972. He worked for two years at Bell Telephone Laboratories, and then became a Professor of Applied Physics at Harvard. In 1979 he joined Exxon to do research on photovoltaic solar energy. Then in 1984, he joined Bell

ESSDERC-ESSCIRC
JOINT PLENARY TALKS

Communications Research, where he was a Distinguished Member of Staff, and also Director of Solid-State Physics Research. In 1992 he joined the University of California, Los Angeles, where he is Professor of Electrical Engineering. He is a Fellow of the Institute of Electrical and Electronic Engineers, the Optical Society of America, and the American Physical Society. Yablonovitch is a Life Member of Eta Kappa Nu, and a Member of the National Academy of Engineering and the National Academy of Sciences.

Michael Shur
"Terahertz Electronics: Devices, Circuits, and Applications"

Transistors with nanometer critical feature sizes, such as HBTs and HEMTs, relying on ballistic transport in semiconductors with small electron effective masses and on innovative designs minimizing parasitics, are penetrating the subterahertz range, still being dominated by two terminal devices. New ideas of using plasma resonances for tunable detection and emission of terahertz radiation are being explored. Plasma effects in polarization-induced electrons and holes in 2D and 1D pyroelectric heterostructures hold promise of an active THz medium. The development of tunable solid state monolithically integrated THz sources and detectors based on these approaches will enable many applications ranging from detection of biological hazardous agents and explosives to medical diagnostics, contactless in-situ testing of integrated circuits, and applications in spectroscopy, radioastronomy and environmental control.

Biography

Michael Shur received his M. S. E. E. degree (with honors) from LETI in 1965, Ph. D. in Physics from A. F. Ioffe Institute in 1967 and Doctor of Science degree from A. F. Ioffe in 1992. He is now Patricia W. and C. Sheldon Roberts'48 Professor of Solid State Electronics, Professor of Physics, and Director of Broadband Data Transport Center at Rensselaer Polytechnic Institute. He is a Fellow of IEEE, of American Physical Society, and of ECS and a member of Eta Kappa Nu, Sigma Xi, Tau Beta Pi, ASEE, and Humboldt Society of America. Dr. Shur is Editor-in-Chief of IJHSES and of the book series on Special Topics in Electronics and Systems.

Ralph Cavin
"Limits of CMOS Devices and Circuits"

Current CMOS devices operate at about six orders of magnitude above the $kT\ln(2)$ joules/bit switching limit imposed by physics. Nevertheless, it can be shown that continued scaling of device features that are then densely packed and operated at attainable frequencies will result in the generation of thermal loads that cannot be managed by any known heat removal technology. We discuss possible successor/complementary logic devices that reduce the level

of heat generation and we especially focus on new non-volatile memory techniques that could radically impact information processing architectures and hence the performance requirements for logic devices.

Biography

Dr. Cavin received his BSEE (1961) and MSEE (1962) from Mississippi State University and his PhD in Electrical Engineering from Auburn University in 1968. He served as a Senior Engineer at the Martin-Marietta Company in Orlando, Florida from 1962 -1965. At Martin, Dr. Cavin was involved in the design and manufacture of missile guidance and control systems. After taking his Ph.D., Dr. Cavin joined the Department of Electrical Engineering at Texas A & M University where he obtained the rank of Full Professor and also served the department as Assistant Head for Research. In 1983, he joined the Semiconductor Research Corporation where he served as Director of Design Sciences research programs until 1989. He became Head of the Department of Electrical and Computer Engineering at North Carolina State University from 1989 - 1994 and was Dean of Engineering at North Carolina State University from 1994 - 1995. He is currently Vice President for Research Operations at the Semiconductor Research Corporation.

Mike Thompson
"Future of CMOS Technology, Manufacturing and Products"

Over the last couple of years, there has been a shift away from the traditional situation where CMOS IC designs and their applications were being limited in their scope by the capability of the available manufacturing technology. The jump to 300mm manufacturing at 90nm and below seems to be turning this phenomenon on its head by offering staggering integration densities and massive production capacities that are becoming much more difficult for designers to exploit due to the shear complexity of the product and application developments. In this talk, we will review some of the likely adaptations of the present design and manufacturing approaches that will allow the gap to be closed.

Biography

Mike Thompson was born in Glasgow, Scotland, in 1957. After graduating from the University of Glasgow with a Bsc Hons in Astronomy with Advanced Mathematics, he started working in 1980 at General Instrument Microelectronics at Glenrothes (Scotland) as a Photolithography Engineer. In 1982, he joined Inmos Ltd at Newport (South Wales, UK), a 100mm wafer fab specialising in high performance memories and microprocessors, that was acquired in 1989 to become SGS-THOMSON Ltd, where he worked until 1991 as Process Development Manager and Engineering Manager. Then in 1991, he left the UK

for France, to work at STMicroelectronics Crolles, ST's first 200 mm wafer fab, where he was appointed Operations Director. Mike Thompson was involved in the first process technology development collaboration between STMicroelectronics and Philips from its start in 1992, as well as in the creation of the STMicroelectronics-France Telecom-CEA/Leti Centre Commun. Today, he has the double responsibility of managing the 200mm wafer fab and contributing to the start-up of Crolles 2, the new 300mm state-of-the-art facility, specialising in high performance technologies for system-on-chip.

Christian Joachim
"Towards a Molecule - Computer? "

There is another world down where miniature machines do not result from a miniaturisation process but from the monumentalisation of the molecular structure. What about assembling machines atom by atom, and stopping at the minimum number of atoms required for the machine to compute, carry, and communicate...? We will present the design of the first prototype of uni-molecular moleculemachines like a wheelbarrow, a Morse manipulator, a Wheatstone bridge, an OR and AND intramolecular logic gate and an atomic wire mould. Some experimental results will be given. Then, we discuss the next step: the design of very complex machines like a full computing unit integrated inside a single molecule.

Biography

Dr. Christian Joachim is Director of Research at CNRS and head of the molecular Nanoscience and Picotechnology group in CEMES/CNRS, Toulouse. His recent accomplishments are the theory of atomic and molecular manipulation with the STM, the discovery of long range tunnel processes through a molecule, the fabrication of metal-insulator-metal planar nanojunctions for the planar implementation of molecular devices and the discovery of the first molecular rotor. More recently, he introduced the concept of mono-molecular electronics, of tunnel wired molecular nano-robots with the design of the first molecular wheelbarrow and is now developing atomic scale technology. He is the author of more than 170 scientific publications and has presented more than 180 talks. Dr. Joachim received the 1988 French Chemical Physics Prize for his work on electron transfer theory, the 1991 IBM France Prize for his work on tunnelling through a molecule and the 1997 Feynman Prize "experimental" for his work on molecular manipulation. In 1999, he received the French Nanotechnology Prize for his work on nanoscale science and the Share University Research Award of IBM for his work on intramolecular circuits. In 2002, he received from the CNRS, the Silver Medal in Chemistry for his work on molecular nanosciences.

ESSCIRC-INVITED PLENARY TALKS

Lawrence E. Larson
"Digital control of RF power amplifiers for next generation wireless communications"

Future generations of wireless communications are expected to place increasing burdens on the efficiency and linearity of power amplifiers, due to the use of more complex waveforms and OFDM. This has implications for the design of transmitters in portable/mobile devices as well as base stations and access points. Although semiconductor device technology has made rapid progress in fundamental power amplifier transistor performance, the use of digital signal processing techniques to optimize the linearity and efficiency provides enormous potential for further improvement (especially on the handset side). This paper will summarize the digital techniques that can be employed to improve the performance of wireless power amplifiers.

Biography

Lawrence E. Larson is currently Director of the UCSD Center for Wireless Communications and the Communications Industry Professor of Electrical and Computer Engineering at the University of California, San Diego. He is the recipient or co-recipient of numerous awards including the 1996 Lawrence A. Hyland Patent Award of Hughes Electronics, for his work on low-noise millimeterwave HEMTs, and the 1999 IBM Microelectronics Excellence Award for his work in Si/SiGe HBT technology. He has published over 200 papers, co-authored three books, has received 27 US patents, and is a Fellow of the IEEE.

Bram Nauta
"Analog/RF circuit design techniques for nanometerscale IC technologies"

CMOS evolution introduces several problems in analog design. Gate-leakage mismatch exceeds conventional matching tolerances requiring active cancellation techniques or alternative architectures. One strategy to deal with the use of lower supply voltages is to operate critical parts at higher supply voltages, by exploiting combinations of thin- and thick-oxide transistors. Alternatively low voltage circuit techniques are successfully developed. In order to benefit from nanometer scale CMOS technology, more functionality is shifted to the digital domain, including parts of the RF circuits.

Biography

Bram Nauta received the M.Sc degree (1987) and the Ph.D. degree (1991) in electrical engineering from the University of Twente, Enschede, The Netherlands. In 1991 he joined the Mixed-Signal Circuits and Systems Department of Philips Research, Eindhoven the Netherlands, where he worked on various analog baseband circuits. In 1998 he returned to the University of Twente, as full professor heading the IC Design group in the MESA+ Research Institute and dept. of Electrical Engineering. His current research interest is high speed analog CMOS circuits for transceivers.

ESSCIRC-INVITED PLENARY TALKS

Stefan Rüping and Berndt Gammel
"SmartCards inside"

Today's SmartCard- and Security-IC's are not only phone cards anymore, they are embedded cryptographic security processors and have to face special challenges concerning architecture, design, methodology and technology. The requirements for power and performance are extremely contradictory. On the one hand, embedded Java capability needs the high performance computing power of a 32bit core including caches. On the other hand the contactless operation mode requires ultra low power ability. SmartCard IC's have specific co-processors for efficient cryptographic execution and a bunch of peripherals to enable a flexible use of the controller for many kinds of applications. Security IC's are subject to attacks. An overview of invasive and non-invasive attacks and also examples for appropriate countermeasures will be given. Exciting future trends will be presented furthermore.

Biographies

Stefan Rüping obtained his Dipl.-Ing. and his Dr.-Ing. in electrical engineering from Dortmund University/Germany. From 1995 to 2000, he was a senior engineer at the Heinz Nixdorf Institute, Paderborn/Germany, doing research on concepts and ASICs for decentralized intelligent systems and artificial neural networks. Since November 2000 he is working on innovations and concepts for high security system and hardware solutions within the Secure Mobile Solutions (SMS) department of Infineon. He is head of the concept engineering group responsible for 8/16 bit smartcard controllers.

Berndt M. Gammel obtained his Dipl. Phys. and his Dr. rer. nat. from Technische Universität München. Since 1998 he is working on microprocessor architectures, concepts and innovations for high security system and hardware solutions within the Security and Chip Card ICs department of Infineon Technologies AG. He is the head of the concept engineering group responsible for the 32 bit smartcard controller family.

Registration from 8:00 am at :

Alpes Congres - Alpexpo
Avenue d'Innsbruck - BP 2408 - 38034 GRENOBLE - France
Tel. +33 (0) 476 39 66 00 (switch board Alpexo)

Organiser:
Simon Deleonibus CEA-LETI, email: sdeleonibus@cea.fr

Short course 1: New process and device concepts

Chair: F. Balestra, IMEP
Room: Chartreuse

8:50-9:00 **Introduction** - F. Balestra, IMEP

9:00-10:30 **Advanced CMOS Devices on Bulk and SOI: Physics, Modeling and Characterisation** - T. Poiroux, CEA LETI

10:30-10:45 Coffee Break

10:45-12:15 **Alternative CMOS Architectures and ITRS Emerging Research Devices** - HS Philip-Wong, University of Stanford

12:15-13:45 Lunch (Sponsored by NANOCMOS)

13:45-14:45 **High-K Gate Dielectrics** - H. Iwai, Tokyo Inst. of Tech

14:45-15:45 **Ion Implantation Damage and Annealing in Silicon** - K. Jones, University of Florida

15:45-16:00 Coffee Break

16:00-17:00 **New Interconnects Schemes: End of Copper, Optical Interconnects?** - S. Laval, IEF, France

Fees:

Regular: 200 EUR (early), 250 EUR (late)
Students: 150 EUR (early), 200 EUR (late)

Short course 2: Advanced concepts for SOC and SIP

Chair: S. Deleonibus, CEA-LETI
Room: Belle étoile

8:50-9:00 **Introduction** - S. Deleonibus CEA-LETI

9:00-10:30 **SOC and SIP for Heterogeneous System Integration** - R. Mertens, IMEC

10:30-10:45 Coffee Break

10:45-12:15 **System-Level Performance Analysis of Advanced CMOS Technologies** - Philip Christie, Philips

12:15-13:45 Lunch (Sponsored by NANOCMOS)

MONDAY, 12 SEPTEMBER

13:45-14:45 **Advanced SiGeC BICMOS Technology for SoC Integration** -
A. Chantre, STMicroelectronics

14:45-15:45 **Embedded Memories** - A. Maurelli, STMicroelectronics

15:45-16:00 Coffee Break

16:00-17:00 **Introducing New Devices on Chip: MEMS, Sensors, etc.** -
P. Ancey, STMicroelectronics

Fees:

Regular: 200 EUR (early), 250 EUR (late)
Students: 150 EUR (early), 200 EUR (late)

Short course 3: Nanoelectronics - Beyond the roadmap Emerging research devices

Chair: G. Baccarani, Univ. Bologna
Room: Meije

8:50-9:00 **Introduction** - G. Baccarani, Univ. Bologna

9:00-10:00 **Molecular Electronics: Self-Assembly and Organisation,
Carbon Nanotubes** - J-P. Bourgoin, CEA

10:00-11:00 **Spin Electronics** - C. Chappert, IEF

11:00-11:15 Coffee Break

11:15-12:15 **Quantum Computing in Quantum Dots** - D. Loss, U. Basel

12:15-13:45 Lunch (Sponsored by NANOCMOS)

Short course 4: Emerging Memory Architectures When will the UNIversal Memory be available?

Chair: R. Bouchakour, Univ. Marseille
Room: Meije

12:15-13:45 Lunch (Sponsored by NANOCMOS)

13:50-14:00 **Introduction** - R. Bouchakour, Univ. Marseille

14:00-15:00 **Technology and Key Design Issues for New Memory Devices
(Embedded and Stand Alone)** - Kinam Kim, Samsung

15:00-16:00 **FeRAM and MRAM Technologies** - Y. Arimoto, Fujitsu

16:00-16:15 Coffee Break

16:15-17:15 **New Memory Concepts: from Silicon Nanocrystal Memories
to Molecular Memories** - B. De Salvo, LETI

Fees (short course 3 + 4):

Regular: 200 EUR (early), 250 EUR (late)
Students: 150 EUR (early), 200 EUR (late)

TUESDAY, 13 SEPTEMBER
SCIENTIFIC PROGRAMME

Introduction and Paper Award 2004

Time: 08:45 - 09:15
Location: Dauphine

Joint Plenary Session

Chairs: S. Cristoloveanu, IMEP (France) ; M. Brillouët, CEA-LETI (France)
Time: 09:15 - 09:55
Location: Dauphine

09:15 **Future Devices for Information Processing**
R. Cavin, V. Zhirnov, Semiconductor Research Corporation, USA

SESSION 1.E. : DC/DC Converters

Chairs: H. Casier, AMIS (Belgium) ; M. Moyal, Consultant (Germany)
Time: 10:00 - 11:00
Location: Chartreuse

1E1

10:00 **A PMOS-Switch Based Charge Pump Allowing Low Cost Implementation on a CMOS Standard Process**
E. Racape, J. Daga, Atmel, France

1E2

10:20 **A PWM Dual-Output DC/DC Boost Converter in a 0.13um CMOS Technology for Cellular-Phone Backlight Application**
S. Kuok Hoon, N. Culp, Texas Instruments, USA; J. Chen, Advanced Analogic Tech, USA; F. Maloberti, University of Pavia, Italy

1E3

10:40 **A New Integrated Charge Pump Architecture Using Dynamic Biasing of Pass Transistors**
L. Mensi, L. Colalongo, A. Richelli, Z. Kovacs, University of Brescia, Italy

SESSION 1.F.: Amplifiers beyond 10 GHz

Chairs: Y. Papananos, National Technical University of Athens (Greece); S. Chakraborty, Texas Instruments (USA)
Time: 10:00 - 11:00
Location: Belle étoile

1F1

10:00 **24 GHz LNA in 90nm RF-CMOS with High-Q Above-IC Inductors**
O. Dupuis, X. Sun, G. Carchon, P. Soussan, IMEC, Belgium; M. Frendahl, Chalmers University of Technology, Sweden; S. Decoutrer, W. De Raedt, IMEC, Belgium

TUESDAY, 13 SEPTEMBER

1F2
10:20 **A 28.5GHz Monolithic Cascode LNA with 70GHz f_T SiGe HBTs**
F. Fortes, J. Freire, Instituto de Telecomunicações, Portugal;
D. Leenaerts, Philips Research, The Netherlands; R. Mahmoudi,
A. Roermund, Technische Universiteit Eindhoven, The Netherlands

1F3
10:40 **A 12.5GHz SiGe BICMOS Limiting Amplifier Using a Dual Offset Cancellation Loop**
A. Maxim, Maxim, USA; D. Antrik, University of Texas at Austin, USA

SESSION 1.G. : Synthesizer Building Blocks

Chairs: M. Tiebout, Infineon Technologies (Germany) ; J. Crols, AnSem (Belgium)
Time: **10:00 - 11:00**
Location: Meije

1G1
10:00 **GMSK Modulation of Subharmonic Injection Locked Oscillators**
T. Finateu, STMicroelectronics, France; Y. Deval, IXL, France; F. Badets,
STMicroelectronics, France; J. Begueret, IXL, France

1G2
10:20 **Phase Noise Degradation of LC-tank VCOs Due to Substrate Noise and Package Coupling**
M. Méndez, D. Mateo, X. Aragonès, J. González, Electronic Engineering
Department, UPC, Spain

1G3
10:40 **A 34GHz/1V Prescaler in 90nm CMOS SOI**
M. Sanduleanu, Philips Research Eindhoven, The Netherlands;
R. Ionita, Institut Superieur d'Electronique de Paris - ISEP, France;
A. Vladimirescu, University of California at Berkeley, BWRC, USA

Coffee Break

Time: **11:00 - 11:20**
Location: Salle de Réception

SESSION 2.E. : Analog Signal Processing

Chairs: H. Grünbacher, Vienna Univ. of Technology (Austria) ; S. Donnay,
IMEC (Belgium)
Time: **11:25 - 12:45**
Location: Chartreuse

2E1
11:25 **Continuous-Time DSPs, Analog/Digital Computers and Other Mixed-Domain Circuits (Invited)**
Y. Tsividis, G. Cowan, Y. Li, K. Shepard, CISL, Department of Electrical
Engineering, Columbia University, USA

2E2

11:45 **A Reconfigurable VLSI Learning Array**
S. Bridges, University of Washington, Computer Science and Engineering, USA; M. Figueroa, Universidad de Concepcion, Electrical Engineering, Chile; D. Hsu, Hamlet, Inc, USA; C. Diorio, University of Washington, Computer Science and Engineering, USA

2E3

12:05 **A Real-Time Image-Feature-Extraction and Vector-Generation VLSI Employing Arrayed-Shift-Register Architecture**
H. Yamasaki, T. Shibata, The University of Tokyo, Japan

2E4

12:25 **A High-Speed Median Filter VLSI Using Floating-Gate-MOS-Based Low-Power Majority Voting Circuits**
H. Yamasaki, T. Shibata, The University of Tokyo, Japan

SESSION 2.F. : Short Range Communications

Chairs: W. Simbuerger, Infineon Technologies (Germany) ; D. Belot, ST Microelectronics (France)
Time: **11:25 - 12:45**
Location: Belle étoile

2F1

11:25 **A Low-Power High-Performance SiGe BiCMOS 802.11a/b/g Transceiver IC for Cellular and Bluetooth Co-Existence Applications**
O. Charlon, M. Locher, H. Visser, D. Duperray, J. Chen, M. Judson, A. Landesman, C. Hritz, U. Kohlschuetter, Y. Zhang, C. Ramesh, A. Daanen, M. Gao, S. Haas, V. Maheshwari, Philips Semiconductors, USA; A. Bury, G. Nitsche, A. Wrzyszcz, Philips Semiconductors, Germany; W. Redman-White, Philips Semiconductors, UK

2F2

11:45 **17 GHz Receiver in TSLP Package for WLAN/ISM Applications in 0.13 μm CMOS**
C. Kienmayer, M. Engl, Infineon Technologies AG, Germany; A. Desch, R. Thüringer, Technical University of Vienna, Austria; M. Berry, University of Ulm, Germany; M. Tiebout, Infineon Technologies AG, Germany; A. Scholtz, Technical University of Vienna, Austria; R. Weigel, Univ. of Erlangen-Nuremberg, Germany

2F3

12:05 **An 18-GHz, 10.9-dBm Fully-Integrated Power Amplifier with 23.5% PAE in 130-nm CMOS**
C. Cao, K. O, H. Xu, Y. Su, University of Florida, USA

2F4

12:25   **SiGe Transformer Matched Power Amplifier for Operation at Millimeter-Wave Frequencies**

U. Pfeiffer, IBM T.J. Watson Research Center, USA; D. Goren, IBM, Israel; B. Floyd, S. Reynolds, IBM T.J. Watson Research Center, USA

SESSION 2.G. :
Low Power and High Performance Digital Circuits

Chairs: S. Rusu, Intel Corporation (USA) ; P. Larsson-Edefors, Chalmers University of Technology (Sweden)

Time: **11:25 - 12:45**

Location: Meije

2G1

11:25   **Dynamic State-Retention FlipFlop for Fine-Grained Sleep Transistor Scheme**

S. Henzler, Technical University of Munich, Germany; T. Nirschl, C. Pacha, Infineon Technologies, Germany; P. Teichmann, M. Eireiner, J. Fischer, Technical University of Munich, Germany; G. Georgakos, J. Berthold, Infineon Technologies, Germany; D. Schmitt-Landsiedel, P. Spindler, M. Fulde, T. Fischer, Technical University of Munich, Germany

2G2

11:45   **Isodelay Output Driver Design using Step-wise Charging for Low Power**

A. Katoch, H. Veendrick, Philips Research Laboratories, The Netherlands

2G3

12:05   **Low Leakage Design Techniques for LUT-based FPGAs**

A. Lodi, L. Ciccarelli, D. Loparco, University of Bologna, Italy; R. Canegallo, STMicroelectronics, Italy; R. Guerrieri, University of Bologna, Italy

2G4

12:25   **An On-Chip Jitter Measurement Circuit with Sub-picosecond Resolution**

K. Jenkins, IBM T.J. Watson Research Center, USA; A. Jose, Columbia University, USA; D. Heidel, IBM T.J. Watson Research Center, USA

Lunch

Time: **12:45 - 14:10**

Location: Les Ecrins

Joint Plenary Session

Chairs: M. Steyaert, Katholieke Universiteit Leuven (Belgium); W. Redman-White, Philips Semiconductors (UK)
Time: 14:15 - 14:55
Location: Dauphine

14:15 **Silicon Nano-Photonics: Where the Photons Meet the Electrons**
E. Yablonovitch, Electrical Engineering Department, University of California, USA

ESSCIRC Plenary Session

Chairs: M. Steyaert, Katholieke Universiteit Leuven (Belgium); W. Redman-White, Philips Semiconductors (UK)
Time: 15:00 - 15:40
Location: Dauphine

15:00 **Digital Control of RF Power Amplifiers for Next-Generation Wireless Communications**
L. Larson, P. Asbeck, D. Kimba, Center for Wireless Communications, University of California, USA

Coffee Break

Time: 15:40 - 16:00
Location: Alpes Congrès

SESSION 3.E. : High Resolution Data Converters

Chairs: D. Macq, AMIS (Belgium) ; D. Johns, University of Toronto (Canada)
Time: 16:00 - 17:00
Location: Dauphine

3E1
16:00 **A 15-bit 30 MS/s 145 mW Three-step ADC for Imaging Applications**
H. van der Ploeg, M. Vertregt, Philips Research, The Netherlands; M. Lammers, Philips ICLab, France

3E2
16:20 **A 220mW 14b 40MSPS Gain Calibrated Pipelined ADC**
J. Bjørnsen, Norwegian University of Science and Technology, Norway; Ø. Moldsvor, T. Sæther, Nordic Semiconductor ASA, Norway; T. Ytterdal, Norwegian University of Science and Technology, Norway

3E3
16:40 **An On-chip Self-calibration Method for Current Mismatch in D/A Converters**
G. Radulov, Eindhoven University of Technology, The Netherlands; P. Quinn, Xilinx, Ireland; H. Hegt, A. van Roermund, Eindhoven University of Technology, The Netherlands

SESSION 3.F. : PLLs

Chairs: J. Long, Technical University of Delft (The Netherlands) ; Q. Huang, ETH Zurich (Switzerland)

Time: 16:00 - 17:00

Location: Oisans

3F1

16:00 **A fast-hopping single-PLL 3-band UWB**

R. van de Beek, D. Leenaerts, G. van der Weide, Philips Research, The Netherlands

3F2

16:20 **Multi-Standard Carrier Generation System for Quad-band GSM / WCDMA (FDD-TDD) / WLAN (802.11 a-b-g) radio**

A. Koukab, Y. Lei, M. Declercq, Ecole Polytechnique Fédérale de Lausanne (EPFL), Switzerland

3F3

16:40 **Fast AFC Technique Using a Code Estimation and Binary Search Algorithm for Wideband Frequency Synthesis**

K. Lee, E. Sung, I. Hwang, B. Park, Samsung Electronics, Korea

SESSION 3.G. : Clocking and Synchronisation

Chairs: W. Dehaene, Katholieke Universiteit Leuven (Belgium); R. Hasholzner, Freescale (Germany)

Time: 16:00 - 17:00

Location: Stendhal

3G1

16:00 **A Novel 40-GHz Flip-Flop-Based Frequency Divider in 0.18 μm CMOS**

R. Mohanavelu, Intel, USA; P. Heydari, University of California, Irvine, USA

3G2

16:20 **A Fast-Lock Mixed-Mode DLL with Wide-Range Operation and Multiphase Outputs**

K. Cheng, Y. Lo, National Central University, Taiwan

3G3

16:40 **A Multichannel 3.5mW/Gbps/Ch Gated Oscillator Based CDR in a 0.18 μm Digital CMOS Technology**

A. Tajalli, EE dept, Sharif U of T, Iran; P. Muller, LSM, EPFL, Lausanne, Switzerland; M. Atarodi, EE dept, Sharif U of T, Iran; Y. Leblebici, LSM, EPFL, Lausanne, Switzerland

RUMP SESSION: Where will the revolutionary solutions come from: technology or design?

Time: **17:00 - 18:30**
Location: Dauphine

Moderators : T. Skotnicki (STMicroelectronics, France) , A. Kaiser (IEMN, France)

ESSDERC Panelists :

* Hiroshi IWAI (Tokyo Institute of Technology, Japan)
* Rainer WASER (RWTH-Aachen, Germany)
* Kazunari ISHIMARU (SoC R&D Center, TOSHIBA Corp., Japan)
* Peter ZEITZOFF (SEMATECH, USA)

ESSCIRC Panelists:

* Clive BITTLESTONE (Texas Instruments, USA)
* Georges GIELEN (K.U. Leuven, Belgium)
* Sreedhar NATARAJAN (Emerging Memory Technologies, Canada)
* Yannis TSIVIDIS (Columbia University, USA)

This rump session brings together eight international experts in technology/devices and advanced design. Each panelist represents a different area of the technology or design: from CMOS manufacturing and advanced Si devices to nanoelectronics beyond CMOS, from analog & RF to memory and CAD. Short presentations are given to stimulate questions and comments from the audience. What are the bottlenecks? What are the perspectives for breakthrough solutions? Will they come from the technology/device side, from the design side, or from both?

Welcome Reception at the "Musée de Grenoble"

Time: 19:00

Grenoble & CMOS interconnects

23

WEDNESDAY, 14 SEPTEMBER
SCIENTIFIC PROGRAMME

Joint Plenary Session

Chairs: C. Enz, CSEM (Switzerland) ; E. Perea, STMicroelectronics (France)
Time: 09:00 - 09:40
Location: Dauphine

09:00 **Terahertz Technology: Devices and Applications**
M. Shur, ECSE Department and Broadband Center, Rensselaer Polytechnic Institute, USA

ESSCIRC Plenary Session

Chairs: C. Enz, CSEM (Switzerland) ; E. Perea, STMicroelectronics (France)
Time: 09:45 - 10:25
Location: Dauphine

09:45 **Analog/RF Circuit Design Techniques for Nanometerscale IC Technologies**
B. Nauta, A. Annema, University of Twente, The Netherlands

Coffee Break (Sponsored by Mentor Graphics)

Time: 10:25 - 10:45
Location: Alpes Congrès

SESSION 4.E. : DSP Building Blocks

Chairs: T. Noll, University of Technology RWTH Aachen (Germany) ; M. Renaudin, TIMA - INPG Grenoble (France)
Time: 10:45 - 12:45
Location: Dauphine

4E1
10:45 **Design for Manufacturing in the Nanoscale Era (Invited)**
C. Bittlestone, Texas Instruments, USA

4E2
11:05 **A 2GHz 13.6mW 12x9b Multiplier for Energy Efficient FFT Accelerators**
S. Hsu, Intel Corporation, USA; V. Venkatraman, University of Massachusetts, USA; S. Mathew, H. Kaul, M. Anders, S. Dighe, Intel Corporation, USA; W. Burleson, University of Massachusetts, USA; R. Krishnamurthy, Intel Corporation, USA

4E3
11:25 **The Vector Fixed Point Unit of the Synergistic Processor Element of the Cell Architecture Processor**
N. Mäding, IBM Entwicklung GmbH, Böblingen, Germany; J. Leenstra, J. Pille, R. Sautter, S. Büttner, S. Ehrenreich, W. Haller, IBM Entwicklung GmbH, Böblingen, Germany

4E4

11:45 **A Fixed-Point Multimedia Co-Processor with 50Mvertices/s Programmable SIMD Vertex Shader for Mobile Applications**
J. Sohn, J. Woo, KAIST, Korea; R. Woo, Texas Instruments Inc., Korea; H. You, KAIST, Korea

4E5

12:05 **A 3.33Gb/s (1200,720) Low-Density Parity Check Code Decoder**
C. Lin, K. Lin, H. Chang, C. Lee, DEE, National Chiao Tung University, Taiwan

4E6

12:25 **ASIC Implementation of a MIMO-OFDM Transceiver for 192 Mbps WLANs**
D. Perels, S. Haene, P. Luethi, A. Burg, W. Fichtner, Integrated Systems Laboratory, ETH Zurich, Switzerland; H. Bölcskei, Communication Technology Laboratory, ETH Zurich, Switzerland; N. Felber, Integrated Systems Laboratory, ETH Zurich, Switzerland

SESSION 4.F. : RF Circuits

Chairs: D. Leenaerts, Philips Research Laboratories (The Netherlands); G. Gramegna, ST Microelectronics (Italy)

Time: **10:45 - 12:45**

Location: Oisans

4F1

10:45 **ESD-protected CMOS 3-5 GHz Wideband LNA+PGA Design for UWB**
R. Salerno, Infineon Technologies, Austria; M. Tiebout, H. Paule, M. Streibl, Infineon Technologies, Germany; C. Sandner, Infineon Technologies, France; K. Kropf, Infineon Technologies, Germany

4F2

11:05 **A 5-GHz BiCMOS Variable-Gain Low Noise Amplifier with Inductorless Low-Gain Branch**
M. Liu, J. Craninckx, IMEC vzw, Belgium

4F3

11:25 **A Cellular-Band CDMA 0.25 μm CMOS LNA Linearized using Active Post-Distortion**
N. Kim, V. Aparin, K. Barnett, C. Persico, Qualcomm, USA

4F4

11:45 **IP2 Calibrator Using Common Mode Feedback circuitry**
W. Kim, S. Yang, Y. Moon, J. Yu, H. Shin, W. Choo, B. Park, Samsung Electronics, Korea

4F5

12:05 **A Modified LMS Adaptive Filter Architecture with Improved Stability at RF**
V. Aparin, Qualcomm Inc., USA

4F6

12:25 **Antenna and Input Stages of a 470-710 MHz Silicon TV Tuner for Portable Applications**
V. Rambeau, H. Brekelmans, M. Notten, Philips Research, The Netherlands; K. Boyle, Philips Research, UK; J. Van Sinderen, Philips Semiconductors, France

SESSION 4.G. : Amplifiers

Chairs: P. Mole, INTERSIL / Elantec Semiconductor (United Kingdom) ; E. Bruun, Technical University of Denmark (Denmark)
Time: **10:45 - 12:45**
Location: Stendhal

4G1

10:45 **CAFFEINE: Template-Free Symbolic Model Generation of Analog Circuits via Canonical Form Functions and Genetic Programming (invited from DATE)**
T. McConaghy, T. Eeckelaert, G. Gielen, K.U. Leuven, ESAT-MICAS, Belgium

4G2

11:05 **A 0.6V 100dB 5.2MHz Transconductance Amplifier Realized in a Multi-VT Process**
A. Bargagli-Stoffi, Technical University of Munich, Germany; J. Sauerbrey, R. Thewes, Infineon Technologies AG, Corporate Research, Munich, Germany; D. Schmitt-Landsiedel, Technical University of Munich, Germany

4G3

11:25 **120nm CMOS OPAMP with 690 MHz f_T and 128 dB DC gain**
F. Schlögl, H. Zimmermann, Vienna University of Technology, Austria

4G4

11:45 **A 1 Watt Audio Amplifier in a Standard Digital 90-nm CMOS Technology**
R. Becker, W. Groeneweg, Philips Semiconductors, Switzerland

4G5

12:05 **100-MS/s 14-b Track-and-Hold Amplifier in 0.18-μm CMOS**
D. Vecchi, C. Azzolini, A. Boni, Dip. di Ingegneria dell'Informazione, University of Parma, Italy; F. Chaahoub, L. Crespi, Conexant Systems, Inc, USA

4G6

12:25 **A Low-Power, 10Gs/s Track-and-Hold Amplifier in SiGe BiCMOS Technology**
Y. Borokhovych, H. Gustat, B. Tillack, B. Heinemann, IHP, Germany; Y. Lu, W. Kuo, X. Li, J. Cressler, R. Krithivasan, School of ECE, USA

WEDNESDAY, 14 SEPTEMBER

Lunch

Time: 12:45 - 14:10
Location: Les Ecrins

Joint Plenary Session

Chairs: H. Iwai, Tokyo Institute of Technology (Japan) ; F. Balestra, IMEP (France)
Time: 14:15 - 14:55
Location: Dauphine

14:15 **Future of CMOS Technology, Manufacturing and Products**
M. Thompson, STMicroelectronics, France

SESSION 5.E. : Ultra Wide Band

Chairs: M. Kokubo, Hitachi (Japan) ; W. Simbuerger, Infineon Technologies (Germany)
Time: 15:00 - 16:00
Location: Chartreuse

5E1
15:00 **A Novel UWB Impulse-Radio Transmitter with All-Digitally-Controlled Pulse Generator**
T. Norimatsu, R. Fujiwara, M. Kokubo, M. Miyazaki, Hitachi Ltd., Japan; Y. Ookuma, M. Hayakawa, S. Kobayashi, N. Koshizuka, K. Sakamura, YRP Ubiquitous Networking Lab., Japan

5E2
15:20 **Single-Chip CMOS Pulse Generator for UWB Systems**
L. Smaini, C. Tinella, D. Helal, C. Stoecklin, L. Chabert, C. Devaucelle, R. Cattenoz, D. Belot, STMicroelectronics, France

5E3
15:40 **15-27 GHz Pseudo-Noise UWB Transmitter for Short-Range Automotive Radar in a Production SiGe Technology**
H. Veenstra, E. van der Heijden, D. van Goor, Philips Research, The Netherlands

SESSION 5.F. : Sensor Interfaces

Chairs: A. Cathelin, ST Microelectronics (France) ; M. Punzenberger, Infineon Technologies Austria AG (Austria)
Time: 15:00 - 16:00
Location: Belle étoile

5F1
15:00 **A 5.1-μW UHF RFID Tag Chip Integrated with Sensors for Wireless Environmental Monitoring**
N. Cho, S. Song, S. Kim, KAIST, Korea; S. Kim, Chungbook National University, Korea; H. Yoo, KAIST, Korea

5F2

15:20   **A High Accurate Logarithmic Amplifier System with Wide Input Range and Extreme Low Temperature Coefficient**
S. Groiß, M. Köberle, Infineon Technologies Austria AG, Austria

5F3

15:40   **A BiCMOS Ultrasound Front End Signal Processor for High Temperature Applications**
O. Vermesan, L. Blystad, R. Bahr, M. Hjelstuen, SINTEF, Norway; L. Beneteau, Schlumberger, USA; B. Froelich, Schlumberger, France

SESSION 5.G. : Test of Digital Circuits and Memory

Chairs: B. Courtois, TIMA - INPG Grenoble (France) ; G. Gielen, Katholieke Universiteit Leuven (Belgium)
Time: **15:00 - 16:00**
Location: Meije

5G1

15:00   **Implementing Multi-Gigahertz Test Systems Using CMOS FPGAs and PECL Components (Invited from DATE)**
D. Keezer, C. Gray, A. Majid, N. Taher, Georgia Institute of Technology, School of Electrical and Computer Engineering, USA

5G2

15:20   **An On-Chip Multi-Channel Waveform Monitor for Mixed Signal VLSI Diagnostics (Invited from DATE)**
K. Noguchi, M. Nagata, Department of Computer and Systems Engineering, Kobe University, Japan

5G3

15:40   **Memory Testing Improvements through Different Stress Conditions (Invited from DATE)**
A. Majhi, M. Azimane, G. Gronthoud, M. Lousberg, Philips Research, The Netherlands; S. Eichenberger, Philips Semiconductors, The Netherlands; F. Bowen, Philips Semiconductors, USA

SESSION 5.H. : Linear High Voltage Circuits

Chairs: M. Moyal, Consultant (Germany) ; M. Steyaert, Katholieke Universiteit Leuven (Belgium)
Time: **15:00 - 16:00**
Location: Sept Laux

5H1

15:00   **A 5.5V SOPA Line Driver in a Standard 1.2V 0.13um CMOS Technology**
B. Serneels, M. Steyaert, W. Dehaene, ESAT-MICAS, Belgium

WEDNESDAY, 14 SEPTEMBER

5H2

15:20   **Silicon Bipolar Circuits for Wideband FM CATV Transmission**
R. Rosales, M. Jackson, University of British Columbia, Canada

5H3

15:40   **SOI Four-Gate Transistor (G⁴-FET) for High Voltage Analog Applications**
S. Chen, J. Vandersand, B. Blalock, University of Tennessee, USA;
K. Akarvardar, S. Cristoloveanu, IMEP, France; M. Mojarradi, JPL, NASA, USA

Coffee Break (Sponsored by Mentor Graphics)

Time: **16:00 - 16:20**
Location: Salle de Réception

SESSION 6.E. : Continuous Time Filters

Chairs: B. Nauta, University of Twente (The Netherlands) ; W. Redman-White, Philips Semiconductors /Southampton (United Kingdom)
Time: **16:20 - 18:00**
Location: Chartreuse

6E1

16:20   **A 1.2V-21dBm OIP3 4th-order Active-gm-RC Reconfigurable (UMTS/WLAN) Filter with On-chip Tuning Designed with an Automatic Tool**
S. D'Amico, V. Giannini, A. Baschirotto, University of Lecce, Italy

6E2

16:40   **A 43dB ACR Low-Pass Filter with Automatic Tuning for Low-IF Conversion DAB/T-DMB Tuner IC**
S. Kim, B. Kim, M. Jeong, Y. Cho, T. Kim, B. Kim, J. Lee, Integrant Technologies Inc., Korea

6E3

17:00   **Ultra Low-Power Analog Morlet Wavelet Filter in 0.18 μm BiCMOS Technology**
S. Haddad, TUDelft, The Netherlands; J. Karel, R. Peeters, R. Westra, University of Maastricht, The Netherlands; W. Serdijn, TUDelft, The Netherlands

6E4

17:20   **A 1.2-V CMOS Complex Bandpass Filter with a Tunable Center Frequency**
H. Majima, H. Ishikuro, K. Agawa, M. Hamada, Toshiba Corp., Japan

6E5

17:40   **A Low-Frequency Sub 1.5-V Micropower Gm-C Filter Based on Subthreshold MIFG MOS Transistors**
A. El Mourabit, G. Lu, P. Pittet, LENAC - University Lyon 1, France

SESSION 6.F. : Sensor Integration

Chairs: C. Hagleitner, IBM Research - Zürich Research Laboratory (Switzerland) ; J. Trontelj, University of Ljubljana (Slovenia)
Time: 16:20 - 18:00
Location: Belle étoile

6F1

16:20 **CMOS Microelectrode Array for Bidirectional Interaction with Neuronal Networks**
F. Heer, S. Hafizovic, W. Franks, ETH Zurich, Switzerland; T. Ugniwenko, A. Blau, C. Ziegler, TU Kaiserslautern, Germany; A. Hierlemann, ETH Zurich, Switzerland

6F2

16:40 **All CMOS Low Power Platfrom for Dielectrophoresis Bio-Analysis**
A. Enteshari, G. Jullien, O. Yadid-Pecht, K. Kaler, University of Calgary, Canada

6F3

17:00 **A CMOS-Based Sensor Array System for Chemical and Biochemical Applications**
M. Zimmermann, T. Volden, K. Kirstein, S. Hafizovic, J. Lichtenberg, A. Hierlemann, ETH Zurich, Switzerland

6F4

17:20 **Electrical Measurement of Alignment for 3D Stacked Chips**
R. Canegallo, STMicroelectronics, Italy; M. Mirandola, A. Fazzi, L. Magagni, R. Guerrieri, ARCES-University of Bologna, Italy; K. Kaschlun, Fraunhofer IZM, Germany

6F5

17:40 **A 0.1% Accuracy 100 Ohm-20 MOhm Dynamic Range Integrated Gas Sensor Interface Circuit with 13+4 Bit Digital Output**
M. Grassi, P. Malcovati, University of Pavia, Italy; A. Baschirotto, University of Lecce, Italy

SESSION 6.G. : Memory Circuits

Chairs: D. Schmitt-Landsiedel, Technical University Munich (Germany); S. Natarajan, Emerging Memory Technologies (Canada)
Time: 16:20 - 18:00
Location: Meije

6G1

16:20 **A 10Mbit, 15GBytes/sec Bandwidth 1T DRAM Chip with Planar MOS Storage Capacitor in an Unmodified 150nm Logic Process for High-Density On-Chip Memory Applications**
D. Somasekhar, S. Lu, B. Bloechel, G. Dermer, B. Shekhar, V. De, K. Lai, Intel Corp, USA

6G2

16:40 **A 8Kb Domino Read SRAM with Hit Logic and Parity Checker**
A. Pelella, A. Tuminaro, R. Freese, Y. Chan, Systems & Technology Group, IBM, USA

6G3

17:00 **Analyzing Static Noise Margin for Sub-Threshold SRAM in 65nm CMOS**
B. Calhoun, A. Chandrakasan, MIT, USA

6G4

17:20 **A Precision High Voltage Wave-Shaper for Multi-Gbit Source Side Injection MLC NOR Flash Memory**
H. Tran, W. Saiki, J. Frayer, T. Vu, A. Ly, S. Nguyen, H. Nguyen, D. Lee, M. Briner, Silicon Storage Technologies, USA

6G5

17:40 **A Novel Circuit Topology for Generating and Validating Digitally Sense Amplifier Differentials for Bulk and SOI**
R. Joshi, Y. Chan, IBM, USA

Gala dinner at the PRISME Seyssins

Time: 7:30

(Bus departure from Alpexpo at 7 pm)

VILLE DE SEYSSINS

LA **METRO.**

Joint Plenary Session

Chairs: T. Skotnicki, STMicroelectronics (France) ; A. Ionescu, EPFL (Switzerland)
Time: 09:00 - 09:40
Location: Dauphine

09:00 **Towards a Molecule - Computer? Resources and Technologies to Compute within a Single Molecule**

C. Joachim, NanoSciences Group, CEMES/CNRS, France

SESSION 7.E. : Analogue Circuits for Communications Applications

Chairs: M. Punzenberger, Infineon Technologies Austria AG (Austria) ; A. Cathelin, ST Microelectronics (France)
Time: 09:45 - 10:45
Location: Chartreuse

7E1
09:45 **A 0.18 μm CMOS Switched Capacitor Voltage Modulator**

K. Cornelissens, P. Reynaert, M. Steyaert, KU Leuven, Belgium

7E2
10:05 **A 1.2V CMOS Multiplier for 10 Gbit/s Equalization**

J. Abbott, C. Plett, J. Rogers, Carleton University, Canada

7E3
10:25 **Realization of a Simple High-Value Grounded Linear Resistance in CMOS Technology**

P. Langlois, University College London, UK; J. Taylor, Bath University, UK; A. Demosthenous, University College London, UK

SESSION 7.F. : VCOs

Chairs: Y. Deval, IXL - University of Bordeaux (France) ; S. Mattisson, Ericsson Mobile (Sweden)
Time: 09:45 - 10:45
Location: Belle étoile

7F1
09:45 **A 100 μW, 1.9GHz Oscillator with Fully Digital Frequency Tuning**

N. Pletcher, J. Rabaey, University of California, Berkeley, USA

7F2
10:05 **Phase Noise Analysis and Design of a 3-GHz Bipolar Differential Colpitts VCO**

X. Wang, Infineon Technologies AG, Germany; A. Fard, Mälardalen University, Sweden; P. Andreani, Technical University of Denmark, Denmark

7F3

10:25   **A Low-Power 5 GHz CMOS LC-VCO Optimized for High-Resistivity SOI Substrates**
P. Delatte, G. Picún, L. Demeûs, CISSOID S.A., Belgium; P. Simon, UCL Microwave Lab, Belgium; D. Flandre, UCL Microelectronics Lab, Belgium

SESSION 7.G. : Crypto Systems

Chairs: A. Rothermel, Universität Ulm (Germany) ; T. Shibata, The University of Tokyo (Japan)
Time: **09:45 - 10:45**
Location: Meije

7G1

09:45   **Physical Random Number Generators for Cryptographic Application in Mobile Devices**
S. Yasuda, T. Tanamoto, R. Ohba, K. Abe, H. Nozaki, S. Fujita, Toshiba Corporation, Japan

7G2

10:05   **A Clock-less Low-Voltage AES Crypto-Processor**
G. Bouesse, M. Renaudin, A. Witon, TIMA Laboratory, France; F. Germain, SGDN/DCSSI, France

7G3

10:25   **Improving DPA Security by Using Globally-Asynchronous Locally-Synchronous Systems**
F. Gürkaynak, S. Oetiker, Integrated Systems Laboratory, ETH Zurich, Switzerland; H. Kaeslin, Microelectronics Design Center, ETH Zurich, Switzerland; N. Felber, W. Fichtner, Integrated Systems Laboratory, ETH Zurich, Switzerland

SESSION 7.H. : Imagers 1

Chairs: W. Brockherde, Fraunhofer IMS (Germany) ; E. Belhaire, IEF - CNRS - University of Paris Sud (France)
Time: **09:45 - 10:45**
Location: Sept Laux

7H1

09:45   **A Cyclic A/D Converter with Pixel Noise and Column-Wise Offset Canceling for CMOS Image Sensors**
M. Furuta, S. Kawahito, The Research Institute of Electronics, Shizuoka Univ., Japan; T. Inoue, Photron Ltd., Japan; Y. Nishikawa, The Research Institute of Electronics, Shizuoka Univ., Japan

7H2

10:05   **A High Dynamic Range, High Linearity CMOS Current-Mode Image Sensor for Computed Tomography**
R. Steadman, G. Vogtmeier, Philips Research GmbH, Germany; A. Kemna, S. Ibnou Quossai, B. Hosticka, Fraunhofer Institute - IMS, Germany

7H3

10:25   **A 35nW/pixel CMOS 2D Visual Motion Sensor**
G. Zhang, H. Lee, J. Liu, University of Texas at Dallas, USA

Coffee Break

Time: **10:45 - 11:05**
Location: Salle de Réception

SESSION 8.E. : High Speed Optical Interfaces

Chairs: W. Pribyl, Austria Mikro Systeme International(Austria) ; H. Casier, AMIS (Belgium)
Time: **11:05 - 12:45**
Location: Chartreuse

8E1

11:05   **Digital Communication Systems: the Problem of Analog Interface Circuits (Invited)**
M. Steyaert, F. Gobert, C. Hermans, P. Reynaert, B. Serneels, ESATMICAS, KULeuven, Belgium

8E2

11:25   **A 10Gb/s, 3.3V, Laser/Modulator Driver with High Power Efficiency**
M. Sanduleanu, E. Stikvoort, Philips Research Eindhoven, The Netherlands

8E3

11:45   **A 3.5Gbit/s Post-Amplifier in 0.18 μm CMOS**
C. Hermans, M. Steyaert, ESAT-MICAS, KULeuven, Belgium

8E4

12:05   **An Integrated Optical Receiver with Wide-Range Timing Discrimination Characteristics**
S. Kurtti, J. Kostamovaara, University of Oulu, Finland

8E5

12:25   **A Programmable OEIC for Laser Applications in the Range from 405nm to 780nm**
C. Seidl, TU-Vienna, Austria; H. Schatzmayer, J. Sturm, M. Leifhelm, S. Groiss, D. Spitzer, H. Schaunig, Infineon Technologies Austria, Austria; H. Zimmermann, TU-Vienna, Austria

SESSION 8.F. : Oversampled Data Converters

Chairs: A. Baschirotto, University of Lecce (Italy) ; A. Wiesbauer, Infineon Technologies Austria AG (Austria)
Time: **11:05 - 12:45**
Location: Belle etoile

8F1

11:05   **A Low-Power 22-bit Incremental ADC with 4 ppm INL, 2 ppm Gain Error and 2 μV DC Offset**

V. Quiquempoix, P. Deval, A. Barreto, G. Bellini, J. Collings, Microchip Technology Inc., USA; J. Markus, J. Silva, G. Temes, Oregon State University, USA

8F2

11:25   **A Time-Interleaved Continuous-Time D-S Modulator with 20MHz Signal Bandwidth**

T. Caldwell, D. Johns, University of Toronto, Canada

8F3

11:45   **A 10mW 81dB Cascaded Multibit Quadrature Sigma-Delta ADC with a Dynamic Element Matching Scheme**

R. Maurino, Analog Devices, UK; C. Papavassiliou, Imperial College, UK

8F4

12:05   **A 75dB Image Rejection IF-Input Quadrature Sampling SC SD Modulator**

W. Cheng, K. Pun, C. Choy, C. Chan, Chinese University of Hong Kong, Hong Kong

8F5

12:25   **An Audio FIR-DAC in a BCD Process for High Power Class-D Amplifiers**

T. Doorn, Philips Research, The Netherlands; E. van Tuijl, University of Twente / Philips Research, The Netherlands; D. Schinkel, A. Annema, University of Twente, The Netherlands; M. Berkhout, Philips Semiconductors, The Netherlands; B. Nauta, University of Twente, The Netherlands

SESSION 8.G. : Digital Power Supply & Wiring

Chairs: S. Donnay, IMEC (Belgium) ; Marcel Profirescu, EDIL Microelectronics R&D Center (Romania)

Time: **11:05 - 12:45**

Location: Meije

8G1

11:05   **Scalable Circuits for Supply Noise Measurement**

V. Abramzon, E. Alon, B. Nezamfar, M. Horowitz, Stanford University, USA

8G2

11:25   **Autonomous di/dt Noise Control Scheme for Margin Aware Operation**

T. Nakura, M. Ikeda, K. Asada, University of Tokyo, Japan

8G3

11:45   **A Built In IDDQ Testing Circuit**
S. Matakias, University of Athens, Greece; Y. Tsiatouhas, University of Ioannina, Greece; A. Arapoyanni, University of Athens, Greece; T. Haniotakis, Southern Illinois University, USA; G. Prenat, S. Mir, TIMA Laboratory, France

8G4

12:05   **Optimally-Placed Twists in Global On-Chip Differential Interconnects**
E. Mensink, D. Schinkel, E. Klumperink, E. van Tuijl, B. Nauta, University of Twente, The Netherlands

8G5

12:25   **Analysis of Low Noise Three-Phase Asynchronous Data Transmission**
N. Li, M. Ikeda, K. Asada, University of Tokyo, Japan

SESSION 8.H. : Imagers 2

Chairs: W. Brockherde, Fraunhofer IMS (Germany) ; E. Belhaire, IEF - CNRS - University of Paris Sud (France)
Time: **11:05 - 12:05**
Location: Sept Laux

8H1

11:05   **Differential Image Sensor with High Common Mode Rejection**
M. Innocent, G. Meynants, Cypress semiconductor (FillFactory), Belgium

8H2

11:25   **A Single-Photon-Avalanche-Diode 3D Imager**
D. Stoppa, ITC-irst, Centre for Scientific and Technological Research, Italy; L. Pancheri, Department of Information and Communication Technologies, Italy; M. Scandiuzzo, M. Malfatti, G. Pedretti, L. Gonzo, ITC-irst, Centre for Scientific and Technological Research, Italy

8H3

11:45   **Correlating PIN-Photodetector with Novel Difference-Integrator Concept for Range-Finding Applications**
A. Nemecek, K. Oberhauser, H. Zimmermann, Institute of Electrical Measurements and Circuit Design, Vienna University of Technology, Austria

Lunch

Time: **12:45 - 14:10**
Location: Les Ecrins

Presentation ESSDERC-ESSCIRC 2006

Time: **14:15 - 14:25**
Location: Dauphine

THURSDAY, 15 SEPTEMBER

Joint Plenary Session

Chairs: A. Kaiser, IEMN-ISEN (France) ; A. Wild, Freescale (USA)
Time: 14:25 - 15:05
Location: Dauphine

14:25 **Silicon Forever! Really?**
H. Stormer, Department of Physics and Department of Applied Physics and Applied Mathematics, Columbia University and Bell Labs, Lucent Technologies, USA

ESSCIRC Plenary Session

Chairs: A. Kaiser, IEMN-ISEN (France) ; A. Wild, Freescale (USA)
Time: 15:10 - 15:50
Location: Dauphine

15:10 **Smart Cards Inside**
B. Gammel, S. Rüping, Infineon Technologies AG, Germany

Coffee Break

Time: 15:50 - 16:10
Location: Alpes Congrès

SESSION 9.E. : Analog Circuits

Chairs: W. Sansen, Katholieke Universiteit Leuven (Belgium) ; W. Kuzmicz, Warsaw University of Technology (Poland)
Time: 16:10 - 17:30
Location: Dauphine

9E1
16:10 **A Novel Current-Mode Very Low Power Analog CMOS Four Quadrant Multiplier**
M. Gravati, M. Valle, DIBE - University of Genova, Italy; G. Ferri, N. Guerrini, DIE - Universita dell'Aquila, Italy; L. Reyes, Universidad de la Republica, Uruguay

9E2
16:30 **A Novel Four-Quadrant Analog Multiplier Using SOI Four-Gate Transistors (G^4-FETs)**
K. Akarvardar, IMEP, France; S. Chen, B. Blalock, University of Tennessee, USA; S. Cristoloveanu, P. Gentil, IMEP, France; M. Mojarradi, JPL, USA

9E3
16:50 **A 1 V, 26 μW Extended Temperature Range Band-gap Reference in 130-nm CMOS Technology**
A. Cabrini, University of Pavia, Italy; G. De Sandre, STMicroelectronics, Italy; L. Gobbi, P. Malcovati, University of Pavia, Italy; M. Pasotti, M. Poles, STMicroelectronics, Italy; F. Rigoni, G. Torelli, University of Pavia, Italy

THURSDAY, 15 SEPTEMBER

9E4

17:10   **A Low-Power 2-GSample/s Comparator in 120 nm CMOS Technology**

B. Goll, H. Zimmermann, Vienna University of Technology, Austria

SESSION 9.F. : Cellular Communications

Chairs: D. Belot, ST Microelectronics (France) ; M. Kokubo, Hitachi (Japan)
Time: **16:10 - 17:10**
Location: Oisans

9F1

16:10   **Variable Gain Amplifier in Polar Loop Modulation Transmitter for EDGE**

M. Ito, T. Yamawaki, Central Research Laboratory, Hitachi, Ltd., Japan; M. Kasahara, Renesas Technology Corp., Japan; S. Williams, TTPCom Limited, UK

9F2

16:30   **WCDMA Multicarrier Receiver for Base-Station Applications**

J. Ryynanen, M. Hotti, V. Saari, ECDL/HUT, Finland; J. Jussila, Nokia, Finland; A. Malinen, L. Sumanen, Texas Instruments, Finland; T. Tikka, K. Halonen, ECDL/HUT, Finland

9F3

16:50   **Fully-Integrated WCDMA SiGeC BiCMOS Transceiver**

B. Pellat, D. Belot, STMicroelectronics SA, France; J. Blanc, F. Goussin, D. Thevenet, S. Majcherczak, F. Reaute, P. Garcia, P. Persechini, STMicroelectronics, France; P. Cerisier, P. Conti, STMicroelectronics, Switzerland; P. Level, M. Kraemer, STMicroelectronics, France; A. Granata, STMicroelectronics, Italy

SESSION 9.G. : High Speed ADCs

Chairs: K. Bult, Broadcom Netherlands (The Netherlands) ; A. Van Roermund, Eindhoven University of Technology (The Netherlands)
Time: **16:10 - 17:30**
Location: Stendhal

9G1

16:10   **A 10BIT 30MSPS CMOS A/D Converter For High Performance Video Applications**

J. Li, J. Zhang, B. Shen, X. Zeng, Fudan University, China; Y. Guo, Shanghai MicroScience Integrated Circuits Co., Ltd, China; T. Tang, Fudan University, China

9G2

16:30   **55-mW 200-MSPS 10-bit Pipeline ADCs for Wireless Receivers**

D. Kurose, T. Ito, T. Ueno, T. Yamaji, T. Itakura, Toshiba Corporation, Japan

9G3

16:50   **Offset and Dynamic Gain-Mismatch Reduction Techniques for 10b 200MS/s Parallel Pipeline ADCs**
S. Lee, K. Kim, J. Kwon, J. Kim, Electronics and Telecommunications Research Institue (ETRI), Korea; S. Lee, Sogang University, Korea

9G4

17:10   **A 9-b 400 Msample/s Pipelined Analog-to-Digital Converter in 90nm CMOS**
C. Peach, University of Washington, USA; A. Ravi, R. Bishop, K. Soumyanath, Intel Corporation, USA; D. Allstot, University of Washington, USA

Closing Session

Time: **17:40 - 18:00**
Location: Dauphine

Farewell party at the Bastille

Time: 19:30

FRIDAY, 16 SEPTEMBER WORKSHOPS

On-site registration for all worshops:
Alpexpo, Avenue d'Innsbruck - BP 2408 - 38034 GRENOBLE - France

DECON 2005 ECS Satellite Symposium

"Crystalline Defects and Contamination:
Their Impact and Control in Device Manufacturing IV"
Thursday, 15 September, 2pm & Friday, 16 September, 9am - 5pm
Room: Sept-Laux

Symposium Description

DECON covers recent developments in science and technology of microelectronic materials regarding defects, impurities and contamination and their impact and control in device manufacturing. It encloses 9 invited and 9 contributed papers organized in four sessions.

Sessions and invited speakers:
1. **Crystalline defects in Si, strained Si, SiGe and Ge crystals and films**
   E. Tomzig (Siltronic AG)
   A. Sakai (Nagoya University)
   G. Rozgonyi (North Carolina State University)
   A. Satta (IMEC)

2. **Impurities and contamination**
   H. Habuka (Yokohama National University)

3. **Characterization techniques**
   S. Kishino (Fukui University of Technology)
   W. Grogger (FELMI, TU Graz)

4. **Device aspects of defects and impurities**
   J. Lyding (University of Illinois)
   L. Pantisano (IMEC)

A **Proceedings Volume** will be available at the symposium containing all invited and contributed papers.

Symposium Fee and Registration (for details see homepage below).
Advance registration payment on the bank account given in the form **until 15 August, 2005**.

On-site Registration on Thursday, 15 September, 2005 from 10.00 a.m.
Payment in cash or by Eurocheque; **no** credit cards.

Fee DECON 2005	in advance	on-site
ECS member/ESSDERC participant	80 EUR	100 EUR
Nonmember	100 EUR	125 EUR
Student	30 EUR	35 EUR

The fee includes coffee and beverages.

FRIDAY, 16 SEPTEMBER WORKSHOPS

Organising Committee
Prof. Bernd O. Kolbesen (J.W. Goethe-Universität, Germany)
Prof. Cor Claeys (IMEC, Belgium)
Dr. Laszlo Fabry (Wacker AG, Germany)
Dr. Francois Tardif (CEA/LETI, France)

Contact Address for Symposium Affairs
Prof. Dr. Bernd O. Kolbesen
Institut für Anorganische Chemie/ Analytische Chemie
J.W. Goethe-Universität
Marie-Curie-Str. 11
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Fax: +49 69 798 29235 / Phone: +49 69 798 29154
e-mail: kolbesen@chemie.uni-frankfurt.de

General Information and registration form available under:
http://www.anorg.chemie.uni-frankfurt.de/AK_Kolbesen/conferences/DECON.html

MOS-AK Workshop
"Principles and Practice of the Compact Modeling and its Standardisation"

Friday, 16 September, 9am - 5pm
Room: Les Bans

Workshop Chair
Dr. W. Grabinski - E-mail: W.Grabinski@freescale.com

Technical Program Coordinator
Prof. H. Iwai - E-mail: iwai@ae.titech.ac.jp

MOS-AK Workshop on compact modeling, integral part of the ESSDERC-ESSCIRC conference, aims to establish a network and discussion forum among experts in the field, create an open platform for information exchange related to compact/Spice modeling, bring people in the compact modeling field together, as well as obtain feedback from technology developers, circuit designers, and CAD tool vendors. The topics cover all important aspects of compact model development, implementation, deployment and standardisation within the main theme - compact models for mainstream CMOS circuit simulation. The specific workshop goal will be to classify the most important directions for the future development of the compact models and to clearly identify areas that need further research.

This workshop is designed for device process engineers (CMOS, SOI, BiCMOS, SiGe) who are interested in device modeling, ICs designers (RF/IF/Analog/Mixed-Signal/SoC) as well as device characterisation, modeling and parameter extraction engineers. The content will be beneficial for anyone who needs to learn what is really behind IC simulation in modern device models. The technical program of MOS-AK Workshop consists of one day of tutorials given by noted academic and industry experts; also a posters session is foreseen with contributions by TU Tokyo, EPFL Lausanne, KUL Leuven, ITE Warsaw, Ansoft, Mentor Graphics, Cascade, STM.

Workshop Programme

Mixed-Mode Device/Circuit Simulation
Tibor Grasser, Institute for Microelectronics, Technical University Vienna, Austria

An Overview of the PSP MOSFET Model
R. van Langevelde1, A.J. Scholten[1], G.D.J. Smit[1], D.B.M. Klaassen[1], G. Gildenblat[2], X. Li[2], H. Wang[2] and W. Wu[2]
[1]Philips Research Laboratories, Eindhoven, The Netherlands, [2]Department of Electrical Engineering, The Pennsylvania State University, University Park, USA

EKV3.0 - A Design-Oriented Compact MOST Model for Advanced CMOS
Matthias Bucher, Technical University of Crete, Greece

A Physically Based, Scalable MOS Varactor Model and Extraction Methodology for RF Applications
James Victory[1], Zhixin Yan[1], Gennady Gildenblat[2], Colin McAndrew[3], Jie Zheng[1]
[1]Jazz Semiconductor, Newport Beach, CA, [2]Pennsylvania State University, State College, PA, [3]Freescale Semiconductor, Tempe, AZ, USA

Compact Model for Nanoscale MOSFETs in an Intermediate Regime Between Ballistic and Diffusive Transport
Giorgio Mugnaini, Giuseppe Iannaccone, Università di Pisa, Italy

Challenges and Strategies for the SPICE Model Extraction and Simulation of the PD-SOI Technology
Jung-Suk Goo, Advanced Micro Devices, Sunnyvale, CA, USA

Asymmetrical Double Gate (DG) MOSFET Compact Modeling
O. Rozeau, M. Reyboz, T. Poiroux, P. Martin, LETI-CEA, Grenoble, France

Circuit Modeling of Non-Volatile Memory Devices
Mike Sadd, Rajesh Rao and Ramachandran Muralidhar, Freescale Semiconductor, Austin, TX, USA

Analog/HV Characterization for 0.35μm High Voltage Technology
Ehrenfried Seebacher, austriamicrosystems AG, Premstätten, Austria

Table Based Models
Victor Bourenkov[1] and Kevin G. McCarthy[2],
[1]Tyndall Nat. Inst, [2]UCC, Cork, Ireland

Acknowledgements:

No registration fee.

FRIDAY, 16 SEPTEMBER WORKSHOPS

SDR/Cognitive Radio:
"Software Defined Radio : Theory, Design and Applications"

Friday, 16 September, 9am - 5pm
Room: Belle étoile

Organized by:
Didier BELOT (ST Microelectronics, FRANCE) and Yann DEVAL (IXL Lab, FRANCE)

Abstract:

Nowadays, a total integration of RF capabilities is required for any kind of electronics system, assuming such a system is supposed to communicate with others - which, actually, is true for virtually each operational system.

As so many communication standards are available at this time, a compliant RF system is expected to address any of these standards on demand, adapting itself to either the frequency of operation or the modulation scheme imposed by the standard, or anything else. Providing such an accommodating behavior to a telecommunication system is a very challenge, and it obviously relies on dedicated embedded software in order to provide the desirable flexibility. Such an approach is known as 'Software Defined Radio' or 'Cognitive Radio', and it appears to be the way RF systems will be designed in the years to come.

Of course, relying on software will make the system both flexible and user-friendly since it will allow the addition of some novel Quality of Service proposal for free - or almost for free…

On the other hand, developing such a paradigm leads to quite complete a system architecture revolution, associated with new design constraints - the latter being driven by specific PHY layer definitions which, in return, will allow the hardware to be able to fulfill specifications which were not even defined at the time the system was established!

Thus Software Defined Radio is still a dream to come but, as a strong research effort is pursued on a worldwide basis, it is expected to bring some very good news in the years to come - if not even earlier!

In order to present SDR concept, the theory, design and applications will be addressed in this workshop. While theory will be addressed by academic speakers, design will be presented by semiconductor experts and applications will be presented by industrial fellows working in various domains of applications such as network management, automotive electronics and cellular phone designs. For the presentations to illustrate as worldwide a vision of future SDR systems as possible, speakers from Europe as well as America will have the opportunity to present their visions during this workshop.

Sampled analog signal processing versus digital signal processing, CMOS versus BiCMOS technologies and SDR oriented RF system architectures versus classical topologies will be addressed and discussed, for the attendees to be able to decide of their own concerning what will really be needed by the microelectronics market in the years to come in order to be able to complete the market requirements in a not-so-far-away future.

Registration fee: 110 EUR

SINANO Workshop
"Nanoscale CMOS and Emerging Post-CMOS Logic and Memory Nanodevices"

16 September, 9am - 5pm
Room : Chartreuse

Organizer:
Francis Balestra, IMEP (CNRS-INPG-UJF), Grenoble, balestra@enserg.fr

Abstract:

This Workshop is sponsored by the Network of Excellence SINANO (Silicon-based Nanodevices) founded by the European Commission for the 6th Framework Progarmme (EC Contract n° 506844).

Over the next quarter century, considerable challenges exist to push the limits of silicon integration down to nanometric dimensions and to enhance device performance in order to meet the ever increasing demands of communications and computing. The aim of this Workshop is to present the status and trends of CMOS and post-CMOS nanodevices for terascale ICs.

In the first part of the Workshop, advanced and ultimate CMOS devices will be presented. The talks will focus on recent advances in strained silicon and SOI structures, metallic source/drain engineering, carrier transport in ultra-thin SOI and FinFETs devices. The best modelling approaches will also be discussed. During the second part, an overview of beyond-CMOS approaches will be shown. Recent prospects in tunneling FETs, hybrid CMOS-nanowires, nanodots, molecular and carbon nanotube devices will be outlined.

Programme:

9:00 Transport in Ultra-Thin SOI Devices - K. Uchida, Toshiba

9:30 Modeling Approaches for Decananometer MOSFETs within SINANO - Luca Selmi, Univ. Udine

10:00 Advancing Strained Silicon - A. O'Niell, Newcastle Univ., P-E. Helstroem, M. Ostling, KTH, K. Lyutovich, E. Kasper, Stuttgart Univ.

10:30 Coffee Break

11:00 Novel Virtual Substrates for Strained SOI - Siegfried Mantl, Forschungszentrum Juelich

11:30 FinFET: a Mature Multi-Gate MOS Technology ? A Wideband Transistor Simulation and Characterisation Approach - Jean-Pierre Raskin, UCL, Abhisek Dixit, Nadine Collaert, IMEC, Tamara Rudenko, ISP Kiev, Tsung Ming Chung, Valeria Kilchytska, Dimitri Lederer, UCL

12:00 Recent Advances in Metallic Source/Drain Engineering - J. Knoch, Forschungszentrum Juelich, E. Dubois, G. Larrieu, IEMN, N. Reckinger, X. Tang, V. Bayot, UCL

FRIDAY, 16 SEPTEMBER WORKSHOPS

12:30   **Lunch**

14:00   **Current Status and Trends of Nanoelectronic Devices** - Yoshio Nishi, Stanford University

14:30   **Molecular/Carbon Nanotube Electronics** - Jimmy Xu, Brown University

15:00   **Hybrid CMOS-Nanowire Circuit Architectures for Digital and Analog Applications** - A. Ionescu, EPFL

15:30   **Coffee Break**

16:00   **Complementary Tunneling-Transistors (TFET): Fabrication and Application down to the 65nm CMOS-Node** - M. Sterkel, T. Nirschl, M. Fulde, P.-F. Wang, D. Schmitt-Landsiede and W. Hansch, Technical Univ. Munich

16:30   **Post-CMOS Generation: the Different Modeling Approaches Developed within SINANO for Nanotubes, Nanodots and Resonant Tunneling Devices** - Philippe Dollfus, IEF

17:00   **End of the Workshop**

No registration fee.

MIMOSA Workshop
"Invisible Electronics for Ambient Intelligence Applications"

16 September, 9am - 5pm
Room : Meije

Contact:
Pascal.Ancey@st.com, Adrian.Ionescu@epfl.ch

This **workshop** is organised by the European Integrated Project MIMOSA (*Microsystem Platform for Mobile Services and Applications: http://www.mimosa-fp6.com/*), which aims at making Ambient Intelligence (AmI) a reality by developing a mobile-phone centric open technology platform. MIMOSA extends the area of telecommunication business to ambient intelligence and thus further supports the strong competitive edge of European industry.

The MIMOSA consortium has a balanced partnership including: *key European industry* among which world leaders in telecommunications and microelectronics: NOKIA and ST Microelectronics, but also some potential end-users like LEGRAND and *key European research institutes:* CEA LETI, Fraunhofer ISIT, LAAS-CNRS, VTT, CSEM, *a technical University:* EPFL, and *active European companies:* SONION, SUUNTO, Alma Consulting Group, including SMEs: CARDIPLUS, ÅMIC, MAS.

FRIDAY, 16 SEPTEMBER WORKSHOPS

In the MIMOSA vision, the personal mobile phone is chosen as the trusted intelligent user interface to Ambient Intelligence and a gateway between the sensors, the network of sensors, the public network and the Internet. MIMOSA develops an open technology platform for implementing ambient intelligence in different application areas. The well-defined platform allows a fast and focused development of both basic technology solutions and system-level applications and services. MIMOSA focuses to develop micro- and nanosystems in several areas of a selected open platform. Examples of micro and nanosystems developments by MIMOSA are (environment domain) wireless remote-powered and autonomous sensors exploiting RFID, low-power radios exploiting RFMEMS, (user domain) microsystem-based intuitive user interfaces, MEMS based user-activity and physiological sensors, (phone domain) MEMS-based inertial, magnetic and audio sensors.

Mimosa workshop is organized as a one-day workshop including an *international invited speaker session* (9:00-12:00), dealing with state-of-the-art in the field of *microsystem technologies* and *low power circuit design* for ambient intelligence (invisible electronics) and a MIMOSA project speaker session (13:30-15:45) that will present the detailed technical advances obtained by the consortium, as well as the established roadmap and vision for needed microsystem technologies and applications. The workshop will end with a **panel session** (16:00-17:00) in which all the invited and MIMOSA speakers will interact with the audience and present their vision on the field.

More information about the detailed programme and workshop registration is available on: http://mimosa2005.epfl.ch

MIMOSA Workshop secretariat:
Isabelle Buzzi and Marie Halm
EPFL STI IMM LEG, ELB 339 (Bâtiment ELB)
Station 11, CH-1015 Lausanne, Switzerland
Email: mimosa@epfl.ch
Phone: +41 21 693 3975, Fax: +41 21 693 3640

Registration fee: 200 EUR

ENIAC Workshop
"Nanoelectronics Technologies 2020: a European Strategic Research Agenda"

16 September, 9am - 3pm
Room: Oisans

Organised by:
ENIAC (European Nanoelectronics Initiative Advisory Council)

FRIDAY, 16 SEPTEMBER WORKSHOPS

Abstract:

The Technology Platform Nanoelectronics is an initiative of major stakeholders in European Nanoelectronics, both industries and research centers, to develop a comprehensive action plan to keep Europe at the leading edge of Nanoelectronics, and to provide European Electronic industry with the key enabling technologies to meet world wide competition.

The back bone of the initiative is the establishment of a Strategic Research Agenda that will detail the research priorities and the schedule for Nanoelectronics in Europe, and drive future research initiatives. A group of researchers from both industry and academia has participated in the definition of this document, and the result of this effort will be presented to the European scientific community by the leader of the sub-groups, which defined the main sections of the agenda.

An open discussion will follow, to collect inputs of scientific community and to refine criteria to be used for future revisions.

Programme

- ▷ Introduction: the European Technology Platform Nanoelectronics
- ▷ The structure of SRA: Executive Summary
- ▷ Presentation of the SRA main sections:
- ▷ More of Moore
- ▷ Beyond CMOS
- ▷ More than Moore
- ▷ Heterogeneous Integration
- ▷ Design
- ▷ Equipment and Materials
- ▷ Round table: methodology for revision and implementation.

Contact: Livio Baldi - livio.baldi@st.com