

The Design and Implementation of the Digital Down Converter Based on the Improved DDS and DSPBuilder Techniques

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ABSTRACT: DDC (Digital Down Converter), as a key part of digital receivers, aims to get low-speed digital baseband signals by extracting and filtering the digital signals transformed by high-speed ADC (Analog Digital Conversion). This paper employs the multi-rate process technique to design the DDC, i.e. firstly conducting data CIC (Cascade Integrator Comb) extraction, then HBF (Half-Band Filtering) and at last low pass filtering. CIC, which doesn't need multiplication, can realize high speed filtering and the HBF has high operation efficiency and good real-time performance. FPGA realization is taken into full consideration during the project design of the top. In the end, this paper adopts the Simulink instrument in MATLAB and combines Altera's signal processing toolbox-DSPBuilder to implement the design scheme by the FPGA. It focuses on the description of FPGA implementation of the digitally controlled oscillator, CIC filter, half-band extracting filter and the low pass filter.

Categories and Subject Descriptors

C.5 [Computer and system implementation]: Digital assistants;
C.1.3 [Architectural Style]: Analog Computers; **C.3 [Special-Purpose and Application-Based Systems]:** Signal processing systems

General Terms

Digital Signal Processing, Digital Filters

Keywords: Direct Digital Synthesizer, DSPBuilder, Digital Down Converter

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1. Introduction

Software radio, as the key technology of present and future wireless communication system, has the fundamental features like broadband, open, programmable and so on. At present, Software radio mostly adopts the Digital Up/Down Converter technology to make itself work because of the process processing speed limitation of A/D/A and DSP chip. In the specific realization of the DDC, it is common to use the special DSP chip. However, the special

chip can't meet the design demand in the high speed signal processing because of its serial execution. At the present stage, it is reasonable to use FPGA device, which provides favorable conditions for the down conversion process of the software radio digital intermediate frequency with its abundant inside resource, parallel processing capacity, and efficient algorithm structure and reconfigurable, to realize the down converter.

The design and realization of the DDC has attracted extensive attention. Mu et al [2] has studied the algorithm of the DDC and optimized the filter by Distributed Arithmetic (DA). The algorithm essence of DA is to change multiplications and additions into table-look-up method because the bit depth of the table equals the filter tap coefficient N, and its scale will increase exponentially along with the increase of N. MalmirChegini et al [3] firstly come up with a kind of algorithm based on FFT and then they give a simplified iterative algorithm for improving the quality of reconstructed baseband signal. Sun et al mainly pay attention to the CIC numerical part of DDC and the Simulink imitation and modeling of the digital mixed converter part. Based on the typical design trend, Cui et al customize DDC for the family wireless communication system, and on system level they mainly draw support from Matlab tool to structure DDC behavioral model. This paper adopts the multi-rate process technology, i.e. firstly conducting data CIC extraction, then HBF and at last low passes filtering. CIC doesn't need multiplication and can realize high speed filtering. HBF has high operation efficiency and good real time performance, Hogenauer structure is employed in the realization of multiple CIC and it can make the realization easy and occupies the least resource. The down converter in this paper obviously lowers the arithmetic speed of the mixer and the filter and thus making the design project easier to FPGA realization, at the same time, the project uses the advanced DDS (Direct Digital Synthesizer) technology, which obviously reduces the needed resource and quantization errors.

2. The Principle of DDC

The core of DDC is to mix intermediate-frequency signal

sampled by A/D with the local digit intermediate-frequency carrier signal from NCO (Numerically Controlled Oscillator) of DDC and down convert the intermediate-frequency signal to the base-band. The down conversion process can be realized from Equation (1) and (2). To put into the intermediate-frequency signal just as the Equation (1) shows. In Equation (1) $A(n)$ is the base-band sampled signal, f_o is the intermediate-frequency carrier frequency, and f_s is the sampling frequency

$$X(n) = A(n) \cos(2\pi f_o / f_s n) \quad (1)$$

After mixing the signal, the signal is expressed by Equation (2).

$$Y(n) = A(n) \cos(2\pi f_o / f_s n) \cos(2\pi f_{Lo} / f_s n) \quad (2)$$

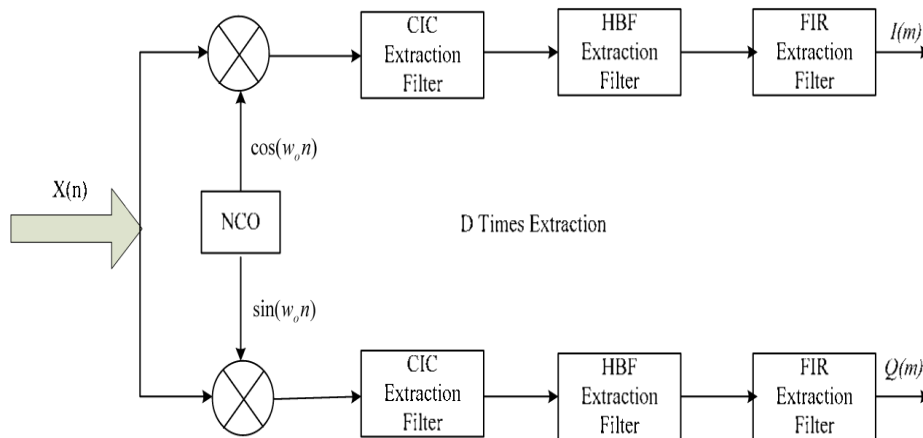


Figure 1. The Principle of DDC

Down conversion is completed. Its system chart, shown by Figure 1, mainly consists of 3 parts: digital oscillator, digital multiplier and digital filter.

In Figure 1, $X(n)$ is the digital signal transferred by high-speed 10-bit ADC; NCO module is the numerically controlled oscillator, and it produces sine wave signal $\cos(w_o n)$ and $\sin(w_o n)$ whose frequency equals that of intermediate-frequency signal. Then we can get base-band signal by multiplying the data transferred by high-speed ADC respectively with the signal produced by NCO (aiming at mixing).

ADC takes inter-mediate frequency sample so the sampling rate may be very high, and the after-mixing data rate equals the sampling rate. However, latter FIR filter can't reach this processing speed at all, then CIC and HBF need to make a general filter before FIR starts filtering. The coefficient of CIC filter is 1 makes it easy to realize, and a very high processing speed can be reached when the hardware works because it only has addition and subtraction without multiplication. Hence it is suitable for the first-grade extraction and huge extraction work in the extraction system. However, the attenuation characteristics of the transition zone and stop band are not so good, so usually the five-stage CIC cascade connection is adopted to increase the attenuation of the transition zone and stop band. The extraction factor is usually 1~32. HBF only has half computation of that of

In Equation (2), f_{Lo} is the local frequency of NCO, and generally $f_{Lo} = f_o$. According to The triangle function equation, we can get that:

$$Y(n) = A(n) * 1/2 * \{ \cos(2\pi(f_o - f_{Lo}) / f_s n) + \cos[2\pi(f_o + f_{Lo}) / f_s n] \} \quad (3)$$

It can be realized from Equation (3) that the after-mixing signal consists of both banes-band signal and high-frequency component. The low-pass filtering will filter the high-frequency signal. The output signal becomes base-band signal.

CIC because half of its coefficients are zero, so it is usually for the second-grade low-pass filter and extraction. The extraction factor of HB is 2, and it is especially suitable for the demand of making half sampling rate reduced. After the filtering action and extraction of CIC and HB, the base-band signal reaches a lower speed instead of the initial high data speed and is suitable for next FIR process. FIR mainly functions are as a shaping filter for the whole signal channel and as well as a matched filter when there is need.

3. Design And Implement of DDC On FPGA

The tradition implement method of DDC is to separate the system design and the concrete realization, which has several problems such as complex development, long design cycle, high development costs and so on. This paper designs the converter with the help of DSPBuilder system-level tool. DSPBuilder is a connector between software QuartusII and MATLAB/Simulink. We firstly analysis, simulate and verify the algorithm in MATLAB/Simulink, secondly we convert the file(.mdl) in MATLAB/Simulink into VHDL language with the help of DSPBuilder, then in the Quartus II we carry out synthesis and simulation and download it into FPGA for empirically validation. Next, we will elaborate the four vital components of DDC: FPGA realization of digitally controlled oscillator, CIC filter, HBF and low-pass filter, respectively.

3.1 Design of digitally controlled oscillator

In this paper we adopt Direct Digital Synthesis (DDS) technology to realize NCO. NCO mainly consists of phase accumulator and ROM look-up tables for sine and cosine. Phase accumulator outputs different phase sequences as the address for ROM according to the different input frequency controlled words. Inside ROM there are all the amplitude codes of one cycle of an output wave, so a serial of discrete amplitude codes can be got during addressing.

In the design of DDC, a pair of orthogonal sine and cosine signal is needed for Orthogonal mediation, so NCO need two ROM look-up tables. ROM look-up chart can change the phase to range of the output signal, the input is the sum of phase registers and phase control words as well as the address value of ROM, and the duration is usually P bits, just the same as the output data. In our design, we make a precise choice of P. P can't be too big, if it is

too big the ROM capacity will increase manifold and the output wave will get noobvious improvement with the limitation of D/A precision. Though the bit of the phase accumulator is N, we only need to take the high P bit and look up the table and make truncation to reduce quantization errors. During the design we take advantage of symmetry of sine (cosine) function to optimize memory space. In the range from 0 to 2π , the sine functional takes $x = \pi$ as its symmetry axis, while in the range from 0 to π , $x = \frac{1}{2\pi}$ is the symmetry axis. Hence, in the sine function chart we can only store the function values whose angles are between 0 to $\frac{1}{2\pi}$, and all these values are positive. Knowing this, we can get the whole sine and cosine periodical charts with some proper changes of the first 1/4 cycle of the sine code chart and save nearly 3/4 ROM resource.

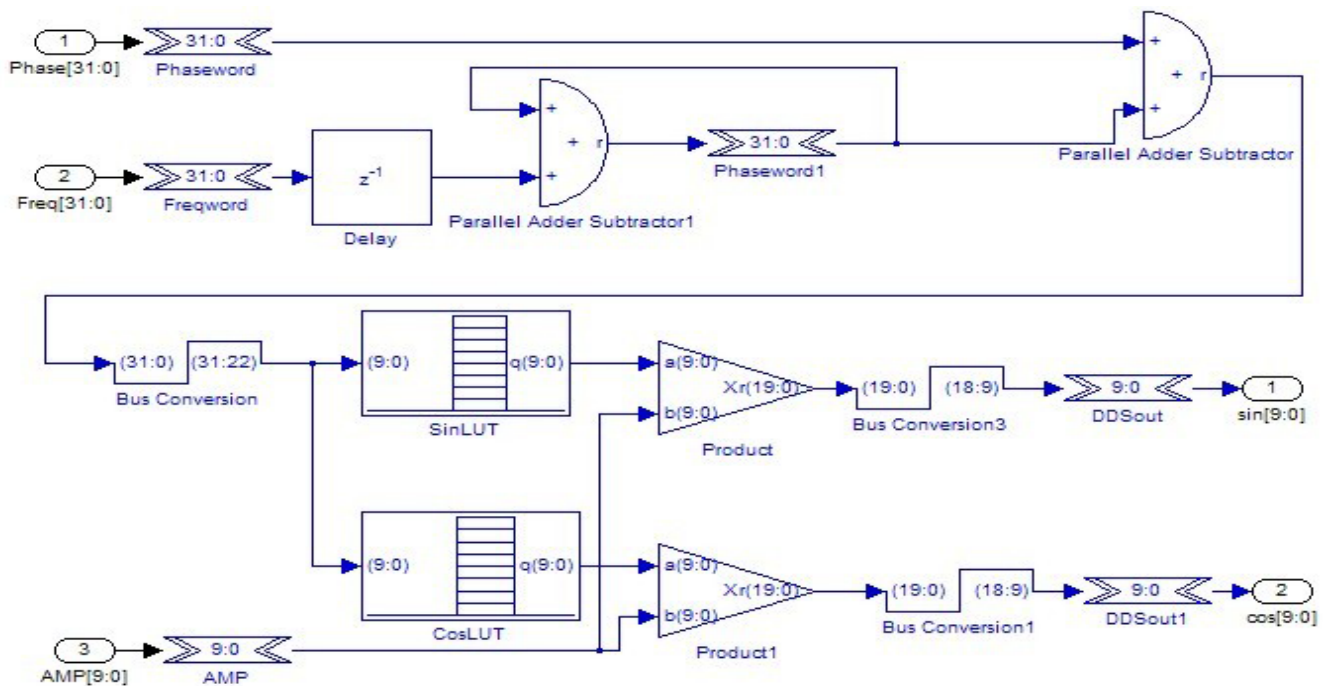


Figure 2. The model of NCO

The model of NCO with the help of DSPBuilder is shown in the Figure 2. The inputs of NCO module are phase, frequency and amplitude, where the phase and amplitude are fixed, and the frequency can be controlled, and the output is 10-bit sine wave and cosine wave. Figure 3 is a simulation wave in Simulink, from which we can realize that the output wave only has slight errors and high resolution ratio.

3.2 Design of CIC

CIC filter is cascaded by integrator and comb filter. In order to increase the stop band attenuation, it usually cascades several integrator filters. If we cascade N Integrator filters, then the amplitude-frequency response can be represented as Equation (4) :

$$H(Z) = \left(\frac{1 - Z^{-DM}}{1 - Z^{-1}} \right) \quad (4)$$

After being transferred by Noble, a Hogenauer decimation filter can be got. In the high-speed design we set D 1 or 2. The system level scheme of Hogenauer decimation filter is shown in Figure (4). This kind of structure is most easy to realize and it occupies the least resource. In reality, we adopt DSPBuilder to structure 5-grade CIC filter. The model the CIC filter is shown in Figure (5).

As shown in Figure 6, the sine wave with noise will become smoother and recover to the original wave that without interference.

3.3 Design of Half-Band Filter (HBF)

HBF is the FIR filter whose frequency response $H(e^{jw})$

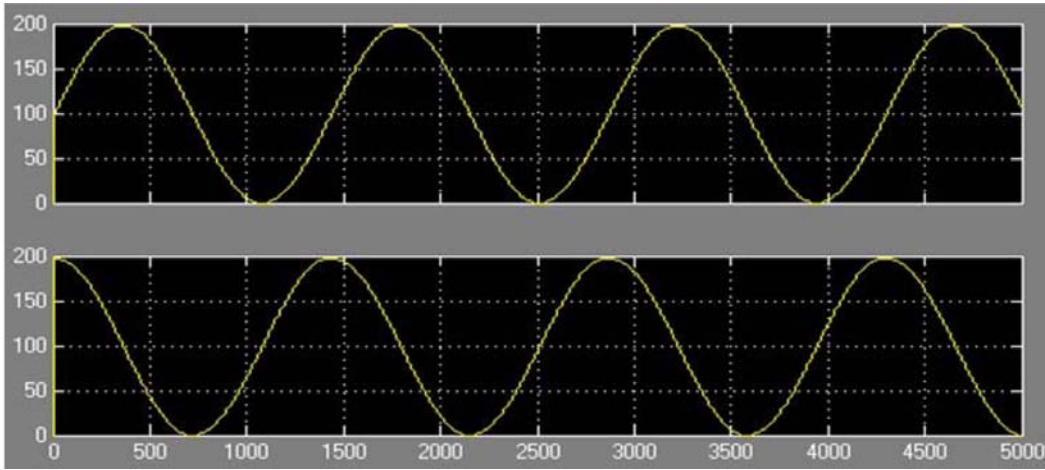


Figure 3. The sine and cosine wave generated by NCO

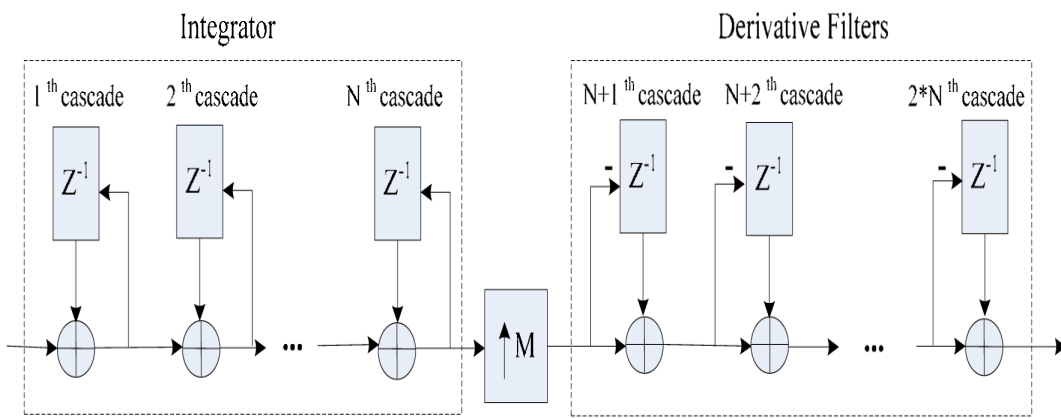


Figure 4. The system level scheme of Hogenauere extractor

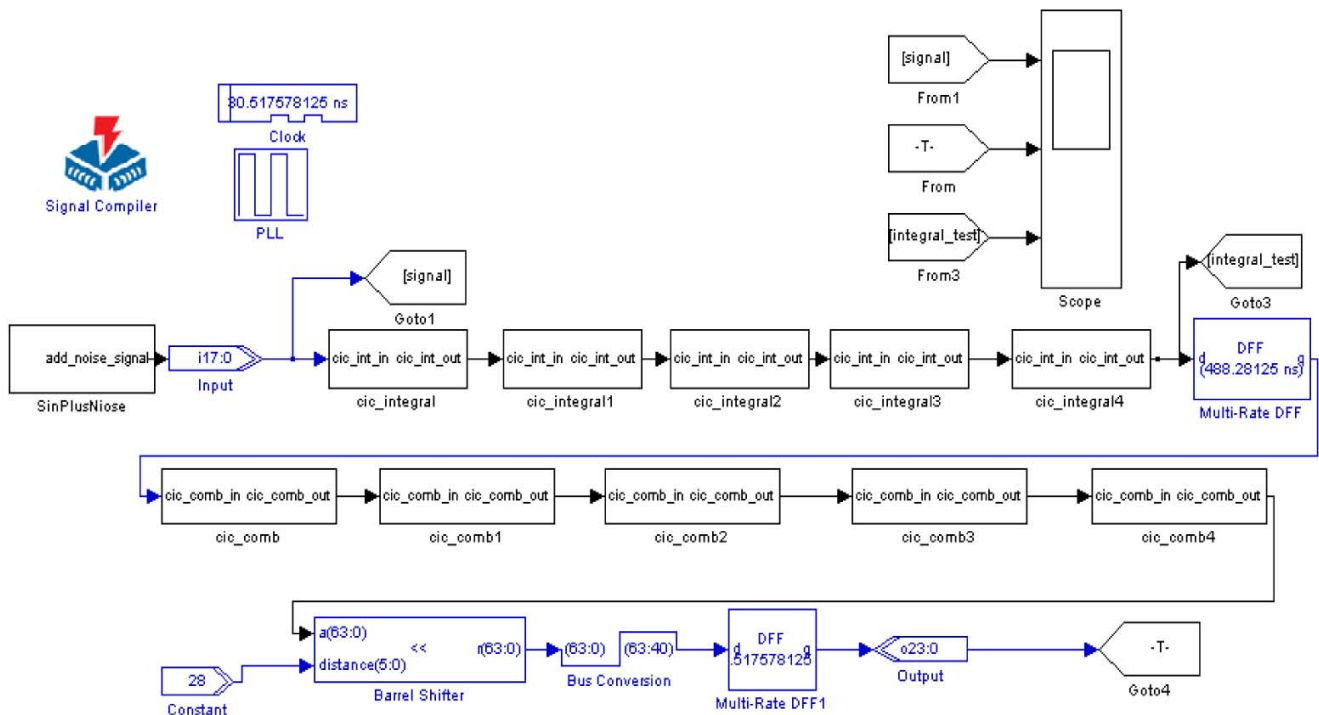


Figure 5. The model of CIC filter

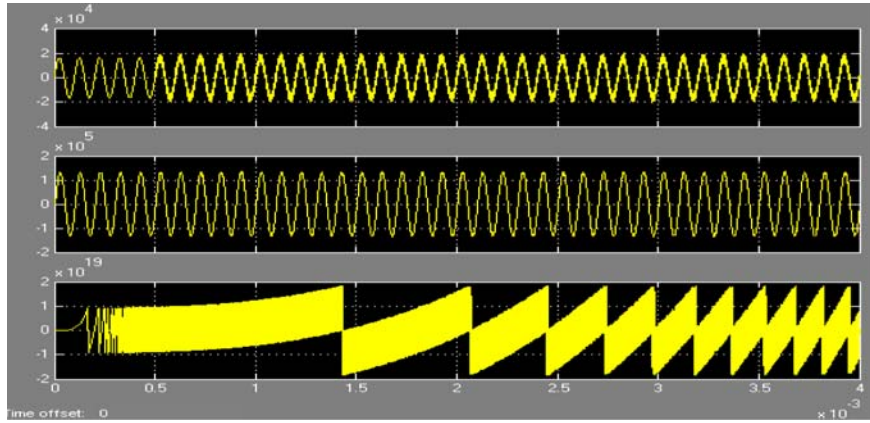


Figure 6. The simulation result of CIC in MATLAB

matches formula (5)

$$w_A = \pi - w_c, \delta_s = \delta_p = \delta \quad (5)$$

Or we can say that HBF stop band's width $\pi - w_a$ equals w_c , the width of pass band, and so does their ripples. HBF has a vital function in the multi-rate signal processing because this kind of filter is especially suitable for the realization of extractor and interpolation within the range of $D = 2^m$, and it has high computing efficiency and real-time characteristic. It can be proved that HBF has the features which Equation (6) (7) (8) show:

$$H(e^{jw}) = 1 - H(e^{j(\pi - w)})$$

$$H\left(e^{j\frac{\pi}{2}}\right) = 0.5$$

$$h(k) = \begin{cases} 1, & k = 0 \\ 0, & k = \pm 2, \pm 4, \dots \end{cases}$$

According to these features, we can work out the model of the HBF which is shown in Figure 7. After going through HBF, the measured signal's frequency gets higher and then decays, as shown in Figure 8.

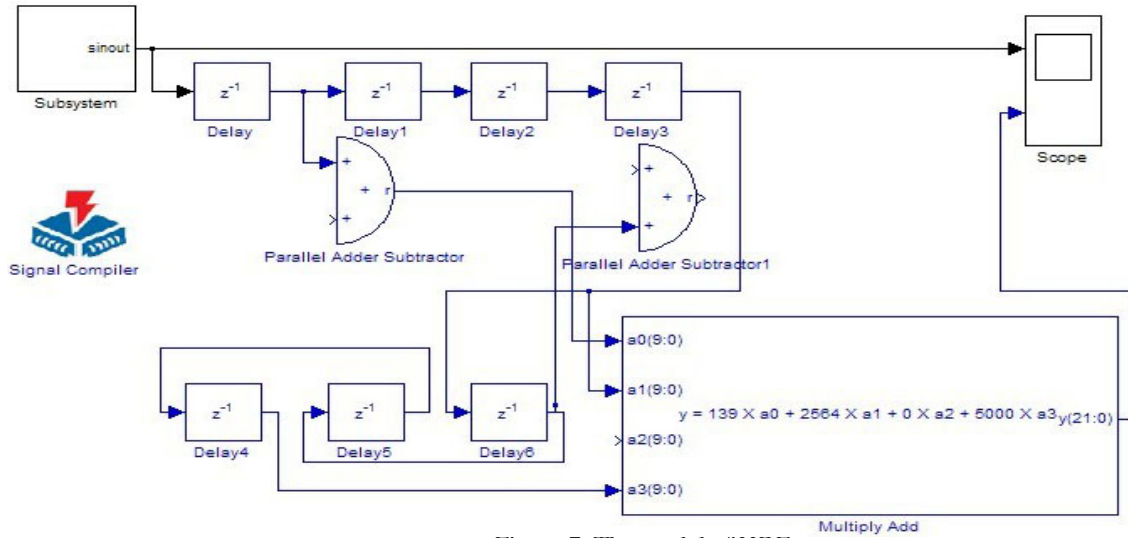


Figure 7. The model of HBF

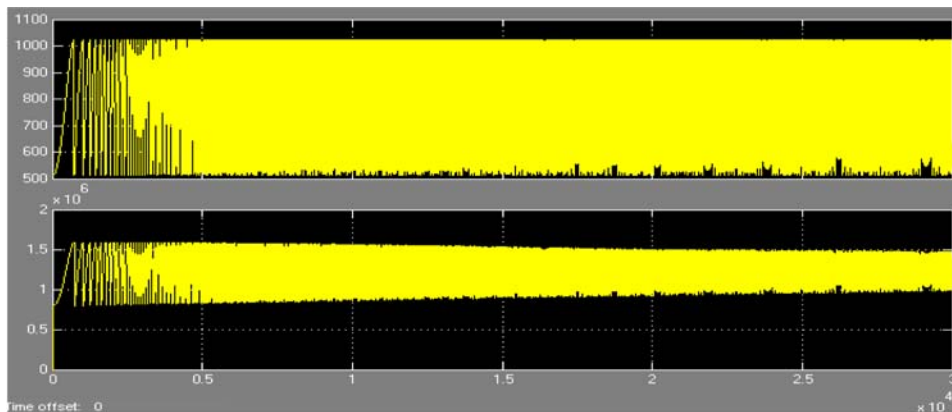


Figure 8. The simulation result of HBF

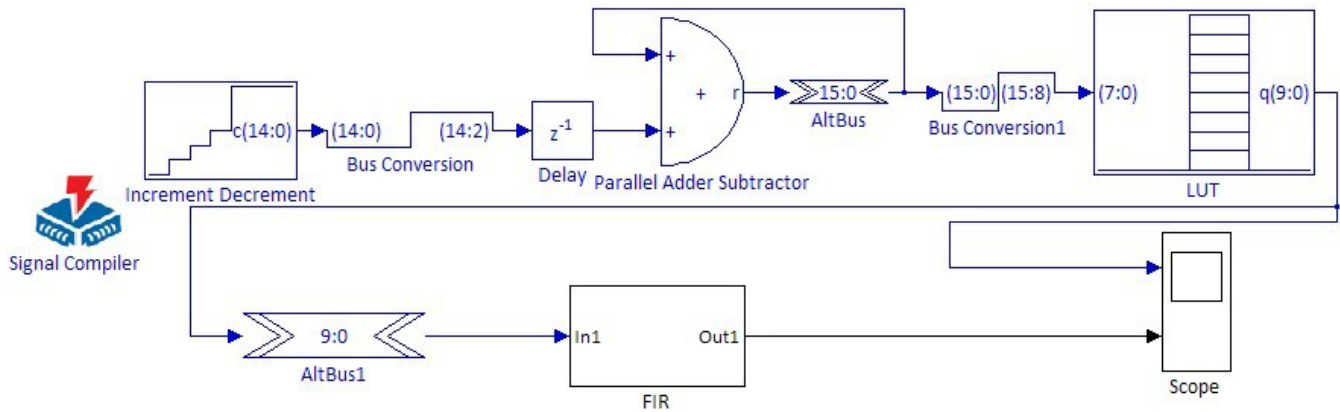


Figure 9. The model of FIR low-pass filter

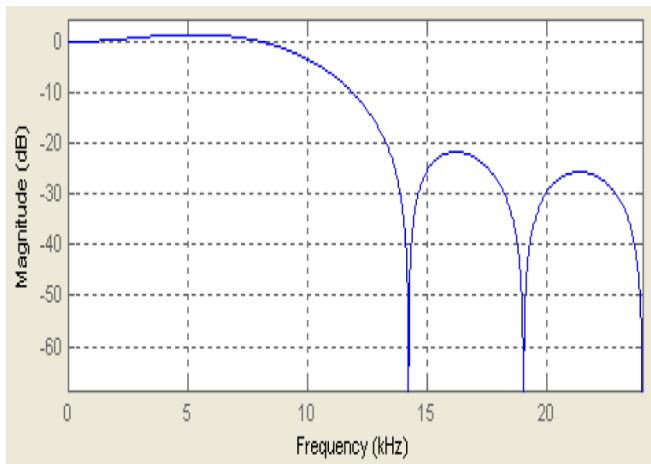


Figure 10. The amplitude-frequency curve of FIR low-pass filter

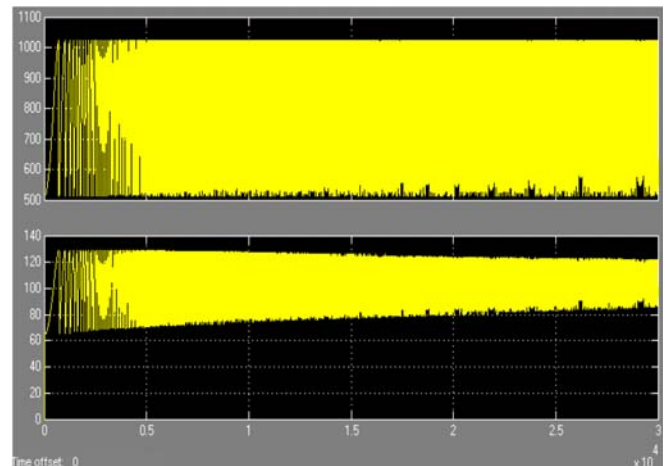


Figure 11. The simulation result of FIR in MATLAB

3.4 Design of Low Pass Filter (FIR)

The FIR filter in this paper adopts linear structure and mainly consists of shift register, multiplying unit and summing unit. In reference to the principle of FIR filter, in the simulation environment of Simulink we can realize a simple FIR filter and complete simulation and configuration of FPGA. In DSPBuilder, the model of FIR low-pass filter is shown in Figure 9.

The filter's amplitude-frequency curve is shown in Figure 10. The amplitude of the measured signal has weakened when its frequency gets higher, like Figure 11 shows.

4. Conclusion

DDC (DDC), as a key component of Digit Receivers, aims to get low-speed digital base-band signals by extracting and filtering the digital signals transformed by high-speed ADC. This paper make full use of MATLAB's Simulink instrument and Altera's signal processing toolbox---- DSPBuilder to design DDC and work out the model. The improved DDS technology not only overcomes the disadvantages of the traditional methods but also reduces errors and software resource. Hogenauer decimation filter makes it easy to extract wave and reduces software

resource. The simulation result indicates the effectiveness of the project.

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