0.35V, 4.1μW, 39MHz Crystal Oscillator in 40nm CMOS

Akira Saito[1], Yunfei Zheng[2], Kazunori Watanabe[1], Takayasu Sakurai[2], and Makoto Takamiya[2]
[1] Semiconductor Technology Academic Research Center (STARC), Yokohama, Japan,
[2] University of Tokyo, Tokyo, Japan
[1]{saito.akira, watanabe.kazunori}@starc.or.jp, [2]{yfzheng, tsakurai, mtaka}@iis.u-tokyo.ac.jp

ABSTRACT
A design methodology for sub-0.5V crystal oscillators is shown to realize an all-sub-0.5V ultra low power RF transceiver for wireless sensor networks. To reduce the minimum operating voltage (V_{DDmin}) of the crystal oscillator, both the optimization of the gate width of the CMOS inverter in the crystal oscillator and the reduction in gate length by CMOS technology scaling are required. In accordance with the developed design methodology, a 39MHz crystal oscillator is designed and fabricated in a 40nm CMOS. The measured power consumption is 4.1μW at 0.35V and 39MHz, and the power supply voltage is the lowest among the previously reported crystal oscillators.

Categories and Subject Descriptors
B.7.1 [**Hardware**]: Integrated Circuits, Types and Design Styles –*Advanced technologies*

General Terms
Measurement, Performance, Design

Keywords
Crystal oscillator, Pierce oscillator, Sub-threshold characteristics, Low Power, Low Voltage, Wireless Sensor Networks

1. INTRODUCTION
An ultra low power RF transceiver is required for wireless sensor networks. Reducing the power supply voltage (V_{DD}) is effective for reducing the power consumption of the transceiver. Sub-0.5V RF receiver circuits [1-4] have been reported. V_{DD} is 0.5V in [1-3] and 0.25V in [4]. A sub-0.5V FBAR oscillator using a forward-biasing bulk has been reported [5]. A sub-0.5V crystal oscillator, however, has not yet been reported. Without a sub-0.5V crystal oscillator, all-sub-0.5V low power RF transceiver cannot be realized. The feasibility of the sub-0.5V operation of a crystal oscillator, however, has not yet been clarified. Therefore, the purpose of this study is to clarify a design methodology for the sub-0.5V crystal oscillator and to demonstrate the sub-0.5V ultra low power operation of the crystal oscillator in a 40nm CMOS. The target frequency of the crystal oscillator is 39MHz. This frequency is multiplied by 8 by a 0.6V injection-locked frequency multiplier [6], and the generated frequency of 315MHz is used as the carrier frequency.

The remainder of this paper is organized as follows. Section 2 presents the design of the sub-0.5V crystal oscillator. Section 3 presents the measured results of the crystal oscillator in a 40nm CMOS. Finally, Section 4 presents the conclusion of this paper.

ISLPED'12, July 30– August 1, 2012, Redondo Beach, California, USA.

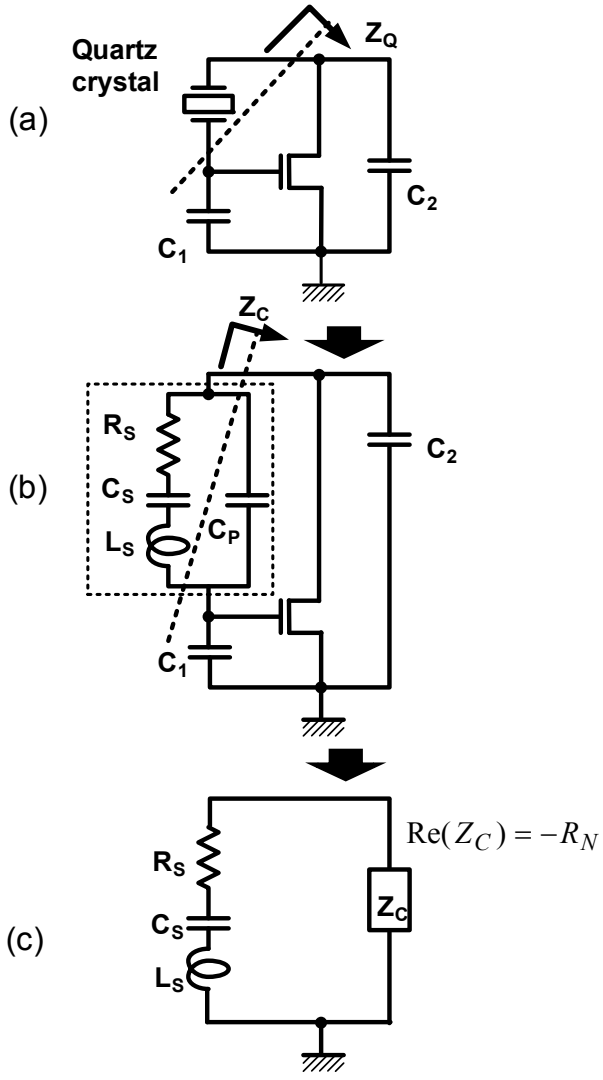

Figure 1: Pierce crystal oscillator. (a) Basic circuit (biasing omitted). (b) Equivalent circuit. (c) Equivalent circuit of (b).

2. DESIGN FOR SUB-0.5V CRYSTAL OSCILLATOR

2.1 Principle of Pierce Oscillator

In the design of a crystal oscillator, the negative resistance is an important design parameter. An oscillator circuit oscillates when the magnitude of the negative resistance is larger than the resistive loss in the quartz crystal. However, an MOS transistor itself does not exhibit I-V characteristics with a negative resistance as observed in a tunnel diode. The Pierce oscillator produces a negative resistance with a transistor and capacitors, and is a typical crystal oscillator.

Figure 1(a) depicts the Pierce crystal oscillator. The quartz crystal and load capacitors (C_1 and C_2) are connected to an nMOSFET. Figure 1(b) shows an equivalent circuit of the Pierce oscillator. The quartz crystal is represented as a serial connection of R_S, C_S, and L_S, and a shunt capacitor (C_P). In the Pierce oscillator, the circuit impedance Z_Q excluding that of the quartz crystal, is expressed as [6]

$$Z_Q = \frac{1}{j\omega C_1} + \frac{1}{j\omega C_2} + \left(\frac{1}{j\omega C_1}\right) \times g_m \times \left(\frac{1}{j\omega C_2}\right), \tag{1}$$

where ω is the angular frequency of oscillation and g_m is the transconductance of the transistor. The real part of Z_Q corresponds to the negative resistance ($-R_{NQ}$, $R_{NQ} > 0$) observed from the quartz crystal. $-R_{NQ}$ is expressed as [7]

$$\mathrm{Re}(Z_Q) = \left(\frac{1}{j\omega C_1}\right) \times g_m \times \left(\frac{1}{j\omega C_2}\right) = -\frac{g_m}{\omega^2 C_1 C_2} \equiv -R_{NQ} \,. \tag{2}$$

The negative resistance is realized by the multiplication of $1/j\omega C_1$ and $1/j\omega C_2$. To increase R_{NQ}, g_m should be increased and C_1 and C_2 should be decreased.

Figure 1(c) shows a circuit equivalent to that in Figure 1(b). The total impedance, excluding R_S, C_S, and L_S, is denoted as Z_C. Z_C consists of Z_Q and C_P, and is thus expressed as [8]

$$Z_C = \left(\frac{1}{j\omega C_P}\right) // Z_Q \,. \tag{3}$$

The real part of Z_C is the negative resistance ($-R_N$, $R_N > 0$) observed from the serial connection of R_S, C_S, and L_S. By substituting Equations (1) and (2) into Equation (3), R_N is expressed as [6]

$$\mathrm{Re}(Z_C) = -\frac{g_m C_1 C_2}{(g_m C_P)^2 + \omega^2 (C_1 C_2 + C_P C_2 + C_P C_1)^2} \equiv -R_N \,. \tag{4}$$

When $C_P = 0$, Equation (4) is equal to Equation (2).

In chip implementation, a Pierce oscillator with a CMOS inverter is often used. Figure 2 shows a Pierce crystal oscillator with a CMOS inverter. The nMOSFET in Figure 1(a) is replaced with the CMOS inverter and a feedback resistor (R_F). R_F induces half V_{DD} biasing to the CMOS inverter. The Pierce oscillator with the CMOS inverter in Figure 2 is equivalent to the Pierce oscillator in Figure 1, assuming that g_m in Equation (4) is determined by the parallel connection of the nMOSFET and pMOSFET.

2.2 Design Strategy for Sub-0.5V Operation

In this section, a design strategy for the sub-0.5V crystal oscillator is discussed. Figure 3 shows the relationships between the condition required for oscillation and the circuit parameters in the Pierce crystal oscillator. The crystal oscillator oscillates when it satisfies the condition

$$R_N \geq R_S \,, \tag{5}$$

where R_S is the parasitic resistance of the quartz crystal shown in Figure 1(b). Equation (2) shows that R_{NQ} is proportional to g_m. Equation (4) also shows that R_N depends on g_m. In the above-threshold region, where the gate-to-source voltage (V_{GS}) is larger than the threshold voltage (V_{TH}), g_m of the MOSFET is expressed as

$$g_m \propto \frac{W}{L}(V_{GS} - V_{TH}), \tag{6}$$

where L is the gate length and W is the gate width. When V_{DD} and V_{GS} are reduced, g_m and R_N decrease, terminating the oscillation. To keep g_m constant when V_{DD} is reduced, W/L should be linearly

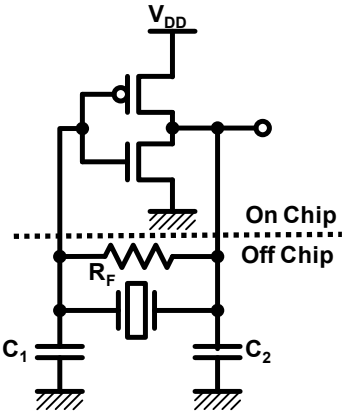

Figure 2: Pierce crystal oscillator with CMOS inverter.

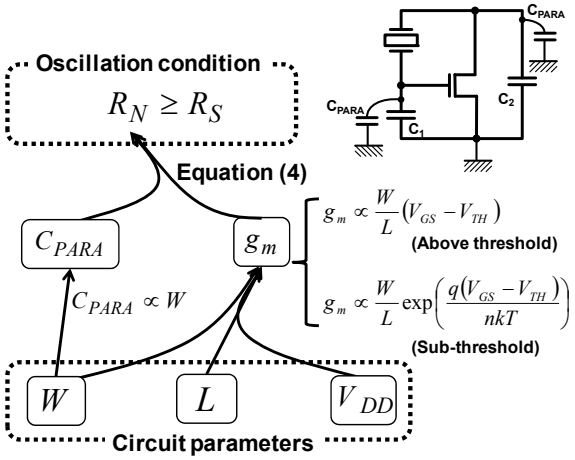

Figure 3: Relationships between condition required for oscillation and circuit parameters in Pierce crystal oscillator.

increased approximately proportionally to $1/V_{DD}$. In contrast, in the sub-threshold region, where V_{GS} is smaller than V_{TH}, g_m of the MOSFET is expressed as

$$g_m \propto \frac{W}{L}\exp\left(\frac{q(V_{GS}-V_{TH})}{nkT}\right), \quad (7)$$

where q is the elementary electric charge, n is constant (1<n<2), k is the Boltzmann coefficient, and T is the absolute temperature. To keep g_m constant when V_{DD} is reduced, W/L should be exponentially increased approximately proportionally to $1/\exp(V_{DD})$. When W is increased, the parasitic capacitance of the transistor (C_{PARA}) also increases because

$$C_{PARA} \propto W \ . \quad (8)$$

According to Equation (4), R_N decreases as C_{PARA} increases, because C_{PARA} is added to C_1 and C_2. Therefore, a large W increases R_N by increasing g_m, while it reduces R_N by increasing C_{PARA}. The trade-off relation suggests that an optimal W exists to minimize V_{DDmin}. The reduction of L increases g_m, and the minimum L is determined by CMOS technology. CMOS technology down scaling also reduces C_{PARA}, thereby increasing R_N.

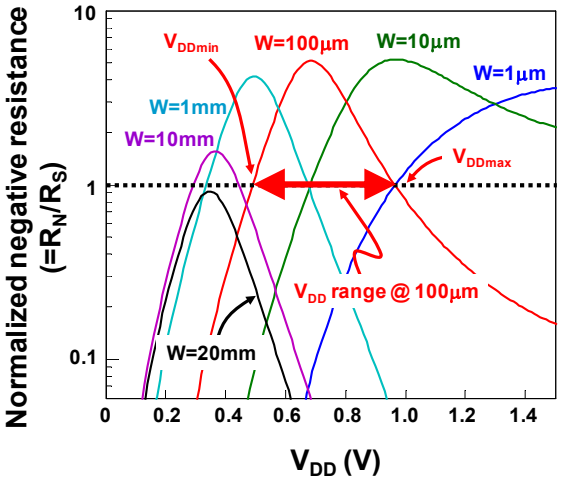

Figure 4: Simulated dependence of negative resistance (R_N) normalized by R_S on V_{DD} in crystal oscillator. The crystal oscillator can oscillate when $R_N/R_S > 1$.

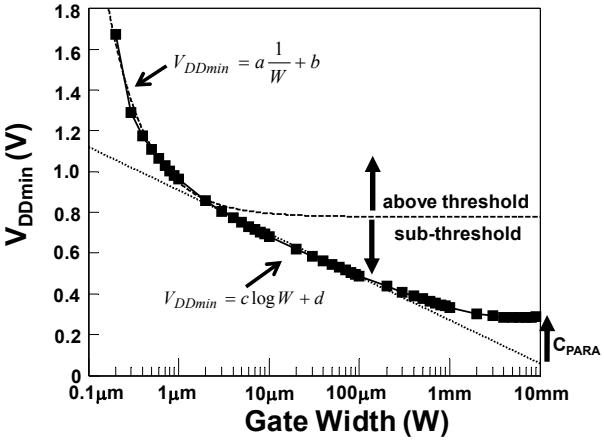

Figure 5: Simulated dependence of V_{DDmin} on W at L=40nm.

2.3 Gate Width Optimization

In this section, optimization of the gate width (W) to reduce V_{DDmin} for the crystal oscillator is discussed. Figure 4 shows the simulated dependence of the negative resistance (R_N) normalized by R_S on V_{DD} in the crystal oscillator. In this SPICE simulation, the W values of the nMOSFET and pMOSFET are the same. L is fixed to 40nm. The resonant frequency of the quartz crystal is 39MHz. The other simulation conditions are R_S=60Ω, C_1=C_2=5pF, and R_F=500kΩ. The crystal oscillator can oscillate when R_N/R_S > 1. This figure clearly shows that an increase in W reduces V_{DDmin}. In the case of $W \le 1$ µm, the crystal oscillator requires V_{DD} above 1.0V to oscillate. The sub-0.5V oscillation requires $W \ge 100$ µm. For example, in the case of $W = 100$ µm, V_{DDmin} (= V_{DD} at R_N/R_S = 1) is 0.49V and the maximum operating V_{DD} (V_{DDmax}) (= V_{DD} when R_N/R_S = 1) is 0.97V. The operating range of V_{DD} is 0.48V (=V_{DDmax}-V_{DDmin}).

In Figure 4, R_N/R_S at W = 1µm *monotonically* increases with V_{DD}, because the transistors operate in the above-threshold region. As shown by Equation (6), g_m *linearly* depends on V_{GS}, and R_N monotonically increases with V_{GS}, as shown by Equation (4). In contrast, R_N/R_S at W > 10µm does not *monotonically* increase with V_{DD}, because the transistors operate in the sub-threshold region. As shown by Equation (7), g_m *exponentially* depends on V_{GS}, and R_N increases in the low-V_{DD} region and decreases in the high-V_{DD} region with increasing V_{GS}, as shown by Equation (4).

Figure 4 also shows that an increase in W reduces the peak value of R_N/R_S. As W increases, both V_{DDmin} and V_{DDmax} decrease and the V_{DD} range (V_{DDmax}-V_{DDmin}) also decreases. At $W \ge 20$ mm, the crystal oscillator cannot oscillate for all values of V_{DD}. This can be explained by the increased C_{PARA} caused by the increases in W, because C_{PARA} is added to C_1 and C_2.

Figure 5 shows the simulated dependence of V_{DDmin} on W. The squares at high V_{DDmin} values (in the above-threshold region) can be fitted as

$$V_{DDmin} = a\frac{1}{W} + b, \quad (9)$$

at $W \le 1$ µm, as shown by the dashed line in Figure 5, where *a* and *b* are constants. The squares at low V_{DDmin} values (in the sub-threshold region) can be fitted as

$$V_{DDmin} = c\log W + d, \quad (10)$$

at $W > 1$µm, as shown by the dotted line in Figure 5, where *c* and *d* are constants. Equations (9) and (10) can be derived from Equations (6) and (7), respectively, assuming that g_m is constant. This curve fitting means that V_{DDmin} at $W \le 1$ µm is determined by the above-threshold operation, while V_{DDmin} at $W > 1$µm is determined by the sub-threshold operation. A V_{DD} of 0.8V is twice of the threshold voltage. At the gate width $W \ge 200$ µm, the squares shift away from the dotted line. This shift can be explained by the reduced negative resistance caused by the increase in C_{PARA} with increasing W. This results in the lower V_{DDmin} limit of 0.28V.

2.4 CMOS Technology Scaling

In this section, reduction of the gate length (L) by CMOS technology scaling to reduce V_{DDmin} for the crystal oscillator is discussed. Figure 6 illustrates the SPICE-simulated dependence of V_{DDmin} on W in the case of three different CMOS technologies. The L values are 40nm, 160nm, and 360nm in the 1.1V 40nm, 1.8V 160nm, and 3.3V 360nm CMOSs, respectively. The curve of the 1.1V 40nm CMOS is the same as that in Figure 6. As L decreases, V_{DDmin} decreases at a fixed W, because g_m is proportional to 1/L, as shown in Equations (6) and (7). As discussed for Figure 5, the lower limit of V_{DDmin} is determined by C_{PARA}. The lower limit of V_{DDmin} in the 40nm, 160nm, and 360nm CMOSs are 0.28V, 0.41V, and 0.78V, respectively. In this manner, the lower limits of V_{DDmin} is reduced by CMOS technology scaling, because C_{PARA} is reduced by CMOS technology scaling. Therefore, the CMOS technology scaling is effective for reducing V_{DDmin} for the crystal oscillator. For example, to achieve a sub-0.5V crystal oscillator, a 40nm or 160nm CMOS is required, as shown in Figure 6.

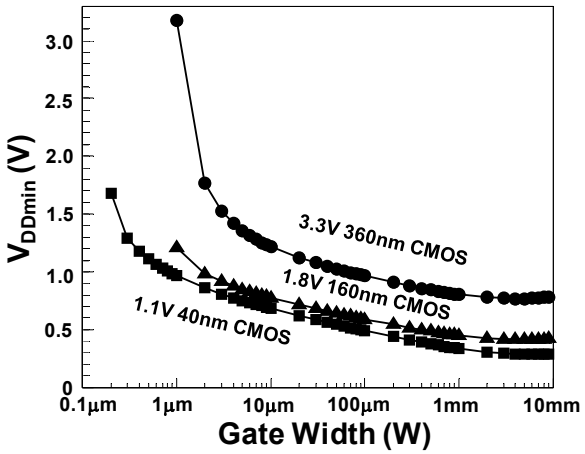

Figure 6: Simulated dependence of V_{DDmin} on W for three different CMOS technologies.

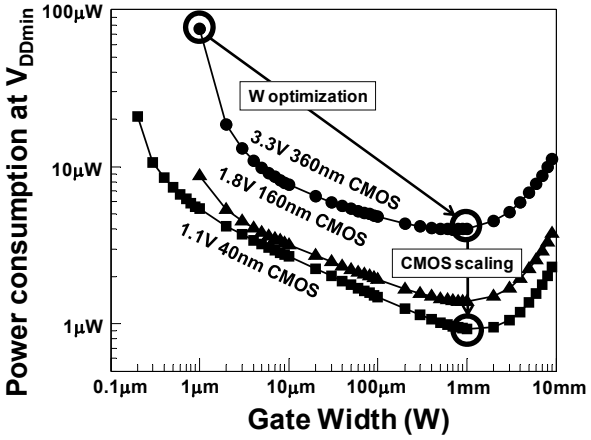

Figure 7: Simulated dependence of power consumption at V_{DDmin} on W for three different CMOS technologies.

2.5 Low Power Design

In this section, the reduction of power by reducing V_{DDmin} for the crystal oscillator is discussed. Figure 7 depicts the SPICE-simulated dependence of the power consumption at V_{DDmin} on W for three different CMOS technologies. The power consumption is minimum at $W = 1$ mm in all three different CMOS technologies. At $W \geq 1$ mm, although V_{DDmin} is constant, as shown in Figure 6, the power consumption increases with increasing W, because C_{PARA} increases and the relevant switching power also increases.

In summary, as shown in Figure 7, the design strategy to reduce V_{DDmin} for the crystal oscillator involves (1) the optimization of W and (2) the reduction of L by CMOS technology scaling. W has an optimum value, because the large W increases R_N by increasing g_m, but it reduces R_N by increasing C_{PARA}. The reduction of L increases g_m and reduces C_{PARA}, thereby increasing R_N and reducing V_{DDmin}, as shown in Figure 3.

3. MEASUREMENT RESULTS

3.1 Chip Implementation

In accordance with the developed design methodology, a 39MHz crystal oscillator is designed and fabricated in a 1.1V 40nm CMOS. Figure 8 shows the chip microphotograph and layout of the crystal oscillator. The core area is 80µm x 130µm. The worst-

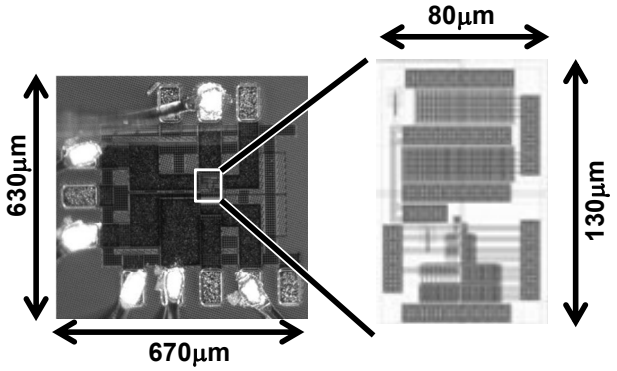

Figure 8: Chip photograph and layout of crystal oscillator.

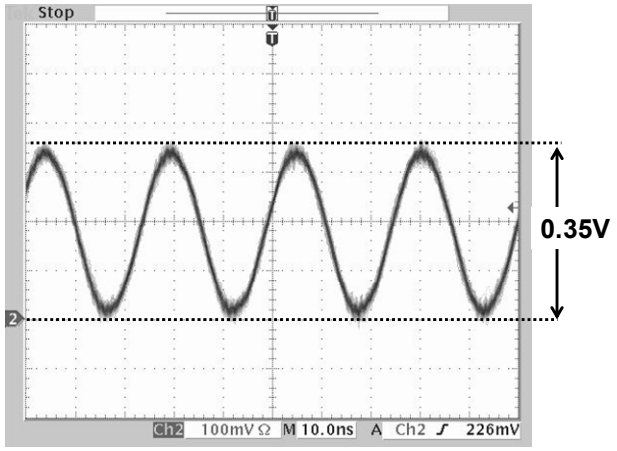

Figure 9: Measured output waveform of 39MHz crystal oscillator at V_{DD}= V_{DDmin} = 0.35V.

case R_S of the quartz crystal shown in the spec sheet is 60Ω. The value of W for the crystal oscillator is optimized to 220μm by considering the worst-case R_S and the oscillator margin for tolerances. This chip is implemented in a PCB with off-chip components such as capacitors (C_1=C_2=5pF).

3.2 Measurements

The measured V_{DDmin} of the 39MHz crystal oscillator is 0.35V. Figure 9 shows the measured output waveform of the 39MHz crystal oscillator at V_{DDmin} = 0.35V. It shows a clear sinusoidal waveform with full swing. Figure 10 shows the measured spectrum of the 39MHz crystal oscillator at V_{DDmin} = 0.35V.

In the measurement, oscillation was observed in the V_{DD} range from 0.35V to 1.1V. The measured V_{DD} range is wider than the simulated V_{DD} range from 0.45V to 0.85V at W=220μm. The mismatch is due to the error in R_S. In the S-parameter measurement of the quartz crystal using a vector network analyzer,

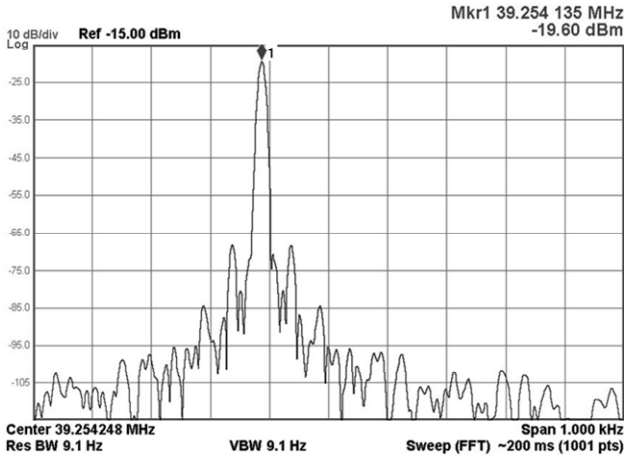

Figure 10: Measured spectrum of 39MHz crystal oscillator.

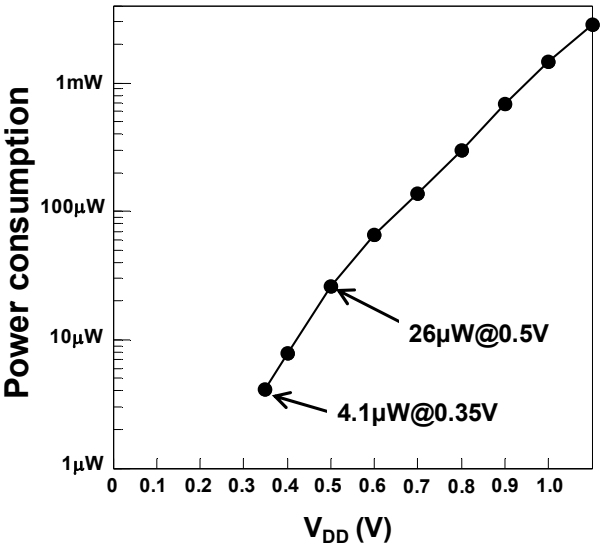

Figure 11: Measured dependence of power consumption on V_{DD} in 39MHz crystal oscillator.

Table I: Performance comparison with previous crystal oscillators.

Reference		[9]	[10]	[11]	[12]	This Work
Frequency	MHz	2.1	2.1	2.1	19	39
CMOS process	μm	3.0	NA	2.0	0.1	0.04
V_{DD}	V	1.5	1.3	1.8	1.2	0.35
Power	μW	1.4	3.0	0.7	21.6	4.1

the measured R_S is 10Ω, which is less than the worst-case R_S of 60 Ω shown in the spec sheet. The smaller than expected R_S results in the wider measured V_{DD} range than that obtained by simulation.

Figure 11 shows the measured dependence of the power consumption on V_{DD} in the 39MHz crystal oscillator. The curve exhibits an exponential dependence on V_{DD} due to the sub-threshold operation. The power consumption is 26μW and 4.1μW at V_{DD} values of 0.5V and 0.35V, respectively.

Table I shows a performance comparison with previously reported crystal oscillators [9-12]. In this work, V_{DD} is the lowest among the previously reported crystal oscillators.

4. CONCLUSION

In this paper, the design methodology for sub-0.5V crystal oscillators is shown to realize an all-sub-0.5V low power RF transceiver for wireless sensor networks. To reduce V_{DDmin} for the crystal oscillator, both the optimization of the gate width (W) and CMOS technology scaling are required. The optimum W is determined by g_m and the parasitic capacitance of the transistors. In accordance with the developed design methodology, a 39MHz crystal oscillator is designed and fabricated in a 40nm CMOS. The measured power consumption is 4.1μW at 0.35V and 39MHz, where both the power supply voltage is the lowest among the previously reported crystal oscillators.

5. ACKNOWLEDGMENTS

This work was carried out as a part of the Extremely Low Power (ELP) project supported by the Ministry of Economy, Trade and Industry (METI) and the New Energy and Industrial Technology Development Organization (NEDO).

6. REFERENCES

[1] N. M. Pletcher, S. Gambini, and J. M. Rabaey, "A 2GHz 52μW Wake-Up Receiver with -72dBm Sensitivity Using Uncertain-IF Architecture", IEEE International Solid-State Circuits Conference, pp. 524-525, Feb. 2008.

[2] X. Huang, S. Rampu, X. Wang, G. Dolmans, and H. de Groot, "A 2.4GHz/915MHz 51μW Wake-Up Receiver with Offset and Noise Suppression", IEEE International Solid-State Circuits Conference, pp. 222-223, Feb. 2010.

[3] A. Saito, K. Honda, Y. Zheng, S. Iguchi, K. Watanabe, T. Sakurai, and M. Takamiya, "An all 0.5V, 1Mbps, 315MHz OOK transceiver with 38-μW carrier-frequency-free intermittent sampling receiver and 52-μW Class-F transmitter in 40-nm CMOS, " IEEE Symposium on VLSI Circuits, June 2012. (To be presented)

[4] A. Heiberg, T. Brown, K. Mayaram, and T. S. Fiez, “A 250 mV, 352μW Low-IF Quadrature GPS Receiver in 130 nm CMOS”, IEEE Symposium on VLSI Circuits, pp.135-136, June 2010.

[5] A. Nelson, J. Hu, J. Kaitila, R. Ruby, B. Otis, “A 22μW, 2.0GHz FBAR Oscillator”, IEEE Radio Frequency Integrated Circuits Symposium, June 2011.

[6] L. Liu, M. Takamiya and T. Sakurai, “315MHz Energy-Efficient Injection-Locked OOK Transmitter and 8.4μW Power-Gated Receiver Front-End for Wireless Ad Hoc Network in 40nm CMOS”, IEEE Symposium on VLSI Circuits, pp.164-165, June 2011.

[7] B. Razavi, Design of Analog CMOS Integrated Circuits, McGraw-Hill, Oct. 2003.

[8] E. Vittoz, Low-Power Crystal and MEMS Oscillators -The Experience of Watch Developments-, Springer-Verlag, Sep. 2010.

[9] E. Vittoz, M. Degrauwe, and S. Bitz, “High-Performance Crystal Oscillator Circuits: Theory and Application”, IEEE Journal of Solid-State Circuits, pp.774 -783, June 1988.

[10] D. Lanfranchi, E. Dijkstra, and D. Aebischer, “A Microprocessor-Based Analog Wristwatch Chip with 3 Second/Year Accuracy”, IEEE International Solid-State Circuits Conference, pp. 92-93, Feb. 1994.

[11] D. Aebischer, H. J. Oguey, and V. R von Kaenel, “A 2.1-MHz Crystal Oscillator Time Base with A Current Consumption under 500 nA”, IEEE Journal of Solid-State Circuits, pp. 999– 1005, July 1997.

[12] R. van Langevelde, M. van Elzakker, D. van Goor, H. Termeer, J. Moss, and A. J. Davie, “An Ultra-Low-Power 868/915 MHz RF Transceiver for Wireless Sensor Network Applications”, IEEE Radio Frequency Integrated Circuits Symposium, pp. 113– 116, June 2009.