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Optimized Temperature in Phosphorous Diffusion Gettering Setup of Chromium Transition Metal in Solar Grade Multicrystalline p-Type Silicon Wafer

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We have investigated in this work the effect of the temperature profile during homogeneous phosphorous diffusion gettering (PDG) on multicrystalline (mc-Si) silicon p-type wafers destined for photovoltaic solar cells. Temperatures were varied from 800 °C to 950 °C with time cycle of 90 minutes. Phosphorous profile of n^+p junction was measured by secondary ion mass spectroscopy (SIMS) from 0.45 μm to 2.4 μm. Chromium concentration profile measured on the same samples by SIMS shows a high accumulated concentration of Cr atoms in the gettering layer at 900 °C and 950 °C, compared to samples obtained at 800 °C and 850 °C. The effective lifetime (τ_{eff}) of minority charge carriers characterized by quasi-steady state photoconductance (QSSPC) is in correlation with these results. From the QSSPC measurements we have observed an amelioration of τ_{eff} from 7 μs before PDG to 26 μs in the samples after PDG, processed at 900 °C. This indicates the extraction of a non-negligible concentration (5×10^{14} cm^{-3} to 5×10^{15} cm^{-3}) of Cr from the bulk to the surface gettering layer, as observed in the chromium SIMS profiles. A light degradation of τ_{eff} (18 μs) is observed in the samples treated at 950 °C due probably to a partial dissolution of the metallic precipitates, especially at the grain boundaries and in the dislocations vicinity. The related $\tau_{\mathrm{Cr\text{-}Impurity}}$ lifetime value of about 8.5 μs is extracted, which is the result of interstitial Cr_i or Cr_iB_s pairs, proving their strongest recombination activity in silicon.

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1. Introduction

Photovoltaic (PV) devices based on silicon (Si) are the most common solar cells currently being produced, and it is mainly due to silicon technology that the PV has grown by 40% per year over the last decade [1]. Gettering of transition metal elements and passivation procedures have been studied for many years and are used effectively to increase the efficiency of multicristalline silicon (mc-Si) which represents more than 55% of the Si PV modules production in the world annually due to the ingoting and wafering process cost, compared with the Czochralski (CZ) monocristalline Si wafers. Unfortunately, this material is characterized by a relatively high density of defects like dislocations, grain-boundaries and the presence of high amount of transition metal elements which act as recombination centers, reducing electrical charge carrier lifetime [2, 3]. The source of this high concentration of transition metal elements in the PV silicon wafers is due to the lower purity of the solar grade (SOG) feedstock used during the ingot growth cycle, as shown in Fig. 1 [2]. The main recombination activity sources in mc-Si wafers come from chromium (Cr) and iron (Fe). Several studies demonstrate that they create interstitial recombination centers and associate with the substitutional boron atoms to create pairs like Fe_iB_s, and Cr_iB_s,

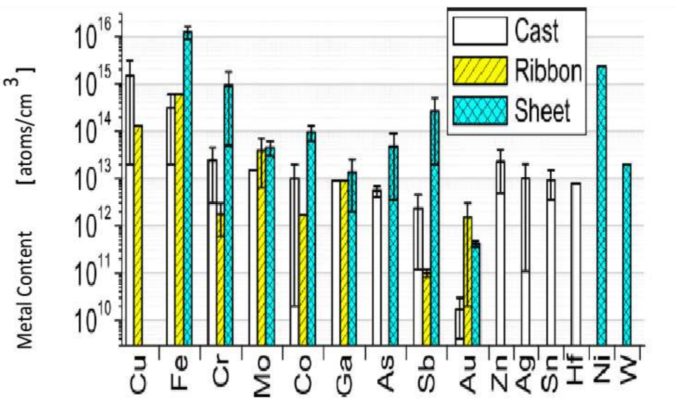

Fig. 1. Metal content in solar-grade silicon multicristalline ingot determined by NAA [2].

which act as acceptors and in some cases as donors depending on the energy position in the gap [4–8]. Table I illustrates the nature of recombination center of Fe and Cr in silicon and the relative capture cross-sections (σ_n, σ_p) in function of their position (interstitial or substitutional) and composition.

To avoid the effect of the transition metallic elements on the carrier lifetime in mc-Si wafer we concentrated on the optimization of the phosphorous diffusion gettering process in a determined range of time and temperature profile. The negative effect of transition metal elements is well known. Cr is detrimental to silicon-based devices,

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TABLE I

Energy levels and capture cross-sections for Fe and Cr-related recombination centers in silicon.

Recombination center	Energy level [eV]	σ_n [cm^{-2}]	σ_p [cm^{-2}]
Fe_i	E_V+0.38	5×10^{-14}	7×10^{-17}
Fe_iB_s acceptors	E_C-0.23	3×10^{-14}	2×10^{-15}
Cr_i	E_C-0.22	2.3×10^{-13}	1.1×10^{-13}
Cr_iB_s	E_V+0.27	1.4×10^{-13}	1×10^{-14}

because it strongly reduces the carrier lifetime of crystalline silicon wafer at a relatively high concentration of about 5×10^{14} cm^{-3}, as measured by SIMS in an earlier study [9].

2. Experiment

In our experiment mc-Si boron doped p-type wafers with resistivity of (1–3) Ω cm were used. All wafers originated from the same briquette and were adjacent. Firstly, the surface was chemically cleaned in NaOH:H_2O bath to remove the saw damage defects, followed by a neutralization step in HCl:H_2O for a few minutes to reduce the presence of Na atoms which act as electrical activation centers. Four batches of few wafers underwent a homogeneous phosphorous gettering process in a pressure controlled atmosphere with different temperatures in the range of 800 to 950 °C during 90 minutes. PDG setup was realized in a tube furnace using a phosphorus oxy-chloride ($POCL_3$) liquid as the diffusion source. The n^+p junction and the chromium profiles relative to each gettering run were measured using secondary ion mass spectroscopy (SIMS) — IMS4FE7 from Cameca, which has a relatively lower detection limit of transition metals than that of the Neutron Atomic Activation (NAA) (2×10^{14} cm^{-3} for Cr). The effective lifetime τ_{eff} measurements were performed using the WCT-120 quasi-steady-state photoconductance technique (QSSPC) to evaluate the effectiveness of the gettering in the mc-Si wafers.

3. Results and discussion

In Fig. 2, the n^+p junction SIMS profiles are illustrated in function of the temperature of the PDG setup. Surface concentration of phosphorous N_s is around 2×10^{21} cm^{-3} for samples treated at 800 °C and 850 °C and drops to 2×10^{20} cm^{-3} for those treated at 900 and 950 °C due to temperature-enhanced diffusion of P atoms. The depth profile is 0.4, 1.5, 1.7 and 2.5 μm for samples treated at 800, 850, 900 and 950 °C, respectively. From Fig. 2 we observe that a great amount of P atoms has quickly diffused into the bulk of the wafer via the crystallographic defects and grain boundaries bellow 0.5 μm in comparison with P profiles obtained at 800 and 850 °C, which indicates that the gettering layer is more important for processes at temperatures bellow 850 °C.

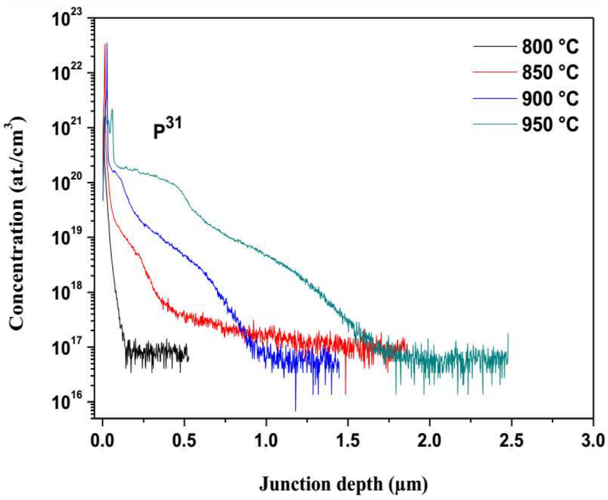

Fig. 2. SIMS spectra of phosphorous profile for different PDG processes.

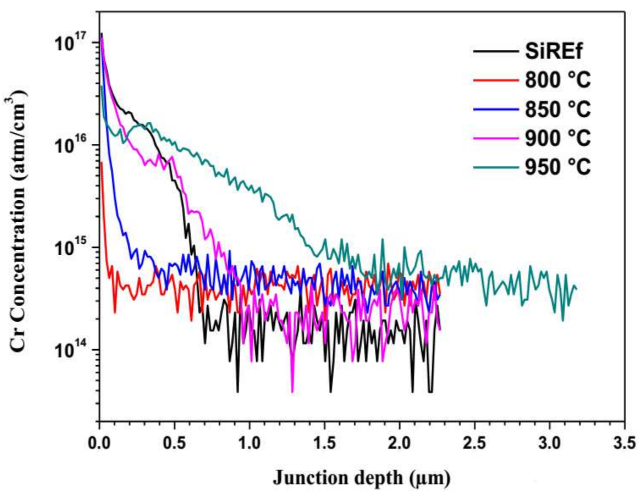

Fig. 3. Evolution of the SIMS profile of chromium in mc-Si with the temperature of PDG processes during 90 min.

After chemical etching of the gettering layer (20 μm from each face), we have characterized the chromium profile for the reference mc-Si wafer and those after the PDG. We can see that a high concentration of Cr atoms has diffused to the silicon surface at 900 °C and 950 °C, regarding their content in the reference sample, as shown in Fig. 3. A part of Cr atoms at relatively high temperature originate from a partial dissolution of precipitates of this metallic element in the vicinity of the crystallographic defects, grain-boundaries. On other hand, the Cr concentration at 800 and 850 °C is lower than that measured in Si-Ref, as a result of low migration of this metallic element to the surface of the treated silicon wafers.

Because the QSSPC technique is very sensitive to surface passivation, before each τ_{eff} measurement, the wafers were chemically cleaned in a piranha etch sequence: HF 10% + H_2SO_4:H_2O_2 at 80 °C for 15 min + HF 10%

to etch the chemically grown SiO_2 layer. The values of τ_{eff} are determined at excess carrier density $n = 1 \times 10^{15}$ cm^{-3} to avoid the effect of the traps in the low injection region. Figure 4 illustrates the effective lifetime measured on mc-Si wafers before and after PDG gettering process. The best amelioration of $\tau_{\mathrm{eff}} = 26$ μs is obtained with PDG run at 900 °C. Remember that the initial values of minority carrier lifetime was around 7 μs. With the PDG runs at 800 °C and 850 °C the lifetime is lightly affected by the gettering process with values of 10 and 11 μs, which indicates a low level of migration of the transition metallic elements from the bulk to the surface. Nevertheless, at 950 °C, degradation of τ_{eff} is observed (18 μs). This result is in correlation with the SIMS profile (Fig. 2). At this temperature stage, the dissolution of the Cr precipitates in the bulk probably takes place, leading to a high concentration of substitutional Cr atoms, acting as recombination centers.

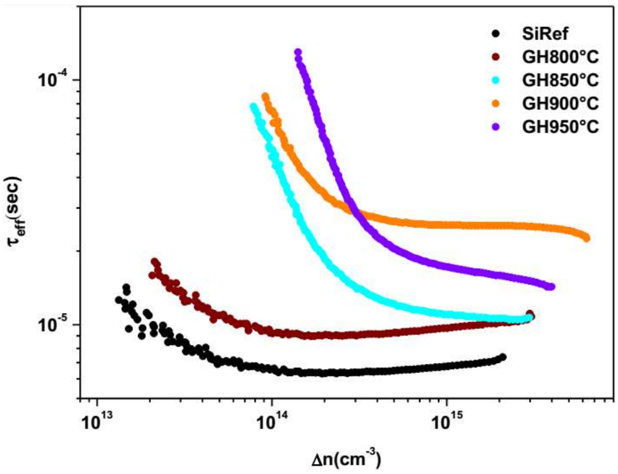

Fig. 4. Evolution of τ_{eff} in mc-Si wafers before and after phosphorous gettering process.

4. Evaluation of effective lifetime with Cr related centers

In the non gettered mc-Si wafer, the bulk lifetime $\tau_{\mathrm{non\,getter}}$ can be expressed as:

$$\frac{1}{\tau_{\text{non-gett}}} = \frac{1}{\tau_{\text{impurity}}} + \frac{1}{\tau_{\text{gett}}}, \tag{1}$$

where τ_{gett} corresponds to carrier lifetime after impurity gettering and the $\tau_{\text{non-gett}}$ represents the minority carrier lifetime before gettering (Reference Si wafer). By measuring τ_{eff} as a function of injection level by QSSPC for both, non gettered mc-Si wafers and the gettered ones we can evaluate the bulk lifetime level related to Cr impurity concentration.

$$\frac{1}{\tau_{\text{impurity}}} = \frac{1}{\tau_{\text{non-gett}}} - \frac{1}{\tau_{\text{gett}}}. \tag{2}$$

Using this model, the carrier lifetime related to the chromium impurity was determined and the results are illustrated in Fig. 5.

From the QSSPC lifetime measurements illustrated in Fig. 5, carried out on the mc-Si wafer before and after

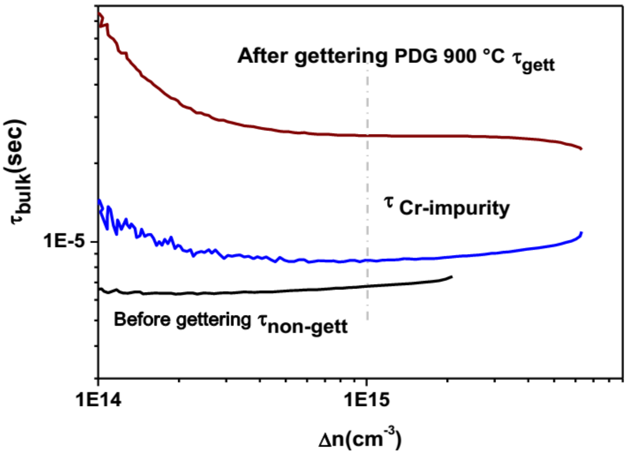

Fig. 5. QSSPC lifetime versus excess carrier density for a mc-Si wafer before and after PDG run with the lifetime related to Cr impurities.

gettering at 900 °C we can deduce that the minority carrier lifetime of the Cr impurity is lower than τ_{gett}, (26 μs). In fact, this τ_{impurity} includes gettering of other elements witch also act as recombination centers, such as Fe, Mn and Cu. Regarding the SIMS curves in Fig. 3, the extraction of a non-negligible concentration (5×10^{14} cm^{-3} to 5×10^{15} cm^{-3}) of Cr_i from the bulk to the surface of the gettering layer, dominates the τ_{gett} component. The QSSPC measured $\tau_{\text{Cr-Impurity}}$ value of about 8.5 μs is a result of interstitial Cr_i or Cr_iB_s pairs, proving their recombination activity, leading to the reduction of the carrier lifetime. Both defects are amongst the strongest known recombination centers in silicon as reported by Schmidt et al. [4].

5. Conclusions

Homogeneous phosphorus diffusion gettering (PDG) on p-type multicristalline silicon (mc-Si) was realized in the temperature range from 800 °C to 950 °C during 90 min. Phosphorous and chromium SIMS profiles suggest that a part of impurity atoms at a relatively higher temperature (950 °C) is driven from a partial dissolution of chromium precipitates in the vicinity of the crystallographic defects, grain-boundaries and from the oxygen precipitates which are generally decorated by metallic impurities. On other hand, the Cr concentration at 800 and 850 °C is lower than that measured in Si-Ref, due to low migration to the surface of the treated silicon wafers. QSSPC-measured values of τ_{eff} at excess carrier density $n = 1 \times 10^{15}$ cm^{-3} before and after PDG gettering process show an amelioration with a maximum of about 26 μs obtained in PDG run at 900 °C. In addition, we have determined τ_{gett} which corresponds to the carrier lifetime after Cr impurity gettering and we have observed that it is lower than $\tau_{\mathrm{eff}} = 26$ μs resulting from the total QSSPC lifetime. These results prove that the strongest recombination activity of chromium in the studied silicon wafers stems from interstitial chromium defects Cr_i and Cr_iB_s.

Acknowledgments

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