Utilizing Reverse Short Channel Effect for Optimal Subthreshold Circuit Design

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ABSTRACT

The impact of the Reverse Short Channel Effect (RSCE) on device current is stronger in the subthreshold region due to the reduced Drain-Induced-Barrier-Lowering (DIBL) and the exponential dependency of current on threshold voltage. This paper describes a device size optimization method for subthreshold circuits utilizing RSCE to achieve high drive current, low device capacitance, less sensitivity to random dopant fluctuations, and better subthreshold swing. Simulation results using ISCAS benchmark circuits show that the critical path delay and power consumption can be improved by up to 10.4% and 34.4%, respectively.

Categories & Subject Descriptors

B.7.1 [**Integrated Circuits**] : Types and Design Styles

General Terms

Design, Performance

Keywords

Subthreshold operation, Subthreshold Circuits, Reverse short channel effect, digital circuits, PVT variations, Optimization.

1. INTRODUCTION

Emerging ultra-low power applications such as portable devices, medical instruments, and wireless sensor networks have extremely stringent power budgets. Subthreshold circuits, which operate at supply voltages lower than the threshold voltage (V_{th}), are considered to be promising candidates for ultra low power systems. Recently, a significant amount of research has been done dealing with subthreshold circuits. Soeleman et al. analyzed various logic styles for subthreshold operation [1]. The impact of PVT variations on subthreshold circuits was investigated in [2] and [3]. Circuits such as analog voltage references, subthreshold SRAMs, tiny-XOR circuits, and adaptive filters for hearing aid applications have been demonstrated [4][5][6][7][8]. New transistor scaling trends dedicated for subthreshold circuits have been suggested in [9].

Short channel devices have been optimized for regular superthreshold circuits to meet various device objectives such as high mobility, reduced Drain-Induced-Barrier-Lowering (DIBL), low leakage current, and minimal V_{th} roll-off. However, a transistor that is optimized for superthreshold logics may not be optimal for achieving low performance and low power in the subthreshold region. Although it would be ideal to have a dedicated process technology optimized for subthreshold circuits, mainstream CMOS technology will continue to scale aiming at optimal performance in conventional superthreshold circuits. In order to design optimal subthreshold circuits using CMOS devices that are targeted for superthreshold operation, it is crucial to develop design techniques that can utilize the side effects that appear in this new regime. SCE (or V_{th} roll-off) is an undesirable phenomenon in short channel devices where V_{th} decreases as the channel length is reduced. Variation in device critical dimensions translates into a larger variation in the threshold voltage as SCE worsens with increasing DIBL [10]. Traditionally, non-uniform HALO doping was used to mitigate this problem by making the depletion widths narrow and hence reducing the DIBL effect. As a byproduct of HALO, a short channel device shows RSCE behavior where the V_{th} decreases as the channel length is increased [11][12]. In subthreshold circuits, the SCE mechanism is not as strong as in superthreshold circuits. On the other hand, RSCE is still significant enough to affect the subthreshold performance.

This paper describes a sizing method that utilizes RSCE to improve performance and power consumption in subthreshold circuits. In section II, we will illustrate general transistor sizing considerations for subthreshold circuits. Section III describes the proposed method utilizing the RSCE to improve drive current, capacitance, process variation, and subthreshold swing. Experimental results are presented in section IV. Finally, we draw conclusions in section V.

2. GATE SIZING CONSIDERATIONS FOR SUBTHRESHOLD CIRCUITS

Conventional superthreshold logics require special modifications in order to achieve optimal performance and power in subthreshold operation. For example, PMOS to NMOS width ratio (PN ratio) and stacked device sizing must be reevaluated for the subthreshold operating voltage. The optimal PN ratio changes in the subthreshold region because the weak-inversion current is also a strong function of the subthreshold slope and is affected significantly by other secondary effects such as narrow width effect, SCE, and RSCE. The significant reduction in the optimal PN ratio with a lower supply voltage can be attributed to the difference in V_{th} and subthreshold slope. Selection of the proper effective width of stacked transistors is also crucial for achieving optimal performance. The effective width of a transistor in a stack of n devices is roughly $1/n$ in the strong-inversion region. This means that in order for an n-stack to conduct the same amount of current as a single transistor, the devices in the stack must each be

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sized up by a factor of *n*. Previous sizing methods for subthreshold logics were based on the traditional assumption that the minimum channel length is optimal for speed and power. This was true in the superthreshold region, but it does not hold true in subthreshold logic because of RSCE. Therefore, a new sizing method suitable for subthreshold circuit which considers the impact of RSCE on drive current, device capacitance, and subthreshold slope is indispensable.

3. PROPOSED TRANSISTOR SIZING METHOD UTILIZING RSCE

3.1 Reverse Short Channel Effect

Fig. 1 (top) shows the threshold voltages as a function of channel length at VDD=1.2V and VDD=0.2V. In the superthreshold region (1.2V), a strong V_{th} roll-off behavior is observed at the minimum channel length due to the high DIBL effect (point A in Fig. 1). To compensate the worsening V_{th} roll-off caused by DIBL in small dimensions, non-uniform p+ doping in the source-body and drain-body boundaries are used to reduce the amount of control the drain has over the channel by making the depletion layer width narrow. These highly doped regions, called HALO implants, can also suppress the body punchthrough [13]. However, as a byproduct of using HALO implants, the threshold voltage decreases as the channel length increases. This phenomenon is known as the RSCE. Fig. 2 (top) illustrates this trend by showing the effective surface doping in the longitudinal direction. RSCE becomes more significant with process scaling due to the higher HALO doping required to negate the aggravating V_{th} roll-off as shown in Fig. 2 (bottom). RSCE is not a major concern in conventional superthreshold designs since SCE is dominant in minimum channel length devices in that region. However, in the subthreshold region, only the RSCE effect is present due to the significantly reduced DIBL. This causes the V_{th} to decrease monotonically, and operating current to increase exponentially, with longer channel length.

3.2 Optimal Channel Length for Maximum Current-Per-Width

As the V_{th} behavior changes significantly in the subthreshold region, the optimal channel length yielding maximum current-per-width changes accordingly. This is illustrated in Fig. 3, where V_{th} and current-per-width are plotted versus channel length. Maximum current-per-width is obtained at the minimum channel length (0.12µm) for VDD=1.2V because W/L is maximized. However, the optimal channel length increases to 0.55µm at VDD=0.2V since the lower V_{th} caused by RSCE provides an exponential increase in current. Current is also proportional to W/L which makes it eventually decrease at channel lengths longer than the optimal. The optimal channel length for maximum current-per-width can be derived theoretically by taking the derivative of the current equation. The RSCE-affected threshold voltage can be expressed as

$$V_{th} = V_{th0} + K_1\left(\sqrt{1+\frac{K_2}{L_{eff}}} - 1\right)\sqrt{\Phi_S} \qquad (1)$$

where V_{th0} is the zero-bias threshold voltage of a long channel device, K_1 and K_2 are technology parameters, L_{eff} is the effective channel length, and Φ_s is the surface potential. DIBL is omitted because its effect is negligible in the subthreshold region, and the body effect is ignored for simplicity. The optimal channel length obtained is

$$L_{eff} = \frac{-K_2 + \sqrt{K_2^{\,2} - 4K_3}}{2} \quad , \quad K_3 = -\frac{K_1^{\,2}\Phi_S}{m^2 V_t^{\,2}} K_2 \qquad (2)$$

The optimal channel length calculated using the analytical expression in (2) is 0.58µm which is very close to 0.55µm from simulation. We can also compare the current at the optimal channel length given by (2) with that at minimum channel length. The maximum current-per-width is 2.5X larger than that at the minimum channel length. However, using a longer channel length can have a negative impact on device capacitance which can affect the CV/I delay. In the following section, we derive the optimal channel length for maximum performance.

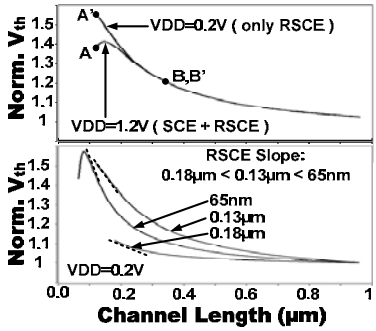

Fig. 1. Dependency of normalized V_{th} on channel length for VDD=1.2V and 0.2V

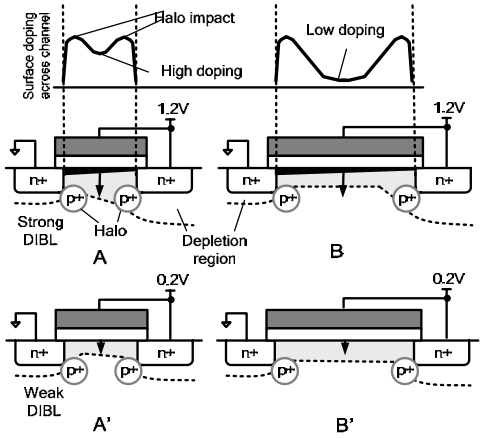

Fig. 2. Device cross sections corresponding to A, A', B, and B' in Fig. 1. Surface doping across channel is shown to illustrate the RSCE.

3.3 Optimal Channel Length for Maximum Performance

Another factor to consider when increasing the channel length for optimal subthreshold sizing is the increase in device capacitance. Delay and power consumption increases linearly with capacitance. Fig. 4 shows the different components of device capacitance in the subthreshold region. C_{DEP} is the depletion width, $C_{GS,GD}$ is the overlap capacitance per width, C_{OX} is the oxide capacitance, and C_J is the junction capacitance per width.

To show the effectiveness of increasing the channel length, the capacitances of a transistor having a constant current is plotted versus channel length in Fig. 5. Note that the device width can be reduced as the channel length is increased since RSCE lowers the V_{th} and exponentially increases the device current. This was not the case for superthreshold circuits where the decrease in W/L had a larger impact on current than the reduction in V_{th} due to RSCE. Increasing the channel length alone has no effect on junction capacitance (C_J). However, since the device width is reduced simultaneously for constant current, the junction capacitance also goes down with a longer channel length as shown in Fig. 5. The increase in gate capacitance (C_G) is moderate between channel lengths of 0.12µm and 0.36µm for two reasons. First, the reduction in width makes the increase in gate area smaller. Second, the RSCE associated with longer channel length makes the depletion capacitance (C_{DEP}) smaller since the depletion layer width increases as shown in Fig. 2. At channel lengths longer than 0.36µm however, C_G increases rapidly since the RSCE is significantly weaker, and gate area must be increased to drive the same current. As a result, there exists a minimum point in total capacitance for iso-current at a channel length of 0.36µm. By using this optimal channel length, we can reduce delay and power consumption in subthreshold circuits.

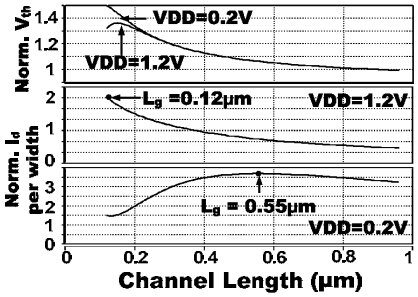

Fig. 3. Dependency of normalized V_{th} and current-per-width on channel length

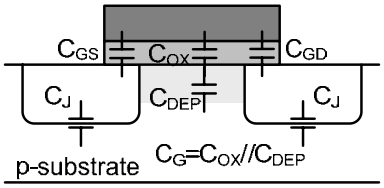

Fig. 4. Capacitance in subthreshold MOS device

3.4 Impact of Process Variation

Random Dopant Fluctuation (RDF) causes random parameter mismatches even between devices with identical layout in close proximity. The standard deviation (σ) of the threshold voltage distribution caused by RDF is proportional to $(WL)^{-1/2}$. Using the proposed sizing method, the gate area for optimal performance increases from 0.24µm^2 (=2µm×0.12µm) to 0.35µm^2 (=0.98µm×0.36µm) as shown in Fig. 5. This interesting characteristic leads to less threshold voltage variations for the proposed sizing scheme. Fig. 6 and Fig. 7 show the Monte Carlo simulation results of the delay and power distribution using a static inverter designed by the proposed and conventional scheme. σ/µ of the delay and power distribution is reduced by 37.5% and 70%, respectively, resulting in a squeezed distribution for the proposed sizing scheme. Simulation results show a 13% improvement in average delay while simultaneously achieving a 31% reduction in average power dissipation.

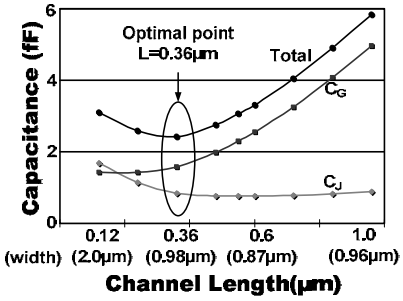

Fig. 5. Capacitance vs. channel length for constant current

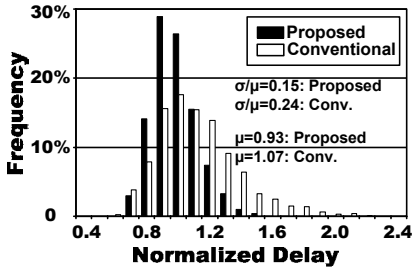

Fig. 6. Delay distribution comparison for a static inverter.

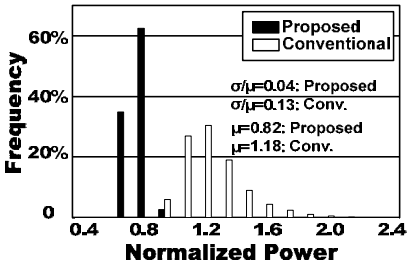

Fig. 7. Power distribution comparison for a static inverter.

3.5 Subthreshold Swing and Ion-to-Ioff Ratio

Subthreshold swing *(S)* is a critical parameter that determines the relationship between subthreshold current and the gate voltage. It is defined as the amount of V_{GS} required to change the subthreshold current by an order of magnitude. *S* has generally been considered a process-dependent parameter. A small *S* is preferred for higher on-current for a given off-current value. Our proposed sizing scheme utilizes a longer channel length which reduces *S* and improves the Ion-to-Ioff ratio. The subthreshold swing can be represented as

$$S = m\frac{kT}{q}\ln 10 \quad (mV/dec) \tag{11}$$

where $$m = 1 + \frac{C_{DEP}}{C_{OX}}, \quad C_{OX} = \frac{\varepsilon_{ox}}{t_{ox}}, \quad C_{DEP} = \frac{\varepsilon_{si}}{W_{DEP}} \tag{12}$$

and kT/q is the thermal voltage.

As explained in section III-C, RSCE increases the depletion width underneath the channel and lowers the depletion capacitance, C_{DEP}. This alters the value of *m* in (12) and reduces *S*.

In this specific process technology, the subthreshold slope of the proposed method is 71mV/dec which is 16mV lower than that of the conventional minimum channel device. The improved subthreshold slope reduces the off-current by 30% for the same on-current and increases the Ion-to-Ioff by a 2.5X, from 190 to 483 at 0.2V.

4. EXPERIMENTAL RESULTS

A delay chain composed of inverters, 2-input NANDs and 2-input NORs was used for the experiments to verify the effectiveness of the proposed sizing scheme. Layout of the sample delay chain is shown in Fig. 8. The conventionally sized gates have a taller layout than the gates sized using the proposed scheme. This is due to the fat devices in the proposed scheme having longer channel lengths and narrower widths. Minimum channel length is used for the PMOS devices since the RSCE was significantly weaker for PMOS transistors in this particular technology. In future technology nodes where RSCE is severe in both PMOS and NMOS devices, our proposed sizing scheme can be applied in general. The layout area of the proposed scheme is 18% smaller compared to that using conventional sizing. The delay variation of the proposed scheme is 38.7% smaller than that of the conventional method for each process corner. The power savings range from 10% to 39%, mainly depending on the current of the conventional scheme which is sensitive to process variations. We tested our sizing method in more general logic paths by synthesizing a number of ISCAS benchmark circuits, as well as different component circuits used in that suite. Two cell libraries were created, each containing inverters, two-input NANDs, and two-input NORs. Critical path delays and power consumption are compared in Table 1. Improvements in delay range from 7.8% to 10.4% depending on the type of logics used in the critical path. In addition, a simultaneous power reduction of 8.4% to 34.4% is achieved with the proposed scheme.

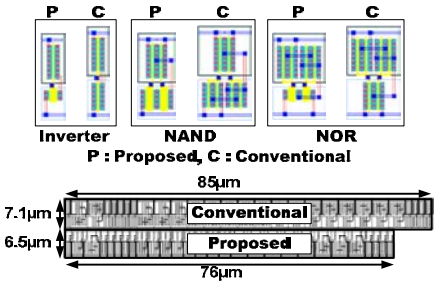

Fig. 8. Layout comparison for basic logic gates and sample delay chain.

5. CONCLUSIONS

RSCE was not a major concern in superthreshold designs. Rather, DIBL and V_{th} roll-off were the main considerations. However, in the subthreshold region, RSCE must be considered for optimal device sizing. We proposed a novel device size optimization scheme which can achieve high drive current, low device capacitance, and high Ion-to-Ioff ratio by utilizing the RSCE. Circuits using the proposed sizing scheme are more robust against RDF because of the increased gate area at the optimal performance point. The average delay was improved by 13% while average power dissipation was reduced by 31%. The proposed scheme also offers a tighter delay and power distribution by improving the σ/μ by 37.5% and 70%, respectively.

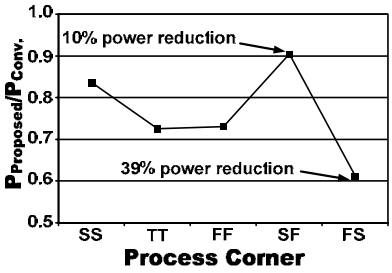

Fig. 9. Comparison of average power for corner parameters.

Table 1. Delay and power comparison for ISCAS.

Circuit	0.2V, Temp=27° (Delay / Power)		
	Conv. (ns)	Proposed (ns)	Improvement
C6288	119 / 2.24	107 / 1.50	10.1 / 33.0 %
C1355	443 / 0.64	397 / 0.42	10.4 / 34.4 %
74283	231 / 1.60	207 / 0.14	10.4 / 13.8 %
74L85	121 / 0.38	110 / 0.26	9.1 / 31.6 %
74182	103 / 0.40	95 / 0.38	7.8 / 8.4 %

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