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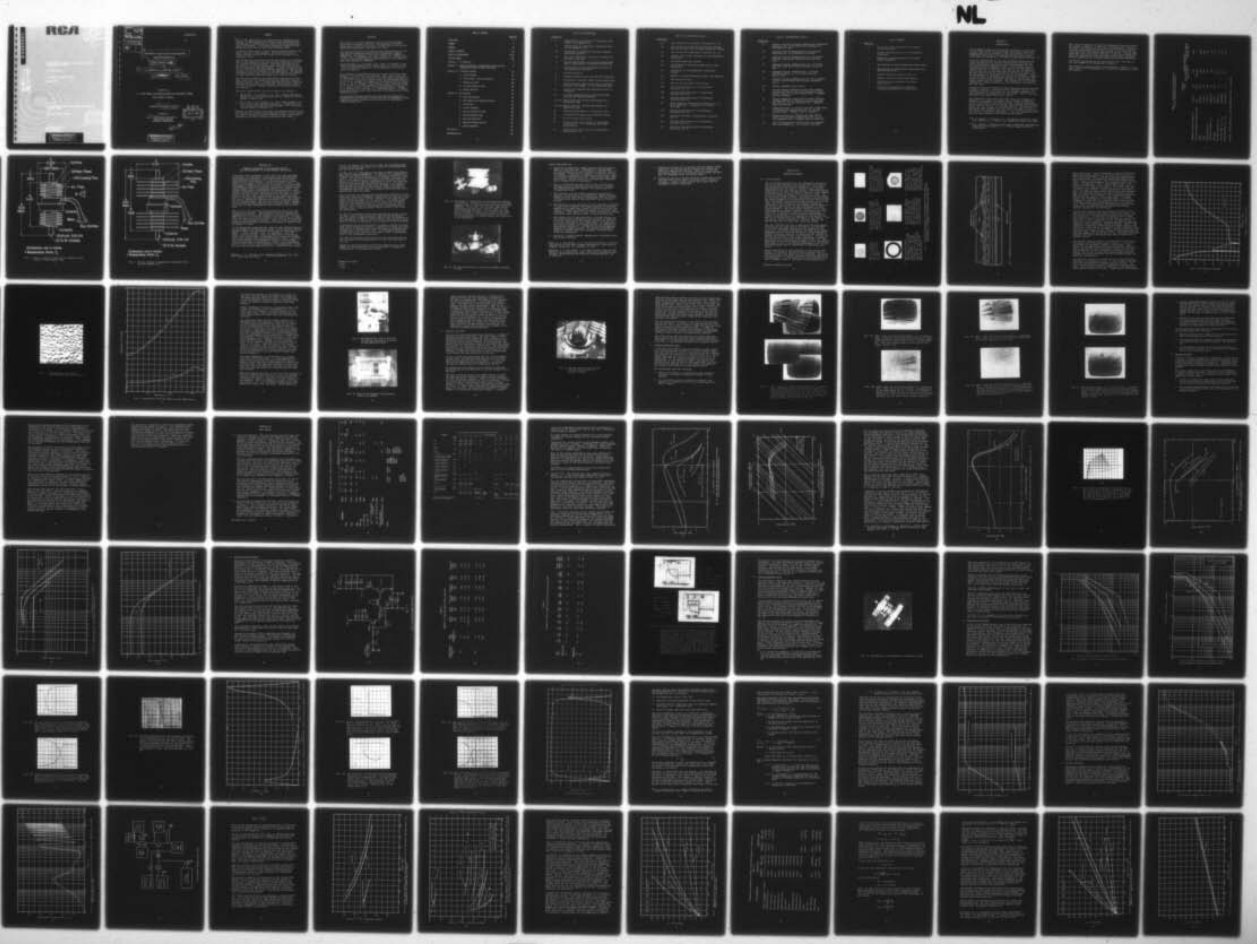

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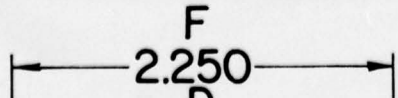

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DEVELOPMENT OF A HIGH VOLTAGE AND HIGH CURRENT TRANSCALENT TRANSISTOR

FINAL TECHNICAL REPORT

BY

S. W. KESSLER, R. E. REED, D. R. TROUT

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Prepared for

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FORT, BELVOIR, VIRGINIA

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Prepared by:
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SUMMARY

All of the objectives of the contract were obtained or exceeded. An NPN Transcalent transistor was developed which was capable of blocking 800 to 1000 volts and of switching up to 150 amperes. A 500 watts dissipation capability was demonstrated as well as very fast switching times.

To achieve these goals, a novel emitter ballast resistor was made a portion of the assembly. This ballast resistor forces current sharing to all areas of the emitter on the transistor chip.

The Transcalent transistor uses two heat-pipes as an integral part of the package to cool the silicon transistor chip and its integral ballast resistor. With heat-pipe cooling of the device, it has been demonstrated that 523 watts of heat can be dissipated from the package. A thermal resistance as low as 0.20°C/watt has been observed between the junction and the base of the fins attached to the heat-pipes. The thermal resistance between the junction and 25°C ambient air flowing at 1650 feet per minute was found to be only 0.35°C/watt.

The switching speeds of the Transcalent transistor are very fast, less than 1.0 microsecond turn-on time and 2.0 microseconds turn-off time. A large area Safe Operating Curve was determined from the second breakdown, current gain, saturation and sustaining voltage characteristics measured during the contract.

Two patent applications were filed during the contract:

1. RCA 69,470 - S. W. Kessler, Jr. etal, "Reinforced Transcalent Device" which was issued as U.S. Patent #3,978,518 issued 31 August 1976.

2. RCA 71,321 - S. W. Kessler, Jr, etal, "Semiconductor Device with Ballast Resistor Adapted for a Transcalent Device" Serial #833,056 Filed 14 September 1977, Confirming License issued 2 November 1977.

Besides the exceptional electrical and thermal characteristics, the Transcalent transistor provides reductions in size, weight and ease of installation when compared to other large power transistors and their externally attached heat sinks.

FOREWORD

This report, the Final Technical Report on the Transcalent transistor development contract, was prepared by the RCA Corporation, Solid State Division, Electro Optics and Devices Power Tube Operations, Lancaster, PA 17604.

The work performed on this contract was authorized by the U.S. Army Mobility Equipment Research and Development Command (MERADCOM), Fort Belvoir, VA, under Contract No. DAAK02-72-C-0642. Mr. R. McKechnie and, more recently, Dr. Russel Eaton, III, the Contracting Officer's Representatives, have administered the program for MERADCOM.

Acknowledgement is also made to Mr. Joseph D. Segrest of the Naval Air Development Center, Warminister, PA, for his financial and technical support to the development of the Transcalent transistor.

The information presented herein covers work authorized under Phases I, II and III of the contract. There were a total of 14 modifications to the contract, the most recent completed on 30 June 1977. The work on the contract was performed primarily by Mr. S. W. Kessler, Sr. Member of the Technical Staff and by Mr. D. R. Trout, Member of the Technical Staff under the supervision of Mr. R. E. Reed, Leader of the Technical Staff and Mr. W. S. Lynch, Manager of Power Products Engineering. Messrs. W. T. Burkins, R. F. Keller, A. J. Witkowski and C. V. Reddig, Engineering Technicians, also assisted in performing the actual program of work.

The specified program of work was successfully completed as evidenced by two new power transistors, RCA developmental types J15490 and J15492, which are now available in experimental sampling quantities.

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Section I

INTRODUCTION

The 60 amperes, 800 volts Transcalent transistor is the third silicon power device to be developed using heat-pipes as an integral part of the package to cool the silicon. The first Transcalent Device was a 250 amperes average current rectifier[1] and the second was a 400 amperes Transcalent Thyristor.[2]

A major accomplishment of the work performed during this contract was defining the need and developing a technique for evenly distributing the emitter current throughout the area of a large silicon transistor wafer. The solution to this problem required a redesign of the ends of the heat-pipes in contact with the silicon from that used for earlier devices, the introduction of a ballast resistor between the end of the emitter heat-pipe and the emitters in the silicon wafer, and the development of techniques for making the assembly. Changes in the closure of the heat-pipes allowed the use of high temperature brazes which eliminated the need to electroplate the copper powder wick with solder. The elimination of the solder improved the thermal conductivity and strength of the wick in the heat-pipe.

Sixteen Transcalent transistors were fabricated and tested using a ballast resistor in series with the transistor wafer. Data characterizing both the electrical and thermal properties of the transistors are summarized in this report. All of the characteristics exceeded the contract goals.

The Transcalent transistors were made using two different fin diameters, two inches in diameter and 4¼ inches in diameter. The two inch diameter fins were the same integral fins as employed in the earlier device designs that required high velocity air at 4000 ft. per min. to cool the devices. The 4¼ inch diameter fins were joined to the heat-pipes with epoxy and had sufficient heat transfer area that an air velocity of only 1650 ft. per min. cooled the transistor. A two inch diameter pin fin was also epoxy bonded to the heat-pipe and tested.

(1) S. W. Kessler, Development of a 250 Ampere Transcalent Rectifier, Report No. 2, Contract No. DAAK02-69-C-0609, June 1970.

(2) S. W. Kessler, 400 Ampere High Power Transcalent Semiconductor Thyristor Device Report No. 5, Contract DAAK02-69-C-0609 Final Report.

The contract objectives along with a summary of the test results are listed in Tables 1, 2 and 3 for the Transcalent transistor. In Table 1 are listed the electrical characteristics. Transistors were fabricated from silicon crystal of two different resistivities, 30 to 40 ohm-cm and 60 to 80 ohm-cm. Devices made using the lower resistivity exhibited a high current capability while the transistors using the higher resistivity sacrificed current capability for a greater sustaining voltage capability.

The thermal characteristic of devices with the 2 inch and 4¼ inch fin diameters are summarized in Table 2.

The mechanical characteristics are summarized in Table 3. Figures 1 and 2 are illustrations of the outline dimensions of each size device.

Table 1 Electrical Characteristics
of the Transcalent Transistor

		Contract Goal	Results Obtained	
			30 to 40 ohm-cm Resistivity	60 to 80 ohm-cm Resistivity
Maximum Voltage Capability	(volts)	750	990	1000
Cut-off Frequency greater than	(Hz)	4000	230,000	--
V_{CBO}	(volts)	750	990	1000
V_{CEV}	(volts)	750	990	1000
*$V_{CE(Sustaining)}$	(volts)	400	510	710
Collector Current, I_c	(amperes)	60	86	43
$V_{CE(SAT)}$	(volts)	1.25	0.6	0.6
*DC Base Current, I_B	(amperes)	10	13.7	10
Turn-On Time ($t_d + t_r$)	(microsec)	5	0.7	0.7
Turn-Off Time ($t_s + t_f$)	(microsec)	10	2.1	2.3

*Pulsed: Pulse duration $\leq$300 microseconds, duty $\leq$2 percent

Table 2 Thermal Characteristics of the Transcalent Transistor

Parameter	Contract Goal	Results Obtained: 2 inch dia. fins	Results Obtained: 4¼ inch dia. fins
Dissipation (watts	500	453 at air velocity of 4000/5000 ft./min. and an average heat-pipe temperature 105.5°C	523 at air velocity of 1550 ft./min. and average heat-pipe temperature of 78°C or 150 CFM
Thermal Impedance (°C/W)	Not spec.		0.13 collector heat-pipe 0.23 emitter heat-pipe
Storage Temperature (°C)	-65 to 200		Room temp. to 135°C
Operating Temperature, T_J (°C)	-65 to 200		Room temp. to 195
Ambient Operating Temp, T_A (°C)	-55 to 125		Room temp. to 125

Table 3 Mechanical Characteristics of the Transcalent Transistor

	Contract Goal	Results Obtained	
		2 inch dia. fins	4¼ inch dia. fins
Weight (oz.)	10	10	30
Volume (in^3)	14	10.8 between studs 11.0 with studs	48.9 49.1
Length including studs (in.)	5	5	5
Length minus studs (in.)		$3.450^{+.025}$	$3.450^{+.025}$
Diameter (in.)		1.938 max.	4.25 ±.05
Heat Sink		None required	None required

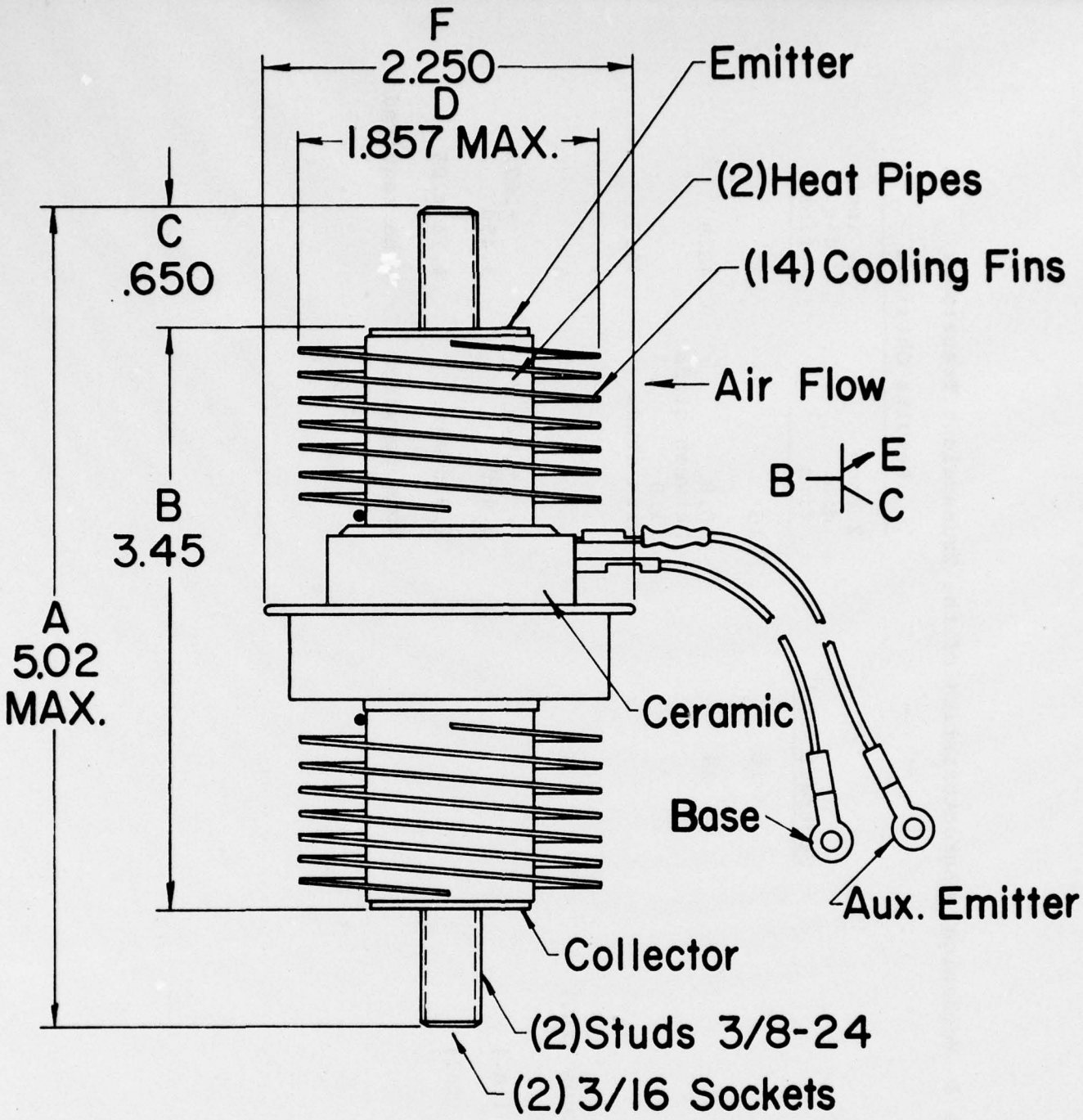


Fig. 1 Outline drawing of Transcalent Transistor with nominal 2 inch diameter fins

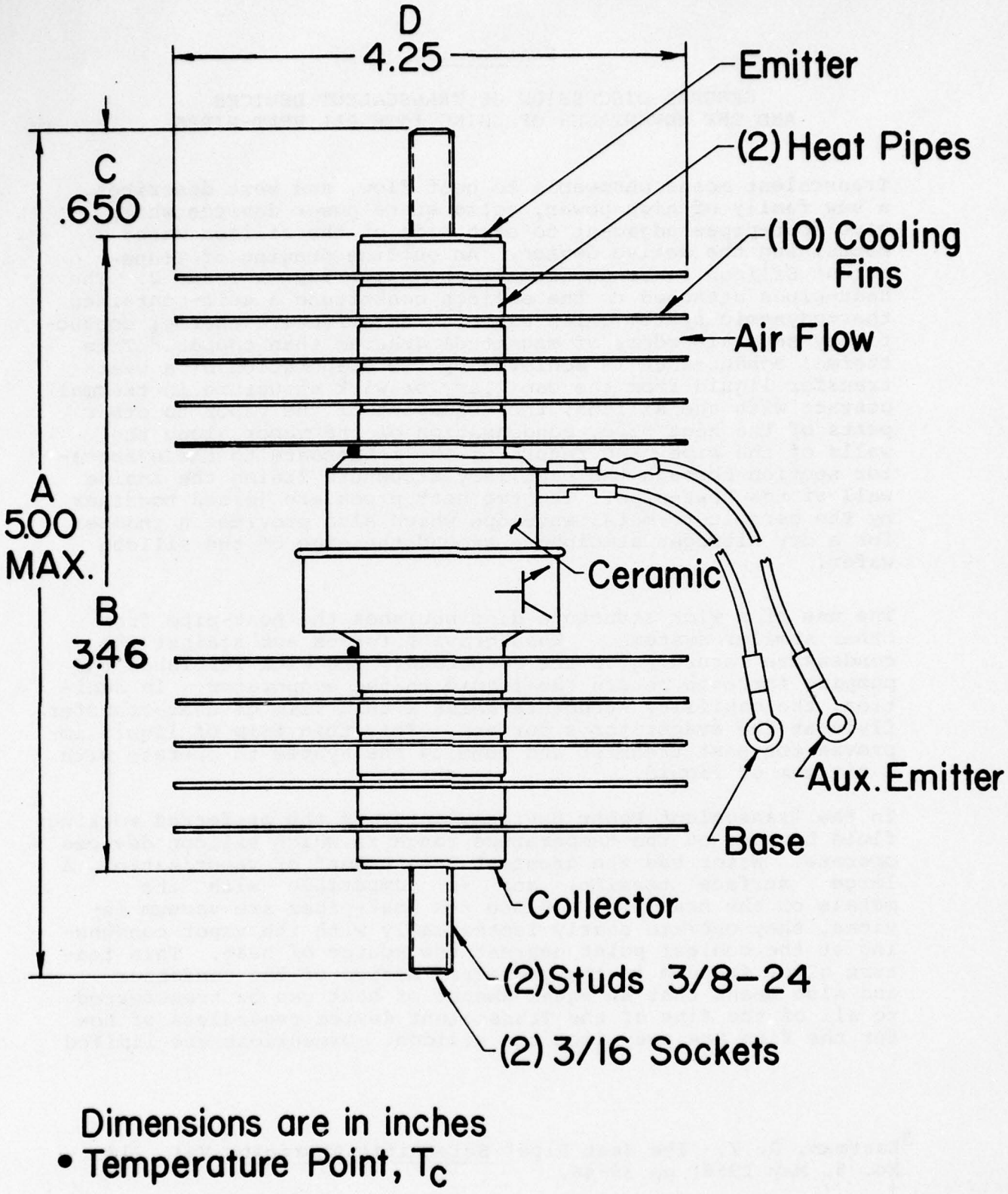


Fig. 2 Outline drawing of Transcalent Transistor with 4½ inch diameter fins

Section II

GENERAL DISCUSSION OF TRANSCALENT DEVICES AND THE ADVANTAGES OF USING INTEGRAL HEAT-PIPES

Transcalent means permeable to heat flow, and best describes a new family of high power, solid state power devices which have heat-pipes adjacent to each side of the silicon wafer containing the active device. An outline drawing of Transcalent Silicon Power Devices is shown in Figures 1 and 2. The heat-pipes attached to the silicon constitute a self-contained thermodynamic system which exhibits an effective thermal conductivity several orders of magnitude greater than copper.[3] This thermal conductance is achieved by the evaporation of a heat-transfer liquid from the capillary or wick structure in thermal contact with the silicon, the transport of the vapor to other parts of the heat pipe, condensation of the vapor along the walls of the pipe, and return of the condensate to the evaporator section through the capillary structure lining the inside wall of the heat-pipe. The two heat pipes are joined together by the ceramic-to-metal envelope which also provides a chamber for a dry nitrogen atmosphere around the edge of the silicon wafer.

The use of a wick structure distinguishes the heat-pipe from other similar systems. When gravity forces act against the condensate returning to the evaporator, the wick furnishes the pumping force to return the liquid to the evaporator. In addition, the capillary structure holds a thin film of heat-transfer fluid at the evaporator's surface. This thin film of liquid improves the heat transfer and permits the system to operate with a minimum of liquid.

In the Transcalent Power Devices, water is the preferred working fluid because of the temperature range in which silicon devices operate. Water has the greatest latent heat of vaporization, a large surface tension, and is compatible with the metals of the heat-pipe. Since the heat-pipes are vacuum devices, they operate nearly isothermally with the vapor condensing at the coolest point nearest the source of heat. This feature gives freedom in the geometric design of the condenser and also means that an equal amount of heat can be transferred to all of the fins of the Transcalent device regardless of how far the fins are away from the silicon. Dimensions are limited

[3]Eastman, G. Y. "The Heat Pipe" Scientific American, Vol. 218, No. 5, May 1968, pp 38-46.

only by the ability of the wick to "pump" the condensate back to the hot surface area where the liquid can be re-evaporated and the cycle repeated.

In 1969, the U.S. Army Mobility Equipment Research and Development Center Command (MERADCOM), Ft. Belvoir, VA, awarded RCA a contract* for the development of a Transcalent Rectifier[1], Type J15401. The rectifier was designed to conduct an average current of 250 amperes and to be cooled with 150 cubic feet per minute of air at an ambient temperature of 70°C. The rectifier with its heat-pipes and cooling fins was only 1-7/8 inches in diameter and five inches long, which included 1.55 inches of stud lengths for fastening high current leads to the device. The complete rectifier, with its integral heat-pipe heat sinks, weighed less than ten ounces.

After achieving the improved heat dissipation capability of the Transcalent Rectifier, MERADCOM requested RCA to develop a Transcalent thyristor[2] (Type J15371), cooled with the same heat-pipe design as was developed for the rectifier. The design objectives for the thyristor were a current rating of 400 amperes (RMS with 180° conduction angle), a critical rate of rise of current (di/dt) rating of 800 amperes per microsecond and a critical rate of rise of voltage (dv/dt) rating of 200 volts per microsecond.

To take full advantage of the heat-pipe cooling of the silicon, the wafer used in the Transcalent thyristor was designed to have the emitter diameter slightly smaller than the diameter of the heat-pipes, so that all of the area of the silicon in which most of the heat is generated is in contact with the heat-pipes.

A photograph of two of the devices is shown in Figure 3a along with larger competitive devices. Competitive devices are often referred to as "hockey-pucks" and are cooled by clamping them between large aluminum heat sinks. The Transcalent packages illustrated in the figure are the same as used in the development of the Transcalent transistor.

The three Transcalent transistors which were developed during this contract and mentioned earlier in this text are shown in Fig. 3b.

Experience with Transcalent devices has demonstrated a large number of advantages when their configuration is compared to "hockey-puck" or stud-mounted devices.

*DAAK02-69-C-0609

[1] ibid

[2] ibid

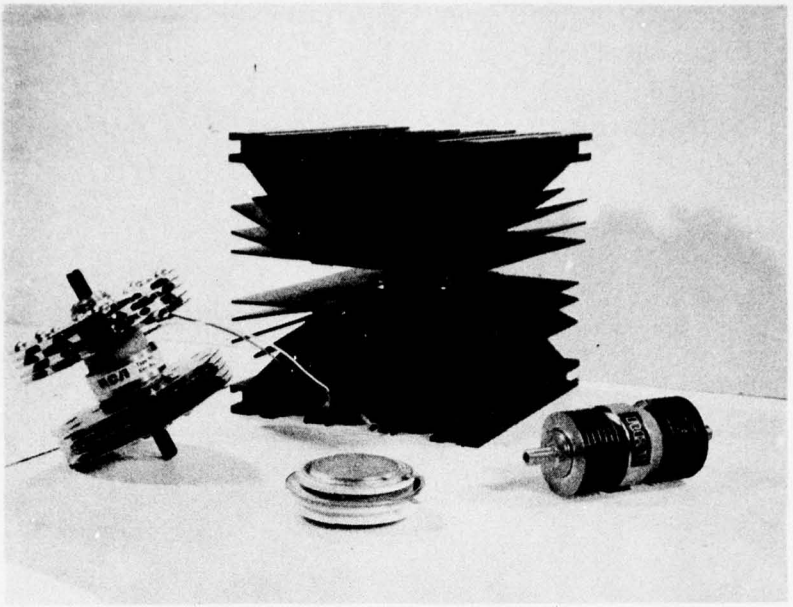


Fig. 3a Photograph of Transcalent devices alongside competitive devices. The device on the right is a 250 amps. (Average Current) Transcalent rectifier developed for MERADCOM. On the left is a 400 amp. (RMS current) Transcalent thyristor with fins 4¼ inches in diameter developed for NADC. In the center is a competitive method of cooling high current solid state devices in which a disc-shaped device (as the one in the foreground) is clamped between the large fins in the background.

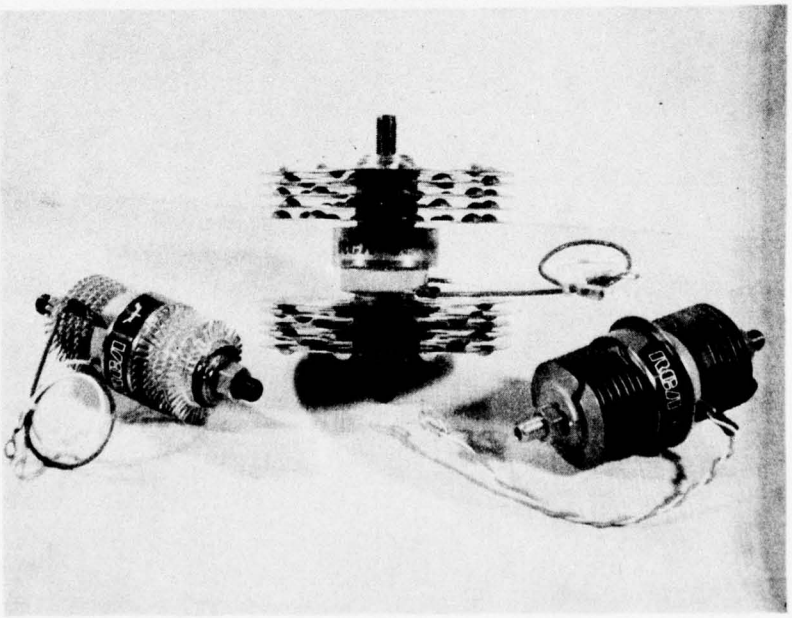


Fig. 3b The three Transcalent Transistor packages described in text.

These advantages are:

1. There are no mechanical clamps fastening the Transcalent device to the heat sink. Clamping of a "hockey-puck" must be uniform or the heat transfer to the heat sink will be impeded. "Hockey-puck" supplier's literature is full of cautions in mounting and torquing the bolts when clamping a device between heat sinks. Over-torquing may crack the silicon. The heat sinks of a Transcalent transistor are an integral part of the device.

2. Heat is extracted from both sides of the silicon with a minimum of material adjacent to the silicon to minimize the temperature gradient between the junction and the ultimate heat sink.

3. The thickness and the thermal properties of materials adjacent to the silicon are optimized to absorb transient surges of power which must be dissipated from the silicon if blocking and control characteristics are to be maintained.

4. The operation of the heat-pipes is very tolerant to changes in power levels because they respond quickly to surges by evaporating an additional amount of working fluid and thus exhibit a decreasing thermal resistance as the power level increases. Thus, there is only a small increase in junction temperature when operating under an overload condition.

5. The assembly has a high resistance to fatigue failure because the materials adjacent to the silicon and bonded to it either nearly match the thermal expansion of the silicon or are designed to yield elastically. By comparison, the rubbing surfaces of a clamped device are subjected to fretting and scoring.[4,5] As fretting debris accumulates between the clamped surfaces, the contact resistance between the adjacent materials increases, altering their electrical impedances.

6. Operation at higher ambient temperatures is possible without current derating.

[4]Comyn, R. H. and Furlani, C. W. "Fretting Corrosion", A Literature Survey TR-1169 Harry Diamond Laboratories, Army Material Command, Washington, DC, December 30, 1963.

[5]Comstock, W. R. and Locher, R. E. "High Current Diode and SCR Reliability Considerations" Power Electronics Specialists Conference, IEEE Aerospace and Electronic Systems Society 1975 p. 224-233.

7. Transcalent Devices are of smaller size and lighter weight because of the greatly reduced temperature gradient between the junction and the fins. Also, all of the fins are equally effective in dissipating heat because the heat-pipe is isothermal along its entire length.

8. Transcalent devices conserve materials because much of the internal space of the device is hollow with a vacuum environment. Lighter weight results and a high ratio of strength-to-weight is achieved.

Section III

TRANSISTOR DESIGN

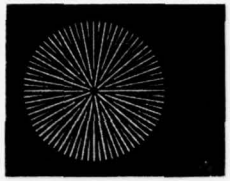
A. Initial Design

The first design objective of the Transcalent transistor was to use the same heat-pipe designs which were used on the Transcalent thyristor and rectifier*. It had been demonstrated that 500 watts of thermal energy could be dissipated using this heat-pipe design. The second design objective was to limit the emitter diameter to the diameter of the heat-pipe in contact with the silicon wafer. By limiting the emitter diameter, the majority of heat losses in the silicon would be within the bounds of the heat-pipe. The inside diameter of the heat-pipe is 0.875 inch and the limiting diameter of the emitters was selected to be 0.820 inch. The 0.055 difference in diameters allowed for spreading of the current and heat through the thickness of the silicon wafer and for slight misalignment of parts during assembly. The third design objective was to have approximately one square centimeter of emitter area with nearly 100 centimeters of emitter-to-base periphery. A high ratio of emitter-to-base periphery reduces emitter current crowding which is a tendency for the emitter current to be concentrated near the edges of the emitter. If the emitter width is less than 0.010 inch, most of the emitter area will be useful for injecting current.

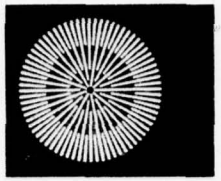
The last restraint was that a simplified heat-pipe design required that the base contact be made at the periphery of the wafer extending from around the diameter of the heat-pipe. With these constraints, the most useful design considered was one in which the emitter fingers extended radially from the center of the wafer with the regions in between the emitters being at base potential. To have sufficient emitter area (1.064 square centimeters) a design was chosen with 72 emitters as is shown in Fig. 4a. This design has an emitter-to-base periphery of 89.4 centimeters. Also shown in Fig. 4 are contact photographs of all of the photolithography used in fabricating a Transcalent transistor.

Before describing the other features of the emitter base design, the design of the metallizing structure used in fabricating the first wafers will be discussed. The metallizing structure is closely related to the construction of the heat-pipes. A cross-section of the metallizing structure is shown in Fig. 5. The base of the transistor is

*Contract DAAK02-69-C-0609



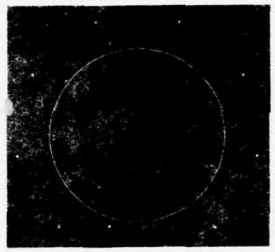
a. Emitter Diffusion Mask: Phosphorus is diffused into the white region to form the 72 N+ emitters



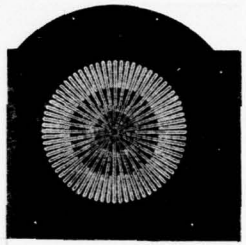
b. P+ Diffusion Mask and Base Metallization Mask: Boron is diffused into the black regions of the mask. The same mask is used to outline the Base Metallization on top of the P+ regions.

c. Trigger or Ballast Etch Mask: This mask is used to etch a moat (white area) in between the emitters and the base to mechanically force base currents beneath the emitters.

d. Emitter Window Mask: This mask is used to etch open windows in the oxide layer covering the base metallization. Contact is made to the emitters in the openings. Contact is made to the base metallization in the area of the broad white circle.



e. Isolation Mask: Emitter and base metallizations are isolated from each other by removing the metal in the white band. The ring is positioned in the black region between the contacts to the emitters and the base in Fig.



f. Emitter-Base Metallization Mask: This mask is a composite of masks b & d. This mask is used to separate emitter and base metallization when a single layer of metal is used to make contact to the two regions.

Fig. 4 Contact photographs of photolithography masks used in fabricating a Transcalent Transistor. All of the masks were drawn by a computer-controlled Gerber machine.

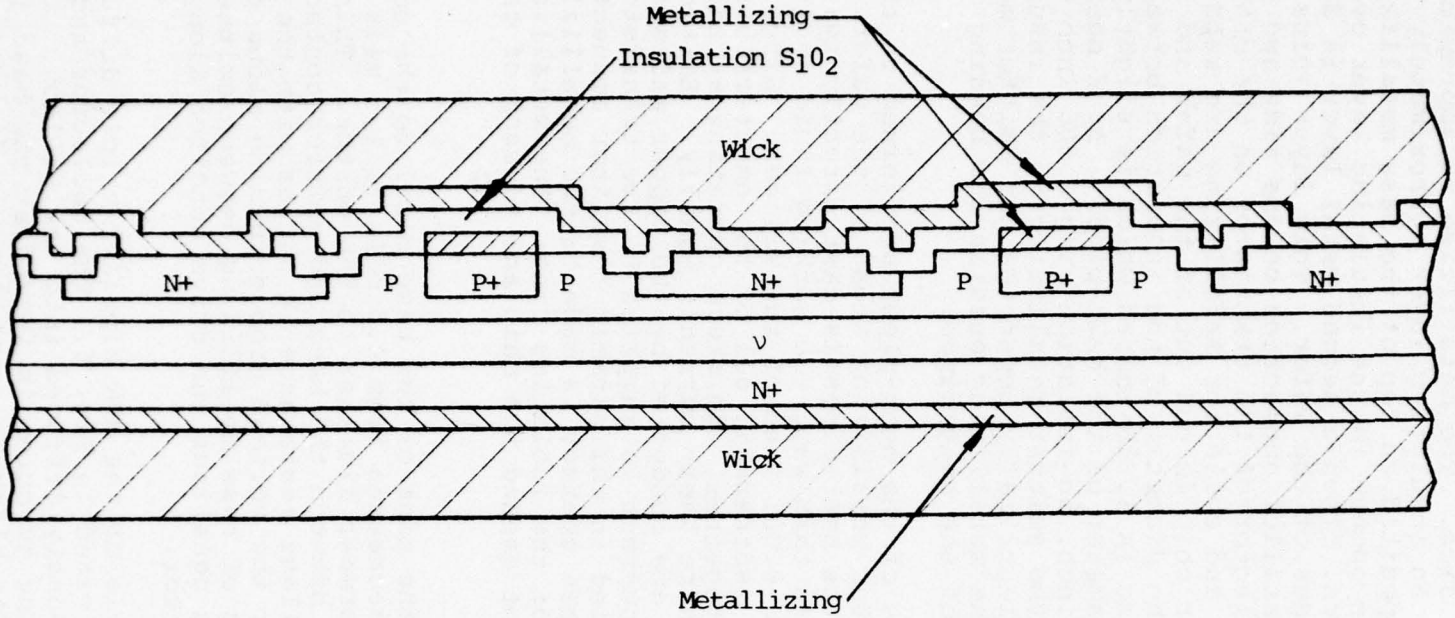


Fig. 5 Cross-section of the metallizing structure of the Transcalent Transistor

metallized first. Photo lithography is used to define the base metallization pattern to the same outline as the P+ ohmic contact diffusion. The metallizing is approximately one micron thick. An insulating layer approximately one micron thick is deposited on top of the base metallization layer. Windows are opened in the insulating layer over the tops of the emitters. Then a second metal layer is deposited on both sides of the wafer. This layer joins the 72 emitters in a parallel connection on one side and makes contact to the collector of the transistor on the other side. The emitter and collector metallizing are separated when the transistor chip is cut out of the wafer and its edge contoured. The diameter of the insulation between the emitter and the base is 1.010 inches which is slightly larger than the diameter of the heat-pipes. At a mean diameter of 0.989 inch, an isolation ring 0.005 inch wide is etched through the emitter metallizing to the insulation. This ring electrically separates the emitter metallizing from the base metallizing outside the bonding (faying) diameter of the heat-pipes.

The feathered walls of the heat-pipes are joined to the emitter and collector metallizing areas of the wafer. The wick structure of the heat-pipes is cast directly against the metallizing. In this way, the working fluid in the heat-pipe is within 0.001 inch of the silicon. Since heat-pipes strive to be isothermal, all of the emitters are thermally coupled together. Emitters operating at the same temperature will share their currents equally. Emitter and collector currents are conducted by the copper walls of the heat-pipes. Base current is supplied to the transistor chip through a lead sealed in the ceramic insulator connecting the two heat-pipes. Base contact is made to the metallizing outside the diameter of the isolation ring. The metallizing distributes the current around the chip and to each of the 72 emitter fingers.

The distance from the edge of the base metal to the edge of the emitter metal decreases from 4.5 mils to 1.5 mils in going from the outermost diameter to the center. This variation in width between the base and emitter contacts adds a variable ballast resistance in series with the base and compensates for the voltage drop occurring along the narrow, thin strips of base metallizing between emitters. The base ballasting equalizes the drive conditon along the length of each emitter.

The diffusion profile of the NPN bipolar, triple diffused structure is illustrated in Fig. 6. The collector and base are first simultaneously diffused into the silicon. The high voltage blocking junction is formed at the base junction. The junction's blocking capability is determined by the starting resistivity of the ν layer and its thicknesses.

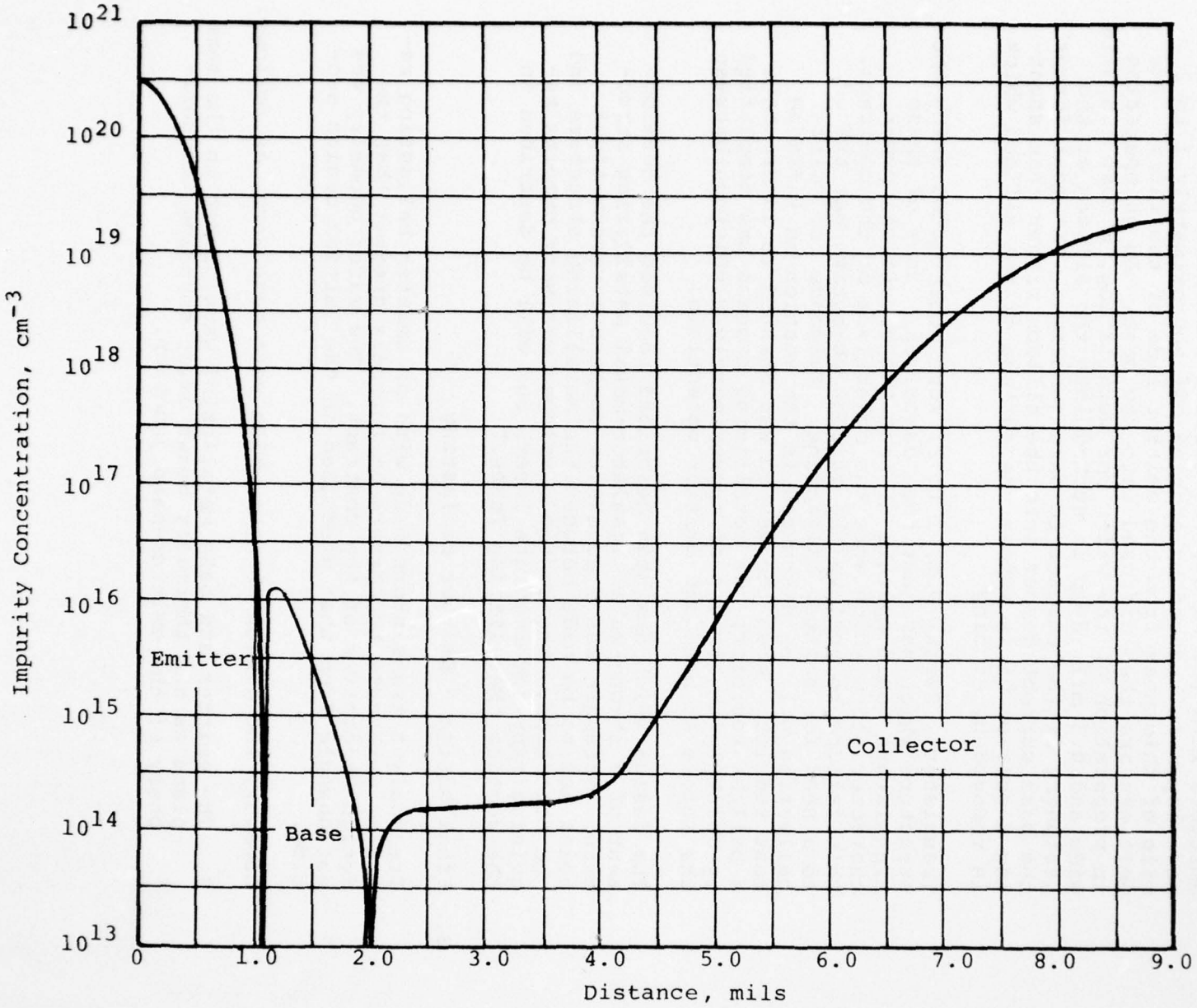


Figure 6 Diffusion Profile

A small additional blocking capability is gained as the depletion layer extends a short distance into the base and into the diffused collector regions. Before diffusing the emitters into the wafer, the surface concentration of the base layer is reduced by etching off approximately 1 to 2 mils of thickness from the emitter side of the wafer. The emitters are then diffused into the base. As an operation in preparation of the wafer for metallizing, a moat 1.5 mils wide and 0.5 mil. deep is etched into the silicon at the periphery of the emitter-to-base junction. The moat forces the base current deeper into the silicon rather than shunting a portion of it across the surface of the silicon which is removed by etching.

Transistors, Serial Nos. 1 to 27 were constructed using the structure which has just been described. None of these transistors would operate at near the electrical power characteristics which were the objectives of the contract. This failure to achieve the current objective was traced to a need for emitter ballasting. Evidence for emitter ballasting will be discussed in the section on infrared test results. When the design was changed to incorporate a ballast resistor, the metallizing process was simplified by creating an air gap of approximately 0.001 inch between the metals at base and emitter potentials.

The design which has been described required the development of a strong-metal insulator-metal metallizing structure. Strength was a necessity because a vacuum-tight joint had to be made between the metallizing structure and the heat-pipe. The system developed was very complex requiring many intermediate layers and will be described in the section "Metallizing Tests."

B. Final Design - Emitter Ballasting

Transcalent transistors made with an emitter ballasting resistor were able to operate at currents greater than the design objectives of the contract. The wafer geometry was not changed from that described in the initial design section.

However, the design changes which were made were, as follows:

1. The emitter and base metallizing were placed on the same plane as the thermally grown oxide covering the periphery of the emitter-base junction.

2. The ends of the heat-pipes adjacent to the silicon were closed with a molybdenum disc. The molybdenum discs were brazed into the heat-pipes at 1020°C so that the copper wick could be sintered at nearly as high a temperature. The high temperature sintering of the wick increased its strength and the thermal conductivity of the wick. There are presently no alloying elements (in the wick) which may degrade the thermal conductivity of the copper. A photograph of the sintered wick is shown in Fig. 7.

   Closing the end of the heat-pipe at this stage of assembly eliminates the need to make a vacuum-tight joint of the heat-pipe to the silicon wafer.

3. A ballast resistor was added to the assembly between the 72 paralleled emitters on the wafer and the molybdenum disc closing the end of heat-pipe. The ballast resistor was made from a silicon wafer of 1 ohm-cm resistivity, 0.006 inch thick. Phosphorus was diffused into both sides of the ballast wafer for making ohmic contact to the silicon. The resistance of the ballast is controlled by the depth of the diffusion of these contacts.

   On the transistor side of the wafer, mesas 1.5 mil. high are formed by etching. The top area of the mesas is the same as the metallizing on the emitters of the transistor wafer. The ballasts are metallized on both sides, using the same tungsten metallizing employed on the transistor wafers. On the mesa side of the resistor, the metal is removed from the area between the mesas.

   Approximately 1/2 mil. of gold plating is deposited on top of each mesa by pulse plating. The gold is added to make a soft contact to the transistor wafer. The ballast resistor was cut from wafer at an angle and at a diameter equal to the contact pattern so that the ends of the contacts could be seen from the opposite side of the wafer.

   The electrical resistance of two ballast resistors versus temperature are illustrated in Fig. 8. The resistors have a positive coefficient of resistance up to 310°C. If one emitter tries to conduct more current than the other emitter fingers, it and the region of the ballast resistor in contact with it will become hotter because of resistive heating.

Fig. 7: Photograph of the sintered wick structure 100 magnification

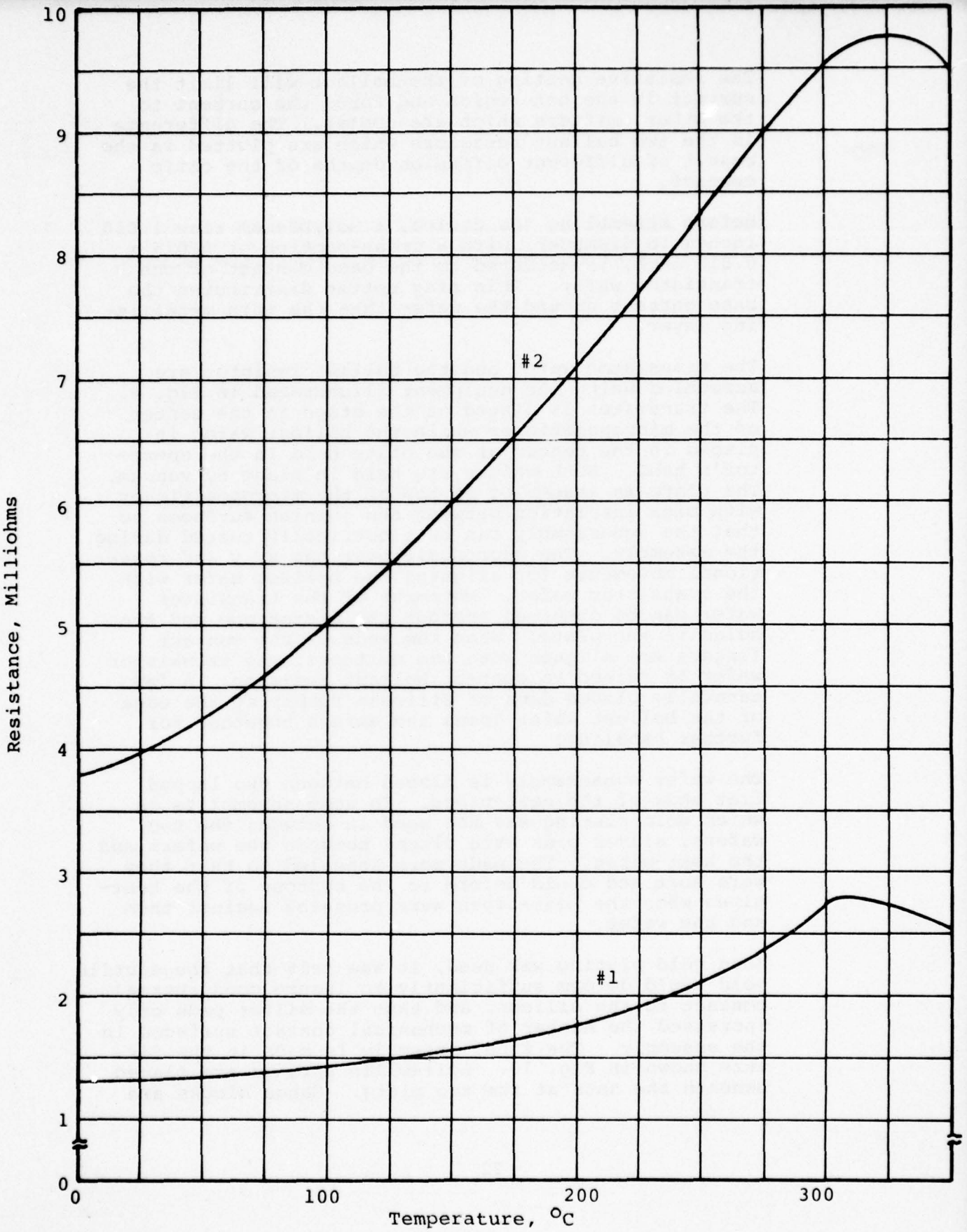


Fig. 8 Resistance of Ballast Wafers versus Temperature

The resistive heating of the ballast will limit the current in the hot region and force the current to the other emitters which are cooler. The difference in the two ballast resistors which are plotted is the result of different diffusion depths of the ohmic contact.

Before assembling the device, a molybdenum ring 1.050 inches in diameter, with a cross-section of 0.075 x 0.015 inch, is soldered to the base contact of the transistor wafer. This ring better distributes the base current around the wafer than the thin metallizing layer.

The transistor wafer and the ballast resistor are assembled using the equipment illustrated in Fig. 9. The transistor is placed on the stage in the center of the micropositioner while the ballast wafer is placed in the center of the plate held in the operator's hand. Both wafers are held in place by vacuum. The plate is assembled on top of the micropositioner with mica insulation between the joining surfaces so that the subassembly can be electrically tested during the assembly. The micropositioner has x, y and rotational movements for aligning the ballast wafer with the transistor wafer. Movement of the transistor wafer can be observed through the microscope and the holes in the plate. When the ends of the contact fingers are aligned with the emitters, the transistor wafer is raised to contact ballast resistor. ·A few carefully placed dabs of silicone rubber at the edge of the ballast wafer joins the wafers together for further handling.

The wafer subassembly is placed between the lapped flat ends of the heat-pipes. In some assemblies in which gold plating was not used in between the two wafers, silver pads were placed between the wafers and the heat-pipes. The pads were annealed so that they were soft and could deform to the contour of the heat-pipes when the heat-pipes were pressing against them and the wafer.

When gold plating was used, it was felt that the ductile gold would deform sufficiently to insure good thermal contact to the silicon, and that the silver pads only increased the number of mechanical contact surfaces in the assembly. The final assembly is made in the fixture shown in Fig. 10. Belleville springs are placed beneath the nuts at the top plate. Gauge blocks are

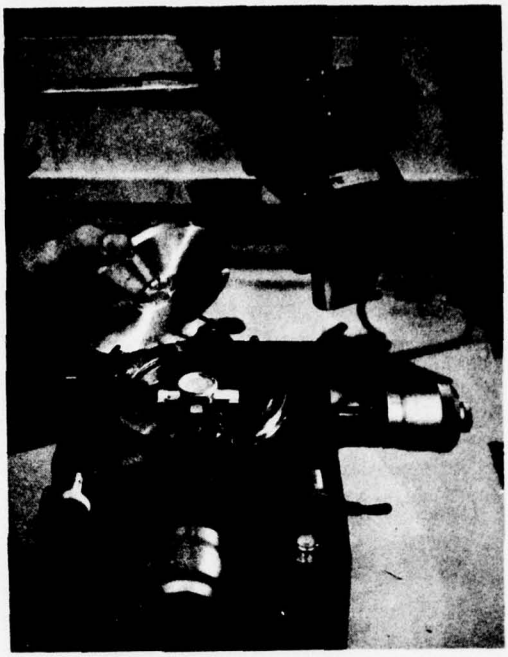


Fig. 9 Micropositioner used to position the ballast resistor with respect to the transistor wafer.

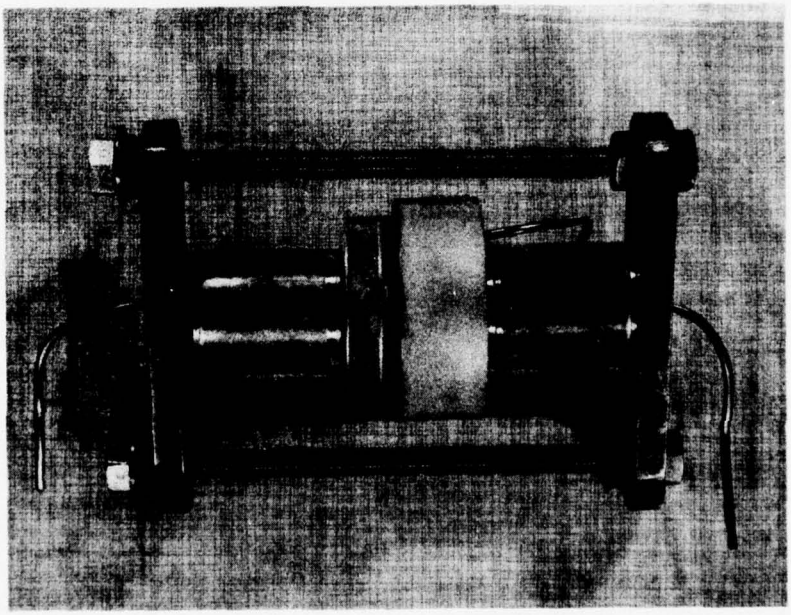


Fig. 10 Fixture for Clamping the Transistor while it is Welded

used to observe the deflection of the Belleville springs as the nuts are tightened. Tightening of the nuts is stopped when the loading on the emitters of the transistor wafer is 1000 pounds per square inch. The weld ring is then slipped into position between the heat-pipes and welded to each of the flanges attached to the heat-pipes. When the fixture is removed, the tensile forces in the threaded rods clamping the wafers are transferred to the weld ring. A photograph with cutaway cross-section of the emitter heat-pipe and the ballast wafer is shown in Fig. 11. Shown in the photograph are 18 emitters not covered by the ballast resistor; the ring for spreading the base current around the wafer, the base lead wire; the molybdenum disc at the end of the emitter heat-pipe; the wick and webs feeding the center of the evaporator; the ceramic-to-metal seal assembly, and the fins attached to the heat-pipe.

C. Metallizing Tests

To build the metal-insulator-metal structure, a number of metallizing tests were tried. The first group of tests employed chemical vapor deposited (CVD) tungsten on an evaporated layer of palladium for base metallizing; both sputtered and CVD silicon dioxide as the insulator; CVD polysilicon and evaporated layers of palladium and finally CVD tungsten for the emitter metallizing. The resistance between the two conductive layers was greater than 40,000 ohms but neither the perfection of the surfaces nor the strength of bonds was sufficient to make a vacuum-tight joint between the heat-pipes and the silicon.

Silicon nitride was substituted for the silicon dioxide in one series of tests but edge definition of the base metallization was too poor to be useful. In this test, the lack of adherence of CVD tungsten to the silicon nitride was used to define the base metal pattern.

An attempt was also made to use silicides for the base metallization but the adherence of the CVD tungsten to it was poor.

The most successful metallizing scheme was one in which the sequence of the layers was always silicon dioxide, silicon, palladium, tungsten, nickel in either a forward or reverse sequence through the list of materials. To use this principle in fabricating a wafer first involved growing a thermal silicon oxide and depositing polysilicon on top of it. Base contact was made by evaporating palladium, CVD tungsten, and evaporating palladium in windows etched in the oxide and polysilicon layers. A reverse

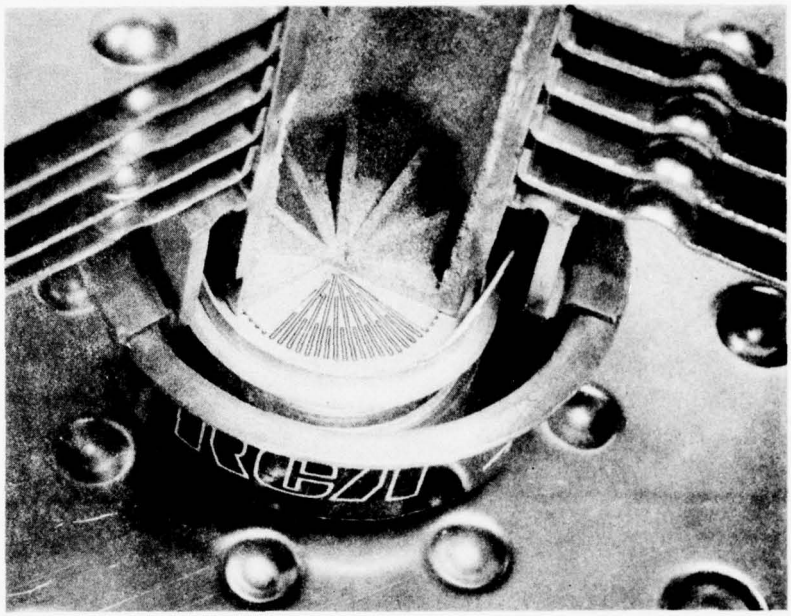


Fig. 11 Cut-away cross-section of the emitter heat-pipe and the ballast resistor.

mask was then used to remove the metals and the ploysilicon from all of the areas but the base contact area. After this etch, silicon dioxide covered the emitters, the lightly p-doped neighboring areas and the three metal layers over the base contact area. Next, polysilicon, silicon dioxide, and polysilicon were vapor deposited on the wafer. The first layer of polysilicon to be deposited is a common neighbor to both the silicon dioxide and palladium in the list of materials. To make contacts to the emitters, windows are etched open through the alternating layers of polysilicon and oxide and then palladium, tungsten and nickel are deposited on the wafer.

The last deposition sequence is also done on the collector side of the wafer. To separate the base metallizing from the emitter, an isolation ring is etched thru the last three layers of metals to the insulating layer. A number of wafers were processed through this sequence of operations successfully but this metallization process was abandoned because it did not seem to be economically feasible.

One device which used this metallizing system developed a short between emitter and base after the heat-pipes were processed. It is believed that water from the wick entered a pin hole in the metallizing which is in contact with it.

D. Infrared Radiation Test

A few transistor wafers were probe tested and their operation observed through the use of a silicon vidicon camera that was sensitive in the near infrared end of the spectrum. The radiation was observed on a television monitor. Photographs depicting the results are shown in Fig. 12 to 14. Contact was made to a multiple number of emitters by two techniques: 1. By pressing a copper ring against the emitters which were raised slightly higher than the plane of the base by plating, and 2. By making wire bonds to the emitters and bridging the base metallization.

The photographs show the following:

1. Most of the current is injected into the transistor structure at points of mechanical contact to the emitter.

2. If a low ohmic contact is made to an emitter, the emitter is injecting current into the base along its entire length.

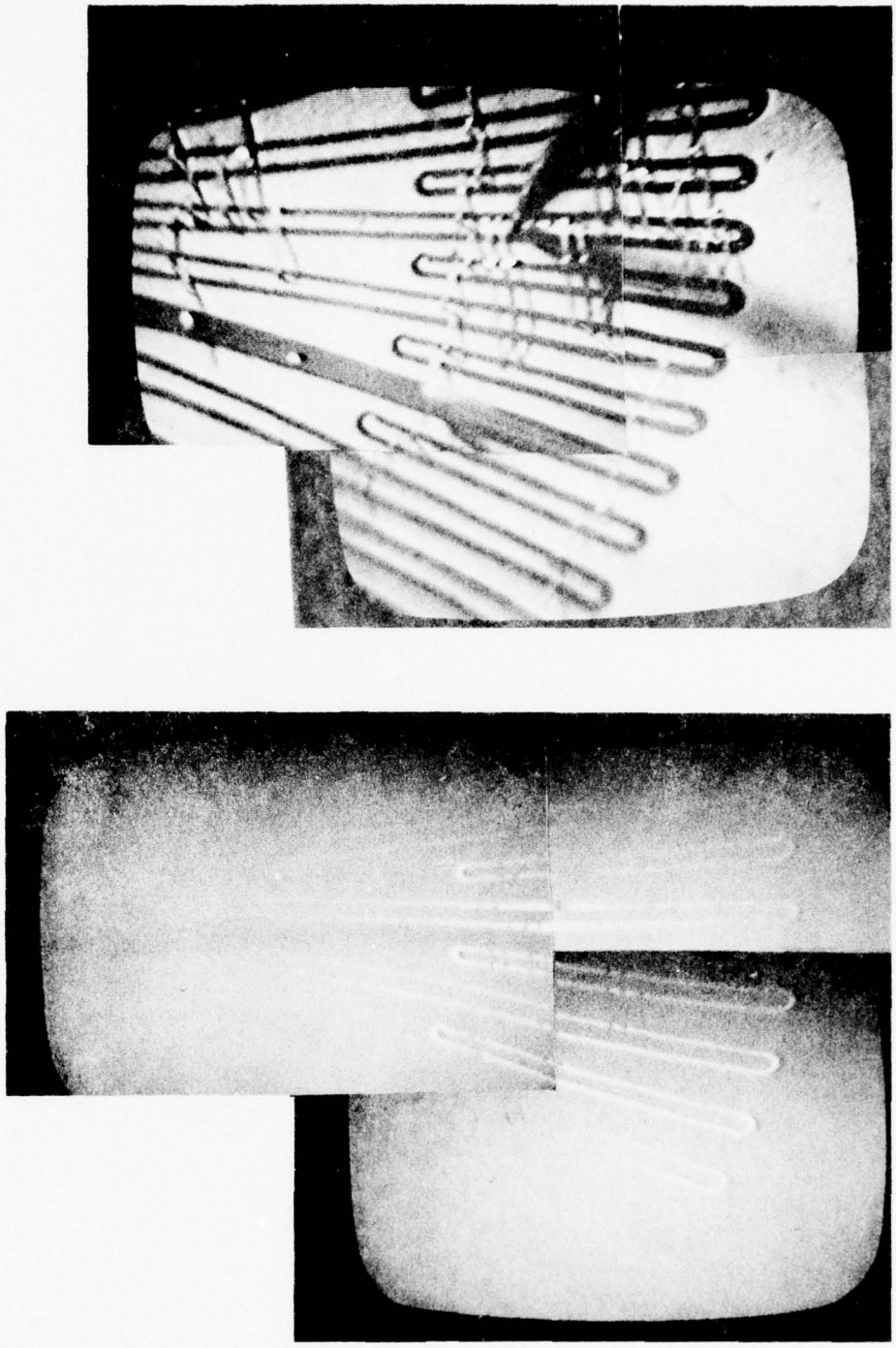


Fig. 12 White light and infrared photographs of a transistor chip. Emitters joined together by wire bonding. The upper photograph is an area of the wafer as observed with white light and the lower photograph is infrared radiation observed from the same area. Note that the most intense radiation is near where the probe is making contact to one emitter.

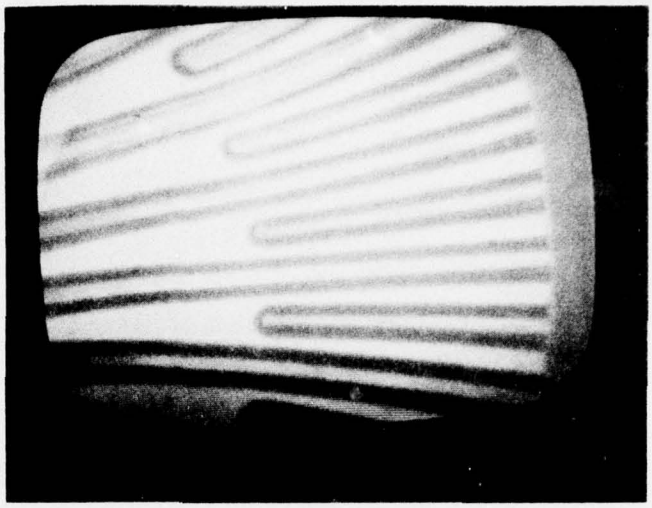


Fig. 13a White light and infrared photograph of a transistor chip. A part of the emitter base structure of Transcalent Transistor chip viewed with an infrared camera with white light and without collector current flowing. The gray crescent shape at the right is the copper contact ring.

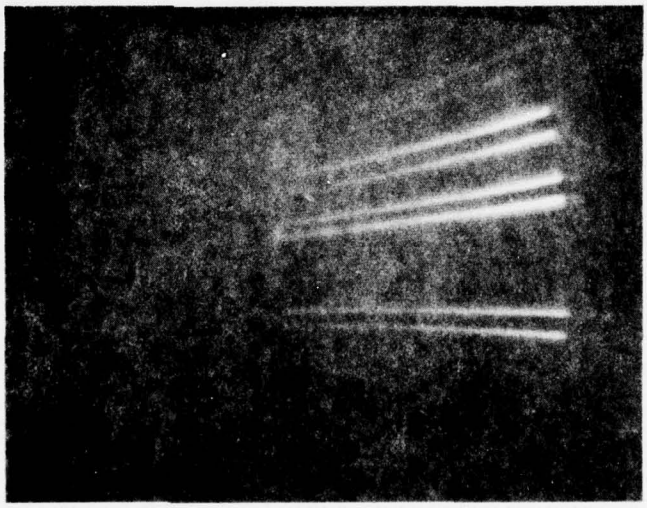


Fig. 13b White light and infrared photograph of a transistor chip. Same region as above viewed in darkness with an infrared camera and I_C = 12 amp. The brightest region is the area of greatest current injection into the emitter. Note that all of the emitters are not operative nor are their entire lengths operative.

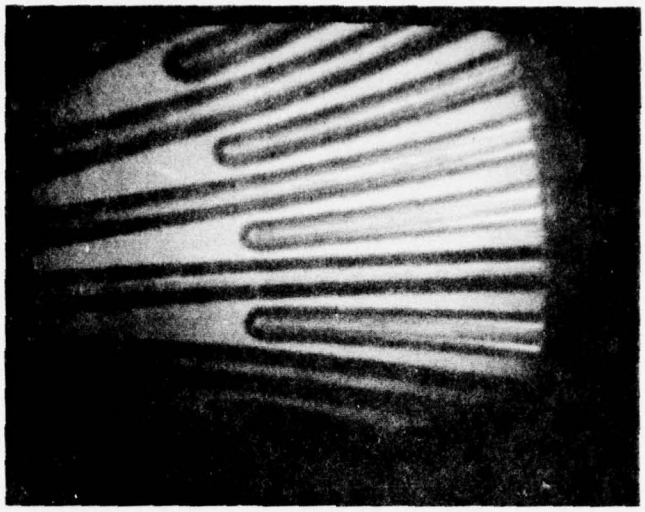


Fig. 13c White light and infrared photograph of a transistor chip. Same region as a viewed in white light with an infrared camera and I_C = 12 amp.

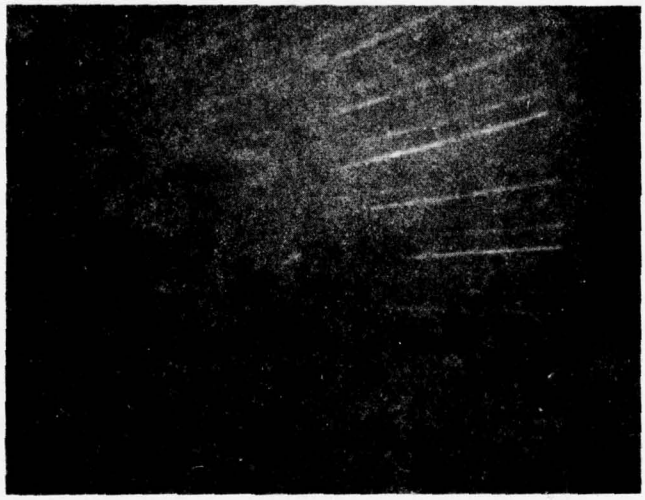


Fig. 13d White light and infrared photograph of a transistor chip. Same region as a viewed in darkness with an infrared camera with emitter base reverse bias showing that electrical contact was being made to the one emitter which was not injecting current when the junction was forward biased.

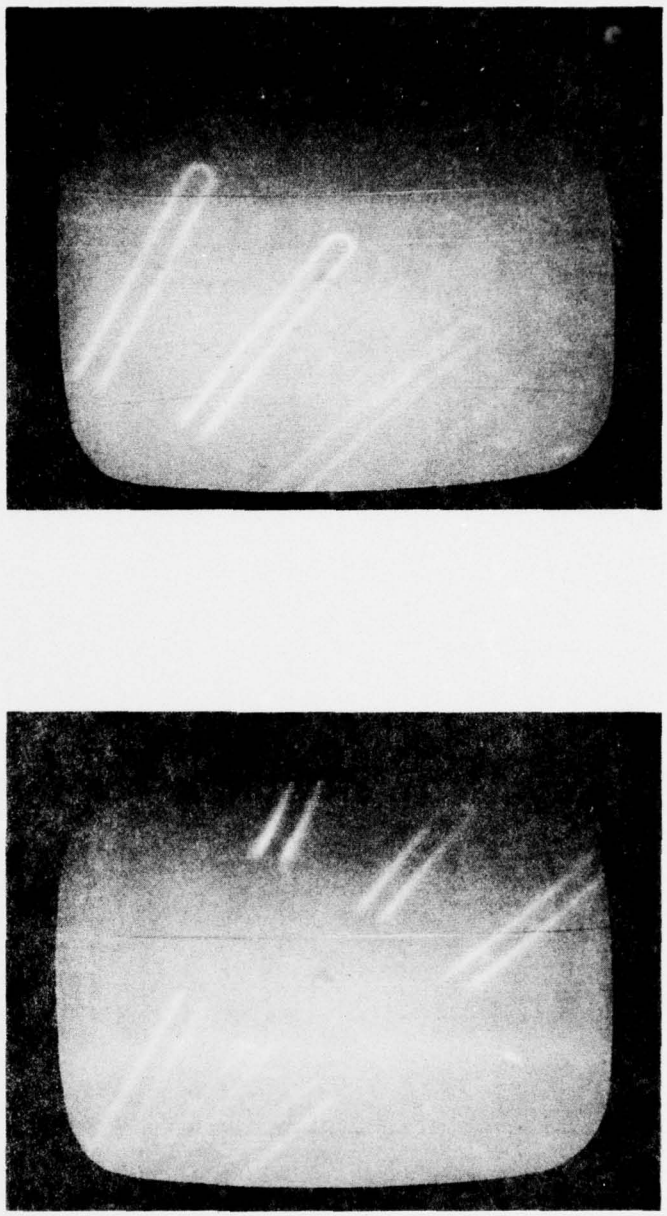


Fig. 14 Infrared photographs of a transistor chip. A portion of the emitter base structure of a Transcalent Transistor chip viewed with an infrared camera in darkness with I_C = 12 amp. The dark band is the shadow of the copper contact ring. Not all of the emitters are injecting current.

3. Contact resistance between emitters varies and those emitters having the lowest contact resistance inject most of the current into the base when the emitter-to-base junction is biased in the forward direction. During the test, most of the current was being conducted through five to seven of the 72 emitters even though the ring was in contact with all of the emitters.

4. Contact to the non-injecting emitters was confirmed by reverse biasing the emitter-to-base junction. The questionable emitter-to-base junction would avalanche at 20 volts and emit infrared light along the periphery of most emitter-to-base junctions.

It was from these tests that the importance of the following configurations were realized:

1. Emitter ballasting was needed to force the emitter current to be shared by all of the emitters,

2. Base metallization was needed to enable the current to be injected along the entire lengths of the emitters, and

3. It was important to make a low resistance contact to each emitter to utilize all of the emitters in parallel or all of the silicon's area.

E. Ballast Resistor

Two emitter ballast designs were considered, one was using a lateral resistor of doped poly crystalline silicon as an intervening layer between oxide layers. A schematic sketch of this structure is shown in Figure 15a. The doped poly crystalline silicon is used to make ohmic contact to the N+ emitter.

The second system to be considered and the one adopted is a vertical ballast resistor. A sketch of this structure is shown in Figure 15b. The vertical ballast resistor was chosen for several reasons.

1. It was not necessary to add value to the transistor wafer which would be an additional loss when factored by the yield of processing the ballast resistor.

2. The possible imperfections in the surface of a multiple layer structure would alter the local resistance of the ballast resistor.

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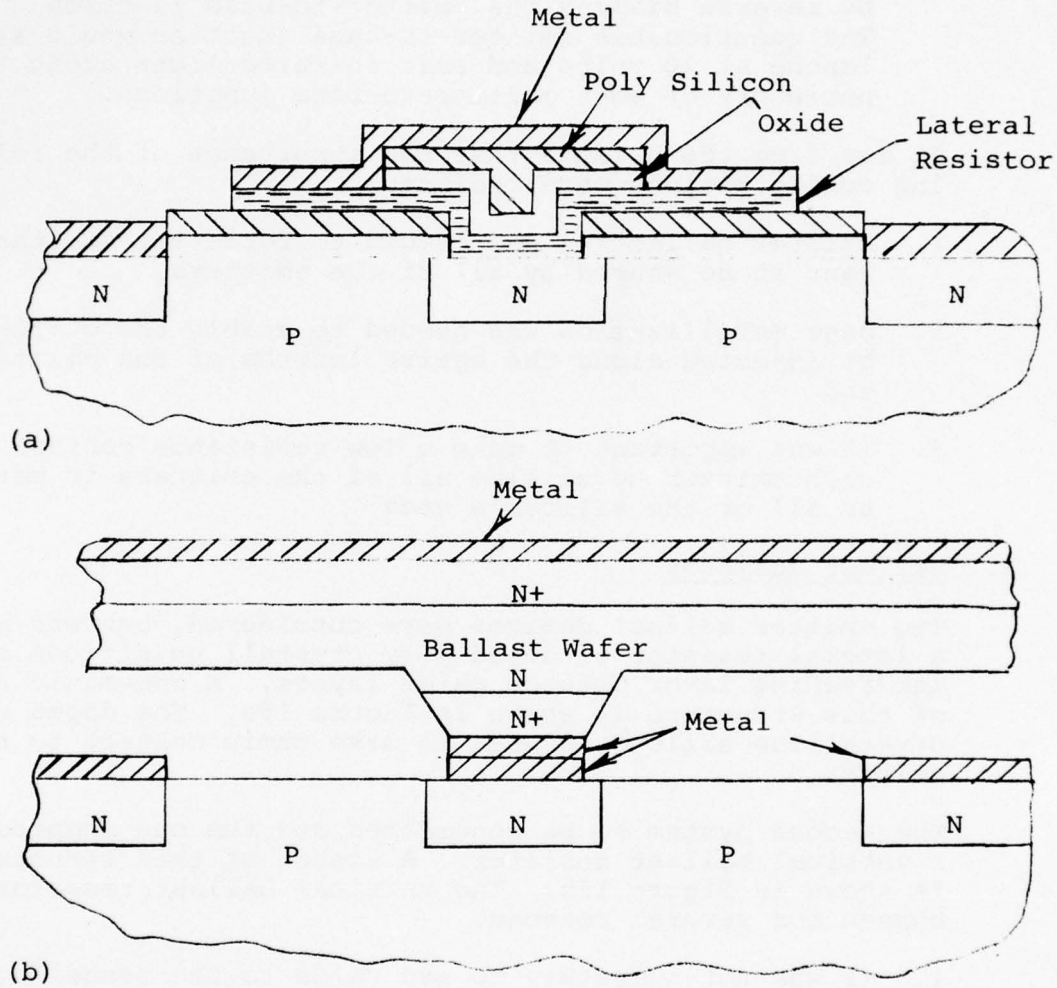


Figure 15 Two Methods of Supplying an Emmitter Ballast

CAUTION: Use only the lubricants specified in E.S. 33-33-805.

BASIC DIMENSIONS	2 PLACE DEC.	3 PLACE DEC.
up to 6"	±.02	±.005
Above 6" to 24"	±.03	±.010
Above 24"	±.06	±.015
Angular Dimensions	± 1/2°	

DESIGN BY	MODEL NO.
DRAWN BY	A SIZE / DWG. NO.

* CHANGE
** ADDITION
*** DELETION

3. The resistance of polycrystalline silicon is dependent upon doping and heat treatment. Since the wafer would be subjected to a multiple number of heat treatments in processing, it was felt that it may be difficult to control the resistance of the ballast resistor.

4. An additional photo resist mask would have to be designed and processed for fabricating the lateral ballast resistor. The lateral ballast had one major advantage which was being sacrificed by this decision and that was, it offered a lower thermal impedance to the emitter heat-pipe.

   Since the ballast resistor was to compensate for non-uniform temperature distributions, it was reasoned that the voltage drop across the resistor should be in the range of 50 to 100 millivolts. This voltage drop across the resistor compares to a change in the forward voltage drop of a junction of 2 millivolts per degree centigrade. If the fact that the voltage drop across the resistor increases with temperature is ignored, the resistor can balance a minimum temperature difference of 25 to 50^{o}C between emitters. If the transistor is conducting 60 amperes, the resistance is $V/I = \frac{0.050}{60} = 8.3 \times 10^{-4}$ ohms, thus only 3.6 watts of power is lost in a one milliohm resistor.

   The chief material specification considered for the resistor was that it have a positive coefficient of change in electrical resistance with increasing temperature. Thus, as the resistor gets hotter by conducting locally greater currents, its local resistance increases and forces the current to areas operating cooler.

A number of materials were considered, as follows:

1. A metal,

2. A cermet-mixture of metal and glass insulator,

3. A suspension of metal particles in a silicone rubber, and

4. A semiconductor such as silicon.

Following are brief comments concerning each material:

If a metal were to be used for the ballast resistor, the length of the resistor would need to be very long because the specific resistance of metals is small in value. The resulting dimensions would not be suitable for the thermal design.

Cermets were discarded because of the uncertainty of the knowledge of the sintered resistance in perpendicular direction of the sheet. The electrical characteristics of cermets are averaged by their packing density of discrete metal particles in the fused glass frit. The quoted electrical characteristics are a sheet measurement after sintering but the resistance of the vertical ballast resistor is a parameter perpendicular to the sheet. Thus, cermets were discarded because of the uncertainty of the knowledge of the sintered resistance in the perpendicular direction of the sheet.

The suspension of metal particles in silicone rubber had to be discarded because it was not capable of conducting a great enough current density to be useful. This was an interesting material because it had the elastic properties of rubber and would only conduct current in those areas squeezed together so that the suspended particles made electrical contact. The material remains an insulator in neighboring areas not squeezed. In assembly, it was conceived that the 72 emitters would be slightly higher than the base region of the transistor and that a thin sheet of the rubber compound be squeezed between the end of the emitter heat-pipe and the transistor wafer such that there would only be conductive paths through the rubber in regions over the tops of the emitters.

Silicon was the material selected for the ballast resistor. If the silicon has a bulk resistivity of 1 to 1.5 ohm-cm, it exhibits a positive coefficient of electrical resistance to a temperature of about 310^{o}C. At higher temperatures the coefficient is negative, exhibiting the electrical characteristics of intrinsic silicon. However, higher temperatures would not be encountered in normal operation.

The one milliohm resistor was tailored from a silicon wafer 0.006 inch thick. The cross-section of a ballast resistor is shown in Figure 15b. Phosphorus is diffused into both sides of the ballast wafer to make ohmic contact to the silicon. Mesas of the same size as the emitters on the transistor wafer are etched into the N, N+ junction on one side and the entire wafer is metallized. The metal is etched off of the silicon in the area surrounding each mesa. A relatively heavy gold plating of 0.0005 inch thickness is deposited on top of each mesa for providing a ductile contact of low electrical resistance to each emitter when the ballast resistor is assembled to the transistor wafer.

The electrical resistance of two ballast resistors versus temperature are shown in Figure 8. The temperature dependent resistance of the ballast nearly triples over a temperature change of 300°C. The resistance of these ballasts was measured on a hot plate by employing a pulse circuit which supplied a pulse of current for 0.1 ms at a duty factor of less than 1 percent. These two resistors could not be used in subsequent devices because the gold plating diffusion bonded to the silver contacts which were used to measure their resistances. For this reason, the resistance of the ballast wafers used in devices is only measured at room temperature pricr to incorporating them in an assembly.

Section IV

TEST RESULTS

A. Early Test Results: The test results from the first transistors to be made and tested are summarized in Table 4. Devices 5 through 27 did not have a ballast wafer in the assembly of the transistor. Transistor #29 was the first device to employ an internal silicon ballast resistor. All of the devices in Table 4 failed at relatively low dissipation powers because of uneven distribution of current between the emitter fingers. The failures of devices 29 to 35 were traced to faults in the mechanical assembly of the devices not evenly distributing the current and their failures lead to the assembly techniques described in the next paragraph.

The best technique found for assembling the transistor is to gold plate the mesas on the ballast resistor with 0.0005 inch of metal, lap flat the ends of the heat-pipe, and let the collector surface of the transistor and the flat surface of the ballast wafer bear against the ends of the heat-pipes. The gold plating yields slightly under a loading of 1000 psi providing an excellent contact between the emitters and the ballast. The loading on the wafer assembly is maintained by placing the external ceramic-to-metal seal assembly of the package in tension.*

The last devices to be fabricated, Serial Nos. 55 and 56, were farther improved by having the collector of the transistor wafer soldered to the collector heat-pipe. By eliminating an internal mechanical interface, this structure lowered the thermal resistance between the junction and the collector heat-pipe. Substitution of a soft metal such as silver foil for the solder joint does not improve the thermal impedance of a mechanical joint of flat surfaces because the foil adds another interface. Quantitative results will be discussed in a following section, "Thermal Impedance."

B. Test Results with Ballasted Devices: The static test results of devices Serial Nos. 37 through 60 are summarized in Table 5. All of these Transcalent transistors were made using silicon ballast resistors. The serial number nearly indicates the sequence in which the transistors were assembled. As the serial number increases, it should be noted that the current capability of the transistor increases and the amount of power dissipated by the heat-pipes, with the exception of Nos. 50 and 51. Devices 50

*US Patent No. 3978518

Table 4 Test Results of Early Transcalent Transistors

Parameter	Units	Device Serial No. 5	8	23	24	27	29	30	31	35
V_{CBO}	Volts	1280	450	330	1000 @ 0.6 mA	400 @ 4 mA	600 @ 0.7 mA		880 @ 0.5 mA	1000
V_{CEO}	Volts	>400	260	250	575 @ 0.3 mA	280	400 @ 4.5 mA			450
V_{EBO}	Volts	1.2	14	19.5	21	21	24		22	20
Peak h_{FE}	times			33	36	33	49	46	40	47
I_C @ peak h_{FE}	Amps.			9.9	7.2	11	6.5	6.5	6.5	6.5
I_C @ h_{FE} = 10										
V_{CE} = 5 V (single sweep of steps)	Amps.			25						
V_{CE} = 10 V (@ 120 Hz DC)	Amps.			40				21		
Power dissipated operating continuously	Watts						170	230		121
Notes:				Al pin fins	Al pin fins	Au/Sn solder between Mo ballast & wafer	Al pin fins			
				Failed on curve tracer @ 50 A			First device with Si ballast wafer			

Table 5 Test Results of Transcalent Transistors with Emitter Ballasting

Parameters	Units	Device Serial No.											
		37	38	39	40	41	44	47	50	51	55	56	60
	Ohm-cm	40	40	30					70	70	40	40	40
V_{CBO}	volts	810 @ 0.5 mA	730 @ 1 mA	790 @ 0.3 mA	40	860			>960	1000	740	860	990
V_{CEO}	volts	440 @ 9 mA	400 @ 17 mA	460 @ 4 mA	40	460			720	690	420	520	520
$V_{CE(sus)}$													
V_{EBO}	volts	17.5	16.0	10.0					22.5	17.0	12.5	17.0	16.5
Peak h_{FE}		37.8	31.0	26.6					42.8		27	38	27.5
I_C @ Peak h_{FE}	amps.	11.0	10.0	13.5					7.0		15	15	7.5
I_C @ h_{FE} = 10, V_{CE} = 5 V pulsed single sweep of step @ 120 Hz		74	49.5	45	74	53			25		70	65	65
I_C @ h_{FE} = 10, V_{CE} = 5 V DC continuous dissipation	amps.	50	41	36	33	27			20	17		53	50
I_C @ h_{FE} = 5.3, V_{CE} = 6 V DC continuous dissipation	amps.			53.5									
I_C @ h_{FE} = 7.83 V_{CE} = 6 V DC continuous dissipation	amps.		32.1										
I_C @ h_{FE} = 6.54 V_{CE} = 7 V DC continuous dissipation	amps.	57											
I_C @ h_{FE} = 3.5	amps.				51.0								
Maximum power dissipated by the heat-pipes during testing	watts	453	325	336	413				300	450	126	398	523.5
Maximum continuous base current during test	amps.	7.11	7.96	10.08	14.68	7.70			7.98	7.39			13.68
$V_{CE(sat)}$*	volts	0.8 @ 35 amps.	1.0 @ 39 amps.	1.0 @ 27 amps.					0.5 @ 22 amps		1.0 @ 55 amps.	1.0 @ 55 amps.	0.4 @ 17 amps.
$I_{C(sat)}$ @ V_{CE} = 1.25V*	amps.	42	35	32					27		63	62	21.5
Max. current to which device was operated	amps.	58	52	53	51	36			35	30		150	72
Notes:		Al pin fins	Al pin fins	Al pin fins	High resistance ballast		Wafer cracked mass	**	4¼ fins Ballast 0.002 Ω		Ballast 0.005 Ω	Ballast 0.004 Ω	Ballast 0.001 Ω
					4¼ fins	4¼ fins			4¼ fins	4¼ fins	4¼ fins	4¼ fins	4¼ fins

*Includes test lead drop of test circuit.
**Joining exp. with Al. experiment.

and 51 were fabricated using crystal with a starting resistivity of 70 ohms-cm while all of the other transistors used 40 ohms-cm crystal.

By using crystal of greater resistivity, it was possible to trade off current capability for a greater voltage capability.

Transistor No. 56 was pulsed to the greatest current, 150 amperes with 300 μs pulses. Transistor No. 60 was operated at the greatest direct current, 72 amperes. While conducting the 72 amperes, the heat-pipes were dissipating 523 watts of thermal energy.

Most of the devices exhibited an open gate collector-to-base voltage greater than 750 volts and collector-to-emitter voltage greater than 400 volts. Several devices were lost in fabrication by cracking the wafers while compression loading the package and by not having all of the electrical leads of the device properly grounded during welding.

Individual test characteristics will be discussed more fully in the following sub-sections.

C. Current Gain: The current gain, h_{FE}, versus collector current, I_C, of the Transcalent transistors having silicon ballast resistors are shown in Fig. 16 to 21.

Fig. 16 compares the current gain of transistors employing crystals with different starting resistivities. The starting resistivity of the silicon crystal for transistor No. 37 was 40 ohm-cm compared to 70 ohms-cm for devices No. 50 and 51. All of the transistors have a moat 0.002 inch wide and 0.0005 inch deep etched around the periphery of each emitter-to-base junction. The etching removes the silicon of higher surface concentration in the region of the junction. This concentration would allow a portion of the base current to be shunted across the surface and reduce h_{FE}. The effect is most noticeable at base currents of less than 0.75 ampere, and probably accounts for the difference in gain of Nos. 50 and 51. No. 51 must have some mechanism for shunting a portion of the base drive to the emitter at the lower collector currents. The shunt has negligible effect at the higher collector currents.

Fig. 17 contains the plots of the current gains versus the collector currents for Transcalent transistor No. 37 at heat-pipe temperatures of 25, 60 and 100°C and with a V_{CE} of 5.0 volts. As the temperature of the device increases, the gain of the transistor decreases for currents greater than the current at the peak gain. At currents less than the current at the peak gain, the gain increases with increasing temperature. This is typical of power transistors.

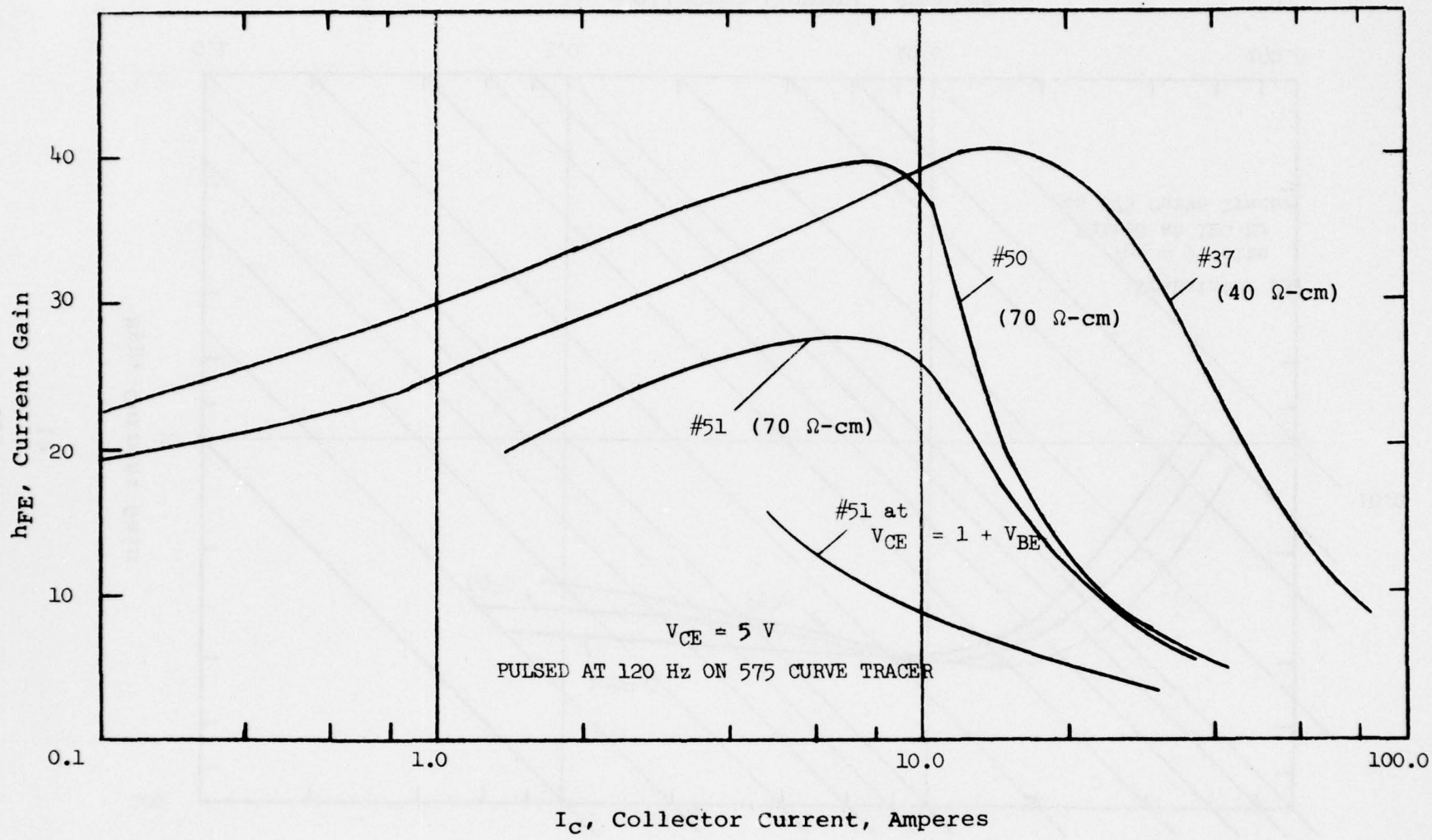


Fig. 16 Direct Current Gain Curves for Transcalent Transistors with Different Starting Crystal Resistivity

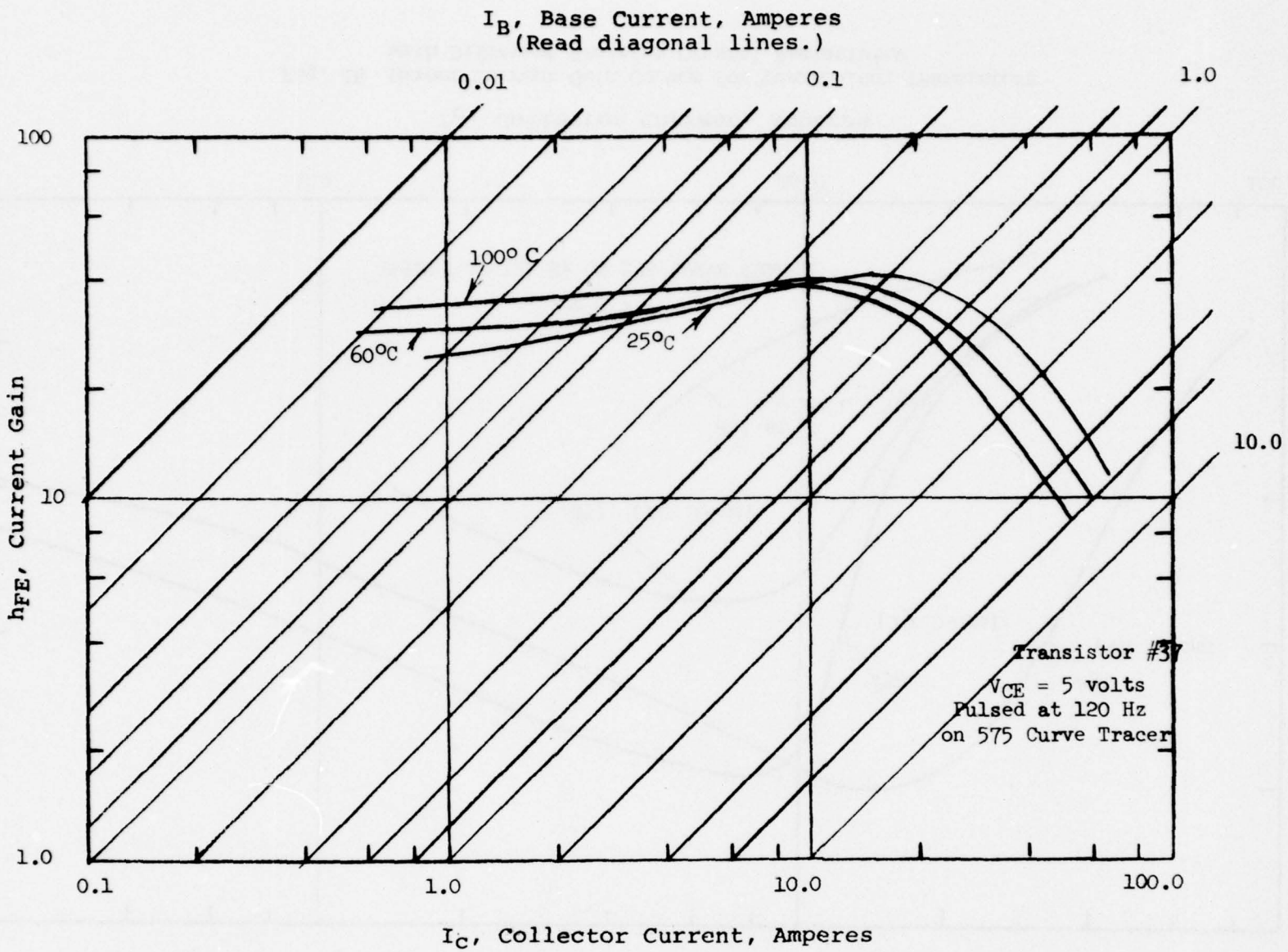


Fig. 17 Pulsed Current Gain Curves for Transcalent Transistor No. 37 at different heat-pipe temperatures.

Fig. 18 shows the current gain of Transcalent transistor No. 60 versus the collector current, I_C, while operating at two different conditions. The pulsed data was gathered from a Tektronix 575 curve tracer in which the base current, I_B, was increased in steps at 120 Hz and at a preset base current per step. The device was triggered once and the collector current at each step of base current was recorded photographically. A typical photographic recording of I_C vs. V_{CE} for various base currents is shown in Fig. 19. The collector current was always less if it was reached through a large number of steps of base current rather than in a few steps. This shift in values is due to heating of the silicon. The current gain for the direct current curve is also less than for a pulsed curve because of the heating of the silicon. This latter curve was determined on device #60 by operating the transistor with a collector-to-emitter voltage of 5 volts while conducting the collector current. At each data point, sufficient time was awaited to record the collector and base currents so that the silicon chip was in thermal equilibrium with the heat-pipes. Thus, when the transistor was conducting an I_C of 70 amperes with a base current, I_B of 12.17 amperes, the power dissipated by the heat-pipes was 365 watts.

Even though the heat-pipes were operating at 68°C, this amount of power heats the silicon sufficiently to slightly degrade the current gain. At V_{CE} = 7 volts, this transistor was operated at a direct current of 72 amperes while dissipating 524 watts of power from the heat-pipes. During these tests, the device was mounted in an air duct slightly larger in cross-section than the device fins and cooled by air flow at a velocity of 1550 ft. per min.

A measure of current crowding can be gained by plotting the logarithm of h_{FE} versus the logarithm of I_C at a collector voltage one volt greater than the voltage between the emitter and base.[6] This kind of data is plotted in Fig. 20 and shows an improvement trend in the assembly of devices. This slope of -1 is an ideal behavior and current crowding is indicated as a device shifts to a -2 slope. Transistors No. 37 and 41 were among the first devices capable of operating at high currents without thermal runaway and show a shift from near a -1 slope to a -2 slope. These two devices were assembled using annealed 5 mil. silver foil between the ends of the heat-pipes and the silicon wafers (transistor and ballast), with a minimum of soft metal between the emitters and the mesas on the ballast wafers. A temporary acrylic binder held the ballast wafer to the transistor wafer while the wafer assembly was being clamped between the ends of the heat-pipes. The binder was dissolved and rinsed away with acetone prior to welding. Experience indicates that some of

(6) J. Olmstead, W. Einthoren, S. Ponczak & P. Kannam "High-Level Current Gain in Bipolar Power Transistors", RCA Review, June 1971, p. 221-246.

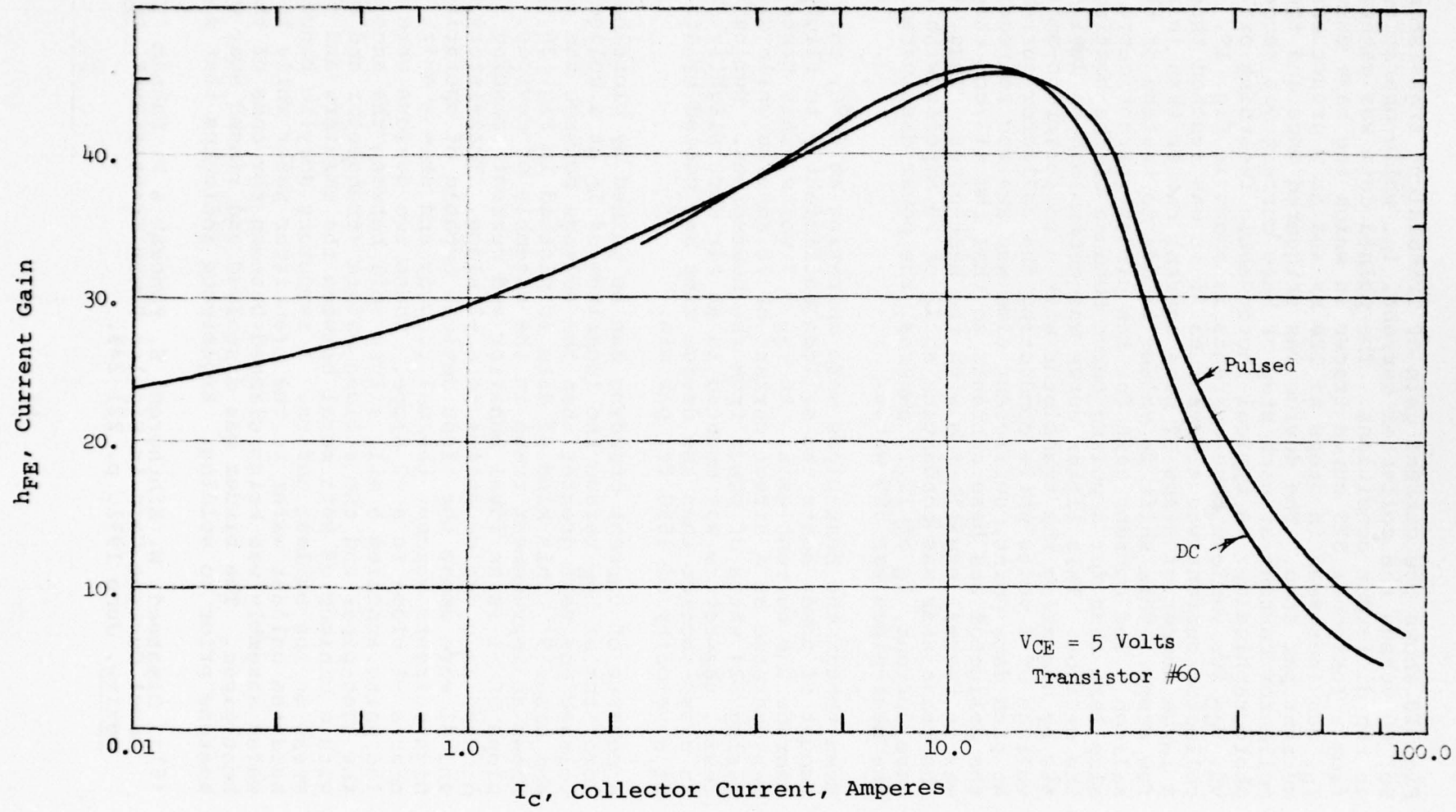


Fig. 18 Pulsed and DC gain curves for Transcalent transistor No. 60

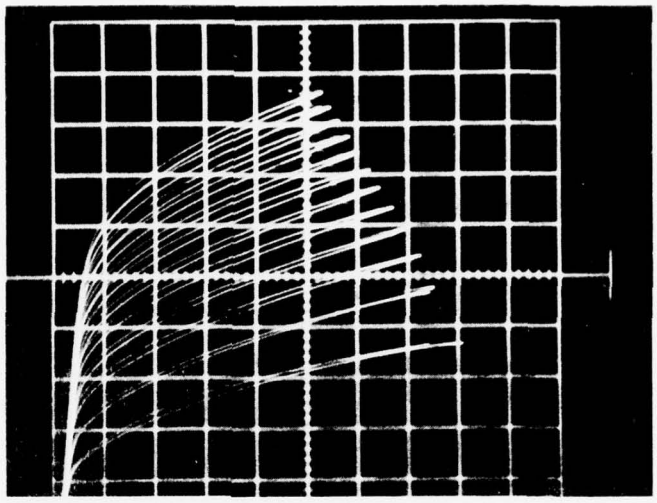


Fig. 19 Gain curves for Transcalent transistor No. 60. The scales are 1 volt/div. horizontal, 10 amp/div. vertical and a base drive of 1 amp/step. The zero current line was lost by the camera so that the first full trace at a base drive of 1 ampere is 32 amperes. The maximum current is 86 amperes at 5.4 volts.

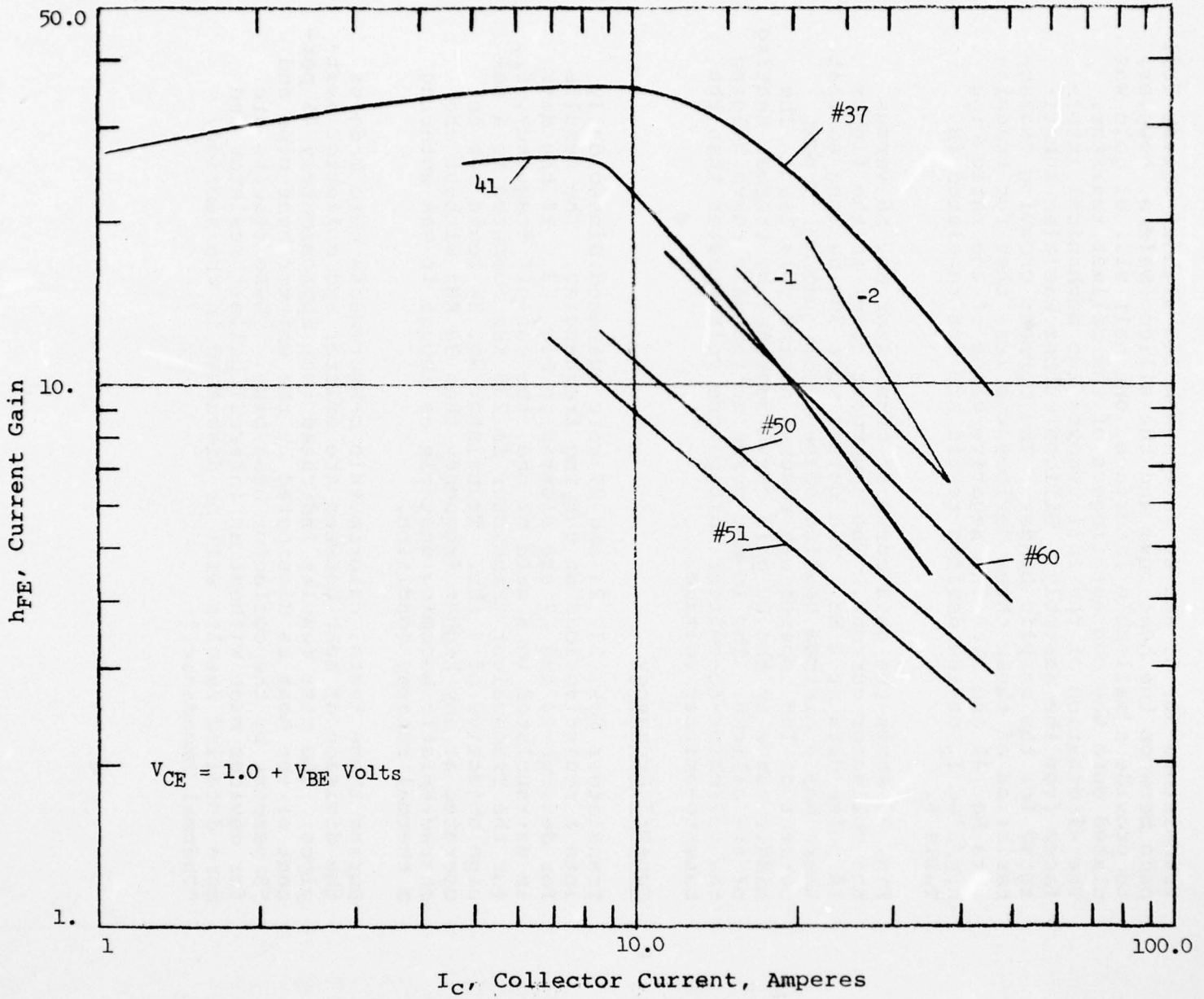


Fig. 20 Gain curves at emitter-to-collector voltage one volt greater than the base-to-emitter voltage.

dissolved binder gets in between the metallizing on the emitter and the ballast and is not rinsed away completely.

Transistors 50, 51 and 60 were assembled without silver foil pads between the heat-pipes and the silicon wafers, however, to provide a malleable interface, one half mil. of gold was plated onto the contact fingers of the ballast resistor. The elimination of the foil removes two mechanical interfaces from the assembly. Silicon rubber was also substituted for the acrylic binder. The current crowding characteristics of these three devices was less than for transistors No. 41 and 37. The negative slope of the ratio $\Delta \log h_{FE}/\Delta \log I_c$ of the devices tested are are tabulated in Table 6.

Fig. 21 shows the gain curve of transistor No. 56 versus the collector current. The uppermost curve in the figure is pulse data at 4 Hz. The pulses were 300 μs long so that there was a minimum heating of the silicon junction. A peak current of 150 amperes was reached during this test. The middle curve is the DC gain curve degraded by thermal heating of the silicon. The lowest curve is the gain curve holding the collector-to-emitter voltage one volt greater than the base-to-emitter voltage.

D. Cut-Off Frequency

Transistors Nos. 23, 24 and 27 were operated sinusoidally into a resistive load at varying frequencies. The results for devices 24 and 27 are plotted in Fig. 22. If the data is extrapolated to a gain of one, the cut-off frequency, f_t, for the Transcalent transistor is 230 KHz compared to a design objective of 4 KHz. Transistor No. 24 could not be operated at any higher frequency than 30 KHz without the characteristic becoming unstable as though it was entering a thermal runaway condition.

During these tests, calorimetric measurements were made of the division of heat between the emitter and collector heat-pipes. The test results indicated that approximately 45 percent of the heat is dissipated by the emitter heat-pipe and 55 percent by the collector heat-pipe. These results are for devices made without an internal ballast resistor and more detailed results will be discussed in the section, "Thermal Impedance."

Slope of the Gain Curves in Figure 20

Table 6

Device No.	$\Delta \log h_{FE} / \Delta \log I_C$
37	-1.47
38	-1.36
39	-1.20
41	-1.20
50	-0.862
51	-0.845
56	-1.01
60	-1.01

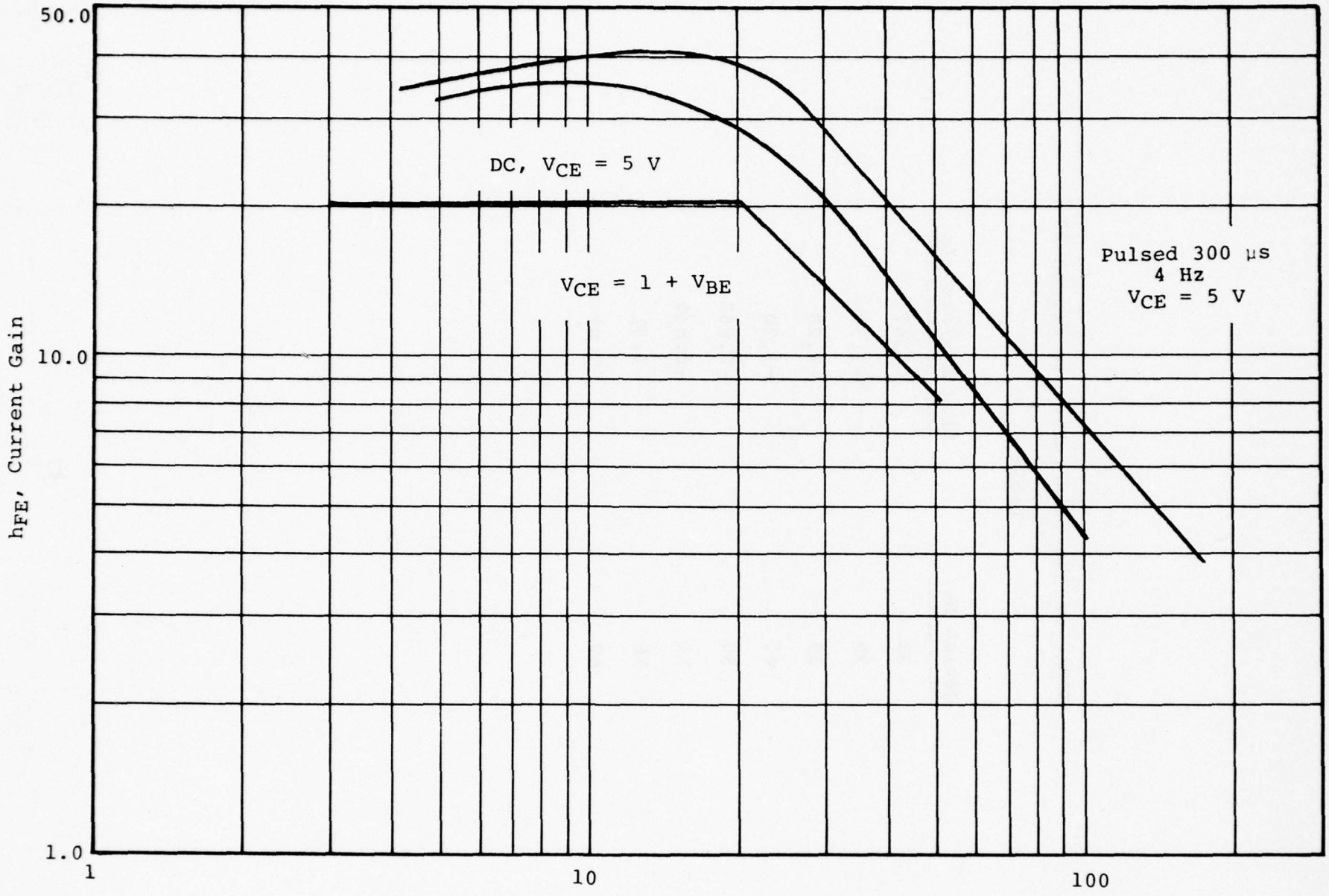


Fig. 21 Current Gain for Transcalent Transistor No. 56

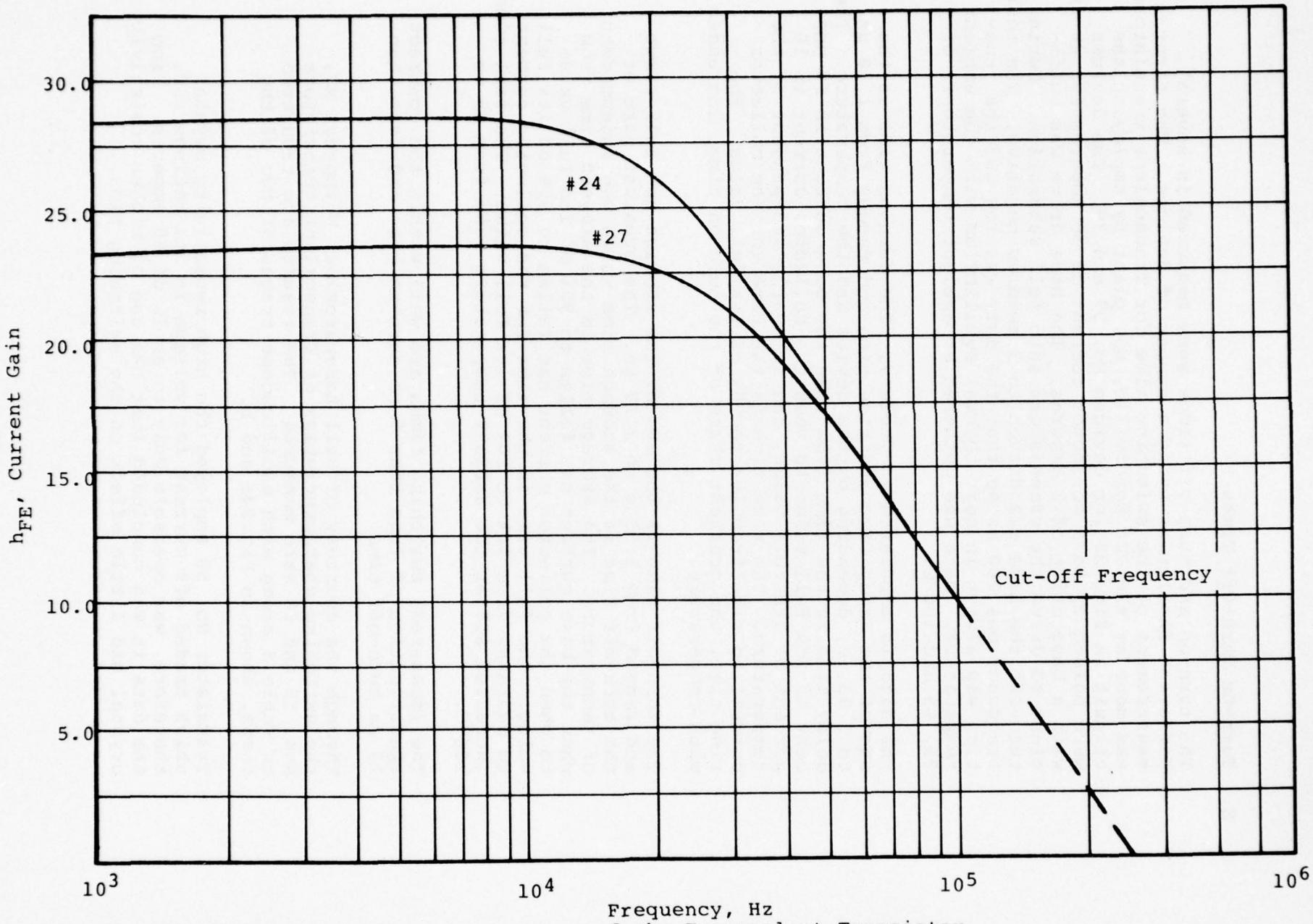


Fig. 22 Current Gain Versus Frequency of the Transcalent Transistor

E. Turn-On Turn-Off Times

The turn-on and turn-off times were measured in several different facilities using a number of devices. The first measurement of the switching time for Transcalent transistors was done at the RCA Somerville, NJ, plant by employing the circuit in Fig. 23 for devices No. 37 and 39. The devices were pulsed up to a collector current of 30 amperes for 20 μs with a base drive of 3 amperes. The base drive was sufficient to drive the transistors into full saturation. During turn-off the base was driven to 3 amperes negative. The test frequency was 200 Hz so that the duty was low and the junction was always in near thermal equilibrium with the ambient temperature. Data was gathered at ambient temperatures of 25, 65 and 100°C.

The data is tabulated in Table 7. The turn-on time is the sum of the delay time and rise time and ranges from 1.18 μs to 1.83 μs, depending on the device and the temperature. The delay time is the time from when the base current is 10 percent of its full value to when the collector current is 10 percent of its full value, and is nearly independent of the temperature. The rise time is the time for the collector current to rise from 10% to 90% of its full value. The rise time, the greatest share of the turn-on time, increases with temperature.

The turn-off time is the sum of the storage and fall times and ranged from 1.53 μs to 2.17 μs. The greatest part of the turn-off time is the storage time which was independent of temperature. The storage time is the elapsed time from when the base current has fallen to 90% of its full value to when the collector current has fallen to 90% of its full value. The fall time is the time for the collector current to decrease from 90% to 10% of its full value. The fall time increased 65% as the ambient temperature rose from 25 to 100°C.

The (measured) switching times are well within the contract specification of less than 5 μs turn-on time and less than 10 μs turn-off time.

Through the courtesy of Bell Laboratories, Whippany, NJ, the switching characteristics of Transcalent transistors Nos. 50 and 60 were measured. The results are tabulated in Table 8 along with oscilloscope traces of two of the tests, shown in Fig. 24a and b.

Transistor No. 50 employed the high resistivity crystal which traded off current for voltage in its ratings and, therefore, was operable only to an I_C of 30 amperes. From the data it was concluded that the use of higher resistivity crystal had little effect on the switching time.

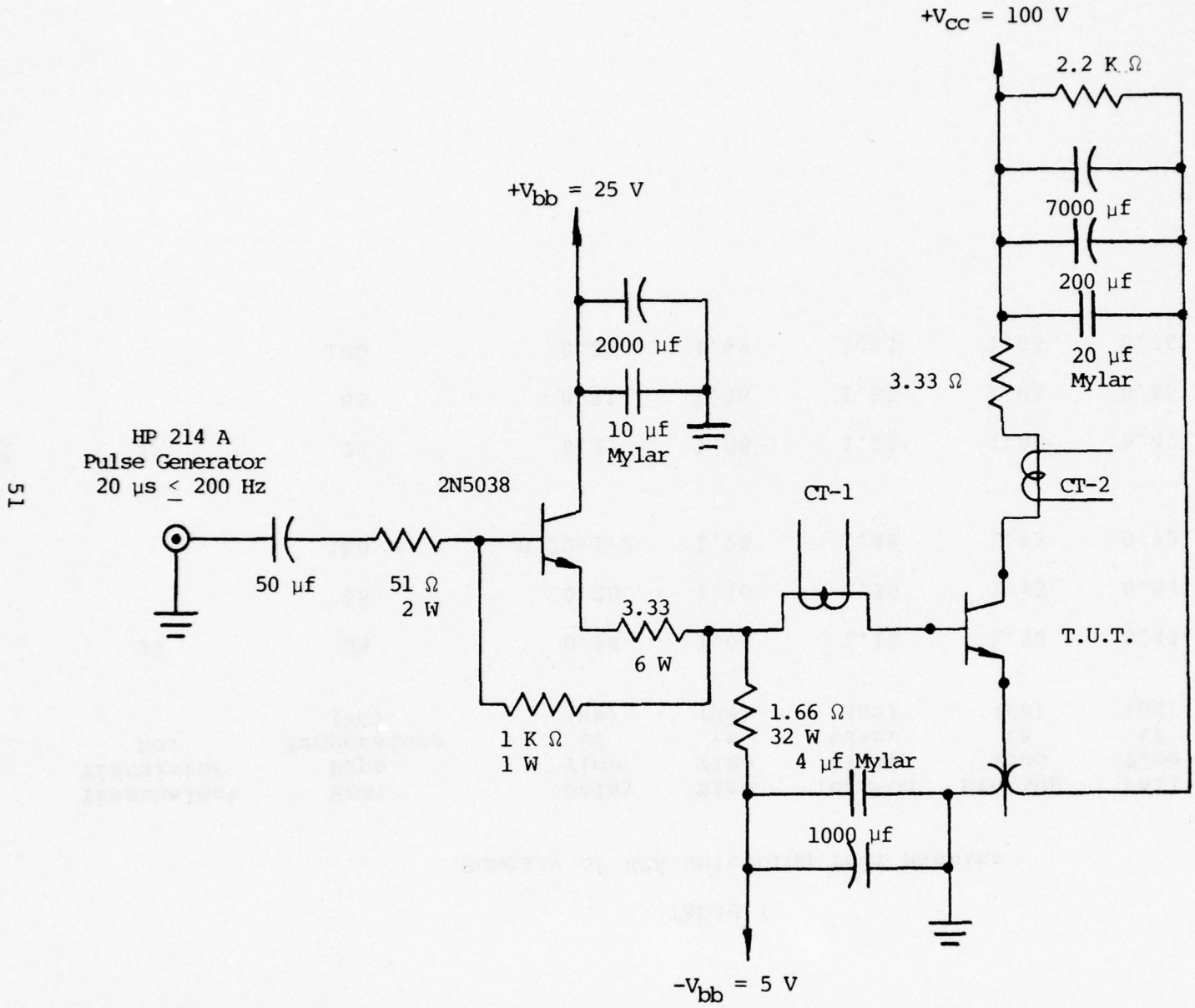


Fig. 23 Switching Speed Test Circuit

Table 7

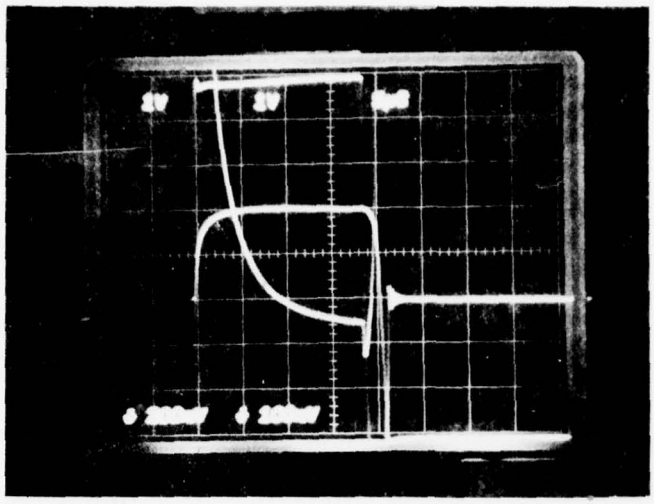
Summary of RCA Switching Test Results

Transcalent Transistor No.	Heat Pipe Temperature (°C)	Delay Time td (μs)	Rise Time tr (μs)	Turn-On Time td+tr (μs)	Storage Time ts (μs)	Fall Time tf (μs)	Turn-Off Time ts+tf (μs)
37	25	0.18	1.00	1.18	1.50	0.47	1.97
	65	0.20	1.10	1.30	1.45	0.64	2.09
	100	0.20-1/2	1.28	1.48	1.45	0.72	2.17
39	25	0.21	1.08	1.28	1.06	0.47	1.53
	65	0.21	1.36	1.57	1.05	0.66	1.71
	100	0.23	1.60	1.83	1.05	0.76	1.81

Table 8

Summary of Bell Laboratory Switching Test Results

Temp. °C	td (μs)	tr (μs)	ts (μs)	tf (μs)	t_{on} (μs)	t_{off} (μs)	I_c (AMP)	$+I_b$ (amp)	$-I_b$ (amp)	V_{cc} (V)	h_{FE} (times)	Pulse Length (μs)	Rep. Rate (pps)
DEVICE #50													
30	0.1	0.6	1.7	0.6	0.7	2.3	30	8	8	50	3.8	22	110
DEVICE #60													
30	0.1	0.6	1.6	0.5	0.7	2.1	60	8	8	105	7.5	60	25
110			1.6	0.9		2.5	60	8	8	105	7.5	25	100



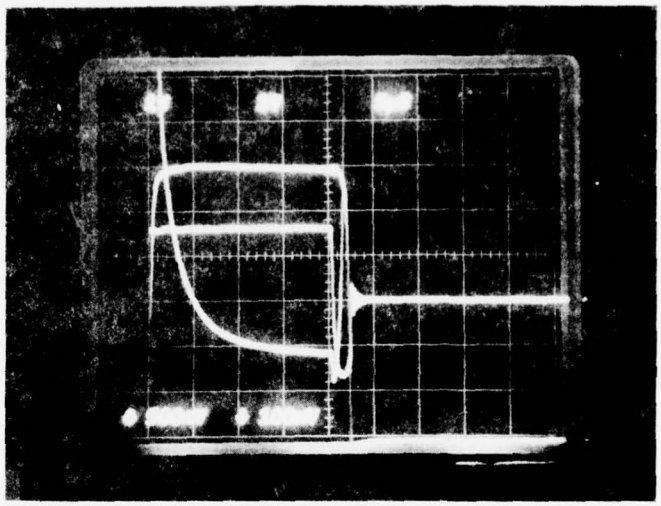
T_C = 125°C

I_C = 50 A

I_B = 10 A 2 A/div.

V_{CE} = 4, 3 & 2½ V

t = 5 μs/div.



100 Hz 30°C

I_C = 10 amp/div.

I_b = 5 amp/div.

$V_{CE(SAT)}$ 1 v/div.

t = 5 μsec/div.

I_C = 60 A

Fig. 24 Oscillographs of switching speed test at Bell Labs.

In both photographs the collector current trace originates at the zero line, lower left corner, rises and falls rapidly, 10 amp/div., forming the broad square wave pulse with the rounded corners. The parabolically falling curve is the V_{CE} voltage drop across the transistor. Zero voltage is at the bottom line of the reticle. Zero base drive is the curve that is off-set 3 div. from the bottom line of the reticle on the right side. In the upper photograph at 125°C, the positive base drive trace is at the top of the photograph and swings negative off the bottom of the photograph. In the lower photograph, both traces of the positive and negative base drive current are evident.

Transistor No. 60 was operated at collector currents up to 60 amperes. The major difference between these test results and those reported in Table 7 is that the storage time is greater. The greater storage time is due to the greater collector current density in these tests. Even though transistor No. 50 was operated at 30 amperes, the same current as devices No. 37 and 39, it was being operated nearer to its maximum current capability.

F. Second Breakdown Tests

The Transcalent transistor was investigated for its safe operating area in the high power region. Limitations for low voltage, high current and for high voltage, very low currents were easily determined by the use of the Tektronix type 576/176 curve tracer and through D.C. testing. However, to submit the device to a maximum stress of high voltage, for known pulse durations, high current control requires special circuitry to prevent destruction of the device under test. This is especially critical when the device operation is carried well into the second-breakdown current area.

A pulsed test circuit, designed for 350 volts and 26 amperes with adjustable pulse widths from ten microseconds to one second, was constructed to test the Transcalent devices to these levels. The original design[7] of this test equipment was for a smaller device but it was felt its capacity would cover critical voltage and current areas. Also since it was anticipated that there may be failures, the decision was made to test the transistor and its ballast wafer in the demountable heat-pipe cooled assembly illustrated in Fig. 25.

The detection circuit utilized in the test equipment that samples the collector-to-emitter voltage of the device under test was tested to determine its speed and sensitivity. It measured +3 volts at 175 nanoseconds, a satisfactory value. Thus, when the device under test is driven into saturation, the emitter voltage must remain three volts below the collector voltage. If the emitter voltage suddenly increases, as in a failure or at the beginning of a current-second breakdown, the detection circuit is activated and the drive to the pass transistors is removed. The detection circuit is gated on only during the current pulse since stored charge in the device under test and a base turn-off diode could cause a false indication at the end of the pulse. A further feature is that the detection circuit is D.C. coupled to accommodate slow changing conditions, for example, in a long pulse gradual failure mode.

(7) R. B. Jarland R. Kumbatoric, "A Test Set for Nondestructive Safe Area Measurements Under High-Voltage, High Current Conditions", AN-6145 RCA Power Transistors Selection Guide/Data/Application Notes 1975, SSD-204C pp. 797-804

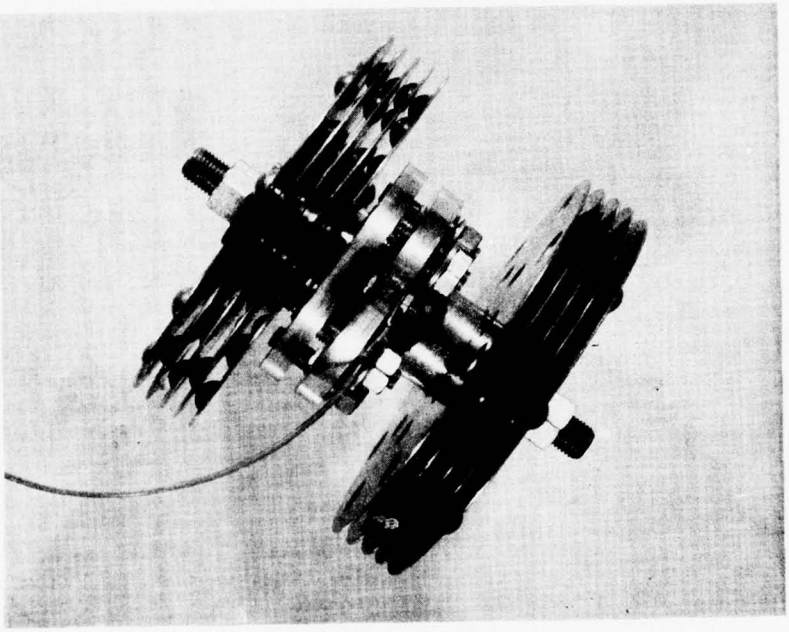


Fig. 25 Photograph of the Demountable Transcalent Package

The inital check-out of the equipment included testing an RCA type 2N5240 transistor which is the device used in the pass transistor test section of the test equipment itself. The results were very gratifying in that the performance was slightly better than the published data for pulse widths of 18,200 and 1000 milliseconds.

Testing proceeded with the demountable Transcalent test fixture, Fig. 25, utilizing pre-processed heat sinks (heat-pipes) that allowed for bolting the transistor wafer and ballast resistor between the collector and emitter heat-pipes. Four wafers, identified as #101, #104, #105 and 107, were tested using these demountable heat sinks.

Data was recorded predominately at 100 μsec, 18 msec, and 1000 msec pulse widths.

Data was repeatable when using the same device but the spread of data at short pulses (100 μsec) was more from device to device than at longer pulses. The composite data for the four devices is shown in Fig. 26. The data is averaged to the worst case device and is, therefore, somewhat conservative. It should be noted that the interval between test pulses was maintained at approximately thirty seconds for the short pulses to two minutes for the long pulses. No forced air cooling was used during these tests and a low duty factor was maintained to prevent elevated junction temperatures.

In Figure 27 is a summary of all test data, defining the safe operating area for the Transcalent transistor.

G. Power Switching Test

In all of the characterizing tests which have been described in the earlier parts of this report, the transistor was tested either at a high current, a high voltage, a low frequency or a very low duty. The test parameters do not simultaneously subject the transistor to the stresses encountered in a high current, high voltage switching application. In a switching application, the current and voltage wave forms must cross each other in time, the transistor must operate at high frequencies and at the same time, dissipate the heat losses in the silicon. To test the Transcalent transistor in a switching application, the circuit shown in Fig. 28 was constructed. The Transcalent transistor was used to switch the power from a 440 volts, 25 amperes D.C. power supply into the 7.5 ohms resistive load. To obtain greater test currents, 60 amperes at a 10 percent duty, the switching transistor and the load were shunted by a 3,300 μf capacitor. The base of the T.U.T. was negatively biased and switched positively through the 500 μf capacitor.

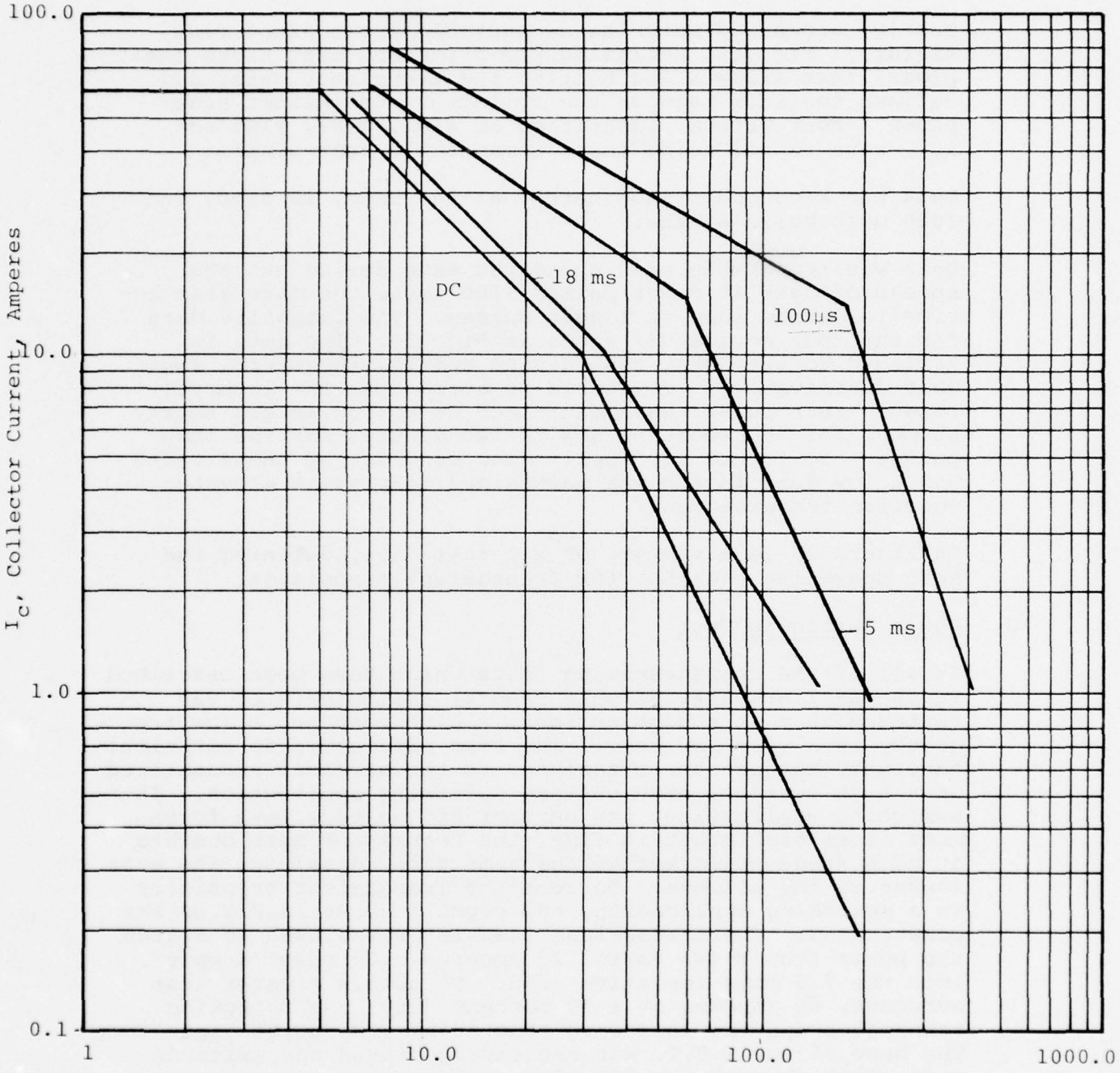


Fig. 26 Summary of Second Breakdown Current Test Results

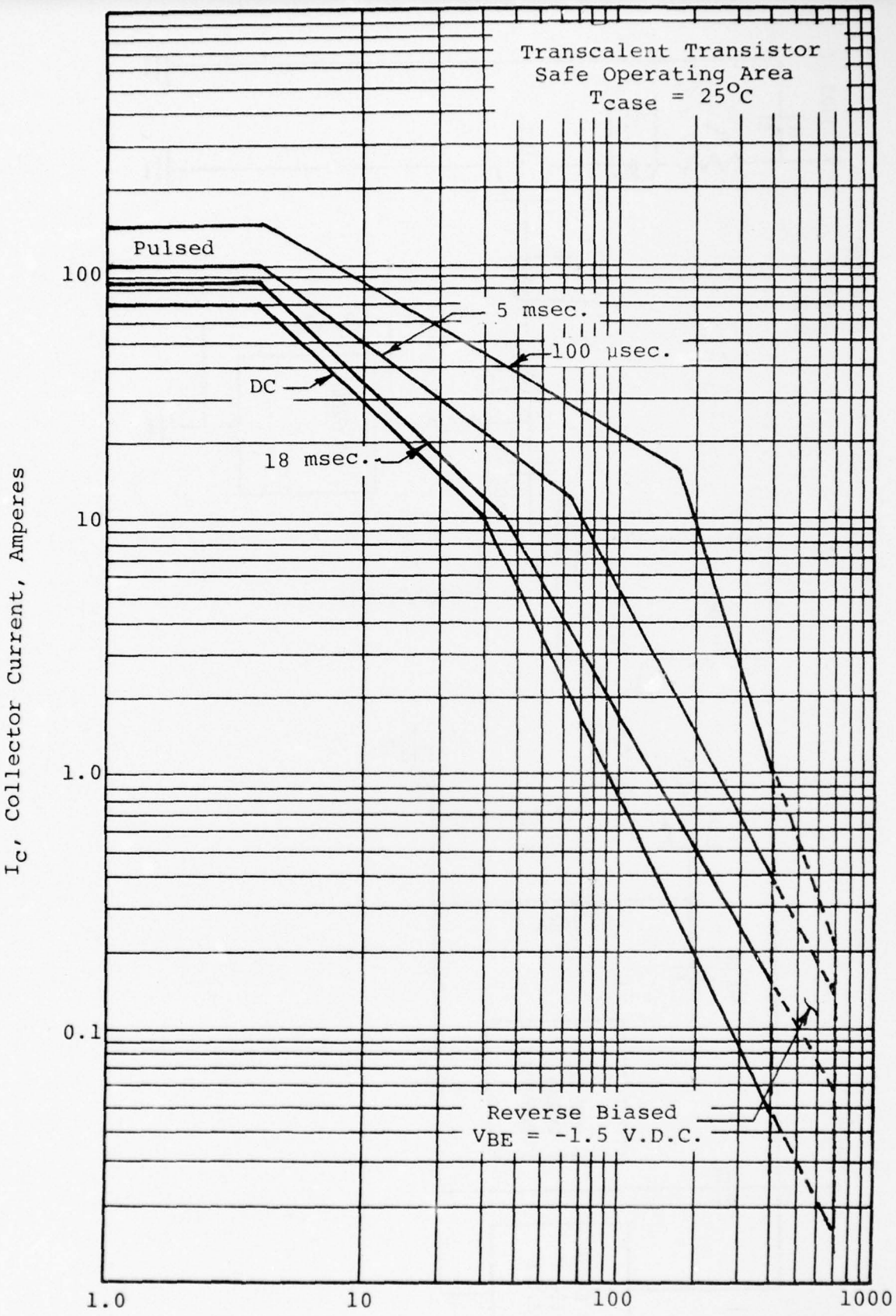


Fig. 27 Transcalent Transistor Safe Operating Area

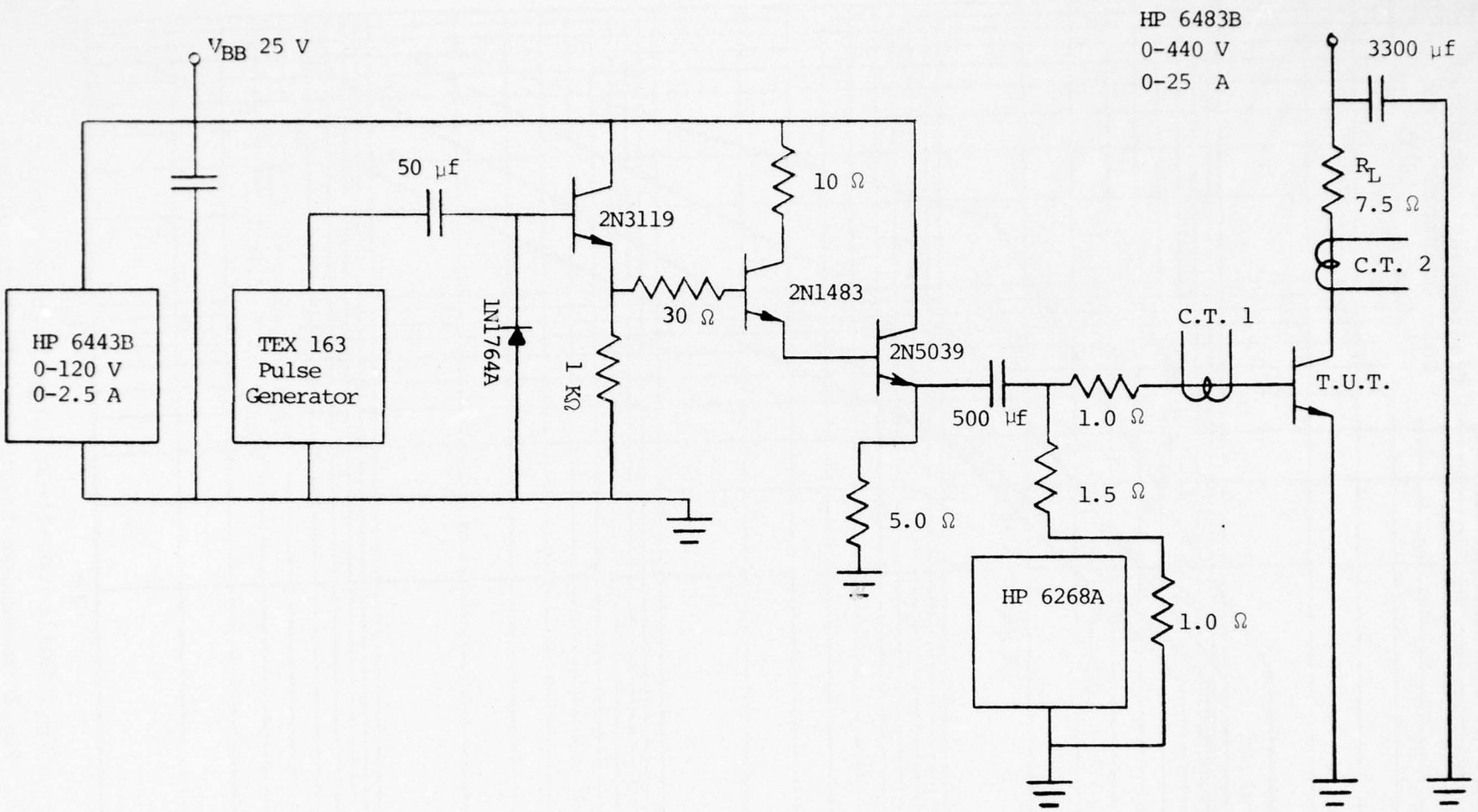


Fig.28 High Current Switching Test Circuit

Transistors Nos. 50 and 60 were tested in the circuit described. Transistor No. 50 was a high voltage, V_{CEO} = 720 v, lower current 35 amperes Transcalent transistor using the high resistivity starting crystal while No. 60 was a lower voltage, V_{CEO} = 520 v, high current, 60 amperes Transcalent transistor using the lower resistivity starting crystal, as described previously.

Transistor No. 50 was operated up to a frequency of 20 KHz while switching 35 amperes into the load from a power supply voltage of 290 volts. Photographs of the leading and trailing edges of the pulse are shown in Fig. 29 a, b, and c. The rise time is 0.75 μs, the fall time 1.4 μs and the storage time 4.0 μs. (The fall time and storage time would have been less but the transistor was only being turned off with a negative base drive of about two amperes. In Fig. 30 is plotted the power dissipated in the silicon while switching 35 amperes at 270 V and a rate of 10 KHz. Most of the power is dissipated when the transistor turns off, a lesser amount of power while turning on and very little power during conduction and blocking.

Similar switching data is shown in Fig. 31 a, b, c, and d and Fig. 32 for Transcalent Transistor No. 60. The test was conducted at 60 amperes, 400 volts, a switching frequency of 5 KHz and a duty of 10 percent. The turn-on time was .8 μs, the storage time 4.5 μs and the fall time .8 μs. The base drive turning the transistor on was 11 amperes and 4.4 turning it off. A negative drive equal to the drive turning the transistor on would have speeded up the turn-off but a larger power supply was not available. The power losses during switching are summarized in Fig. 32 . The peak dissipation during turn-off is 8700 watts. Thus, the power loss during conduction is minimal if the transistor is driven into full saturation. In Fig. 31 b, the saturation voltage drop is a minimum 0.8 volt which means that 48 watts are the losses in the silicon at that instance. An SCR would have had much greater losses and would not have been able to switch as rapidly. With these tests, it was demonstrated that the Transcalent transistor could switch up to 24 kW of power.

H. Transit Thermal Analysis

As an aid to design of the RCA Transcalent devices, Dr. Russell Eaton, III of MERADCOM developed a thermodynamic analytical computer model for predicting the time dependent temperature distributions in a Transcalent device consisting of a silicon chip and the contiguous wick structures. The model, which is based on four important assumptions for a simplified device geometry and constant material properties,

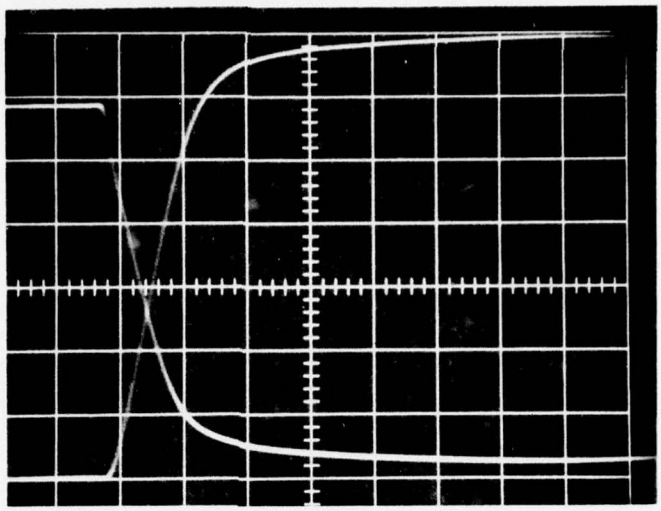


Fig. 29a Turn-on characteristics of Transcalent Transistor No. 50 switching 35 A from 290 Vdc at 20 KHz. The upper curve starting on the left and falling is the V_{CE} voltage trace. The other curve is the current trace. The vertical scales are 50 V/div. and 5A/div. The horizontal scale is 0.5 μs/div.

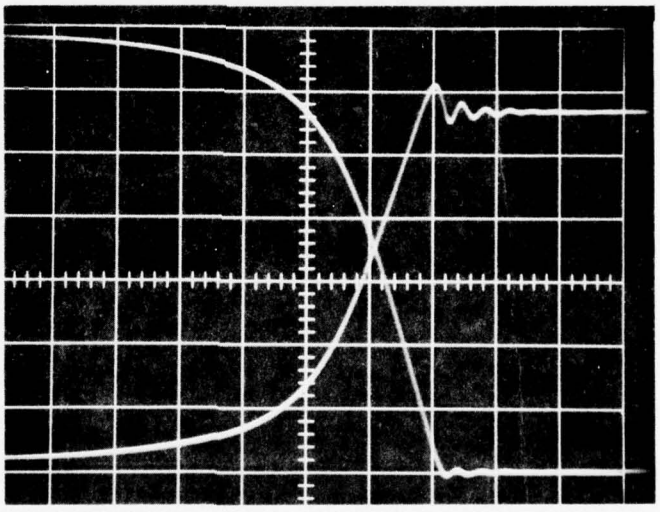


Fig. 29b Turn-off characteristics of Transcalent Transistor No. 50 switching 35 A at 285 V and at 20 KHz. The falling curve on the left is the current trace and the rising curve is the voltage trace. The time base is 0.5 μs/div.

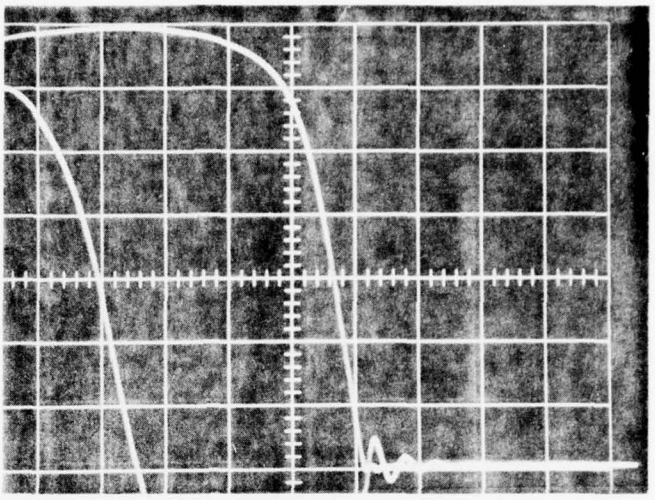


Fig. 29c Turn-off characteristics of Transcalent Transistor No. 50 switching 35 A at 285 V and 20 KHz. The traces are the collector and base current. The lower curve starting at the left is the base drive. The time difference between the two curves is due to storage of carriers in the transistor. The vertical scales are: collector current: 5 A/div; base current; 2 A/div. and the time base is 1 μs/ div.

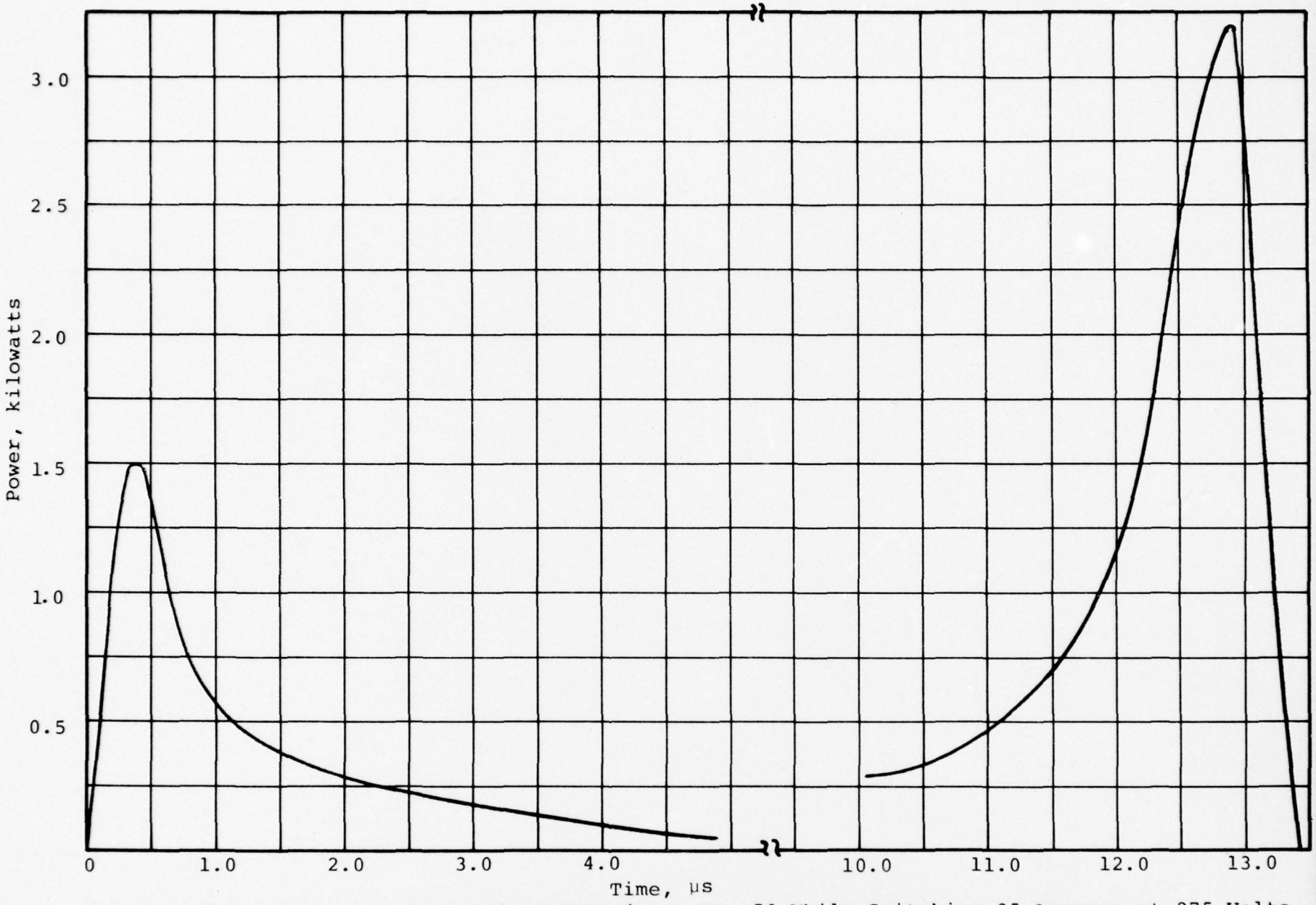


Fig. 30 Power Losses in Transcalent Transistor No. 50 While Switching 35 Amperes at 275 Volts

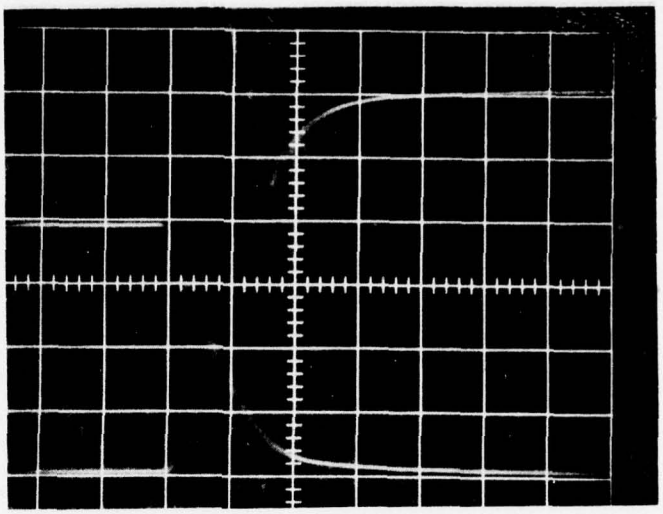


Fig. 31a Turn-on characteristics of Transcalent Transistor No. 60 switching 60 A from 400 Vdc. The upper trace on the left is V_{CE} = 400 V and the upper on the right is i_C = 60 A. The zero voltage and current reference is the solid line at the bottom. The horizontal scale is 0.5 μs/div. and the vertical scales are 100 v/div. and 10 A/div, respectively.

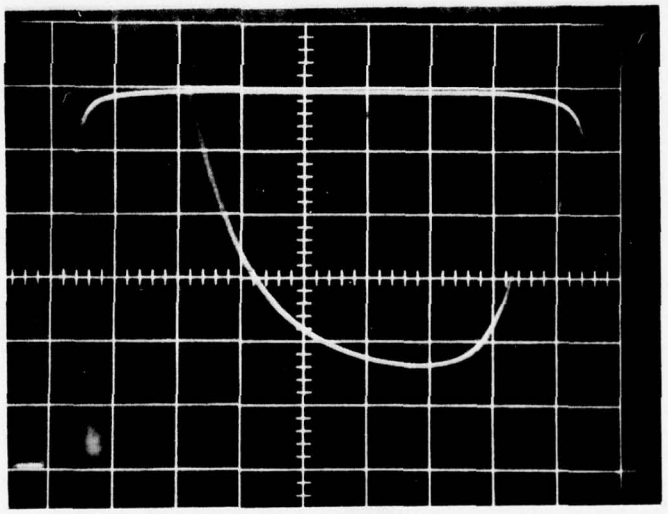


Fig. 31b The saturation voltage drop across Transcalent Transistor No. 60 is evident in this expanded trace while conducting 60 A. The nearly horizontal trace at the top is i_C and the lowest trace is $V_{CE(sat)}$. The horizontal trace is 2.0 μs/div. and the vertical scales are 0.5 v/div. and 10 A/div. The zero ref. is the bottom solid line.

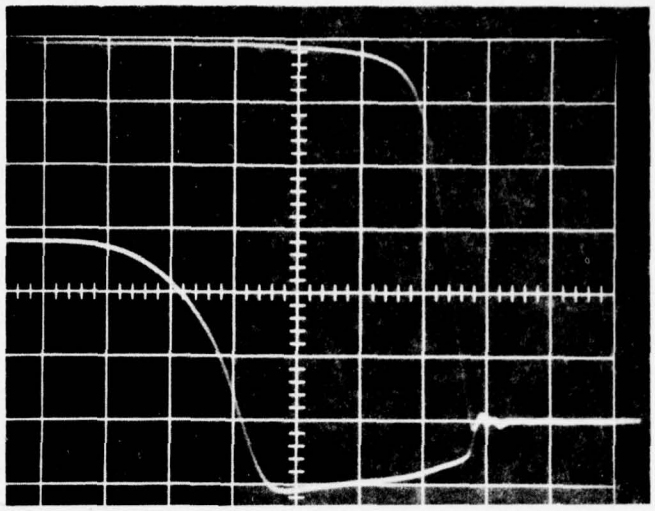


Fig. 31c The turn-off characteristics of Transcalent No. 60. The uppermost trace is i_C = 60 A and lower curve is $\pm i_B$. The horizontal scale is 1.0 μs/div. and the vertical scales are 4 A/div. for i_B and 10 A/div. for i_C. The zero reference is the second solid line from the bottom.

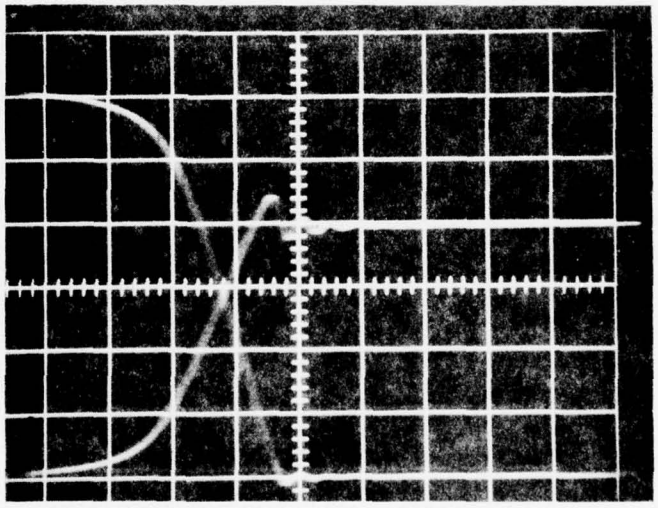


Fig. 31d Fall time characteristics of Transcalent Transistor No. 60. The uppermost curve, starting on the left, is the current trace. The lower curve, starting on the left and rising, is the voltage between the collector and the emitter. The vertical current scale is 10 A/div., the vertical voltage scale is 100 v/div. with their zero values being the solid line at the bottom of the photograph. The time scale is 0.5 μs/div.

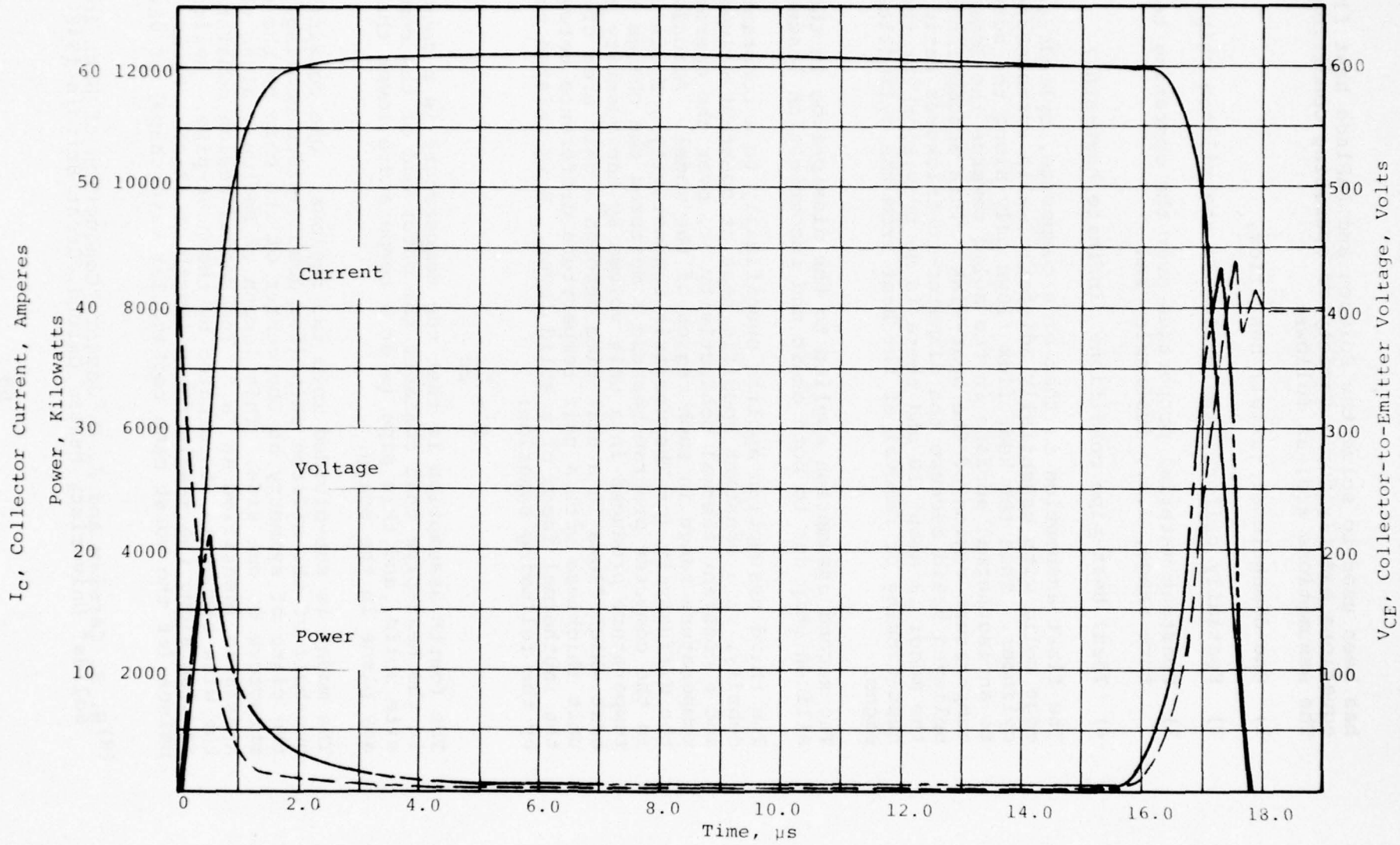


Fig. 32 Current, Voltage and Power Losses While Transcalent Transistor No. 60 was Switching 60 Amperes at 400 Volts and at 5 KHz

has been used to solve the Poisson and LaPlace heat flux equations exactly for a variety of operating conditions.[8] The assumptions are, as follows:

1) One-dimensional (axial) heat flow,

2) Spatially uniform dissipation in the silicon chip,

3) Constant material properties over the operating temperature range, i.e., isotropic; and

4) Ideal heat-pipe conditions (infinite heat-sink).

The first assumption is that of a composite, cylindrical edge solid with essentially adiabatic walls surrounding the cylinder. Thus the heat flux flows only along the normal to an isothermal surface in the solid towards the lower temperature region of the heat-sink. This assumption is believed valid because the diameter-to-thickness ratio of the model is about 10 and there is no provision for the heat-sinking or removal of the heat from the cylindrical edges.

The second assumption applies to the dissipation in the silicon chip due to both ohmic and recombination losses.

The third assumption applies specifically to a constant mass density, ρ; a constant specific heat at constant volume, c; and a constant thermal conductivity, κ, over the operating temperature range in each region of the model. Actually, the diffusivity (or Thermometric Conductivity), K, is used in the computer program because K measures the change in temperature produced in a unit volume by the quantity of heat which flows in a unit time through a unit area of a unit thickness with a unit temperature difference between the isothermal faces of a solid layer. K is related to κ by the following equation:

$$K = \frac{\kappa}{\rho c} \qquad (1)$$

The fourth assumption is that the temperature is a constant in the heat-pipe that contacts the outer end of the composite solid, and this pipe is at a temperature lower than any plane in the solid.

The model is sub-divided into two regions. One consists of one-half of the silicon chip (for double-sided cooling) from the plane of symmetry at the center of the chip to the wick structure on one side. This length of Region I along the x-axis is identified as "a." The second region consists of the wick structure, terminated by the heat-pipe. Region II is also along the x-axis for a length of (ℓ-a). Power pulses (of the worst case rectangular wave shape) of varying

[8] H. S. Carslaw and J. C. Jaeger "Conduction of Heat in Solids" Univeristy Press, Oxford, Great Britain 1948

duty factors provide the source term in Region I. This source term is a function of time, t, only.

The basic equations include the one-dimensional diffusion equations for each region of the model. For each of the two regions the differential equations for the diffusion of the heat flux are, as follows:

$$\nabla^2_I T_I(x,t) = \rho_I \frac{c_I}{\kappa_I}\left[\frac{\partial T_I(x,t)}{\partial t}\right]\frac{-A}{\kappa_I} \tag{2}$$

where: T is the temperature in ^oC,
x is the distance in centimeters from the plane of symmetry in the range of $0 \leq x \leq a$,

t is the time in seconds from the application of the power source,

I is the subscript that denotes the values of each parameter in Region I, and

A is the heat source term per unit time per unit volume.

$$\nabla^2_{II} T_{II}(x,t) = \rho_{II} \frac{c_{II}}{\kappa_{II}}\left[\frac{\partial T_{II}(x,t)}{\partial t}\right] \tag{3}$$

where: II is the subscript that denotes the values in Region II and

x is the range of $a \leq x \leq \ell$.

Note that there is no source term in Region II.

The following boundary conditions are applied to (2) and (3):

@ x = 0; $\text{grad}_I T_I(0,t) = 0$; since the central isothermal plane divides the heat flux flowing to each heat-pipe and can thus be treated as a perfect insulator.

@ x = a; $\kappa_I \text{grad}_I T_I(a,t) = \kappa_{II} \text{grad}_{II} T_{II}(a,t)$; the Lorentz conductivity equation for the conservation of energy constraint of continuous flux.

@ x = a; $T_I(a,t) = T_{II}(a,t)$; the continuity of temperature constraint.

@ $x = \ell$; $T_{II}(\ell,t)$ = Constant = $0^{o}C$; the assumed ambient condition of the infinite heat sink.

Solutions of (2) and (3) involve the use of Laplace Transforms to reduce the partial differential equations to ordinary differential equations and the inverse transforms which lead to convolution integrals. The resulting Transcendental equations for the temperatures are extremely complicated, thus, the details of these solutions have been omitted from this report to allow adequate space for both the empirical and the experimental results.

The solutions have been converted into a graphical digital computer code, which is programmed to run on a MERADCOM minicomputer system consisting of a PDP 15/76 and a Tek. 4010 graphics terminal. An overlay system permits the code, which consists of the main program and sub-routines, to be run on the minicomputer system even though the entire code is too large to fit into the memory core of the computer (limited to 16K at one time). This code permits the designers to vary interactively the geometry of the device and the wick, as well as the frequency of the maximum amplitude of the power pulse. When the results are presented graphically, the designers can observe the effects these variables have upon the transient and equilibrium thermal behavior of the modeled devices.

As an option, the user can select any device isothermal plane between the center of the silicon and the heat-pipe to display the temperature as a function of the time after turn-on. The computed results are also available to the user in tabular form. This code has provided the designers of the Transcalent devices with an important tool for quickly determining the effects that their design choices have upon the thermal behavior of the design variables. Other applications at different power levels can also be evaluated prior to operation of the device in a new circuit. Reliable operation at safe temperatures can thus be predicted or verified in advance of the circuit fabrication. A few of the case studies and their results are described in the following paragraphs.

In Fig. 33 are plotted the computed junction temperatures of Transcalent transistor No. 60 dissipating a record 523 watts. The two curves are for different areas, the emitter and the collector areas. Note that much better cooling was predicted on the collector side resulting from the larger area in contact with the heat-pipe. On the emitter side, only the area of the emitter finger contacting mesas (of the ballast resistor) was assumed. The boundary condition of the same temperature at the junction will result in the temperature of the actual operating device to fall between the two curves.

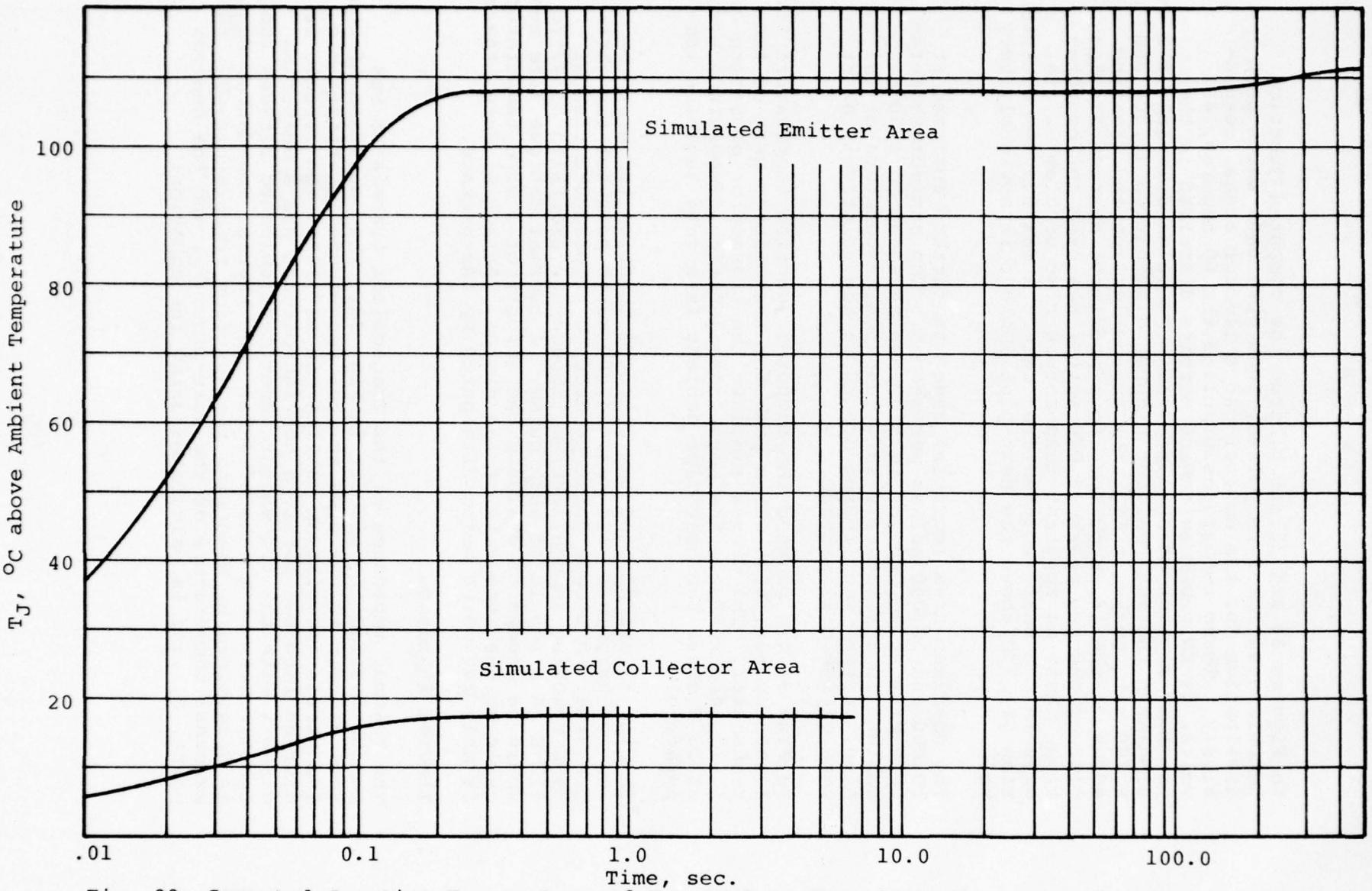


Fig. 33 Computed Junction Temperature of Transcalent Transistor No. 60 Dissipating 523 Watts

In Figures 34 and 35 are plotted the computed junction temperatures for 2 μs pulses, 5000 pps, 6000 watts peak dissipation for the emitter and collector areas, respectively. These two graphs simulate the 60 amperes, 400 volts, 24 KW power switching service described in the previous section of this report. The pulse duration of 2 μs simulates the intervals of highest dissipation (4,300 and 8,700 watt peaks in Fig. 32) at the leading and trailing edges of the 18 μs pulse. An approximate average dissipation of the two peaks (6,000 watts) was used for computation. Note no apparent temperature rise problem exists, even in the small emitter area case. A maximum temperature rise of 13°C above the heat-pipe ambient is obviously very safe.

The smallest area (emitter) case was further analyzed at 10,000 and 20,000 pulses per second. The maximum temperature rise at 20,000 pps is 51°C, which added to a 50°C ambient is a relatively safe junction temperature of 101°C. Also, thermal equilibrium occurs in the relatively short time of 200 milliseconds.

In Fig. 36 are plotted the computed junction temperature for 2 μsec pulses, 6000 watts peak for the emitter area of the transistor. The curves simulate the transistor operating at 5, 10, and 20 KHz. The worst case junction temperature rise of 51°C above the heat-pipe ambient is a safe junction temperature.

In Fig. 37 are plotted the computed junction temperatures for 100 μs pulses, 100 pps, 24,000 watts peak for the emitter area. A single pulse produces a temperature rise of 54°C reaching an equilibrium temperature excursion of 47 to 112°C as a result of each pulse. A thermal fatigue life test would be needed to evaluate the effects of a 65°C temperature cycle on the integrity of the device. At a 0.01 duty, there is only 240 watts being dissipated by the package.

I. Thermal Impedance

The thermal impedance of the Transcalent transistor was measured using the circuit in Fig. 38. The operation of the test circuit is the same as that recommended in Electronic Industries Association publication RS-313B. The circuit is divided into two parts, a heating circuit and a measuring circuit with the transistor under test switched between the two circuits at a rate of 4 Hz. The thermal impedance, $R_{\theta JC}$, is determined by measuring the junction temperature, T_J, the external temperature of the heat-pipe, T_C, and the heating power, P, and is calculated using the equation:

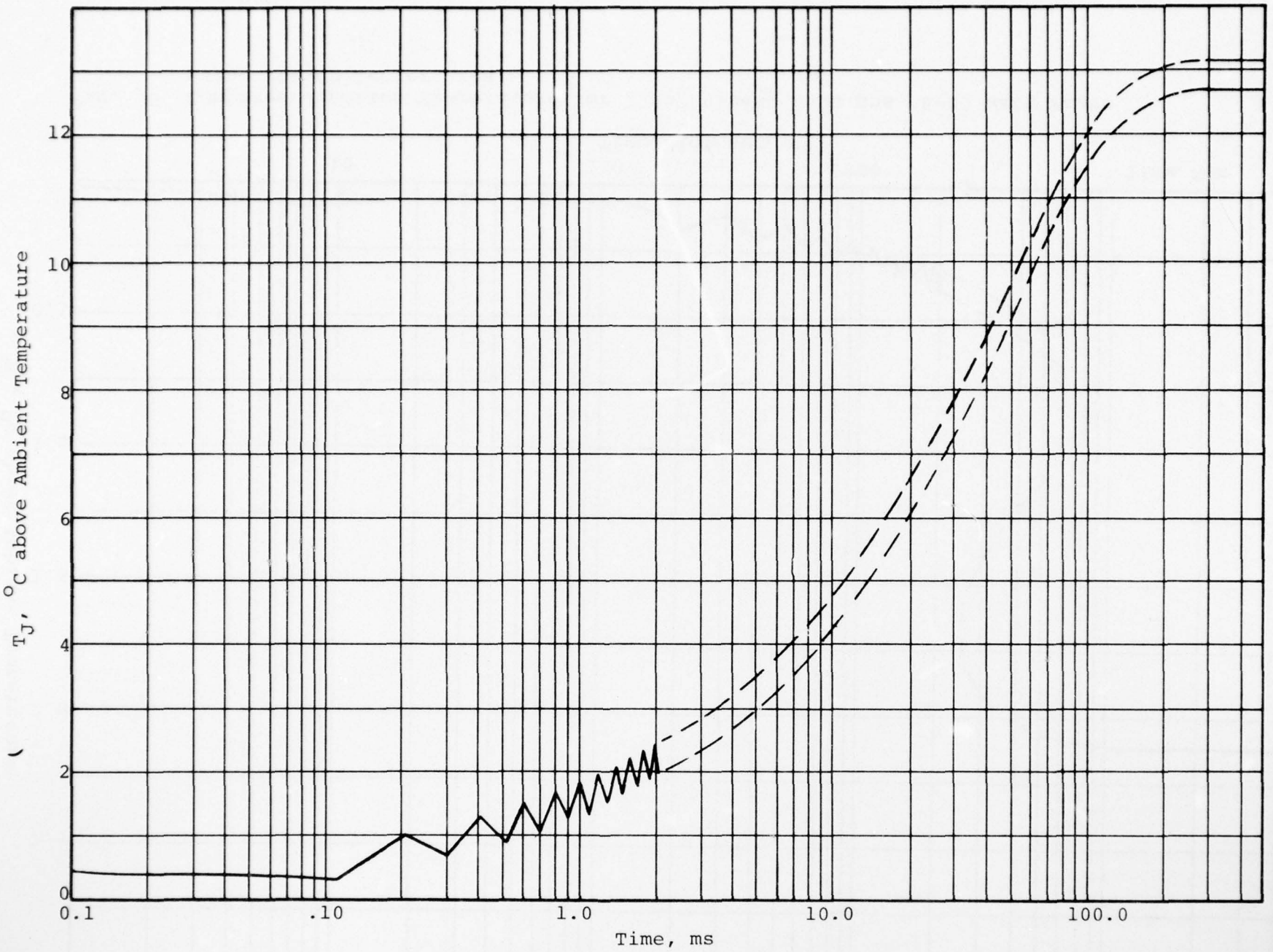


Fig. 34 Computed Junction Temperature for 2 μs Pulses, 5000 pps, 6000 Watts per Peak, using the Emitter Area

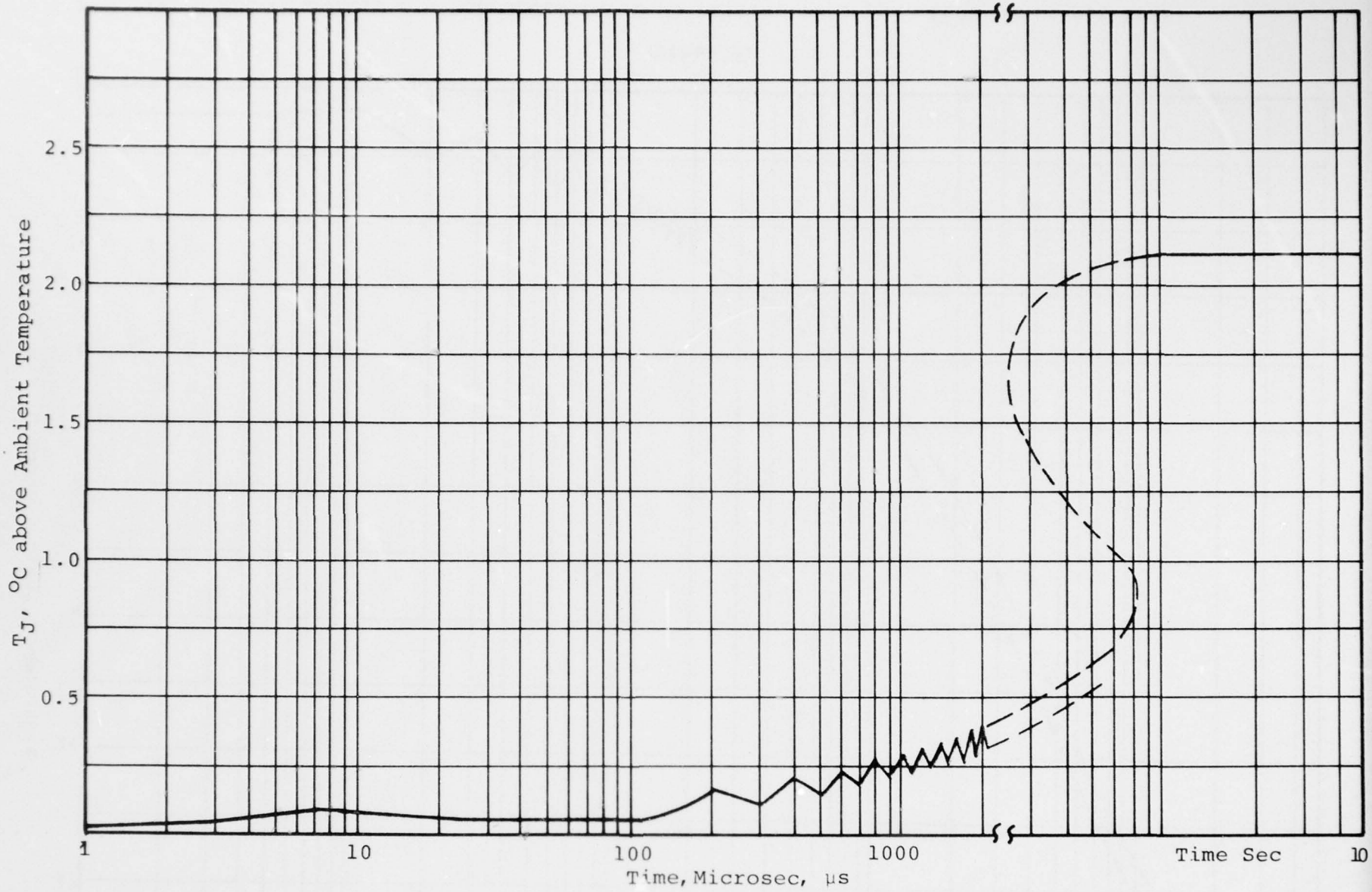


Fig. 35 Computed Junction Temperature for 2 μs Pulses, 5000 pps, 6000 Watt Peaks using the Collector Area

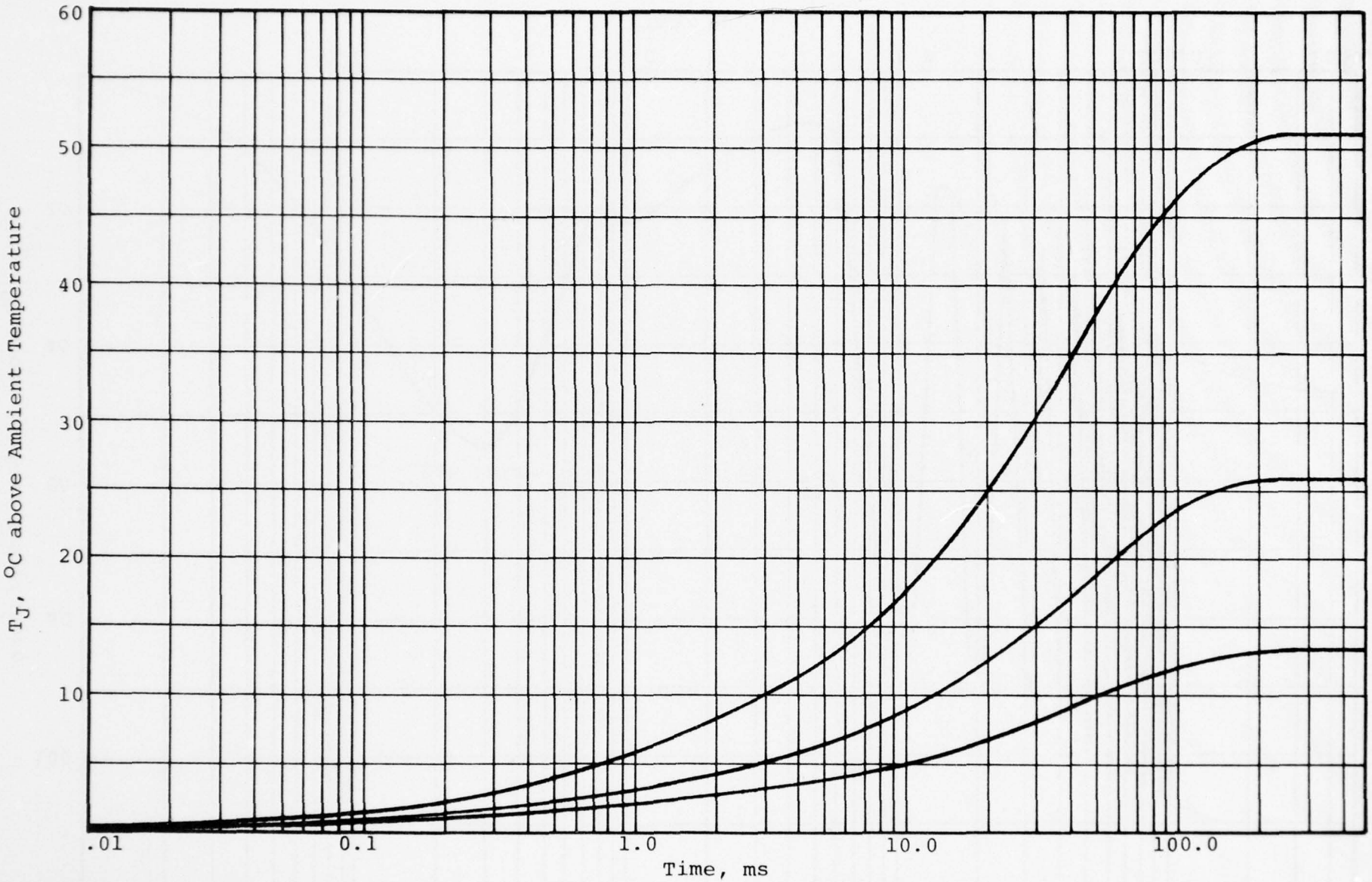


Fig. 36 Computed Junction Temperatures, 2 μs Pulses, 6000 Watts Peaks, 5, 10, 20 KHz, using the Emitter Area

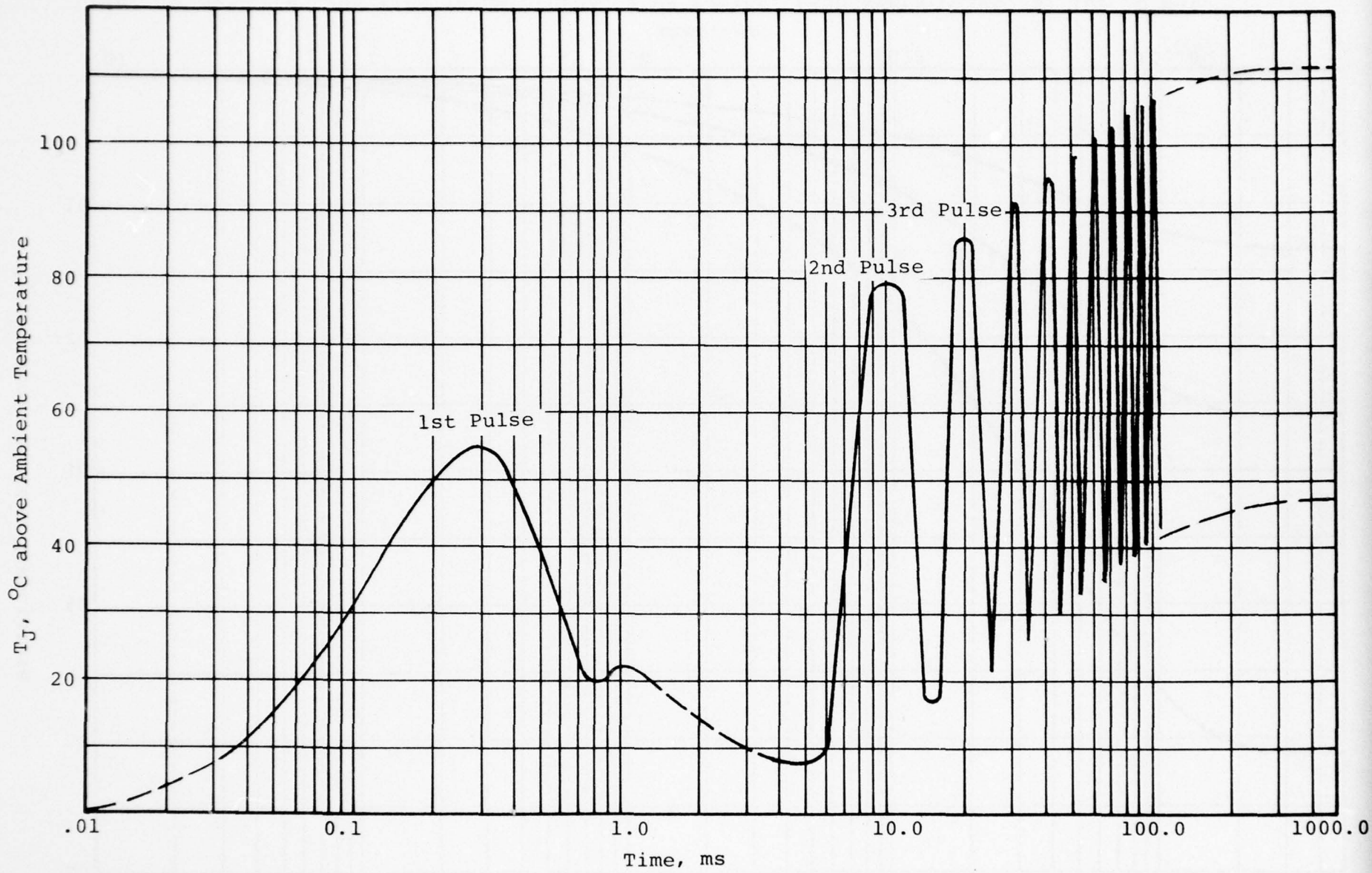


Fig. 37 Computed Junction Temperature for 100 μs Pulses, 100 pps, 24000 Watts per Peak using the Emitter Area

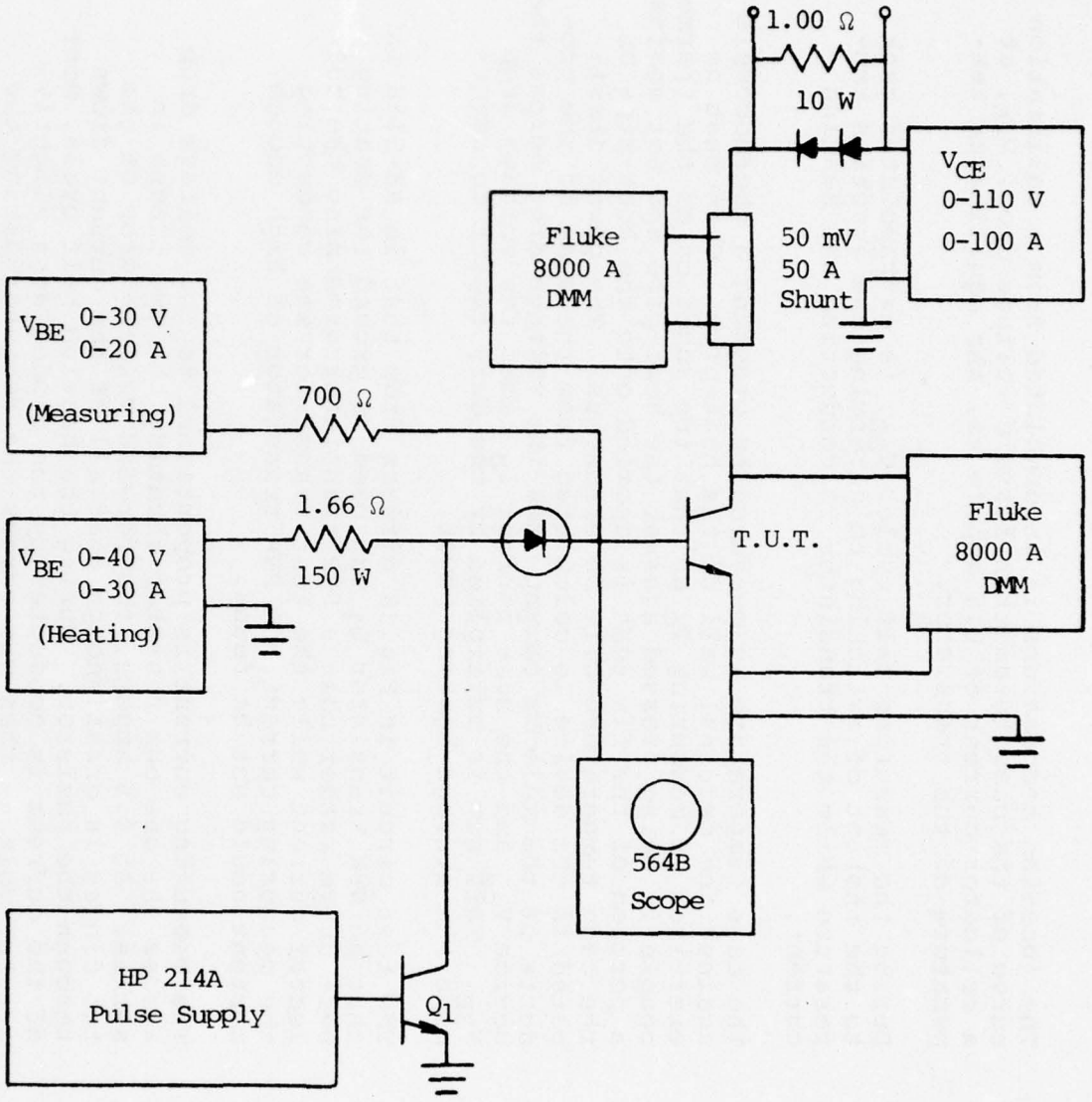


Fig. 38 Thermal Impedance Test Circuit

$$R_{\theta_{J-C}} = \frac{T_J - T_C}{P}$$

The junction temperature is interpolated from a calibration curve of the base-to-emitter forward voltage drop, V_{BE}, at a collector current of 0.5 ampere vs. the equilibrium temperature of the transistor.

During the measuring half cycle, V_{BE}, is extrapolated back to the instant of switching to determine the junction temperature while the transistor is conducting the heating current.

The case temperature is measured by pressing a thermocouple against the external wall of the heat-pipe. Care must be exercised in measuring T_c so that the junction of the thermocouple is being pressed against the heat-pipe and not against a portion of the fin that is epoxied onto the heat-pipe or the case temperature will be erroneous. The power dissipated in the device is calculated from the sums of the products of the collector current times the voltage drop across the device V_{ce} and the base current I_b times the voltage drop V_{BE}. This sum is multiplied by the duty factor to determine the average heating power.

The test circuit in Fig.38 differs from that in RS-313B in that an NPN transistor Q_1 was used to ground the heating base drive rather than a PNP transistor grounding the collector current while the test transistor was conducting the measuring current. A PNP transistor of high enough current could not be found.

The measuring current is proportional to the voltage drop across the one ohm resistor shunting the two diodes in series. At 0.5 ampere, the forward voltage drop of the two diodes is great enough that all of the current flows through the resistor. During the heating half cycle, most of the current is conducted by the diodes at a slightly greater voltage than was across the resistor during the measuring portion of the cycle. This avoids over dissipation in the one ohm resistor.

The thermal resistance data is summarized in Figures 39 and 40 . In Figure 39 is the thermal impedance between the junction and case versus the input power with the cooling air moving across the fins at three different velocities. The data is the average of three devices 50, 51 and 60 which were assembled by clamping the ballast and transistor wafers between the heat-pipes.

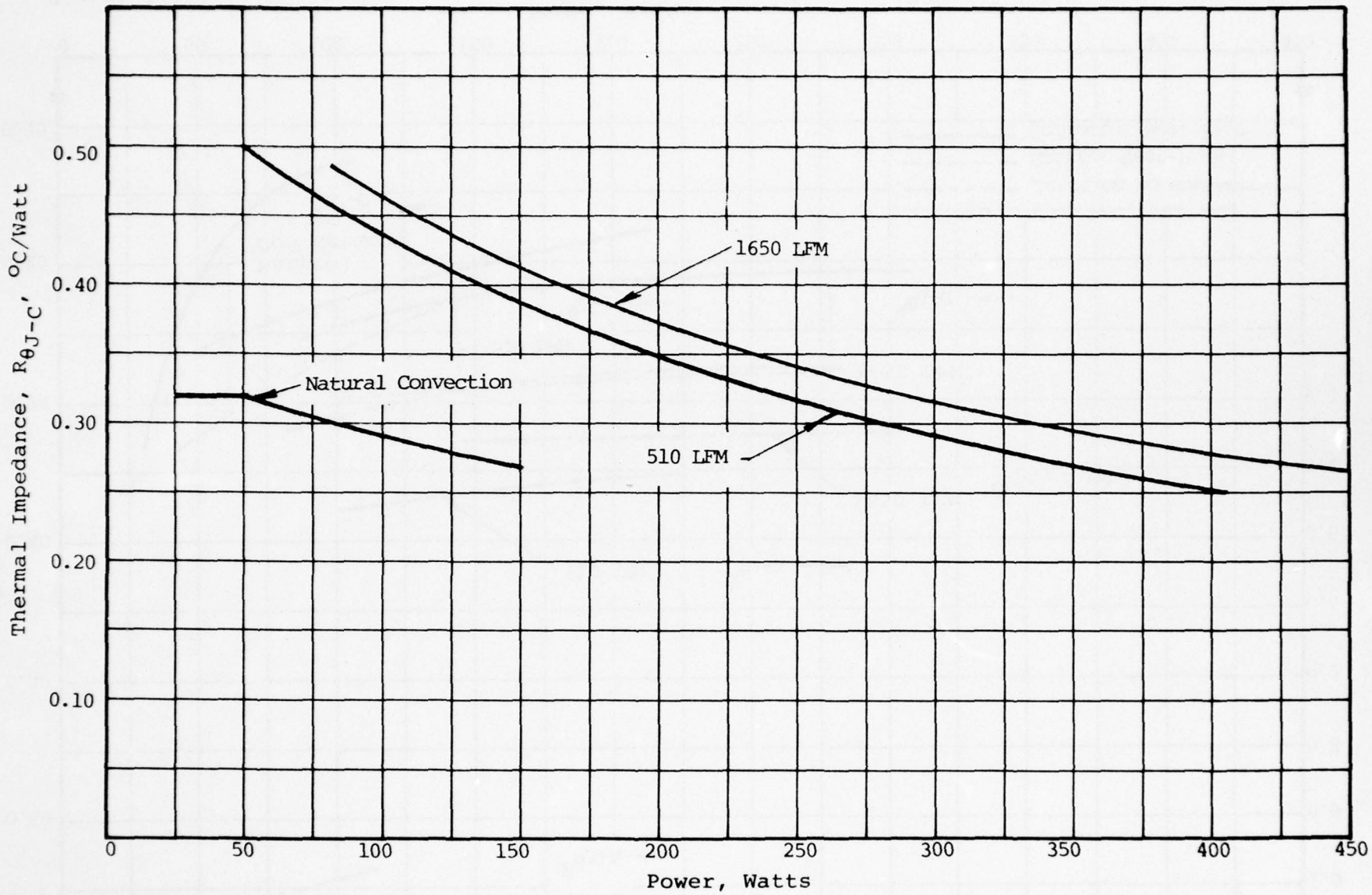


Fig. 39 Average Thermal Impedance between Junction and Base of Fins for Transcalent Transistor with 10, 4¼ inch Diameter Fins. Assembly made by Clamping.

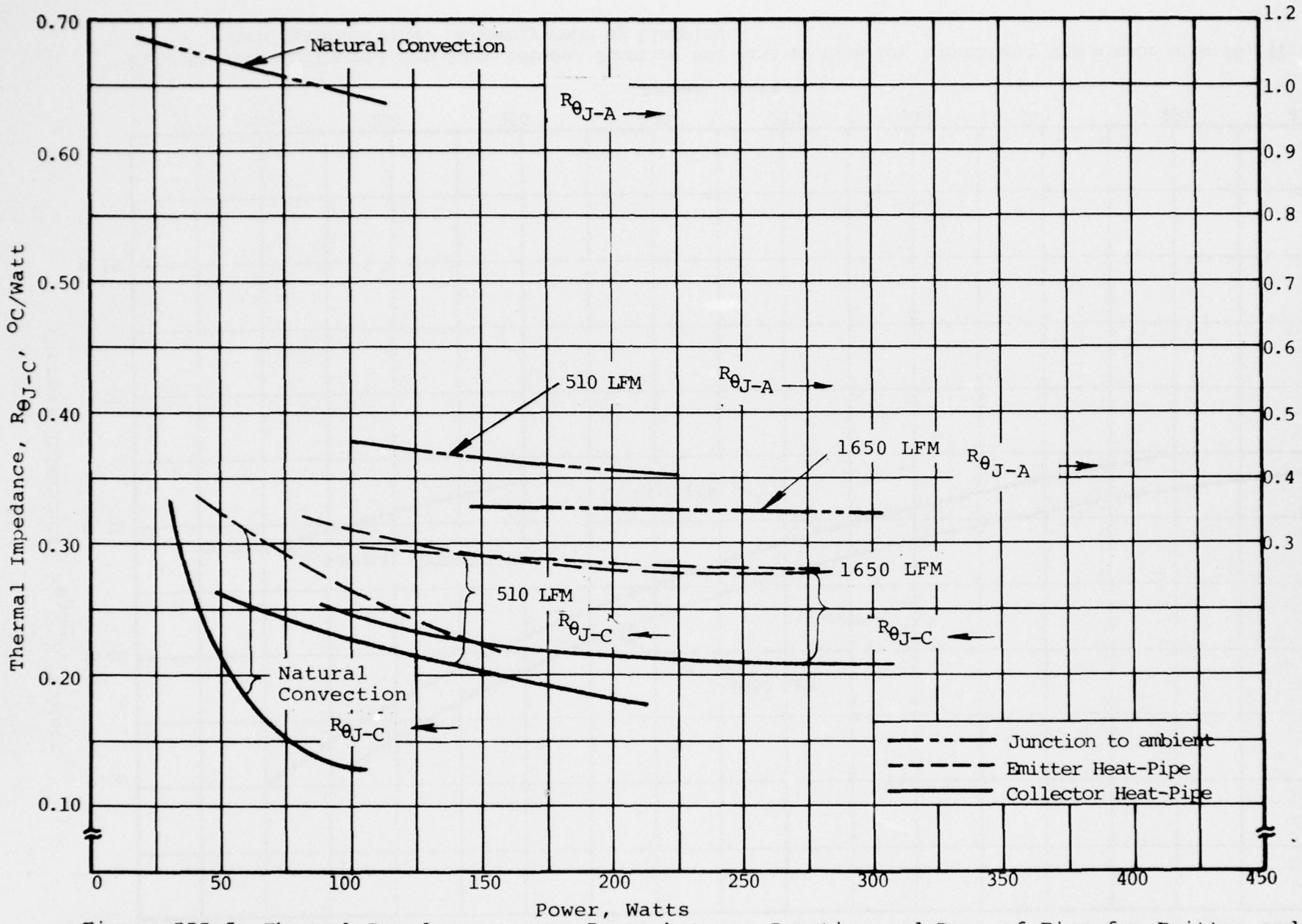


Figure III-5 Thermal Impedance versus Power between Junction and Base of Fins for Emitter and Collector Heat-Pipes with 10, 4¼ inch Diameter Fins. Assembly made by soldering the J15492 Transcalent Transistor.

Note that the thermal resistance decreases with increasing amounts of power. As the power being dissipated increases, there are more molecules of water being evaporated from the wick nearest the silicon, and in turn increasing the operating temperature and pressure of the heat-pipe. The asymtotic value of 0.25°C/watt is the thermal resistance through all of the solid materials and mechanical interfaces between the junction and external surface of the heat-pipe. In these experiments, in which the transistor wafer was not soldered to the collector heat-pipe, the two heat-pipes operated at nearly the same temperature.

Fig. 41 shows the rise in junction and case temperatures versus the power dissipated. It should be noted that while a Transcalent transistor thermal impedance exhibits a negative slope with increasing power that the temperatures used in computing the thermal resistance values are always rising with increasing increments of power.

In Fig. 40 is a summary of the thermal impedance results for devices No. 55 and 56 which were assembled by soldering the transistor wafer to the collector heat-pipe. There are several noticeable differences from the results discussed in the preceding paragraph. The heat-pipes do not operate at the same temperature and, therefore, the thermal impedances of the emitter and collector heat-pipes are different. The thermal impedance of the soldered joint to the collector heat-pipe is less than the mechanical joint to the emitter heat-pipe. In fact, the thermal impedance of the emitter heat is nearly the same as that reported for a clamped assembly, Fig. 39 . The slope of the thermal resistance curve for the emitter heat-pipe is not as great as that in Fig. 39 because it is in parallel with the collector heat-pipe whose thermal resistance has been markedly improved. The thermal resistance for the transistor is, therefore, the average curve for the two heat-pipes in parallel. In the upper half of Fig. 40 are plotted the thermal impedances between the junction and the ambient air at 25°C with three different air velocities.

A theoretical estimate of thermal impedance was calculated assuming that all of the heat was generated in the center of the transistor wafer. The cross-sectional area for heat flowing from the transistor wafer to the emitter heat-pipe was chosen as the emitter area of 1.064 cm^2. The cross-sectional area for the heat flowing through the ballast wafer was assumed to be twice the emitter area. On the collector side of the transistor wafer, the area for heat transfer was assumed to be just the area beneath the emitter diameter. The actual areas were used to calculate the heat transfer through all other parts of the assembly. The thicknesses and temperature gradients through each part are summarized in Table 9.

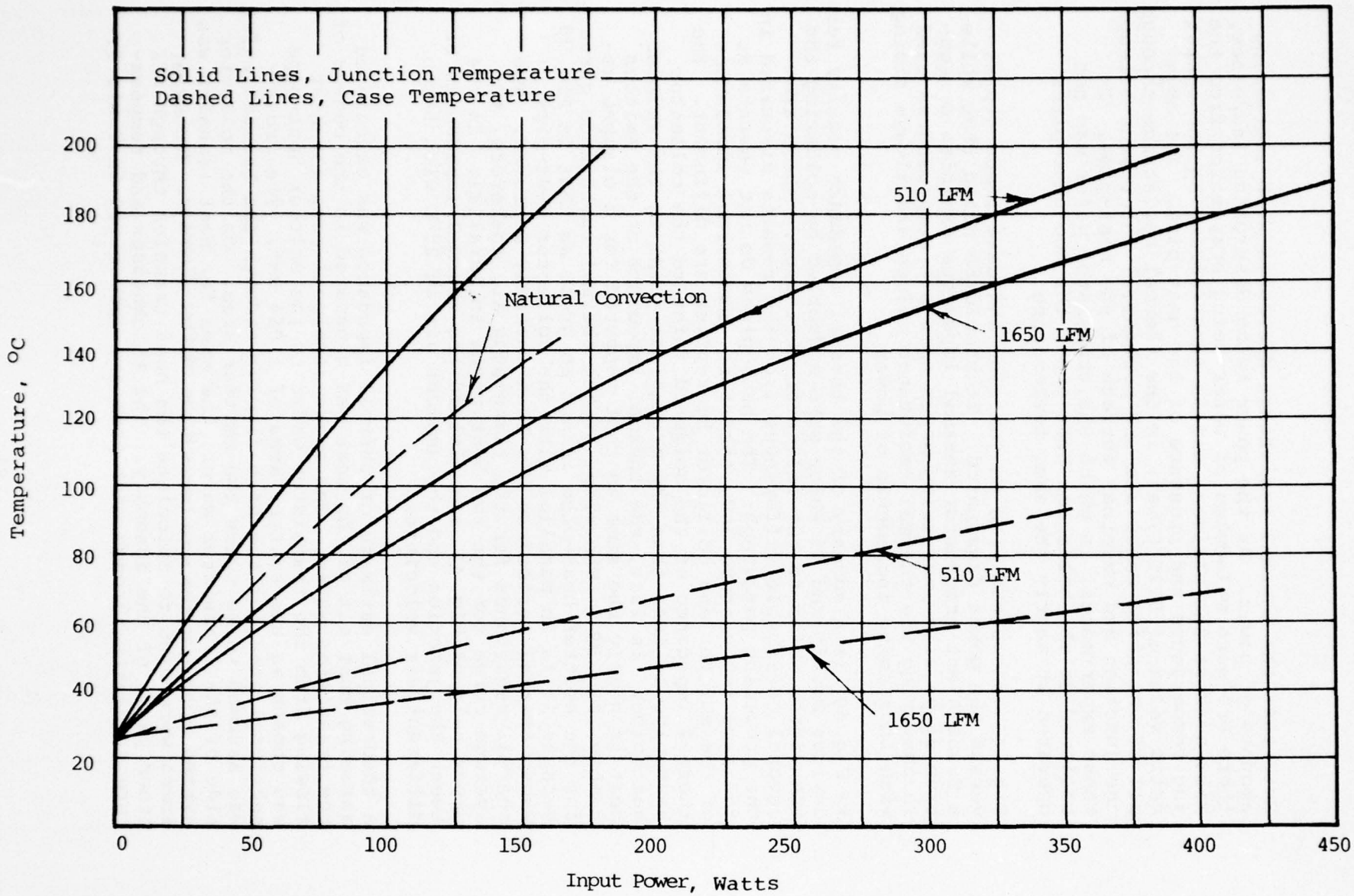


Fig. 41 Temperature Rise of Junction and Case versus Power for Transcalent Transistor with 10 4¼ inch Diameter Fins and Clamped Assembly

Thicknesses and Temperature Gradient through Each Material of Construction

TABLE 9

Part Description	Emitter Side		Collector Side	
	Thickness	Temp. Grad.	Thickness	Temp. Grad.
Center of transistor to emitter or collector	3.5×10^{-3} in.	$3.12 \times 10^{-3} Q_E$	3.5×10^{-3} in.	$3.12 \times 10^{-3} Q_C$
Tungsten metallizing	5.9×10^{-5}	$8.44 \times 10^{-5} Q_E$	5.9×10^{-5}	$2.7 \times 10^{-5} Q_C$
Nickel metallizing	5.9×10^{-5}	$1.53 \times 10^{-4} Q_E$	5.9×10^{-5}	$4.9 \times 10^{-5} Q_C$
Gold metallizing	5×10^{-4}	$4.03 \times 10^{-4} Q_E$		
Nickel metallizing	5.9×10^{-5}	$1.53 \times 10^{-4} Q_E$		
Tungsten metallizing	5.9×10^{-4}	$8.44 \times 10^{-5} Q_E$		
Mesa fingers	1.5×10^{-3}	$4.18 \times 10^{-3} Q_E$		
Ballast	4.5×10^{-3}	$6.27 \times 10^{-3} Q_E$		
Tungsten metallizing	5.9×10^{-5}	$2.77 \times 10^{-5} Q_E$		
Nickel metallizing	5.9×10^{-5}	$5.02 \times 10^{-5} Q_E$		
Molybdenum disc	5×10^{-2}	$2.16 \times 10^{-2} Q_E$	3×10^{-2}	$1.3 \times 10^{-2} Q_C$
Solder			5×10^{-4}	$1.14 \times 10^{-3} Q_C$
Moly disc				
Wick evaporator	5×10^{-2}	$2.08 \times 10^{-2} Q_E$	5×10^{-2}	$2.08 \times 10^{-2} Q_C$
Wick condenser	4.2×10^{-2}	$4 \times 10^{-4} Q_E$	4.2×10^{-2}	$4.0 \times 10^{-4} Q_C$
Wall	6.2×10^{-2}	$2.0 \times 10^{-4} Q_E$	6.2×10^{-2}	$2.0 \times 10^{-4} Q_C$

If the center plane of the transistor wafer is a dividing plane for heat being dissipated to the collector and emitter heat-pipes; then it can be assumed that the temperature gradients are equal from the center of the transistor to the evaporating surfaces in the heat-pipes

$$\Delta T_E = \frac{\ell}{KA} Q_E = {}^{\Delta}T_C = \frac{\ell}{KA} Q_E$$

$$\text{or } 0.0569\ Q_E = 0.371\ Q_C$$

where Q_E and Q_C are the amounts of heat flowing to each heat-pipe, respectively, and ℓ/KA coefficient is characteristic of each material. K is the material's thermal conductivity, and A is the cross-sectional area and ℓ is the distance through which the heat flows. Each material and its coefficients are tabulated in Table 9. The numerical coefficients, 0.0569 and 0.371 are the summation of the coefficients from the center of the transistor to the evaporation of either the emitter or collector heat-pipe.

If the total heat generated is Q,

$$Q = Q_E + Q_C.$$

By solving the temperature gradient equation for Q_C;

$$Q_C = \frac{0.0569}{0.0371} Q_E = 1.53\ Q_E$$

and by substitution,

$$Q_E = 0.39\ Q \text{ Watts}$$

$$Q_C = 0.61\ Q \text{ Watts}$$

Thus, the heat flow is divided 61 percent to the collector heat-pipe and 39 percent to the emitter heat-pipe. Using this calculated division of heat, the impedance between the junction to the evaporating surface of the heat-pipes is, as follows:

$$R_{\theta_E} = \frac{0.0569\ Q_E}{Q_E}$$

$$R_{\theta_C} = \frac{0.0371\ Q_C}{Q_C}$$

For these calculations, it was assumed that the thermal conductivity of the wick was $1/k = 0.276^{o}C/in.\left(\frac{watt}{in^2}\right)$ #

When these results are compared to measured values, the actual thermal resistance is greater than that predicted. The reasons are the uncertainty in the conductivity of the wick and the difficulty of measuring a surface temperature without embedding the thermocouple into it. When the ratios of the calculated emitter-to-collector thermal impedance, $\frac{0.0371}{0.0569} = 0.65$, is compared to the measured, $\frac{0.15}{0.24} = 0.625$, there is closer agreement.

In Figures 41 and 42 curves are shown depicting the temperature rise of the junction and heat-pipes for two of the kinds of assemblies which have been discussed. The data is at three different cooling air flows. From these curves, it should be noted that the transistor and the heat-pipes get hotter with increasing amounts of power even though the thermal resistance of the device is decreasing. The limiting factor is the highest junction temperature allowable for the application. Allowance for overload conditions and reliability factor are two parameters which must also be considered in selecting an operating junction temperature.

In Fig. 43 is plotted the temperature rise of a transistor made with aluminum pin fins attached to the heat-pipes and cooled with air in the velocity range of 4000 to 5000 LFM. The temperature rise is similar to the transistors made with 4¼ inches diameter fins cooled with air moving at 1650 LFM. A squirrel cage fan with a 1/3 hp motor was needed to cool the transistor at 4000 LFM. The thermal impedance of the transistor with aluminum pin fins was not measured because the devices were shipped under the contract before the thermal impedance circuit was constructed.

Transcalent transistors were constructed with aluminum pin fins because the high temperature brazing techniques making use of Wolverine fin tubing had not yet been developed. The Wolverine fin tubing contains phosphorus which volatilizes rapidly forming voids in the joint when alloyed with high melting point braze materials.

Brazes made in this manner using the Wolverine tubing were not vacuum-tight. The use of aluminum pin fins that were cemented onto the heat-pipes using a heat transfer epoxy proved to be a successful substitution.

#In Report No. 2, Development of a 250 Ampere Transcalent Rectifier, Contract DAAK02-69-C-0609, it was shown that the ΔT through the vapor was $0.035^{o}C$. A formula for estimating the thermal conductivity of the wick was also shown.

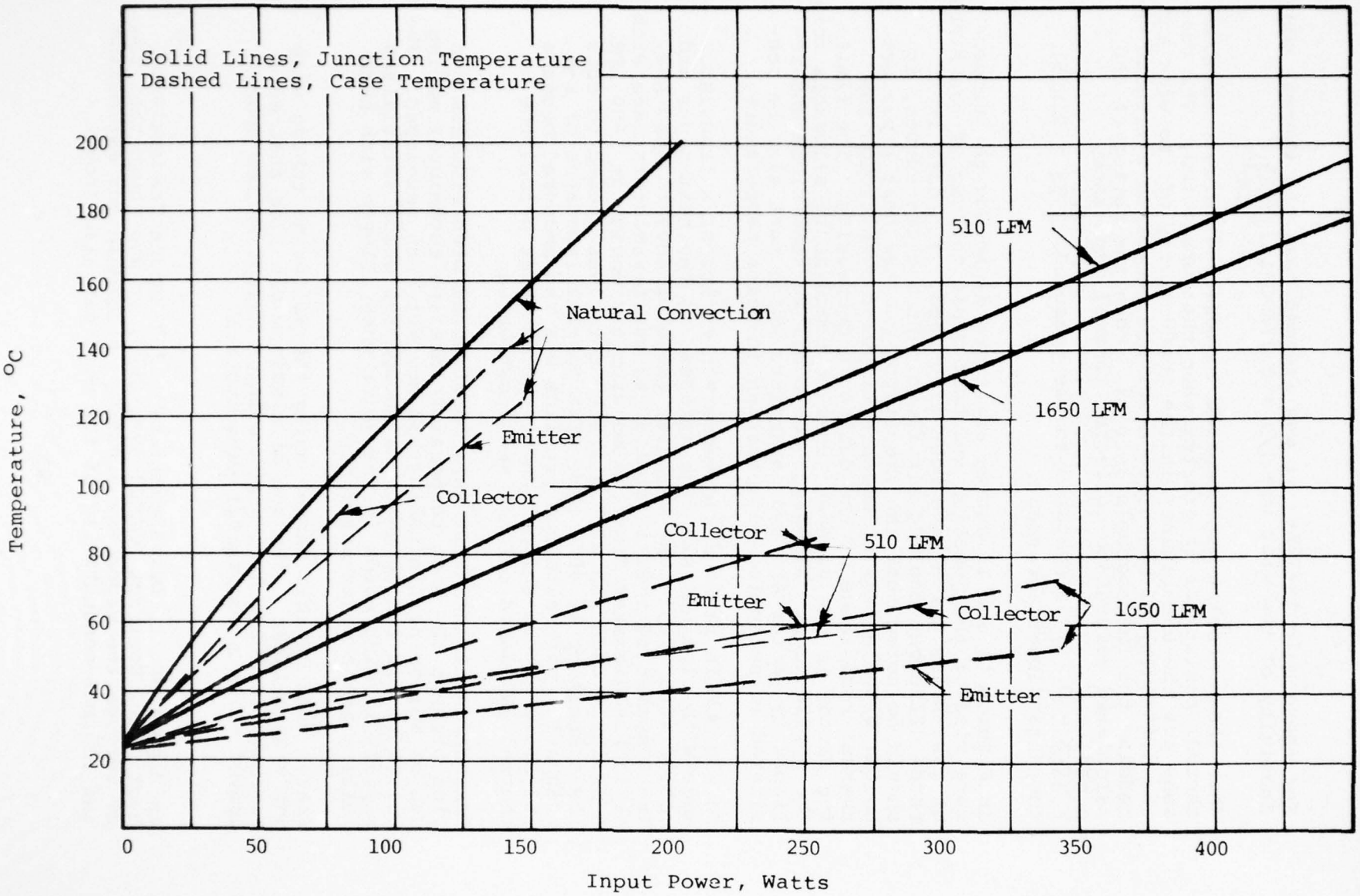


Fig. 42 Temperature Rise of Junction and Case versus Power for Transcalent Transistors with 10, 4¼ inch Diameter Fins. Assembly made by Soldering.

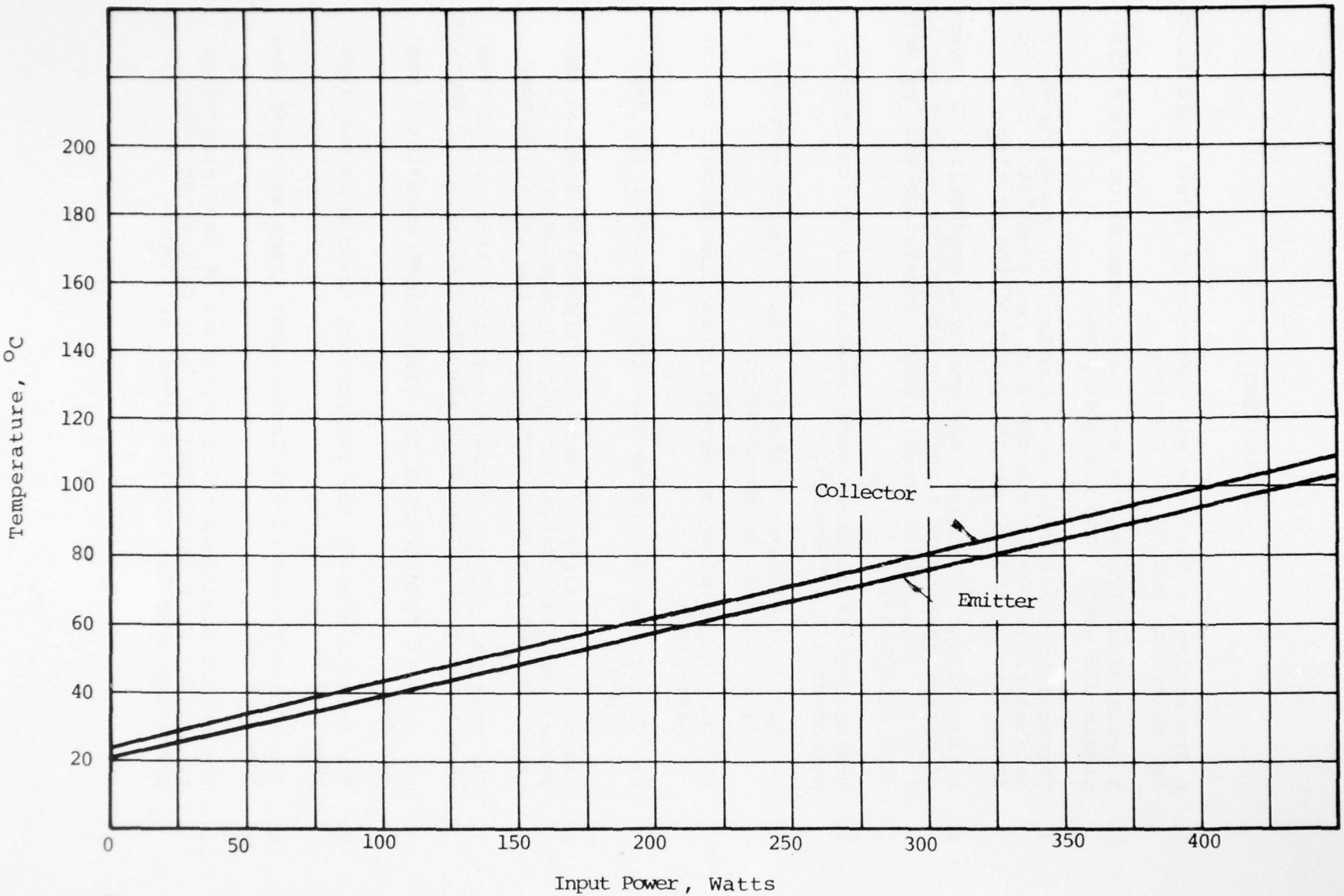


Fig. 43 Heat-Pipe Temperature versus Power for Transistor with Aluminum Pin Fins, Air Velocity 4000 LFM

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DEVELOPMENT OF A HIGH VOLTAGE AND HIGH CURRENT TRANSCALENT TRAN--ETC(U)
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CONCLUSIONS

1. A Transcalent transistor was constructed which could block 860 volts and switch 150 amperes.

2. A Transcalent transistor was constructed which could dissipate 523 watts from the heat-pipes.

3. Transcalent transistors were constructed employing silicon ballast resistors in contact with the transistor chip to force current sharing to all parts of the emitter.

4. A Transcalent transistor was operated conducting 72 amperes of direct current at a collector-to-emitter voltage of 7 volts. Variations of gain with temperature and V_{CE} were also determined.

5. Transcalent transistors were constructed employing three different fin structures.

   a) Two inch diameter Wolverine fins - copper extruded fins integral to the heat-pipe.

   b) Two inches diameter aluminum pin fins epoxied to the heat-pipes.

   c) Copper fins 4¼ inches diameter epoxied to the heat-pipes.

6. Transcalent transistors were constructed by loading the ballast and the transistor chip in compression while using the ceramic/metal envelope as the tension member.

7. The peak gain of the Transcalent transistor ranged from 26.6 to 42.8 at currents in the range of 10 to 15 amperes.

8. The cut-off frequency of the Transcalent Transistor was 230 KHz.

9. The turn-on time of the Transcalent transistor was less than 1.0 μs.

10. The turn-off time of the Transcalent transistor was less than 2.0 μs.

11. The second breakdown characteristics of the Transcalent transistor were determined to fully define the safe-operating-area for the transistor at 25°C.

12. The Transcalent transistor was operated in a resistive load circuit switching 60 amperes at 400 volts and at 5 KHz. In another test a Transcalent transistor was operated at 30 amperes and 20 KHz.

13. A Transient computerized thermal analysis was made by the C.O.T.R. between the junction of the transistor and the evaporator of the heat-pipe for a number of operating conditions.

14. The thermal impedance of the Transcalent transistor was determined and is a function of the power being dissipated and the air velocity cooling the device. Typical asymptotic values were:

$R_{\theta J-C} = 0.20^{o}C/W$	$R_{\theta J-A} = 0.99^{o}C/W$;	100 W natural convection
$R_{\theta J-C} = 0.23$	$R_{\theta J-A} = 0.41$	200 W 510 LFM
$R_{\theta J-C} = 0.25$	$R_{\theta J-A} = 0.35$	275 W 1650 LFM

Sixty-one percent of the thermal energy is dissipated by the collector heat-pipe. Soldering the transistor chip to the collector heat-pipe improved the heat transfer from the silicon to the heat-pipe.

15. The base drive current distribution to all parts of the transistor chip is improved by soldering a metal ring onto the base contact area of the wafer.

16. The saturation voltage is only 0.8 volts at 60 amperes even with the ballast resistor in series with the emitter.

17. A vertical ballast resistor was selected as the most practical ballasting structure for the Transcalent transistor. The resistor has a positive coefficient of electrical resistance with increasing temperature.

18. Two Transcalent transistors were fabricated using high resistivity silicon crystal 70 ohm-cm for the starting wafers. The units exhibited blocking voltages greater than 1000 volts. The current capability of the devices was only half that of devices made with lower resistivity crystal, 40 ohm-cm.

RECOMMENDATIONS

1. An improved base lead through the ceramic is needed. In switching applications, it is desirable to drive the base with enough current to insure that the transistor is in full saturation. When the transistor is saturated, there is a minimum of thermal dissipation.

   Base drive currents would need to be in the range of 30 to 40 amperes to reach saturation at a collector current of 100-150 amperes. The small kovar pin used in the package designed for the contract can only be operated at 30 amperes pulsed or 14 amperes d.c.

2. The base connection inside the package should be redesigned to be as a mechanical contact which is made while assembling the device.

3. Additional electrical testing is needed with emphasis applied to more elevated temperature tests. Leakage current, gain curves, and the safe operating area must be determined at the anticipated junction operating temperatures.

4. More environmental testing is needed. The assembly of the Transcalent transistor differs somewhat from other Transcalent devices in that there are internal mechanical interfaces prestressed in compression. It is not known how these interfaces will behave in shock and vibration, thermal cycling and under other environmental stresses.

5. Assembly techniques must be improved to make the Transcalent transistor economical to manufacture in volume. Alignment of the ballast and transistor wafers is a labor-intensive process.

6. A larger Transcalent transistor should be designed. Transcalent devices do not have the same design limitation as devices which are clamped between solid heat sinks. In designing a larger device clamped between heat sinks, consideration must be given to the longer heat transfer path from the center of the silicon chip to the surfaces of the heat sink. The operating temperature of the heat sink is fixed by the maximum junction temperature, the conductivity of the heat sink and the length of the heat transfer path. For this reason, larger clamped devices are designed at a lower current density. However, the Transcalent devices do not have to be designed to a lower current density when they are scaled larger because the center area of the chip is cooled by the heat-pipe as effectively as the area near the edge of the chip.

7. The reverse bias second breakdown $E_{s/b}$ of the Transcalent transistor must be evaluated.

8. The Transcalent transistor should be tested in an inductive switching circuit. Inductive circuits create the most severe service conditions because the transistor must conduct the inductive current while the transistor is switching to its blocking mode. As blocking occurs, the decaying currents will induce large voltage transients close to the rating of the transistor. Snubber circuits should also be considered to minimize the switching losses.

9. Simplified construction methods must be considered at all phases of fabrication such as metallizing, diffusing the ballast resistor and assembly.

10. Life testing of the Transcalent transistor must be done.

11. The design of other Transcalent devices must be considered such as the Darlington transistor, power field effect transistor, the gate turn-off thyristors and the asymmetrical SCR. The characteristics of all of these devices mentioned would benefit from the lower thermal impedance provided by the Transcalent package.

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