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Research and Development on Advanced Silicon Carbide Thin Film Growth Techniques and Fabrication of High Power and Microwave Frequency Silicon Carbide-Based Device Structures

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13. ABSTRACT (Maximum 200 words)

Thin films of pure and Al-doped β-SiC have been grown on 4° off-axis Si(100) and c-axis oriented α(6H)-SiC in the temperature range of 1025–1250°C using gas-source molecular-beam epitaxy. Cross-sectional TEM confirmed the epitaxial relationship between the films and the substrates. Double positioning boundaries have not been observed in the material grown on the 6H-SiC substrates. Platinum and Ti circular contacts were epitaxially deposited on α(6H)-SiC via electron beam MBE at room temperature. Leakage currents at $-10V$ were as low as 5×10^{-18} A/cm^2. The ideality factors were approximately unity. Barrier heights for the as-grown Ti and Pt contacts were determined from C-V measurements to be 0.88 eV and 1.02 eV, respectively. Theoretical investigations of the physical limitations to the RF operation of SiC IMPATT diodes has shown that good RF output power can be obtained from these devices. However, the low magnitude of the charge carrier mobility in SiC limits the magnitude of the RF voltage that can be supported, and thereby prevents efficient dc to RF power conversion. MESFETs have been fabricated with values of f_t and f_{max} of 4.5 GHz and 3.0 GHz, respectively. The measured DC power density was extremely high with a value of 12.4 W/mm. Solutions to the problems of parasitics from source and gate resistances are described.

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I. Growth and Characterization of β-SiC Films Grown on Si by Gas-Source Molecular Beam Epitaxy*

L. B. Rowland, S. Tanaka, R. S. Kern, and R. F. Davis

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Abstract. Films of β-SiC have been grown on 4° off-axis Si (100) substrates from 1198 to 1398 K by gas-source MBE using Si_2H_6 and C_2H_4. Monocrystalline films were obtained at temperatures as low as 1248 K, as confirmed by electron diffraction. The latter films were specularly reflective. However, SEM revealed growth pits extending to the SiC surface as well as preferential growth on the pit edges. Cross-sectional TEM analysis confirmed the epitaxial relationship between the film and the Si substrate. Misfit dislocations and microtwins were also observed.

1. Introduction

At present, economics and availability make Si and a two-step chemical vapor deposition (CVD) the most commonly used substrate and process route for the growth of SiC films. However, mismatches in lattice parameters and coefficients of thermal expansion of 20% and 8%, respectively, exist between the two materials. The CVD process involves the reaction of the Si substrate surface with a C-containing gaseous species to form a "converted" layer of β-SiC [1] prior to subsequent deposition of the β-SiC film using both C- and Si-containing precursors.

However, the high growth temperatures and level of control of growth parameters and doping species obtained with CVD have sparked interest in the technique of gas-source molecular beam epitaxy (GSMBE) for growth of SiC [2-4]. The latter technique allows for precise control of growth parameters and minimization of sample contamination during deposition and was used in the studies described below. Experiments were conducted to determine the feasibility of SiC growth directly on Si (100) and to offer a comparison to films to be grown on converted layers in the near future. Effects of the C_2H_4/Si_2H_6 ratio and growth temperature on film morphology and quality were examined.
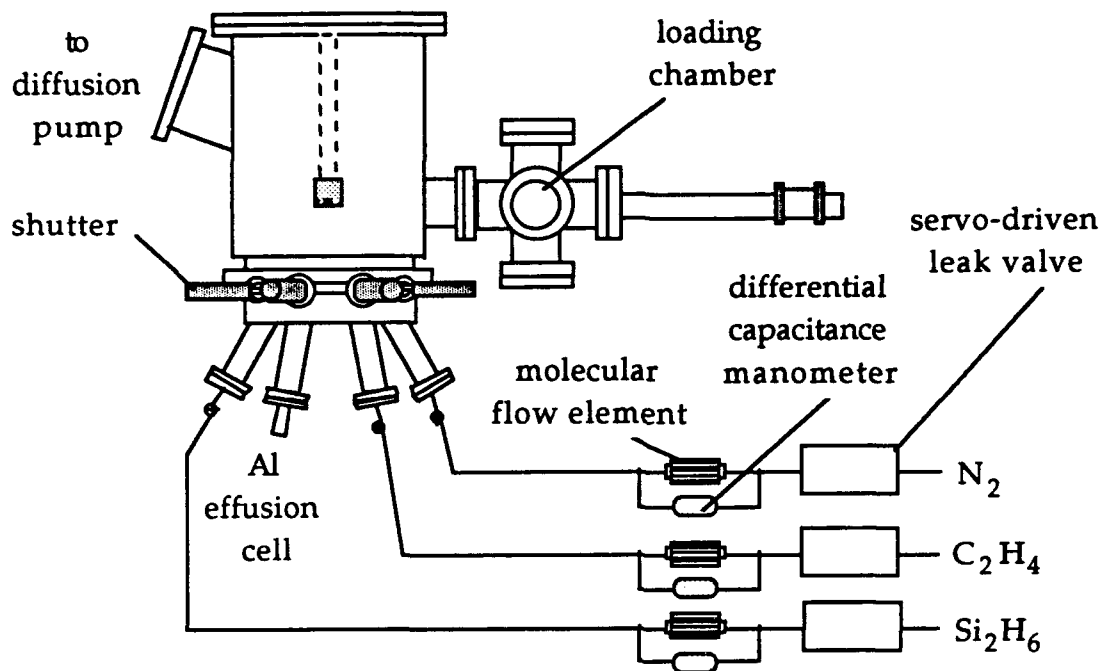

Figure 1. Schematic of molecular beam epitaxy apparatus

2. Experimental Procedures

Growth experiments were conducted using Si substrates primarily cut 4° off (100) toward the [011] direction. The use of off-axis substrates eliminates inversion domain boundaries (IDB's) [5,6]. The chemically cleaned (5 min H_2SO_4 (60°C), 1 min DI rinse, 5 min 1:1 H_2O_2/NH_4OH (60°C), 1 min DI rinse, 5 min BOE, 1 min DIrinse) substrates were introduced into the growth chamber shown in Figure 1 (6 x 10^{-10} torr base pressure) through a load lock (5 x 10^{-8} torr base pressure) and resistively heated for 180 s at the growth temperature to desorb the native oxide layer. The heating assembly consisted of a tungsten wire coil surrounded by a SiC-coated graphite shell. Layers of W and Mo heat shielding were placed on the inside of this shell to reflect heat onto the backside of the sample. This heater is capable of long-term operation at constant temperatures (±3°C) to 1600 K, as measured with an infrared thermometer.

The introduction of ethylene and disilane (both 99.99% purity) into the growth chamber were controlled by a differential pressure transducer which measured the pressure drop across a flow element of essentially constant conductance [7,8]. The pressure drop across the element, ΔP, and the conductance of the element, C, were then converted to flow rate, Q, using the relation $Q = C\Delta P$. A servo-driven leak valve was used to stabilize the flow at the desired level via a feedback loop. In this manner the flow rate of a gaseous species (and
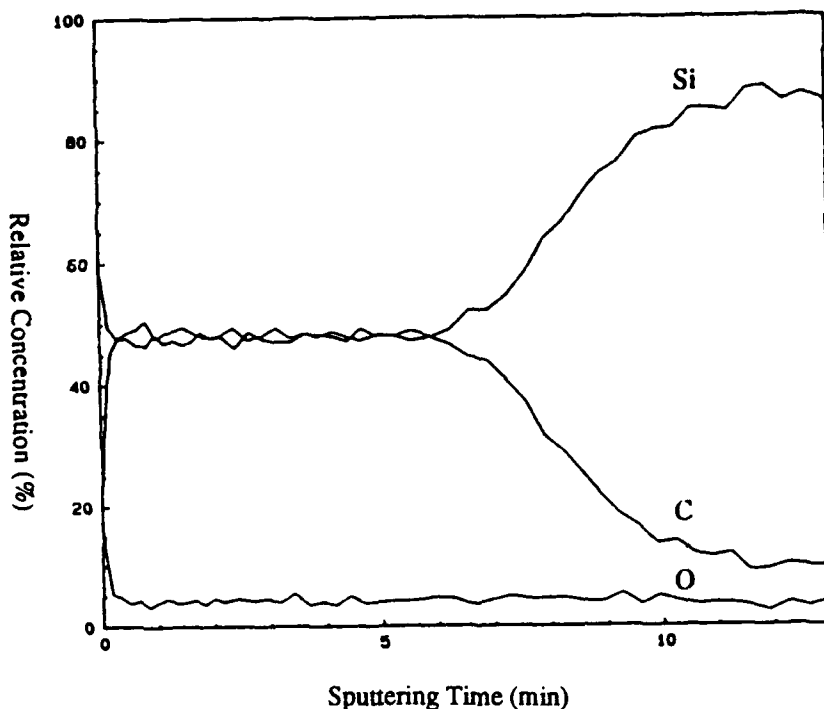
Figure 2. Auger depth profile of sample grown at 1075°C

consequently species flux) were known and controlled at flow rates substantially less than 1 sccm.

Growth conditions used in this study were as follows: temperature, 1298-1498 K; pressure, 4-6 x 10^{-5} torr; Si_2H_6 flow rate, 0.40-2.0 sccm; C_2H_4 flow rate, 2.0 sccm; and time, 90 min. The resulting films were 30-50 nm in thickness. The chemical composition and depth profile of each sample were obtained using a scanning Auger microprobe. Samples which showed a 1:1 Si to C ratio from the Auger results were examined using an optical microscope and a field-emission scanning electron microscope (SEM) to observe surface morphology. Reflection high-energy electron diffraction (RHEED) was used after growth was completed to determine the crystalline quality of the SiC surface. Cross-sectional transmission electron microscopy (XTEM) also was employed to analyze representative β-SiC films. XTEM sample preparation procedures were similar to those used in Ref. 9.

3. Results and Discussion

Auger spectra from the surface of each sample showed the presence of an oxide from atmospheric exposure between growth and analysis. However, the underlying films in most samples were stoichiometric SiC. Figure 2 shows the Auger depth profile adjusted for differences in Auger yield of Si and C from a sample grown directly on off-axis (100) Si at 1298 K using 2.0 sccm C_2H_4 and 0.4

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a) 1075°C, C/Si: 5:1   b) 975°C, C/Si: 2:1

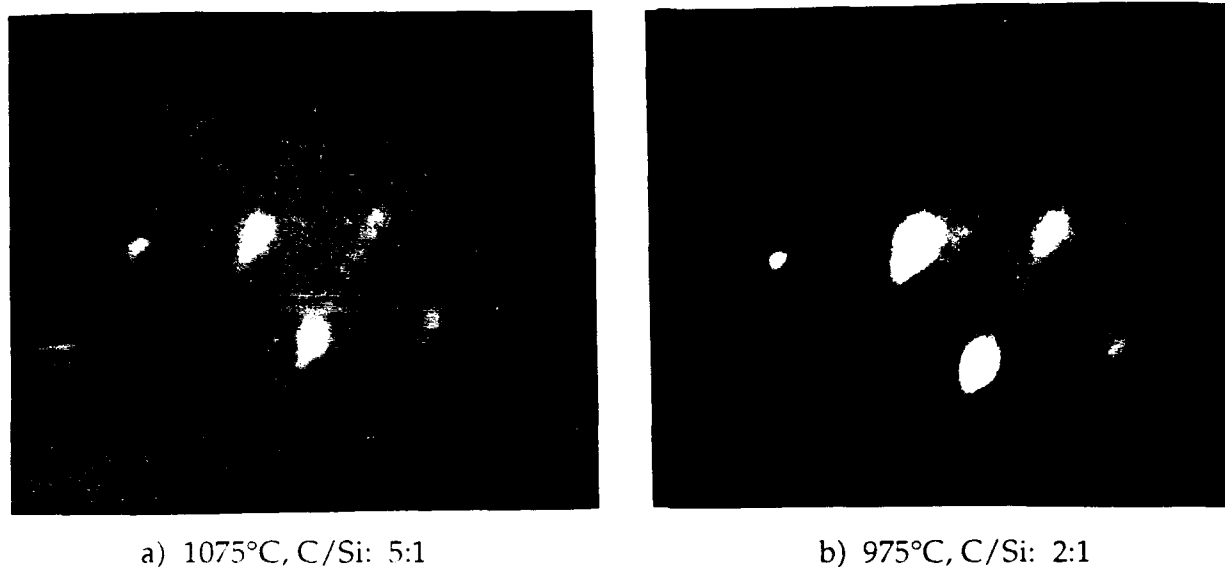Figure 3. RHEED of β-SiC films on Si (100) substrates

sccm Si$_2$H$_6$ for 90 min. The results indicate essentially a 1:1 SiC ratio. The oxygen profile within the film is representative of the background level for this Auger system. A monocrystalline β-SiC film previously grown in our laboratory on (100) Si using CVD showed a depth profile nearly identical to that found in the SiC film shown in the figure. Figure 3(a) shows the RHEED pattern ([110] beam azimuth) of the same sample used to obtain the Auger profile of Fig. 2. The RHEED pattern of a sample grown for 90 min on off-axis (100) Si at 1248 K with 2.0 sccm C$_2$H$_4$ and 1.0 sccm Si$_2$H$_6$ is shown in Fig 3(b). Both samples were monocrystalline β-SiC and were of similar crystalline quality. Twin spots were detected in the RHEED micrographs.

Auger results indicated that only certain C$_2$H$_4$:Si$_2$H$_6$ flow ratio and temperature combinations resulted in growth of single phase SiC. For example, Si-rich films were obtained for 2.0 sccm C$_2$H$_4$ and 0.4 sccm Si$_2$H$_6$ at 1248 K and at 1348 K. However, at 1298 K, the film grown using these flow rates was stoichiometric SiC. Films grown using 2.0 sccm C$_2$H$_4$ and 2.0 sccm Si$_2$H$_6$ were also Si-rich at 1348 K, but were stoichometric at 1298 and 1248 K. Films grown using 2.0 sccm C$_2$H$_4$ and 1.0 sccm Si$_2$H$_6$ were nominally 1:1 SiC over the entire temperature range investigated. The reasons for these variations are being studied.

Films which were monocrystalline SiC appeared smooth to the naked eye and had a yellowish tinge. Figure 4 is an SEM micrograph of the surface of a sample grown at 1298 K using 2.0 sccm C$_2$H$_4$ and 0.4 sccm Si$_2$H$_6$. At this
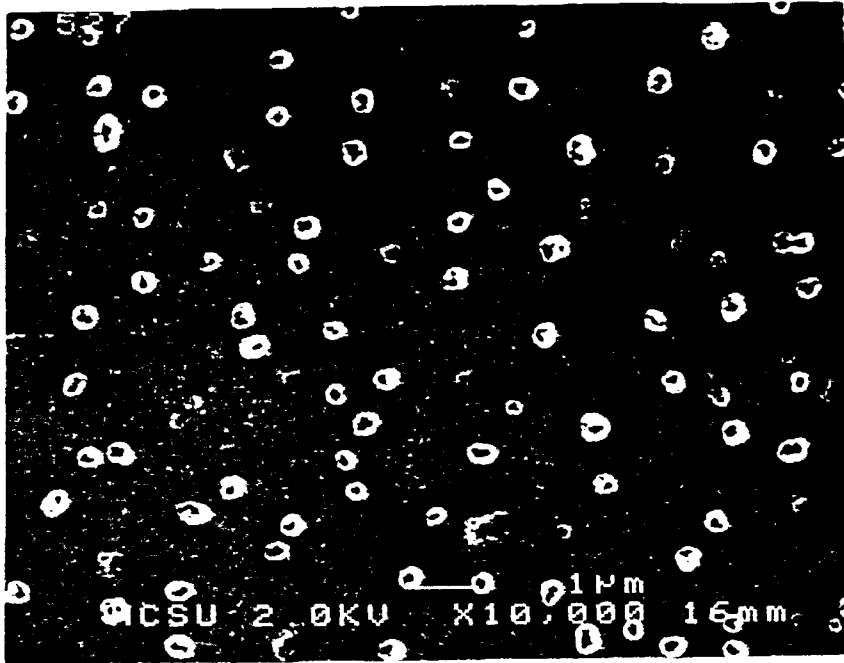
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Figure 4. SEM micrograph of β-SiC grown at 1075°C showing preferential growth on pitted regions

resolution, the surface continued to appear fairly smooth except for the presence of pitted regions on the SiC surface. Many of these pits, which are believed to be pyramidal and bounded by {111} planes [10], have preferential growth on their edges. Similar examination of other samples with differing gas source ratios and temperatures provided evidence that growth on the pit edges eventually converges above the center of the pit, forming a hillock above each pit [11].

Transmission electron microscopy (TEM) was used to evaluate the structural quality of the films. Figure 5 shows a high-resolution cross-sectional micrograph and corresponding (110) electron diffraction patterns of both the β-SiC film grown at 1298 K for 90 min and the Si substrate. Both the SiC/Si interface and the SiC surface were fairly rough. The region at the substrate/film interface appears to be amorphous in the micrograph; this is believed to be caused by damage from the ion milling used as part of the TEM sample preparation procedure [1]. A high concentration of defects, namely [111] microtwins and misfit dislocations, are readily visible in the SiC film in the figure. An epitaxial relationship between the SiC film and the Si substrate can clearly be seen in the figure.

Growth thicknesses were estimated from Auger depth profiles and correlated with thicknesses obtained for samples examined using XTEM. The average values were 30-50 nm for 90 min of growth. Experiments designed to increase the SiC growth rate by changing source flow rates or using more reactive, carbon-bearing species are currently in progress.
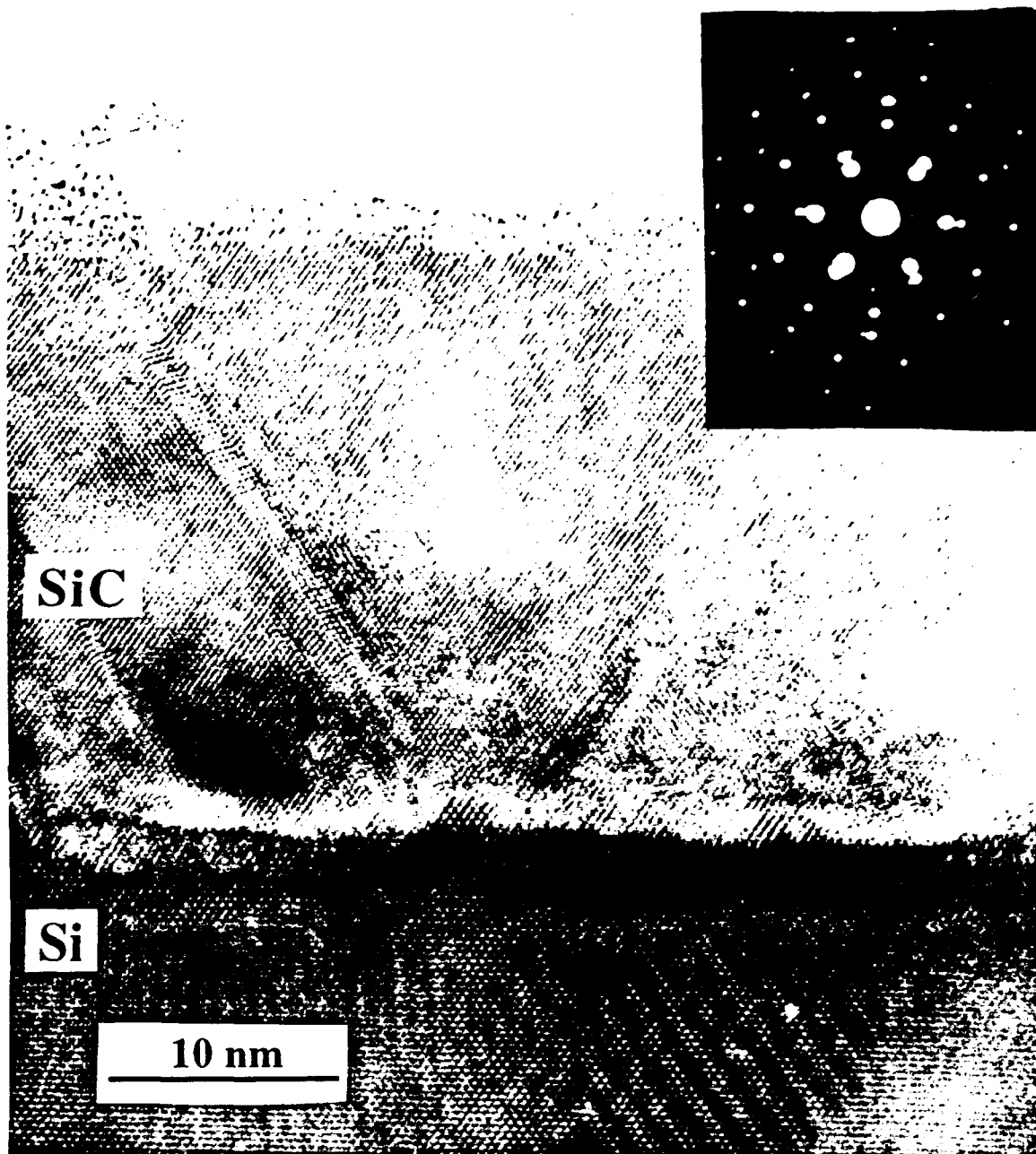
Figure 5: Cross-sectional TEM micrograph of SiC/Si sample grown at 1075°C with inset of selected area diffraction pattern of the SiC film and Si (100) substrate

4. Conclusions

Monocrystalline β-SiC films were grown by GSMBE on off-axis Si (100) substrates using Si_2H_6 and C_2H_4 at temperatures as low as 1248 K. This temperature is much lower than that typically used for SiC CVD growth. Films appeared smooth and specular to the naked eye, but {111} pyramidal growth pits were present on

the film surface. Preferential growth on the pit edges under certain growth conditions was also observed. Cross-sectional TEM analysis of selected SiC films showed the presence of [111] microtwins and visually confirmed the epitaxial relationship between the film and the Si substrate.

Acknowledgements

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II. Gas-Source Molecular Beam Epitaxy of Al-Doped β-SiC on 6H-SiC

A. Introduction

Beta SiC, the lone zincblende (cubic) polytype in the Si-C system, is a candidate material for use in specialized electronic applications because of its attractive physical and electronic properties. These characteristics include wide band gap (2.2 eV at 300K) [1], high breakdown electric field (2.5×10^6 V/cm) [2], high thermal conductivity (3.9 W/cm °C) [3], high melting point (3103K at 30 atm) [4], high saturated drift velocity (2×10^7 m/s) [5, 6], and small dielectric constant (9.7), such as 6H-SiC [7], β-SiC is preferable to hexagonal SiC for most device applications.

Most β-SiC thin film growth to date has been performed on Si substrates. Large-area, crack-free, and relatively thick (up to 30 μm) epitaxial β-SiC thin films have been grown on Si (100) by exposing the Si substrate to C-bearing gaseous species prior to further SiC growth [8-10]. However, these films exhibited large numbers of line and planar defects due to large lattice and thermal mismatches between SiC and Si. One particular type of planar defect, the inversion domain boundary (IDB), was eliminated with the use of Si (100) substrates cut 2°-4° toward [011] [11-13]. Growth on Si substrates has allowed understanding of the SiC growth processes and device development to occur, but the large thermal and lattice mismatches between SiC and Si hamper further development using Si substrates. As a result, considerable effort has been exerted to develop methods for growth of SiC single crystal substrates for homoepitaxial growth of SiC thin films.

Since the 1950's, monocrystalline single crystals of α(6H)-SiC have been formed using the Lely sublimation process [14]. However, since nucleation was uncontrolled using this process, material having a single polytype and uniform doping concentration was difficult. Alpha-SiC single crystals inadvertently formed during the industrial Acheson process have also been used as substrates for SiC growth. However, neither these crystals nor those formed using the Lely process are large enough for practical device applications. Recently, through the use of a seeded sublimation-growth process, boules of single polytype 6H-SiC of > 1 inch diameter with much higher quality than that obtained using the Lely process have been grown. The use of single crystals of the 6H polytype cut from these boules has given a significant boost to SiC device development.

The use of nominally on-axis α(6H)-SiC substrates has usually resulted in growth of β-SiC (111) films [15]. These films have typically had much lower defect densities than those grown on Si substrates. The major defects present in β-SiC/6H-SiC films have been double positioning boundaries (DPB) [16]. Despite the presence of DPBs, the resultant material was of sufficient quality to further device development of SiC. The use of off-axis 6H-SiC (0001)

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substrates has resulted in growth of high-quality monocrystalline 6H-SiC layers with very low defect densities [17].

In addition, the use of more advanced deposition techniques, such as molecular beam epitaxy (MBE), has been reported for SiC film deposition. The employment of this technique allows for the reduction in the growth temperature from the 1400-1500°C range which is used in CVD on 6H-SiC substrates. Silicon and C electron-beam sources have been used to epitaxially deposit SiC on 6H-SiC (0001) at a temperature of 1150°C [18]. Ion-beam deposition of epitaxial β-SiC on 6H-SiC has also been obtained at the temperature of 750°C using mass-separated ion beams of $^{30}Si^+$ and $^{13}C^+$ [19]. In order to reduce the temperature of deposition, decrease defect density, and improve electrical characteristics of doped and undoped SiC films, a gas-source molecular beam epitaxy (GSMBE) system has been designed, fabricated, and commissioned for this purpose at NCSU for the research in this contract. In this report, the preliminary results of the epitaxial growth and doping of β-SiC (111) films on 6H-SiC (0001) substrates using this system are presented.

B. Experimental Details

These films were grown on the Si face of 6H-SiC (0001) substrates provided by Cree Research, Inc. The substrates were nominally on-axis (± 1° off (0001)), as determined by X-ray diffraction using the Laue back-reflection method. Films were grown using the MBE/ALE system detailed in previous reports. Readers are referred to these reports for a description and schematics of the system. The material sources used include the gases of Si_2H_6 for silicon, C_2H_4 for carbon and solid Al for the p-type dopant. The last material was evaporated from a standard Knudsen-cell. The 6H-SiC substrates were chemically cleaned prior to growth using a BOE etch at room temperature for 5 min, followed by a DI water rinse for 2 min. This limited cleaning process was used to preserve a sputtered carbon layer present on the back of the wafer as an aid in temperature measurement.

In order to desorb hydrocarbon and oxide layers from the SiC surface, the sample was heated under vacuum to 1250°C for 5 min prior to growth. An Al-doped layer of β-SiC was formed by GSMBE on the converted layer using these conditions: Si_2H_6 flow, 0.5 sccm; C_2H_4 flow, 1.0 sccm; sample temperature, 1250°C; Al source temperature, 960°C; and time, 100 min. The system base pressure was less than 1×10^{-9} torr; pressures during the SiC GSMBE growth typically reached 3×10^{-5} torr.

The surface morphology of the resultant films was examined using optical microscopy and field-emission scanning electron microscopy (SEM). The change of atomic concentration of Al vs. depth was determined using secondary ion mass spectrometry (SIMS). A Cameca IMS-3f ion microprobe was used for this purpose. Mass-filtered O_2^+ at 50 keV was used as the primary ion with a beam raster size of 250 μm. The atomic concentration of Al at each point in

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the SIMS profile was obtained by multiplying a conversion factor by the value of the Al/Si count ratio at that point. The conversion factor was determined from the product of the Al/Si count ratio of an Al-implanted profile standard and the theoretically calculated atomic concentration at the peak of this standard. High-resolution transmission electron microscopy (HRTEM) was employed to determine the defects and crystalline structure present in the film as well as examining the film/interface region. An Akashi EM-002B HRTEM was used for this purpose.

C. Results

An SEM micrograph of a heavily Al-doped film grown on SiC (0001) is shown in Figure 1. The surface of the film is fairly smooth, though the existence of small platelets on the surface can be seen as areas of lighter contrast in the micrograph. In the research reported by other investigators [15], optical microscopy normally has revealed a mosaic structure consisting of what appeared to be steps and ledges on the β-SiC film on the α-SiC substrate. However, an examination of the film grown in the present research using Nomarski optical microscopy found only occasional areas with this mosaic pattern. The steps and ledges typically seen result from double positioning boundaries, which result when two adjacent β-SiC (111) nuclei form rotated 60° to each other about the <111> axis [16]. Over the bulk of this film, very few of these DPBs could be found using Nomarski optical microscopy or SEM. It is unclear whether the lack of appearance of DPBs is due to the fact that the film is quite thin (100 nm) or that the nuclei are very small, or the presence of Al has a positive effect or that low temperature MBE growth is effective in eliminating these defects. Plan view TEM and X-ray topography has been used in the past to elucidate these defects, and these techniques will be attempted to determine the presence of DPBs.

A plot of Al atomic concentration vs. depth for this sample is shown in Figure 2. The substrate should have a much lower concentration of Al than the film which was intentionally heavily doped. The peak concentration of Al is high (5×10^{20} cm^{-3}). However, the Al concentration drops rapidly with depth. It is believed that the small hump seen at a sample depth of about 100 nm denotes the interface between the β-SiC film and the 6H-SiC substrate. There should be some small amount of strain at this interface (even though the substrate and film are both SiC). This strain is primarily due to the different doping levels and impurity concentrations of the film from the substrate, and also the different crystal structures of the two SiC polytypes. This interfacial strain energy, though small, would enable the formation of lower-energy sites for impurity species such as Al. This decrease in lattice strain energy resulting from the incorporation of Al near the interface would encourage migration of this species to the interface during deposition.
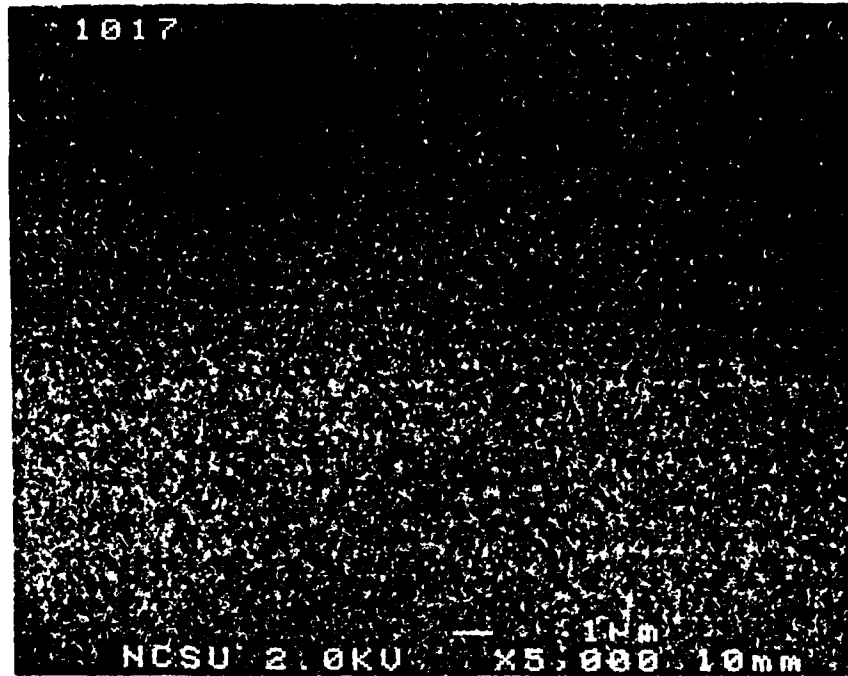
Figure 1: Scanning electron microscopy micrograph of the surface morphology of a heavily Al-doped β-SiC film by scanning electron microscopy.
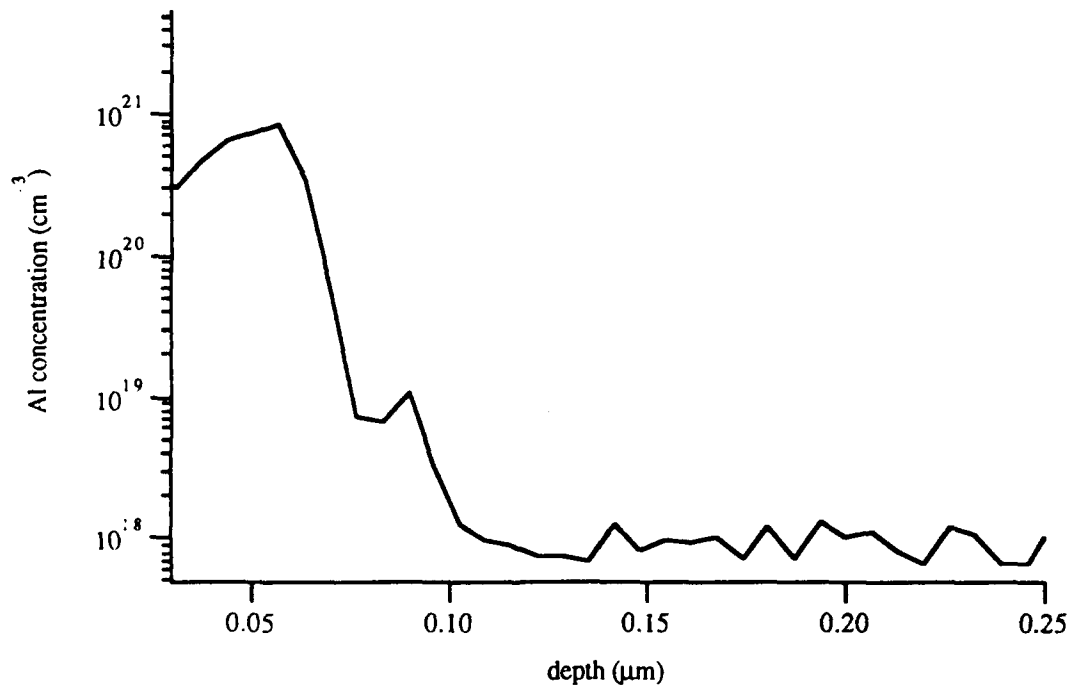
Figure 2: Atomic concentration vs. depth of Al in β-SiC film deposited on α(6H)-SiC substrate.

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Figure 3 is a cross-sectional HRTEM micrograph of a portion of the film and the β-SiC/6H-SiC interface. The substrate is oriented so that the [11$\bar{2}$0] direction of the 6H-SiC substrate is perpendicular to the plane of the image. It was deduced that the 6H-SiC substrate used in this experiment was almost exactly in the (0001) orientation due to the lack of steps at the top of the 6H-SiC substrate layer. From the lattice images of the film, the grown layer is deduced to be cubic and in the (111) orientation. Several (111) stacking faults can be seen in the micrograph (where the film appears to become 6H-SiC for a few layers). A selected area diffraction (SAD) pattern of the film and the substrate is shown in Figure 4. Diffraction spots from both the 6H-SiC substrate and the β-SiC layer can be seen. The epitaxial relationship between the substrate and the β-SiC film can also be observed both from the micrograph and the corresponding SAD pattern.

Figure 3:   Cross-sectional HRTEM image of β-SiC film and 6H-SiC substrate.

Figure 4:   Selected area diffraction pattern of β-SiC film and 6H-SiC substrate.

D. Discussion

The surface morphology of the as-grown film is fairly smooth, and appears to be relatively free of DPBs, as compared to conventional CVD growth. Several researchers [17-21] have suggested that vari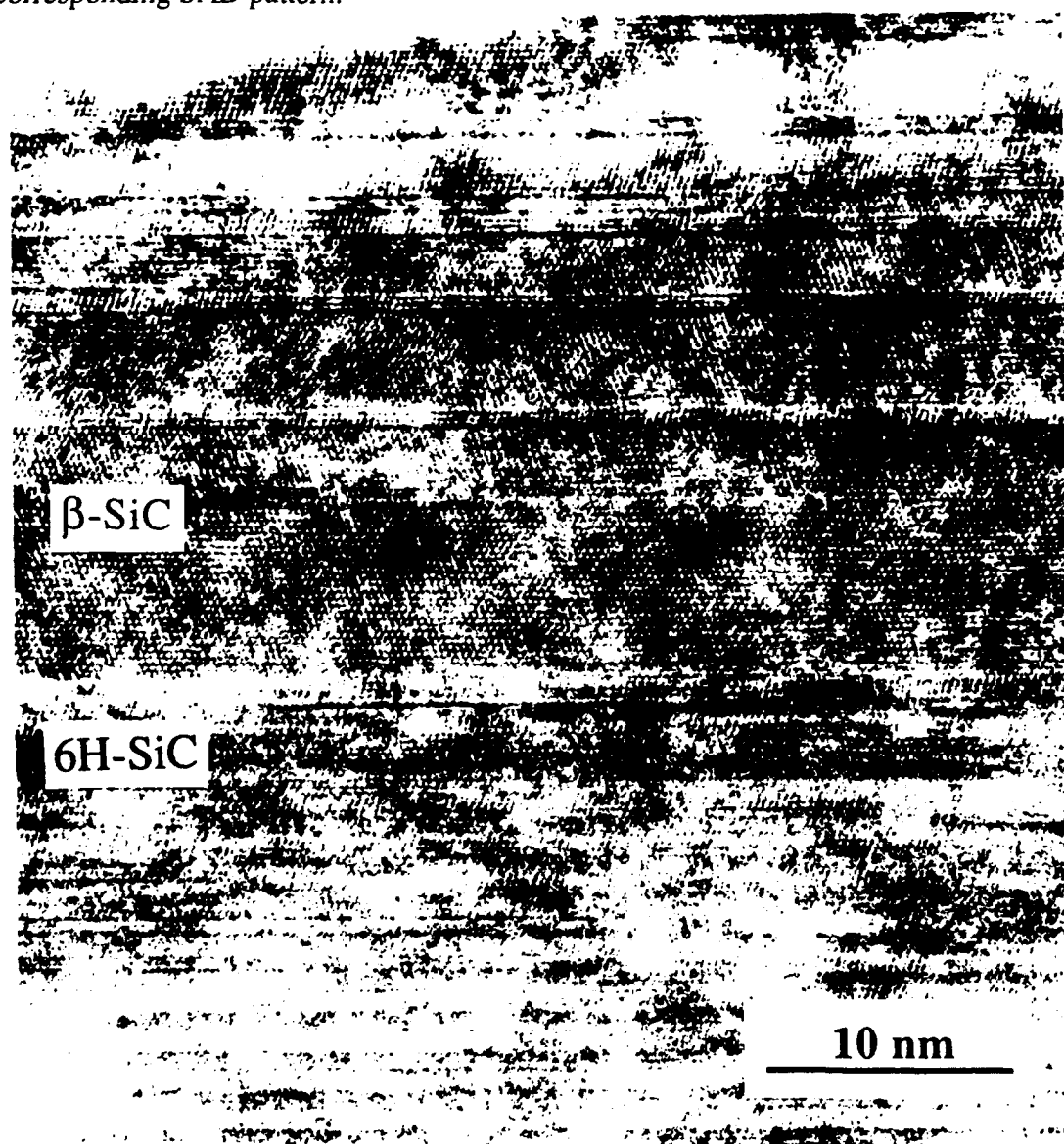ations in surface treatment prior to growth can change the density of or virtually eliminate DPBs formed on the resultant film. Variations in cleaning method have been shown to change DPB density, with the lowest DPB density obtained on the as-received wafers in one study [20]. The effects of annealing in H_2 and growth of thin Si and C layers prior to β-SiC growth on 6H-SiC substrates have also been examined, with most promising results obtained using conversion of a Si pre-growth layer to SiC followed by SiC film growth [21]. In any case, pre-growth treatment of the substrate has been shown to affect DPB density. It is conceivable that DPB formation could be arrested using MBE, if the initial several layers formed were somehow continuous. The level of control using MBE is much greater than with CVD, and this greater control could allow for layer growth on 6H-SiC substrates. Examining the films during growth using *in situ* reflection high-energy electron diffraction (RHEED), as is planned in the near future, should prove conclusive as far as determining whether layer growth is present in the first few monolayers of β-SiC. In addition, as mentioned previously, examination of the MBE-grown films using other methods such as plan-view TEM is necessary to determine whether DPBs actually are present.

The β-SiC film discussed in this report is heavily doped with Al, with a peak concentration of 7×10^{20} cm^{-3}. A value of concentration this high is suspect, and as a result, attempts to

duplicate this result are in process. I-V characteristics taken without a rectifying contact indicate that this sample is p-type. Electrical measurements (I-V and C-V) on this sample are being conducted in order to determine both carrier concentration in the layer as well as characterize the p-type β-SiC/n-type 6H-SiC p-n junction. A high concentration of Al may help to explain the presence of <111> stacking faults seen in Figure 3. The concentration of Al in this film, if the SIMS data is correct, would produce large amounts of strain in the film because of the larger size of the Al atom in a tetrahedral bonding configuration. This strain could induce the formation of these stacking faults as a way of alleviating it. Double crystal X-ray diffraction could prove useful in determining the amount of strain present.

E. Conclusions

Gas source MBE growth of heavily Al-doped epitaxial layers of β-SiC (111) on 6H-SiC (0001) has been achieved at 1250°C using C_2H_4 and Si_2H_6 as source gases. This growth temperature is 250°C lower than that typically used in CVD. High-resolution TEM showed a coherent interface between the film and substrate and the presence of [111] stacking faults. The latter occurred periodically in the β-SiC film. These stacking faults may prove to be due to strain induced by the large concentration of Al present in the film. Surface morphological examination of films using SEM and optical microscopy showed an apparent lack of DPB formation. Further characterization is necessary to determine whether or not DPBs exist in these films. SIMS analysis suggested the presence of a high concentration of Al in these films. Electrical measurements will be conducted in the near future.

F. Future Work

Films of both β-SiC and 6H-SiC will be grown on 6H-SiC (0001) substrates. Al-doped films will be grown to determine the ratio of atomic concentration to carrier concentration. In addition, undoped β- and 6H-SiC will be grown to determine background concentrations of impurity species such as N and residual carrier concentrations. P-n junctions grown using this system will be electrically characterized and leakage currents and diode ideality factors obtained.

Growth on RF-sputtered SiC layers on Si cut 3.5° off (100) will also be attempted. This approach will be tried in order to potentially prevent the formation of <111> pits in the Si substrate (these pits are mentioned in the previous section) and to produce very flat surfaces. If these layers are successful in serving as a template for smooth epitaxial β-SiC films, then electrical measurements on these films will be performed as well.

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III. DEPOSITION AND CHARACTERIZATION OF TITANIUM AND PLATINUM RECTIFYING CONTACTS ON N-TYPE ALPHA 6H-SiC

A. Introduction

A critical issue in current SiC device technology is the ability to choose metals which are good ohmic and rectifying contacts stable at high temperatures. This issue is in turn dependent upon the ability to create a clean surface, to unpin the Fermi level in the semiconductor, and to identify any changes in phase which occur as the temperature is raised.

And therefore, it is an interplay between science and technology which is critically necessary for both long and short term advancement of the quality of contacts.

For an ideal, abrupt junction (at which thermionic emission over the barrier holds) the barrier height is defined by the Schottky-Mott limit, or the difference between the metal work function and the electron affinity of the semiconductor. However, interface states between the metal and semiconductor and traps common to wide bandgap semiconductors cause deviations from ideality. In fact, Pelletier *et al.* [1] have reported Fermi level pinning in 6H-SiC due to intrinsic surface states, indicating little dependence of barrier height on the work function of the metal. On the other hand, Waldrop *et al.* [2] have reported strong work function dependence for metal/β-SiC barrier heights, giving encouragement for the ability to control barrier heights of metals on 6H-SiC.

This report describes the characteristics of Ti and Pt contacts (which were chosen based on their work functions and physical properties) to n-type 6H-SiC. Because Pt has one of the largest work functions of all pure metals, a large barrier Schottky contact is predicted for an ideal junction The merits for Ti/SiC contacts include the similar crystal structures of Ti and 6H-SiC and knowledge of phase formation from previous studies of Ti/SiC diffusion couples [3]. The identification of phases as a function of annealing provides a foundation for understanding the electrical characteristics as the chemistry of the metal-SiC contact changes.

Not only is the particular choice of metal important, but the processing also plays a critical role. More specifically, the nature of the substrate surface, in terms of contaminants, depends on the processing techniques and can control the contact characteristics. This report describes the surface preparation procedure used to produce a 'clean' SiC surface, as well as the results of chemical analysis of the surface at key steps in the cleaning process, the deposition procedures and the results of electrical measurements of the characteristics of the contacts.

B. Experimental Procedure

Vicinal single crystal, nitrogen-doped, n-type ($10^{16} - 10^{18}$ cm^{-3}) substrates of 6H-SiC (0001) containing 0.5-0.8 μm thick, nitrogen-doped ($10^{16} - 10^{17}$ cm^{-3}) homoepitaxial films

were provided by Cree Research, Inc. The Si-terminated (0001) surface, tilted 3°-4° towards [11$\bar{2}$0] was used for all depositions and analyses.

Prior to the deposition of the Ti contacts, the SiC substrates were cleaned using a sequence which involved a a 10 min. dip in an ethanol / hydrofluoric acid / deionized water (10:1:1) solution and a thermal desorption in ultra-high vacuum (UHV) (1–5 × 10^{-10} Torr). All processing steps were the same for the Pt contacts, except that a 10% solution of HF in deionized water was substituted for the wet chemical clean. A resistive graphite heater was used to heat the substrates at 700°C for 15 min. X-ray photoelectron spectroscopy (XPS) and low energy electron diffraction (LEED), both accessible by UHV transfer from the heating station and deposition chamber, were used to monitor surface chemistry and structure, respectively. The XPS system consisted of a Riber Mac2 semi-dispersive electron energy analyzer and a Riber pulse counter. The LEED studies were conducted using a Physical Electronics Instruments 11-020 electron gun. The metals were deposited onto unheated substrates by electron beam evaporation (base pressure < 2 × 10^{-10} Torr). The first 10 nm were deposited at a rate of 1 nm/min. The deposition rate was then increased to 2 – 3 nm/min. to give a total thickness of 100 nm. For electrical characterization, vertical contact structures consisting of 500 µm and 750 µm diameter circular contacts were created by depositing the metal through a Mo mask in contact with the (0001) SiC epitaxial layer, leaving a patterned metal film. Conductive liquid Ag served as the large area back contact. All subsequent annealing was done in UHV. Current-voltage (I-V) measurements were taken with a Rucker & Kolls Model 260 probe station in conjunction with an HP 4145A Semiconductor Parameter Analyzer.

Capacitance-voltage (C-V) measurements were taken with a Keithley Model 5956 Package 82 Simultaneous CV System in conjunction with an HP vector PC-308. The contact structures were the same as above. Measurements were taken at a frequency of 1 MHz.

Ti/SiC samples were prepared in cross-section for TEM analysis. High resolution images and selected area diffraction patterns were obtained with an ISI EM 002B operating at 200 kV.

C. Results
1. SiC Surface

The surface chemistry and structure of substrates after surface preparation were monitored with XPS and LEED, respectively. After chemically cleaning the substrates in a solution of ethanol, HF, and deionized water for 10 min., XPS results showed a Si 2p peak at approximately 101 eV, indicative of Si to C bonding in SiC [4-6]. No Si-O bonding which has been reported at 102.1 – 102.5 eV [4], was detected in the signal. However, small amounts of O and F were detected Other than a shift attributed to sample charging, the Si

peak remained essentially the same after a 700°C desorption for 15 min. On the other hand, a C 1s peak at 285 eV present initially was removed after the desorption. This change indicates the desorption of adventitious C (i.e hydrocarbons), while the major peak remained at 283.5 eV, as expected for C to Si bonding in SiC [4-7].

2. Ti Contacts

Electrical characteristics of both as-deposited and annealed Ti contacts to n-type SiC (1×10^{16} cm^{-3}) were measured. Current-voltage characteristics of as-deposited Ti (curve (a) in Figure 1) were rectifying with typical leakage currents at –10 V of 6 nA (1×10^{-7} A/cm^2); however, values as low as 0.4 nA (9×10^{-8} A/cm^2) were observed. Hard breakdown was not observed to a voltage of –100 V; instead, the leakage current continuously increased, reaching 30 µA at –100V. This soft breakdown is thought to be due to sharp-edge effects from the contact geometries. After annealing in UHV for 20 min. at 700°C, the characteristics degraded (curve (b) in Figure 1). However, the characteristics improved again with each subsequent 20 min. anneal (curves (c) and (d) in Figure 1).
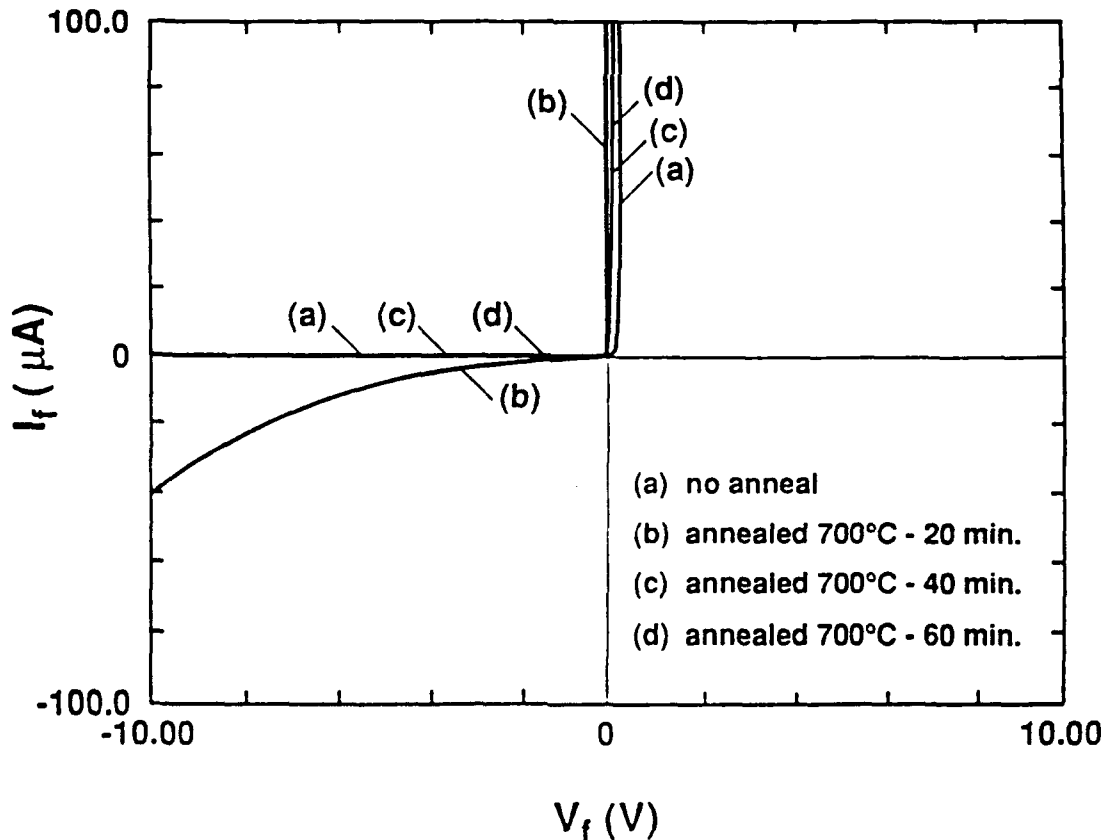

Figure 1.   Current-voltage characteristics of Ti deposited on (0001) 6H-SiC epitaxial layer. (2.0×10^{-3} cm^2 contact area).

Notably low ideality factors for silicon carbide were calculated from plots of log I vs. V for all but the first anneal (Figure 2). For diodes in which the dominant current transport mechanism is thermionic emission and values of voltage V are greater than $3kT/q$, the diode equation can be written as $J = J_o \exp(qV/nkT)$ [9], where J is the current density and n is defined as the ideality factor. Plots of log I vs. V showed linearity over 3 decades of current yielding values of n below 1.1. No ideality factor could be calculated for the first anneal as the linear regime was too small.

Although the calculated ideality factors are low, thermionic emission may not be the dominant current transport mechanism; therefore values for barrier height cannot be directly determined from current-voltage measurements (e.g. see Ref. [10]). Plots of log I vs. log V in the low voltage regime (Figure 3) indicate that current transport is probably dominated by space charge limited current (SCLC), a mechanism which frequently occurs in wide bandgap semiconductors [11].

On the other hand, barrier height values were calculated from differential capacitance measurements as a function of reverse voltage. A plot of $1/C^2$ vs. V should give a straight line such that

$$\Phi_B = V_I + \xi + kT/q \qquad (2)$$

where Φ_B is the barrier height, V_I is the extrapolated intercept at $1/C^2 = 0$, and ξ is the energy difference between the Fermi level and the bottom of the conduction band [9]. Figures 4 and 5 show $1/C^2$ vs. V plots for an as-deposited and an annealed Ti contact, respectively. These curves deviate slightly from linearity but appear to be linear over $1 - 2V$. The deviation from linearity may be caused by series resistance and/or deep level traps in the bandgap of the semiconductor. By extrapolating the linear (low voltage) region of the curves, the voltage intercepts were found to be 0.67 V for the unannealed contact and 0.84 V for the annealed contact. For a doping level of 10^{16} cm^{-3}, these intercepts correspond to a barrier height of 0.88V for the as-deposited Ti/SiC and 1.04V for the annealed Ti/SiC.

Low energy electron diffraction, in which a diffraction pattern from the surface-region is obtained, was used to monitor the surface structure. The LEED pattern remained an ordered 1×1 after deposition of Ti and also through annealing to 900°C in 100°C increments for 10 min. at each temperature. Both Ti (a = 2.95 A, c = 4.68 A) and 6H-SiC (a = 3.08 A, c = 15.11 A) have hexagonal crystal structures, corresponding to a 4% lattice mismatch in the (0001) basal plane. The consistent 1×1 pattern of the SiC surface and these deposited Ti films indicates that growth has occurred epitaxially. Phase identification and structural analysis has been accomplished through collaboration with M.J. Kim and J.S. Bow at Arizona State

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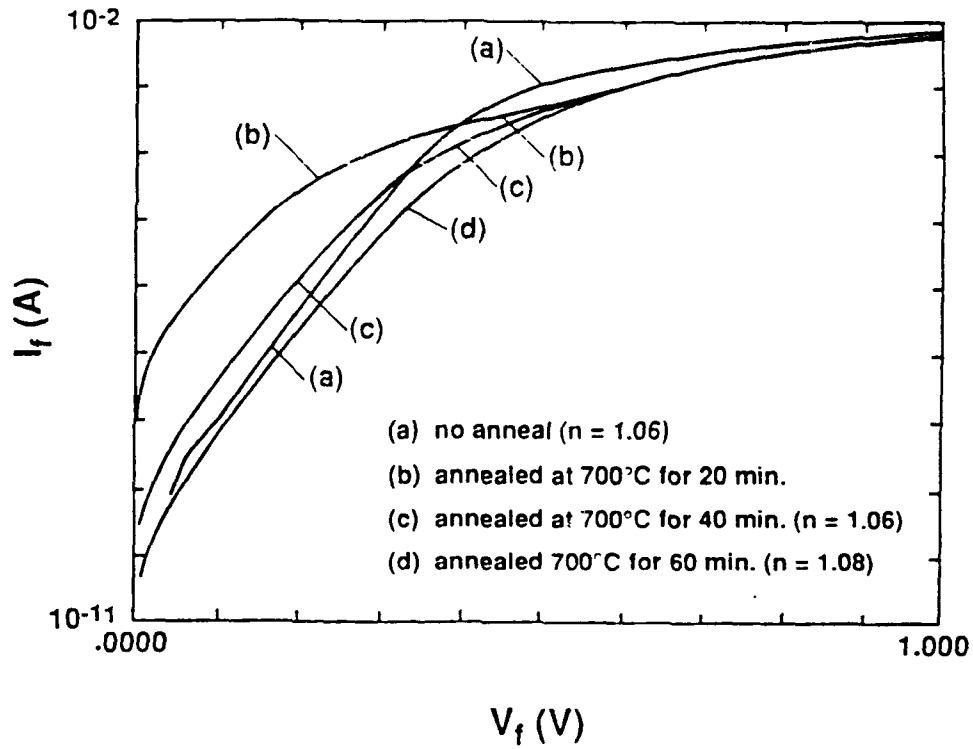
Figure 2. Log I vs. V of Ti deposited on (0001) 6H-SiC.

Within the figure:

10⁻² at top, I_f (A) on y-axis

(a)
(b)
(b)
(c)
(d)
(c)
(a)

(a) no anneal (n = 1.06)

(b) annealed at 700°C for 20 min.

(c) annealed at 700°C for 40 min. (n = 1.06)

(d) annealed 700°C for 60 min. (n = 1.08)

10⁻¹¹ at bottom, .0000 to 1.000 on x-axis

V_f (V)
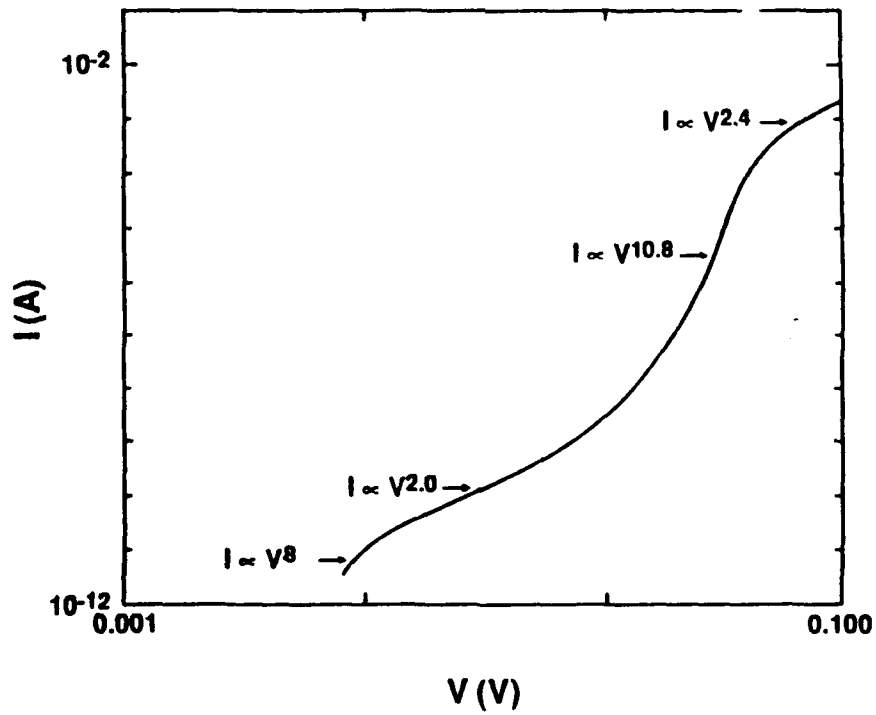
Figure 3. Log I vs. log V of as-deposited Ti/SiC.

Within the figure:

10⁻² at top, I (A) on y-axis

$I \propto V^{2.4}$ →

$I \propto V^{10.8}$ →

$I \propto V^{2.0}$ →

$I \propto V^8$ →

10⁻¹² at bottom, 0.001 to 0.100 on x-axis

V (V)

20

Figure 4. Differential capacitance-voltage measurements for as-deposited Ti/SiC plotted as $1/C^2$ vs. V. $\Phi_B \cong 0.88$ V.

Figure 5. Differential capacitance voltage measurements for annealed (700°C for 60 min.) Ti/SiC plotted as $1/C^2$ vs. V. $\Phi_B \cong 1.04$ V.

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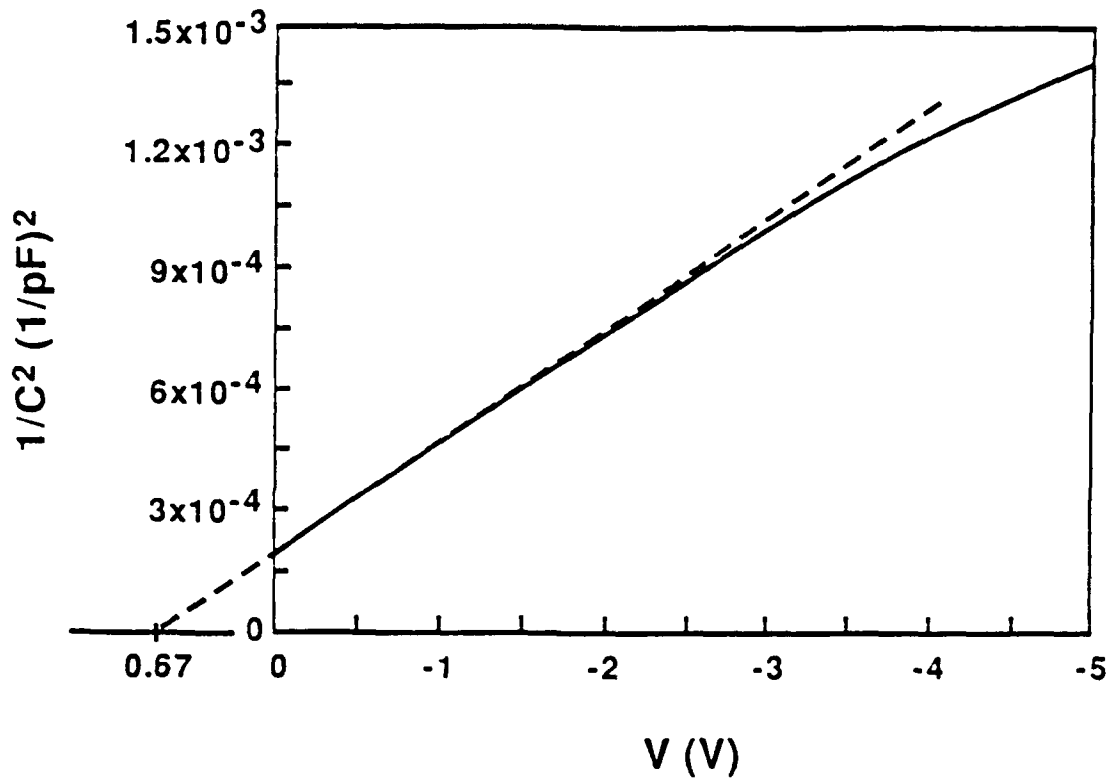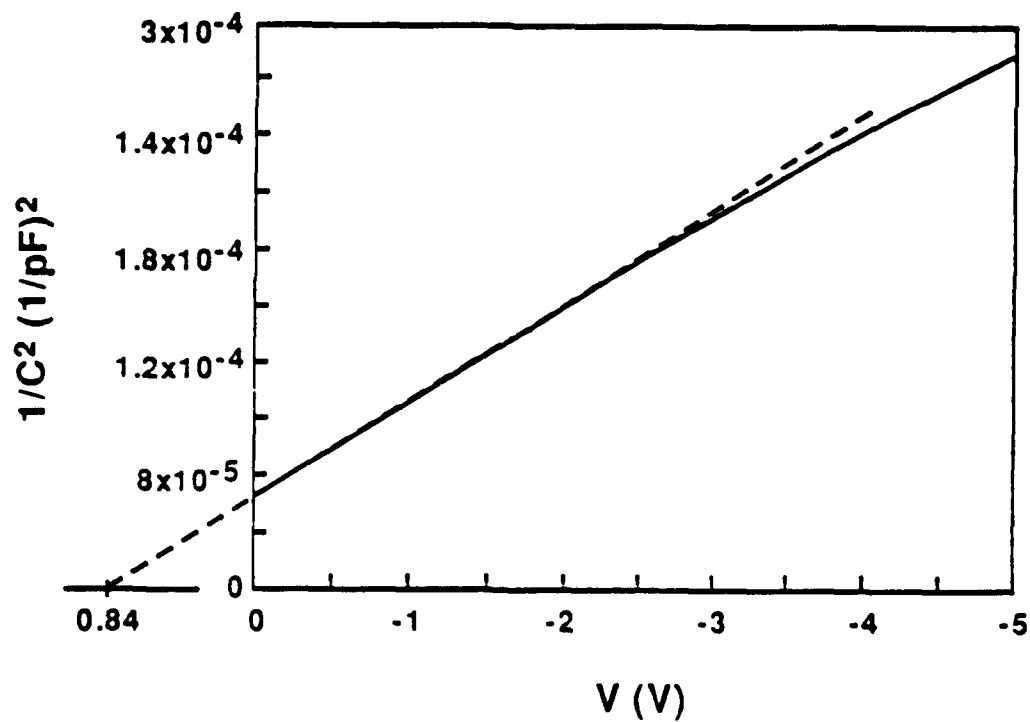University's Facility for High Resolution Microscopy. Figure 6 shows a high resolution image of titanium deposited on a bulk SiC (no epilayer) substrate at 400°C. The 6-layer periodicity in the SiC meets the 2-layer periodicity of the Ti at a non-atomically smooth interface. Close examination of the interface reveals that there appears to be regions of lattice matching. The strain resulting from the 4% lattice mismatch between the film and substrate is relieved by threading dislocations. Selected area diffraction patterns (Figure 7) show a superposition of the spot pattern for the film on that for the substrate, confirming the growth of single crystal titanium. For each orientation of the 6H-SiC [8], the Ti spots lie outside the SiC spots due to the smaller lattice parameter of Ti.
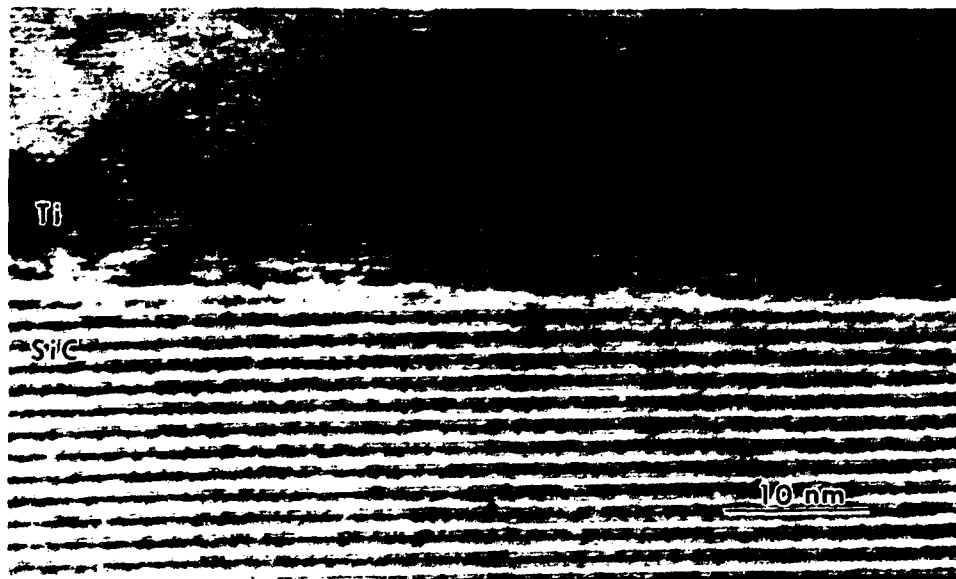

Figure 6. High resolution transmission electron micrograph of as-deposited Ti/SiC interface in cross-section. Ti deposited on (0001) SiC at 400°C.

Figure 7. Selected area diffraction patterns of as-deposited Ti/SiC interface region in cross-section. Ti deposited on (0001) 6H-SiC at 400°C.

After depositing Ti onto a 6H-SiC epilayer at room temperature and annealing at 700°C for 20 minutes, a reacted layer approximately 20 nm thick has formed (Figure 8). Selected area diffraction patterns of the interface region (Figure 9) showed spots other than those seen for the as-deposited Ti/SiC interface. The 'extra' spots were identified as Ti_5Si_3 and TiC. The arrangement of these phases can be seen in Figure 10, which shows a magnification of the region marked "1" in Figure 8. A rather uniform layer of Ti_5Si_3 appears to form at the interface with SiC with particles of TiC at locations along the Ti/Ti_5Si_3 interface.

Figure 8. Cross-sectional high resolution TEM image of Ti/SiC reaction zone (annealed at 700°C for 20 minutes). Ti deposited on (0001) 6H-SiC at room temperature.
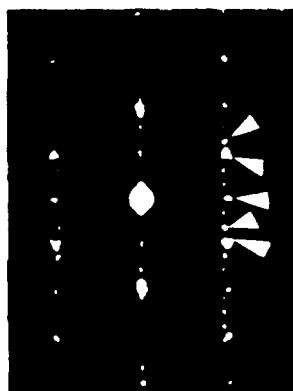
Figure 9. Selected area diffraction patterns of annealed (700°C for 20 min.) Ti/SiC interface region in cross-section. Ti deposited on (0001) 6H-SiC at room temperature.
z = $[11\bar{2}0]$ $_{SiC}$ = $[11\bar{2}0]_{Ti}$ = $[45\bar{1}0]_{Ti5Si3}$ = $[011]_{TiC}$ "1" = Ti_5Si_3 "2" = TiC.

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Figure 10. Magnification of the region marked "1" in Figure 8.

3. Pt Contacts

Current-voltage measurements of Pt contacts deposited on (0001) n-type SiC were also rectifying with typical leakage currents of 5×10^{-8} A/cm^2 at -10 V (Figure 11). The 'soft' breakdown observed is attributed to sharp edge effects due to the contact geometry and not to the material itself. However, it is the forward characteristics which give the most insight into the description of the contacts, and in particular the current transport mechanism.
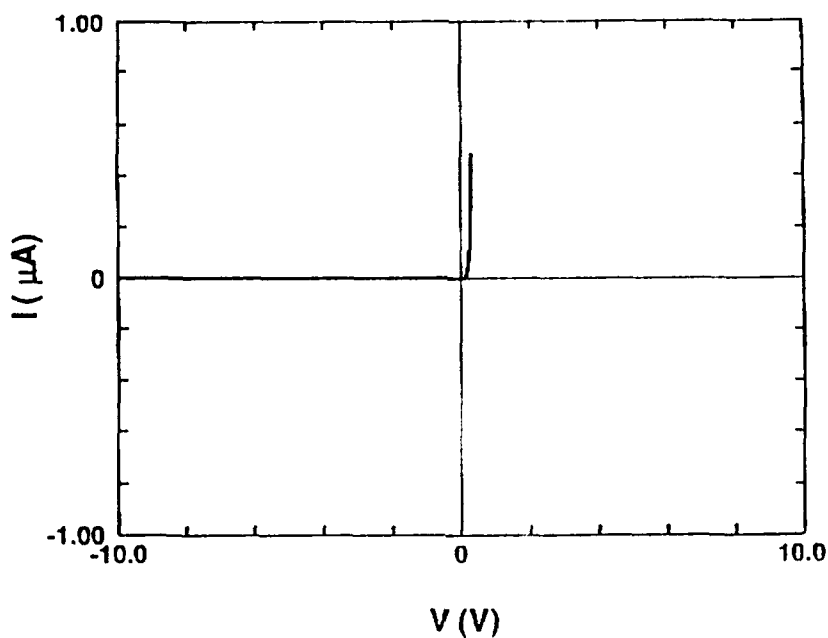
Figure 11. Current-voltage characteristics of Pt deposited on (0001) 6H-SiC epitaxial layer. (2.0×10^{-3} cm^2 contact area).

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As was found for the Ti contacts, low ideality factors (1.02 – 1.08) were calculated for the Pt contacts (Figure 12). However, log I vs. log V plots are in contrast to those for Ti contacts. Figure 13 shows slopes much higher than a slope of 2, which is expected for space charge limited current [11]. The high slopes from the log I vs. log V plots in combination with the excellent log I vs. V characteristics suggest the possibility for thermionic emission controlled current.
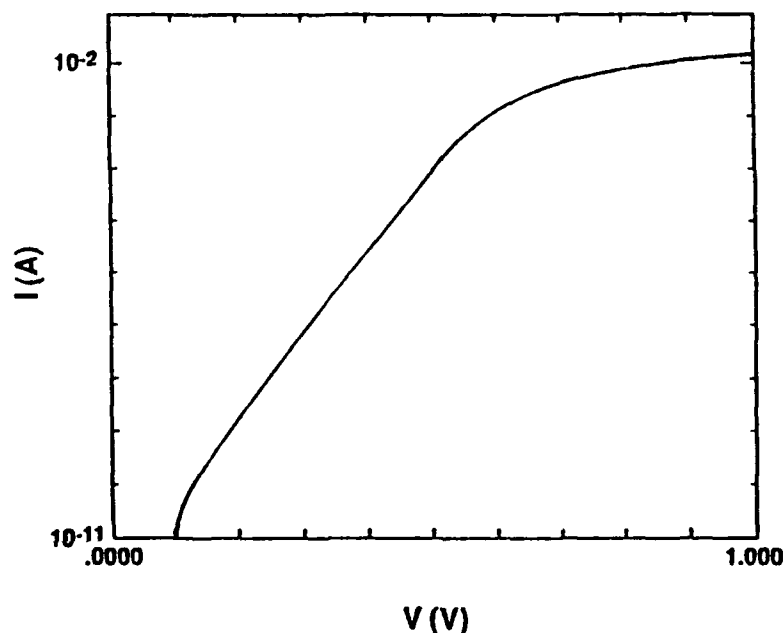
Figure 12. Log I vs. V of Pt deposited on (0001) 6H-SiC.

Figure 13. Log I vs. log V of as-deposited Pt/SiC.

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A barrier height was estimated from capacitance – voltage measurements. A plot of $1/C^2$ vs. V shown in Figure 14 has an intercept on the voltage axis of 0.89 V. Again, the curve is linear over a 1-2 V range. For a doping level of 2×10^{17} cm^{-3}, this intercept corresponds to a barrier height of 1.02 V.
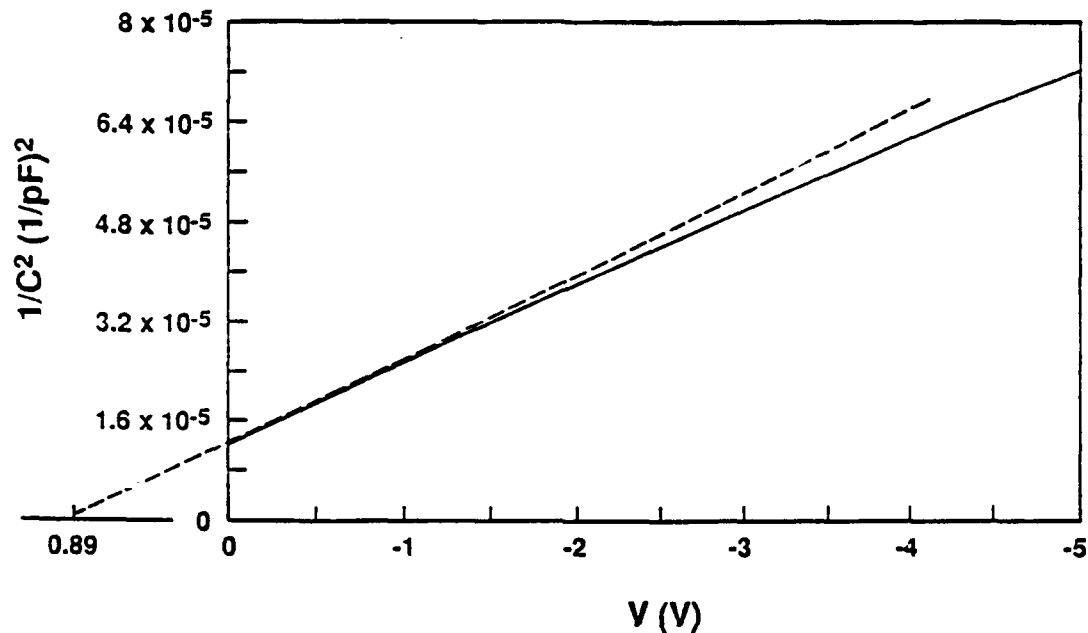
Figure 14. Differential capacitance-voltage measurements for as-deposited Pt/SiC plotted as $1/C^2$ vs. V. $\Phi_B \cong 1.02$ V.

D. Discussion

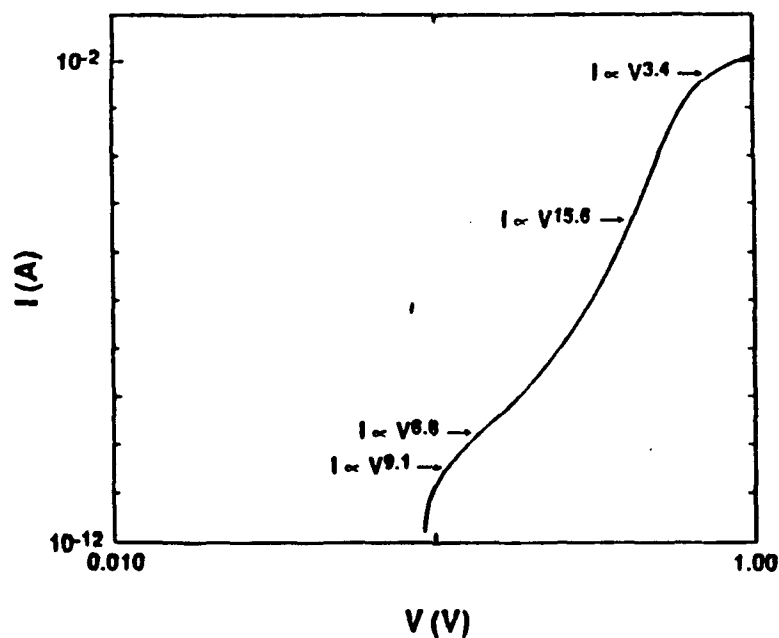By subtracting the electron affinity of the semiconductor from the work function of the metal, theoretical, ideal barrier heights were calculated. Pelletier et. al. [1] have reported the Fermi level to be pinned near midgap in 6H-SiC with a work function of approximately 4.8 eV (intrinsic). Using a calculated value of 1.44 eV for the intrinsic Fermi level (measured from the the top of the valence band), the electron affinity (measured from the bottom of the conduction band to vacuum level) is estimated to be 3.38 eV. The work function of Ti is 4.33 eV, and that of Pt is 5.65 eV. From these work function values, barrier heights of 0.95 eV and 2.27 eV, respectively, are predicted. Although the 0.88 eV value calculated from C-V measurements for Ti (Figure 4) corresponds to a 7% difference from the predicted value of 0.95 eV, the calculated and predicted barrier heights for Pt correspond to a 55% difference. In addition, the measured barrier heights for the Ti and Pt contacts are within 0.14 eV of each other. It is obvious that more barrier height measurements are necessary before a conclusion can be drawn as to an accurate description of band bending and barrier heights.

The reaction chemistry on annealing directly affects the electrical characteristics (e.g. barrier height) because the characteristics become dependent upon the new interface formed with SiC. A reaction path in Ti/SiC diffusion couples at 1200°C in which TiC_{1-x} particles form in a matrix of Ti_5Si_3 has been reported [12] and is very similar to the results found in this study. However, some questions still remain in that the reported work function value of 3.71 eV for Ti_5Si_3 [13] would indicate a smaller barrier height of 0.33 eV. This prediction contradicts the experimental data (Fig. 8) in which a larger barrier height than that of the as-deposited Ti/SiC was calculated. With these issues in mind, more research on barrier heights and phase chemistry in the Ti/SiC system is anticipated.

The initial results from current-voltage measurements on Pt contacts give encouragement for taking elevated temperature measurements (and from these calculate Richardson's constant) and trying to determine barrier height. Not only were low ideality factors calculated from log I vs. V plots with a linear region of 5 decades of current, but log I vs. log V plots showed slopes which appear to be more indicative of thermionic emission than of space charge limited current. Comparison of Figures 2 and 12 shows that Pt has a sharper rise in current, which turns on at a higher voltage.

On the other hand, questions are raised from capacitance-voltage measurements. By extrapolating the low voltage region of the $1/C^2$ vs. V plot, a barrier height of 1.02 eV was calculated. This value is much lower than the 2.27 eV value predicted and close to the 0.88 eV calculated for as-deposited Ti. This may indicate that the Fermi level is pinned in the SiC due to surface states or traps in the bandgap. However, no conclusions can be drawn without further barrier height measurements and possibly measurement of traps by deep level transient spectroscopy (DLTS).

E. Conclusions

Both Pt and Ti contacts deposited on (0001) 6H-SiC at room temperature were rectifying with calculated ideality factors less than 1.1. While log I vs. log V plots of Ti contacts in the low voltage regime indicate that space charge limited current is the dominant transport mechanism, thermionic emission may hold for the Pt contacts.

Barrier heights were estimated from differential capacitance – voltage measurements. The measured value of 0.88 V for as-deposited Ti agrees quite well with the predicted value of 0.95 V. On the other hand, the increase in barrier height to 1.04 V for the annealed contact (700°C for 60 minutes) contradicts the decrease in barrier height predicted for the phases identified at the interface. After annealing for 20 minutes at 700°C, the interface has been found to consist of Ti_5Si_3 with particles of TiC.

Pt showed little variation from Ti in its barrier height measurements. The calculated value of 1.02 V is 55% smaller than the 2.27 V barrier calculated for the ideal case. The initial

measurements on Pt seem to indicate that there is little or no correlation between the barrier height and the work function of the metal.

F. Future Research Plans and Goals

1. Ti Contacts

The bulk of the experiments on Ti contacts. will be completed. The anticipated work includes analyzing the XPS valence structure taken of a Ti deposition series on SiC. If no chemical interaction is assumed, a barrier height can be calculated by comparing the valence band edge of the SiC with the Fermi level after depositing the Ti layers.

More study of the interfacial reaction zone is also anticipated. By studying samples which have been annealed for longer periods of time, the progression of the reaction can be observed, and the exact nature of the electrical interface may be better understood.

2. Pt Contacts

As described above, the initial electrical characteristics (i.e. low leakage, low ideality factors, and high log I − log V slopes) have provided the impetus for measuring I-V characteristics at elevated temperatures. By comparing the characteristics, it will be determined whether a value for barrier height can be determined. In addition, other techniques such as XPS and internal photoemission will be used to try to determine barrier height.

An annealing series will be begun to correlate electrical characteristics with the phases formed at the interface. TEM will play an integral role in identifying the phases formed; the electrical characteristics would then be attributed to the new phases(s) identified at the interface with SiC.

3. Hf, Sr, and Co Contacts

A similar study to those of Ti and Pt contacts will be begun for Hf, Sr, and Co contacts. Hf has been inserted in the electron beam evaporation system and is ready to be deposited. Preliminary electrical measurements will be taken of each of these contacts, and an in-depth, electrical-chemical-structural study will be carried out .

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IV. Modeling and Characterization of Electronic Devices Fabricated from SiC—*6H-SiC IMPATT Performance and Limitations**

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Abstract

The physical limitations to the RF operation of IMPATT diodes resulting from the low magnitude of the charge carrier mobility in SiC are investigated by means of a numerical device model. The results of this investigation indicate that good RF output power can be obtained from SiC IMPATTs. However, the low magnitude of the charge carrier mobility in SiC limits the magnitude of the RF voltage that can be supported, and thereby prevents efficient dc to RF power conversion.

A. Introduction

Considerable interest has developed in the application of the wide bandgap semiconductor materials, diamond and SiC, for power electronics. Several of the properties of these materials, including high operating temperature, high thermal conductivity, high saturation velocities for charge carriers, and high breakdown voltages, suggest that these materials have potential to far out perform conventional semiconductors in electronic applications. Several figures-of-merit, which indicate the relative potential of elemental and compound semiconductor for high power applications, have shown that α-6H-SiC has significant advantages over Si, GaAs, and GaP [1]. While these figures-of-merit are convenient in providing an initial indication of the material performance, only the large signal simulation of a specific electronic device with experimentally measured material parameters will provide a reliable indication of the advantages of these materials. The use of such a device model makes it possible to adjust design parameters so that the material characteristics that improve performance are maximized, while any detrimental material effects are removed or limited.

Presented here are the results of an investigation into the simulated performance of 6H-SiC double -drift IMPATT diodes. A large-signal device physics model of an IMPATT diode, based upon drift/diffusion carrier transport (i.e., Boltzmann transport) and electric field

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* The following is a preprint of a paper recently completed and submitted for publication.

dependent impact ionization, is employed to study SiC at the four frequencies of 35, 44, 60, and 94 GHz.

The large-signal model used considers only carrier transport and carrier generation in evaluating the performance of a semiconductor material. Such constraints as the thermal conductivity and load impedance matching are used to determine the optimum current density and device area for a particular frequency. These constraints allow for the comparison of SiC diodes to the actual performance of conventional IMPATTs.

B. Material Parameters

The RF performance of 6H-SiC IMPATT diodes is determined by both the structural design (i.e., doping levels and layer thickness) and the electronic transport properties of the material. Electronic material parameters of interest are electron and hole transport characteristics as described by the mobile charge carrier velocity-field and diffusion-field characteristics. A list of the cogent parameters is given in Table I.

Table I. Material Parameters for 6H-SiC Used in the IMPATT Simulations.

Parameter	Value
Hole Mobility (μ_p)	50 cm^2/V-s
Hole Saturation Velocity (v_{psat})	5.4×10^6 cm/s
Hole Diff. Coef. (D_p)	0.55 cm^2/s
Electron Mobility (μ_n)	250 cm^2/V-s
Electron Saturation Velocity (v_{nsat})	2.0×10^7 cm/s
Electron Diff. Coef. (D_n)	9.88 cm^2/s
Ionization Constants	
(α_p)	4.65x×10^6 cm^{-1}
(α_n)	4.65×10^4 cm^{-1}
($\beta_{n,p}$)	1.2×10^7 V/cm
Dielectric Constant (ε_r)	9.7
Thermal Conductivity (κ_T)	5 W/cm-°C

Experimental velocity-field characteristics have been reported for 6H-SiC [2,3]. The velocity-field characteristics for both electrons and holes for several semiconductors are compared in Figures 1 and 2. The saturation velocity for electrons in 6H-SiC is 2×10^7 cm/s at room temperature for nitrogen doped SiC (with n=10^{17} cm^{-3}). From Figure 1, it is observed that the saturation velocity for electrons in a 6H-SiC exceeds that of Si, InP and GaAs and

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suggests that this wide bandgap material would be superior as a high frequency semiconductor. The electron low field mobility for an impurity concentration of 10^{17} cm^{-3} is 250 cm^2/v-s. The low field mobility for holes is between 40 and 60 cm^2/v-s for a carrier concentration of 5×10^{15} cm^{-3}, but hole saturation velocity is still undetermined.
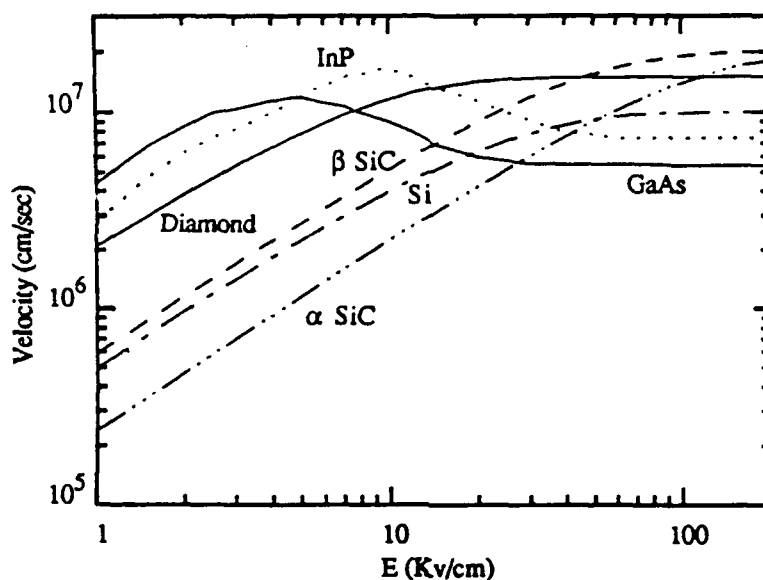
Figure 1. Electron velocity vs. electric field for several semiconductors at $N_D = 10^{17}$ cm^{-3}.
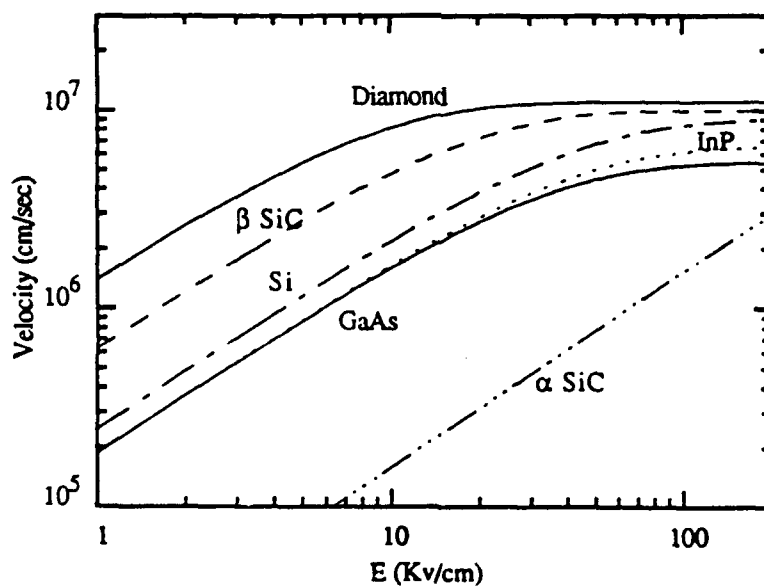

Figure 2. Hole velocity vs. electric field for several semiconductors at $N_D = 10^{17}$ cm^{-3}.

The saturation velocity for holes in SiC is estimated to be about 5.4×10^6 cm/s. This value of saturation velocity allows the holes and electrons to saturate at the same electric field (approx. 2-300 kV/cm). While it might be reasonable to assume a saturation velocity for holes

in SiC equal to that of electrons, the electric field necessary for saturation to occur would be 3 to 4 times greater. In an IMPATT diode, where carriers move across the active region at the saturation velocity, the minimum electric field could exceed 1 MV/cm. An electric field of this magnitude would produce significant avalanche throughout the device.

Because of the lack of information regarding the diffusion coefficient, the Einstein relationship is used to calculate the diffusion coefficients from the mobility measurements. A constant value for the diffusion coefficients is assumed.

While many investigators have reported avalanche breakdown in 6H-SiC [4-7], two have considered the effect of the direction of the electric field relative to the c axis of the hexagonal crystal [8,9]. Dmitriev, et. al., find 6H-SiC to be strongly anisotropic with respect to avalanche breakdown. Epitaxial 6H-SiC is typically grown in the c direction and conventional IMPATT diode fabrication would produce devices with the electric field also in the c direction. Dmitriev finds that the process of impact ionization is decisively influenced by superstructure splitting in the conduction band and that holes dominate the carrier generation. The avalanche generation by electrons is considered insignificant. Anikin, et. al., also find the avalanche breakdown to be anisotropic and dominated by hole generation, but believe that the avalanche mechanism involves deep level states corresponding to residual impurities and not the conduction band superstructure. While only the ionization rates and not the avalanche mechanism are needed to perform initial device simulations, future simulations might need to consider the effects of temperature and current density on the avalanche generation rates. The ionization rates when the field is parallel to the c axis are as follows:

$$\beta_p = 4.65 \times 10^6 exp(-1.2 \times 10^7 /E)$$

and

$$\alpha_n = \beta_p /100$$

where β_p and α_n are the ionization rates for holes and electrons, respectively, and are given per centimeter. Avalanche rates have not been reported for electrons, but are considered insignificant. In these simulations, electron avalanche rates were assumed to be about 1 % of the value found for holes.

C. SiC IMPATT Performance

The dopant levels and thicknesses for the layers of the double-drift, uniformly doped 6H-SiC IMPATT diodes were optimized to provide the maximum RF output power. These SiC profiles differ from the design found for the other semiconductors, due to the requirements that holes initiate the avalanche current and to the poor transport properties of SiC holes, as indicated in Table II.

Table II. Optimized Profiles for SiC Double Drift IMPATT Diodes.

Freq (GHz)	p-region Doping (10^{17} cm^{-3})	P-Width (µm)	n-region Doping (10^{17} cm^{-3})	n-Width (µm)
35	1.50	1.00	0.63	2.30
44	1.80	0.90	1.00	1.70
60	2.20	0.75	1.15	1.40
94	2.50	0.60	1.50	1.10

For 6H-SiC, with it's higher thermal conductivity and breakdown voltage, the use of the same current densities that are acceptable for Si or GaAs would be misleading in the comparison. In order to include these additional factors in the evaluation of SiC IMPATTs, an area-current density (A-J) analysis procedure devised by Blakey and Linton is employed [10]. This technique establishes the limits of allowed combinations of device area and dc current density. The allowed combinations are limited by several mechanisms. These mechanisms include thermal limitations, space-charge induced field perturbations, the minimum diode impedance, and the avalanche resonance limit for current density, as described by Gilden and Hines [11]. Each of these limitations gives rise to a boundary in the A-J plane between allowed and unallowed combinations of device area and current densit. The location of each of these boundary lines is a function of the material, the diode structure, and the frequency.

An example of the A-J analysis for the 44 GHz SiC IMPATT is presented in Figure 3. For this IMPATT diode and the other SiC diodes investigated, RF power was limited by the thermal resistance and the high breakdown voltages.

For CW operation this analysis, in conjunction with the large signal model, predicts maximum RF output power for SiC IMPATTs to be about 2.1 W at 35 GHz, 3.26 W at 44 GHz, 3.92 W at 60 GHz, and 1 W at 94 GHz, as indicated in Table III.

In α-SiC, velocity saturation occurs when the electric field approaches 300 kV/cm. For Si, GaAs, InP and Diamond, velocity saturation requires an electric field of no more than 100 kV/cm, as indicated in Figs. 1 and 2. The higher electric field increases the portion of the applied voltage that cannot be modulated, and decreases the dc to RF conversion efficiency of the diode.

Figure 4 shows a terminal RF voltage waveform of 80 v, and the current waveforms for a 44 GHz SiC IMPATT with RF voltages of 80, 110 and 130 v. The RF voltage of 80 volts is about 20% of the dc voltage that is applied to the SiC diode, which is biased with a dc voltage of 440 v. For materials such as diamond and GaAs, the optimum RF voltage that can be supported by the diode is greater than 50% of the dc voltage. When the RF voltage is increased
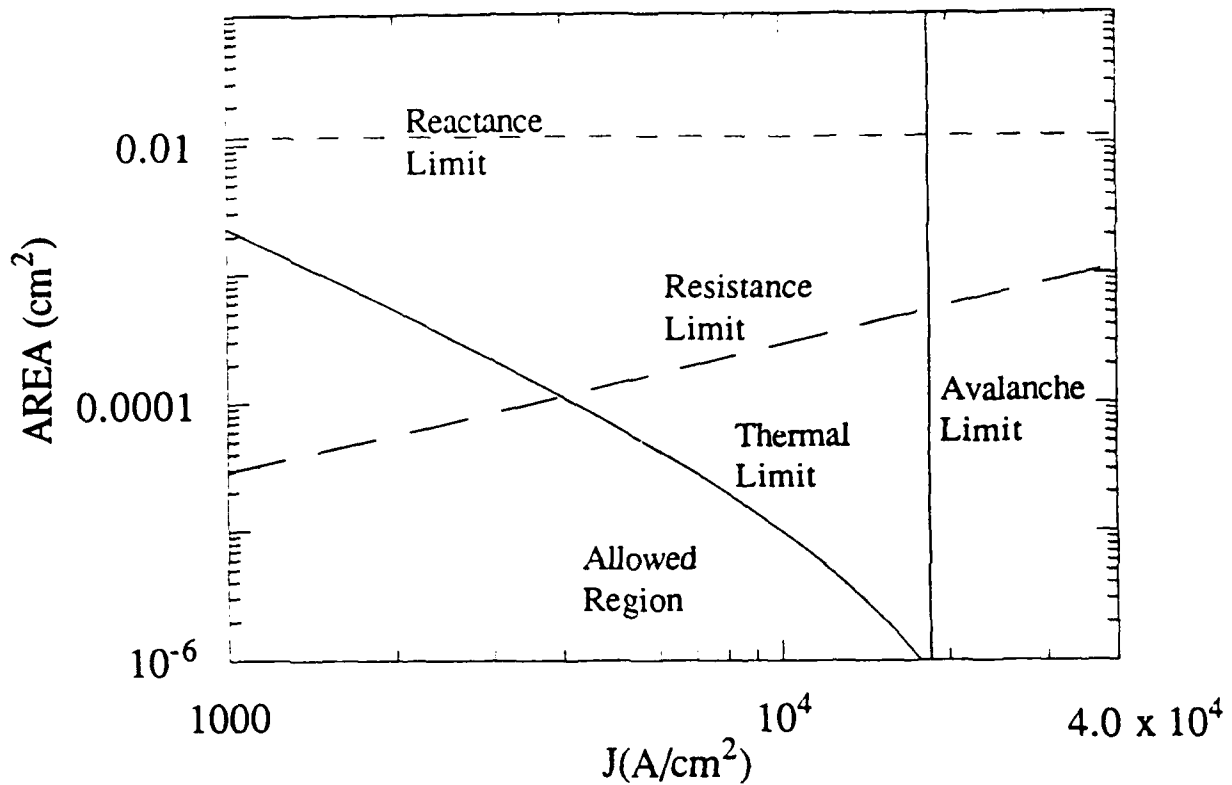
Figure 3.   A-J plane analysis: a technique for IMPATT diode optimization. The analysis for a 44 GHz diode is shown.
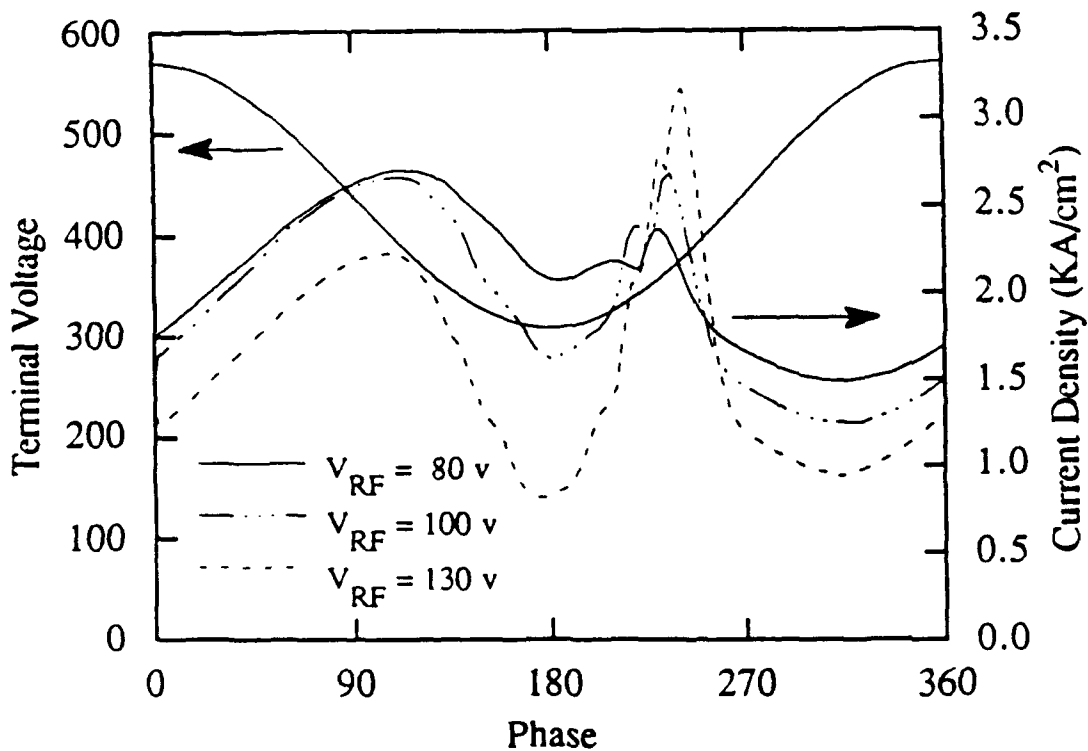

Figure 4.   The terminal current vs. phase for a 44 GHz SiC IMPATT for RF voltages of 80, 100, and 1130 volts. The terminal voltage waveform for 80 volts is included.

for the SiC device, the limitations due to the low mobility of the holes become apparent. As the magnitude of the RF voltage is increased, there is a drop in the terminal current near 180 degrees. This occurs because the terminal voltage has dropped to its minimum at 180 degrees and the electric field has fallen below the level necessary to maintain the charge carriers at their saturated velocity. As the terminal voltage increases, the electric field rises and the terminal current rises again. It is the low field mobility of holes that limits the magnitude of the RF voltage that can be supported by SiC IMPATTs. This effect has also been observed in the simulation of diamond and GaAs IMPATTs under large RF voltage conditions, but the effect is not as severe as for SiC.

Table III contains the CW performance and, in some cases, the current density and area were adjusted to investigate the change in RF output power and efficiency. Higher current density increases the efficiency of the SiC diodes, but the thermal limitations decrease the diode area and usually decrease the RF output power. The performance of SiC IMPATTs is compared with other materials in Figure 5. While the RF output power for SiC devices is similar to Si and GaAs IMPATTs, the dc to RF conversion efficiency for SiC diodes is much less.

Table III. SiC Diode CW RF Performance Chacteristics.

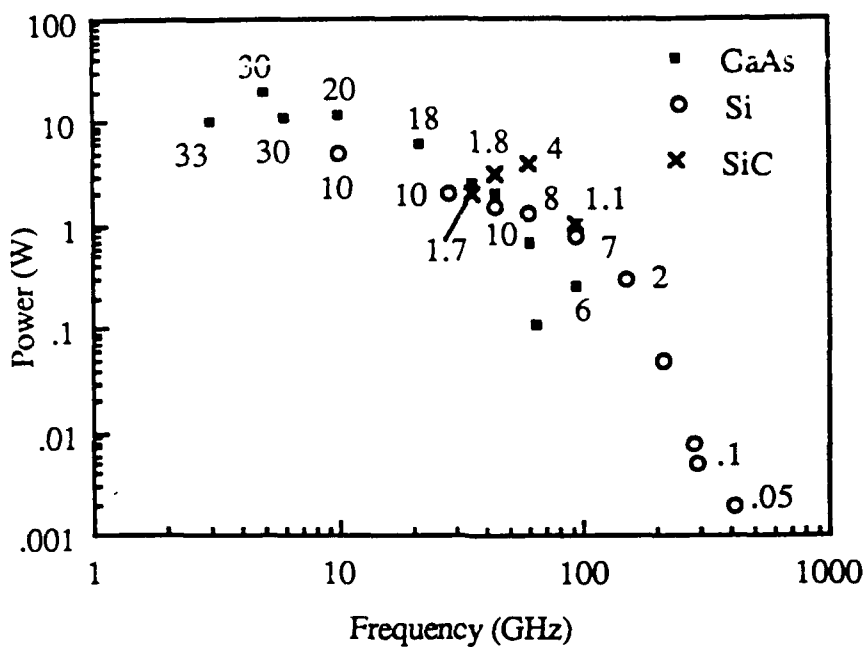| Freq (GHz)	Area (cm^{-2})	J (kA/cm^2)	I (mA)	Vdc (V)	PRF (W)	η (%)
35	7.0×10^{-5}	4.0	280	512.4	2.10	1.7
35	2.3×10^{-5}	6.0	138	517.2	0.92	1.6
44	1.1×10^{-4}	4.0	440	436.9	3.26	1.8
44	2.0×10^{-5}	8.0	160	425.6	0.25	2.1
44	2.0×10^{-6}	15.0	30	426.2	0.36	3.2
60	3.3×10^{-5}	3.0	100	355.9	0.21	0.6
60	5.6×10^{-5}	5.0	280	352.1	.84	1.88
60	2.9×10^{-5}	8.5	247	372.7	3.92	4.28
94	3.8×10^{-5}	10.5	400	243.1	1.03	1.1
94	2.1×10^{-6}	28.6	60	236.3	0.42	3.0

Figure 5. The output power for GaAs, Si and SiC IMPATT diodes. Numbers represent power conversion efficiency (%).

The saturation velocity of holes was assumed to be 5.4×10^6 cm/s. Although there is uncertainty in the actual value for the hole saturation velocity due to a lack of measurements, and the actual value could possibly be higher than the value assumed here. A higher saturation velocity would require a longer p-region to maintain a constant time delay as the holes traversed the drift region. Also, due to the low mobility of holes, the minimum electric field necessary to maintain velocity saturation would increase. The increases in device length and minimum electric field would increase the applied voltage, and increase the dc power dissipation, thereby enhancing thermal degradation. The thermal limitation could be eleviated by pulse bias operation.

Although the RF performance of double drift diodes in SiC is limited by the low mobility of holes and the need for holes to generate the avalanche current, this investigation indicates that single drift IMPATT diodes should perform much better than similar diodes fabricated from conventional semiconductors. In a single drift p^+n SiC diode, holes initiate the avalanche and constitute the avalanche current that flows across the junction. The low mobility of SiC holes suggests that the hole diffusion coefficient would also be low and the diffused holes would remain close to the junction. This would limit the width of the avalanche region for the diode and decrease the avalanche voltage. The additional holes that are generated in the n-region of the SiC would be swept towards the junction and collected. These holes would move toward the junction, where the electric field strength increases, and the probability that these holes would cause additional ionization increases.

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The thermal limitation of SiC diodes is reduced in single drift structures due to the lower breakdown voltages. Single drift diodes also reduce the distance between the heat producing junction and the heat sink and reduce the thermal resistance.

The dc solution for a 60 GHz SiC device as shown in Figure 6 indicates how the hole transport properties and avalanche generation control the structure of these IMPATTs. In this structure, the avalanche current is generated in the p-region of the device where there is a sufficient number of holes to initiate the avalanche current.
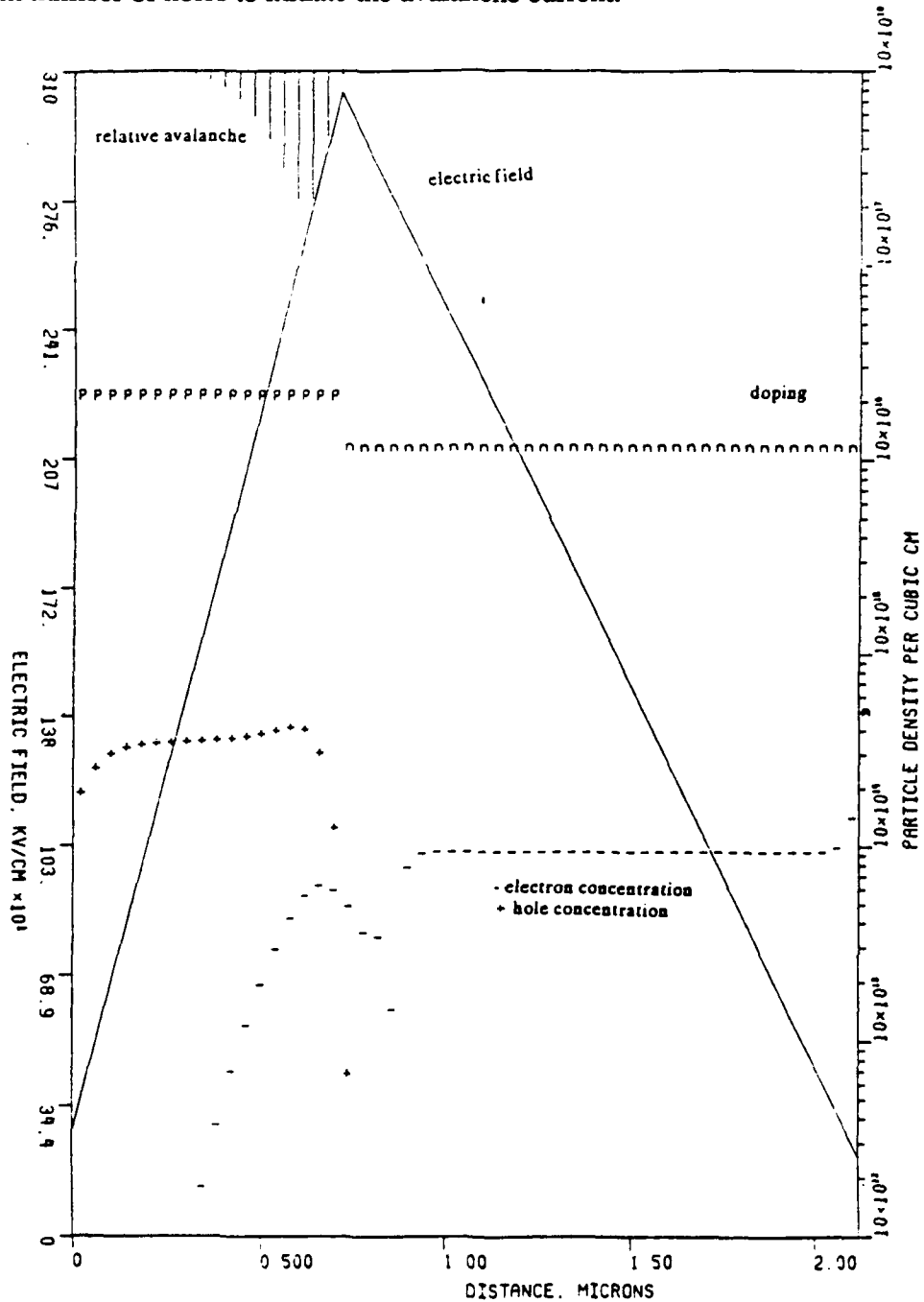

Figure 6. DC solution for the 60 GHz SiC IMPATT.

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D. Conclusions

The RF performance of 6H-SiC IMPATT diodes has been investigated by means of a theoretical, physics based device model. It is found that the combination of high breakdown voltage and thermal considerations limit the practical current density at which the diodes can be operated. The problem is more severe for double-drift diode structures. Additionally, it is found that the low field mobility of holes prevent double drift SiC IMPATTs from supporting large RF voltages, thereby reducing the dc to RF conversion efficiency possible. The RF power output of SiC IMPATTs is similar to that possible from comparable devices fabricated from Si, but the conversion efficiency is significantly reduced. Possible improvements may be obtainable from single-drift, n-type devices. Such a device would have lower breakdown voltage and improved thermal resistance. The device would not rely on the transit time delay of holes and the degrading effects of the low magnitude hole mobility on conversion efficiency would be reduced.

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V. Fabrication and Characterization of High Power/High Frequency α(6H)-SiC MESFETs with Exceptional Power Densities

A. Introduction

High frequency MESFET devices were reported in the previous year that showed, for the first time, significant power gain in the microwave frequency range. In the present report, much better high frequency characteristics are reported, both in terms of operating frequency and in power handling capability. The best values of f_t and f_{max} reported for these devices were 4.5 GHz and 3.0 GHz, respectively. At 1.0 GHz, these devices had a power gain of 13.5 dB and a current gain of 12.5 dB. The devices were measured to drain voltages of 40 V with an on-current of 310 mA, resulting in a very high DC power density of 12.4 W/mm.

The improved characteristics of these devices are due to two factors. The first is the use of a thicker gold overlayer on the gate. The gold overlayer thickness of the present devices was 1.0 μm; whereas, the previous devices had a thickness of 0.75 μm. This resulted in a reduced parasitic gate resistance. The second factor was the use of a thicker channel layer, which reduced the source resistance and increased the DC power density.

Additionally, some new experimental MESFET structures are being fabricated to further improve the high power / high frequency behavior of 6H-SiC by reducing both the gate resistance and source resistance. These new structures encompass both fabrication procedures and device design. While these devices have not yet been completed, they should result in significant improvements in the high frequency characteristics of 6H-SiC MESFETs.

The other high frequency device that has been investigated is an IMPATT diode. The last report reported some very good avalanche results using the "high-low" doping structure. These devices were pn junction based structures. Some devices were demonstrated to withstand as much as much as 124 kW/cm^2 of avalanche power density at 95 V. While these characteristics were promising, the measured forward resistance of the diode structure was still too high. A forward bias resistivity of 8.2×10^{-4} Ω-cm^2 was measured on these devices. While the unthinned substrate contributed much of this resistance, about 2.2×10^{-4} Ω-cm^2 was calculated to be due to the p-type ohmic contact. This resistivity is considered to be too high for efficient operation at 60 GHz, and therefore the focus for IMPATT diodes has been shifted to reducing the contact resistance. Also, the epitaxial doping was reduced in order to get a lower voltage avalanche.

B. Experimental Procedure
1. High Power / High Frequency MESFETs

The substrates used for this research were sliced from lightly nitrogen doped, n-type 6H-SiC single crystal boules. The substrates were subsequently lapped and polished into wafers

suitable for epitaxial growth. Thin films of monocrystalline 6H-SiC (0001), both p- and n-type, were epitaxially grown on these n-type 6H-SiC (0001) wafers. The MESFET, shown in cross-section in Figure 1, consisted of a 2 μm thick p-type epitaxial layer of 6H-SiC having a carrier concentration in the range of 5×10^{15} cm^{-3} grown on the n-type 6H-SiC substrate. This p-type layer acted as the buried layer to confine the current to a thin n-type active region which was subsequently grown. This top n-type epitaxial layer had a carrier concentration in the range of 1.2×10^{17} cm^{-3} and a thickness of about 0.3 μm depending on the doping and desired pinch-off voltage of the device. The formation of the ion implanted wells, ohmic contacts, and Schottky contacts on the channel layer is discussed below.
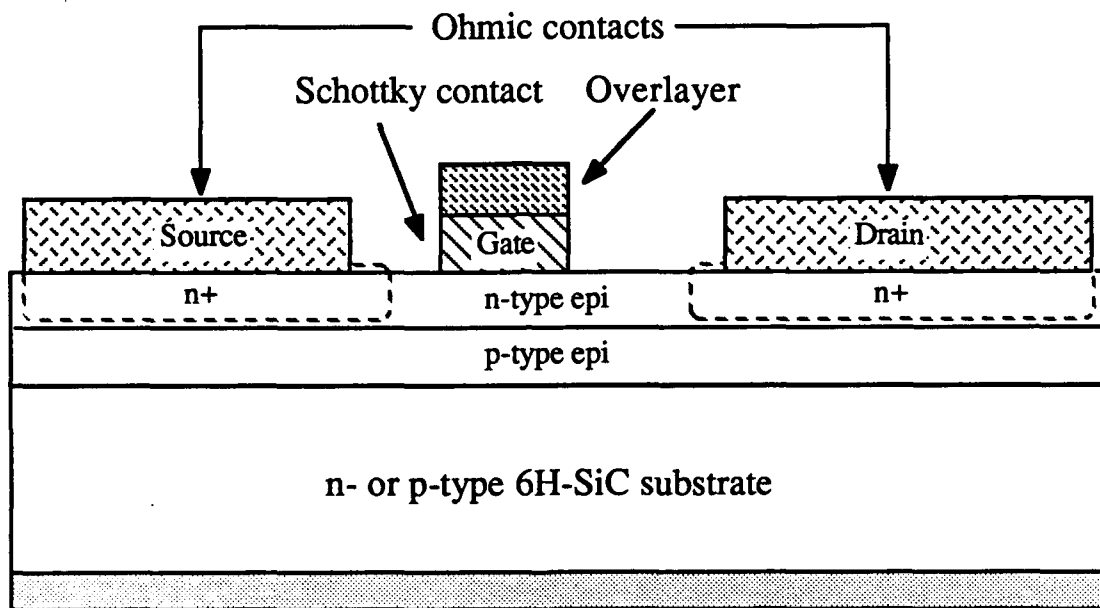

Figure 1: Cross-sectional view of 6H-SiC MESFET design utilizing ion implanted n$^+$ source and drain wells, and a buried p-type isolation layer.

The design for the high power-high frequency SiC MESFET is shown in Figure 2. This design uses a 1 mm gate width consisting of two 500 μm long gate fingers. Submicron gate lengths were used on this mask, varying from 0.6 μm to 1.0 μm. The gate - drain spacing was 1.6 μm to allow high drain voltages to be attained. The source - gate spacing was 1.1 μm for all of the devices except the smallest gate length, which had a 0.6 μm spacing. To keep the gate capacitance at a minimum, the gate contact pad area was kept to the minimum value (100 μm diameter) that still allowed reliable wire bonding. The source and drain contacts were made to n$^+$ source and drain wells that were formed via high temperature N$^+$ ion implantation, as was shown in cross-section in Figure 1. Finally, source and drain metal overlayers were used to facilitate better contacting for probing as well as wire bonding.
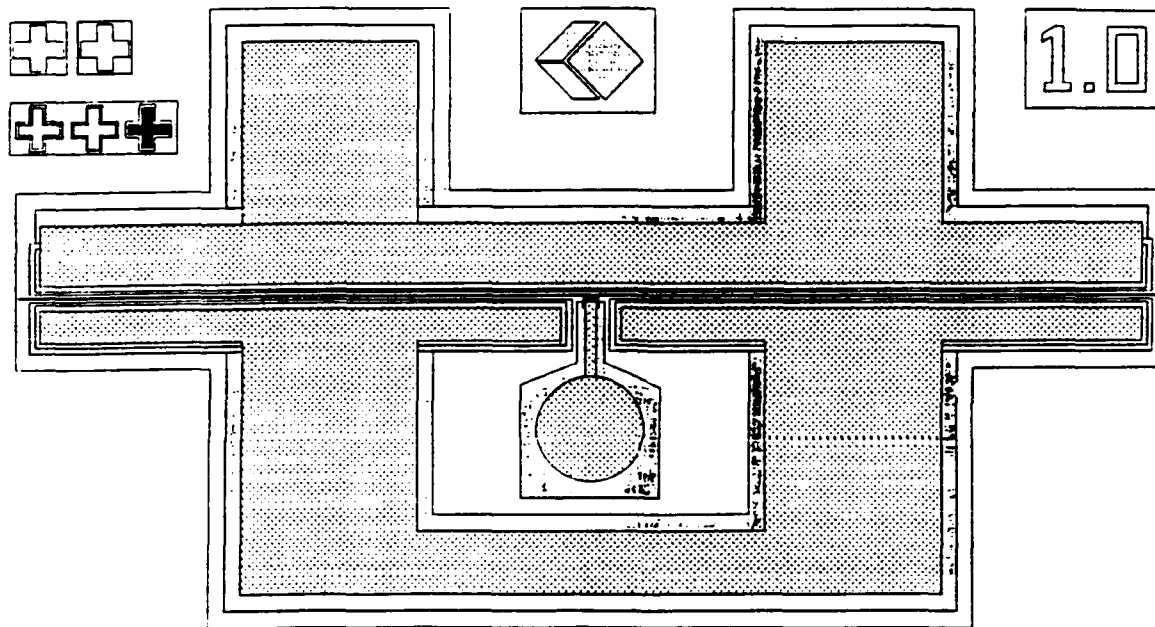
Figure 2: Design for high power / high frequency SiC MESFET. Gate lengths vary from 1.0 μm to 0.6 μm, and source-to-drain distances vary from 3.5 μm to 2.9 μm. The gate width is 1 mm.

The fabrication of these devices was as follows. The entire device was first isolated on a mesa. Using conventional photolithography techniques, a sputtered aluminum film was patterned onto the SiC surface, which acted as a mask for the reactive ion etching of the isolation mesa. The material around the mesa was etched sufficiently deeply to penetrate through the top n-type layer into the buried p-type layer. The Al was then stripped, and polysilicon was deposited and patterned. This opened windows for the source and drain pattern. The samples were then ion implanted with N^+ to form n^+ source and drain wells, using the polysilicon as the implant mask. The implants were subsequently annealed and the samples oxidized to grow a thin passivating layer of SiO_2. A 1.0 μm thick layer of SiO_2 was then deposited, using a low temperature chemical vapor deposition process, over the thin thermal oxide and was patterned to form the center gate contact isolation pad and interconnect bars. Windows for the source and drain contacts were then opened in the SiO_2 and the ohmic contacts were deposited and patterned using the "lift-off" technique. After these ohmic contacts were annealed, the fine line gate Schottky contact with overlayer was patterned using an excimer laser stepper. Finally, the gate contact pad metallization was deposited and patterned on the SiO_2 isolation pad.

One of the key steps in this process scheme was the gate lithography. A process was developed for achieving fine line lithography on SiC wafers using a GCA ALS LaserStep 200

(an excimer laser stepper) at the Microelectronics Center of North Carolina (MCNC) on a subcontract basis. This process, which used Shipley 8843-I deep UV photoresist, resulted in very good fine line lithography that allowed gate lengths as small as 0.6 μm to be developed.

Some of the devices utilized a mesa source and drain structure rather than using ion implantation. After epitaxial growth of the n-type channel layer, another n-type layer with heavy nitrogen doping was grown on top. This layer typically had a thickness of 0.2 μm and a doping of 1×10^{19} cm^{-3}. The source and drain were defined by reactive ion etching the n$^+$ layer except where the source and drain contacts were to go, using the same mask as was used for the ion implants. The insulator layers and gate contacts were then deposited on the etched back channel layer, just as was done for the devices previously discussed.

2. IMPATT Diodes

All of the IMPATT diodes that were fabricated during this reporting period used the "high-low" design for low voltage avalanche and were p-n junction based. These devices had the epitaxial structure for the breakdown layers as shown in Figure 3. The starting N-doped substrates were n-type with n = $1-3 \times 10^{18}$ cm^{-3}. The first epilayer, which served as the drift layer, was then grown with a thickness of 1.2 μm and a carrier concentration of $3-4 \times 10^{15}$ cm^{-3}. As was stated earlier, a lower voltage avalanche was desired; therefore, this layer was much lower doped than the previous IMPATTs. This layer was followed by a more heavily doped avalanche layer with a thickness of 0.22 μm and carrier concentration of $6-7 \times 10^{17}$ cm^{-3}. Finally, the p-n junction IMPATT wafers had a p$^+$ layer grown on them that was 0.5 μm thick. Because the emphasis of this batch was to reduce the p-type ohmic contact resistance, maximum Al doping was used. Thus the layers were too heavily doped to be able to measure with a mercury probe, but are assumed to have carrier concentrations at least as high as $1.5-2.5 \times 10^{19}$ cm^{-3}, as compared with the $p = 4-6 \times 10^{18}$ cm^{-3} doping level used in the previous devices.

The device fabrication for the IMPATT diodes involved first lapping the wafers to a thickness in the range of 150-200 μm thick by diamond grinding the backside of the wafers. The diode mesas were then formed via reactive ion etching using Al as the mask material. The mesas were etched through the epilayers into the n$^+$ substrate. The samples were then oxidized in wet O_2 to form a passivating layer of oxide on the mesa sidewalls. Using photolithography, windows were etched in the oxide for the topside ohmic contacts. The topside contacts were then formed on the front and backside of the wafer. Seven different diameter dots, varying from 38.1 μm to 381 μm, were used.
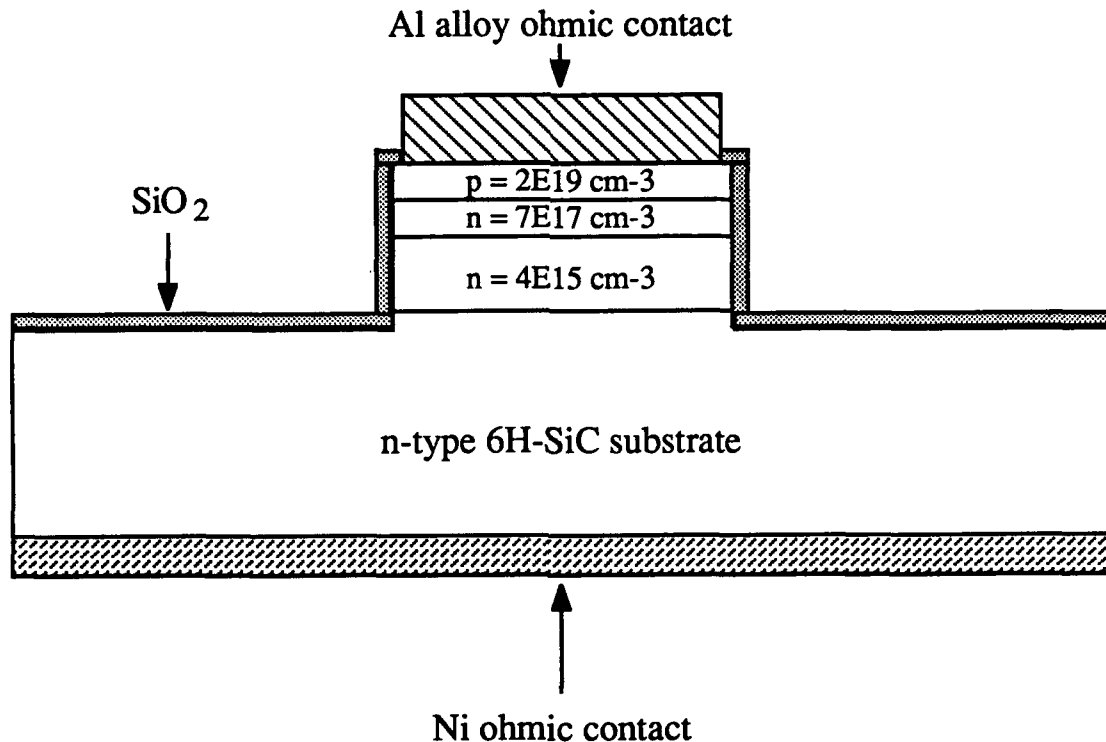
Figure 3: Cross-sectional view of p-n junction "high-low" IMPATT diode structure in 6H-SiC.

C. Results and Discussion

1. High Power / High Frequency MESFETs

The MESFET device characteristics previously reported showed good current saturation to 35 V. The maximum current for this device was only 50 mA, because the channel thickness was not as thick as it should have been, as evidenced by the pinch-off voltage of $V_G = -4.5$ V and the measured source-drain resistance of 67 Ω. Using a Cascade Microprober, the f_t and f_{max} of this device were measured to be 2.4 GHz and 1.9 GHz, respectively, and the power gain at 1.0 GHz was 7.0 dB.

In order to reduce the source resistance, the channel thickness of subsequent devices was increased, allowing pinch-off voltages of -10 V or more. Also, the best of the new wafers utilized ion implanted source and drain wells instead of the "mesa-style" MESFETs. It is assumed that the ion implanted wells result in a lower source and drain resistance because of the ability to dope to very high levels with implantation. Also, as mentioned earlier, a thicker gold overlayer (1 μm) was used to reduce gate resistance, and a thicker isolating SiO_2 layer (1 μm) was employed to reduce gate capacitance.

A typical current-voltage plot, obtained from a 60 Hz curve tracer, of one of these 6H-SiC MESFETs is shown in Figure 4. This device had a gate length and width of 0.6 μm and

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1 mm, respectively, and had a breakdown voltage at $V_D = 50$ V. The maximum transconductance of this device was about 25 mS/mm at $V_D = 40$ V and $V_G = 0$ V, and the measured channel resistance was 43 Ω. The gate leakage at $V_G = 0$ V and $V_D = 40$ V was about 350 μA. The drain on-current at $V_G = 0$ V (I_{DSS}) was 310 mA/mm with a pinch-off voltage (V_{po}) of $V_G = -17$ V. By achieving this I_{DSS} at $V_D = 40$ V, the corresponding DC power density of this device was 12.4 W/mm. This power level is two to three times higher than can be achieved with equivalent GaAs or Si devices.
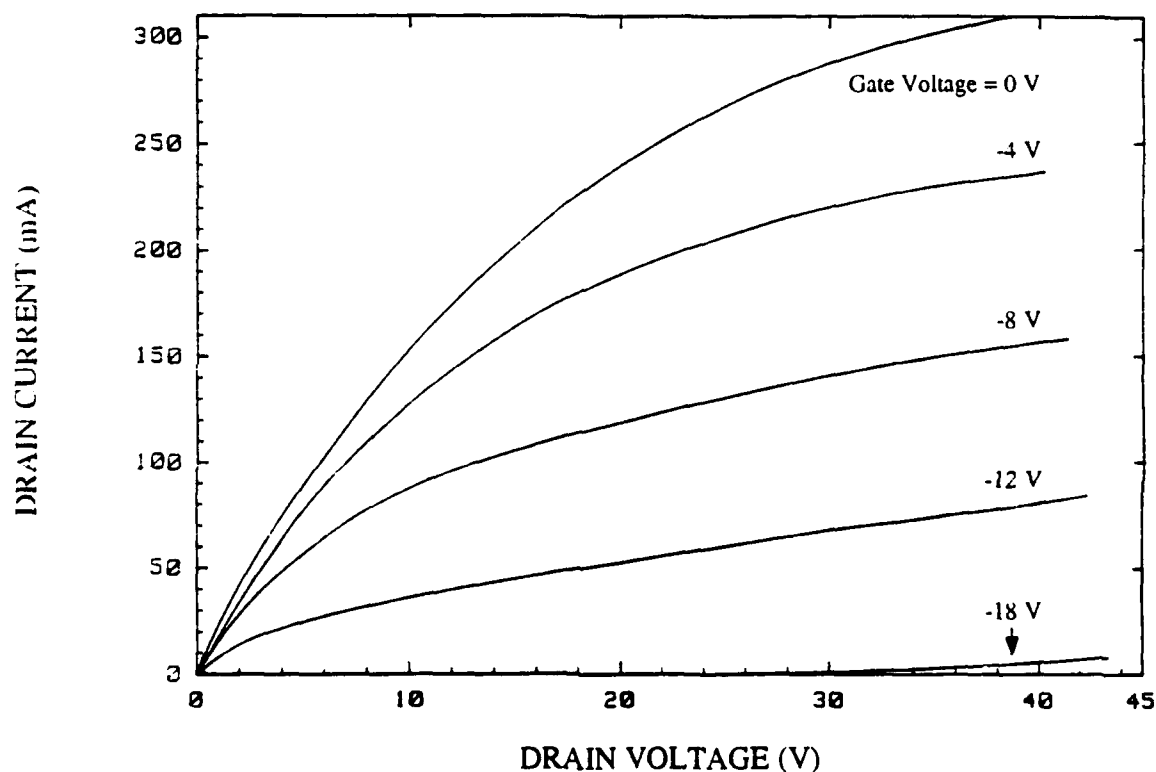

Figure 4:   Drain current-voltage characteristics (at 60 Hz) of a high frequency 6H-SiC MESFET using the structures shown in Figures 1 and 2. Gate length and width are 0.6 μm and 1 mm, respectively. Source-to-drain length is 2.9 μm.

This device was measured at high frequency using an HP 8510 automatic network analyzer with a Cascade Microprober for standard S-parameter measurements. The plot in Figure 5 shows that this device has a threshold frequency (f_t) of about 4.5 GHz, where the H_{21} parameter crosses 0 dB gain. The device has a maximum frequency (f_{max}) of about 3.0 GHz, where the power gain (G_{max}) crosses 0 dB gain. At 1.0 GHz, this device had a power gain and a current gain of 13.5 dB and 12.5 dB, respectively. While RF power measurements have not yet been performed on these devices, it is anticipated that significant RF power output will be achieved at 1 GHz.
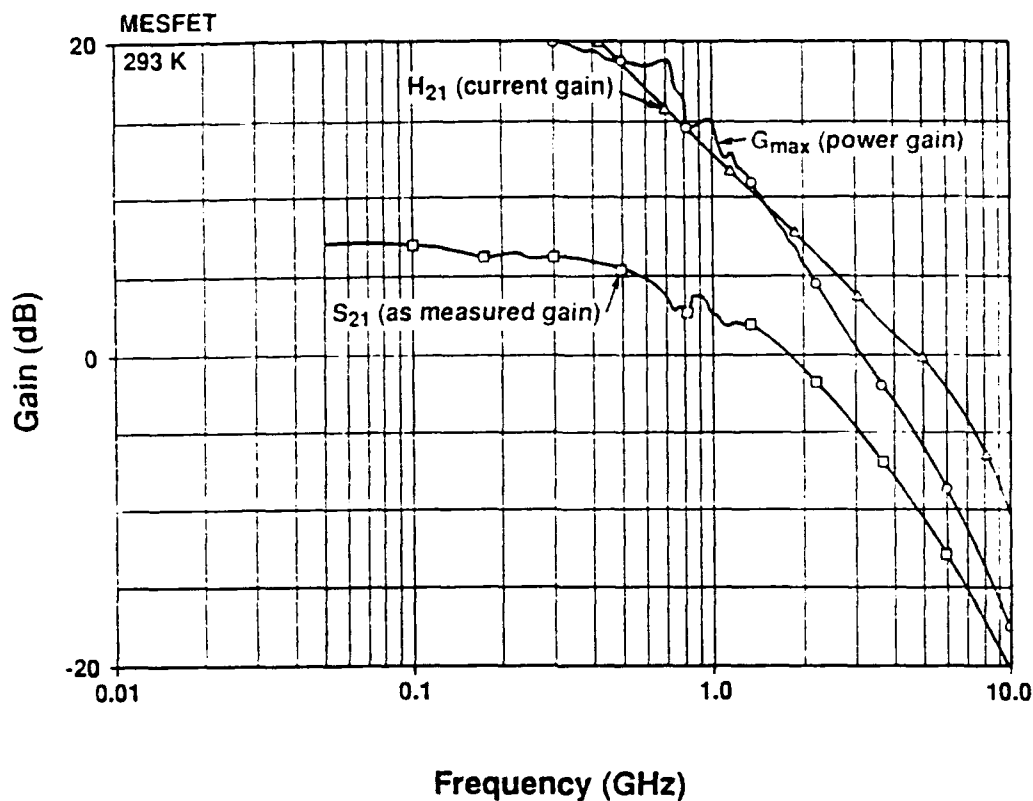
Figure 5: High frequency parameters, S_{21}, G_{max}, and H_{21}, as a function of frequency for the 0.6 μm gate length device shown in Figure 4. Measurement conditions were $V_D = 35$ V, $I_D = 260$ mA, $V_G = -3.0$ V, and $I_G = 258$ μA.

It is obvious from the I-V curves that these SiC devices can operate at extremely high drain and gate biases (40 V) for submicron devices as compared with the 5-10 V typically achievable with submicron GaAs devices. Therefore, it is easy to see that SiC MESFETs should be able to operate at much higher power levels than GaAs. While there are also marked improvements in high frequency operation, they are still somewhat lower than desired. However, the is still much room for improvement of the high frequency parasitics in these devices. The gate overlayers of these devices are still not sufficiently thick at 1.0 μm. Given the very small cross-section and the long finger length (500 μm), the series resistance along the gate fingers still have values in the range of 10-20 Ω. For GaAs MESFETs, it has been found that 10 Ω of gate resistance is a "critical" value to avoid serious parasitic effects, with a preferred value of 1.5 Ω. These low values of gate resistance are achieved by using thick overlayers of gold on top of the gate contacts, quite often employing techniques that enlarge the cross-sectional area (eg., mushroom gates). As such, future efforts for 6H-SiC MESFETs will be to further reduce the parasitic gate resistance by both reducing the gate finger length and by investigating mushroom gate technology.

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In order to further reduce the source resistance, the channel doping may be increased. As such, two new batches of wafers with channel doping in the range of $1.4\text{-}4\times10^{17}$ cm^{-3} have been grown. These wafers will be finished during the next reporting period. While these wafer batches will result in significant reductions in source resistance, a new device design is required to make a dramatic reduction in source resistance. A common method for greatly reducing the source resistance of GaAs MESFETs is to fabricate them with recessed gates. This is a method by which the channel layer is much thicker than normal, but is thinned to the proper thickness directly below the gate, keeping the source-gate cross-sectional area much larger. This structure should be particularly important for 6H-SiC because it allows one to compensate for the relatively low electron mobility.

Therefore, a batch of wafers was grown during the previous reporting period with which to fabricate some recessed gate 6H-SiC MESFETs. Two different channel thicknesses were used for the channel layer. Three were about 210 nm thicker than required and another three were 280 nm thicker than required. These wafers already contain ion implanted source and drain wells, and the ohmic contacts have been patterned and annealed. Preliminary tests on dummy wafers have been conducted with encouraging results. Recesses for the gates were reactive ion etched prior to the deposition of the gate metal. The test wafers showed that the majority of the gates were successfully patterned with submicron lines within the recess trenches. The real wafers will be attempted within the next month.

As discussed in the previous report, an attempt at packaging some high frequency MESFETs for RF power testing has been conducted. The devices were successfully diced with no degradation to the operating characteristics. Because of the high power levels at which the devices would operate, it was decided that the MESFETs should be brazed to the headers (standard ceramic microwave packages) as opposed to using silver epoxy. Unfortunately, the high temperature brazing process caused severe electrical degradation of the MESFET's I-V characteristics because of damage to the gate. Therefore, no RF power measurements were performed.

While this degradation phenomenon was discouraging, it was not altogether unexpected. We have also been developing MESFETs for high temperature operation at Cree under a different contract effort. In the course of this research, it was found that the gate metal must be annealed in order to avoid this degradation effect. After annealing, the gates are very stable at high temperature. The difficulty with the microwave MESFETs is related to the fact that these devices also have a gold gate overlayer that is deposited at the same time as the gate metal. Because of the fear of degrading the contacts via gold diffusion, we have not annealed the Schottky contacts on the microwave devices.

In order to determine the effect of annealing Schottky contacts with gold overlayers, a set of wafers were grown with n-type epilayers for making Schottky diodes. These large area

Schottky diodes were fabricated with and without gold overlayers. After annealing the Schottky contacts, the differences between the devices were characterized. From these results, it was determined that the Schottky contacts with gold overlayers could be successfully annealed without degradation of the contact quality. The gate annealing step will now be performed on one of the new higher power MESFET structures to confirm these experiments.

2. IMPATT Diodes

The p-n junction high-low IMPATT structures reported in the last period showed very low reverse bias leakage currents and a sharp avalanche breakdown with a negative resistance slope. The average leakage current at V = -80 V was 80 nA; at V = -50 V, the leakage current was about 2 nA ($J = 2.5\times10^{-5}$ A/cm^2). The avalanche current of this device at 90 V gave a corresponding avalanche power density of about 120 kW/cm^2. This is a very high power density, and it is expected that the junction temperature at this power level is quite high. Indeed, further increases in avalanche current began to degrade the performance of the device.

The forward bias I-V characteristics of the previous IMPATT diodes showed a turn-on voltage of about 2.6 V and had a forward current of 50 mA at about 3.5 V. Thus, the diode had a forward resistance of about 18 Ω, or 8.2×10^{-4} Ω-cm^2. Using known bulk resistivities and ohmic contact resistivities for 6H-SiC, the component of the resistance due to the substrate was calculated to be about 5.4 Ω. The p-type *ohmic contact resistance* was calculated to be about 9.0 Ω (2.2×10^{-4} Ω-cm^2) and the resistance due to the low doped drift region was about 3.0 Ω. Finally, the n-type ohmic contact was calculated to be about 0.6 Ω, resulting in a total resistance of 18 Ω. If a 6H-SiC IMPATT diode was fabricated with a thinned substrate and backside contact vias, then the substrate resistance could be ignored. However, the p-type ohmic contact resistance would contribute about 72% of the resistance.

Therefore the purpose of the next batch of IMPATT diode wafers was to greatly reduce the p-type ohmic contact resistance. The most obvious method of achieving lower contact resistance was to increase the p-type doping level. If the carrier concentration of the p$^+$ layer could be increased from the 5×10^{18} cm^{-3}, obtained with the previous diodes, a concentration to $>2\times10^{19}$ cm^{-3}, the p-type ohmic contact resistance would be reduced by a factor of about three.

The wafers that were grown for this batch did have very heavy Al doping such that the carrier concentration was in the range of $1.5-2.5\times10^{19}$ cm^{-3}. While the resulting devices were quite conductive, they unfortunately showed much poorer I-V characteristics than the previous batch. The leakage currents began to increase dramatically above 30 V reverse bias. No desirable avalanche characteristics were observed for any of the wafers that were fabricated.

It is assumed that the difference between this batch and the last one lies in the very high Al doping level. By going to very high Al levels, there is a correspondingly high concentration of Al in the thermally grown SiO$_2$. It is proposed that the Al concentration in the present batch

was so high that it degraded the insulating and passivating properties of the SiO_2 grown on the mesa exposed junction. Thus, a large amount of interfacial leakage current was generated at the junction around the periphery of the device when the reverse bias exceeded about 30 V.

D. Conclusions

High power / high frequency 6H-SiC MESFETs have been fabricated that show high gain at microwave frequencies, with the highest values for f_t and f_{max} being 4.5 GHz and 3.0 GHz, respectively. The measured DC power density was extraordinarily high, with a value of 12.4 W/mm. The main two parasitics that are currently limiting the high frequency behavior of these devices are source resistance and gate resistance.

Two different methods are being pursued to reduce the source resistance. These methods are 1) increasing the channel doping, and 2) use of recessed gate structures. Two different methods are being pursued to reduce the gate resistance. The first is to simply decrease the finger length by more than half. The second is to try to fabricate a "mushroom" style gate.

Attempts at reducing the p-type ohmic contact resistance of pn junction high-low IMPATT diodes were made by using very heavy Al doping. The devices showed much worse reverse bias leakage currents than the previous devices fabricated. It is assumed that the very high concentration of Al in the subsequently grown SiO_2 passivation layer resulted in poor passivating properties, which allowed a large amount of interfacial leakage current to be generated at the junction periphery.

E. Future Research Plans/Goals

The plans for the next period are to finish the device fabrication of the higher doped MESFETs and the recessed gate MESFETs that are in process. These devices will then be evaluated electrically with both DC and RF measurements.

Perhaps the most important project to be completed during the next period is to perform RF power testing on the SiC MESFETs. The first measurements to be made will be on the devices that were reported above. These devices will be RF power tested at the Naval Research Laboratories. This laboratory has a full RF measurement set-up that can also perform RF power testing at high temperature (up to 200°C) and reliability testing at 2.0 GHz. This RF testing will be performed during January 1992.

Because of the limited funds available as the end of this contract nears, it is unlikely that any more IMPATT diodes will be fabricated under this effort. The rest of the effort on this contract will focus instead on improving the frequency range of the SiC MESFET devices.