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# **MODULATION-BASED ULTRAWIDEBAND SELF-INTERFERENCE CANCELLATION (MUSIC)**

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**APRIL 2023  
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# 1 INTRODUCTION

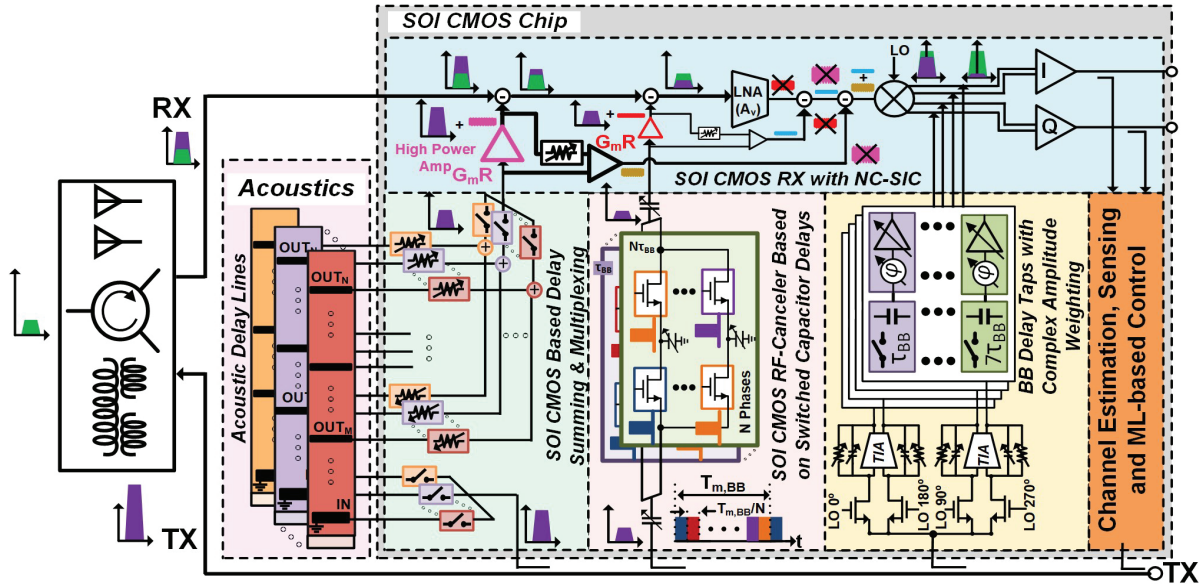


Fig. 1: System Architecture of the MUSIC Module

Simultaneous-transmit-and-receive (STAR) or full-duplex (FD) transceivers are challenged by the tremendous self-interference from the transmitter to the receiver. This self-interference (i) is typically 130dB larger than the desired signal, demanding very high levels of cancellation (SIC), (ii) undergoes substantial frequency dispersion due to long delay spreads in the self-interference channel, (iii) and is subject to changes in the electromagnetic environment, requiring adaptive cancellation. Consequently, despite research efforts over the past five years or so, including pioneering efforts by CoSMIC lab under PI Prof. Krishnaswamy over several DARPA programs such as RF-FPGA, ACT and SPAR, current solutions achieve insufficient cancellation over narrow bandwidths and consume substantial DC power while significantly degrading receiver noise. This effort attempted to leverage several breakthrough innovative concepts to propose a **Modulated Ultra-wideband Self-Interference Cancellation (MUSIC)** module that meets, and in several cases, exceeds the DARPA WARP metrics in both 0.1-1/1-6GHz bands, including:

1. **Quasi-electrostatic (Switched-Capacitor) Delay Lines:** that are wideband, highly-miniaturized, low-loss, fully-integrated in CMOS, and can support embedded voltage gain, enabling replication of the long delay spreads of the SI channel, allowing wide cancellation bandwidths, while relaxing the active gain requirements in the SIC path.
2. **Active Noise-Cancelled Self-Interference Cancellation (NC-SIC):** in which, the active RX-side cancellation circuit is able to cancel +10-20dBm SI levels while cancelling its own noise and distortion.
3. **Metamaterial/Switched-Resonator-Based Multi-port Delay Lines:** that are compact, low loss, operate in the 0.1-1/1-6 GHz ranges, respectively, and enable

transformative delay-bandwidth (DBW) products for acoustics, providing coarse high-linearity delay for the first-line-of-defense cancellation.

4. **Hybrid Analog-Digital Embedded Sensing and Machine Learning (ML)-based Control:** consisting of a wideband channel estimator with direct signal-to-feature conversion and an embedded neural processor that runs an ML/optimization model, which dynamically adapts the coefficients of the multi-domain FIR filter canceller in real-time.

## 2 WIDEBAND FIR CANCELLATION BASED ON CLOCK BOOSTED N-PATH STACKED-CAPACITOR DELAY LINES WITH HIGH LINEARITY

Realizing Full-duplex (FD) transceivers require suppressing high power levels of self-interference (SI) of the order of +0dBm down till -80dBm using SI cancelers which recreate the SI channel delay spreads while being able to provide high levels of output power matching that of the SI, with minimum noise figure penalty and real-time canceller adaptation. Previous implementations of SI cancelers based on frequency-domain equalization (FDE) [1] demand multiple widely-tunable power-hungry high-Q filters, while those based on FIR-based time-domain equalization (TDE) [2–5] require large delays with fine resolution. The canceler linearity is limited by the supply voltage of the technology and passive implementations of FDE and TDE cancelers require bulky inductors and long transmission lines respectively, which is not conducive to integration.

This work introduces utilizes an N-path switched-capacitor (SC) delay-line with stacked-capacitor voltage gain while enabling nearly ten nanoseconds of RF true-time delay across a large BW (DC-1GHz) and introduces (i) clock-boosted transmission gate switches to enhance the linearity of the RF Canceler (ii) a modified LNTA-canceler which absorbs the FIR weighting, summation, and output buffer requirements of the canceler into the LNTA with independent control over NF-linearity trade-off. We leverage programmable delays to realize a 11-tap RF canceler operating across DC - 1GHz with delays ranging from 0.25ps - 8ns and a complex-weighted 8-tap BB canceler with delays ranging from 10ns - 85ns.

### 2.1 Clock-Boosted N-Path Stacked-Capacitor Based Delay

Delays based on the sample-hold-and-release principle of SC circuits [4] can enable large delays ( $\propto 1/f_s$  over antialiasing  $BW=f_s/2$ ) within a compact area. By staggering the input (charging) and output (discharging) phases by  $90^\circ$ , a true-time delay determined by the clocks can be achieved. Additionally, the BW can be enhanced to  $Nf_s/2$  by using a time-interleaved N-path structure. Switch parasitics and rise/fall time of the clocks results in additional loss which is compensated by using capacitor-stacking to achieve passive voltage gain as in Fig. 2. For high input power levels, the VGS of the switch transistors varies significantly which could change the operation of the switch and modulates the switch resistance thus compromising the linearity of the RF Canceler. We propose utilizing transmission gate switches to alleviate this issue as the variation in the switch resistance is lowered. Further, we utilize a clock-boosting scheme to drive the switches with a higher voltage switch which improves the power handling of the switches significantly when used in tandem with transmission gate switches. The implementation of the RF Canceler is shown in Fig. 3



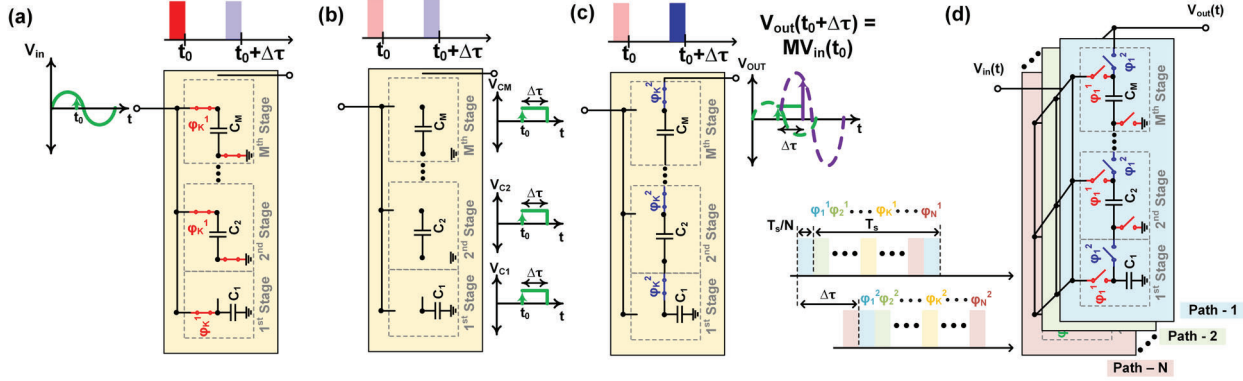


Fig. 2: Proposed N-path, switched-capacitor delay line with stacked-capacitor voltage gain

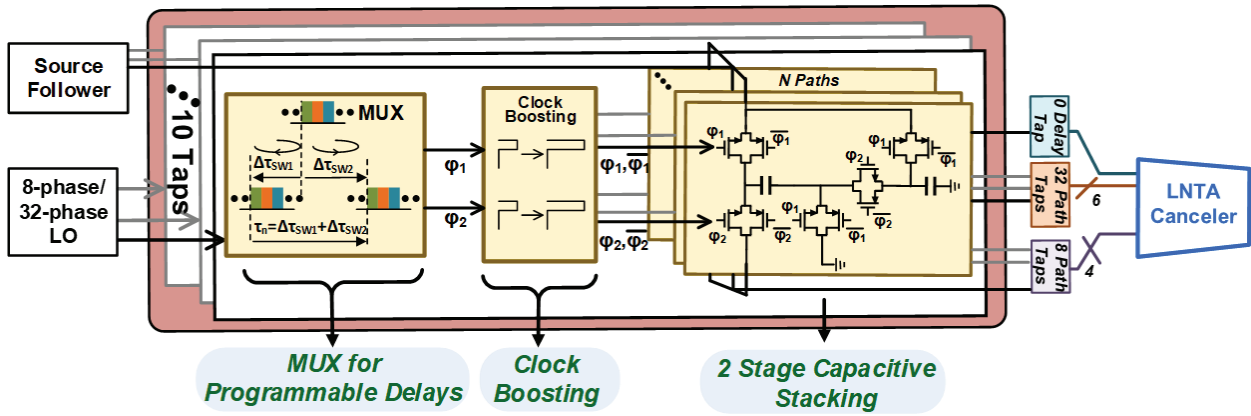
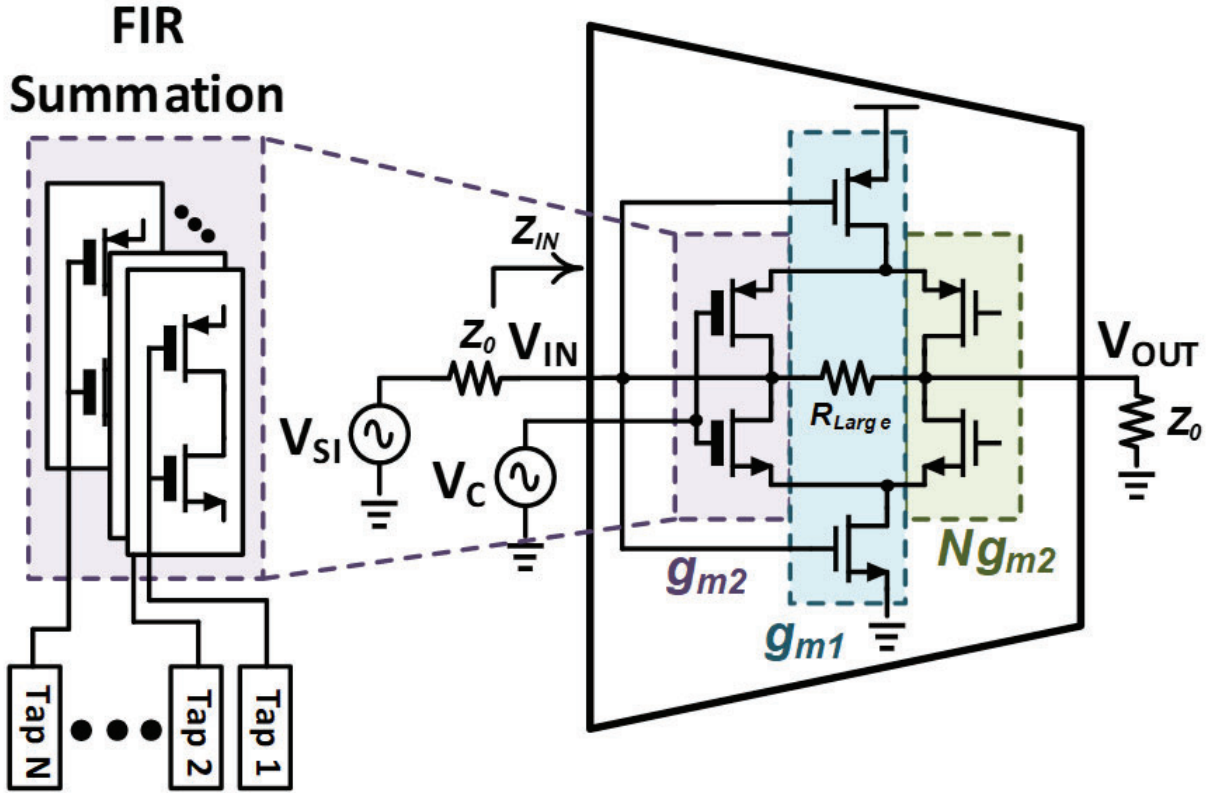


Fig. 3: Implementation of the Clock-boosted Stacked-capacitor Based RF Canceller with 1 Zero-delay Tap, 4 Low-delay, and 6 High-delay Taps

## 2.2 Integrated LNTA-Canceller

A TDE FIR canceler requires FIR weighting, summation, and injection into the RX. The LNTA-canceler [5] absorbs these functions into the LNTA, resulting in a lower NF by up to 1dB. The LNTA-canceler follows the partial-noise-cancelling LNTA, where a part of the current from the tail transistor is steered back to the RX input through a common gate (CG) device to provide wideband input matching and partial noise cancellation. Driving the gate of the CG device with an appropriately scaled SI replica results in a cancellation path which provides partial SI cancellation at the input of the LNTA of  $1/N$  (-15dB in our implementation), where  $N$  is the ratio of the output current to the steered-back current while providing complete suppression of the SI current at the LNTA output. The NF of the receiver is dependent on  $N$  and the transconductance of the CG device whereas the gain and linearity of the cancellation path is dependent on just the transconductance of the CG device. Each of the transconductances are individually tunable as they don't share any drain current and hence the FD receiver can be reprogrammed to trade-off the NF and linearity.

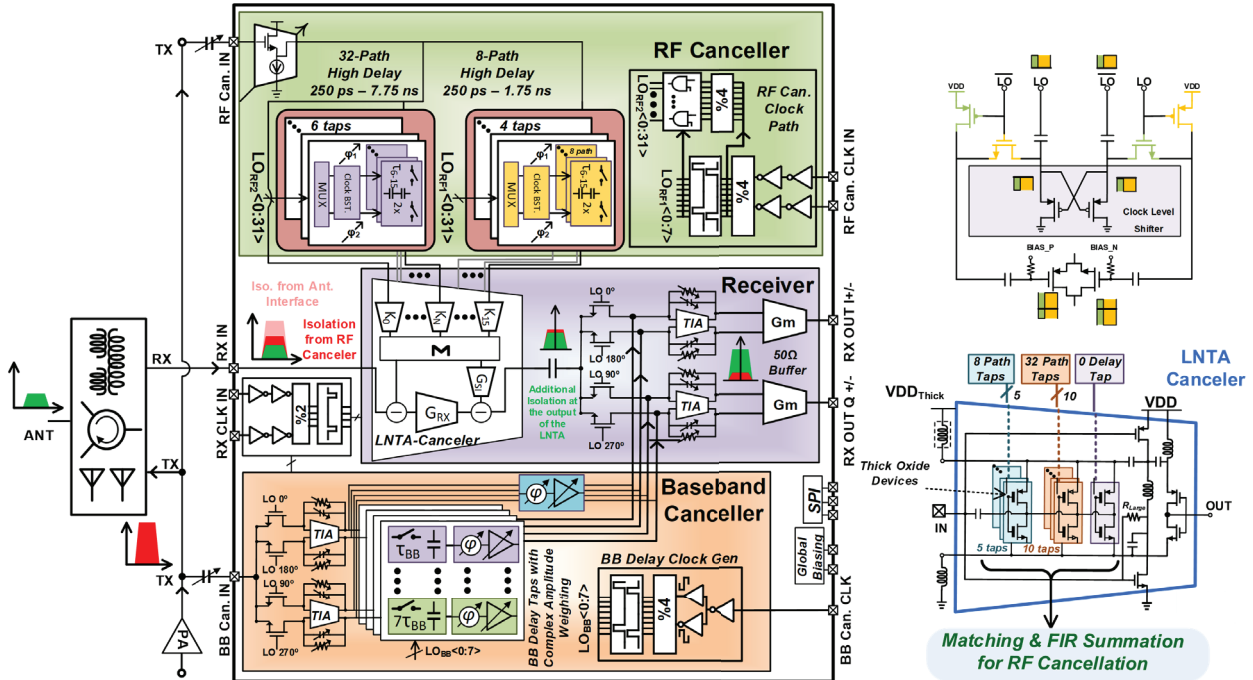


**Fig. 4: Conceptual Implementation of the LNTA Canceler Accomplishing FIR Weighting, Summation and Injection of the Cancellation Signal into the RX**

The CG device is split into 10 segments, whose gates are connected to the outputs of the delay taps. By segmenting and individually controlling these CG slices further, FIR weighting is achieved. At low SI levels, the weights are chosen for minimal NF degradation (low power (LP) mode). At high SI levels, larger weights are chosen for up to 6dB higher SI power handling in the RF canceler (high power (HP) mode) at the expense of additional 2dB NF degradation. The conceptual implementation of the LNTA-Canceler is shown in Fig. 4

### 2.3 Block Level Implementation

Fig. 5 shows the circuit diagram of the FD RX. TX power is capacitively coupled to the RF canceler, and then fed to the delay taps by source-follower buffers. System analysis reveals while the overall SIC is a function of both the canceler delay resolution ( $\Delta\tau$ ) and the maximum delay ( $N\Delta\tau$ ). However, only a fraction of the total N delays are used in any given situation as an increase in the number of taps leads to higher FIR losses. Therefore, we implemented a 11-tap RF canceler with 32 possible delay settings, namely 1 zero-delay tap, 4 low-delay, 4-path delay taps with  $F_{S,RF8}=500\text{MHz}$ , and 6 high-delay, 32-path delay taps with  $F_{S,RF32}=125\text{MHz}$ . Each of the 8-path (32-path) delays can be programmed to one of the delays ranging from  $T_{S,RF8}/8, \dots, 7T_{S,RF8}/8$  ( $T_{S,RF32}/32, \dots, 7T_{S,RF32}/32$ ), resulting in delays of 250ps - 1.75ns (250ps - 7.75ns).



**Fig. 5: Block Diagram of the Implemented CMOS Chip with Further Details on the Implementation of the LNTA Canceler and the Clock Boosting**

The 2-stage capacitive stacking results in a passive voltage gain of 5-2dB across DC to 1GHz for 8-path delays and 4-0dB for 32-path delays. Since capacitive stacking is more sensitive to parasitics, we implement 4 of the 6 32-path delays without capacitive stacking as the benefit from capacitive stacking deteriorates significantly at higher frequencies due to the higher parasitic capacitance for 32-path delays. The BB canceler consists of a 4-phase I/Q down-mixer, followed by I/Q BB TIAs. These are followed by 4-sets of 1 zero-delay tap and 7 8-path SC delay taps with increasing phase staggering resulting in delays ranging from  $T_{S, BB}/8, \dots, 7T_{S, BB}/8$ . Due to the low BB frequencies, these taps can be clocked at much lower frequencies (e.g. 10MHz) to realize large delays (12.5ns-87.5ns with 12.5ns step). The I/Q outputs of the BB delay taps are then passed to vector-modulators performing complex weighting, and are injected into the RX chain at the outputs of the RX mixers. The implemented 65nm CMOS FD receiver occupies a chip area  $8.8mm^2$ .

## 2.4 Measurements

Measurements of the RFIC are currently in progress, and unfortunately could not be completed by the end of the technical period of performance due to IC fabrication delays.

### 3 A MODULATION-DEFINED RF MICRO-ACOUSTIC DELAY LINE BASED ON SCALN MEMS RESONATORS FOR SELF- INTERFERENCE CANCELLATION

Achieving wideband SI cancellation requires emulating the frequency response of the highly dispersive SI channel for the entire bandwidth [1]. Thus, the canceller should also have a tunable and dispersive frequency response with sufficient group delay. Such a canceller can be implemented by having multiple delay taps with variable gain amplifiers (VGA) and phase shifters whose signals are combined to obtain a dispersive frequency response. The gains and phases of the VGAs and phase shifters can be tuned appropriately, realizing an FIR filter with a response matching that of the frequency response of the channel. Having large delays in the taps enables higher cancellations as they can capture the finer variations in the frequency response of the SI channel.

Conventional passive ladder delay-elements based on MEMS resonators [6], require frequency trimming between the series resonator and the shunt resonator resonance frequencies, typically in the few percent order, set by  $kt^2$ , leaving little design room for BW enhancement, as  $kt^2$  is typically set by MEMS mode excitation.

In this work, we propose a time-variant modulation-defined filter (MDF), capable of synthesizing a wide-band response with tunable group delay (GD) and fractionally low modulation frequency ( $f_m$ ), thanks to the strategic use of custom designed RF MEMS resonators, relaxing constraints on  $kt^2$  requirements for wide-band operation. As  $f_m \ll f_{res}$ , the circuit operation completely differs from N-path circuits [7,8], rather operating in a delay element region of operation for sequentially switched circuits.

#### 3.1 Methods

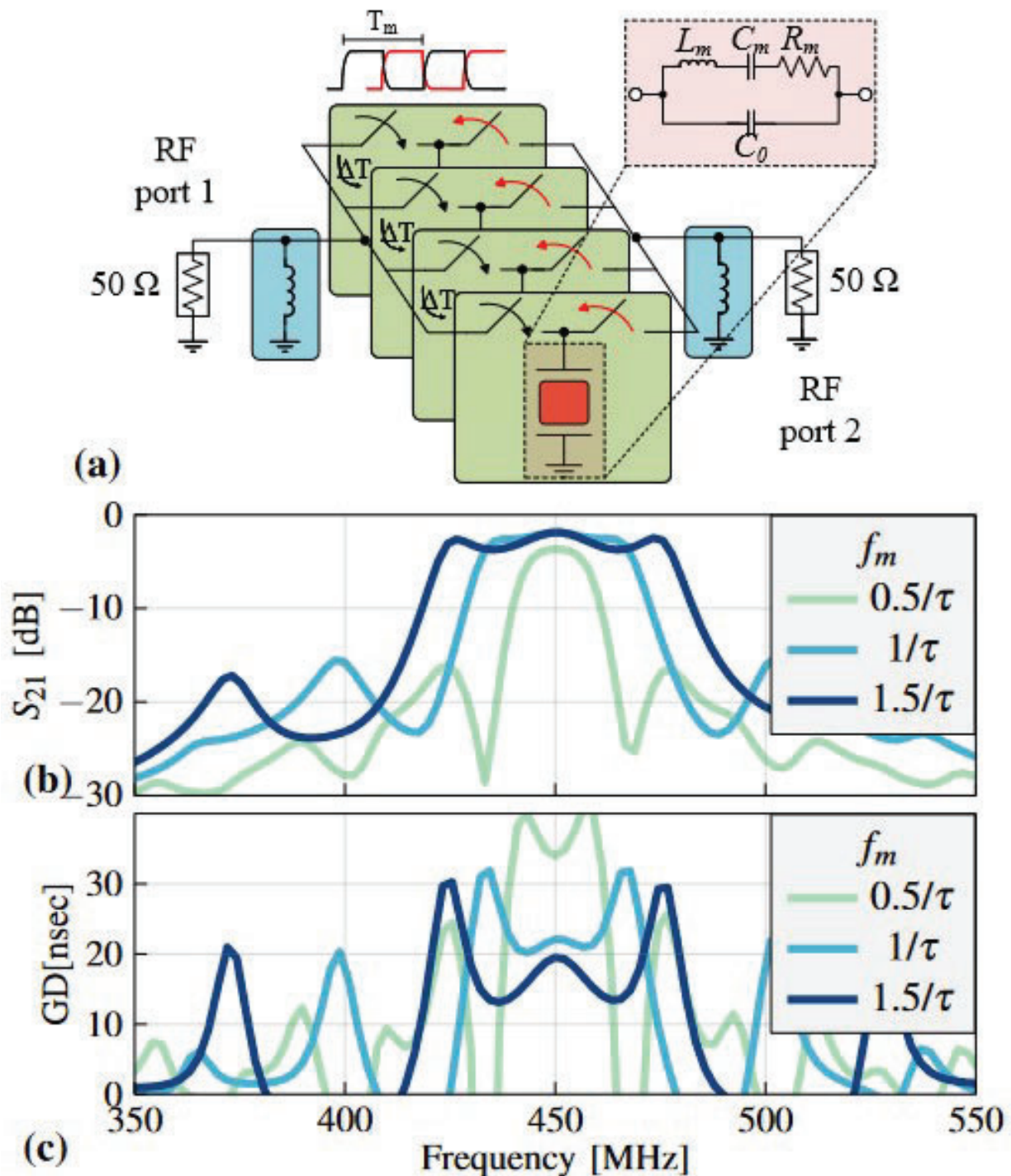
The schematic for the proposed Modulation-Defined Filter (MDF) is sketched in 6(a). An array of  $N$  cells is used to connect two RF ports through a periodic ON/OFF modulation pattern of series-connected switches, so that, within a modulation period  $T_m$ , a resonator with resonance frequency  $f_{res}$  is connected for a time  $DT_m$  (where  $D$  is the duty cycle) to port 1 and for a time  $(1-D)T_m$  to port 2. Each cell is driven with a clock skew  $\Delta T = 1/NT_m$  to achieve a symmetric operation with minimized distortion. As  $D=0.5$  for this work based on 4 cells, their phases overlap for  $T_m/4$  at each port.

The signal transfer through the modulated network exhibits artificial poles: for a signal at  $f_{res} \pm kf_m$ , part of the input spectrum will be up/down-converted to the passive pole at  $f_{res}$ , resulting in an overall signal transfer with an infinite set of poles at  $f_{res} \pm (2k+1)f_m$  obtained through modulation. In a similar way, transmission zeros are introduced at  $f_{res} \pm 2kf_m$ . Therefore, the proposed actuation scheme results in a dispersive delay line element, with a BW that is limited by the spacing of the first two artificial poles, so that

$$BW \approx 2f_m \quad (1)$$

For a given  $\tau$  (and damping rate  $f_{m,0} = 1/\tau$ ), one can show that a low IL can be reached at  $f_{res}$  for  $f_m > f_{m,0}$ . In fact, for  $f_m \ll f_{m,0}$ , the circuit will reach steady state for each clock period so that





**Fig. 6: Simulation Results for a 4-path MEMS based MDF Actuated with 50% Duty Cycle Signals Staggered by  $T_m/4$ . A Case Scenario Design using 4 Identical MEMS Resonators with  $k_t^2=3\%$ ,  $Q_m=600$ ,  $f_{res}=450\text{MHz}$ ,  $Z_m=50\Omega$  and  $R_s=2\Omega$  is Presented.**

*Based on the calculated passive risetime of, S-parameters are shown for  $f_m=8.6\text{ MHz}$ ,  $17.2\text{ MHz}$  and  $25.7\text{ MHz}$  (respectively  $0.5$ ,  $1$ , and  $1.5\tau$ ).*

no signal transfer will occur. For  $f_m \gg f_{m,0}$ , instead, in-band ripples become larger and larger, eventually setting an upper limit to the achievable BW. Therefore, the achievable characteristics of an MDF are mainly set by the resonator  $\tau$  when loaded by an RF port. For a discrete LC resonator,  $\tau_{LC} = 1/2/Q_L/\omega_{res}$ , where  $\omega_{res} = 2\pi f_{res}$  and  $Q_L$  is the loaded quality factor of the resonator [9]. Due to the low internal quality factors of inductor coils,  $Q_L$  below 10 leads to MDF with  $f_{ms}$  approaching 10 to 50% of  $f_{res}$ . Such high  $f_{ms}$  result in higher dynamic power consumption and reduced linearity, as well as ultra-wideband response 20 to 100% BWs, orders of magnitude higher than what required in channel-selective front-ends [10,11]. Conversely, the deployment of micro-acoustic MEMS resonators based on thin-film piezoelectric technology offer an exciting opportunity in this framework to synthesize lower fractional BWs, at reduced power consumption, maintaining high linearity and at the same time displaying interesting BW tunability features and wider BW than passive only MEMS-based ladder structures.

Starting from the conventional modified Butterworth-Van-Dyke model of piezoelectric MEMS resonators [12], it is possible to describe  $\tau_{MEMS}$  for resonant input stimulus

$$\tau_{MEMS} = \frac{Z_m}{Z_0} \frac{2}{k_t^2 \omega_{res}} \quad (2)$$

if  $R_m \ll Z_0$ , i.e. the resonator loss is negligible with respect to the RF port impedance. As shown, a low fractional bandwidth can be achieved thanks to the characteristic low-to-moderate  $k_t^2$  achieved with AlN and ScAlN piezoelectric film (ranging from 1 to 10% depending on Sc doping and excited acoustic mode [13]), and it can further be refined by proper resonator area sizing (i.e. via designing  $Z_m$ ).

Using the MEMS design parameters in 6, a 58 nsec risetime is calculated via 2 and used to set the  $f_m$  range used to drive a 4-path MEMS MDF with 50% duty-cycle. Obtained simulated S-parameters in 6-(b,c) show a clear BW widening mechanism as  $f_m$  increases, achieving tunable GD accordingly, at 2 to 6% fractional  $f_m$  for  $k_t^2=3\%$ .

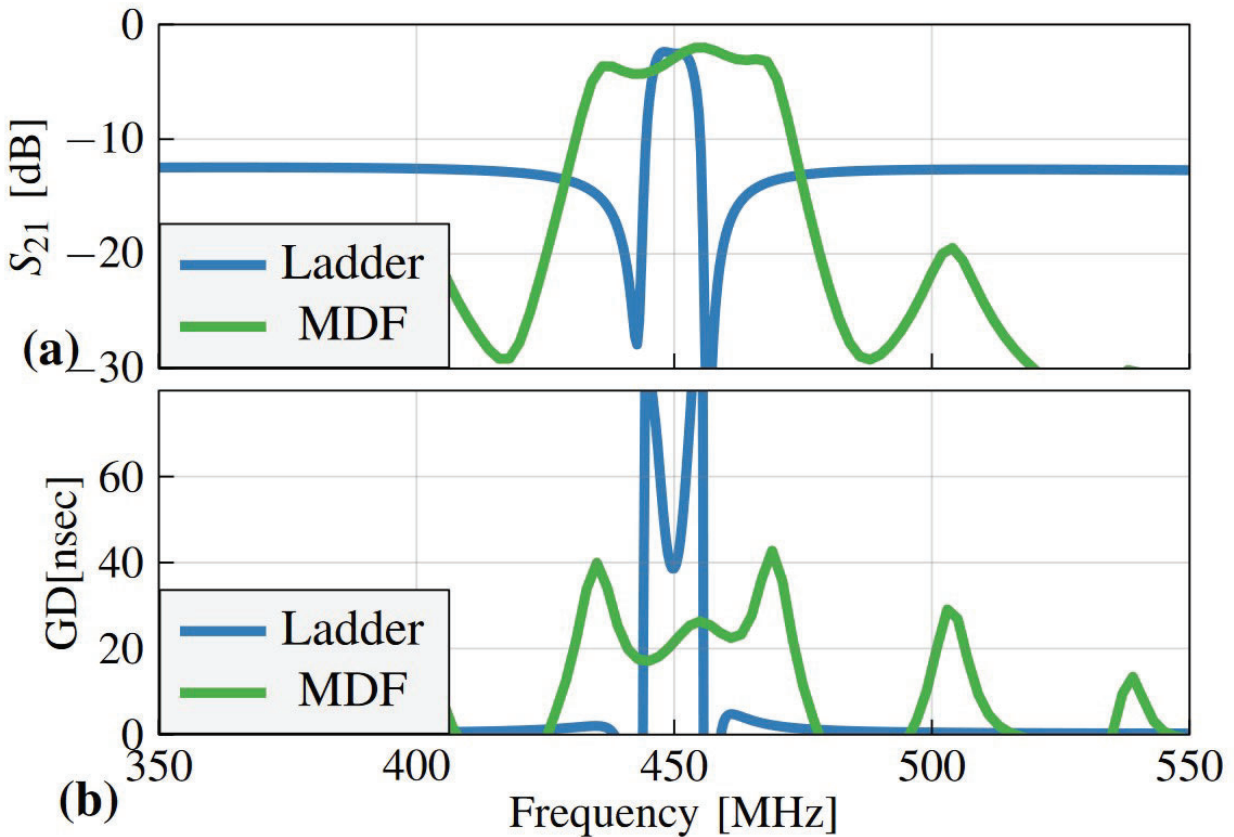
### 3.2 Design and fabrication of Grounded Bottom Electrode ScAlN MEMS resonator

An array of MEMS resonators on 30% Sc-doped AlN film devices were designed and fabricated. Due to current challenges in defining electrode patterns before ScAlN deposition, an unpatterned bottom electrode design [15] was chosen 8(e).

Despite inherent  $k_t^2$  degradation arising for poor lateral electric field coupling, a wide range of  $Z_m$  were achieved, realizing resonator with a static impedance  $Z_m=25\Omega$  at 430MHz with overall very minimal electrode loading (8(f)).

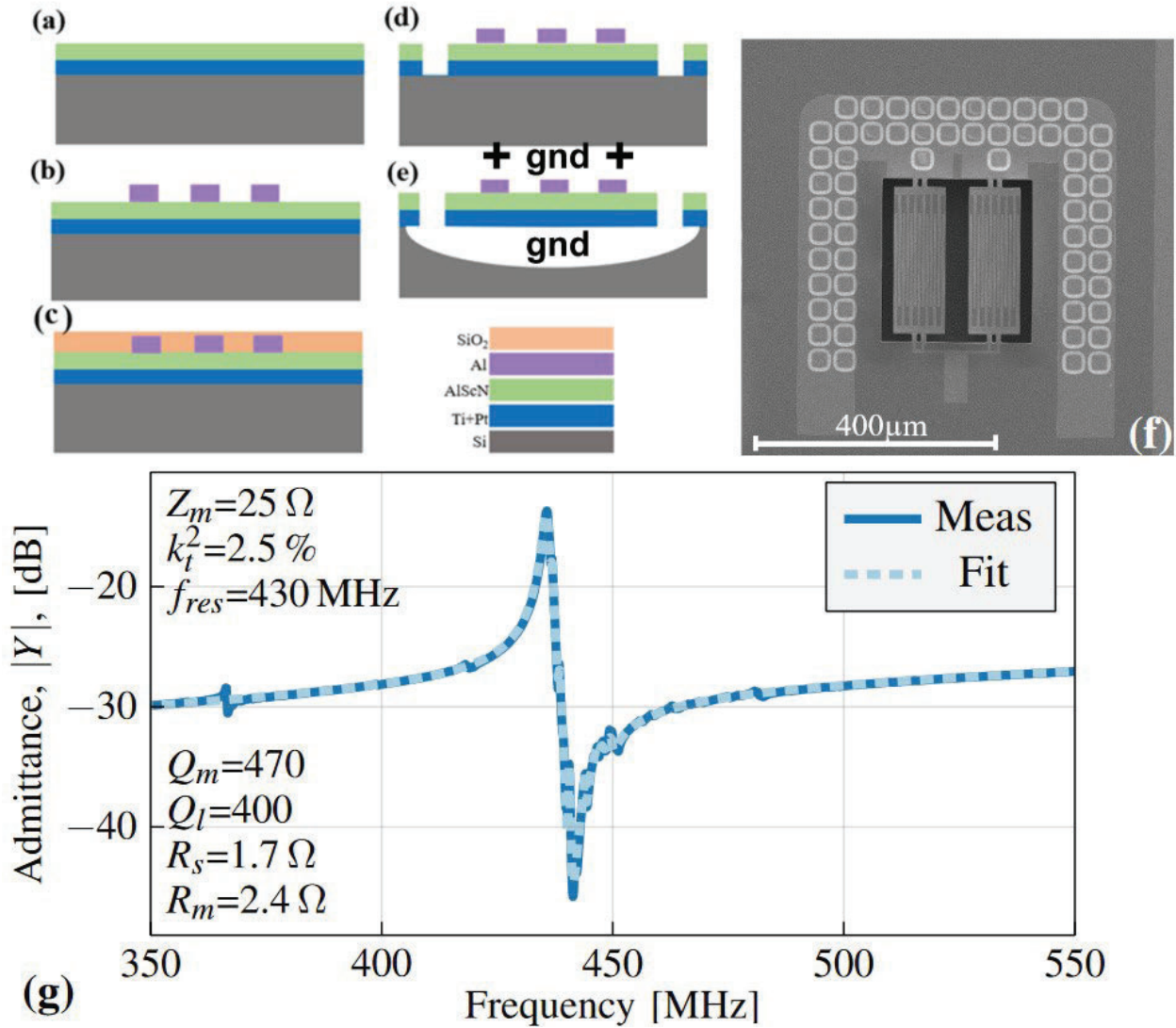
Resonators were built using a 4-mask fabrication process, as shown in 8(a-e). First, 10 nm of Ti and 100 nm of Pt were sputter deposited to form bottom electrode, followed without breaking vacuum by sputter deposition of AlScN with 28% Sc and thickness target of 500nm 8(a).

Rocking curve scan revealed  $1.8^\circ$  FWHM, indicating good crystal quality. Vias were wet etched to connect bottom and top electrode followed by sputter deposition of 120nm thick Al top electrode (8(b)). Patterned SiO<sub>2</sub>(8(c)) layer was used as a hard mask for dry etching of AlScN trenches (8(d)).



**Fig. 7: Comparison of Conventional 4th order MEMS ladder Filter Topology with the Proposed 4-path MDF**

*The same resonator parameters of 6 are used, and identical resonator areas (leading to  $50\Omega$  resonators) are used for the ladder filter, showcasing comparable IL (considering a  $5\Omega R_{on}$  switch resistance), three-fold BW, higher rejection and smaller group delay (15nsec vs 60nsec at 450MHz) .*



**Fig. 8: (a-e) Fabrication Step of AlScN Resonator Fabrication, (f) SEM of Realized Device along with (g) Measured Admittance Response, Compared to Multi-modal mBVD fit of Resonator Performance, obtained with Custom Routine in [14]**

Finally, resonators were dry released in XeF<sub>2</sub> plasma (8(e)), resulting in devices in 8-(f), captured via scanning electron micrograph (SEM). A reduction of 20% in  $k_t^2$  is observed due to parasitic ground coupling to the bottom electrode in the device fixture, leading to a measured  $k_t^2 = 2.5\%$ . While admittedly degraded with respect to AlScN-on-Si devices [16, 17], this platform provided a quick turnaround resonator technology based on ScAlN, capable of high-capacity density and promising  $Q \approx 500$ . An arrayed version of these devices were arranged in a common ground configuration for dicing and heterogeneous integration with RF circuitry to realize the MDF.



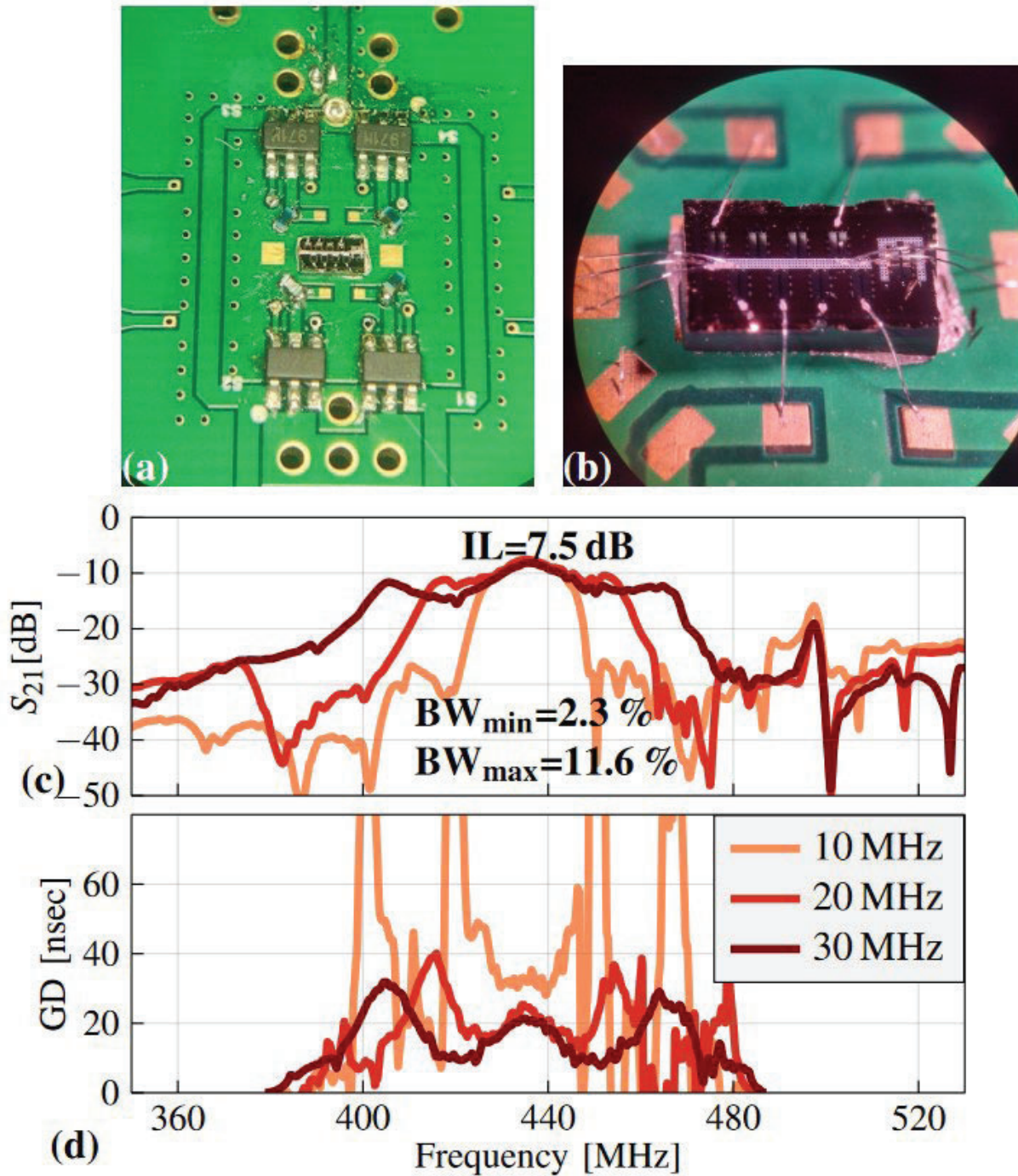
### 3.3 Experimental demonstration of MDF and SI cancellation

A high-power handling tunable delay line for adaptive SI cancellation, enabled by micro-acoustic technologies and operating in the low VHF range (between 400 and 500 MHz) was targeted for the DARPA WARP program [18]. The above-mentioned resonator array was diced and released in a 0.5mm×2mm die, die-attached and integrated via wire-bonds on a PCB with commercial SPDT switches by MA-COM™ [19] (9(a-b)).

A measurement campaign for the assembled PCB is shown in presented in 9-(c,d). The filter response is shown for various  $f_m$ , ranging from 10MHz (2.3% of  $f_c$ ) to 30MHz (7% of  $f_c$ ). The achieved IL=7.5dB is significantly degraded from 4dB foreseen for a MEMS resonator with  $FoM=12$ , due to the need for compensation inductors to minimize parasitic capacitance, as well as RF leakage from the SMD SPDT switch. 10dB RL is obtained in each state for the entire band. The MDF distortion was measured by capturing the output of the filter when a single tone at  $f_c$  (430MHz); the first and strongest couple of cross-modulation tones were measured at  $f_c \pm 4f_m$ , and a suppression of 28dBc was measured in the worst case, therefore preventing in-band distortion to corrupt SNR in practical channel-selection applications. An excellent 17dBm  $P_{1dB}$  input linearity is reported for this prototype, limited by MEMS device linearity, limited at  $P_{in} > 15dBm$ .

We experimented on the use of the prototyped MDF as an SI canceler, given the flexibility and the reduced power consumption (10s of  $\mu W$ ) obtained by the low-fractional  $f_m$  tunable-BW architecture, a wide range of GD and BW to cancel out TX-RX leakage in Full-Duplex systems [20].

An experimental setup was built where a TX signal is provided from the Port-1 of a Vector Network Analyzer (VNA) which is connected to the Port-1 of a COTS ferrite circulator with its Port-2 terminated by a conventional 50 $\Omega$  termination emulating a matched antenna and its Port-3 connected to the Port-2 of the VNA to capture the TX-RX leakage. A 10dB microwave coupler is used to couple 10dB of TX power which is split into two paths using a power splitter. These paths consist of a variable gain amplifier and phase shifter to control the gain and phase of these paths. One of the paths utilizes the MEMS resonator-based delay element to provide a delay spread between the two paths. The signals from both the paths are re-combined and are injected into the RX port using a 10dB coupler. The gains and phases of both the paths are optimized such that the SI is cancelled with the TX-RX leakage captured using the VNA is minimized thereby achieving 40dB SI suppression over 40MHz with at least 12dB arising from the micro-acoustic delay of the MDF.



**Fig. 9: (a-b) Details of the MDF Prototype, Built from a Custom 0.5x2 mm MEMS Chip, Die-attached and Wire-bonded to the PCB and Routed to 4 SPDT COTS RF MACOM Switches, (c-d)  $S_{21}$  and GD Recorded for Various  $f_m$  (GD Windowed Around 433MHz) A peak IL of 7.5dB is measured for resonators with  $FoM=12$ . The MDF realizes an outstanding BW tunability between 10 to 50MHz, based on resonators with  $k_r^2 = 2.6\%$ , achieved for a  $f_m/f_c = 2.3\%$ ,  $4.6\%$  and  $7\%$ , respectively.**

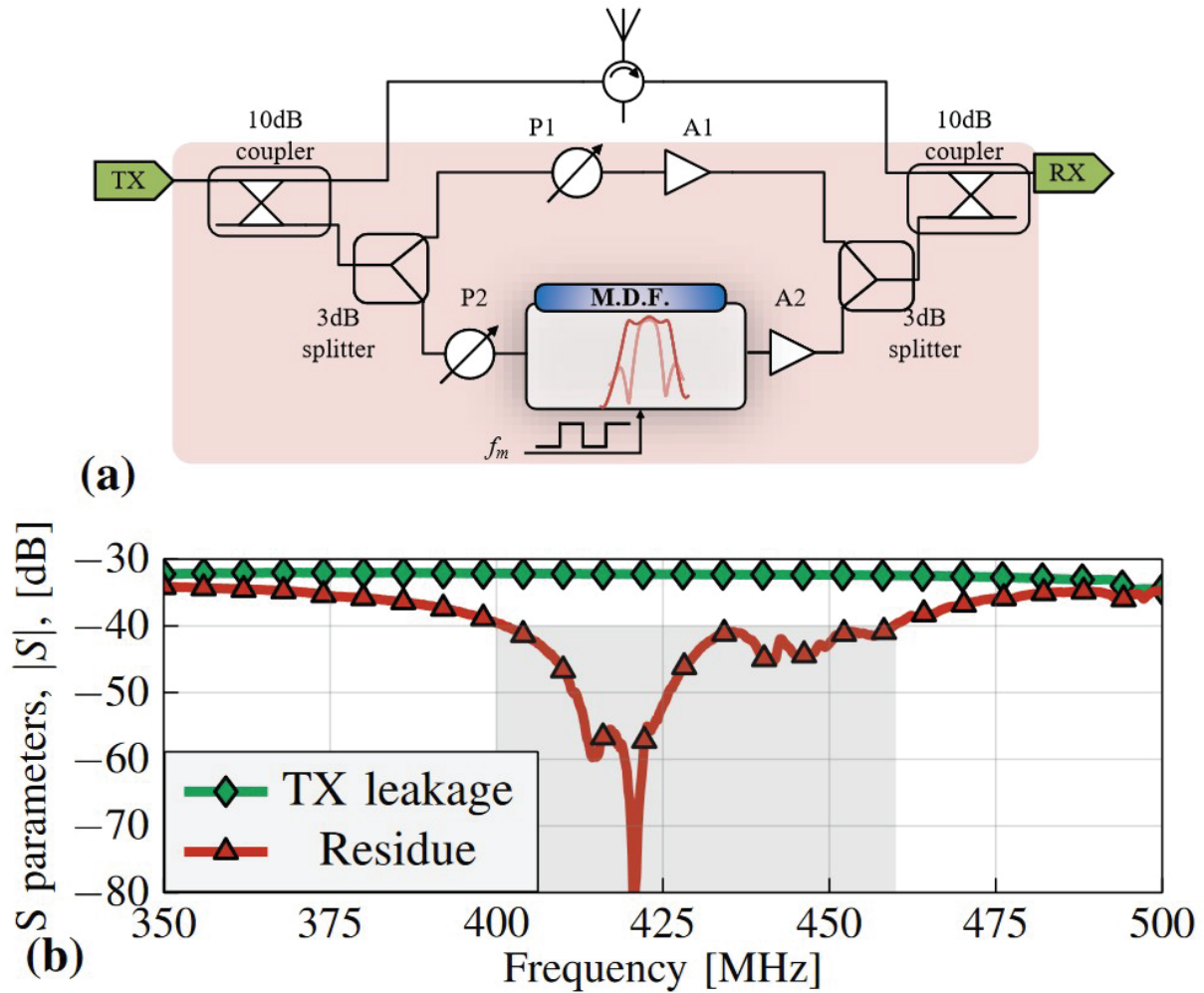


Fig. 10: (a) Proposed Schematic for Cancellation of Self-interference Signal Coming from TX Leakage Based on the MDF, (b) Measured Residual from the Proposed Experimental Setup

## 4 CONCLUSION

This project explored Quasi-electrostatic (Switched-Capacitor) Delay Lines, Active Noise-Cancelled Self-Interference Cancellation (NC-SIC), and Switched-Resonator-Based Multi-port Acoustic Delay Lines to meet the challenging DARPA WARP self-interference canceller metrics. Topics for future work include: 1) completion of the measurements of the CMOS self-interference cancelling IC to determine compliance with Phase 1 specifications, and 2) combining and acoustic-delay-line-based canceller with the CMOS self-interference cancelling IC to further improve performance and approach Phase 2 metrics.

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## LIST OF ACRONYMS, ABBREVIATIONS, AND SYMBOLS

<b>ACRONYM</b>	<b>DESCRIPTION</b>
STAR	Simultaneous-Transmit-and-Receive
FD	Full-Duplex
SIC	Self-Interference Cancellation
MUSIC	Modulated Ultra-wideband Self-Interference Cancellation
NC-SIC	Noise-Cancelled Self-Interference Cancellation
ML	Machine Learning
FDE	Frequency-Domain Equalization
TDE	Time-Domain Equalization
RF	Radio Frequency
SC	Switched-Capacitor
LNTA	Low Noise Transconductance Amplifier
NF	Noise Figure
LP	Low Power
HP	High Power
VGA	Variable Gain Amplifiers
GD	Group Delay
MEMS	Micro-Electromechanical Systems
MDF	Modulation-Defined Filter
BW	Bandwidth
SEM	Scanning Electron Micrograph
VHF	Very High Frequency
VNA	Vector Network Analyzer
TX	Transmit
RX	Receive
FIR	Finite Impulse Response