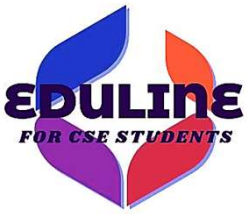
MODULE 1

INTRODUCTION TO 8086 MICROPROCESSOR

CO – Students will be able to summarize the architecture and modes of operations of 8086microprocessor.



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MICROPROCESSOR

- It is a program controlled semiconductor device, which fetches (from memory), decodes and executes instructions.
- It is used as CPU in computers
- Microprocessors consist of an ALU (Arithmetic Logic Unit), an array of registers and a CU(Control Unit).
- ALU performs arithmetic and Logical operations on data received from the memory or an input device. Register array consist of registers and accumulator. The control unit controls the flow of data and instructions with in the computer.

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- Microprocessor follows the sequence – Fetch, Decode and execute.
- Initially the instructions are stored in memory in a sequential order. The microprocessor fetches these instructions from memory then decodes it and executes those instructions till STOP instruction reached. Later it sends the result in binary to the output port. Between these processes , the registers stores the temporary data and ALU performs the computing functions.
- The microprocessor is identified with the size of the data, the ALU of the processor can work with at a time.
- The 8085 processor has 8 bit ALU , hence it is called 8-bit processor. The 8086 processor has 16 bit ALU and it is called 16-bit processor.

8086 MICROPROCESSOR

- First 16-bit processor released by INTEL in the year 1978
- 8086 is designed using HMOS (High density n-type Metal Oxide Silicon field effect Transistors) technology, and now it is manufactured using HMOS III technology, contains approximately 29,000 transistors.
- 8086 is packed in a 40 pin DIP (Dual Inline Package),and requires 5 volt supply.
- 8086 does not have internal clock circuit. The 8284 clock generator is used to generate the required clock for 8086.
- The maximum internal clock of 8086 is 5MHz.

- Other variations of 8086 with different clock rate are
  - **8086-1 : 10MHz**
  - **8086-2 : 8MHz**
  - **8086-4 : 4MHz**
- It consist of powerful instruction set , which provides operations like multiplication and division easily.
- It supports two modes of operations, that is maximum mode and minimum mode.
- Maximum mode is suitable for system having multiple processors and minimum mode is suitable for system having Single processor.
- It was the first 16-bit processor having 16 bit ALU, 16 bit Registers, internal data bus and 16 bit external data bus resulting in faster processing.

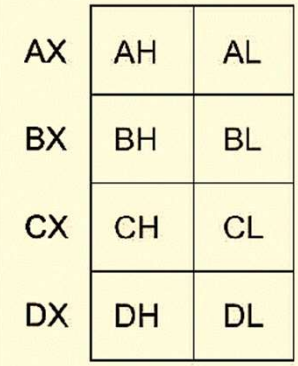
REGISTER ORGANIZATION OF 8086

- 8086 contains general purpose and special purpose registers. All registers are 16 bit registers.
- General purpose registers are used to holding data, variables and intermediate results temporarily.
- Special purpose registers are used as a segment registers, pointers , index registers or as offset storage registers for particular addressing modes.

a) GENERAL DATA REGISTERS

- The registers AX, BX, CX and DX are the general purpose 16 bit registers.

- AX is used as 16 bit accumulator, with the lower 8 bits of AX designated as AL and the higher 8 bits as AH.
- The letter L and H specify Lower and Higher bytes of a particular register.
- The letter X is used to specify the complete 16 bit register.
- The register BX is used as offset storage for forming physical address. Used as base register. Store starting base address of the memory area with in the data segment.

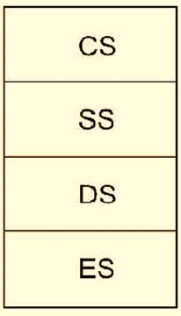


General data registers

- CX is used as a default counter (store loop counter)
- DX is used as an implicit operand or destination in case of a few instructions. (Hold I/O port addresses for I/O instructions)

b) SEGMENT REGISTERS

- Segment is a logical unit of memory. Minimum size of segment can be 16 bytes and maximum can be 64 KB.
- **CS – Code Segment Register**
- **DS – Data Segment Register**
- **ES – Extra Segment Register**
- **SS – Stack Segment Register**



Segment registers

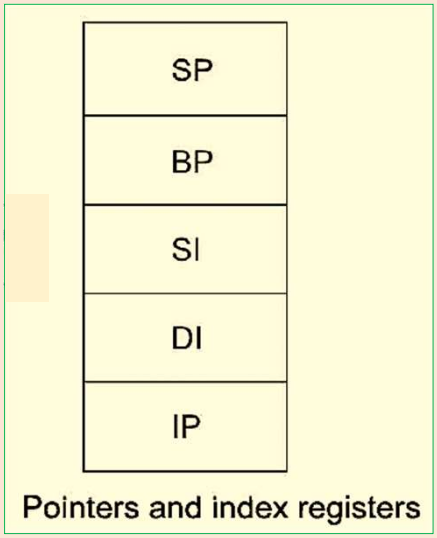
❖Segmentation

- Segmentation is the process in which the main memory of the computer is logically divided in to different segments and each segment has its own base address.
- It is basically used to enhance the speed of execution of the computer system so that the processor is able to fetch and execute the data from the memory easily and fast.
- **CS** contains the segment address for the code where the executable program is stored.
- **DS** points to the data segment of the memory where the data is stored.
- **ES** points to another data segment of the memory .It also contains data.

- **SS** is used for addressing stack segment of the memory. Stack segment is used to store stack data.
- The segment register hold the upper 16 bits of the starting address (base address) of 4 memory segments that 8086 is working with at any particular time.
- While addressing any location in the memory bank, the physical address is calculated from two parts. The first is Segment address, second is offset.
- Any of the pointers and index registers or BX may contain the offset of the location to be addressed.

c) POINTERS & INDEX REGISTERS

- Pointers – IP, BP, SP
- Index Registers – SI, DI
  - SP – Stack Pointer
  - BP – Base Pointer
  - IP – Instruction Pointer
  - SI – Source Index
  - DI – Destination Index



Pointers and index registers

- The pointer IP contains the offset with in the code segment.
- BP contains the offset with in the data segment
- SP contains the offset with in the stack segment
- Index registers are useful for string manipulations
- SI is used to store the offset of source data in data segment. DI is used to store the offset of destination in data segment or extra segment.

d) FLAG REGISTER

- Contains the results of computations in the ALU.
- It also contains some flag bits to control the CPU operations.

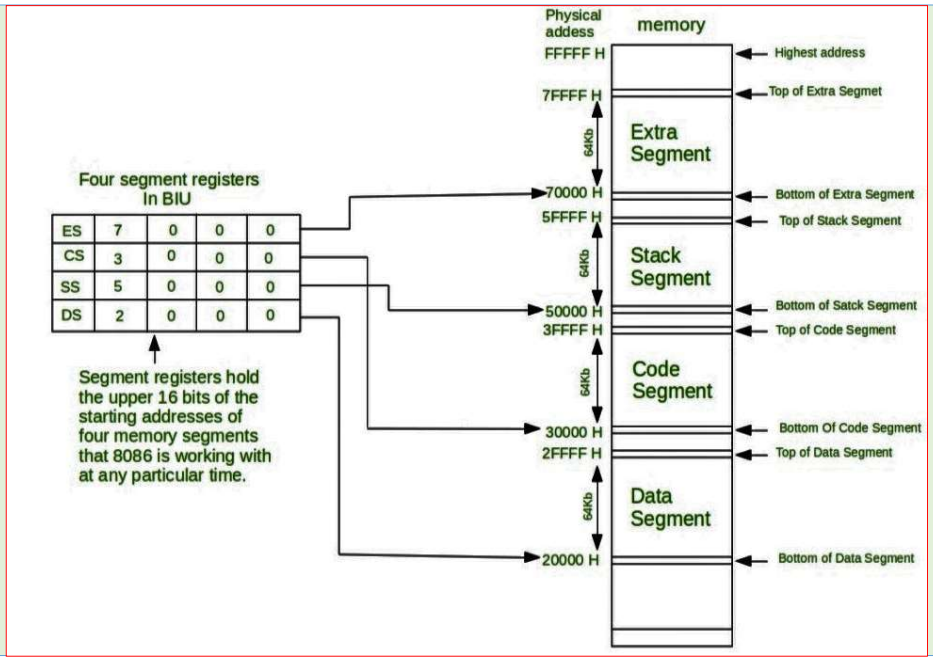
8086 ARCHITECTURE

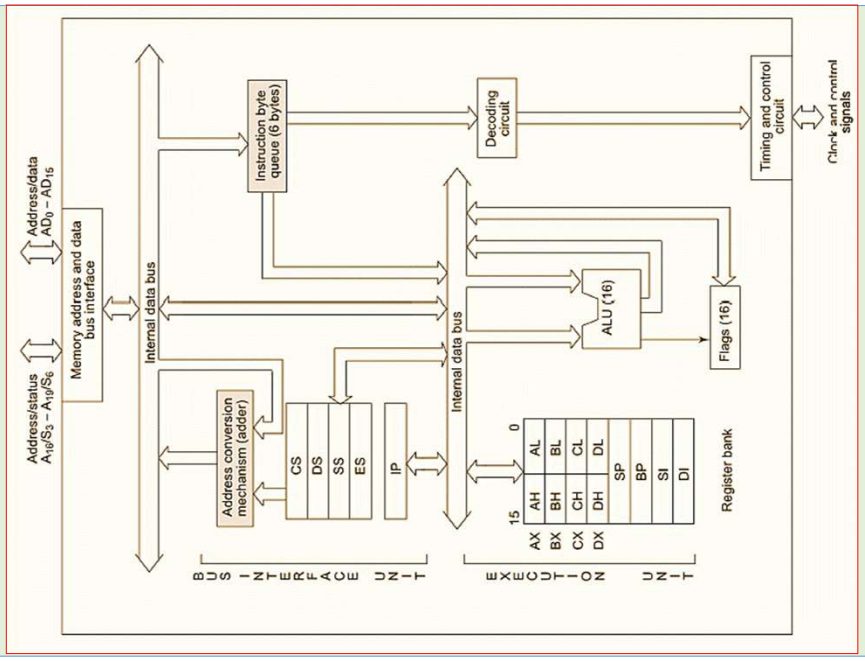
- 8086 provides 16 bit ALU , 16 bit registers and segmented memory addressing capabilities.
- 8086 has a rich instruction set , powerful interrupt structure.8086 has pipelined architecture.
- The architecture of 8086 can be internally divided into two separate functional units.
  - **Bus Interface Unit (BIU)**
  - **Execution Unit (EU)**
- The BIU fetch instructions , reads data from memory and I/O ports, write data to memory and I/O ports.

- The BIU contains the circuit for physical address calculations (address generation unit) , bus control unit, segment registers, Instruction pointer and instruction queue.
- The EU execute instructions that have already been fetched by the BIU. The BIU and EU functions independently.
- The instruction queue is a FIFO (First In First Out)group of registers. The size of queue is 6 bytes. The BIU fetches instruction code from memory and store in queue. The EU fetches instruction codes from the queue.
- BIU is responsible for establishing communication with external devices and peripherals including memory via bus.

- The complete physical address which is **20 bit long** generated using segment and offset registers ,each 16 bit long. The content of the segment register is called segment address and offset register content is called offset address.
- For generating a physical address, segment address is shifted left bit-wise 4 times, and to this result, offset address is added to produce 20 bit physical address.

Segment address	⟶ 1005H	
Offset address	⟶ 5555H	
Segment address	⟶ 1005H ⟶	0001 0000 0000 0101
Shifted by 4 bit positions	⟶	0001 0000 0000 0101 0000
	+	
Offset address	⟶	0101 0101 0101 0101
Physical address	⟶	0001 0101 0101 1010 0101
		1 5 5 A 5





- The segment register indicate the base address of a particular segment , while the offset indicate the distance of the required memory location in the segment from the base address.
- In execution unit 16 bit ALU performs arithmetic and logical operations. 16 bit flag register contains the result of execution by ALU.

❖Memory Segmentation

- To address a specific memory location, with in a segment we need an offset address. The offset address is also 16 bit long so that the maximum offset value can be **FFFFH** and the maximum size of any segment is thus ***64K*** locations.

- Two types of segments are overlapping segments and non-overlapping segments.

➢ **Overlapping Segment :** A segment starts at a particular address and its maximum size can go up to 64KB. But if another segment starts before this 64KB locations of the first segment , the two segments are said to be overlapping segments.

➢ **Non-Overlapping Segment :** A segment starts at a particular address and its maximum size can go up to 64 kilobytes. If another segment starts along with this 64Kbytes location of the first segment, then the two are said to be Non-overlapping segment.

❖Advantages of memory Segmentation

- It provide a powerful memory management mechanism.
- Data related or stack related operation can be performed in different segments.
- Code related operations can be done in separate code segments
- It allows to processes to easily share data.
- It allows to extend the address capability of a processor. Ie, segmentation allows the use of 16-bit registers to give an addressing capability of 1MB. Without segmentation it would require 20 bit registers.

❖FLAG REGISTER

- A flag is a flip-flop used to store the information about the status of the processor and the status of the instruction executed most recently. 8086 has **9 flags**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X	X	X	X	O	D	I	T	S	Z	X	Ac	X	P	X	Cy

O — Overflow flag
D — Direction flag
I — Interrupt flag
T — Trap flag
S — Sign flag
Z — Zero flag
Ac — Auxiliary carry flag
P — Parity flag
Cy — Carry flag
X — Not used

- **O – Overflow Flag** : This flag is set if an overflow occurs.
- **D – Direction Flag** : Used by string manipulation instructions. If this flag bit is 0, the string is processed beginning from the lowest address to the highest address (auto incrementing mode). Otherwise the string is processed from the highest address towards the lowest address (auto decrementing mode)
- **I – Interrupt Flag** : If this flag is set , the maskable interrupt are recognized by the CPU , otherwise they are ignored.
- **T – Trap Flag** : If this flag is set , the trap interrupt is generated after execution of each instruction.
- **S – Sign Flag** : This flag is set when the result of any computation is negative.

- **Z – Zero Flag** : This flag is set , the result of the computation is zero or comparison performed by the previous instructions is zero
- **Ac –Auxiliary carry Flag** : This is set if there is a carry from the lowest nibble.
- **P – Parity Flag** : This flag is set to 1 , if the result has even parity and the parity is cleared to zero for odd parity of the result
- **Cy – Carry Flag** : is set if there is a carry from the addition or borrow from subtraction.

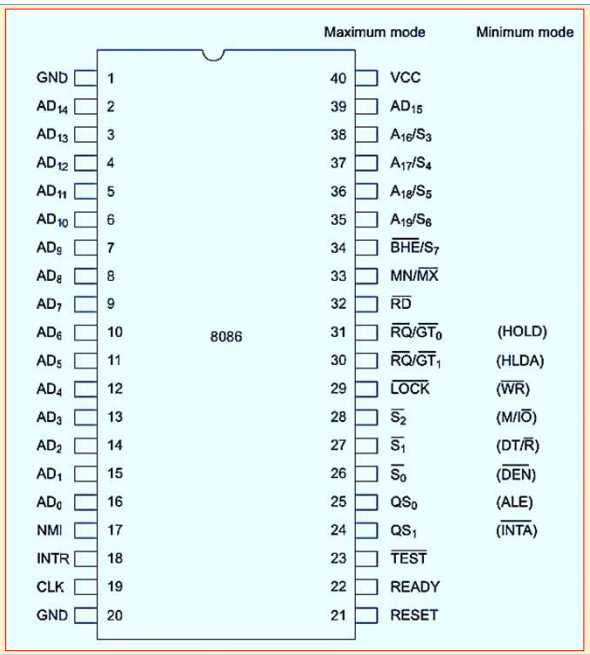
SIGNAL DESCRIPTIONS OF 8086

- The microprocessor 8086 is a 16 bit CPU available in three clock rates (5, 8 and 10 MHz) and it operate in a single processor and multi processor configurations, to achieve high performance.

➢**The signals can be categorized in to three groups**

1. Signals having common functions for maximum mode
2. Signals having special functions for minimum mode
3. Signals having special functions for maximum mode

❖**Pin configurations of 8086**



➢**AD_{15} - AD_0** : (Address/Data bus). These are 16 address data bus. AD_0 - AD_7 carries low order byte data and AD_8 - AD_{15} carries high order byte data. During the first clock cycle it carries 16 bit address and after that it carries 16 bit data.

➢**A_{19}/S_6 , A_{18}/S_5 , A_{17}/S_4 , A_{16}/S_3** : (Address/Status bus). These are the four address /status bus. During the first clock cycle , it carries 4 bit address and later it carries status signals.

A_{17} | S_4	A_{16} | S_3	Function
0	0	Extra segment access
0	1	Stack segment access
1	0	Code segment access
1	1	Data segment access

- **$\overline{BHE}$ / S_7 :** (Bus High Enable/ Status) . It is used to indicate the transfer of data using data bus D_5 - D_8. This signal is low during the first clock cycle , there after it is active.
- **$\overline{RD}$:** (Read) used to read signal for read operation. It is an out put signal . It is active when low.
- **READY :** This is an acknowledgement from the slow devices or memory that they have completed the data transfer. It is an active high (1) signal.
- **INTR :** (Interrupt Request). It is an interrupt request signal which is sampled during the last clock cycle of each instruction to determine if the processor considered this as an interrupt or not. This signal is active high and internally synchronized.

- **$\overline{TEST}$:** This input is examined by a **WAIT** instruction. If the TEST pin goes low (0), execution will continue, else the processor remains in an idle state.
- **NMI :** (Non Maskable Interrupt). This is an edge triggered input which causes a Type2 Interrupt. NMI is non maskable internally by software. This input is internally synchronized.
- **RESET :** It is used to restart the execution. It causes the processor to immediately terminate its present activity. This signal is active high and must be active for at least 4 clock cycles. RESET is also internally synchronized.

- **CLK** : (Clock Input). Clock input provides the basic timing for processor operation and bus control activity. It is an asymmetric square wave with a 33% duty cycle.
- **VCC :** Power supply (+5v DC)
- **GND** : Ground for the internal circuit
- **MN/$\overline{\text{MX}}$** : (Minimum/Maximum). This pin signal indicates what mode of the processor will operate in.
- **M/$\overline{\text{IO}}$** : (Memory/ IO) . This signal is used to distinguish between memory and I/O operations. When it is low it indicates the CPU is having an I/O operation. When it is high it indicates that the CPU is having a memory operation.

- **$\overline{\text{INTA}}$** : (Interrupt Acknowledge). When the microprocessor receives this signal, it acknowledges the interrupt. When it goes low it means that the processor has accepted the interrupt.
- **ALE** : (Address Latch Enable). This output signal indicate the availability of the valid address on the address/data line. This signal is active high. A positive pulse is generated each time the processor begins any operation.
- **DT/ $\overline{\text{R}}$** : (Data Transmit / Receive). It decides the direction of data flow through the transreceivers (bidirectional buffers). The signal is high when the data is transmitted and the signal is low when the processor is receiving data.

- **$\overline{DEN}$:** (Data Enable). This signal indicate the availability of valid data over the address/data lines. It is used to enable the transreceiver to separate data from the Address/Data bus.
- **HOLD :** This signal indicates to the processor that external devices are requesting to access the Address /Data buses.
- **HLDA** : (Hold Acknowledge). This signal acknowledges the HOLD signal.
- **$\overline{S_2}$, $\overline{S_1}$, $\overline{S_0}$** : (Status Lines). These are the status lines (signals) that provides the status of operation, which is used by the bus controller 8288 to generate memory and I/O control signals. Following table shows the status line.

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$\overline{S}_2$	$\overline{S}_1$	$\overline{S}_0$	*Indication*
0	0	0	Interrupt acknowledge
0	0	1	Read I/O port
0	1	0	Write I/O port
0	1	1	Halt
1	0	0	Code access
1	0	1	Read memory
1	1	0	Write memory
1	1	1	Passive

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➢ $\overline{\text{LOCK}}$: It is an active low pin. This indicate that other system bus masters will be prevented from gaining the system bus , while the lock signal is low.

➢ QS_1, QS_0 : (Queue Status). These signals indicate the status of the internal 8086 instruction queue according to the table shown below.

QS_1	QS_0	*Indication*
0	0	No operation
0	1	First byte of opcode from the queue
1	0	Empty queue
1	1	Subsequent byte from the queue

➢ $\overline{\text{RQ}}$/ $\overline{GT_0}$, $\overline{\text{RQ}}$/ $\overline{GT_1}$: (Request/Grant). It is used by other processors requesting the CPU to release the system bus. When the signal is received by CPU, then it sends acknowledgement. RT/GT_0 has a higher priority than RQ/ GT_1. Each of the pin is bidirectional.

MINIMUM MODE 8086 SYSTEM &TIMING

- 8086 is operated in minimum mode by strapping its MN/$\overline{MX}$ pin to logic 1.
- In this mode all the control signals are given out by the microprocessor chip itself. There is a single microprocessor in minimum mode system.
- The remaining components in the systems are latches, transreceivers, clock generator, memory and I/O devices.
- It has 20 address lines and 16 data lines , the 8086 CPU require three octal address latches and two octal data buffers for the complete address and data separation.

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❖**Latches:** They are generally buffered output D-type Flip Flops like 74 LS 373 or 8288. They are used for separating the valid address from the multiplexed Address/ Data signals and are controlled by the ALE signal generated by 8086.

❖**Trans-receivers :** They are the bidirectional buffers and some times they are called as data amplifiers. They are required to separate the valid data from the time multiplexed Address/Data signals. They are controlled by two signals namely $\overline{DEN}$ and DT/$\overline{R}$. The $\overline{DEN}$ signal indicate that the availability of valid data over the Address/Data lines. The DT/$\overline{R}$ signal indicate direction of data , ie from or to the processor.

- Usually EPROM are used for monitor storage, while RAM for users program storage

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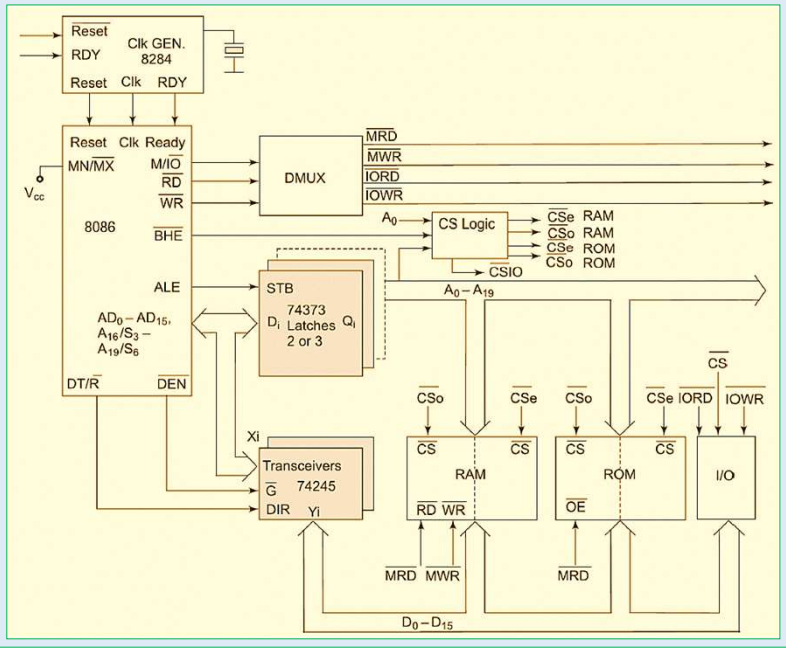
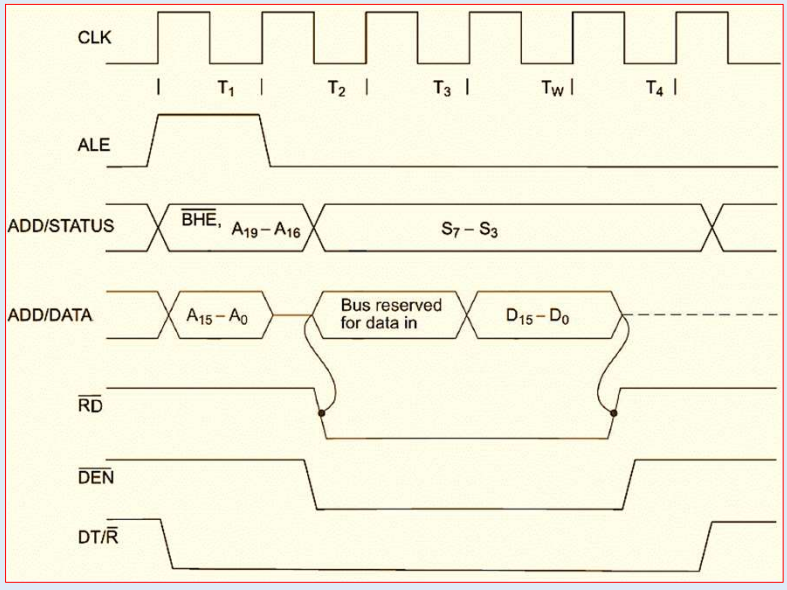


❖Read Cycle timing diagram for minimum mode



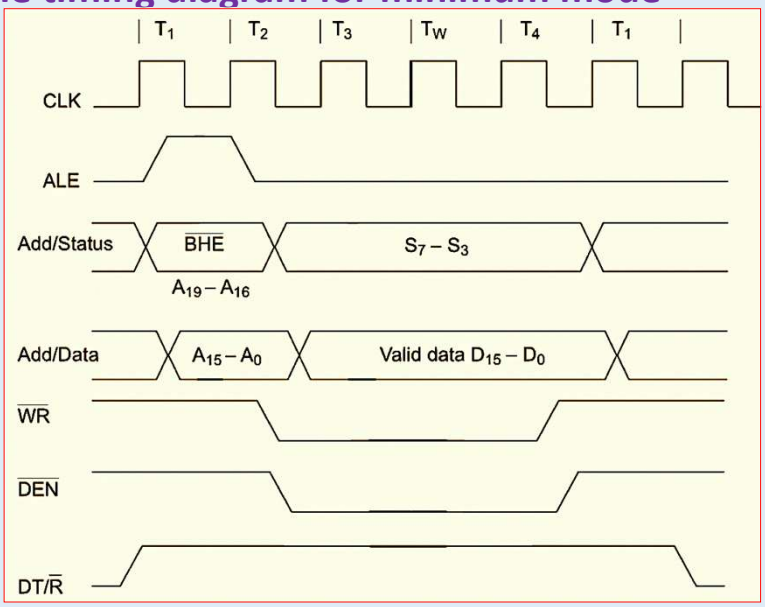
- T1 , T2 , T3 and T4 are clock pulse. One timing cycle having 4 clock pulse including waiting time Tw.
- During T1 clock pulse Address Latch Enable become high. So whenever ALE is high during T1 cycle , then we can send the address and data on to the bus
- During T1 clock pulse address will be active . During the remaining pulse the status will be active.
- During first clock pulse the address is placed on the address bus after that the data will be placed on the data bus (D_{15}-D_0). Here AD_0-AD_{15} is demultiplexed as A_{15}-A_0 and D_0-D_{15} . First address will be placed after that the bus is reserved for data in. ie, D_0-D_{15} during remaining clock pulse.

- $\overline{RD}$: [$\overline{RD}$ = $\overline{0}$= 1 (Active)] During T2 to T4 the data bus is active . So we are performing read operation.
- $\overline{DEN}$: [$\overline{DEN}$=$\overline{0}$=1 (Active)] Data Enable is also active during T2 to T4 clock pulse.
- DT/$\overline{R}$: Reading means receiving the data (R) and data transmitting (DT) is writing operation. To make $\overline{R}$ as active (1) we have to put 0

The M/$\overline{IO}$, $\overline{RD}$ and $\overline{WR}$ signals indicate the type of data transfer.

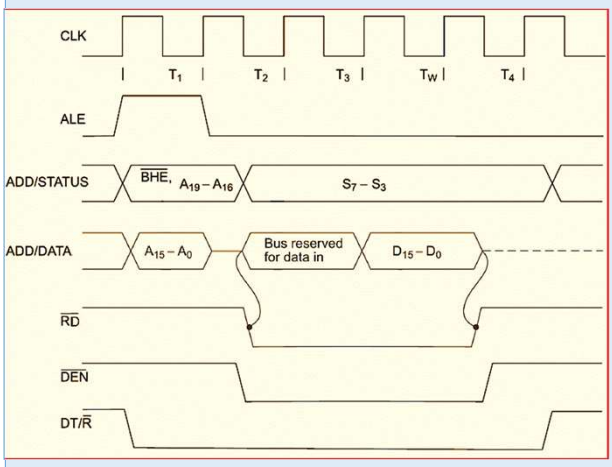
$M/\overline{IO}$	$\overline{RD}$	$\overline{DEN}$	Transfer Type
0	0	1	I/O read
0	1	0	I/O write
1	0	1	Memory read
1	1	0	Memory write

❖Write Cycle timing diagram for minimum mode

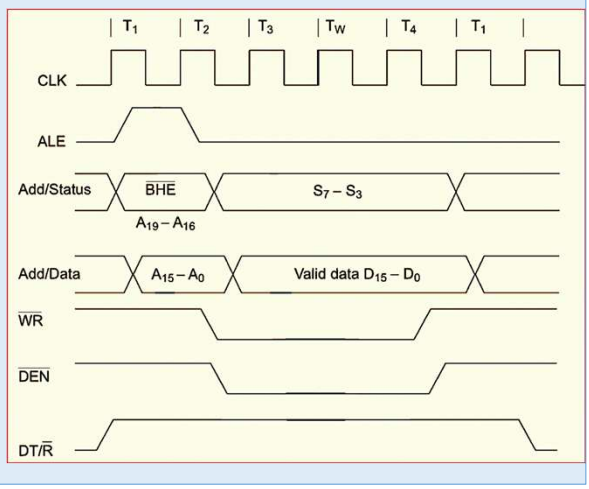


- Whatever the valid data that is placed on the data bus that we have to be write to the external devices.

READ



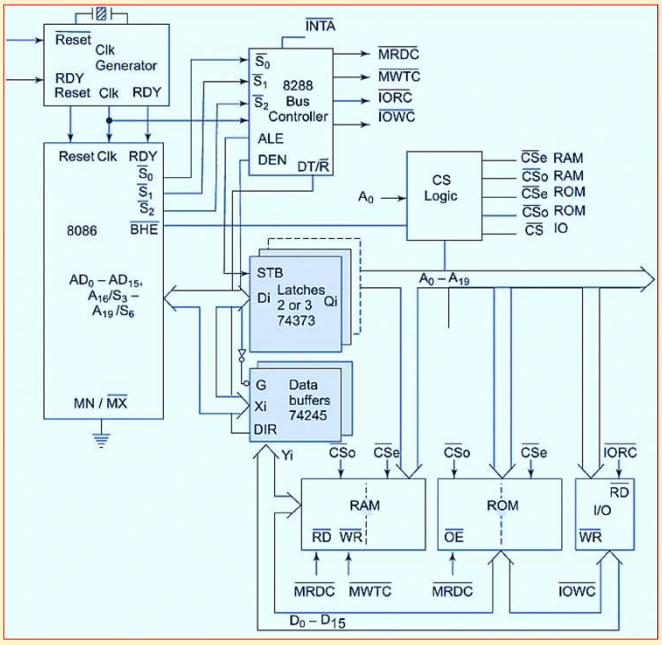
WRITE



MAXIMUM MODE 8086 SYSTEM

- In maximum mode 8086 is operated by strapping the MN/$\overline{MX}$ pin to ground (Logic Low)
- In this mode the processor derives the status signals $\overline{S_2}$, $\overline{S_1}$ and $\overline{S_0}$. Another chip called bus controller ,derives the control signals using this status information.
- In the maximum mode there may be more than one microprocessor in the system configuration.

❖Maximum Mode 8086 System

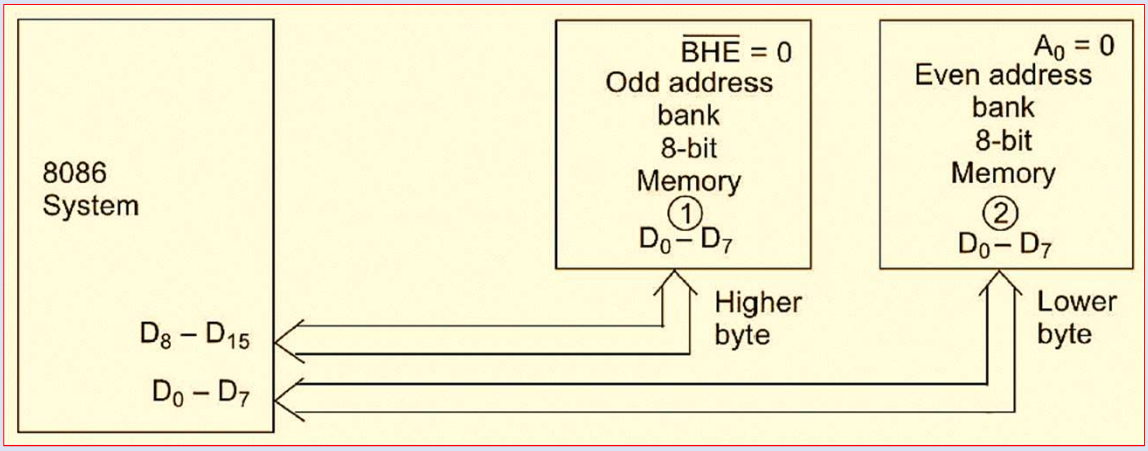


- The basic function of the bus controller chip **IC8288** is to derive control signals like $\overline{RD}$ and $\overline{WR}$, $\overline{DEN}$, DT/$\overline{R}$, ALE etc.; using the information made available by the processor on the status line.
- The $\overline{AEN}$, $\overline{IOB}$ and CEN pins are specially useful for multiprocessor systems. $\overline{AEN}$ and IOB are generally grounded. CEN pin is usually tied to +5v.
- The $\overline{IORC}$, $\overline{IOWC}$ are IO read command and IO write command signals respectively.
- The $\overline{MRDC}$, $\overline{MWTC}$ are memory read command and memory write command signals respectively.
- The CS Logic block represents Chip Select Logic. ‘e’ and ‘o’ represents Even and Odd memory bank

MEMORY ORGANIZATION

- In 8086 ,the 1 MB memory is physically organized as **odd bank** and **even bank** each of 512Kbytes.
- Byte data with even address is transferred on D_7-D_0 and Byte data with odd address is transferred on D_{15}-D_8bus lines.
- The processor provides two enable signals $\overline{BHE}$ and A_0 for selection of either even or odd or both the banks
- If the processor fetches a word (consecutive two bytes) from memory, the opcodes and operands are identified by the internal decoder circuit.

❖Physical memory organization



- It is better to locate word data at an even address. To read or write a complete word from/ to memory , if it is located at an even address , only one read or write cycle is required.
- If the word is located at an odd address the first read or write cycle is required for accessing the lower byte while the second one is required for accessing the higher bytes. Thus two bus cycle are required if a word is located at an odd address.
- If 8086 transfers a 16 bit data to or from memory , both of the memory bank must be selected for the 16 bit operation. The two signals A_0 and **BHE** solve the problem of selection of appropriate memory bank as presented in the following table.

- Certain locations in memory are reserved for specific CPU operations. The location **FFFF0H to FFFFFH** are reserved for jump to initialization programme and I/O processor initialization.
- The location **00000H to 003FFH** are reserved for interrupt vector table.

$\overline{BHE}$	A_0	Indication
0	0	Whole word (2 bytes)
0	1	Upper byte from or to odd address.
1	0	Lower byte from or to even address
1	1	None.

COMPARISON OF 8086 &8088

8086	8088
• It has 16 bit data bus • It can read or write 8/16 bit data at a time • Memory space is organized as two 512KB (2×512KB = 1 MB) banks • It can operate at three clock speed , ie ; 5MHz , 8MHz and 10MHz • Instruction queue is 6 bit long • It has BHE pin • It draws maximum supply current of 360MA	• It has 8 bit data bus • It can only do so for 8 bit data • It is implemented as a single 1MB bank • It is available only in two clock speed , ie; 5MHz and 8MHz • Instruction queue is 4 bit long • This pin is replaced by status output (SSO),since it can read or write only 8 bit data • It draws maximum supply current of 340MA

8086 MACHINE LANGUAGE INSTRUCTION FORMAT

- A machine language instruction format has one or more number of fields associated with it.
  - The first field is called as operation code field or op-code field, which indicates the type of operation to be performed by the CPU
  - The instruction format also contains other fields known as operand fields
  - The CPU executes the instruction using the information which reside in these fields
  - There are six general formats of instructions in 8086 instruction set. The length of an instruction may vary from 1 byte to 6 bytes

1. One Byte Instruction:

- This format is only one byte long and may have the implied data or register operands.
- The least significant 3-bits of the opcode are used for specifying the register operand, if any.
- Otherwise, all the 8 bits form an opcode and the operands are implied

2. Register to Register:

- This format is 2 bytes long. The first byte of the code specifies the operation code and width of the operand specified by 'w' bit.
- The second byte of the code shows the register operands and R/M field, as shown below.

- The register represented by the **REG** field is one of the operands.
- The R/M field specifies another register or memory location i.e. the other operand

D7 D1	D0	D7 D6	D5 D4 D3	D2 D1 D0
OPCODE	W	11	REG	R/M

3. Register to/from memory with no displacement:

- This format is also 2 bytes long and similar to the Register to Register format except for the **MOD** field as shown.

D7 D1	D0	D7 D6	D5 D4 D3	D2 D1 D0
OPCODE	W	MOD	REG	R/M

- The MOD field shows the mode of addressing. The MOD, R/M, REG and the 'W' fields are decided in Table 2.2

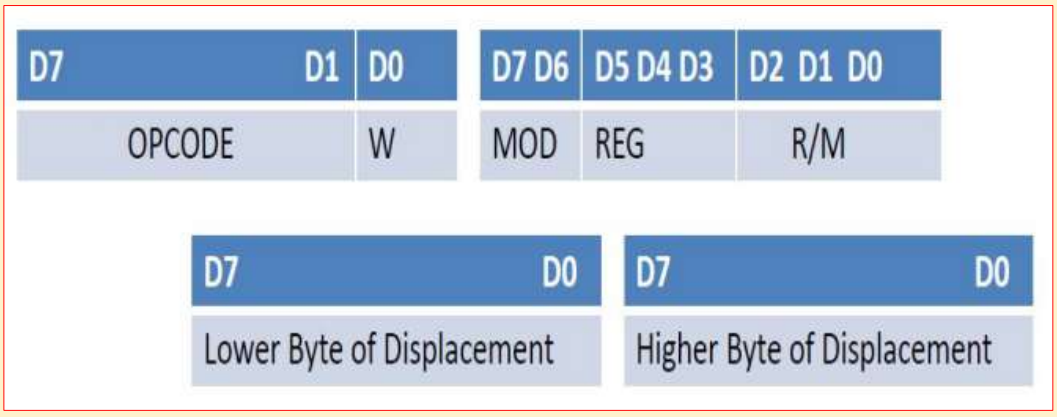
Table 2.2 *Addressing Modes and the Corresponding MOD, REG and R/M Fields*

Operands	Memory Operands			Register Operands	
	No Displacement	Displacement 8-bit	Displacement 16-bit		
MOD / R/M	00	01	10	11	
				W = 0	W = 1
000	(BX) + (SI)	(BX) + (SI) + D8	(BX) + (SI) + D16	AL	AX
001	(BX) + (DI)	(BX) + (DI) + D8	(BX) + (DI) + D16	CL	CX
010	(BP) + (SI)	(BP) + (SI) + D8	(BP) + (SI) + D16	DL	DX
011	(BP) + (DI)	(BP) + (DI) + D8	(BP) + (DI) + D16	BL	BX
100	(SI)	(SI) + D8	(SI) + D16	AH	SP
101	(DI)	(DI) + D8	(DI) + D16	CH	BP
110	D16	(BP) + D8	(BP) + D16	DH	SI
111	(BX)	(BX) + D8	(BX) + D16	BH	DI

Note: 1. D8 and D16 represent 8 and 16 bit displacements respectively.
2. The default segment for the addressing modes using BP and SP is SS. For all other addressing modes the default segments are DS or ES.

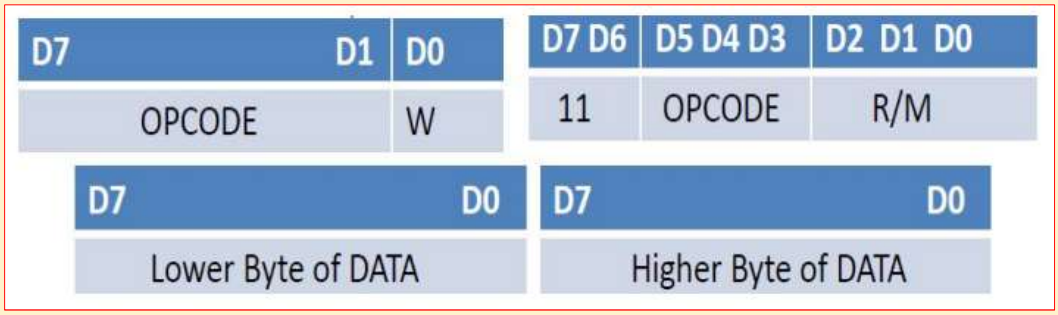
4. Register to/from Memory with Displacement:

- This type of instruction format contains 1 or 2 additional bytes for displacement along with 2 byte format of the register to/from memory without displacement. The format is as shown below.



5. Immediate Operand to Register:

- In this format, the first byte as well as the 3-bits from the second byte which are used for REG field in case of register to register format are used for opcode.
- It also contains one or two bytes of immediate data. The complete instruction format is as shown below.



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