Bus Bar Design for High-Power Inverters

Alan Dorneles Callegaro, *Student Member, IEEE*, Jing Guo, *Student Member, IEEE*, Michael Eull, *Student Member, IEEE*, Benjamin Danen, *Student Member, IEEE*, Jason Gibson, Matthias Preindl, *Member, IEEE*, Berker Bilgin, *Senior Member, IEEE*, and Ali Emadi, *Fellow, IEEE*

***Abstract*—This paper presents a comprehensive analysis about bus bar design procedure. Some applications in terms of rated power and shape are investigated regarding their particular requirements and challenges. The dc-link capacitor selection is one of the first and most important steps. It not only dictates the bus bar complexity but also is the key to accomplish a high-power density prototype. Current density and distribution is discussed in this paper based on simulation results. Moreover, the effects of stray inductance and capacitance are explained along with the dc-link capacitors and power semiconductor devices. Simulated results are compared with measurements by a high precision impedance analyzer, which shows the reliability of 3-D modeling-based designs.**

***Index Terms*—Bus bar, high-power inverter, power electronics, SRM inverter, stray capacitance, stray inductance, three-phase inverter.**

I. Introduction

BUS bars have been present in power distribution systems for many years. In their most basic form, bus bars are large conductors used to transmit significant quantities of current where a wiring scheme is infeasible. With power transistors continuing to move upward in current levels and switching frequency, laminated bus bars have been attracting increasing interest from both industry and academia for the system benefits they exhibit. These include a low impedance via tightly coupled conducting planes, a simplification in system assembly and reliability enhancements.

Many studies have been undertaken that involve the design and use of a bus bar for some applications [1]–[8]. Often, the design of the bus bar and necessary considerations are not discussed in great detail, with most of the attention being paid to minimizing the stray inductance. This does not detract from the quality of the work; indeed, many interesting results are presented that, when put together, help to guide the design process. In [1], the basics for low-inductance bus bar design are laid out and the benefits of such an approach are exhibited. At around the same time, other researchers presented a different approach to bus bar design for a single-phase inverter that removed one layer in the stackup and showed a benefit in the inductance, although it did cost them in complexity [4]. In [3], several theories are tested and their respective benefits and drawbacks shown. A bus bar for Silicon Carbide MOSFET modules was designed and tested in [5], albeit at low frequencies, adding to the general body of work.

Some unique approaches were taken as more researchers published on the subject. One of the most interesting is presented in [8], where a multilayer design, with several forward, return, and grounding planes are present. The result is a lower inductance and reduced electromagnetic emissions. Others built on this and previous ideas by analyzing special structures for multilevel converters. In [2] and [6], the respective authors built multilevel converters with bus bars and, in the latter, a listing of bus bar topologies from previous studies for different converter applications was presented.

Other researchers have considered thermal effects driven by the generated power losses [9], [10]. In [9], a model is created to analyze the steady state and transient performance of a single bus bar, independent of material and geometry. In [10], a scalable lumped parameter thermal model is developed for a laminated bus bar, with estimated and actual temperatures being reasonably close.

Few sources discuss design practices explicitly. A good resource in the literature is [7], where several key aspects are considered: integration of the capacitors and switches, holes, insulation material, and overall dimensioning. Bus bar manufacturers normally provide some advice and support on their websites as well, with one such example being found on [11]. The provided information is often not exhaustive and does not cover complex geometries, leaving designers to estimate performance under such conditions, opening up the opportunity for suboptimal designs to be manufactured.

With respect to multilayer designs, they afford the opportunity to decrease losses and, potentially, the parasitic inductance of the interconnected system. Some research has been done on this subject, with a proposed reduced layer bus bar proposed in [4], where the dc-link bus bars are parallel to one another on the same plane and the phase output is separated from the two by a layer of insulation. Two instances of intricate multilayer

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A. D. Callegaro, J. Guo, B. Danen, B. Bilgin, and A. Emadi are with the McMaster Automotive Resource Centre, McMaster University, Hamilton, ON L8P 0A6, Canada (e-mail: dornelea@mcmaster.ca; guoj25@mcmaster.ca; danenbh@mcmaster.ca; bilginb@mcmaster.ca; emadi@mcmaster.ca).

M. Eull and M. Preindl are with the Department of Electrical Engineering, Columbia University in the City of New York, New York, NY 10027 USA (e-mail: we2148@columbia.edu; matthias.preindl@columbia.edu).

J. Gibson is with the MERSEN Electrical Power, New York, NY 14623 USA (e-mail: Jason.Gibson@lbb.mersen.com).

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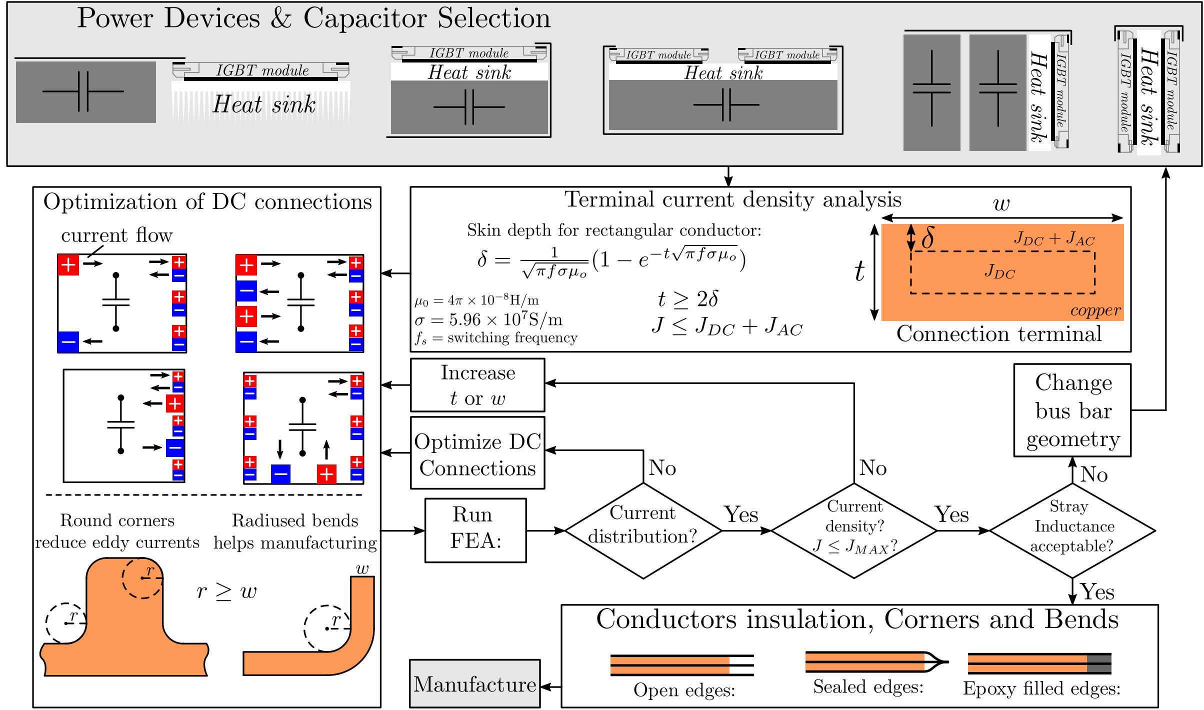

Fig. 1. Bus bar design procedure. Components selection, ac and dc current density analysis, 3-D modeling and finite element analysis (FEA) simulations, and insulation material selection are involved in this process.

arrangements for multilevel inverters are presented in [6] and [2] and, in [8], a truly multilayer bus bar design is shown. In all three papers, moving to multilayer designs has benefited the inductance. There are certainly added costs and complexities moving from a single conductor bus bar to a multilayer one. One of the main design considerations that has to be designed around is the hi-pot test, which is a high-potential test to verify the electrical insulation between the bus bar conductors. However, coupling multilayer designs with aluminum as the conductor could yield benefits in terms of mass reduction, but at the expense of higher losses.

This paper endeavors to outline a design process for a bus bar. Experimental results for five physically realized designs are presented to show the validity of the approaches used. In Section II, general design considerations are discussed where a step-by-step procedure for a bus bar design and optimization is proposed. Section III provides a detailed analysis of current ripple generated by the switching operations of a three-phase inverter using sinusoidal pulse width modulation (PWM). A number of key subjects are covered in Section IV—including the current density, skin and proximity effects, and parasitic parameters—and simulations are provided to show how they may be obtained. Section V provides experimental results to substantiate the design principles and simulations discussed in preceding sections. Last, conclusions are drawn on the efficacy of the presented paper.

II. Design Considerations

A. Bus Bar Shape Definition and Manufacturing Feasibility

Distinct converter topologies and applications require special characteristics for the shape and dimensions of a bus bar. In terms of mechanical construction, the number of inputs and outputs can dictate the design complexity. Also, on the electrical point of view, the average and rms current amplitude as well as the low- and high-frequency components are responsible for the bus bar thickness and number of connections in order to improve the current distribution. However, the most crucial point for a good bus bar design is the dc-link capacitance requirement.

As illustrated by Fig. 1, a bus bar design is composed of several steps. Power semiconductors and dc-link capacitor geometry are chosen to optimize the power density as well as to minimize the bus bar complexity. Some examples are presented at the first step including air and water cooled configurations. The next step comprehends terminal connection size in regards to current density and skin effect. It is important to note that, from the results obtained on bus bars A, B, and D, terminal connections have a significant impact on stray inductance. Once bus bar thickness and terminals are defined, dc and ac connections are defined on a 3-D CAD model. For a better current distribution, dc input connections must be symmetrically positioned relative to the power modules. For the ac current distribution, the symmetry between dc-link capacitor and power semiconductor modules is also necessary. Sharp corners and bends can cause eddy currents and consequently voltage drops, which results in losses and heat generation, “the surface impedance has the maximum value at the conductor edge. The sharper the edge, the greater the value of $Z_{s,\max}$” [12]. To avoid these effects, corners and bends should have a sufficient radius, as illustrated in Fig. 1. Simulation analysis is an important step in order to guarantee the bus bar performance. This is can be an iterative process where the terminal connection, dimensions, or geometry of the bus bar can be updated to match requirements such as current density, distribution, and stray inductance. Finally,

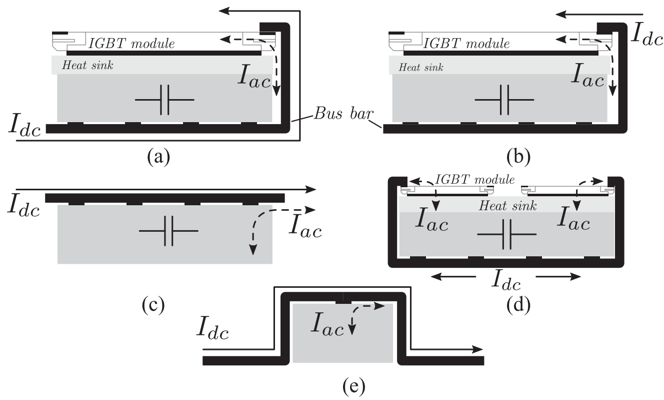

Fig. 2. DC and ac current paths for different bus bar applications. The dc current represents the input average current and the ac component is circulating between the IGBT/MOSFET terminals and dc-link capacitor.

according to the application requirements, the insulation material and configuration are defined and the manufacturing process begins.

Fig. 2 shows the five applications that are discussed in the paper and Fig. 3 shows the prototypes for those applications. Fig. 3(a) and (b) illustrates two solutions where both the IGBT module and film capacitor are coupled to a water cooled thermal plate. Although both bus bar designs look similar, there is a major difference between them. In the first case, the dc input is connected to the left side which makes both dc and ac current components circulate through the bus bar increasing its current density and losses. In the second design, as shown in Fig. 4, the dc input connection is closer to the IGBT module and consequently the majority of the current on the bus bar is the high-frequency component; as a result the ohmic losses can be reduced. During the component selection process of bus bar B, the SBE power ring capacitor was chosen due its higher current rating and capacitance value. Another option for this case was the LH3 series film capacitor from electronic concepts, with slightly lower rated current and capacitance at the same voltage rating.

Simpler bus bar configurations are shown in Fig. 3(c) and (e). Type C consists of a flat bus bar connecting the input and output with the dc-link capacitor, while type E is shaped around the capacitors. In most cases, the ability to share the heat sink between the power semiconductors and dc-link capacitor is lost in this configuration. For applications such as a dual-inverter topology, where two inverters are sharing the same bus bar and dc-link capacitors, bus bar type D has its dc input connection in the middle of the bus bar, as illustrated in Fig. 3(d).

Cylindrical and rectangular capacitors are most commonly employed, and in terms of technology, the options are ceramic, electrolytic, or film capacitors. For the sake of safety and robustness, film capacitor are widely implemented nowadays. The design and number of capacitors also affects the number of holes and connection points. This increases the possibility of an electrical short area (hi-pot failure) and complicates the design.

The most common and easiest connection method for a capacitor onto a bus bar is a screw or bolt on connection. Soldering or spot welding connection methods can also be used, but they greatly increase the cost and complexity of the design. In sum, the bus bar design starts along with the power electronics converter design.

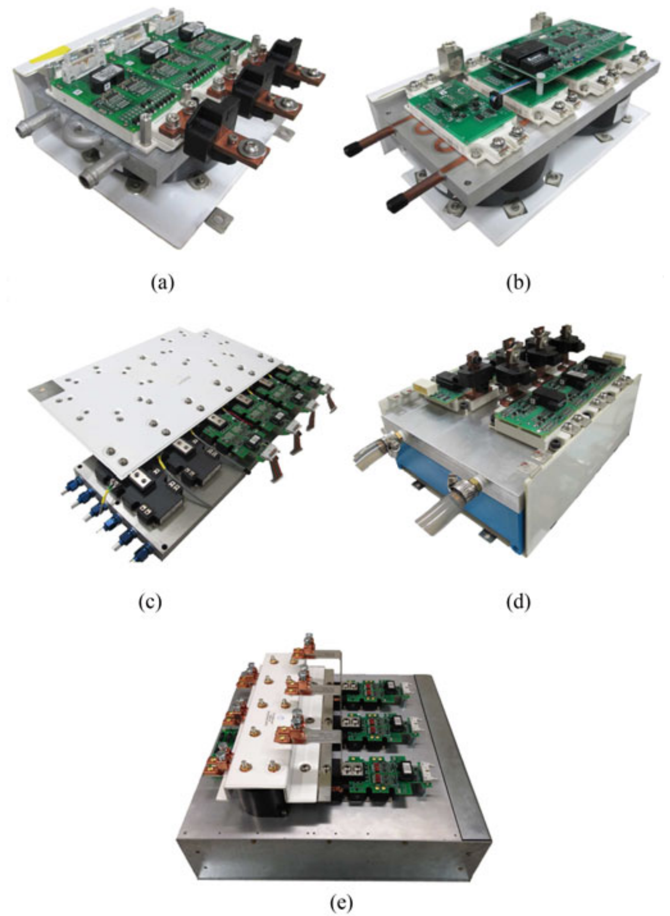

Fig. 3. High-power inverter prototypes with five different bus bar designs. (a) Bus bar type A, three-phase inverter. (b) Bus bar type B, four-phase asymmetric bridge switched reluctance machine (SRM) inverter. (c) Bus bar type C, three-phase SRM inverter. (d) Bus bar type D, dual three-phase inverter. (e) Bus bar type E, three-phase inverter.

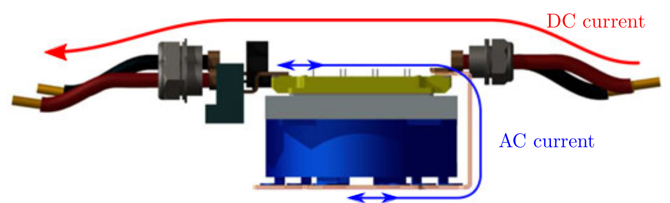

Fig. 4. DC and ac current flow in bus bar type B.

Although the general shape and configuration of the bus bar is defined by the designer and the component layout of the system, the manufacturer will make suggestions for complexity and cost reduction. Since all bends or forms in the metal increase cost, the majority of shapes that deviates the bus bar from the flat plate stock shape will be done using a separate manufacturing operation. Each individual manufacturing operation can have its own costs associated with it, such as:

1) General run-time cost. This is the general labor, machine rate, and overhead cost applied to an operation.

2) Setup cost. This is the time to set up and calibrate the machine to perform the manufacturing operation. The setup time is spread across the lot size being run.
3) Certain operations, such as bending the metal, may require a unique tool, fixture, or die to perform the operation. This unique tool will cost to that job as a one-time charge.

In general, the process of reviewing or creating a design requires an in-depth knowledge of the manufacturing process. In terms of bending, a general guideline is to make the inside radius of a bend equal to or greater than the overall thickness of the bar or sheet to bend. For bending raw metal sheets or bars, it is possible to make the inside bend radius smaller than the metal thickness, but it can introduce problems or make the operation more difficult. Inside and outside corners of a stamped plate should be radiused for several reasons. By radiusing the inside and outside corners of a stamped plate, the lamination will stretch and form better over the corner, there will be fewer eddy currents and resulting hot spots and the sharp corner will require less time and care to reduce its burr.

When designing a higher level assembly, whether it is assembled by hand with operators or by automated machinery, the physical space and limitations must be considered. The order of assembly is important. Once the first component is attached, we must make sure that there is room to attach the second. Not only the actual space it will occupy, but also the path to get the second component into position should be taken into account. Once all of the assembly is verified, there has to be room to maneuver the required tools. If a screw is needed to assemble a component, then there has to be room for the screw driver and an operator's hand to work the screw driver. Finally, possible servicing such as periodical inspection, maintenance, cleaning, or replacement must be considered.

B. Conductor Insulation

The selection of the electrical insulation is driven by the operating voltage, the operating temperature, and the environment in which it has to function. The operating voltage dictates the required dielectric strength of the insulation which in turn depends on the material used.

The most common materials are: Nomex, Tedlar, Mylar, Kapton, Ultem, Valox, epoxy-glass, heat shrink tubing, and epoxy powder coating, or some combination of them [13]. For high-frequency ac applications, the material Nomex type 410 from DuPont has a dielectric strength of 34 kV/mm for a thickness of 0.18 mm and 32 kV/mm for 0.51 mm [14]. As the insulation thickness increases, the dielectric-strength decreases, and consequently, as estimated by (6) in Section III-B, the bus bar capacitance is also reduced. A higher capacitance value decreases the overall bus bar impedance and consequently reduces the noise produced by parasitic inductances at high frequencies. This explains the importance of high-dielectric-strength material combined with high-technology manufacturing.

The creepage distance, which can cause short circuits, should be considered as well and is dictated by the exterior material of the insulation film (bare film or coated with resin) and the environment it is in. If the surface of the bus bar (between two potentials) has moisture or has dirt or debris on it, the creepage distance may be significantly reduced and the current can track along the surface of the insulation easier to create a short. The severity of the contamination is typically defined by the pollution degree rating [15].

Pollution degree affects the creepage and clearance distances required to ensure the safety of a product and it is classified according to the amount of dry pollution and condensation in the environment. Safety standards bodies such as Underwriters Laboratories (UL) and IEC categorize them as follows:

Pollution Degree 1: No pollution or only dry, nonconductive pollution occurs and has no effect. Examples are, sealed components and within air/water tight enclosures.

Pollution Degree 2: Normally only nonconductive pollution occurs. Temporary conductivity caused by condensation is to be expected, commonly present in offices and laboratories.

Pollution Degree 3: Conductive pollution or dry nonconductive pollution that becomes conductive due to condensation. Often the case in industrial environments or manufacturing areas (harsh environments).

Pollution Degree 4: The pollution generates persistent conductivity caused by conductive dust, rain, or snow.

The pollution degree can also impact the selection of the insulation type. Certain materials will simply not hold up well under certain conditions. Nomex for example is a popular insulation material that has been in use for decades. It is however, an aramid paper. This means it is hydroscopic and has the potential to absorb moisture. Once this happens, the dielectric rating is severely degraded and may also cause delamination.

Since each insulation material has an upper and a lower temperature limit for functionality, this must also be taken into account. The upper limit is typically the parameter that causes design issues. One must consider both the ambient temperature and the self-heating temperature rise of the bus bar. The lower temperature limit is rarely a problem, but must be considered if there are any shock or vibration conditions that can occur at those lower temperatures.

How the bus bar is to be used and what it comes into contact with must be considered, when selecting the insulation material. Most laminating films are relatively durable, but can be cut creating an insulation fault. It must also be considered if another component may impact or rub against the laminated surface, which can result in a hi-pot failure.

With any of these potential "severe physical use" conditions, an alternate material should be considered, such as powder coating or a secondary material on top of the laminated surface. Powder coating is a hard, durable, and chemical resistant dielectric coating that can be used instead of or in conjunction with lamination. Secondary barrier materials such as FR-4 (Flame Retardant) or GPO3 (Glass Polyester Laminate, NEMA LI-1) are also common in these conditions.

The choice of the thickness is typically driven by the dielectric requirement, but can also be driven by the physical design of the conductors themselves. The flexibility of the insulating material must also be considered. Under severe vibration or flexation conditions, powder coating can crack and fail. The design may also require the conductor to be formed after being laminated.

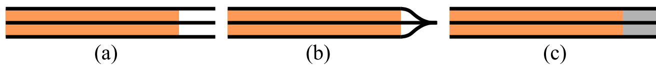

Fig. 5. Conductors insulation: (a) Simplest and least expensive. (b) Insulation is pinched closed and sealed on itself. (c) Epoxy filled edges.

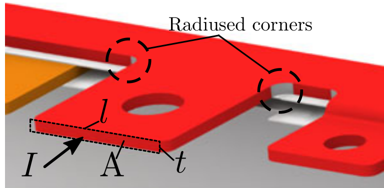

Fig. 6. Bus bar thickness design considerations based on maximum current density J [A/mm^2].

This requires a film that can stretch and bend with the conductor. Most films can do this, Nomex is one that cannot.

Finally, as illustrated in Fig. 5, the *edge conditioning* of the bus bar defines the conductor edges protection from contamination and shorting. Open edge is the most susceptible to contamination and hi-pot failure and is typically used in clean and dry environments. The sealed edge gives some protection against mild contamination and is the most common and typically not more expensive than the open edge. However, the tooling cost can be higher for complicated laminating fixtures. In the third method, the channels formed in the open edge technique are now filled with an epoxy. This gives a strong and durable barrier to contamination and moisture.

C. Conductor Thickness and Current Density

When mechanical strength is not the main requirement, the copper thickness is defined by the input and output terminal connectors. As illustrated by Fig. 6, given the maximum current density J [A/mm^2] and the length l available, the thickness w is calculated to keep the current density within its specification. For instance, in high current applications, the dc input is split in two or more connectors in order to improve the current distribution with acceptable copper thickness. As illustrated by Fig. 9, dc current distribution is improved by splitting the positive and negative terminals in three. This reduces ohmic losses and evenly spread the heat across the bus bar, which reduces the hot spots. Typically, the bus bar conductors are sized for a 30 °C self-heating temperature.

The lower boundaries in bus bar design require: a minimum conductor thickness to prevent it from melting when the nominal current is applied and a minimum insulation thickness to sustain the intended operating voltage. An upper boundary does not explicitly exist and, thus, is decided by the designer as a result of system constraints and desires: size, weight, cost, and electrical and thermal performance. Depending on the thickness of the copper, it may be prudent to thicken the dielectric material to minimize the impact of swarf when pressing the sheets together.

A rule of thumb for bus bar design is to not allow the current density to exceed 5A/mm^2 [16]. A higher threshold would mean that a smaller cross sectional area is needed, allowing for a size reduction in the vertical or horizontal directions. A lower threshold would be the inverse: more material, in either axis, is needed to reduce the current density and, consequently, the losses. More material, in turn, leads to a more expensive and heavier bus bar. For complex bus bar shapes, the mass can be approximated by breaking it up into discrete segments that are easy to calculate. For a more precise calculation, the mass of the dielectric material and the adhesive holding the pieces together can be calculated; however, these are relatively small values when compared to the conductor and, unless the application is severely weight restricted, need not be considered.

D. Noncopper Conductors

Additional subjects of interest, though not detailed in depth in this paper, are the transition to noncopper materials (e.g., aluminum). Working with aluminum has advantages and drawbacks. Aluminum, relative to copper, has a density that is 33% lower than that of copper; however, both its electrical and thermal conductivity are 60% lower in comparison, depending on the alloy used. Therefore, an aluminum design should weigh 66% less than a copper one of equivalent thickness. But, because of the conductivity difference explained above, the weight reduction from a copper bus bar is about 33%. The cost saving of a cheaper per-pound price of aluminum is also eroded by this as well.

Aluminum is also particularly good for mass production. It can be made as a mould that offers more consistent results. However, the manufacturability impact of doubling the conductor thickness must be considered. Going from a 1-mm thick copper conductor to a 2-mm thick aluminum one is typically not a problem. But if the copper conductor is already 3 mm thick, doubling it to 6 mm will greatly impact many aspects of the manufacturing process.

Other lossy conductors, such as nickel, can be added to the surface of the copper conductors to reduce high-frequency harmonics [17]. This combination will attenuate the high-frequency noise, which is pushed to the surface to travel through the lossy nickel due to the skin effect. The low-frequency current will be distributed throughout the less-resistive copper.

III. Simulations

In this section, simulations that are used to predict the bus bar performance are introduced. Following the steps described in Section II, the bus bar can be preliminarily designed. Then the next step is the bus bar performance evaluation. If the predicted bus bar performance meets the requirements, the bus bar can be sent for manufacturing; otherwise, modifications in the initial design might be demanded based on the simulation results.

Bus bars can be designed according to the packages and locations of the selected switching devices and dc-link capacitors. To evaluate the performance of a bus bar before it is manufactured, analysis could be done by simulation using an electromagnetic simulation software, such as ANSYS Maxwell. In the simulations, the current density and distribution can be estimated based on different inverter operating conditions. Additionally, the current excitations should be defined by (1), where $I_{\mathrm{ave,in}}$, $I_{\mathrm{rms,in}}$, $I_{\mathrm{rms,ripple}}$, M, and $\cos\phi$ indicate the average and rms value of

TABLE I
SYSTEM PARAMETERS OF APPLICATIONS

Bus bar parameters	A	B	C	D	E
V_{dc}[V]	300	600	600	425	300
$I_{\text{rms,out}}$ [A]	212	400	600	365	450
$I_{\text{ave,in}}$ [A]	195	300	250	400	410
$I_{\text{rms,in}}$ [A]	230	350	425	435	490
$I_{\text{rms-ripple}}$ [A]	123.5	-	-	237	270

the dc-link current, rms ripple current, modulation index, and power factor, respectively, [18]–[21]:

$$I_{\text{rms,ripple}} = \sqrt{I^2{}_{\text{rms,in}} - I^2{}_{\text{ave,in}}} = I_{\text{rms}} \cdot \sqrt{\frac{\sqrt{3}M}{2\pi} + \left(\frac{2\sqrt{3}M}{\pi} - \frac{9}{8}M^2\right) \cdot \cos^2\phi}. \quad (1)$$

As it is mentioned above, the design should meet the requirement of current density limitation (a typical value for passive cooled bus bars is 5 A/mm^2) to prevent overheating in any part of the bus bar. Meanwhile, to achieve balanced current sharing at the output terminals and among the dc-link capacitors, the current distribution on bus bars needs to be evaluated. [22]

Furthermore, 3-D analysis is necessary to calculate the parasitic parameters of the bus bar, so resistance and bus bar power loss can be obtained. Resistance varies depending on the frequency of the ac current. The relationship between the frequency and the resistance can be obtained through simulation as well. However, the resistance of the bus bar is typically small and the amount of power loss is usually negligible compared to the total power loss of the entire inverter. Moreover, the value of bus bar stray inductance can be estimated. To prevent switching devices being damaged by large voltage spikes during turn-OFF transients and to reduce switching power loss of the device and the stray impedance of the bus bar, the total inductance in the circuit has to be minimized. Generally, the total circuit inductance includes dc-link capacitor equivalent series inductance, switching device equivalent inductance, and the bus bar stray inductance. Even though it is possible to select switching devices and capacitors with relatively small inductance, there is only a limited improvement on the total circuit inductance. Nevertheless, by laminating two conductors (positive and negative plate) the mutual inductance is maximized and significant reduction in the bus bar stray inductance can be achieved. As a result, the total inductance in the circuit is also minimized. Therefore, the stray inductance analysis is very important in dc bus bar design. Another parameter that needs to be analyzed is the stray capacitance, which should be maximized in the design to reduce the stray impedance and the electromagnetic interference (EMI) [1], [23]. Table I shows the parameters corresponding to each bus bar design given in Fig. 3.

A. Current Density

The analysis of current density and current distribution is indispensable. A bus bar design should satisfy the current density

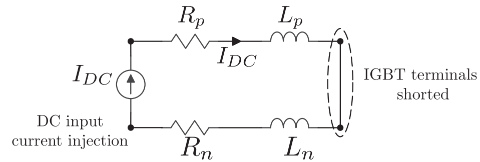

Fig. 7. Bus bar simulation: dc analysis equivalent circuit.

requirement; thus, the overheat on entire bus bar or in some of its local areas can be prevented. In addition, some applications contain more than one dc-link capacitor and, to ensure that each capacitor operates under similar conditions, the ac current distribution and the current sharing among the capacitors should be balanced. The phase currents, and consequently the current through the power devices, are defined by the load demand and individually controlled by the control algorithm. Therefore, for a three-phase balanced load, currents through the power semiconductors are also balanced.

In an inverter, the dc bus current can be presented by the sum of dc and ac current components. The dc current component is $I_{\text{ave,in}}$, while the ac current component is the dc-link capacitor current, and its rms value is $I_{\text{rms,in}}$. As a result, the current distribution of dc component and ac component can be evaluated by dc analysis and ac analysis, respectively. The bus bar is modeled with a single average *R-L* model. In the design process, asymmetries are typically analyzed with FEA using a 3-D model of the bus bar.

In dc analysis, a dc current is injected from the dc input terminals into the bus bar, as shown in Fig. 7. R_p, L_p, R_n, and L_n stand for the resistance and stray inductance of bus bar positive plate (p) and negative plate (n), respectively. At the same time, the positive plate and the negative plate of the bus bar are shorted at the power switching device terminals [4]. Thus, the current distribution on the bus bar between input terminals and switching device is analyzed. To implement the simulation, excitation current is defined as the rms value of inverter input current.

A preliminary design of an inverter dc bus bar with one set of dc input is shown in Fig. 9(a). It is obvious that the current distribution is unbalanced and higher current density is acquired around the area near dc input terminals on both plates.

To improve the current distribution, a bus bar with three sets of dc inputs is designed. It can be seen in Fig. 9(b) that dc inputs are distributed along one side of the bus bar and the current flow on the entire bus bar is balanced. Therefore, the current density analysis shown in Fig. 6 holds.

Then the ac analysis can be implemented to evaluate the bus bar current distribution between capacitors and switching devices. In other words, the current sharing among dc-link capacitors is analyzed. The equivalent circuit of ac analysis is shown in Fig. 8. Here, an ac excitation current is injected into the bus bar from switching device terminals. In addition, the positive plate and the negative plate of the bus bar are shorted at dc-link capacitor terminals.

The current distribution in ac analysis in the preliminary design in Fig. 9(c) is similar to the revised design in Fig. 9(d). This validates that the ac current distribution is defined by the

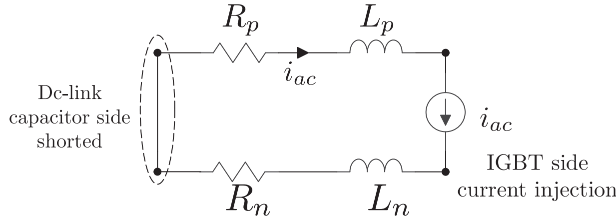

Fig. 8. Bus bar simulation: ac analysis equivalent circuit.

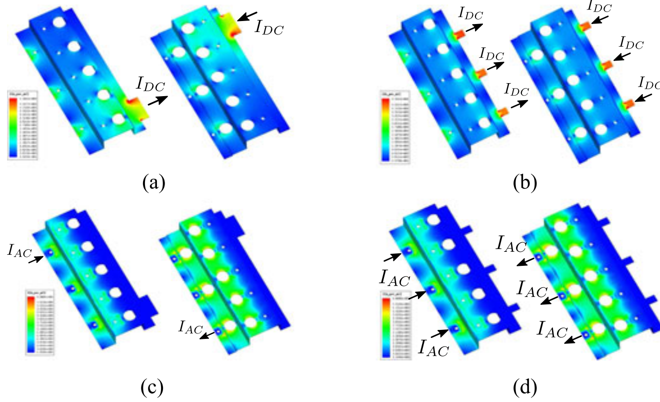

Fig. 9. DC and ac analysis for inverter dc-link current density and distribution with three sets of dc input (the negative plate is shown on the left and the positive plate is shown on the right, maximum current density of 5 A/mm^2). (a) DC analysis for inverter dc-link current density and distribution with one set of dc input. (b) DC analysis for inverter dc-link current density and distribution with three sets of dc input. (c) AC analysis for inverter dc-link current density and distribution with one set of dc input. (d) AC analysis for inverter dc-link current density and distribution with three sets of dc input.

location of the capacitors and switches rather than those of dc input tabs.

Both the skin and proximity effects contribute to design challenges by increasing the losses and reducing the region of effectively utilized conductor. If the goal is to stay below a prescribed current density, then these effects need to be carefully studied. In the dc case, the thickness of the conductor is chosen to meet a chosen maximum current density. In the ac case, when skin and proximity effects are present, current flows closer to the surface of the material, reducing the effective conducting area. This requires a reconsideration of a bus bar's layout. A bus bar designed with dc current density in mind would result in a significant amount of wasted conductor with a sufficiently high-frequency ac current.

The skin effect can be considered using the skin depth, which is the distance from the surface that the ac current flows. This depth depends on the conductor itself as well as the frequency of the current. Generally, the skin depth can be approximated while neglecting the thickness of the conductor. When the material thickness is comparable to the skin depth, it should be taken into account [24], [25]. This is often the case with bus bars currents at intermediate frequencies, when the skin depth is similar to the thickness of the bus bar. The equation to approximate skin depth while accounting for the thickness is given in (2). An illustration of the skin effect and the comparison between analytical and FEA results is shown by Fig. 10:

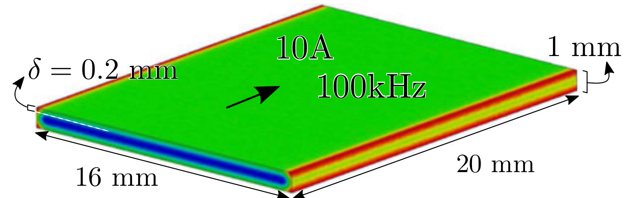

Fig. 10. Skin effect simulation analysis for a rectangular conductor showing the comparison between analytic and FEA results.

$$\delta = \frac{1}{\sqrt{\pi f \sigma \mu}}(1 - e^{-t\sqrt{\pi f \sigma \mu}}). \tag{2}$$

An imbalance in the current density distribution is possible when considering complex geometries and, in particular, those that are asymmetric. In these cases, it may be necessary to guide currents—both dc and ac—to their respective locations by adding features to reroute current. For example, in the ac ripple current case, currents flow from the power module through the dc-link capacitors and back. If a significant imbalance is present, then it could result in accelerated failure of the capacitors and, consequently, for the inverter as a whole. Equal current sharing between devices is critical to the long-term reliability of negative temperature coefficient components, such as electrolytic capacitors, IGBTs, and diodes.

When assessing the rerouting of currents, the focus is normally placed on minimizing the current density through a vulnerable path or the current balancing of active and passive components. The most reliable method by which these issues can be avoided is to ensure that the paths are symmetric and of the same length. This, however, is not always possible and, indeed, for many designs, is infeasible. Hence, in some cases, it becomes necessary to consider adding intentional obstacles (holes) to the current flow path to make it an unattractive route.

Fig. 11 illustrates such an idea. The point of injection is one of three IGBT module terminals and, in this case, it is in a location where it is impossible to guarantee equal current sharing between capacitors, with the left-most one experiencing the highest current and, therefore, losses. Fig. 11(a) shows the bus bar with no alterations, whereas Fig. 11(b) and (c) shows it with symmetrical cuts, triangular and round added, respectively. The current density, while not drastically different, has been reduced on the left-hand side with current being pushed rightward, thereby reducing the stresses on the left-most capacitor. A sweep of incision dimensions can be made and the current sunk by each capacitor evaluated until a suitable result is achieved.

In order to address the current distribution problem, Fig. 12 illustrates two different design for dc input connections for the same application. On first design, the input connectors are concentrated at the edge of the bus bar. This configuration may cause a hot spot due to the higher current density on the top and bottom layer at the same bus bar region. This overheat may damage the insulation material and consequently reduce the converter robustness.

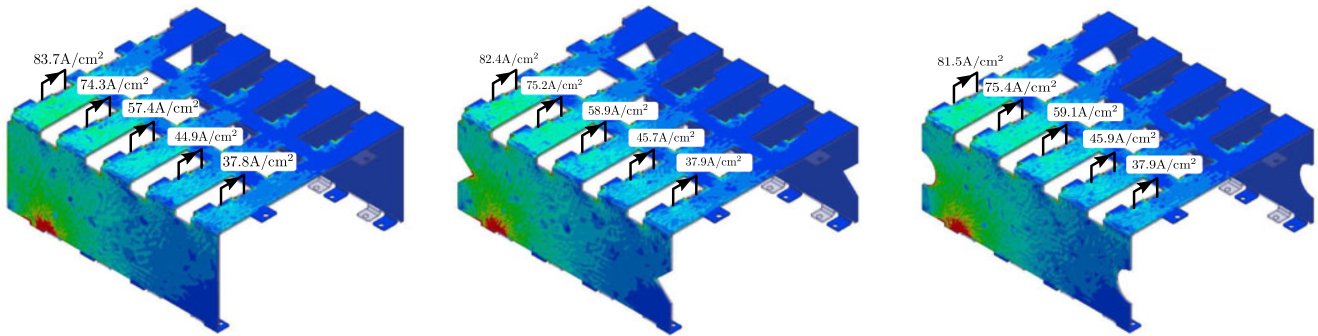

Fig. 11. AC current guiding by using incisions in the bus bar. (a) Bus bar with no cut. (b) Bus bar with triangular cut. (c) Bus bar with round cut.

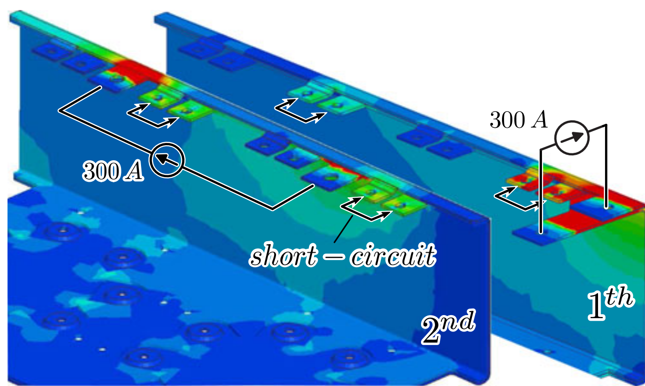

Fig. 12. Current distribution analysis for two configurations of input dc current connections, maximum current density of 5 A/mm^2.

TABLE II
STRAY RESISTANCE OBTAINED FROM SIMULATIONS

Frequency [kHz]	Resistance [mΩ]	Bus bar power loss [W]		
		Negative plate	Positive plate	Total
0	0.158	1.41	1.53	2.94
10	0.219	1.49	1.42	2.91
20	0.251	1.87	1.77	3.64
30	0.270	2.07	1.96	4.03
40	0.284	2.22	2.14	4.36
50	0.295	2.33	2.21	4.54
60	0.304	2.41	2.28	4.69
70	0.311	2.47	2.35	4.82
80	0.317	2.54	2.41	4.95
90	0.322	2.57	2.44	5.01
100	0.327	2.62	2.48	5.10

B. Parasitics

1) Resistance: The evaluation of parasitics in a bus bar, including resistance, stray inductance, and capacitance, is also very important. First, the resistance affects power loss on a bus bar. Thus, low bus bar resistance is preferred. Generally, the resistance is determined by materials and shape of the conductor.

Bus bar E is taken as an example in resistance calculation. Table II presents the resistance and ohmic loss acquired by dc- and ac-analysis. It demonstrates that as the current frequency increases, the value of resistance grows and it results in higher ohmic loss on both negative and positive plates [26], [27]. However, the total ohmic loss on the bus bar is only several watts that is negligible compared to the inverter power loss.

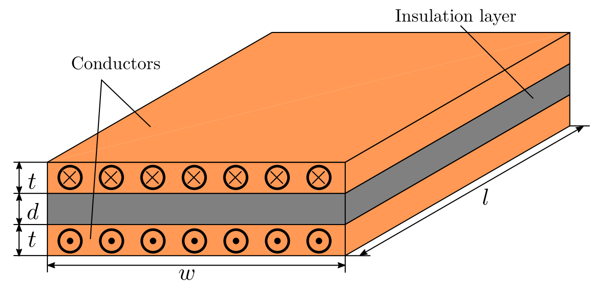

Fig. 13. Example of bus bar structure.

2) Stray Inductance: The stray inductance defines the voltage spike during turn-OFF transient of the switching device. A high voltage spike, which may damage the semiconductors, is caused by a large parasitic inductance. Furthermore, it results in higher switching power loss and EMI, and it also restricts the switching frequency of the inverter due to the thermal limitations [28]. If the connection terminals for capacitors and power modules are asymmetrically located, the parasitic impedance difference in each current path may affect current sharing [29].

To understand and reduce this voltage spike and its resulting effects, the stray inductance of the bus bar should be estimated and minimized. A bus bar is a collection of parallel plates, and an example is given in Fig. 13, where w, t, l, and d indicate width, thickness, and length of each conductor, and the distance between two conductors, respectively. The inductance of flat plates (3) can be used to approximate the self-inductance of the entire conductor [30]–[32], which is valid only for the dc current analysis:

$$L_{\mathrm{self}} = 2l\left(\log(\frac{2l}{w+t}) + 0.5 + 0.2235(\frac{w+t}{l})\right) \times 10^{-7}. \tag{3}$$

From (3), it can be concluded that an increase in either the width or thickness reduces the inductance. However, thick bus bar design renders high material cost. To achieve the minimized inductance and material cost, the bus bar is designed with large width and small thickness, which is commonly utilized by conventional flat plate design.

Furthermore, the flux linkages of two conductors will cancel each other due to their opposite current directions shown in

TABLE III
STRAY INDUCTANCE [nH] OBTAINED FROM SIMULATIONS

Frequency [kHz]	Bus bar type				
	A	B	C	D	E
10	21.38	24.01	11.16	13.90	9.82
20	20.46	23.33	10.68	13.14	9.36
30	20.05	23.04	10.46	12.80	9.19
40	19.79	22.87	10.34	12.59	9.10
50	19.62	22.77	10.27	12.45	9.05
60	19.49	22.7	10.22	12.35	9.00
70	19.39	22.65	10.18	12.26	8.98
80	19.31	22.62	10.16	12.20	8.96
90	19.24	22.59	10.14	12.14	8.94
100	19.19	22.57	10.12	12.10	8.93

Fig. 13, and the total stray inductance of the dc bus bar can be expressed in the following equation [33]–[35]:

$$L_{\text{total}} = 2 \cdot (L_{\text{self}} - L_M). \tag{4}$$

It can be seen in (4) that the way to design a bus bar with a total inductance as small as possible is to design it with the maximized mutual inductance and is to maximize the overlap area of two conductors. Therefore, the laminated bus bar structure is preferred in the design [33].

The stray inductance of the bus bar will change with frequency as well, due to the skin effect and unintended parasitics. It has been shown that the inductance can be split into two, the internal inductance that changes with frequency, and the external inductance that will be constant [36]. Results from [37] back up this claim, showing the measured inductance up to 5 MHz that asymptotes at high frequencies. The stray inductance acquired in simulations is indicated in Table III. This shows similar behavior, and asymptotes in a similar way.

Now that the bus bar stray inductance is obtained, the maximum voltage spike can be calculated by analyzing the current flow during the turn-OFF transient of the switching devices. Take the inverter topology as an example, when phase A upper switch is being turned OFF, the current flow is analyzed when currents in Phase A and C are positive, whereas it is negative in Phase B. The equivalent circuit is given in Fig. 14. In the figure, it can be seen when T_1 is being turned OFF, the current (i_{a1}) in blue path decreases from i_a to zero while the current (i_{a2}) in green path increases from zero to i_a. Thus there are two current changes causing voltage spike across T_1.

And then, according to [36], [38]–[40], the voltage spike and the voltage across T_1 during turn-OFF transient are calculated in Table IV. The parameters used in calculations are selected based on the peak value of inverter output current, IGBT current fall time during turn-OFF, and the dc-link voltage.

3) Stray Capacitance: The stray capacitance benefits the system by reducing the total impedance of the bus bar and providing a filter for high-frequency noise. Generally, the resistance of a bus bar is small and negligible, thus the total impedance of the bus bar can be expressed by (5). Obviously, to achieve low impedance, the stray capacitance should be designed as large as possible while the stray inductance is minimized [1], [41]:

$$Z = \sqrt{\frac{L}{C}}. \tag{5}$$

The stray capacitance of a laminated bus bar is defined by the geometry of conductors and the thickness of dielectric material between positive and negative conductors, which can be obtained in (6) [42],

$$C = \varepsilon_0 \cdot \varepsilon_r \frac{\omega \cdot l}{d} \tag{6}$$

where, ε_r is relative permittivity.

Based on the expression above, the maximum capacitance can be achieved by enlarging the area of one conductor overlapping the other and reducing d; nevertheless, the self-inductance is proportional to l. Thus, to maximize the capacitance without increasing the inductance, thickness of the dielectric material d should be minimized under the condition of satisfying insulation requirement [23], [31]. As per the previous discussion, simulations can be used for a more accurate capacitance estimation for both dc and ac analysis.

An additional benefit of the capacitance is its ability to filter high-frequency noise. EMI is an issue in power electronics due to the several kilo hertz switching frequency of the inverter.

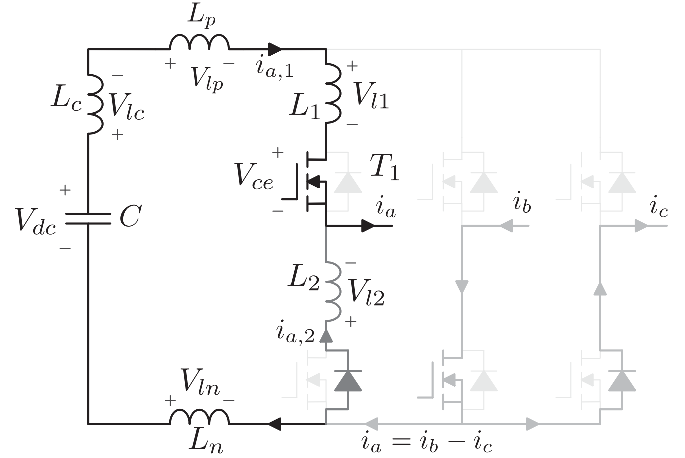

Fig. 14. Current flow in equivalent circuit during the turn-OFF of phase-A upper switch.

TABLE IV
SYSTEM PARAMETERS AND ESTIMATED VOLTAGE SPIKE

Total inductance and estimated voltage spike	Bus bar type				
	A	B	C	D	E
L_c [nH]	5	5	5	15	40
No. of caps	1	2	2	5	5
Total L_c [nH]	5	2.5	2.5	3	8
L_{IGBT} [nH]	20	23	18	14	18
$L_{\text{bus-bar}}$ [nH]	21.38	24.01	11.16	13.90	9.82
ΔI [A]	212	400	600	516	640
Δt [ns]	75	105	160	60	160
V_{dc} [V]	300	600	600	425	300
ΔV [V]	130	188	118	265	143.28
V_{peak} [V]	430	788	718	690	443.28

This switching introduces high-frequency noise into the system. The laminated structure of the bus bar creates a high-frequency capacitor that helps mitigate the noise propagation [8], [43], though this unintended filter is likely not enough to completely remove the issue.

C. High-Frequency Bus Bar Modeling & Analysis

An unavoidable result of fast switching devices is the high-frequency harmonics, termed EMI [44]. The magnitude and propagation of these harmonics depends on the switching device, the switching speed, and the components of the system. The bus bar has a significant effect on this by introducing inductance and capacitance to the main paths of the converter. EMI can be detrimental to various parts of the system, and should be considered as a metic when planning to switch at high frequencies.

The noise produced by the devices can propagate through the electrical system (conducted EMI) via the stray capacitance of the system to grounded components, such as the capacitance between the bus bar and the cold plate. The harmonics can transfer through the ground to susceptible devices imposing a number of negative effects. Typical problems caused are measurement errors in sensors, false control signals, and interference in the gate voltages of switching devices [45]. Excessive noise can deteriorate control, reduce efficiency and cause the system to malfunction. Depending on the use, there may also be regulations [46].

At high frequencies, the harmonics will begin to radiate as well, using the propagation path as an antenna. Reducing EMI in general will reduce the radiated interference, but steps can be taken to further reduce it by adding a shielding layer to the design [44]. It can be used to shield the entire bus bar, or to separate different positive and negative conducting plates.

The source of EMI is the fast current changes causing overvoltages and the resulting oscillations. Through the reduction of the bus bar's inductance, the overvoltage is reduced as well as the EMI [1]. Further, having a low impedance generally reduces the EMI of the system [7]. Minimizing the inductance and increasing the capacitance are some of the main goals of a bus bar, and has been discussed above. Another benefit of the capacitance is the implicit differential mode filter, helping reduce the harmonics between the positive and negative plates.

If necessary, this filter can be expanded on by adding more layers to the bus bar, for example adding a grounded layer between the positive and negative plates to create a common mode filter as well. This has been demonstrated in [8] showing reduced EMI, with only a small increase in size. A benefit of using the bus bar as a filter is the minimal equivalent stray inductance. Any external filter will have significantly more due to the required connection.

Another method to filter the EMI is by adding a lossy material to the surfaces of the conducting plates. This has been shown in [17], where nickel is added to the surface of the copper conductor. High-frequency harmonics, which are pushed to the surface due to the skin effect, will travel through the lossy nickel, attenuating the noise. This can be taken further by adding a magnetic core around the bus bar, which was shown to further reduce the EMI, but the size of the core may interfere with the design layout and reduce the power density. Adding additional layers will also increase the complexity and cost to the bus bar construction, so should only be employed when necessary.

Fig. 15. Actual bus bar setup and 3-D model for measurement and simulation, respectively.

The amount of EMI can be estimated and used to classify the bus bar performance based on regulation values. It can also be useful to simulate the effect of adding an EMI filter, and to evaluate its effectiveness. Simulations are typically done by finding an equivalent circuit for the bus bar and running a circuit simulation [47], [48]. Modern electromagnetic software, such as ANSYS Q3D, gives the ability to find an equivalent circuit from FEA, but other techniques including PEEC [49] and Cauer Networks [50] can be used as well. If the physical bus bar is available, the model can be validated or improved by measuring the impedance spectrum. This can be done by using an impedance analyzer or by employing time domain reflectometry [51].

Modeling these effects can give insight into future problems as well as validate the design. Of course this is most useful while designing the bus bar to allow changes if the EMI is too large, or to help design a filter to mitigate it. If the magnitude of conducted EMI is too large, an external filter may be required. However, this will lead to increase in cost and reduction in power density. By knowing and designing for reduced EMI, the filter size can be reduced, or removed entirely. Keeping the EMI small ensures the system is more robust, accurate, and safe.

IV. TESTING

In order to validate the bus bar designs and analysis, stray inductance and capacitance were measured using a precision impedance analyzer, e.g., Keysight 4294A. As previously stated, the capacitor connections must be short circuited to evaluate the bus bar stray inductance. As shown in Fig. 15, the capacitor terminals were shorted using stainless steel washers. These connections add parasitic inductances to the circuit and by adding the exact same connections and material to the 3-D model the results can be confronted side by side.

The measured and simulated results for stray inductance are presented in Table V for bus bars A, B, and C. Moreover, for the stray capacitance the dc-link capacitor connections were left open while the capacitance was analyzed at the IGBT terminal, and the results are presented on Table VI. Both results present

TABLE V
MEASURED STRAY INDUCTANCES [nH] OF DESIGNED BUS-BARS (L_s: SIMULATION RESULTS; L_m: MEASURED RESULTS)

Frequency [kHz]	Bus bar type					
	A		B		C	
	L_s	L_m	L_s	L_m	L_s	L_m
10	21.38	30.7	24.01	25.4	11.16	46.2
20	20.46	29.9	23.33	23.55	10.68	18.6
30	20.05	26.3	23.04	23.39	10.46	14.3
40	19.79	25.6	22.87	23.25	10.34	11.6
50	19.62	25.3	22.77	22.15	10.27	9.8
60	19.49	25.05	22.7	22.26	10.22	9.6
70	19.39	24.95	22.65	21.5	10.18	9.3
80	19.31	24.8	22.62	22.22	10.16	10.1
90	19.24	24.15	22.59	21.85	10.14	10.5
100	19.19	23.8	22.57	21.92	10.12	11.2

TABLE VI
MEASURED STRAY CAPACITANCES OF DESIGNED BUS-BARS (C_s: SIMULATION RESULTS; C_m: MEASURED RESULTS)

Frequency [kHz]	Bus bar stray capacitance [nF]					
	A		B		C	
	C_s	C_m	C_s	C_m	C_s	C_m
10	4.26	4.443	11.059	10.98	24.005	24.9
20	4.259	4.422	11.056	10.92	23.999	24.78
30	4.257	4.409	11.053	10.89	23.992	24.7
40	4.256	4.399	11.049	10.86	23.984	24.64
50	4.255	4.39	11.047	10.83	23.977	24.6
60	4.254	4.383	11.044	10.82	23.97	24.55
70	4.253	4.377	11.041	10.80	23.964	24.52
80	4.252	4.371	11.048	10.79	23.958	24.48
90	4.252	4.366	11.036	10.77	23.954	24.46
100	4.251	4.363	11.034	10.75	23.95	24.44

relatively good accuracy, which proves the reliability of 3-D modeling and simulations techniques.

In order to test the current sharing among the dc-link capacitors, bus bar E is selected, which is designed for an inverter with five dc-link capacitors and three IGBT modules. To prevent any of the capacitors being overloaded, the connection holes on the bus bar E are located symmetrically; therefore, the ac current distribution should be balanced and it is validated by experimental results. The experimental setup is shown in Fig. 16.

The ac current on the bus bar circulates between five dc-link capacitors and three IGBT modules, as a result, the experimental verification for ac current distribution can be implemented by examining the currents in each dc-link capacitors. The current in one of the capacitors is shown in Fig. 17(a), while a zoomed in view is shown in Fig. 17(b).

To validate the balanced distribution of ac current on the bus bar E, the capacitor currents are measured under three different connections, seen in Fig. 18, where the dc input terminals were chosen as current injection points.

Using three Rogowski ac current probes, five capacitor currents are measured and presented in Figs. 19–21. The

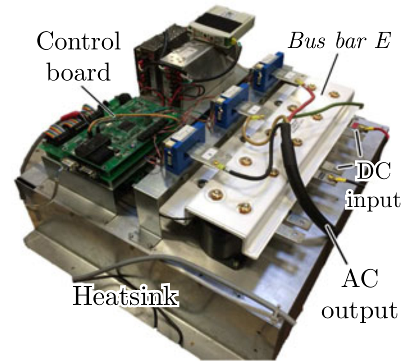

Fig. 16. Bus bar E testing setup.

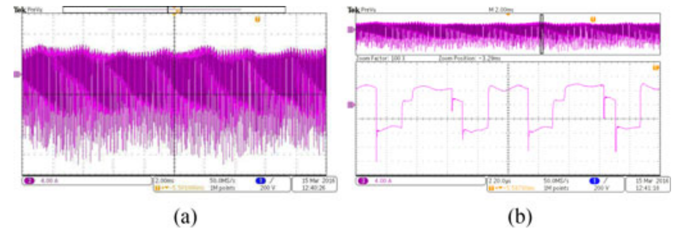

Fig. 17. Current in one dc-link capacitor. (a) Overview. (b) Zoomed view.

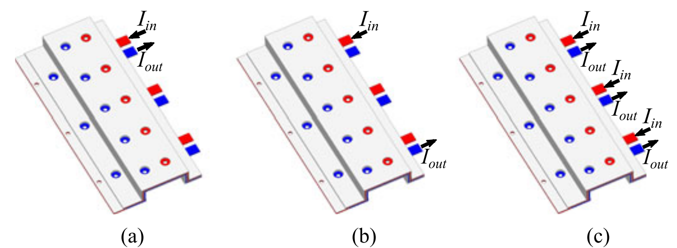

Fig. 18. DC input connection types used in experimental verification for bus bar E. (a) DC connection type I. (b) DC connection type II. (c) DC connection type III.

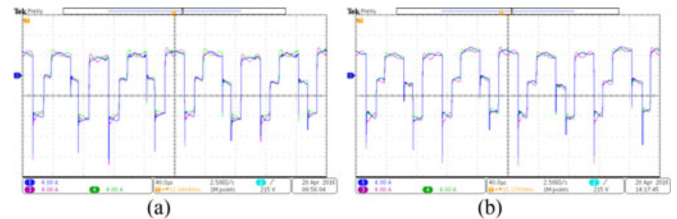

Fig. 19. DC-link capacitor current with connection type I. (a) Currents in capacitor 1, 3, 5. (b) Currents in capacitor 2, 3, 4.

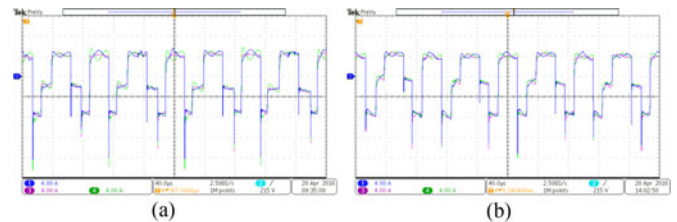

Fig. 20. DC-link capacitor current with connection type II. (a) Currents in capacitor 1, 3, 5. (b) Currents in capacitor 2, 3, 4.

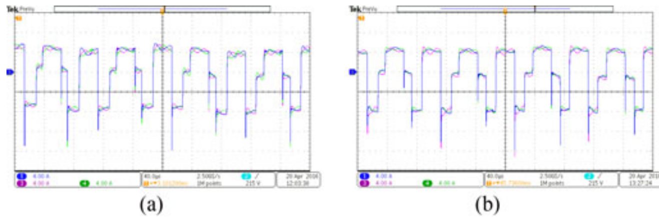

Fig. 21. DC-link capacitor current with connection type III. (a) Currents in capacitor 1, 3, 5. (b) Currents in capacitor 2, 3, 4.

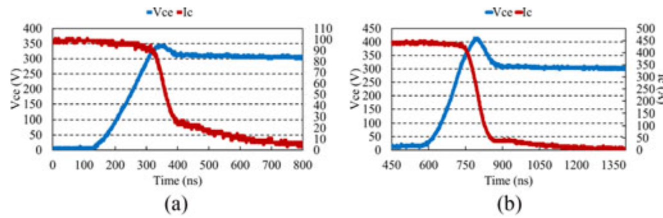

Fig. 22. Experimental data plotted IGBT voltage and current curves during turn-OFF transient. (a) When $I_c = 101$ A. (b) When $I_c = 448.8$ A.

TABLE VII
ESTIMATED AND EXPERIMENTAL MEASURED VOLTAGE SPIKE

Parameters	Case 1		Case 2	
	Calculated	Experimental	Calculated	Experimental
I_c (A)	208	208	306	306
V_{ce} (V)	300	300	300	300
Δt (ns)	115	115	140	140
L_{stray} (nH)	44.34	42.02	44.34	43
V_{spike} (V)	80.2	76	96.9	94
V_{peak} (V)	380.2	376	396.9	394

experimental results show that a bus bar is an effective way to distribute current between passive and active components. Considering the inverter implemented by bus-bar E, the symmetry between capacitors and IGBT modules allows a balanced operation in a three-phase balanced system; therefore, the high-frequency current will also be balanced.

Finally, to verify the evaluated stray inductance in the circuit loop, double pulse test [52], [53] is implemented for bus bar E to capture the IGBT switching transients. The data of voltage spike during turn-OFF transient is obtained experimentally, and it is plotted in Fig. 22. Utilizing the calculation method illustrated in previous section, the estimated voltage spike and experimental measured voltage spike are demonstrated in Table VII. To ensure these results comparable, the estimated result are obtained based on the experimentally measured current and transient time.

As presented by on Table V, the stray inductance of bus bar C is lower than the values of A and B. Bus bar C is expected to have a higher stray inductance because its total length is bigger than the other designs. However, bus bars A and B were designed with rectangular terminals, resulting in a higher stray inductance value. Also, bus bar E has the same IGBT connection and also presents small values for this quantity, as shown in Table III. This represents an important point to be considered during the design process.

V. CONCLUSION

A comprehensive bus bar design analysis is presented in this paper. Based on different application requirements, packages of power modules, and dc-link capacitors, five bus bar layouts are designed. The current density, current distribution, and parasitic parameters of each bus bar are evaluated by simulations and experiments.

1) The current density of each bus bar is under the specification.
2) Based on the given power module locations, the current distribution of dc component is defined by the positions of dc input tabs, while that of ac component is related to where the dc-link capacitors are located. In addition, some intentional obstacles can be created on the bus bar to achieve balanced current sharing.
3) Bus bar resistance and ohmic power loss are obtained. It is proved that this resistance is usually in the order of milliohms and the bus bar total ohmic loss is less than 10 W. Thus, comparing to the converter power loss, the ohmic loss of bus bar is negligible.
4) The bus bar inductance and capacitance are investigated. According to the simulation results and measurements, the predicted values of inductance and capacitance are close to the measurements. The voltage spike caused by the stray inductance is estimated and experimentally validated.

In sum, a bus bar assembly (laminated) will typically have a lower profile and use less space than wires or cables. The lamination process utilizes a thin dielectric film to separate the conductors. This thin and consistent gap results in lower and more consistent stray inductance. Along with inductance, the capacitance of the bus bar is also improved (increased). Especially in inverters, this lower inductance and high capacitance might allow eliminating the snubber capacitors. In terms of thermal management, the increased surface area of flat conductors over wires means improved and more rapid cooling. Power density is also a major requirement where the physical space taken up by a laminated bus bar is typically smaller than wires. In addition, the shape allows for tighter and improved use of the space. Overall, this makes bus bars a clear choice when designing a high power converter.

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Alan Dorneles Callegaro (S'15) received the B.Sc. and M.Sc. degrees in electrical engineering from Federal University of Santa Catarina (UFSC), Florianopolis, Brazil, in 2011 and 2013, respectively. In 2015, he joined the McMaster Automotive Resource Centre, McMaster University, Hamilton, Canada, where he is currently working toward the Ph.D. degree in electrical engineering at the Canada Excellence Research Chair in Hybrid Power train Program.

He was with the Power Electronics Institute, Florianopolis, Brazil, from 2013 to 2014. His research interests include high-power inverters, switched reluctance machines, noise and vibration analysis of traction motors, and motor control.

Jing Guo (S'15) received the B.S., M.S., and Ph.D. degrees in electrical engineering from Beijing Jiao Tong University, Beijing, China, in 2009, Illinois Institute of Technology (IIT), Chicago, IL, USA, in 2012 and McMaster University, Hamilton, ON, Canada, in 2017, respectively.

She was a Research Assistant at the Electrical and Computer Engineering Department, IIT from October 2012 to December 2012. Currently, she is a post doctoral fellow in the Program of the Canada Excellence Research Chair in Hybrid Powertrain at McMaster Automotive Resource Centre, Hamilton, ON, Canada. Her main research interests include power switch modeling and inverter design.

Michael Eull (S'12) photographs and biographies not available at the time of publication.

Benjamin Danen (S'17) received the Bachelor's of Engineering and Master's of Engineering in electrical engineering from McMaster University, Hamilton, ON, Canada, in 2014 and 2016, respectively.

He joined MARC in September 2014 as a Research Assistant for the Canada Excellence Research Chair in Hybrid Powertrain Program, where he currently serves as a Research Engineer. His areas of research include motor control, system modeling and power electronics.

Jason Gibson received the Associates degrees in engineering, the Bachelor's degree in business administration, and the Executive Master's degree in business administration. He recently received the Executive MBA degree in Business Administration and Management from Rochester Institute of Technology (RIT).

He is shifting his professional focus to Product Management and executive leadership. He has 20 years of experience in custom engineered product design in technologies ranging from bus bars, forgings, plastic injection molding, solenoids, and valves.

Matthias Preindl (S'12–M'15) received the B.Sc. degree in electrical engineering (*summa cum laude*) from the University of Padua, Padua, Italy, the M.Sc. degree in electrical engineering and information technology from ETH Zurich, Zurich, Switzerland, and the Ph.D. degree in energy engineering from the University of Padua, in 2008, 2010, and 2014, respectively.

He was an R&D Engineer of power electronics and drives at Leitwind AG, Sterzing, Italy (2010–2012), a Postdoctoral Research Associate with the McMaster Institute for Automotive Research and Technology, McMaster University, Hamilton, ON, Canada (2014–2015), and a Sessional Professor in the Department of Electrical and Computer Engineering, McMaster University (2015). He is currently an Assistant Professor in the Department of Electrical Engineering, Columbia University in the City of New York, NY, USA.

Dr. Preindl received the Career Award of the Futura Foundation in South Tyrol, Italy, and the CAREER Award of the US National Science Foundation in 2016 and 2017, respectively.

Berker Bilgin (S'09–M'12–SM'16) received the Ph.D. degree in electrical engineering from Illinois Institute of Technology, Chicago, IL, USA. He is currently working toward the MBA degree at the DeGroote School of Business, McMaster University.

He is the Research Program Manager in Canada Excellence Research Chair in Hybrid Powertrain Program in McMaster Institute for Automotive Research and Technology, McMaster University, Hamilton, ON, Canada. He is managing many multidisciplinary projects on the design of electric machines, power electronics, electric motor drives, and electrified powertrains.

Dr. Bilgin was the General Chair of the 2016 IEEE Transportation Electrification Conference and Expo.

Ali Emadi (S'98–M'00–SM'03–F'13) received the B.S. and M.S. degrees in electrical engineering (highest distinction) from Sharif University of Technology, Tehran, Iran, in 1995 and 1997, respectively, and the Ph.D. degree in electrical engineering from Texas A&M University, College Station, TX, USA, in 2000.

He is the Canada Excellence Research Chair in Hybrid Powertrain, McMaster University, Hamilton, ON, Canada. Before joining McMaster University, he was the Harris Perlstein Endowed Chair Professor of engineering and the Director of the Electric Power and Power Electronics Center and Grainger Laboratories, Illinois Institute of Technology in Chicago, IL, USA, where he established research and teaching facilities as well as courses in power electronics, motor drives, and vehicular power systems. He was the Founder, Chairman, and President of Hybrid Electric Vehicle Technologies, Inc., a university spin-off company of Illinois Tech. He is the principal author/coauthor of more than 400 journal and conference papers as well as several books including *Vehicular Electric Power Systems* (2003), *Energy Efficient Electric Motors* (2004), *Uninterruptible Power Supplies and Active Filters* (2004), *Modern Electric, Hybrid Electric*, and *Fuel Cell Vehicles* (2nd ed, 2009), and *Integrated Power Electronic Converters and Digital Control* (2009). He is also the editor of the *Handbook of Automotive Power Electronics and Motor Drives* (2005) and *Advanced Electric Drive Vehicles* (2014).

Dr. Emadi was the Inaugural General Chair of the 2012 IEEE Transportation Electrification Conference and Expo and has chaired several IEEE and SAE conferences in the areas of vehicle power and propulsion. He is the founding Editor-in-Chief of the IEEE TRANSACTIONS ON TRANSPORTATION ELECTRIFICATION. He received numerous awards and recognitions. He was the advisor for the Formula Hybrid Teams at Illinois Tech and McMaster University, which received the GM Best Engineered Hybrid System Award at the 2010, 2013, and 2015 competitions.